LOW-POWER RF DESIGN:
SELECTIVE POWER-GATED ADDRESS DECODER

By

CHIANG CHIA YEONG

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DECLARATION OF ORIGINALITY

I declare that this report entitled "**SELECTIVE POWER-GATED ADDRESS DECODER**" is my own work except as cited in the references. The report has not been accepted for any degree and is not being submitted concurrently in candidature for any degree or other award.

Signature: _____

Name: Chiang Chia Yeong

Date: 7th April 2014

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ABSTRACTS

A register file is a paramount part in a central processing unit (CPU) design. It has a similar function with SRAM except that register file is located in processors' core. Register file ought to have a smaller size than SRAM and needs multi-ports to serve several function unit in processors simultaneously and rapidly. Power consumption of a CPU increase simultaneously which cause IC manufacturers taking it as consideration when designing a CPU. In this project, low power register file through selective-power-gated address decoder is being developed. On top of that, low power selective power-gated and drowsy mode memory array and low power selective power-gated domino multiplexer have to be develop to synchronize with address decoder in this project to implement a low power register file. By implementing power-gated technique and valid bit in address decoder, the overall system still can operate while most parts of the circuit is power-down which mean that minimum power consumed. By reducing the power consumption of the register file, the overall power consumption of CPU will also reduce which will helps in handheld and portable devices with CPU inside to prolongs the usable time.

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Chapter 1: Introduction

1.1 Project Background

In every central processing unit (CPU) there is an array of processor registers, register file. A register file is constructed with the combination of address decoder, SRAM cells and domino multiplexer. Register file must be fast to work in high speed for high performance superscalar processors to execute multiple parallel instructions. Modern integrated circuit-based register files are designed by using fast static RAMs with multiple ports. Central processing unit (CPU) can be found in high technology products such as computer, mobile devices, tablet and so on which is important in our daily life as nowadays people cannot live without it.

As for the technology trends now moving toward hand-held and portable devices, how long will the devices last is taking into consideration. Nowadays, the processor that available in the market already achieve high level of performance which cause high power consumption. This kind of processor is not suitable for a hand-held device. There is a need to come out with processor with low power consumption. Some performance trade off that consumers do not really realize when using it for better power consumption when designing a CPU.

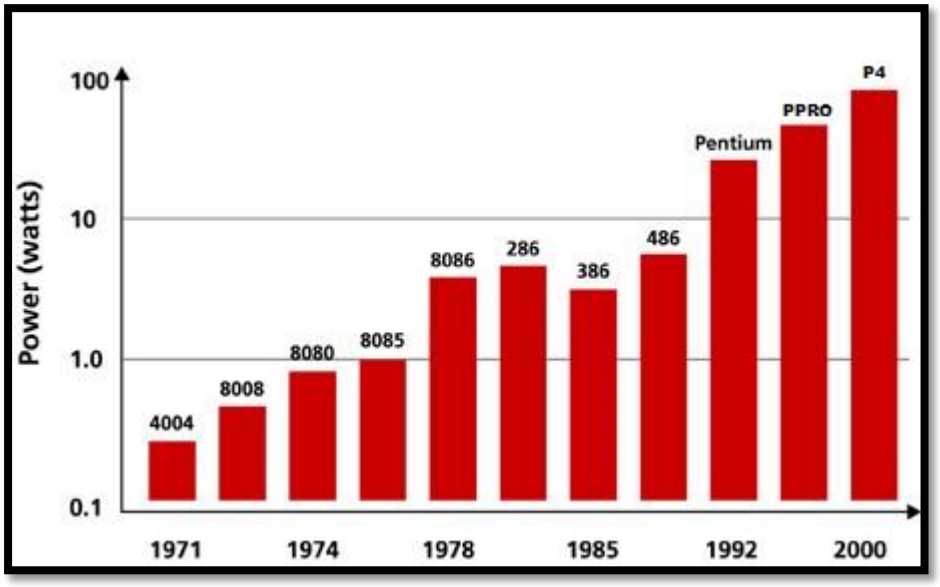


Figure 1 Power Trend for Intel processor. Figure adapted from reference [12]

Figure 1 above shows that the power trend of Intel processor from year 1971 to year 2000. The power consumption of CPU increase simultaneously. Power consumption has become a big problem for almost all IC manufacturers of mobile or hand-held devices. Intel is starting to focus on power consumption and to overcome this issue. For example, Intel 1st Generation Intel Core i7 (Nehalem) has a TDP (Thermal Design Power) of 130W compare with the latest Intel processor, Intel 4th Generation Intel Core i7 (Haswell) which only has a TDP of 75W. By comparing this two processor, Intel is doing a good job in reducing the power consumption as the power consumed was reduced almost 40%.

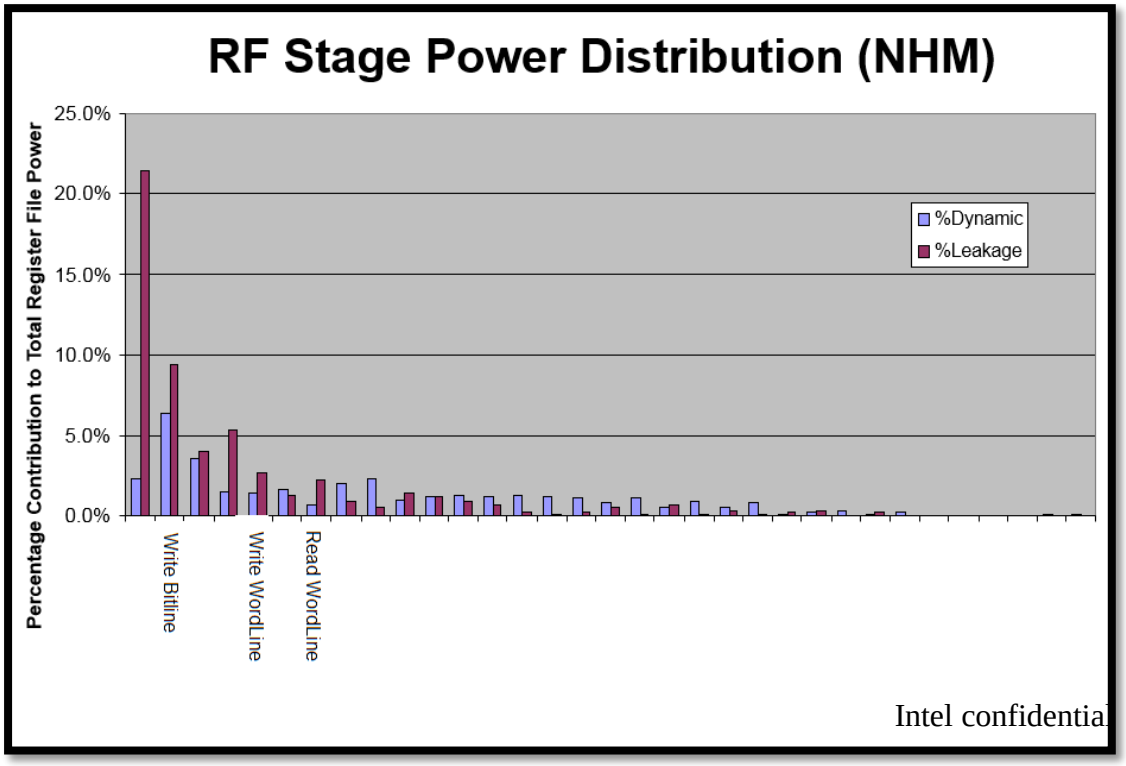


Figure 2 RF stage power distribution

In fact, reduction of power consumption has becoming first consideration while designing a CPU. For example, Intel's register file consuming about 27% of overall power in CPU. In the register file, address decoder has the highest leakage power in terms of Write Bitline, Write WordLine and Read Wordline which is show in Figure 2. Therefore in this project, power reduction of the address decoder will be focused. A low power methodology is proposed for the address decoder in register file which is Selective Power-Gated Decoder.

1.2 Problem Statements

As for now, the current CPU available in market are designed to be power on every single parts inside the CPU which cause to higher power consumption. During normal operation of CPU, usually only small parts of circuit being used consistently. However, the current design of address decoder in register file used in conventional processor turn on the entire address decoder without caring is the block is in used or not. This something like a global switch, when u power-on the whole decoder is turned on, when u power-down the whole decoder is turned off.

By turning on the whole decoder not only consume a lot of power, leakage power also will be produced. Although when particular block is not in used, the transistors is in turn "off" state but this will also cause leakage power due to sub-threshold current flows from V_{DD} to V_{SS}. Therefore, existing design causes a lot of power dissipation because only a certain block is used during operation while other block are all in stand-by mode.

Lastly, usually set of data are being arranged in the same index call a block. After accessed certain data and move onto access neighbouring data, then only decoder power-on the required entry which slow down the performance as delay in power-up the required memory cell.

1.3 Project Scope and Objectives

1.3.1 Project Objectives

The main objective of this project is to study and verify on the power efficiency of address decoder used in register file in CPU micro-architecture. A few designs had been proposed to reduce the power consumption. The outcomes can be seen by comparing the amount of power reduced by proposed designs with conventional address decoder design.

The first objective of this project is to study and compare the static-power for address decoder in register file. Static-power is known as leakage power which is the power that produced when current flows that occurs regardless of voltage transitions (switching) and mostly are from sub-threshold current of turn off transistors. In order to full fill this objective, selective power-gated address decoder is proposed.

The second objective is to examine and reduce the leakage power of address decoder during operation through block-based power-gating. This is to study the amount of power reduction can be achieved through block-based power-gating based on the data-validity of the associated memory block. The related block is power-down when the block doesn't content valid data.

The last objective is to study the power-up delay penalty by using forward-addressing and examining the efficiency of delay reduction of address decoder. This is to study the amount of delay can be reduced when an on-request entry is being power-up concurrently with the next address. This is based on the Principle of Spatial Locality that when a data is being access, the neighbouring data is likely to be access next/soon.

1.3.2 Project Scope

This project is being undertaken to reduce the power consumption of address decoder used in conventional CPU micro-architecture. A Low-Power Register File Design, Selective power-gated decoder is proposed overcomes high power consumption issue. Several development of address decoder are designed in this project.

1. Static-power reduction comparison for address decoder in register file with two different power-gated schemes which are multilayer transistors and by using logic gate.
2. On operation static-power reduction for address decoder in register file through block-based power-gating. Implement of valid bit in the address decoder to check the data-validity so to power-down the related block which do not have valid data being written into memory cell.
3. Power-up delay penalty reduction using forward-addressing. By some modification of existing address decoder used in Intel, when an entry is required, the next entry (entry+1) is also power-up so that when the next entry is being called, delay can be reduced.

At the end of this project, full schematic design of large-scale address decoder and detailed power analysis of different type of proposed design and existing design will be delivered.

1.4 Innovations / Contributions

The main contribution of this project is to study and verify on the power efficiency of register file's address decoder. In order to provide more convenience products such as hand-held devices which provides high performance and low power consumption, power reduction had been taken in as an aspect that designer should take care of. Hence, by reducing the power consumption of address decoder will directly affect the overall power consumption of CPU as register file taken up to 27% of the whole CPU.

Besides, the implement of selective power-gated address decoder is study and compare with conventional address decoder to verify the efficiency of power reduction of proposed design. Selective power-gated address decoder is believe to reduce the power consumption as the power-gated address decoder with valid bit detection which will only turn on particular block that contain valid data so that the system still can operate while most parts of the circuit is power-down.

Furthermore, this project also implement forward-addressing in the address decoder to shorten the wake up delay. This implementation could be useful because block that had been power-down can wake up faster compare to existing address decoder. This is because when an entry is being called, a signal is send to the next entry to turn on the particular entry. So we can actually save up a lot of time delay from this concept.

1.5 Methods/Technology Involved

There are few technologies that involved throughout this project in order to complete this project. First, the semiconductor C5 mocmos 300nm design environment is one of the technologies. In this project the modification and implementation of address decoder in register file is based on C5 mocmos 300nm design environment. Besides that, comparison of outcomes will be made with existing conventional design as bench-mark.

Other than that, Electric VLSI Design System is also involved in this project. This tool used to draw the schematics of proposed design, selective power-gated address decoder and implementation of forward addressing in transistor level. Furthermore, LTspice IV, a SPICE simulator is also used in this project. This tool is used to simulate waveform for voltage, current, timing delay and power consumption of the schematic.

Chapter 2: Article Review

2.1 Low Power Techniques

Power has been a second concern in chip design following first order issues such as cost, area and timing. Today, most of the processor design, the power budget is one of the most important design goals for the project. Power management had comes in in this point. During designing a processor, manage power in all modes of operation is taking into consideration. Dynamic power is manage during device operation while static power is manage during standby. This purpose is to maintain device performance while minimizing power consumption.

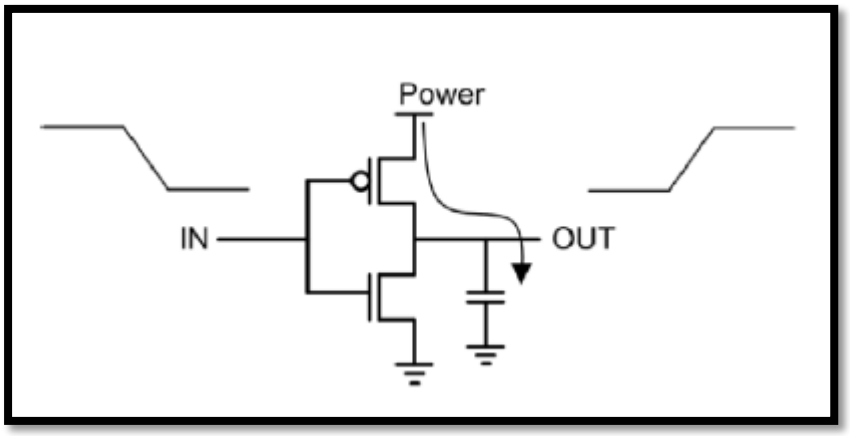


Figure 3 Dynamic Power

Dynamic power is the power consumed when the device is active which mean that when signal are changing values. The primary source of dynamic power consumption is switching point. By referring to Figure 3, when the output is from ‘0’ to ‘1’, capacitive load of PMOS is charged while the output from ‘1’ to ‘0’, capacitive load of NMOS is discharged which cause the dynamic power. Besides switching power, internal power also contributes to dynamic power. Internal power is the power that consumed by the cell when an input changes, but output does not change.

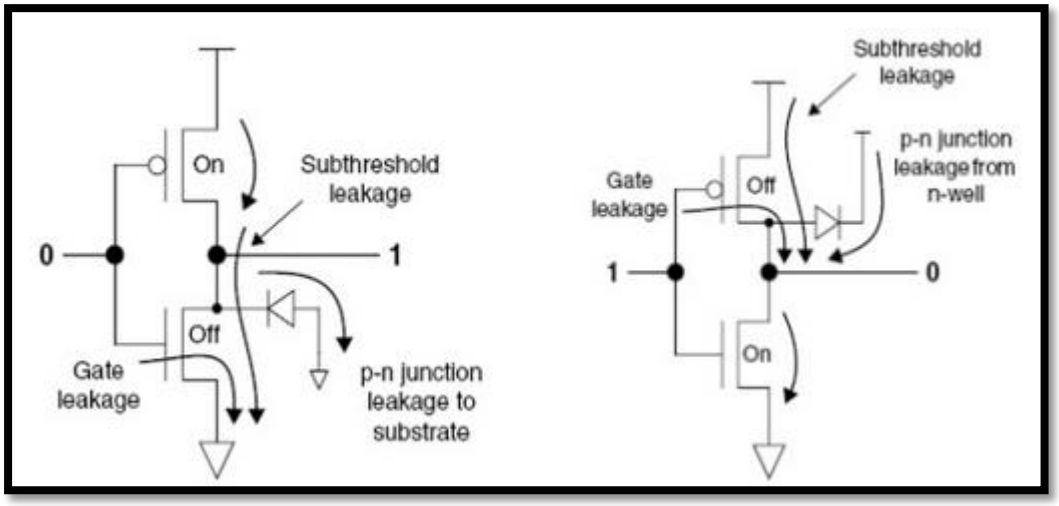


Figure 4 Static Power. Figure adapted from reference [14]

Static power is also known as leakage power is the power consumed when the device is powered up but no signals are changing value. Static power consumption is due to leakage. Refer to Figure 4, there are few major sources of leakage currents in a CMOS gate.

- Sub-threshold Leakage is the current that always flow from source to drain of a transistor operating in weak inversion region (Vgs close to Vth).
- Gate Leakage is the current which high electric field flows across the gate through a thin gate oxide to substrate due to gate oxide tunnelling.
- Gate Induced Drain Leakage (GIDL) caused by high field effect in the drain junction of MOS transistors. GIDL increases with higher supply voltage, thinner oxide and increasing in Vdb and Vdg.
- Reverse Bias Junction Leakage is caused by minority carrier drift and generation of electron and hole pairs in depletion regions.

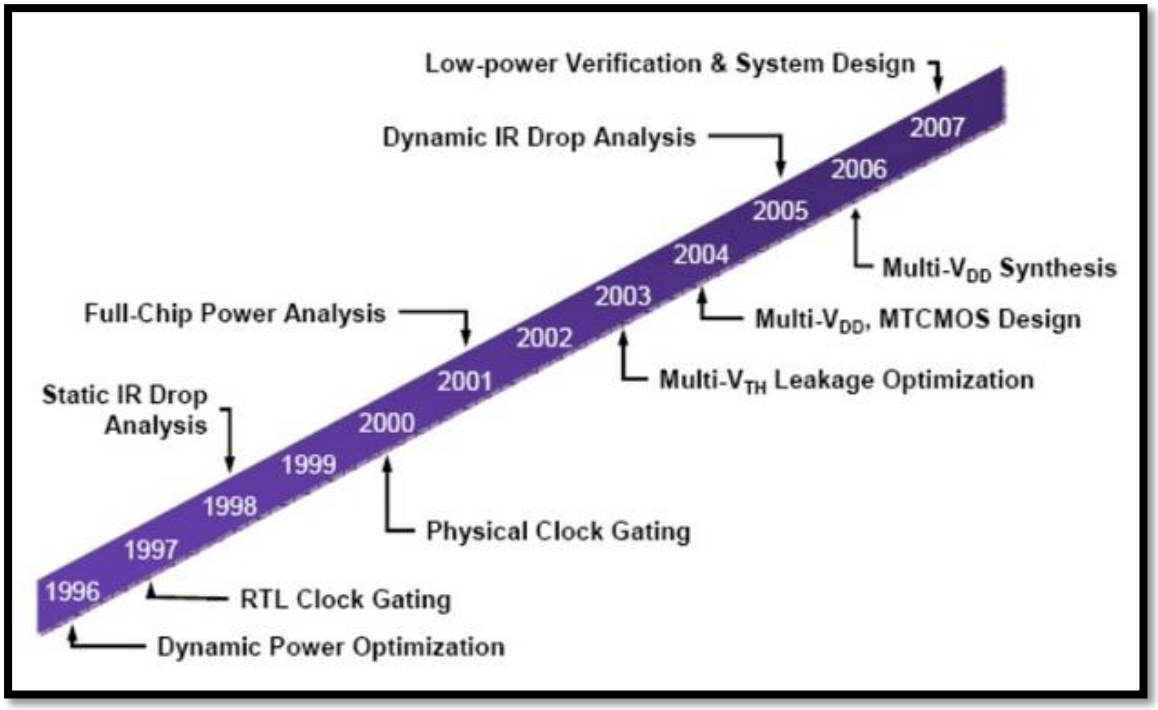


Figure 5 Evolution of low power techniques. Figure adapted from reference [14]

Refer to Figure 5 there are a lot ways to resolve the power consumption issues. From the Figure can see that low power techniques moving from dynamic power optimization to clock gating and slowly to Multi-V_{DD} design. Those methods had been proven the efficiency in reducing power consumption.

2.1.1 Clock Gating

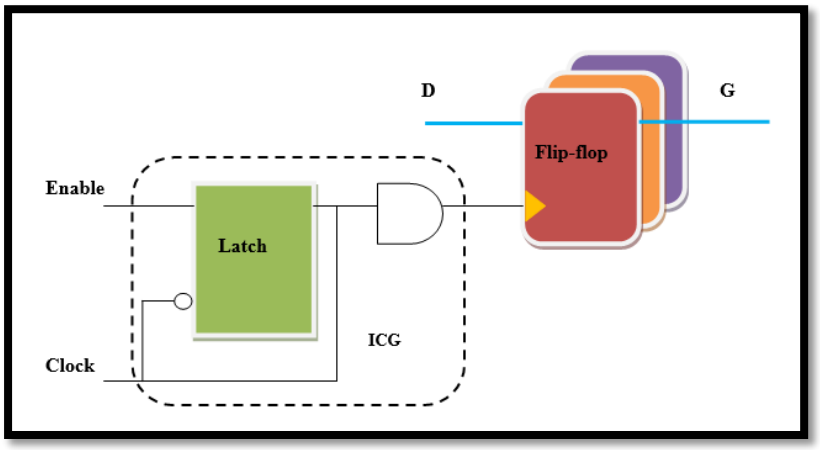


Figure 6 Clock Gating

In a processor chip, clock tree consume more than 50% of dynamic power. This power consumed by combinatorial logic whose values are changing on each clock edge. The most common way to reduce this power is to turn off the clock when they are not required which is basically named as clock gating. Clock gating mean that gate the clocks of flip-flop which have common enable signal. This clock gating logic is generally in the form of integrated clock gating (ICG) cells.

There are two types of clock gating styles available. Latch free clock gating is implement by using a simple AND or OR gate. This type of clock gating very less being used because glitches are unavoidable. Another type is Latch-Based clock gating which adds a level-sensitive latch on the design. It holds the enable signal from the active edge of the clock until the falling edge of clock.

2.1.2 Multi V_{DD}

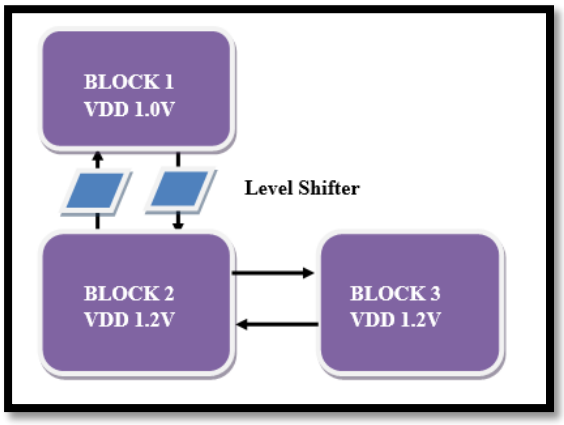


Figure 7 Multi V_{DD}

Dynamic power is directly proportional to power V_{DD}. Hence reducing power significantly improves the power performance. At the same time gate delay due to the decreased of voltage in the design. High voltage is applied to timing critical path to meet the performance and the rest of the blocks runs in low voltage so that the overall system performance is maintained. Areas with different voltages must be designed physically separate from one another and a cell called level shifter is inserted to enable the interface signals between one block and another block to convert the signal level.

Multi voltage design strategies can be classified as follows:

- Static Voltage Scaling (SVS) mean that different but fixed voltage is applied to different blocks or subsystems of the design.
- Multi-level Voltage Scaling (MVS) mean that the block or subsystem of design is switched between two or more voltage levels.

- Dynamic Voltage and Frequency Scaling (DVFS) mean that voltage and frequency is dynamically varied as per the different working modes of the design so to achieve power efficiency.
- Adaptive Voltage Scaling (AVS) mean that voltage is controlled using a control loop.

2.2 Power Gating

Power gating is a technology that has been gaining popularity in recent years. It reduces the leak current by shutting off the flow of current to blocks of circuit that are not currently in use. Power gating will affect design architecture more than clock gating. It increases time delays, as power gated modes have to be safely entered and exited.

The most basic form of power gating control is by implement an externally switched power supply to achieve long term leakage power reduction. This approach takes longest time and requires more energy to restore the power to a gated block. To shut off the block for small intervals of time, internal power gating can be a better solution.

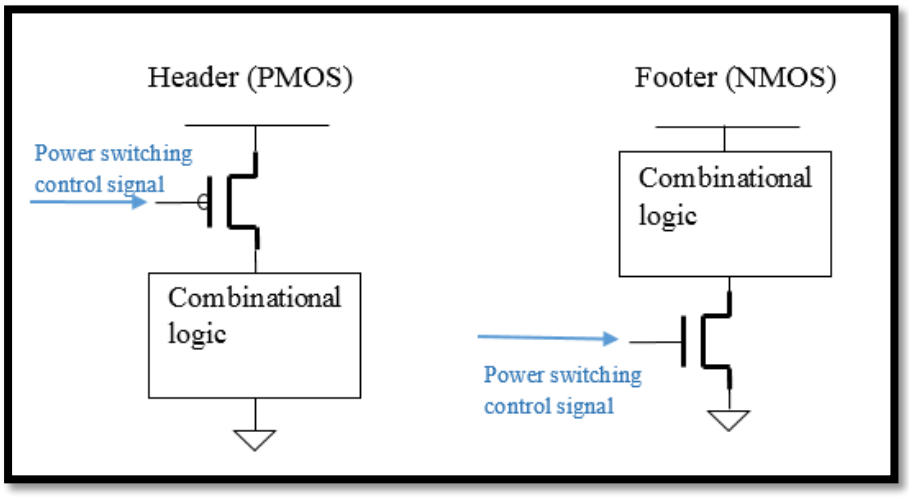


Figure 8 Header and Footer switch

Power gating uses PMOS as header switches to shut off power supply to parts of a design in standby or sleep mode while NMOS as footer switches used as sleep transistors. The sleep transistors is turn off when the block is in idle mode, the circuit is disconnected from VDD/Vss which will help in reduction of leakage power.

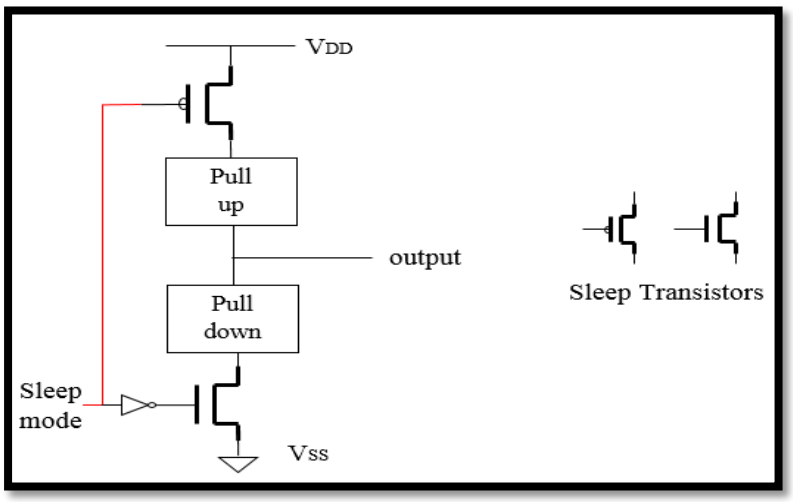


Figure 9 Power-Gated Combinational Circuits

By referring to Figure 9, if sleep mode = '0', the sleep transistors will turn on and the circuit is working normally which mean the sleep mode is being disabled. While the sleep mode is enabled, sleep mode = '1', the sleep transistors will turn off which will disconnected the circuit from VDD and Vss thus reduce the leakage power.

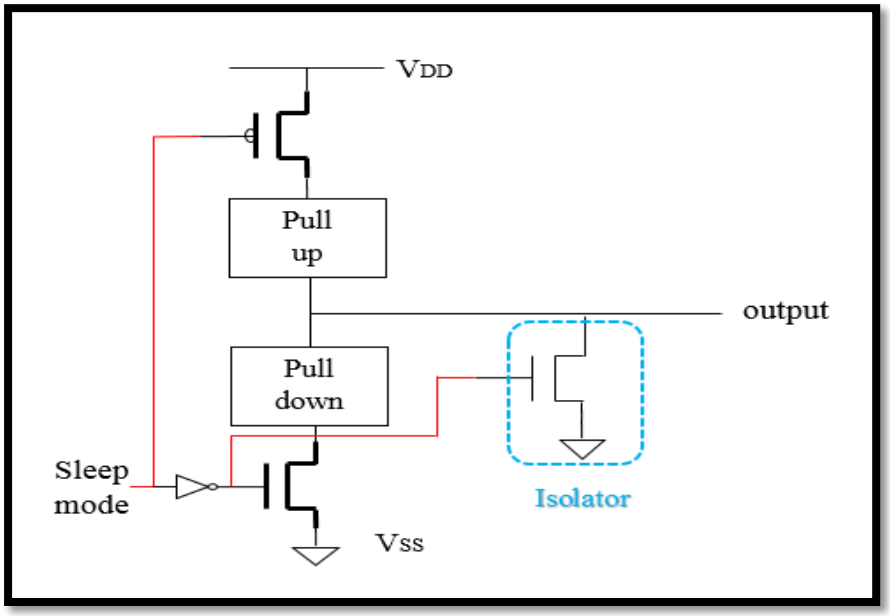


Figure 10 Isolator

When the block is power down, the output of the power-gated block are concern in this case, since they can cause electrical or functional problems in other power-up block. So to solve this problem, an isolator is added in the power-gated circuit. When sleep mode is enable, the isolator will also activate and pull down the output of power-gated block to ground which is shown in Figure 10.

As mentioned in above, power gating is designed by adding PMOS and NMOS to the particular block as a switch. So here comes the consideration that which type of transistor should be used in power gating circuit as there are several type of transistors available in the industry. Basically there are three major type of transistors which is high-speed transistor, nominal transistor and low-leakage transistor.

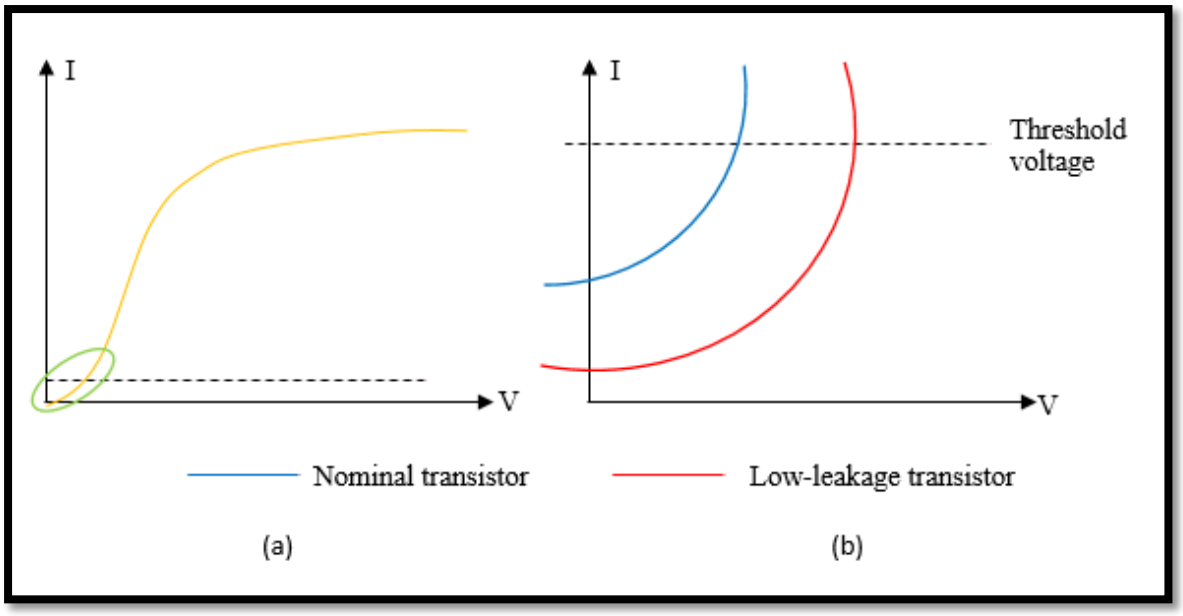


Figure 11 (a) transistor voltage against current (b) zoom in of cut-off region

Threshold voltage of a transistor will affect the speed and power dissipation of the circuit. By referring to Figure 11 (b), the threshold voltage of a transistor will affect the leakage current. The higher the threshold voltage, the lower the leakage current. Therefore, decrement of threshold voltage will cause in increasing of power dissipation.

High-speed transistor provided fastest switching speed but in the same time it also contributed highest leakage power. High speed transistor is used in critical timing path circuits which required high speed to maintain the performance.

Furthermore, low-leakage transistor have lowest leakage power as can know from the name of the transistor. The trade-off is it is the slowest transistor among the others transistor in term of switching speed. Low-leakage transistor are more suitable to use as sleep transistor in power-gating design as power-gating main purpose is to reduce the leakage power.

Lastly, nominal transistor is somehow between high-speed transistor and low-leakage transistor in term of switching speed and leakage power contributed. Nominal transistor is more balance type of transistor which are normally used in general logic gate design. By choosing the right transistor is very important as different threshold voltage will affect in performance and power dissipation.

2.3 SRAM and Register File Architecture

Static Random Access Memory (SRAM) is a type of memory used as the building block of most caches because of its superior performance over other memory structures like Dynamic Random Access Memory (DRAM). The term static differentiates it from DRAM which must be refresh simultaneously. SRAM is still volatile in the sense that data is eventually lost when the memory is power down.

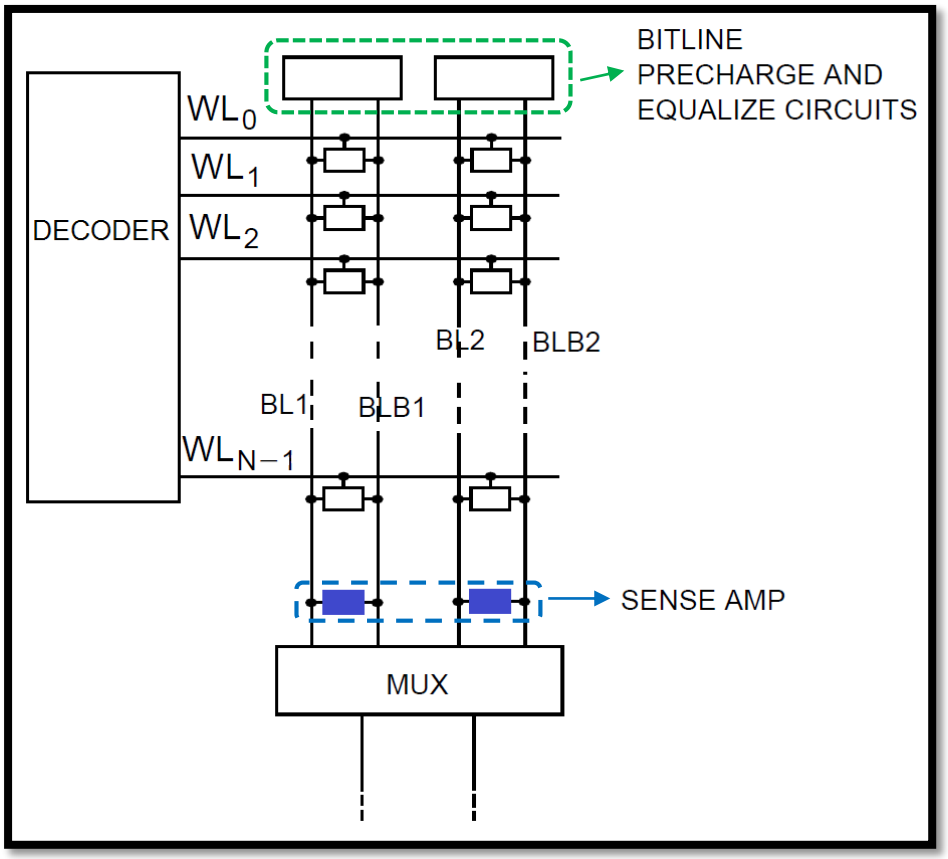


Figure 12 SRAM Architecture

Figure 12 shows a general SRAM which build up from few parts which are row decoder, SRAM array, sense amplifier, pre-charge circuit, equalizer circuit and column multiplexer. All bitlines (BL) are to be precharged to V_{DD} so when one of the wordline (WL) asserted, all the memory cells that connected to this wordline will have their pass transistors enabled.

During a read operation, both of the bitlines are precharged to high. After that the wordline is asserted high. One of the bitlines will pull down by the cell. The bitlines are connected to sense amplifier that recognizes if a logic data is '1' or '0' is stored in the selected elementary cell. Then this sense amplifier then transfers the logic state to the output buffer which is connected to the output pad.

During a write operation, one of the bitline is asserted high while another bitline asserted low. After that, asserted the particular wordline. Data comes in from the bitline. It then moves to the write circuitry. Since the write circuitry drivers are stronger than the back-to-back inverters, the data will forced onto the cell. When the operation is completed, the wordline is deasserted so that the data is keep in the back-to-back inverters for a read cycle.

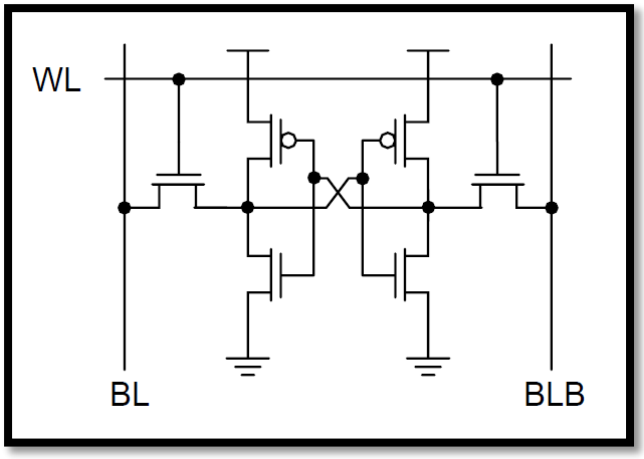


Figure 13 6T SRAM cell. Figure adapted from reference [4]

Figure 13 describes the most basic unit of a SRAM, a single data bit memory is implemented. The SRAM is implemented by 2 back-to-back inverters accessed using two pass transistors. The back-to-back inverters connection creates regenerative feedback that allows it to store a single bit of data. In 6T SRAM cell, there are 2 bitlines which is BL and BLB which carrying the data during read or write operation. In this SRAM cell, there is only one R/W port that can be used for either read or write at a time.

The row decoder is required for a SRAM circuit. Row decoder is actually a normal address decoder with one hot output to active one row of the memory array. The decoder will decode the inputs and will enables the corresponding wordlines to allow memory array to process with read and write operation. When the number of memory address becomes very large, the addresses are usually split into multiple blocks, each of which is decoded separately. More details about address decoder will be discuss in next section.

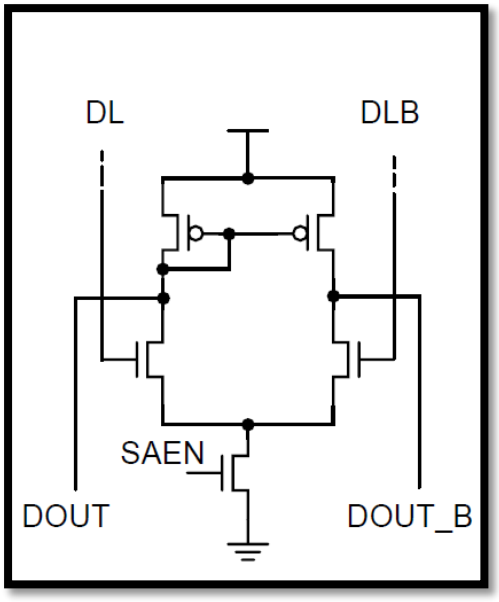


Figure 14 Sense Amplifier. Figure adapted from reference [4]

Sense amplifier is one of part in the read circuitry in SRAM. Sense amplifier is use to sense the logic levels from bitline which represent a data bit ‘1’ or ‘0’ which stored in memory cell, and amplify the small voltage swing to proper logic levels so that the data can be interpreted properly at the output. There is one sense amplifier for each column of memory array.

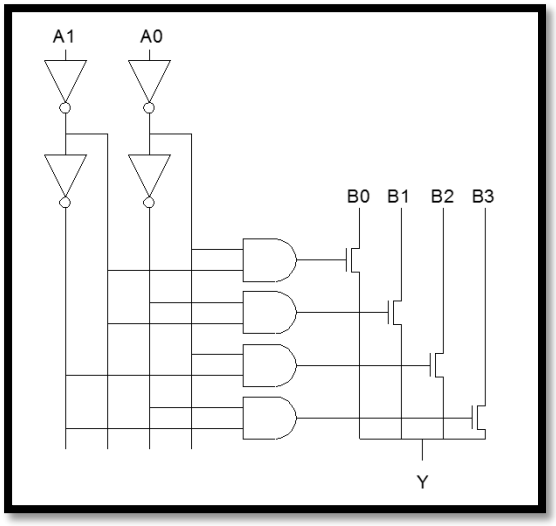


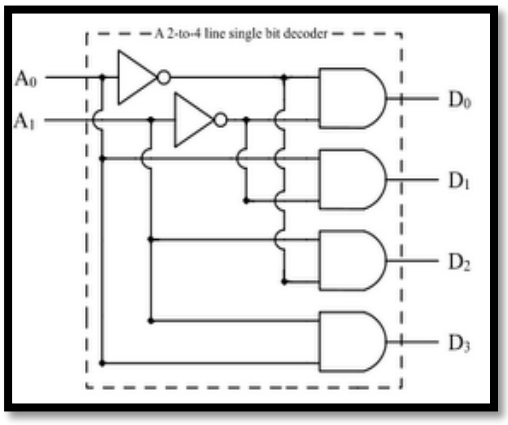
Figure 15 Multiplexer with pass transistors. Figure adapted from reference [4]

There is a need of decoder for column address. A multiplexer is use to select the column for read and write operation on particular column. Circuit that perform read and write on the array are from column circuitry. When write operation, the multiplexer must activated the selected column bitline so that the bitline can drive to ground.

SRAM architecture and register file has similar functionality except that register file have both read and write port and is located inside a processor. SRAM read and write operation through the same port while register has different port for read and write operation. Hence, register file can do serve several operation simultaneously and rapidly.

2.4 Address Decoder Architecture

Address decoder are simply a collection of logic gates which has at least two bits as input to active particular block through selection lines as output. Address decoding is a simple process of receiving address information and providing signals to initiate and perform operation on the addressed location.



A0	A1	D0	D1	D2	D3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Figure 16 2-to-4 Address Decoder

Table 1 Truth table for 2-to-4 decoder

Figure adapted from reference [3]

Address decoder feeding an address value into a binary decoder (n to 2^n) and using the asserted output to active particular memory cells with this address. By referring to Figure 16, the decoder involve a single AND operation on the input address and works together with inverters to come out with one hot activate at the output.

The main concern in address decoder is the large fan-in and fan-out requirements of typical memories due to the decoded address bit number and the amount of cells that to be driven. Which this designs, the address decoder will contributes significantly to the critical path delay and total power dissipation.

One of the techniques used in minimizing fan-in is a method calling predecoding. Predecoding involves using a smaller input address bit decoder as subset of the address. The output of these predecoders are then combined with lower fan-in gates to come out with final address decoder.

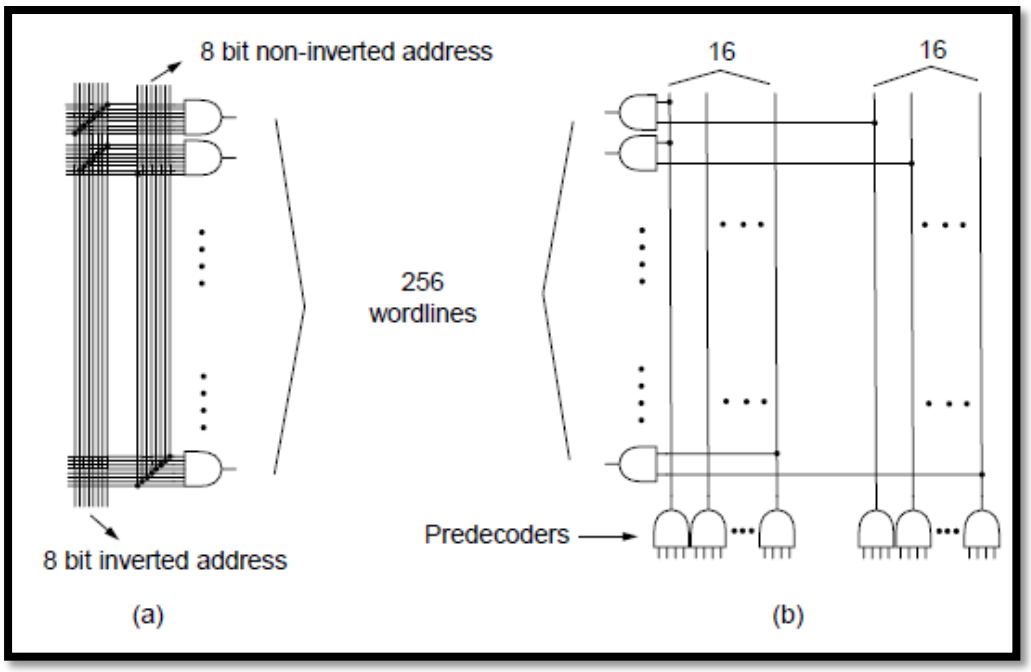


Figure 17 (a) typical 4-to-16 decoder (b) 4-to-16 decoder with predecoders

Figure adapted from reference [4]

Referring to Figure 17(a), an 8-input AND gates is used. These will have higher gate capacitances compared to 2-input AND gates which resulting in larger delays, higher power dissipation and larger area in the layout designs. Looking at Figure 17(b), the 8-bit input is divided into two subsets. 4-input AND gates are used to generate possible combinations and the final wordlines are generated using 2-input AND gates to combine the output from two subsets. With the implementation of predecoders, faster speed, lower power and smaller area circuit can be designed.

Register file practiced in the industry today splits the job of reading and writing the SRAM cells independently. The most significant address bit is used to select between read and write operation. Besides, the output is arranged in alternated sequences which shown in Figure 18 below.

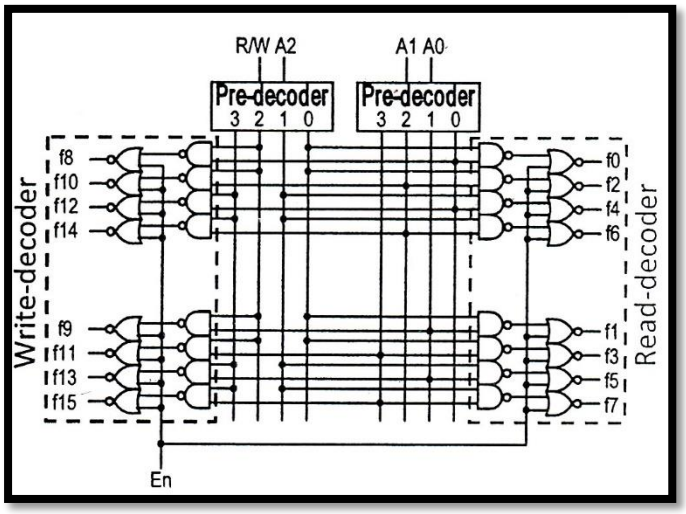


Figure 18 Address decoder with read/write decoder. Figure adapted from reference [17]

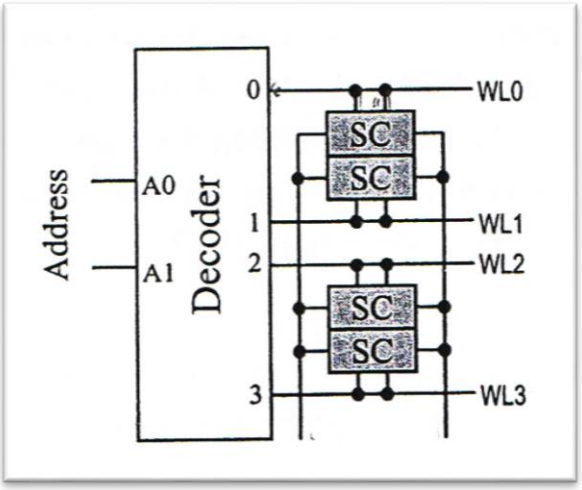


Figure 19 Address decoder used in register file. Figure adapted from reference [17]

To operate the processor, address decoder is needed to power-up the desired address location of memory cells. When address decoder feed in address bit, it will decode and asserted one hot activation signal to the output that connected to the wordlines (WL) of memory cells which will activate the subset of memory cells with associated with this address. When the address bit is being feed, the most significant bit will decided to active the read decoder or the write decoder. When a read process is required, the read decoder will asserted high the read wordlines (RDWL) for the memory cells with associated address. While a write process is operating, the write decoder will asserted high the write wordlines (WRWL) for the memory cells with the address.

By referring to research paper from RWTH Aachen University, Germany, they proposed another low-power address decoder by using tree address decoder. A binary tree address decoder utilizing the back-biasing technique which helps to acquire a set of optimal parameter estimations comprising different capacities. Moreover, the concept of binary tree decoder can be extended to tree decoder with various fan-outs

and depths which will enlarges the set of parameters which are considered in the optimization strategy.

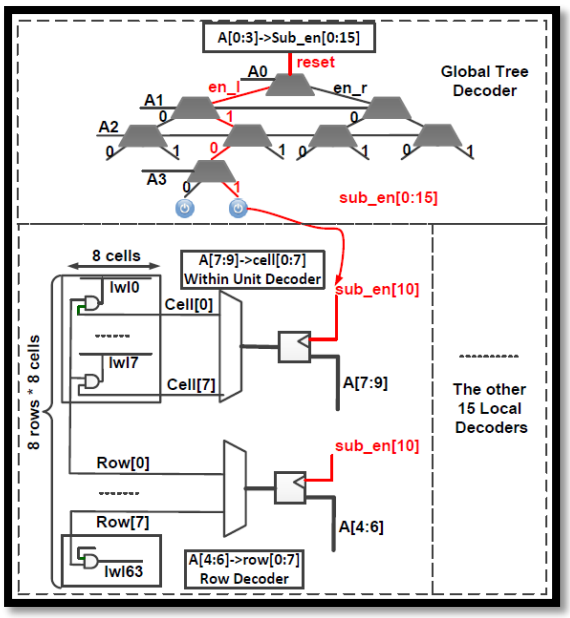


Figure 20 Tree Decoder Structure. Figure adapted from reference [22]

By referring to Figure 20, the address decoding behaves like a depth-first search operation in a binary tree. Each demux unit in the binary tree has two children nodes. One bit address signal and the active high enable signal produce two enable signals for left child and right child in the next level.

The advantages of this decoder are the critical path is proven to be short and the power dissipation is low due to fewer activated transistors. The second advantage is the number of local decoders can be reduced for decreasing area and energy by sharing a local decoder within multi-memory sub-blocks. Last, the optimal depth of the tree decoder can be derived easily according to the presented parameter model without considering the fan-out of each NAND or NOR stage like in the hierarchical decoder.

Chapter 3 Methodology

The purpose of this project is to compare the advantages and weakness of various power gating schemes for address decoder which mentioned earlier and also to examining the efficiency of power reduction when the address decoder is power-gated with several proposed designs compare to existing conventional design. The proposed design are expected to reduce the power consumption of conventional CPU microarchitecture as unused circuits had been power-gated.

Figure 21 shown the circuit design for 48 entries selective power-gated address decoder that had been proposed in this project. Basically this decoder have 2 predecoder, predecoder<0> and predecoder<1>. Predecoder<0> take care of the lower 8 bits. It will only active high one of the input of eight input for of all 6 blocks in the decoder which output a 6 cold. While predecoder<1> will take care of activating one of the 6 cold become 1 cold output.

Referring to Figure 21, only one of the NAND gate in the green colour box will active at once. While the clock is asserted high, the output of the NAND gate will pass through an inverter and will active the particular block. The NAND gate inside the block combining the input signal for predecoder<1> and predecoder<0> which will outcome a 1 cold output.

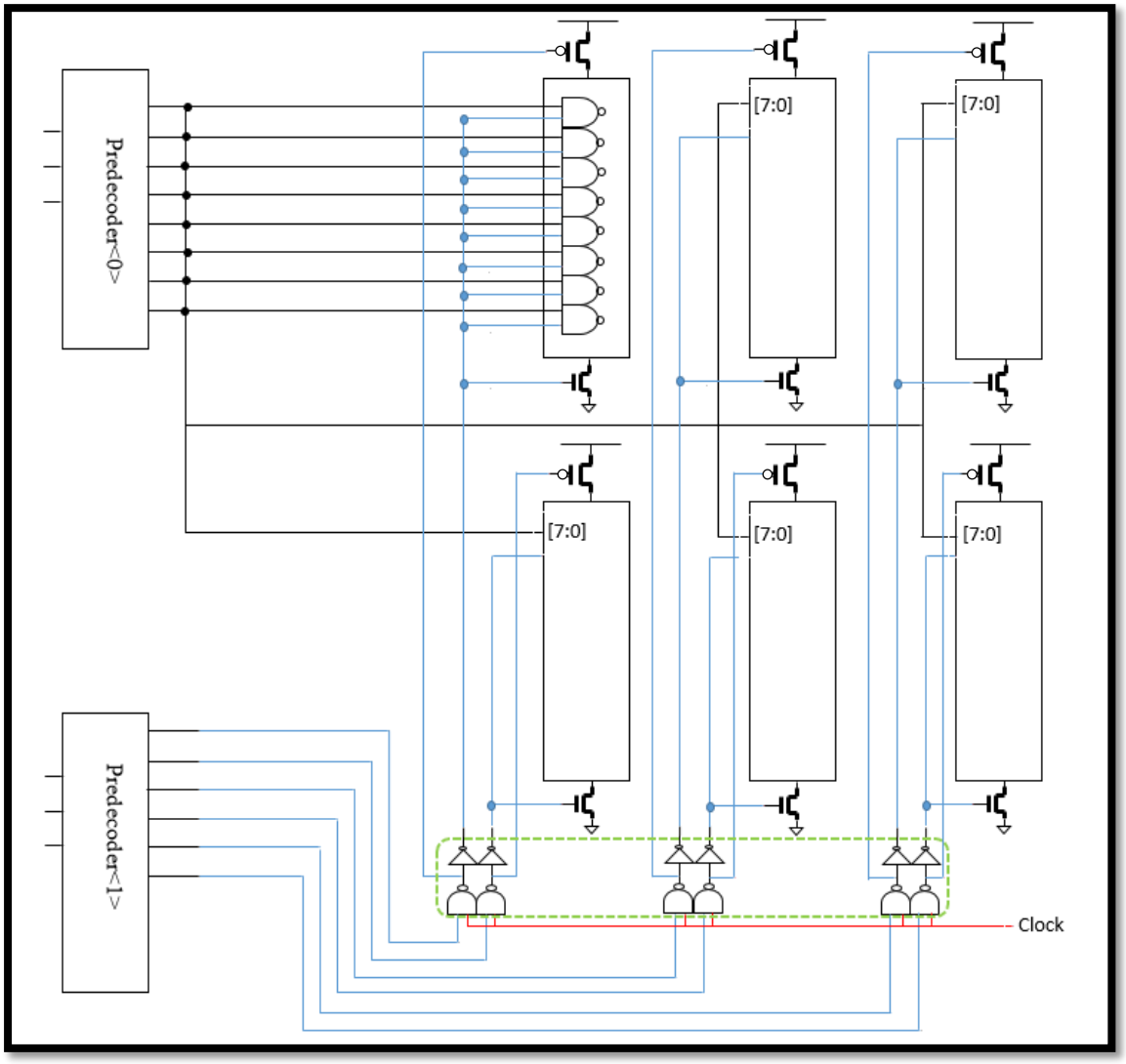


Figure 21 Selective Power-gated Address Decoder

3.1 Valid bit and Power-gate

In previous section mentioned that when implementing power gating in address decoder, power switching control signal acts as the control signal of the sleep transistors which is used to power-up and power-down the header and footer of a circuit. In this project, the proposed design used valid bit as the control signal throughout the whole register file. The valid bit is generated from memory array file and is feedback to address decoder. Memory array only generated one type of valid bit signal to share with domino multiplexer, address decoder and memory array itself.

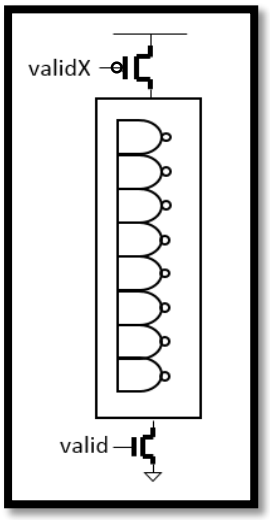
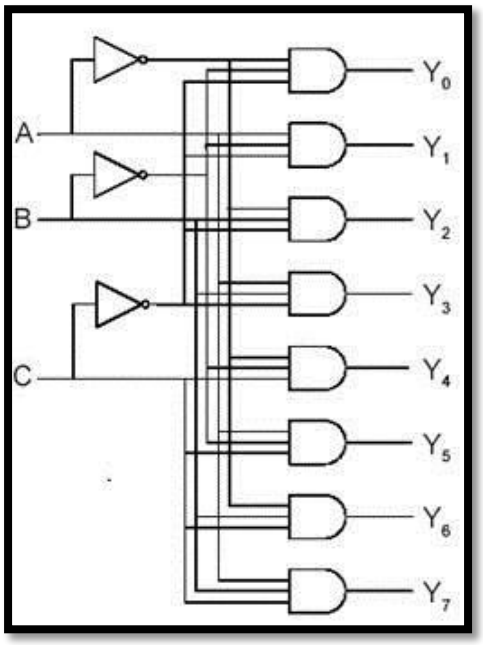


Figure 22 Valid bit

For the proposed design selective power-gated decoder, the PMOS acts a header switch which is control by validX. While NMOS acts a footer switch which control by valid. Other than valid signal, both power gate also control by ck signal which is the output signal from predecoder<1> which is use to select which block to be activated.

3.2 Shared Decoder



C	B	A	output
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Figure 23 3-to-8 Conventional Decoder

Table 2 Truth table for 3-to-8 decoder

Figure adapted from reference [18]

Shared Decoder is the idea of sharing the NMOS pull-downs for the input that having the same state at output. For example, the input C will always be '0' for output 0-4. Therefore they can share their NMOS.

Shared Decoder ideally will be faster than the traditional decoder. Besides it also consumes less power than traditional decoder as it reduced the number of NMOS. By implementing shared decoder in register file will somehow speed up the circuit and the same time reduce the power consumption.

3.3 Power-gating Decoder

In order to improve the power dissipation of address decoder, there are 2 proposed schemes in this project which are multilayers transistors and by using logic gate.

Power-gating decoder mean that the header and footer will be power-down at the same time. In this case, this block will output a high impendence, Z which may cause some functional problem to power-up block. Therefore, an isolator is connected to the circuit to drive the output to ground so that the output of power-down block will be '0' which won't cause any issue to other blocks.

Power-gated the decoder by using logic gate is expected to have shorter wake-up delay while power-gated the decoder by using multilayers transistors design is expected to have lower leakage power. In this project, the result of both method will be examine to see the amount of delay against power consumption.

Design 1 is implement by using multilayers transistor. The first layer is the block based power gated transistor and the second layer is the data validity power-gated transistor. While Design 2 is implement by using NOR logic gate the control signal validx and clkx to control footer power gate. For header power gate, the control signal is by using the NAND gate with valid and clk signal.

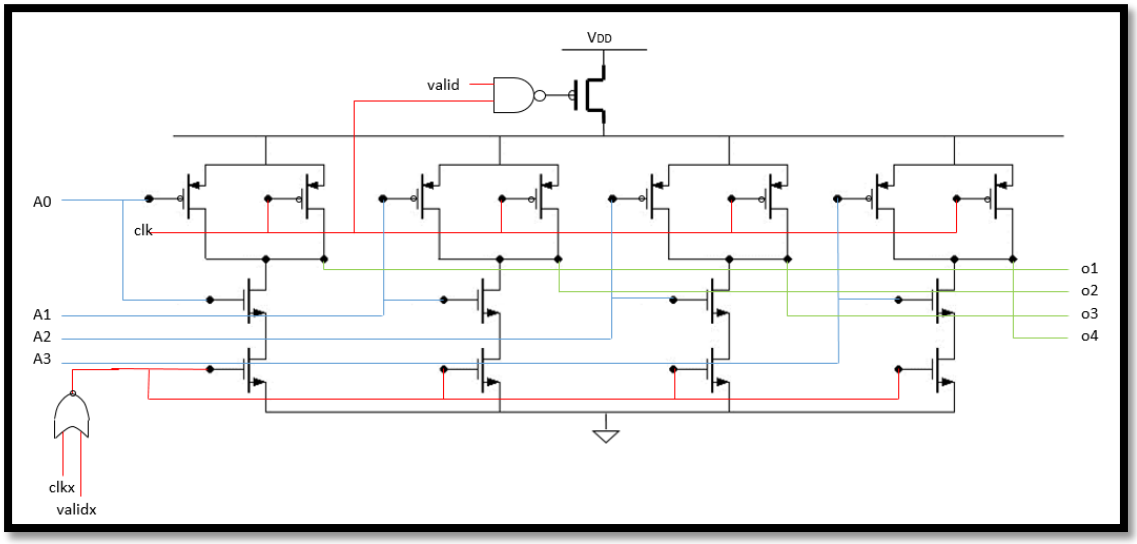


Figure 24 Selective power-gated Address Decoder with NOR and NAND gate

Figure 24 shows a parts of address decoder. Looking at the 4 NAND2 gate in the decoder, when the related entries doesn't contain valid data the footer switch is switched off to reduce leakage. On the other hand, when the V_{DD} is being gated, the potential different of output will drop which will reduce the potential difference between output and V_{SS} and therefore reduce leakage.

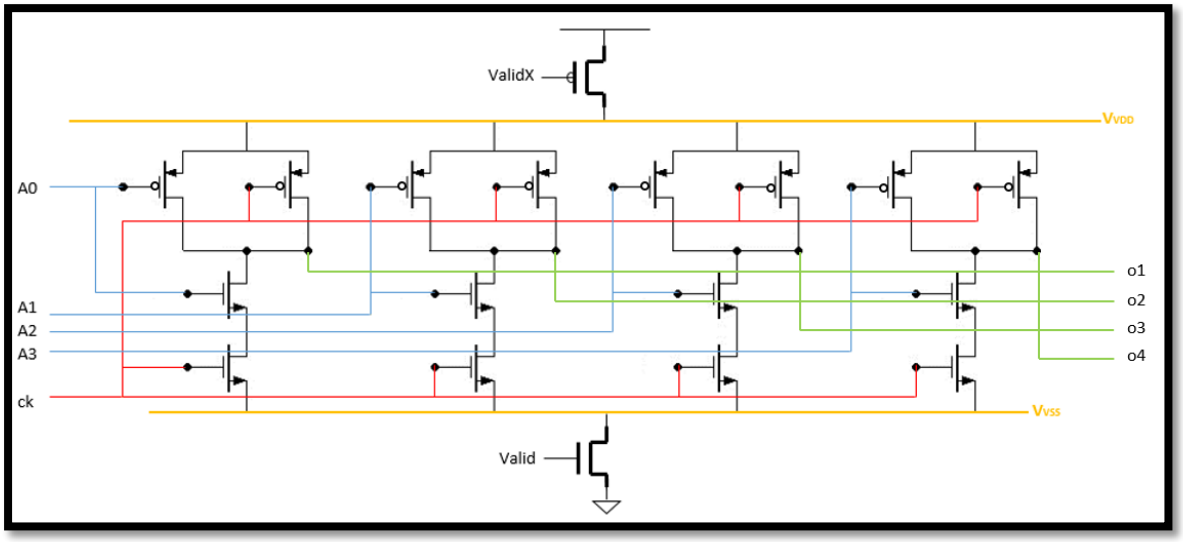


Figure 25 Selective Power-gated Address Decoder with multi-layers transistors

Figure 25 shows the second proposed circuit design for this project. By adding sleep transistors as switch at the header and footer. In the design, there is extra 1 more layer of transistor compare to the previous design that shown in Figure 24. When there are no valid entries in the particular block, the transistor is turn off. When transistor is turn off, it is similar to a resistor which mean that more leakage current will be reduced. When there are related entries which contain valid data, the block is power-up which will turn on the power-gate switch. For header, the VDD will output to VVDD which will supply current to the circuit while footer switch is turn on, VVSS will acts as ground to drive the output.

There will be some trade-off in this design so to reduce the power dissipation. By adding a power-gate in a circuit, it will increase the delay on normal operation especially rise

time, sleep and wake time. Besides, the dynamic power consume when power down and power up will also increase. Comparison will be made with existing conventional design to check on the usability of the proposed design.

The outcomes of this two circuit will be examine to check that which designs is more suitable to use in selective power-gated address decoder. For Figure 24 which design using a NOR and NAND gate is expected to have a high performance speed and for Figure 25 which design using multi-layers transistors is expected to have lower leakage power due to the current have to pass through a few layers of transistors.

3.4 Selective Power-Gate Decoder block based on data-validity

In this project, one of the objective is to reduce the on-operation static-power for address decoder through block-based power gating. By checking through the data-validity of the memory block, if the block doesn't content valid data the whole block will be power-gated.

Data validity is implemented in memory array which is used to check which entries contain valid data. The data validity circuit will output a signal to the power-gated decoder as a control signal for power-gate. By referring to Figure 26 which is the zoom in picture for a single block in Figure 21.

In this design, the power-gated transistor are control by 2 signal which is valid bit generated from memory array and output from the predecoder<1>. This is to ensure that only block with valid data and is requested for operation is power-up so to reduce the leakage power. By shutting down the whole block, this may cause some wake-time delay. So this project also have to examine the trade-off in wake-time penalty against the reduction of power consumption.

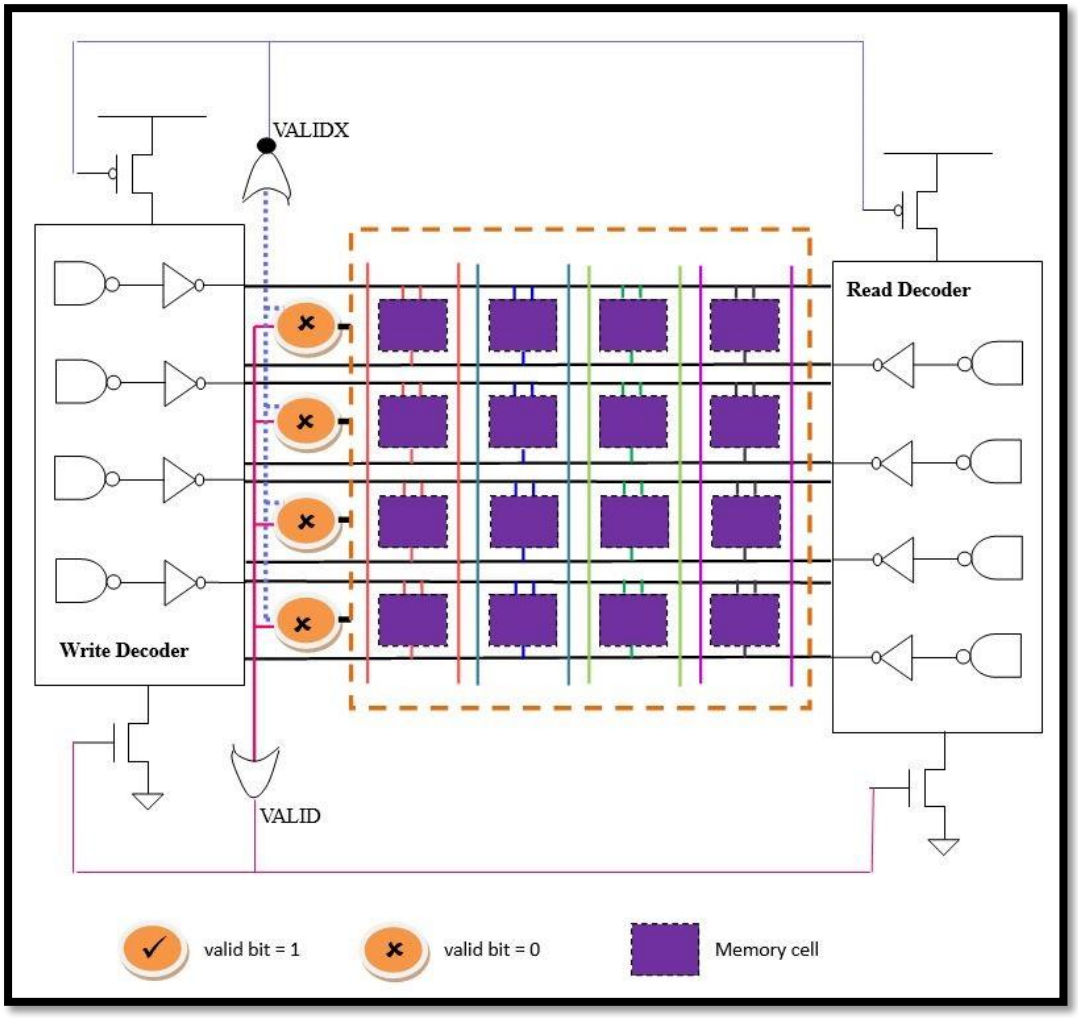


Figure 26 Single block decoder with no valid data

Figure above shown the proposed design for address decoder with valid bit detection. All the valid bit will OR together and the output of OR gate will connect to the power-gate. When all the row doesn't content valid data, the valid signal will output a '0' and validx will output a '1' which will power-down this block by turning off the sleep transistor.

The particular block only can power-down if all the rows doesn't contain valid data. For example, in Figure 27 shows that only 1 row of memory cell contain valid data but the other 3 rows doesn't contain valid data. In this case, this block cannot be power-down as there are memory cell that contain valid data. In the sense, no matter how many row doesn't contains valid data, only one memory cell contain valid data, the block have to be power up also.

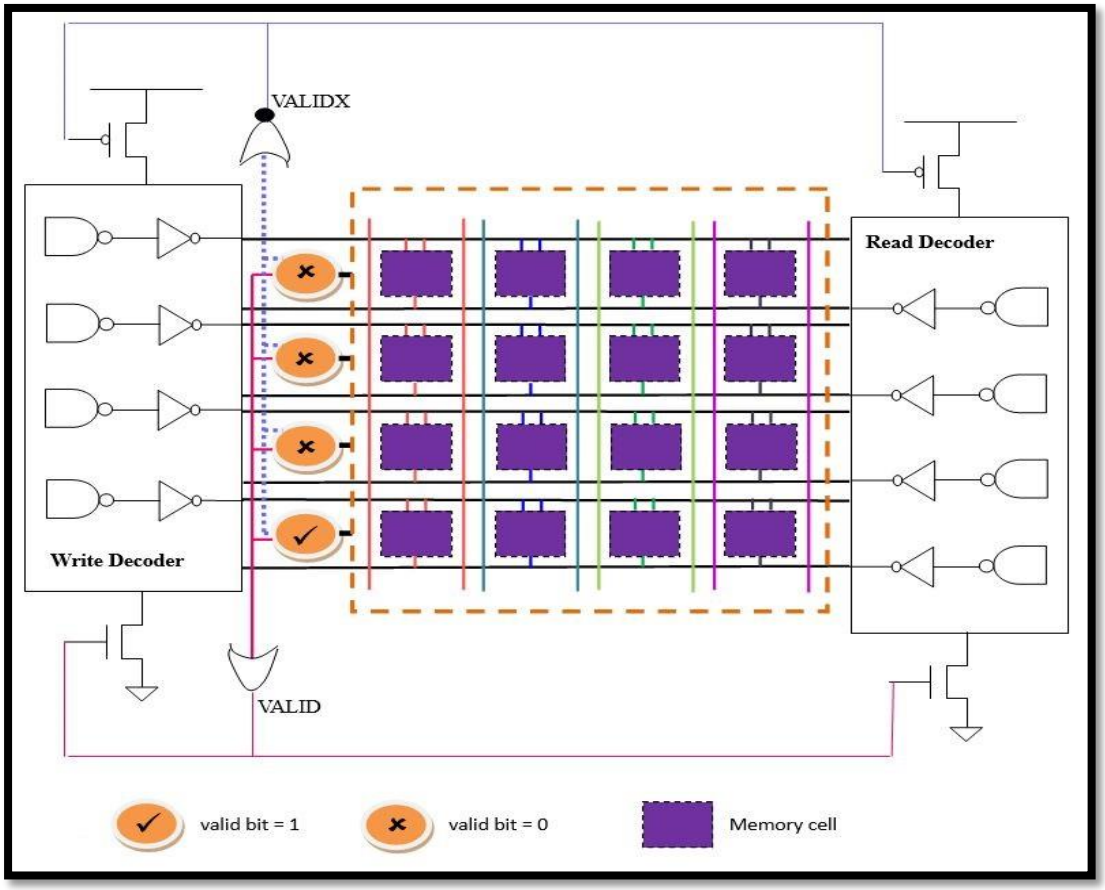


Figure 27 Single block decoder with valid data

3.5 Forward Addressing

Although power-gated idle blocks can reduced power consumption, but when a power-down block is required, it takes longer time to wake up from idle mode. By implementing forward addressing in the decoder, the amount of delay cause by power gating may reduce when an on-request entry is being power-up.

According to Principle of Spatial Locality, if a particular memory location is being referenced, then it is likely that nearby memory locations will be referenced in the near future. In this case it is common to attempt to activate the neighbouring memory location next to the current memory location which is worthwhile to prepare for faster access.

Forward addressing only beneficial where memory location is referenced according to Principle of Spatial Locality. If every address location is equally randomly accessible from the CPU, then forward addressing is utterly irrelevant. If this is the case, by implementing forward addressing in decoder it may cause a longer delay because of the extra logic gate before activating the memory cell.

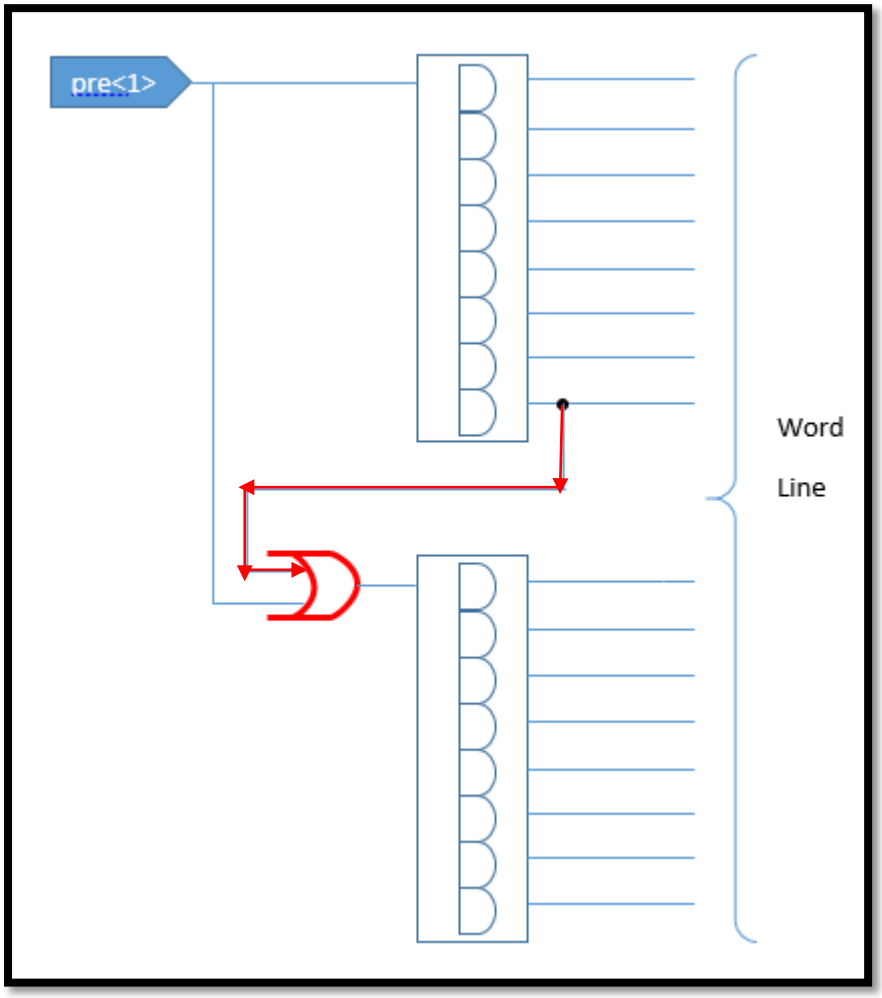


Figure 28 Address Decoder with Forward Addressing

The proposed design for address decoder with forward addressing is by adding an OR gate between the output of last entry of sub decoder and output from predecoder<1> as shown in Figure 28. For example by referring to the red arrow, when the last entry is being requested, the same signal that active the last memory cell will also connected to the OR gate to turn on the sub decoder block.

3.6 Expected Output

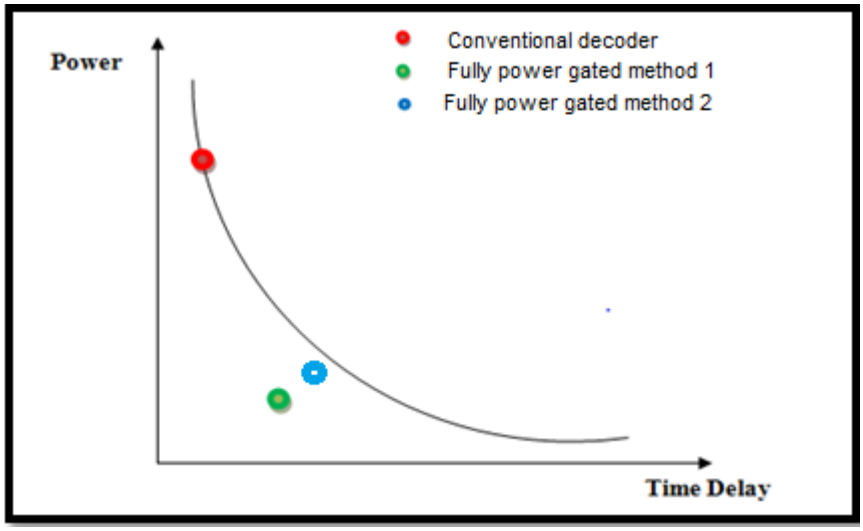


Figure 29 Expected output for proposed schemes

As shown in the graph above, the red dot indicated the power consumption that introduced by address decoder which used in the conventional decoder design. In order to solve the high power dissipation in existing design now, power-gated and forward addressing has proposed in this project. There are 2 various type of circuit which using power gating techniques has proposed, the first type is power gated with multilayer and the other type is power-gated using logic gate as shown in figure24 and figure 25 respectively.

This 2 type of power gated will be tested on leakage power dissipation by comparing with the conventional design. Besides that, Design 1 and Design 2 also will be comparing among themselves in terms of static power consumption and performance. The green dot refers to the power consumption for the execution of Design 1 power

gating which will consume lesser power than Design 2 because of the multilayer footer power switch, transistor behaviours like resistor when it is closed, hence when decoder is not valid, the footer switched will be turning off, the resistor will block the current, and power dissipation will be reduced.

For the forward addressing, it can reduce the wake-delay penalty significantly by turning on the adjacent entry using Principle Spatial Locality. However, this proposed solution will be only useful when the next referring address location follow the sequence sequentially. This proposed solution is to study the improvement in terms of timing.

3.7 Timeline

3.7.1 Project 1 Timeline

ID	Task Name	Start	Finish	Duration
1	Discussion and Decide Project Title	27-May-13	31-May-13	5d
2	Problem statement and Objective	01-Jun-13	07-Jun-13	7d
3	Research Paper & Literature Review	08-Jun-13	27-Jun-13	20d
4	Methodology of Project	28-Jun-13	12-Jul-13	15d
5	Preliminary Report	13-Jul-13	30-Jul-13	18d
6	Submission of Preliminary Report	31-Jul-13	31-Jul-13	1d
7	Finalization of Project 1 Report	01-Aug-13	18-Aug-13	18d
8	Submission of Project 1	19-Aug-13	19-Aug-13	1d
9	Poster and Presentation slide preparation	20-Aug-13	25-Aug-13	6d
10	Oral Presentation of Project 1	28-Aug-13	28-Aug-13	1d
11	Poster Submission	28-Aug-13	28-Aug-13	1d

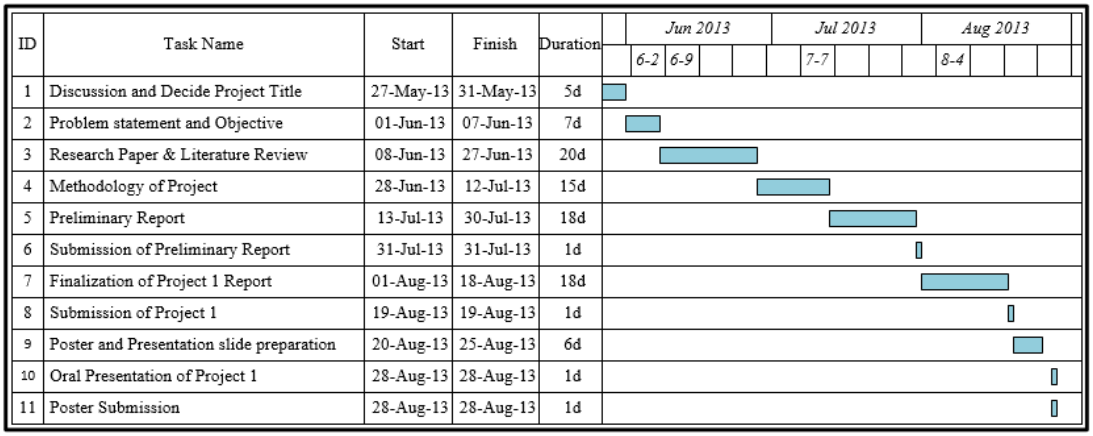


Figure 30 Gantt chart for Project 1

3.7.2 Project 2 Timeline

ID	Task Name	Start	Finish	Duration
1	Discussion on project scale and design	13-Jan-14	17-Jan-14	5d
2	Implementation Proposed Design circuit	18-Jan-14	27-Jan-14	10d
3	Combination and Testing with other parts	28-Jan-14	30-Jan-14	3d
4	Implementation project on larger scale	31-Jan-14	19-Feb-14	20d
5	Power and time analysis	20-Feb-14	11-Mar-14	20d
6	Submission of Draft report	12-Mar-14	12-Mar-14	1d
7	Enhancement and finalize Project 2	13-Mar-14	03-Apr-14	22d
8	Turnitin check	04-Apr-14	04-Apr-14	1d
9	Submission of Project 2	07-Apr-14	07-Apr-14	1d
10	Preparation for Presentation and Poster	08-Apr-14	15-Apr-14	8d
11	Oral presentation and Poster Submission	16-Apr-14	16-Apr-14	1d

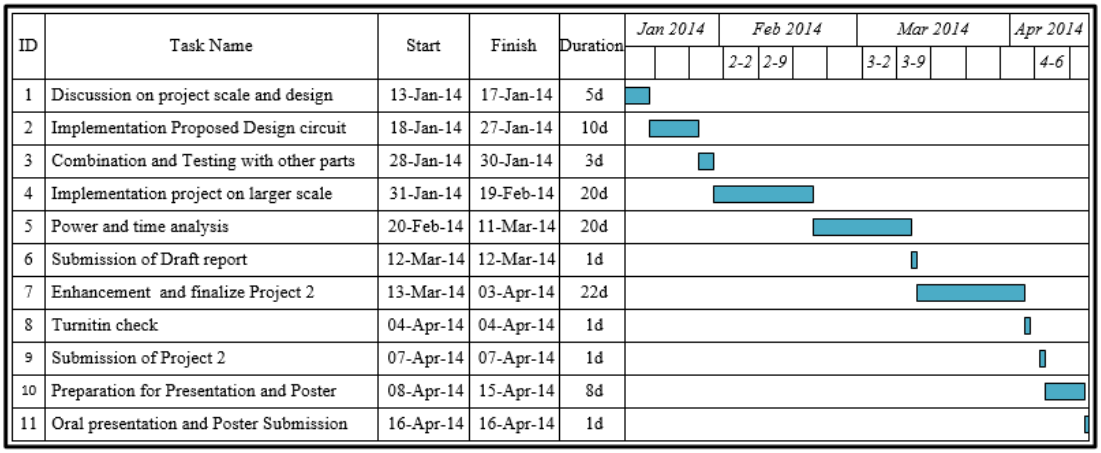


Figure 31 Gantt chart for Project 2

Chapter 4: Implementation and Verification of Proposed Designs

4.1 Implementation of Proposed Designs

In this project, the schematic of proposed selective power-gated address decoder are draw with Electric VLSI and analyse by using LTspice IV. All the schematics will draw based on C5 mocmos 300nm. LTspice IV will be used to simulate waveform on voltage, current and delay.

4.1.1 Conventional Address Decoder

Figure 34 below shows a conventional 6 to 64 address decoder which construct with two 3 to 8 predecoder (Figure 32) and 8 block of decoders (Figure 33).

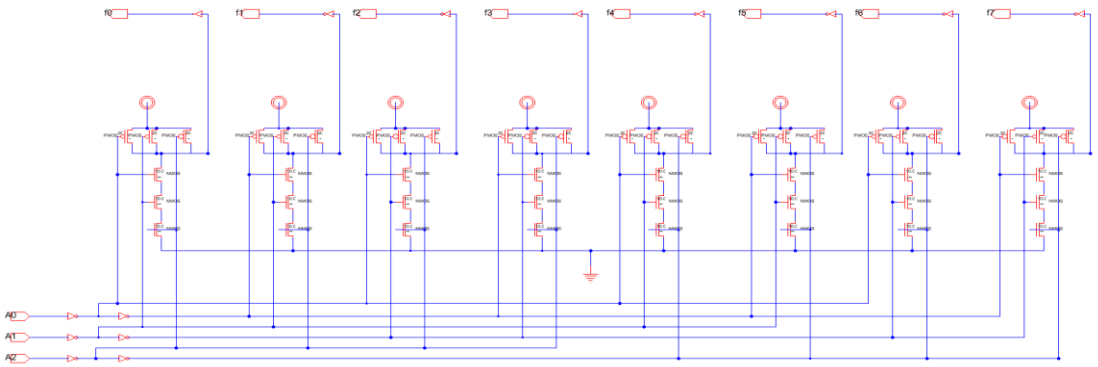


Figure 32 3 to 8 Predecoder

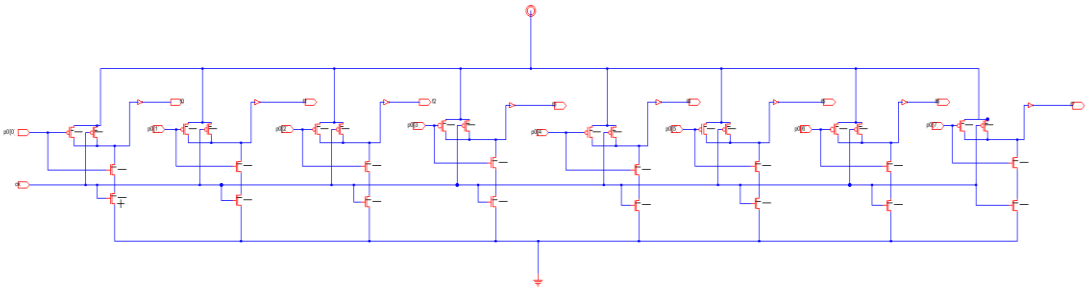


Figure 33 8 input Decoder block

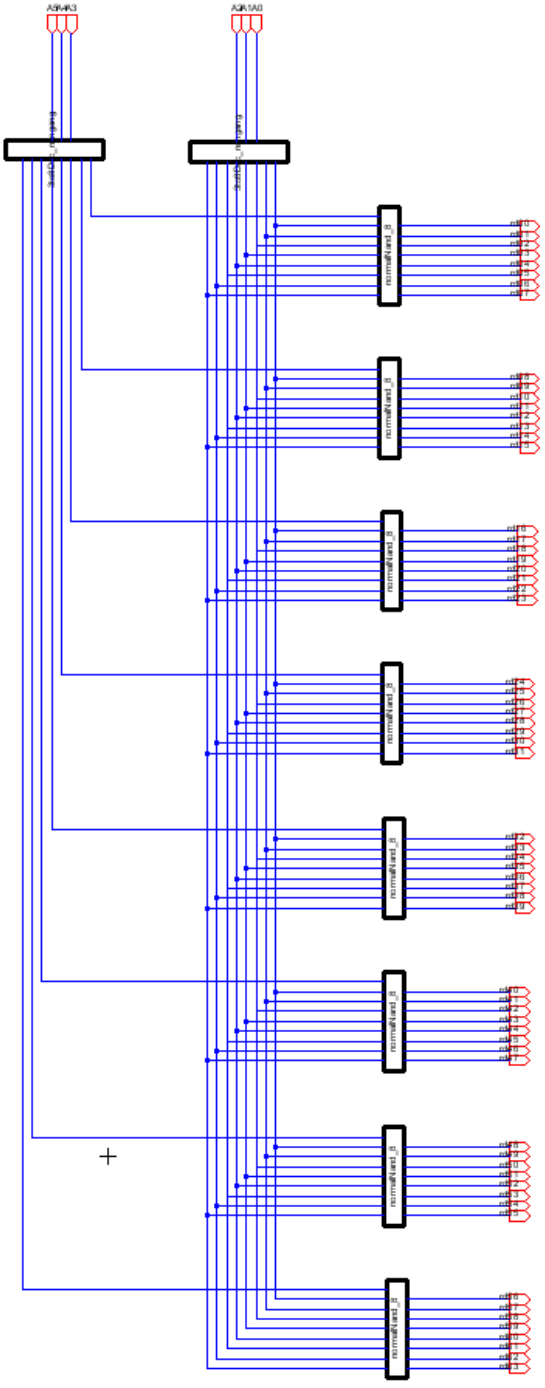


Figure 34 conventional 6 to 64 Address Decoder

As shown in Figure 34, predecoder<1> is use to choose which decoder block to be activate while predecoder<0> take care of lower bit address to produce signal to choose which entry to be activate.

Figure 35 shows the timing diagram for 6-to-64 decoder. While A5, A4, A3 signal is 000, predecoder<1> will activated the first block. For lower bit address A2, A1, A0 signal is 000, predecoder<0> will activated the first entry. Therefore rd00 will be asserted. On the next clock cycle, A5, A4, A3 signal remain the same, while the A2, A1, A0 signal become 001. In this case, the same block will be activated while predecoder<0> will activated the second entry. Therefore rd01 will be asserted.

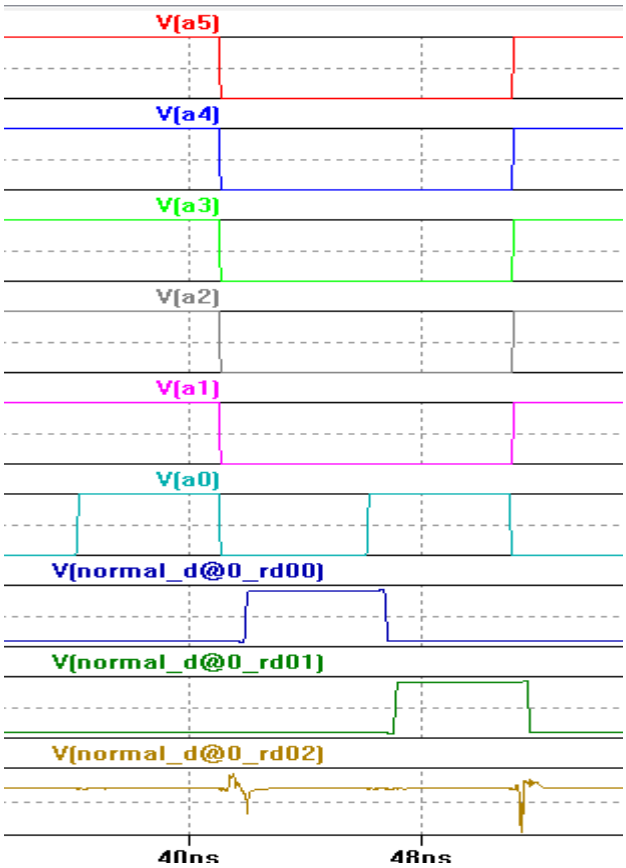


Figure 35 Timing Diagram for 6 to 64 Address decoder

4.1.2 Proposed Design Read Decoder

In this project, all the proposed design decoder are implement by using shared decoder. Shared decoder is also known as tree decoder. Figure 36 shows the decoder share the pull down NMOS for the same state at the output (green box). Other than predecoder, Design 1 and Design 2 read decoder and write decoder are also using shared decoder base implementation.

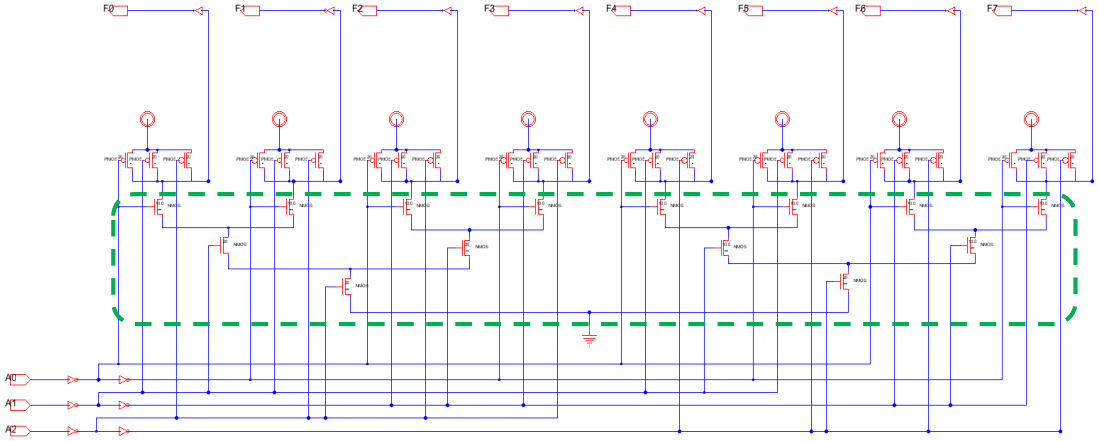


Figure 36 Shared decoder based 3-to-8 Predecoder

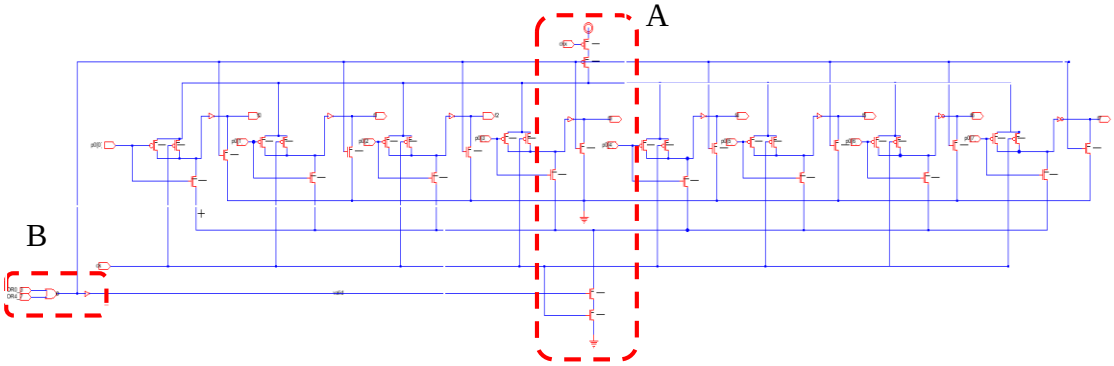


Figure 37 Design 1 Read Decoder Block

Design 1 Read Decoder is implement by using 2 layer of power gate transistor. The first layer of power gate is controlled by block based signal, ckx (pull up network) and ck (pull down network). While the second layer of power gate is controlled by validity signal, validx (pull up network) and valid (pull down network). This can be seen from figure 38 which is a zoom in version of figure 37. Isolator (green box) is being add to the design so that when decoder block is turn off, isolator will pull down the output to 0.

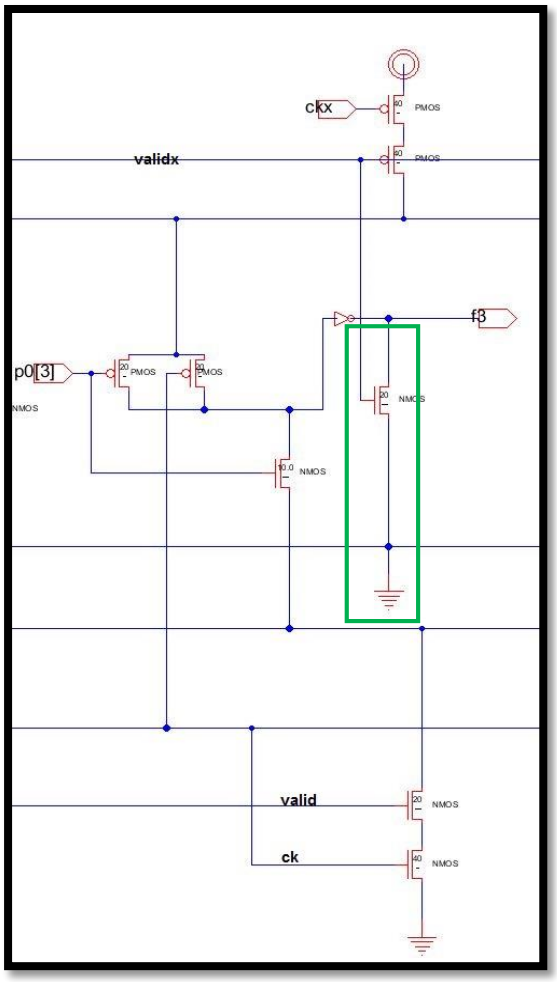


Figure 38 Zoom In of Figure 37--A

For control signal valid and validx, both signal are obtain from memory cells.

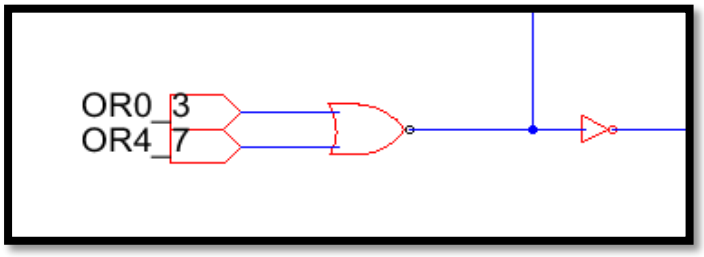


Figure 39 Zoom In of Figure 37 –B

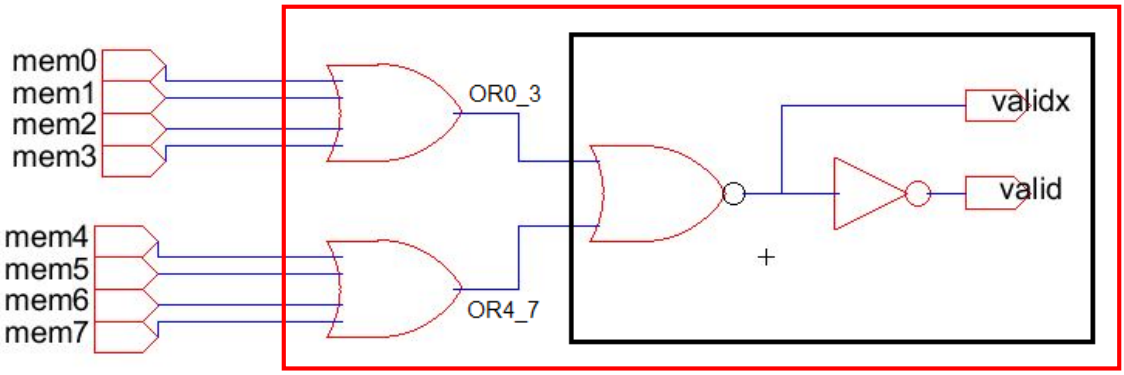


Figure 40 valid bit circuit

In figure 39 shows that how address decoder obtain control signal from memory cells. In address decoder only the boxed circuit (black) is included while other part remain in memory cells. This is to save the number of input in for the decoder. In this case we only need 2 input pin which is OR0_3 and OR4_7.

If the red box circuit is included in address decoder design, then every single block of address decoder will need extra 8 input pin.

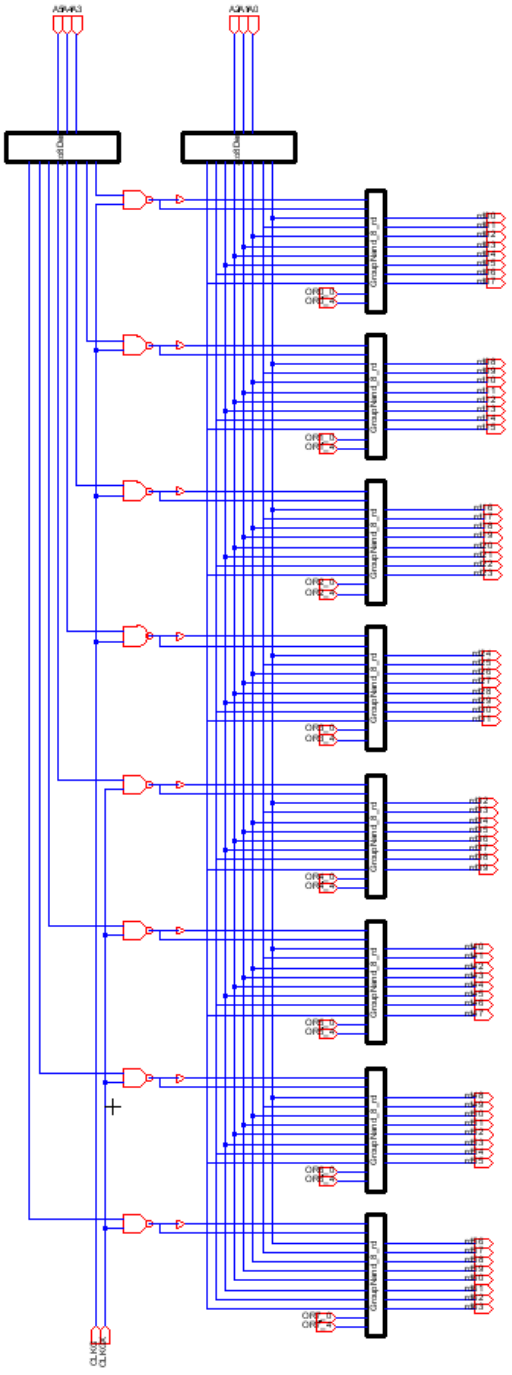


Figure 41 Design 1 6-to-64 Read Decoder

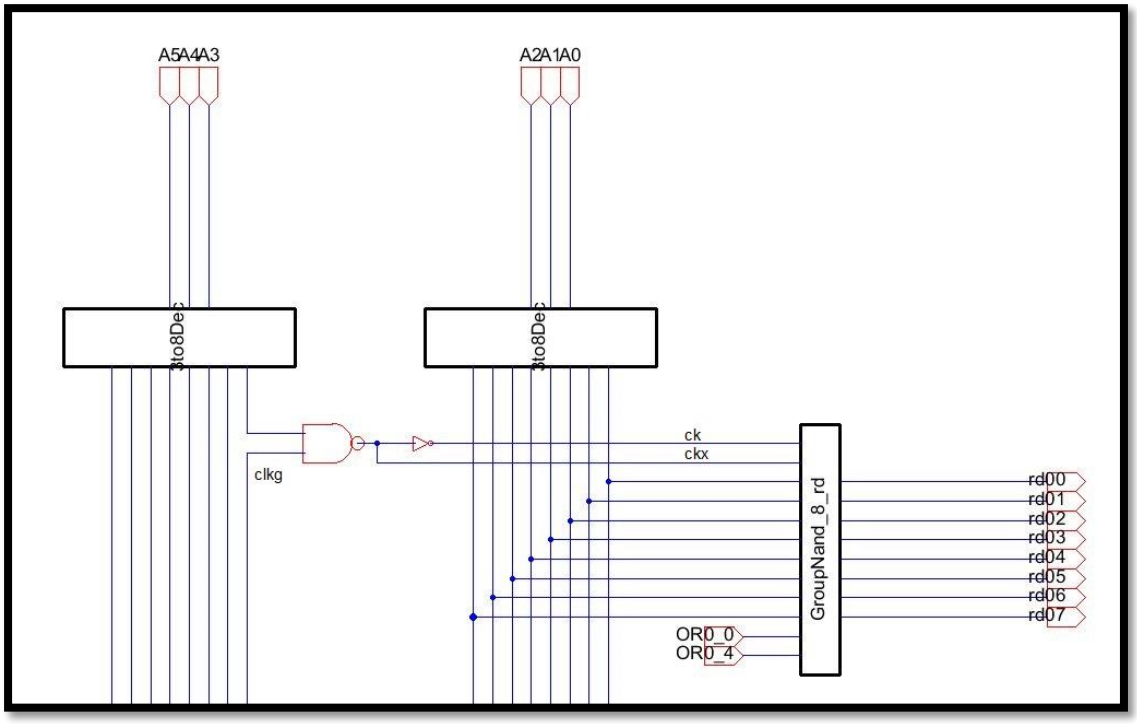


Figure 42 Zoom in of Figure 41

The block based control signal are obtain from Figure 42. The address decoder function every time clkg (gated clock) asserted high. Predecoder<1> (A5, A4, A3) will select which block to activate and the signal will NAND together with clkg to provide block based control signal.

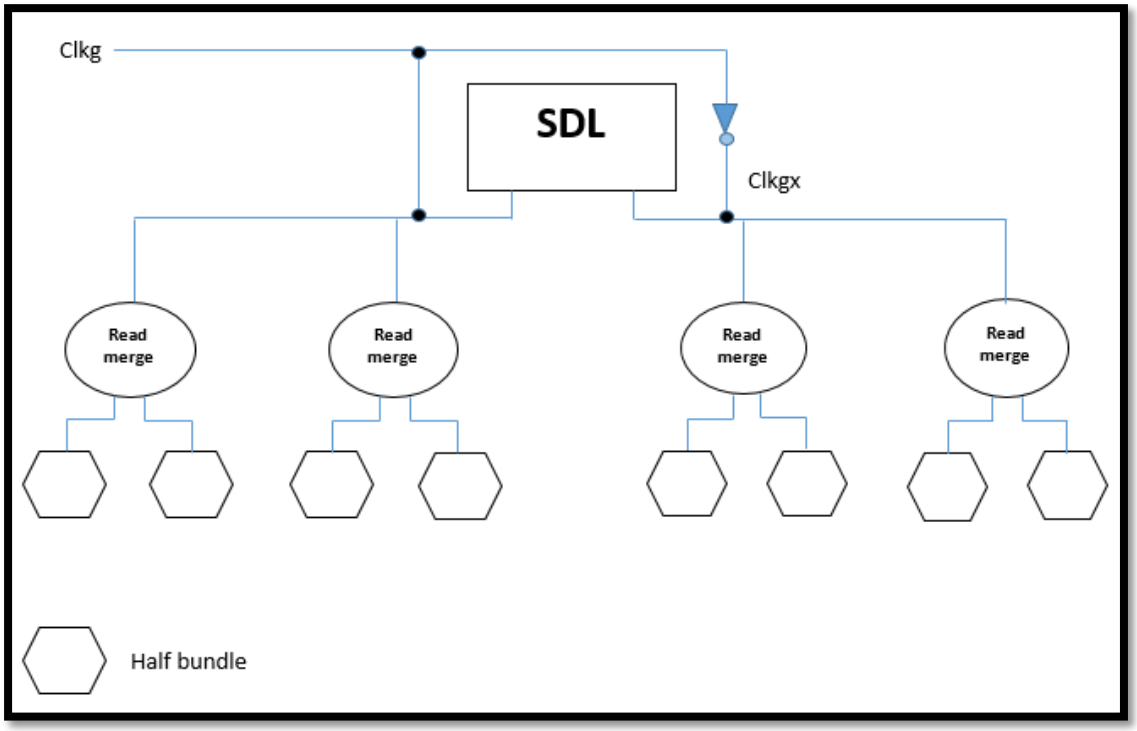


Figure 43 clkg and clkgx for domino multiplexer

As can see from figure 41, there are 2 gated clock signal which are clkg (gated clock) and clkgx (inverse gated clock). This is because read decoder need to synchronize with domino multiplexer when domino multiplexer performs pre-charge and evaluation phase. Domino multiplexer is separate into left bundle and right bundle while one bundle is pre-charge another bundle is evaluation. So read decoder need to have to different control signal to prevent contention happen as shown in figure 43.

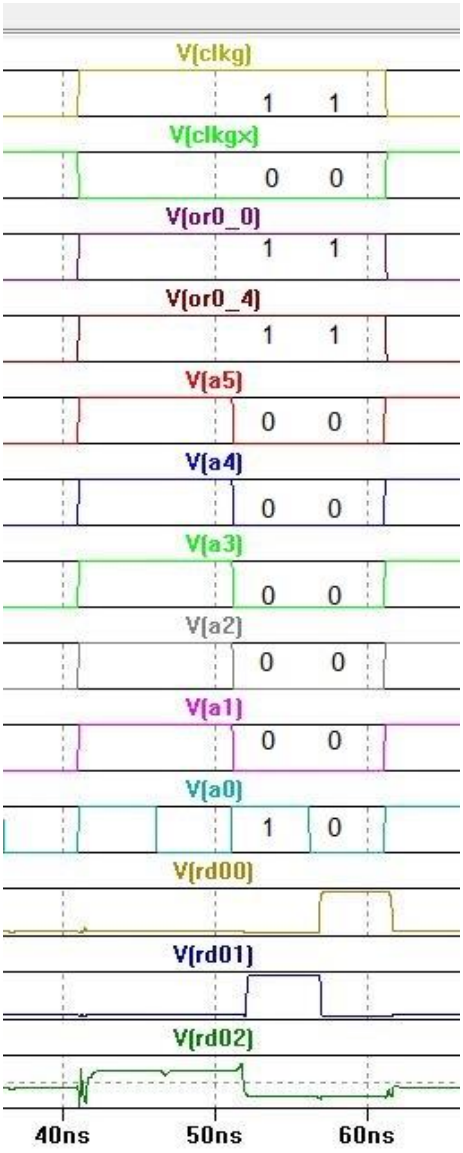


Figure 44 Timing Diagram for Design 1 Address Decoder

From the timing diagram we can see that Design 1 Address Decoder has the same output compare with conventional address decoder. When clkg = 1, and clkgx = 0 it mean the block is activated and or0_0 and or0_4 =1 mean that there are valid data in memory cell.

Design 2 read decoder is implement by only using 1 layer of power gate transistor with NAND and NOR gate. Pull up network power gate is control by valid signal NAND with ck signal while pull down network power gate is control by validx signal NOR with ckx signal. Isolator (green box) is also added in this design.

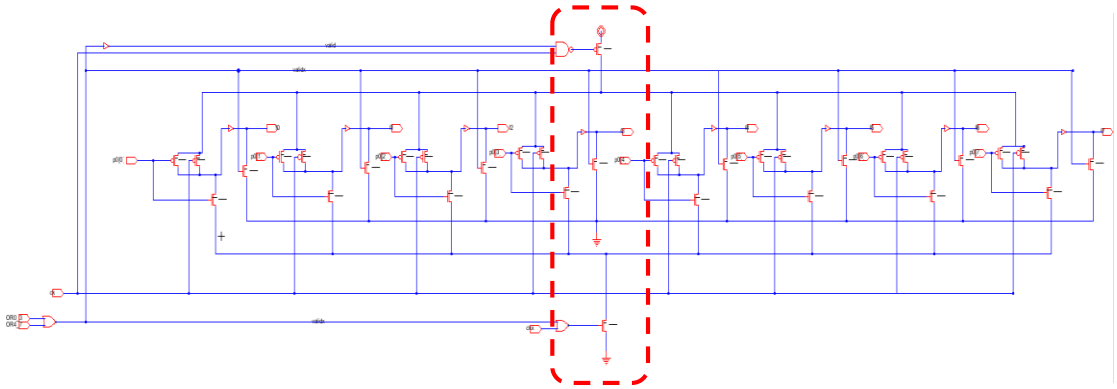


Figure 45 Design 2 Read Decoder Block

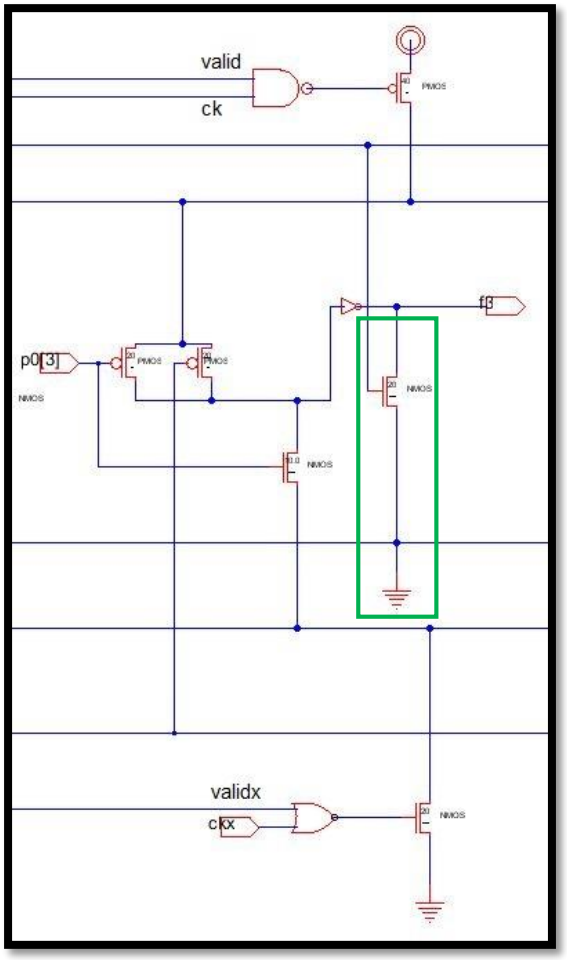


Figure 46 Zoom in of Figure 45

For Design 2 address decoder, the control signal ck, ckx, valid, validx is obtain exactly the same with Design 1 address decoder. Design 1 and Design 2 have the same main frame. Both using the same 3-to-8 predecoder, valid bit circuit, and block based signal circuit. The only different is read decoder block which show in figure 47(red box).

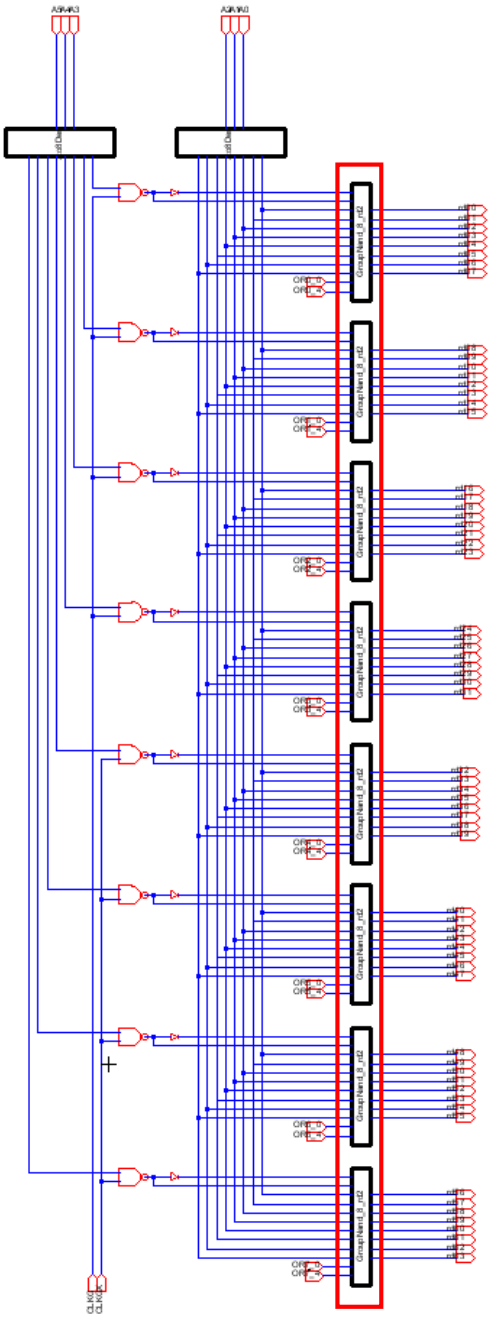


Figure 47 Design 2 Read Decoder Block

4.1.3 Proposed Design Write Decoder

In register file, there are 2 type of decoder which are read decoder and write decoder. For read decoder, we can power-gated the block based on data validity and on demand. This is because we only read a memory array when the address is being called and the memory array contain valid data. But for write decoder, no matter the memory array contain valid data or not, write decoder have to assert the memory cell to write in the data. Therefore, write decoder only have one type of design.

Write decoder is also similar to read decoder. Both using the same 3-to-8 predecoder and block based signal circuit. Write decoder input has change to B5, B4, B3, B2, B1, B0 for easy recognize purpose.

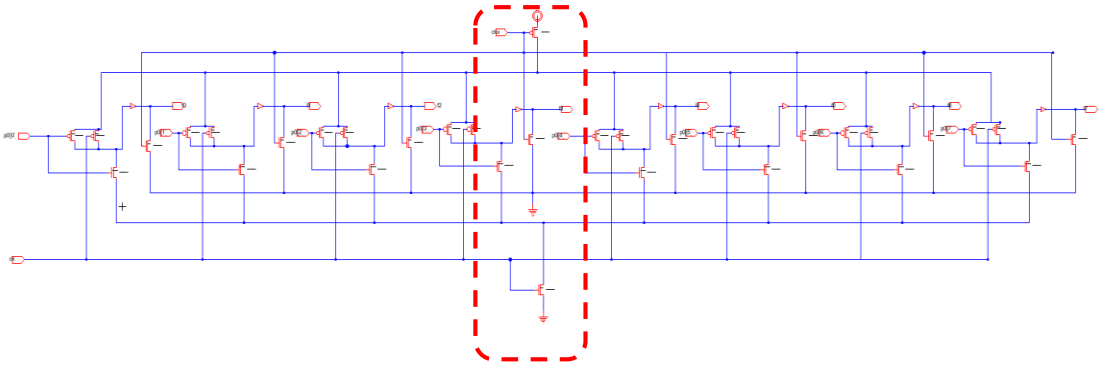


Figure 48 Write Decoder Block

Figure 49 shows the pull up network power gate is being control by ckx signal while pull down network power gate is being control by ck signal. Isolator (green box) is also added in write decoder block to pull down the impedance value when the decoder block is power off.

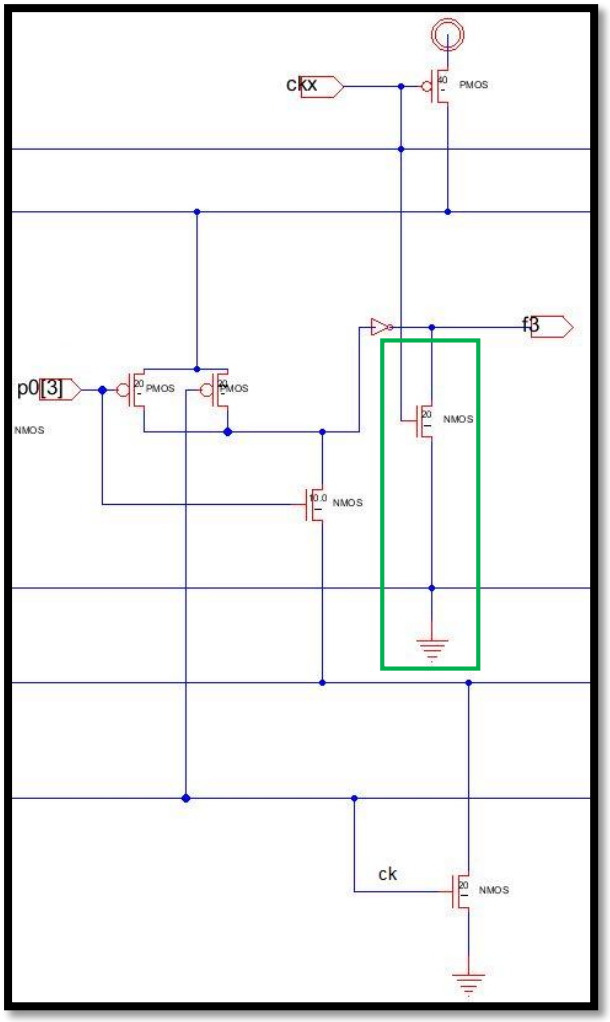


Figure 49 Zoom In of Figure 48

Notice that from figure 49, there is only one control signal clkg (gated clock) for write decoder. This is because domino multiplexer is not in use when write process. The whole write process is just communication between decoder, memory cells and input data.

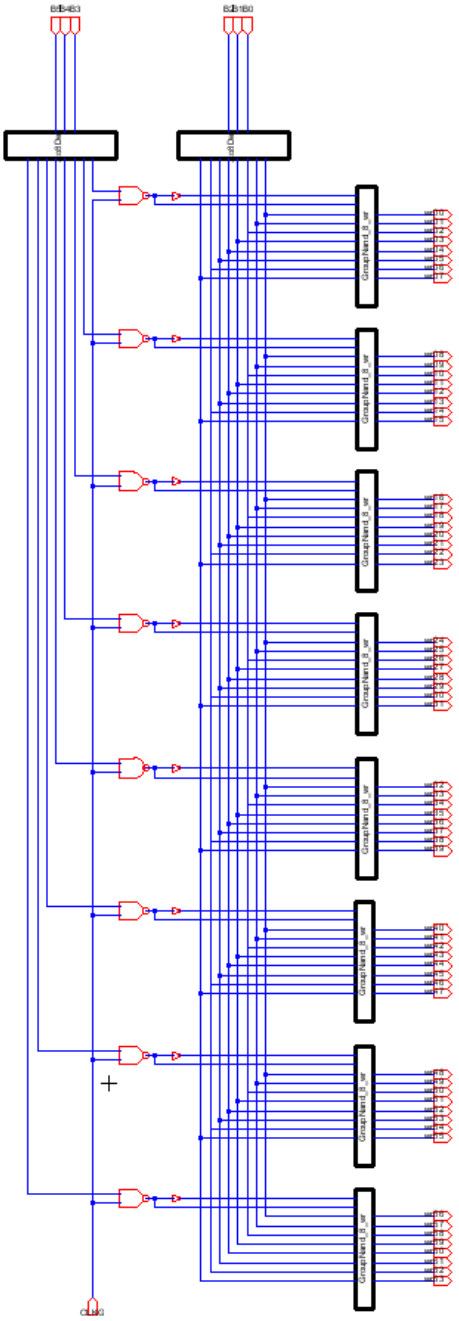


Figure 50 6-to-64 Write Decoder

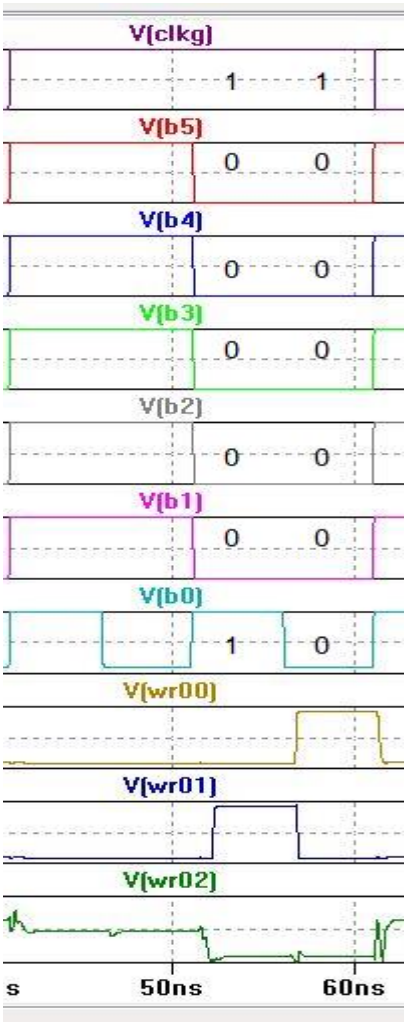


Figure 51 Timing Diagram for write decoder

While B5, B4, B3 signal is 000, predecoder<1> will asserted and AND with clkg to activated the first block. For lower bit address B2, B1, B0 signal is 000, predecoder<0> will activated the first entry. Therefore wr00 will be asserted. On the next clock cycle, B5, B4, B3 signal remain the same, while the A2, A1, A0 signal become 001. In this case, the same block will be activated while predecoder<0> will activated the second entry. Therefore wr01 will be asserted.

4.1.4 Forward addressing

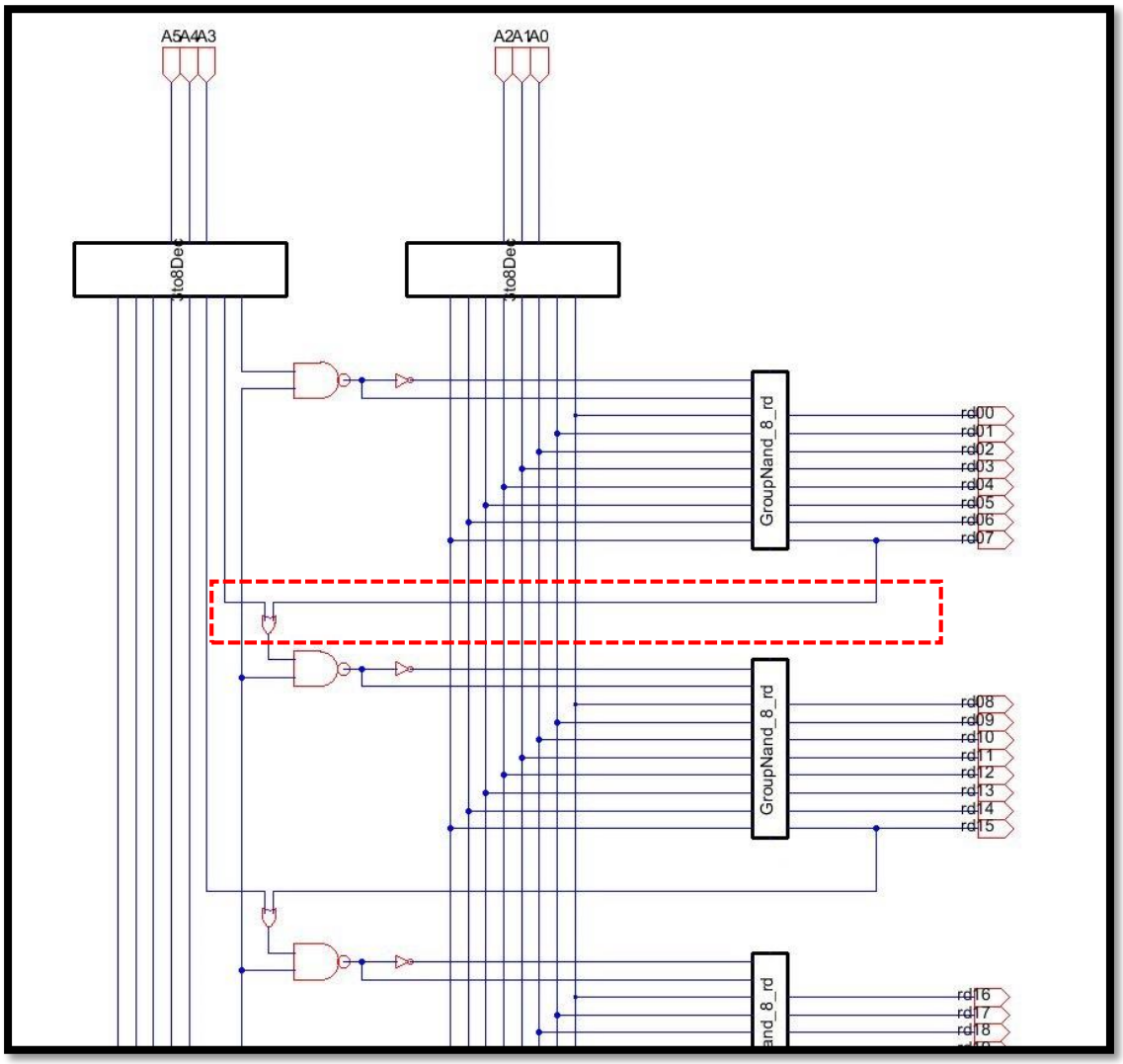


Figure 52 Forward addressing

Figure 52 is the forward addressing implemented in addressing decoder to speed up the activation speed. OR gate is added in with input from the last entry of the decoder block and predecoder<1>. This is to ensure that the block that being call can be power up or

when the last entry is being activated the next block is power up to prepare for to being call.

This design is implemented together with block-based power-gated. When the decoder is being power off for power saving purpose but the same time it will also cause delay when reactivate the decoder block. Therefore, forward addressing is used to speed up the address decoder by power up the particular decoder block before the entry being call according to Principle of Spatial Locality.

4.2 Testing and Verification of the Result for the Proposed Designs

LTspice IV is use in this project for simulation purpose. In order to verify the power efficiency of the proposed designs in this projects, several tests will be conducted to compare the power consumption and time delay between conventional designs and proposed design, Selective power-gated address decoder.

There are 2 main conditions that used to control the power gated which are data validity and on-demand. Therefore this 2 conditions will take into consideration when conducting the tests. To study on power consumption, VDD and VSS need to be observed. The test is carry out by pulling out the VDD and VSS of the whole address decoder (every predecoder, every sub decoder block) and connect together to a main VDD and main VSS.

The testing of address decoder is differentiate into 4 test case. First of all, study will be conduct on read decoder design 1 and design 2 with four condition which are block on--valid on, block on--valid off, block off--valid on, and block off--valid off. Block on mean that the sub decoder block is being power on and valid on mean that there are valid data contains inside the memory cells. Next, write decoder will be test only based on block based power-gated. This is because no matter the memory cell contains valid data or not, write decoder still have to asserted the entry that being call so that input data can be written into the memory cell.

The third test case is to verify and study about block based power-gated. This will test different number of decoder blocks that have been power down and the power consumed. Follow by verify implement of forwarding address. For this test case, the speed will be taking into consideration. Basically, the test are going to carry out by looking into the transition of the signal. The time from 10% to 90% when the transition of signal will be compare with conventional address decoder.

Before carry out the analysis and testing on all the designs, the proposed design have been combined with memory array and domino multiplexer to ensure that the address decoder is fully functional.

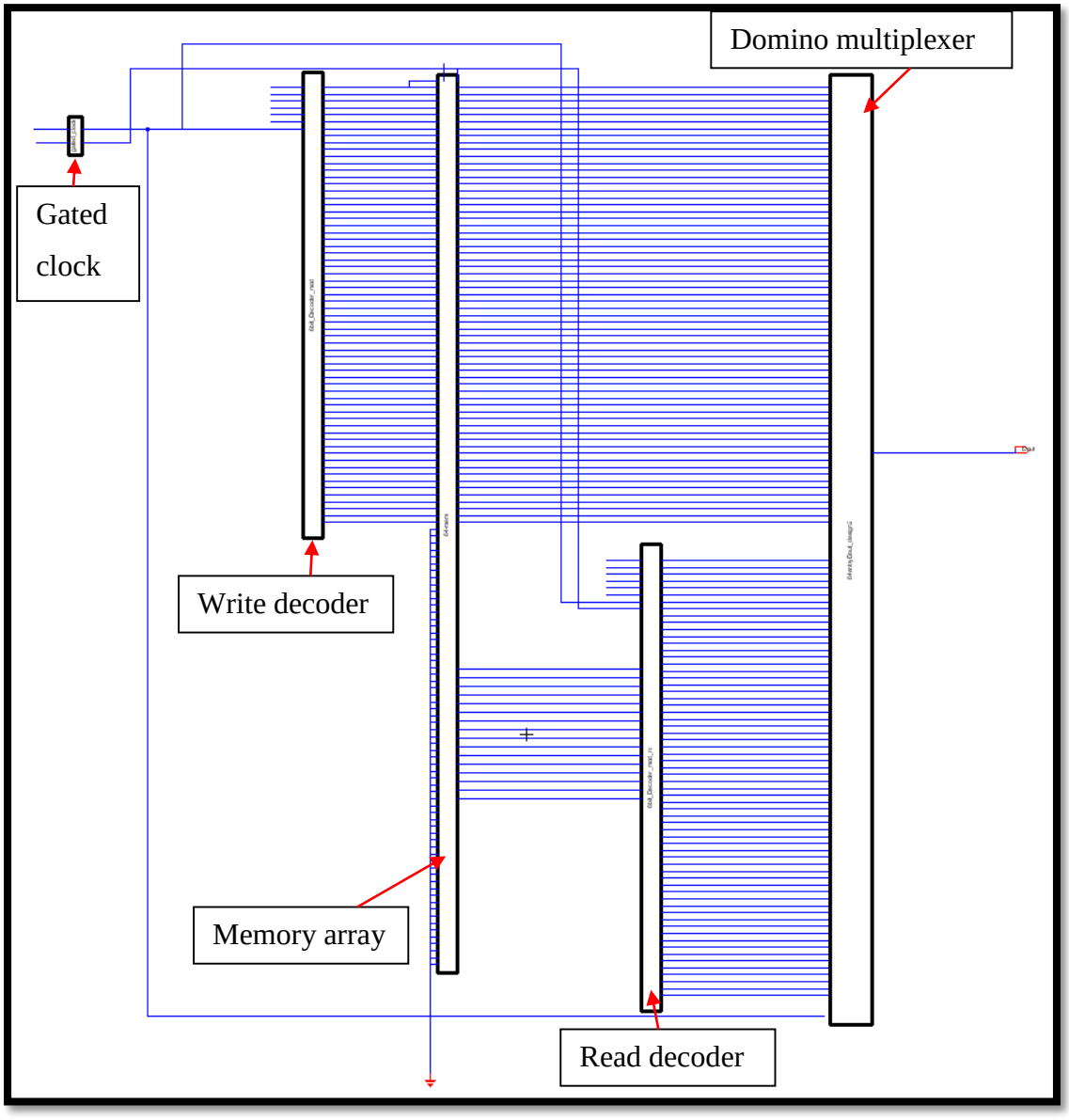


Figure 53 Register File

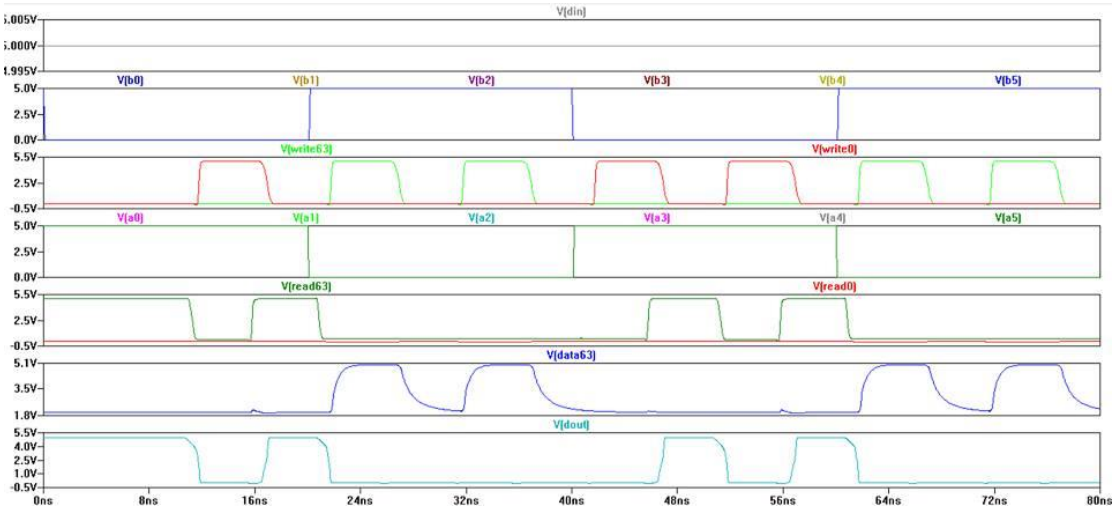


Figure 54 Timing Diagram for Register File

By looking at the timing diagram above, when the write decoder input B5, B4, B3, B2, B1, B0 = 1, the output write63 is asserted when every time clock asserted high. The data din =1 will be write into memory cell (data63).

As for read process, when read decoder input A5, A4, A3, A2, A1 = 1, the output read63 will asserted and data in memory cell will be read as register output(dout). Notice that when read decoder input A5, A4, A3, A2, A1 = 0, read0 did not asserted high. This is because the block do not contain valid data so the block is turn off and the output is pull down to 0 by isolator.

4.2.1 Normal Decoder

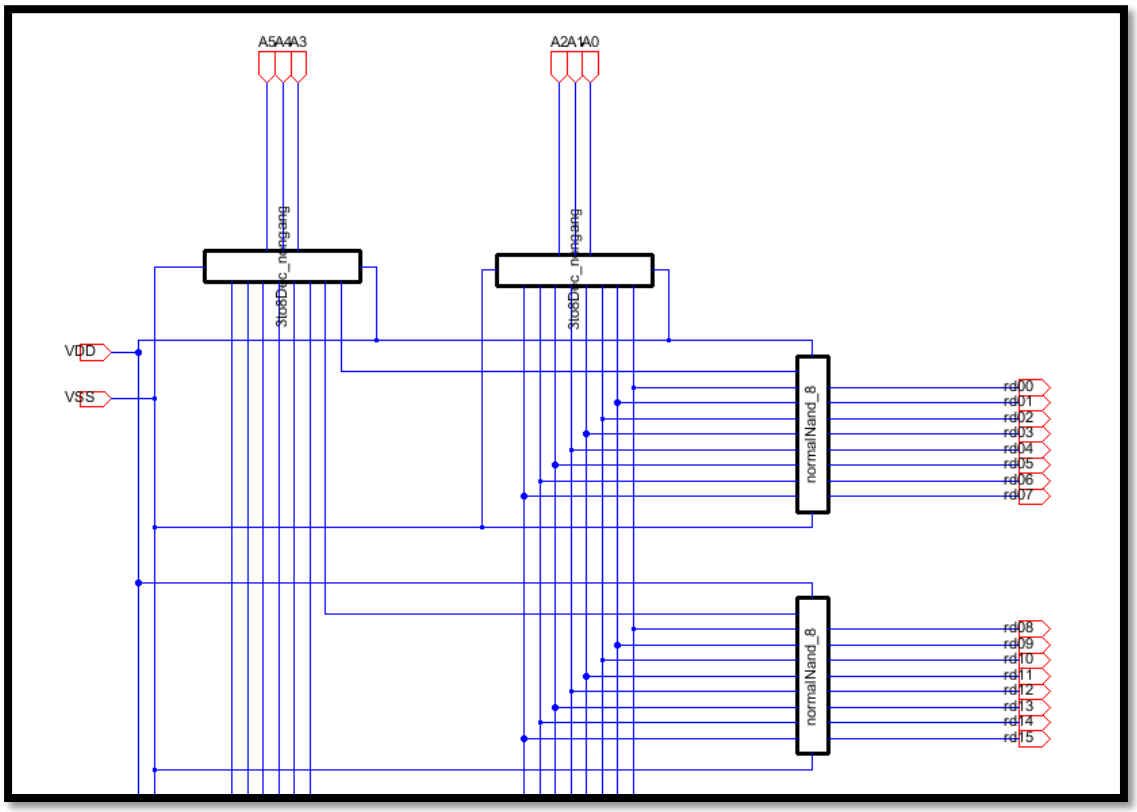


Figure 55 Test - Conventional Decoder

Conventional Decoder		ivdd	ivss
000000	Rd00	-1.2437nA	41.051pA
101010	Rd42	-1.2437nA	41.051pA
111111	Rd63	-1.2437nA	41.051pA

Table 3 Leakage of conventional Decoder

The decoder had been testing with different address input to test the stability of current leakage. All address input having the same ivdd and ivss.

4.2.2 Read Decoder & Write Decoder

From the timing diagram below, shows that the proposed design address decoder only function when the block is being power up and contain valid data. When clkg = '1' and clkgx = '0', the block is being power up. Signal or0_0 and or0_4 that obtains from memory cells are the control signal for data validity. When or0_0 and or0_4 = '1', the block contains valid data.

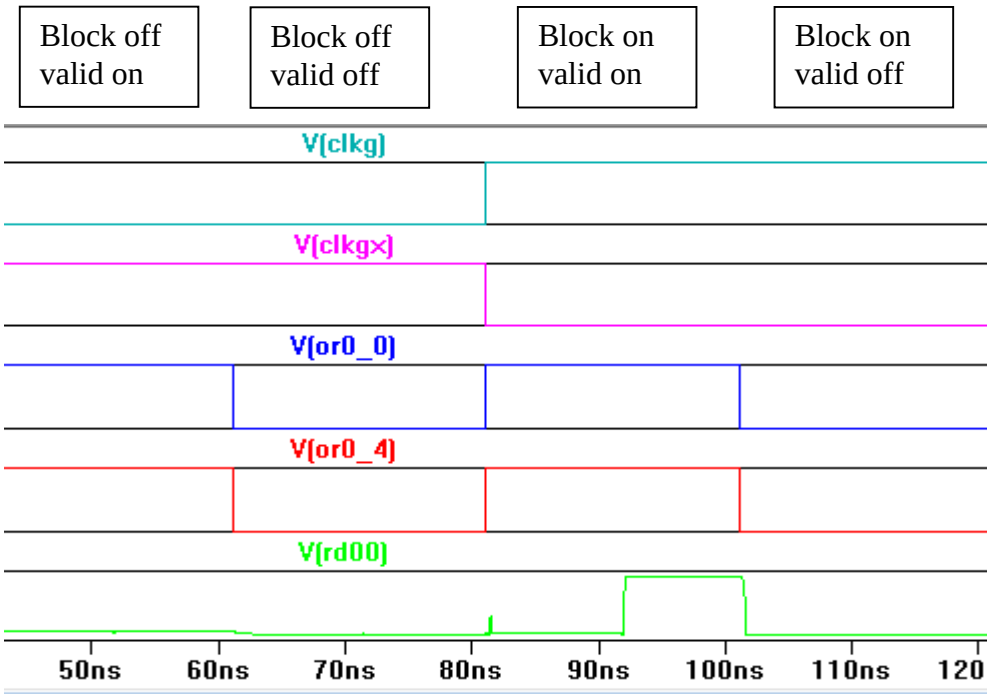


Figure 56 Timing diagram for Proposed Read Decoder

Read Decoder Design 1		ivdd	ivss
Block on, valid on			
000000	Rd00	-9.24143mA	41.051pA
111111	Rd63	-9.24143mA	41.051pA
Block on, valid off			
000000	Rd00	-10.3635mA	32.0622pA
111111	Rd63	-10.3635mA	32.0622pA
Block off, valid on			
000000	Rd00	-10.6146mA	32.2423pA
111111	Rd63	-10.6146mA	32.2423pA
Block off, valid off			
000000	Rd00	-10.4886mA	32.0587pA
111111	Rd63	-10.4886mA	32.0587pA

Table 4 Leakage of Design 1 Read Decoder

Read Decoder Design 2		ivdd	ivss
Block on, valid on			
000000	Rd00	-8.32664mA	40.9749pA
111111	Rd63	-8.32664mA	40.9749pA
Block on, valid off			
000000	Rd00	-9.4024mA	30.9461pA
111111	Rd63	-9.4024mA	30.9461pA
Block off, valid on			
000000	Rd00	-9.51616mA	30.9668pA
111111	Rd63	-9.51616mA	30.9668pA
Block off, valid off			
000000	Rd00	-9.52782mA	30.9668pA
111111	Rd63	-9.52782mA	30.9668pA

Table 5 Leakage of Design 2 Read Decoder

Write decoder only consider on block based power-gated. The data validity do not take in as consideration as regardless memory cells contains valid data or not, write decoder have to be functioning to write in the input data. The write decoder block is powered up when clkg =’1’ and clkgx = ‘0’ as can be see from timing diagram below

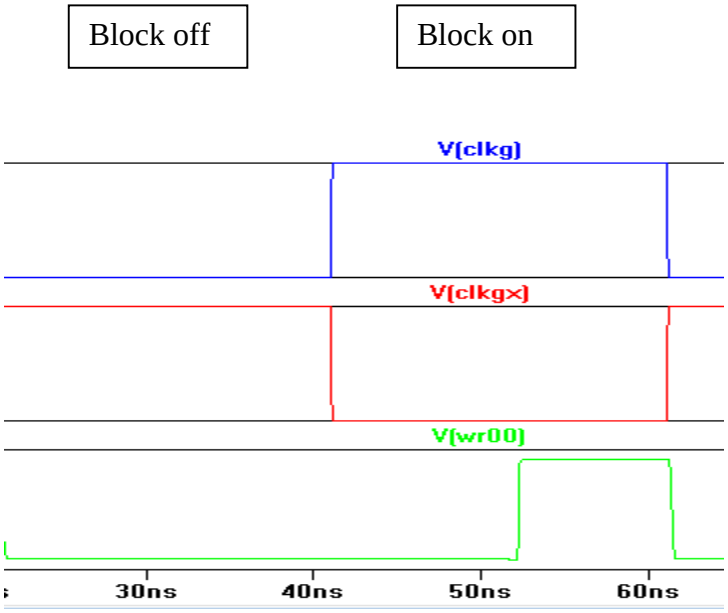


Figure 57 Timing diagram for Proposed Write Decoder

Write Decoder		ivdd	Ivss
Block on			
000000	wr00	-8.40822mA	40.9749pA
111111	wr63	-8.40822mA	40.9749pA
Block off			
000000	wr00	-9.6094mA	30.9668pA
111111	wr63	-9.6094mA	30.9668pA

Table 6 Leakage of write decoder

In previous chapter mentioned that the proposed design address decoder will reduce the power consumption compare to conventional. Design 1 is expected to more power saving compare to Design 2. Both Design 1 and Design 2 proposed designs are expected to reduce the power consumption compare to conventional design because the proposed designs are being powered down when there are no valid data and not being called.

However, those tables above shows that the proposed designs are out of the expectation. From the real results, both Design 1 and Design 2 proposed design did not reduce the power consumption but increase a lot of power consumption compare to conventional design. The analysis results shows that the power consumption increase from conventional design follow by Design 2 and highest power consumption is Design 1. From the table, it shows that both Design 1 and Design 2 have about $7x10^6$ times power consumption compare to conventional design. As for write decoder, because only a single layer of power-gated transistor the power consumption is about $4x10^6$ times compare to conventional design.

There are few possible problems that caused this unexpected results. Firstly, the limitation of open source design environment tools that available is not the most suitable environment for this project. This is because limited library that can be found to use in Electric VLSI. Semiconductor C5 mocmos 300nm library is not the ideal model to analysis and verify the leakage power because for 300nm scale transistor, the leakage current does not affect much on power consumption. The ideal design environment should be 50nm-100nm design environment.

The number of transistors in proposed power-gated schematic design may be one of the problem. The number of transistors in proposed designs is more than conventional design. This is because addition logic gate to the design and isolator for every output of decoder. Each transistor contribute leakage current and by adding up all the leakage current it will become a significant amount of power consumption.

Notice that mentioned in chapter 2, there are several type of transistors such as low-leakage transistor, high speed transistor and nominal transistor. Different type of transistor should be used in different circuit. Low leakage transistor which refer to the transistor with high threshold voltage, lower speed and low power consumption compare to nominal transistor. This transistor is the best type to use as power-gate transistor. However in this project, nominal transistor is use as power-gate transistor. This is because the library that available for Electric VLSI, C5 mocmos 300nm model only have one type of transistor. Therefore the reduction of power consumption may not be effective.

Lastly, Electric VLSI and LT Spice IV are not the ideal design tools to evaluate power consumption. This is because those tools do not provide function or method that can observe the power dissipation of the circuit. In order to analysis the power consumption, VDD and VSS have to be manually pull up as external source to observe. This may cause inaccuracy of testing.

4.2.3 Analysis on Design 1 and Design 2 Read Decoder

By referring back to Figure 37 (Design 1) and Figure 45 (Design 2), ideally Design 1 should be lesser leakage compared to Design 2 due to multilayers of power-gate transistor. As mentioned before, when transistor is being powered off, it acts as a resistor which will reduction the current leakage. However, from the table 4 and table 5 above, it shows that surprisingly Design 2 consume less power (about 10%) than Design 1.

There are few possible problem that cause this to happen. First, for multilayers transistor, the aspect ratio for the PMOS and NMOS need do double up for every extra layer in the circuit in order to ensure the driven current is big enough to supply for all the circuit.

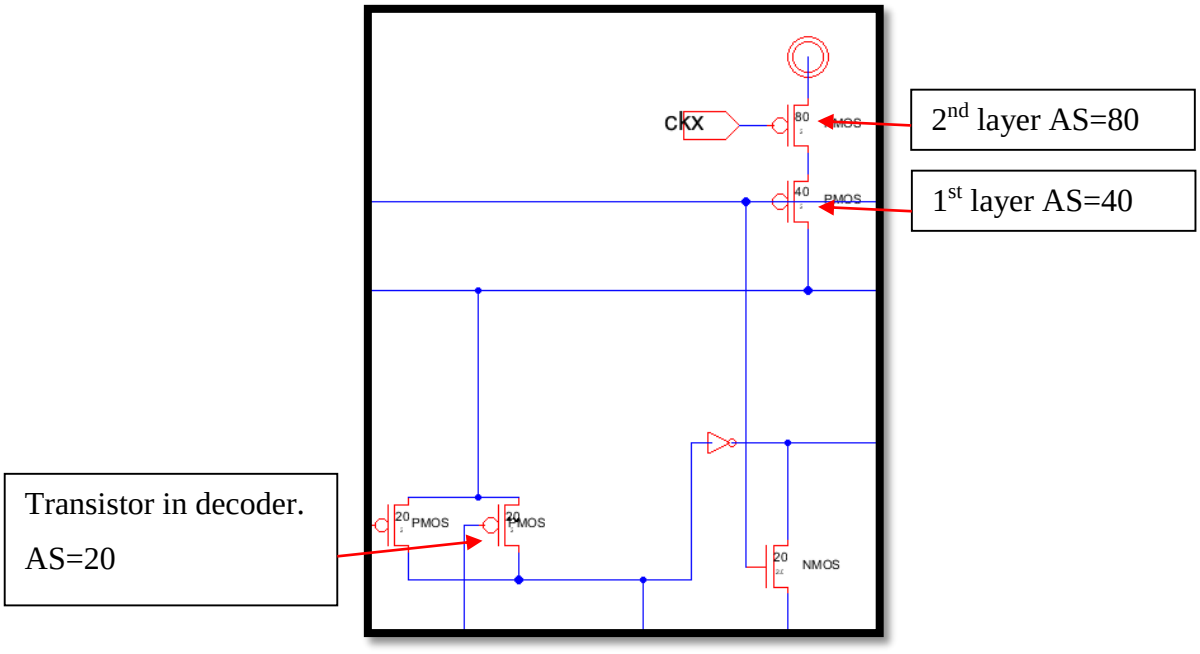


Figure 58 Aspect Ratio of transistor

From Figure 58, can be seen that the 2nd layer transistor aspect ratio is 4 times the transistor in decoder. As for Design 2, although there is only 1 layer of transistor (lesser resistance) but the aspect ratio is relatively smaller compare to Design 1. So this may be the reason why Design 1 is more power consumed than Design 2. Besides, as mentioned before, the type of transistor used as power-gated transistor may also cause this problem.

As for time delay, initially the Design 2 supposed to be faster compare to Design 1. From the test result show below, Design 2 is slightly faster than Design 1 as expected because of only single layers of transistor control by logic gate compare with multilayers transistor. Current did not need to pass through 2 level of power-gate transistor before can reach decoder circuit.

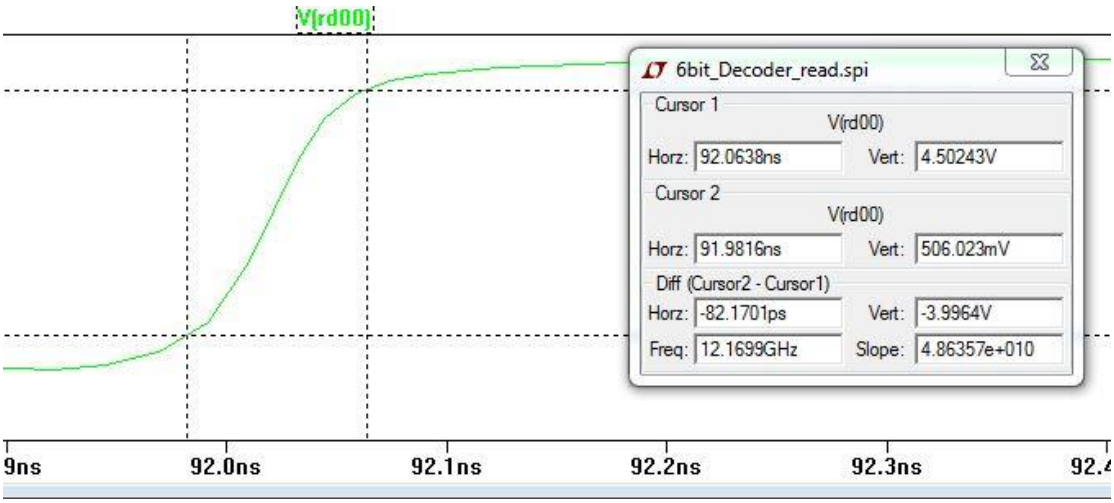


Figure 59 Time delay for Design 1

92.0638ns – 91.9816ns = 0.0822ns

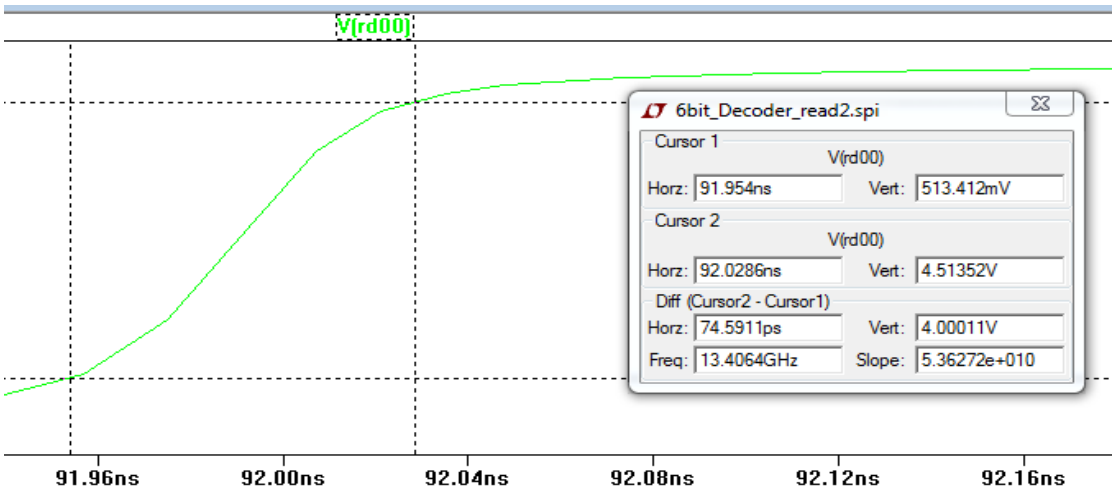


Figure 60 Time delay for Design 2

92.0286ns – 91.954ns = 0.0746ns

4.2.4 Analysis on Forward Addressing

Analysis on forward addressing implementation in decoder is main focus on time delay. The analysis is carry out by looking into the rising time of the signal when the particular entry is being call. By referring back to Figure 52, rd07 is the last entry of the first sub decoder block while rd08 is the first entry of the second sub decoder block. Forward addressing is implemented in here. Therefore, the rising time of signal transition of rd08 is study and verify for this test case.

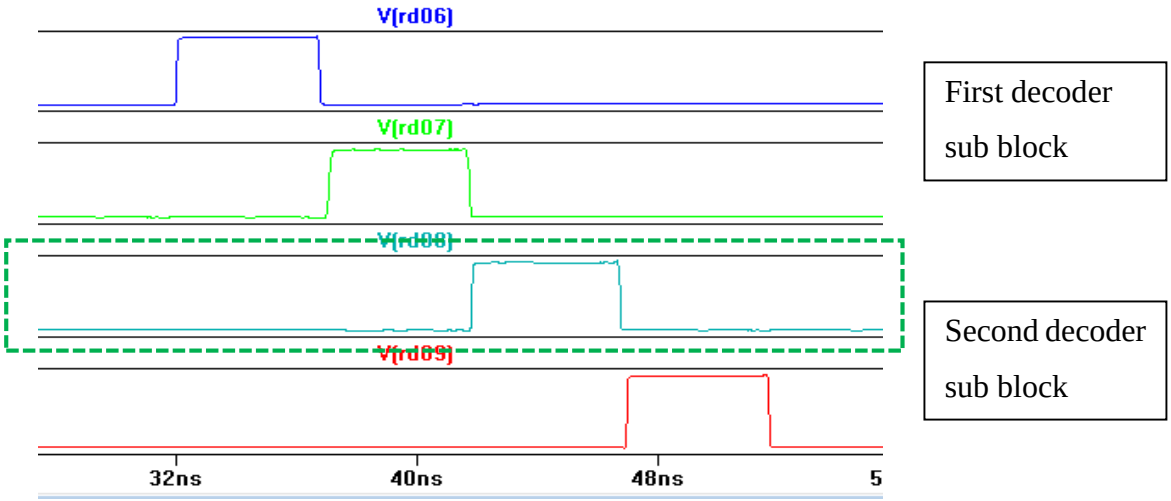


Figure 61 Timing diagram for Forward Addressing

By referring to the test result below, it prove that the implementation of forward addressing success to shorten the time delay. The design is not only shorten the rising time, the signal is also asserted ahead compare to decoder that without implementation of forward addressing. This is mainly because by implement forward addressing, the second sub decoder block is already powered up when the last entry of first sub decoder is being call. So when the entry of second sub decoder block is being call, the decoder block is already power up and can function simultaneously.

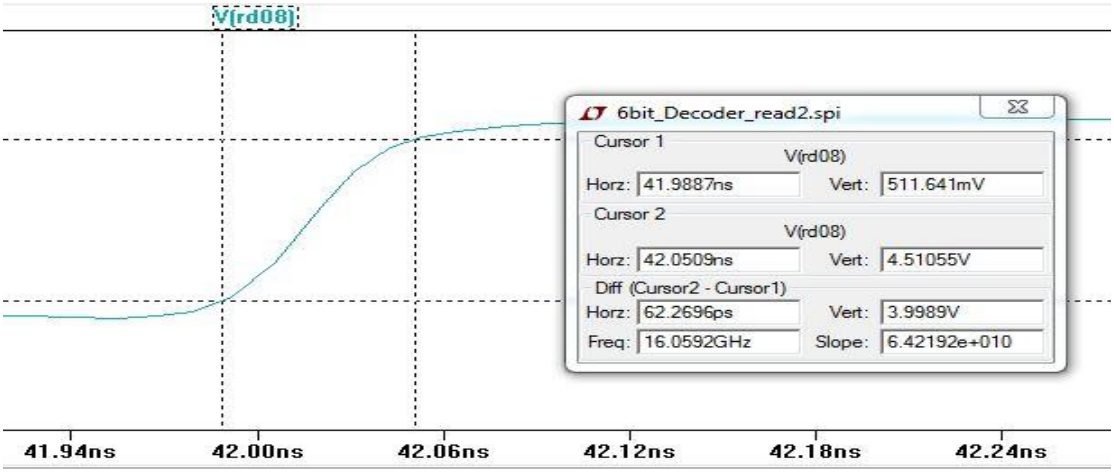


Figure 62 Timing Diagram for Decoder without Forward Adressing

42.0509ns – 41.9887ns = 0.0622ns

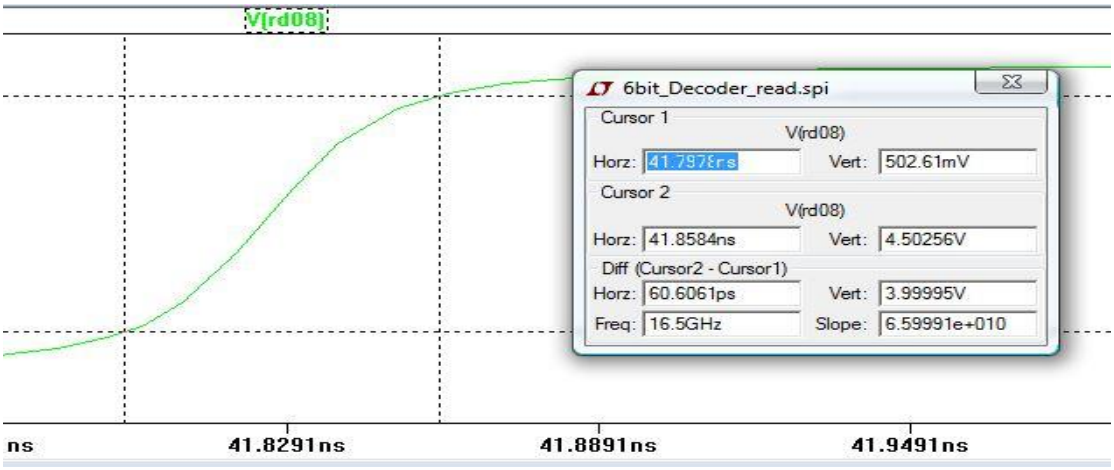


Figure 63 Timing Diagram for Decoder with Forward Addressing

41.8584ns – 41.7978ns = 0.0606ns

Chapter 5: Conclusion

The technology trends nowadays moving toward hand-held devices, some of the high-technology devices contain processor that not only having high performance, power efficiency is also a big consideration. Reduction of power consumption for IC manufacturer already being second priority followed by first priority which are cost, area and timing.

This project is proposed to overcome high power consumption issue to fulfil what the world need now. In order to reduce the power consumption, power-gated schemes for address decoder is proposed. In the same time to reduce the time delay that cause by adding power-gated to address decoder, forward-addressing is proposed. The proposed solutions are expected to improve on the power efficiency of address decoder in register file compare with existing design in conventional CPU micro-architecture.

First of all, after done all the verification and analysis on static power and time delay for proposed design, can conclude that the implementation of forward addressing in address decoder has improved the time delay as what expected. This is mainly because of the addition OR gate to power on the next sub decoder block when the last entry is being call. However, this may scale up the circuit of the decoder, as every sub decoder needed to add in an extra OR gate.

Unfortunately, after done verification on power consumption, the proposed power-gating designs did not outcome the result as what expected. The proposed designs not only fail to improve on power consumption, it also consume more power than

conventional address decoder. There are few problem that mentioned before that affect the result. Firstly, the lack of library for Electric VLSI which forced this project to work under 300nm environment will affect the power consumption. Next, there is no other low-leakage transistor available in C5 mosmos model to be used as power-gate transistor and the number of transistor increased in proposed design may also affect the power consumption. Lastly, the lack of verification power function or method in circuit design and evaluating tools may also cause inaccuracy to the power consumption.

There are some future work need to be done in order to improve the current design. So modifications on the proposed design is needed in order to improve the accuracy and performance of the design. First of all, all designs in project should work with a proper design tool that have specific functions on verifying power consumption. Next, in order to reduce the power consumption, this project should works in 50nm-100nm environment models instead of 300nm model, the model currently using. Furthermore, the environment models should also have different type of transistor or able to customize the property of transistor. So that the power-gate transistor can use lower leakage transistor to optimize the designs.

In conclusion, the proposed designs in this project may not be prefect. There are still a lot of modifications, improvements, and developments need to be done on this project in order to achieve low power consumption of existing conventional address decoder that used in register file without trade off the performance of address decoder.

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