LOW-POWER RF DESIGN:
SELECTIVE POWER-GATED AND DROWSY MEMORY ARRAY

By

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DECLARATION OF ORIGINALITY

I declare that this report entitled "**SELECTIVE POWER-GATED AND DROWSY MEMORY ARRAY**" is my own work except as cited in the references. The report has not been accepted for any degree and is not being submitted concurrently in candidature for any degree or other award.

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I would like to express my sincere thanks and appreciation to my supervisors, Mr. Kuek Chian Shiun who has given me this bright opportunity to engage in an IC design project. It is my first step to establish a career in IC design field. A million thanks to you.

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Finally, I must say thanks to my love one and my family for their love, support and continuous encouragement throughout the course.

ABSTRACTS

Register File is one of the sections which located inside CPU (Central Processing Unit) to increase the speed and efficiency of processor. However, high power consumption of register file has drawn the attention from most of the IC manufactures. In this project, some modified designs which mainly focus in memory array part are proposed in order to reduce the power consumption. By implementing power-gating and valid bit methodologies, theoretically, some unused part of memory array could be switched off or retained by lower power supply which can actually save a lot of power. By improving the power-efficiency of memory array, and cooperate with low power decoder and domino multiplexer, which can eventually come out with a register file with low power consumption without much degradation in performance.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Chapter 1: Introduction

1.1 Project Background

Register file, an array of processor registers in a CPU (Central Processing Unit) which can be found in a lot of high technologies today for example laptop, smart phone, tablets and so on. Nowadays, modern integrated circuit based register files are generally designed in such a way of fast static RAMS (Random Access Memory) with multiple ports. The way to distinguish the ordinary SRAM with such RAMs (register file) is that such RAMs are having separated ports for read and write process instead of read and write though the same ports.

As nowadays technologies become more and more advanced, the performance is everything that consumers and social concern about. In order to produce better and more competitive technology products, all aspects such as low power consumption, low cost, timing, high speed and so on, must take under consideration while we're designing the register file which is located inside the CPU that will directly influence the performance of the product.

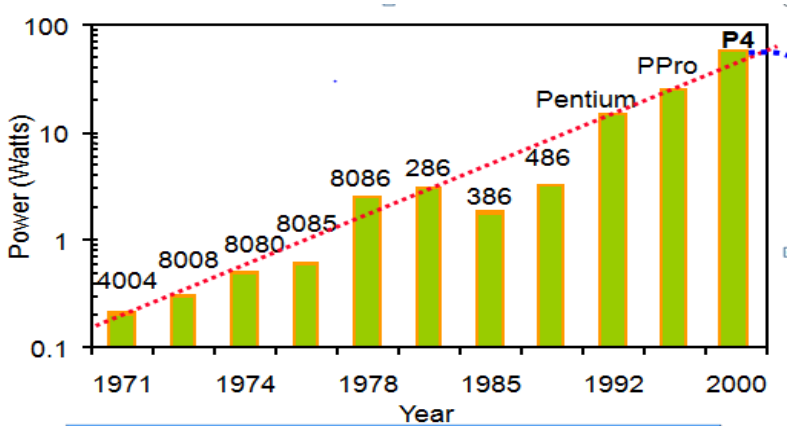


Figure 1 Power Trend

One of the major issues is power consumption. According to the research data from the figure above, power increased exponentially from year 1971 to year 2000, hence products design with low power are highly demanding in the market nowadays. Therefore in order to fulfill market needs, low power IC design for memory circuits which used in CPU architecture is one of the way, particularly, the memory array section of register file.

In fact, there's almost all IC manufactures of mobile or handheld devices have this power issue and has been trying to work it out. Let me give an example here which is Intel's register file used in 22nm Haswell architecture. Inside Haswell architecture, RF (register file) takes up to 27% from the overall power consumption. Memory arrays rank the highest leakage power in terms of Bitcell storage (as shown in fig 2) and the highest rank of dynamic power in terms of Write Bitline (as shown in fig 2).

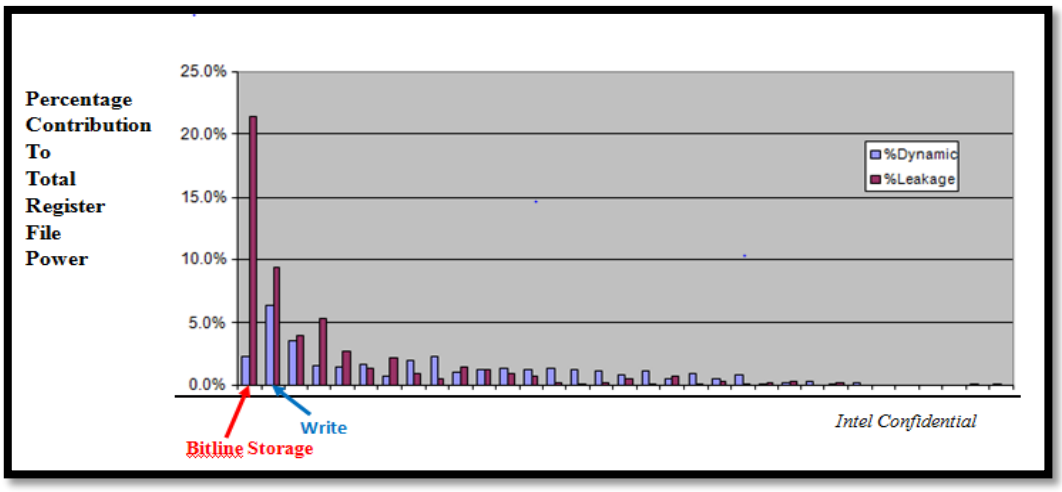


Figure 2 Power Consumption in Register File

Hence, in order to improve power efficiency, low power techniques have been introduced into the register file — memory array design.

1.2 Problem Statement

As mentioned in the section before, problem domain of this project is mainly study on the power consumption of the proposed designs which specifically design for low power consumption in order to overcome the power efficiency problem. Firstly, as we know user normally operates read and write process only on small fraction of the circuit. However, the design of memory array in register file nowadays will consume a lot of power due to the reason that no matter the memory cells are currently being accessed or not, all the cells will always supplied by power. It's like global switch concept, if powered off then will shut the whole circuit down.

Furthermore, the power loss is also very high in order to retain the storage inside the memory cell when it is in sleep mode. In other words, in actual practice we can use lower power to retain the data but due to there is only one type of power supply in the whole design, therefore, causing a lot of power dissipation when it comes to the case that only one or a few memory cell is actually running while others is only retaining the data.

Unused cell also consume power. The word unused cell is actually referred to the memory cell which is no valid data inside. However, the current design cannot differentiate which cell is used and which cell is unused, so the circuit will supply the nominal Vdd to the cell in order to make sure the cell works properly.

Lastly, power consumption caused by the writing process into the memory cell. That means the switching power either from 1 to 0 or from 0 to 1.This switching of data can actually cause a lot of power loss to the whole register file.

1.3 Project Scope & Objectives

1.3.1 Project objectives

The main objective of this project is to design a low power design over the originally basic design of memory array which located inside register file. The study on the improvement of power efficiency will be conducted by comparing the proposed design with the conventional design in order to verify the modified design. Basically, there are some sub-objectives in this project which are listed below.

Sub Objectives:

Firstly, enable nominal Vdd to be executed during operation based on ON-DEMAND cell, which means that partial off or supply low-Vdd to those memory cells which is not currently accessed. ON-DEMAND referred to the memory cells which intend to use for reading or writing process at that moment.

Secondly, reduce the leakage of memory cell during sleep mode. Next, entries with empty data will be identified by the specific circuit and will be powered down. This objective is actually refers to another condition, Data Validity that will be discussed furthermore in the section later. Basically, these three sub-objectives that mentioned here is to study the static power saving.

Besides that, we will also reduce the dynamic power of data-writing. This objective is to study the prospect of dynamic power saving and write-speed improvement if the targeted memory cell is powered down for a short while before new valid data is writing inside.

1.3.2 Project scope

According to the problem statements and the project objectives in the section before, now we will discuss on the project scope.

1. **Provide on-demand nominal Vdd to currently accessed memory cell while provide low-Vdd of power gate to off-demand memory cells.**
2. **Turn on drowsy mode which is low-Vdd to those cells that have valid data but is not currently being used, low power will be supplied to retain the storage inside.**
3. **Using valid bit to identify the empty cells and power off the whole cell to reduce power consumption.**
4. **Momentarily power down the targeted cell which prior to writing process to reduce write power (dynamic power).**

1.4 Innovations / Contributions

The main contribution of this program is the study of improvement on the power efficiency compared to the current based design.

Furthermore, partial power-gating by implementing valid bit which need to add one more bit for data to determine the validity of data. By using power gating, the system still can function and work well while almost all of the components inside are powered off.

Moreover, inside this project, drowsy mode will be introduced to the memory array. Drowsy mode which means by when the memory cell is not currently in used, we use lower Vdd to maintain the data that stored inside. By using this concept can actually save a lot of power in terms of data storing.

1.5 Technology Involved

There are a few of technologies and designs that involved throughout this whole project. The first one will be conventional register file design which will be used as a reference of some conventional design parameters and so on during the project implementation, besides that the conventional design also will be used for benchmarking and result comparing purposes. Secondly, Electric VLSI version 9.03 circuit-level design entry which is used for circuit design and some very basic error checking such as whether all the pins are connected, are there any redundant pins or arcs and so on. Following by LTspiceIV simulator for waveform, current, power checking after the design has been compiled and simulating by writing a Spice Code. Lastly will be the mocmos technology which consists of the pre-define design rules, C5_models which is 300nm scale for transistor-level (circuit level) design tools.

Chapter 2: Article Review

2.1 Low Power Techniques

As we know, power consumption can be divided into 2 main types which are dynamic power and static power.

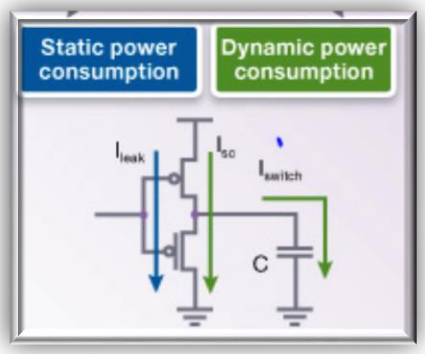


Figure 3 Static and Dynamic Power [Adapted from: Reference [11]]

Dynamic power (refer to Fig 3 green arrow) is the power loss when the device is active and the value of the signals are switching from one state to another. Dynamic power consists of switching power, which is the power consumed caused by the charged and discharged of output capacitance of gate, and internal power, which also known as short circuit power, caused by the short circuit or crowbar current when both NMOS and PMOS are on plus the internal capacitance.

Static power (refer to Fig 3 blue arrow), also called leakage power is the power that dissipated whenever the device is powered up. Static power is constant which means that it doesn't matter if there is a value changing or not, power will still consume. There are few types of source in the static power. First one is sub-threshold leakage, caused

by drain-to-source current when the transistor is not completely off. Next one is gate leakage which caused by the current from gate to substrate due to tunnelling Following by gate-induced drain leakage that caused by current flows from drain to substrate induced by high Vdg. Lastly, the most common one is reverse bias junction leakage which caused by minority carrier drift through generation of electron/hole pairs in depletion regions.

To resolve the power consumption issues, some general low power techniques have been introduced into technology industries to overcome the power problems. Those methods which have been proven efficiency in reducing the power dissipation into considerable amount, consists of clock gating, multi Vdd, stack transistor and so. Now, we will briefly introduce these techniques.

2.1.1 Clock Gating

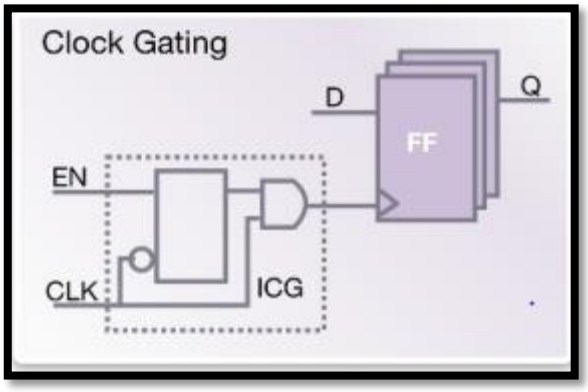


Figure 4 Clock Gating [Adapted from: Reference [11]]

The very basic idea of these methods is when the new data that ready to be written inside the circuit is being identified that exactly same with the previous data inside, clock will be turning off. In other words, clock will only turn on when it is needed. In clock gating, it is implemented by adding an enable signal to gate the clock signal as shown in the figure above, when the enable signal is 0, no dynamic power will be consumed as the clock is being shut off.

Initially, there are two types of clock gating available which are latch-based clock gating and latch-free clock gating. Latch-free clock gating means using simple logic AND or gate to implement this techniques. Latch-based clock gating will use a level-sensitive latch to hold the enable signal from the rising edge of clock until the falling edge of clock, which is more widely use compare to latch-free based in order to solve power-efficiency problem.

2.1.2 Multi-Voltage (MV)

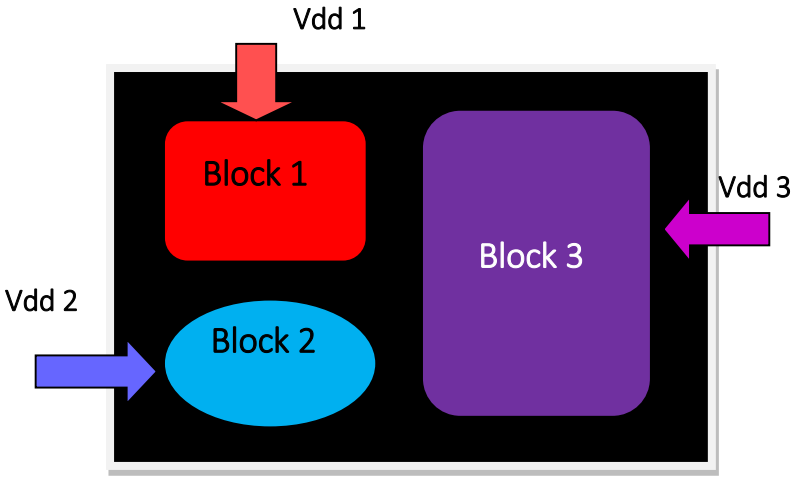


Figure 5 Multi Vdd

Dynamic power is directly proportional to power supply (Vdd). This method can be implemented through assign different voltage levels to different blocks/areas based on their demands respectively. Low supply is good enough for those low demand blocks in order to accomplish their task. In other words, the circuit should design in such a way that provide high supply to those specific areas which require higher voltage to accomplish their specific task and produce better result while other portions will be connecting to lower power supply. Eventually, it improves power-efficiency significantly.

2.1.3 Power Gating

When the particular block or circuit is not being used, it's advisable to turn the whole block/circuit off in order to reduce leakage power. Power gating is one of the effective ways to overcome this problem. Power gating is also one of the low power techniques. If a comparison made between power gating and clock gating, power gating will affect more to the design architecture. Shutting down the current flow of whole unused block will reduce a lot of leakage power since the power dissipation of the area is reduced to 0. However, there is a limitation of power-gating, as power gated modes need to be executed safely for entering and exiting, which will introduce time delay to the whole circuit.

For this power gating methods, the most basic form is implemented by adding an external switch power supply. This way is actually directly apply to the circuit to achieve long-term static power reduction. As for short-term static power reduction, internal power gating is more advisable which will only shut the unused block off for a very short while.

Normally, power gating uses low-leakage PMOS and NMOS transistor as header and footer switch respectively (refer to Fig.6). The reason why PMOS will be as a header switch is because it drives good 1 and poor 0 while NMOS drives good 0 and poor 1, thus PMOS connected to Vdd while NMOS connected to Vss. These so called power switches is added to supply rails to shut-down logic. Header switch can use to shut off the power supply to parts of a circuit which in standby mode or sleep mode (drowsy mode) while footer switch is normally used as sleep transistors. Generally, these two

type of switches will be used together in order to implement power gating in the circuit design.

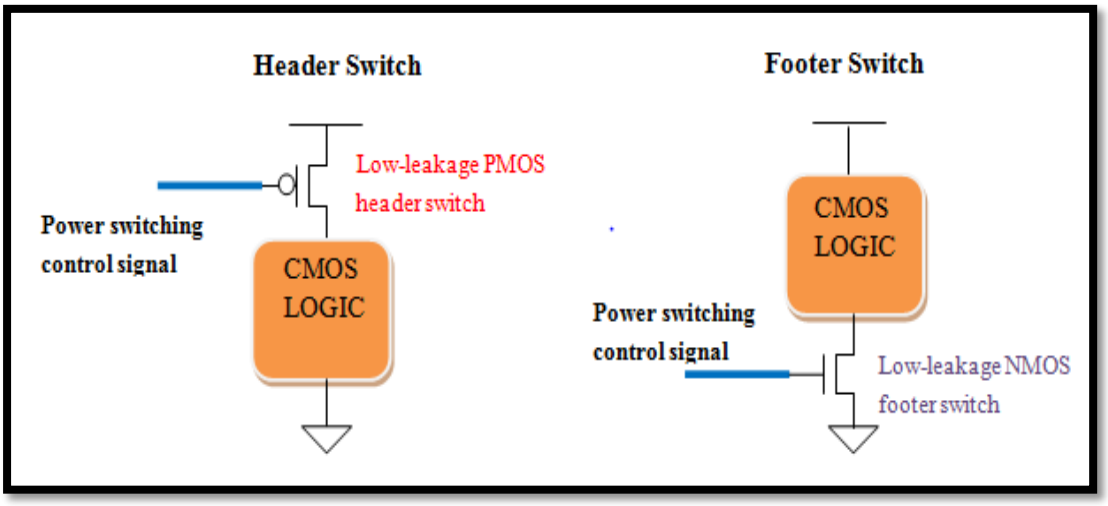


Figure 6 Header and Footer Switch

Now, let's consider a simple CMOS log with pull up and pull down network as shown in Fig 6 with directly connect to power supply and ground, which means that the circuit will continue consume power even though they are not currently processing. Unlike clock gating, instead of reduce dynamic power, power gating reduce leakage power. By using the concept of header and footer switch, circuit in Fig 6 has been modified into Fig 7 to reduce leakage power.

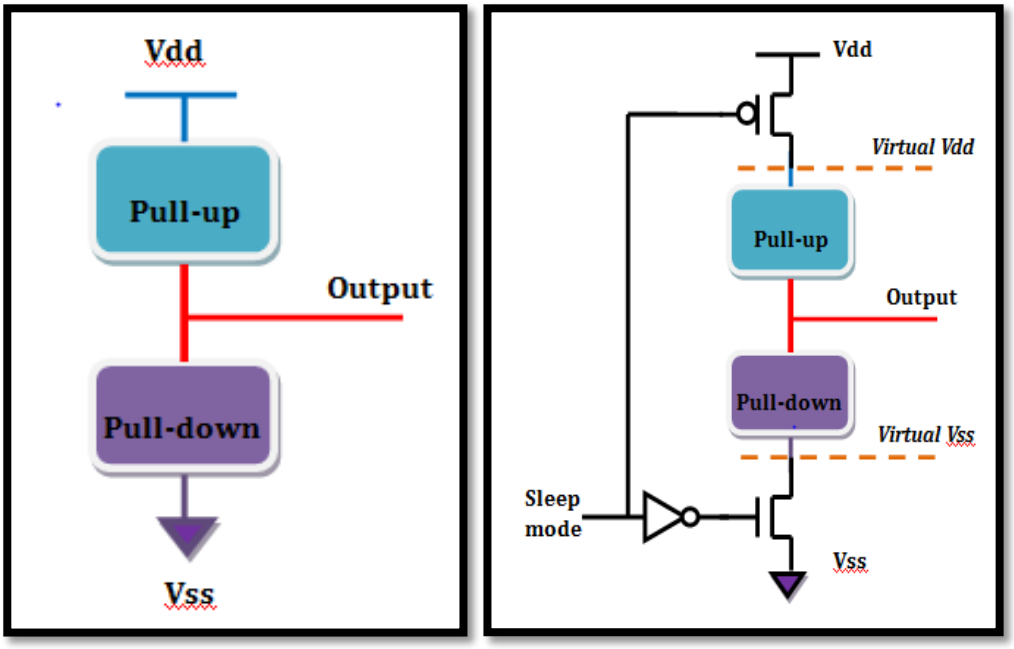


Figure 7 Sleep transistor

When sleep mode is disabled, means sleep mode equals to 0, those power switches will be turn on, the logic circuit still function as the same. While when sleep mode is enabled, sleep mode equals to 1, power switched will be switched off, virtual Vdd and virtual Vss will not disconnected from power supply, thus no leakage power is consumed.

As we know, transistor threshold voltage will directly effect on the power dissipation and the speed of the design. Leakage power consumption is primarily resulted from unwanted drain-to-source current between the transistor channels when the transistor is powered-off but it isn't fully off. The variation of threshold voltage of transistors will strongly influence the amount of leakage current loss due to the reason of leakage current increase as threshold voltage decrease as shown in Fig 8. Thus, due to power

consumption is directly proportional to leakage current (I), when leakage current increase, power loss increase. Decrement in transistor threshold voltage will cause the increment of power dissipation.

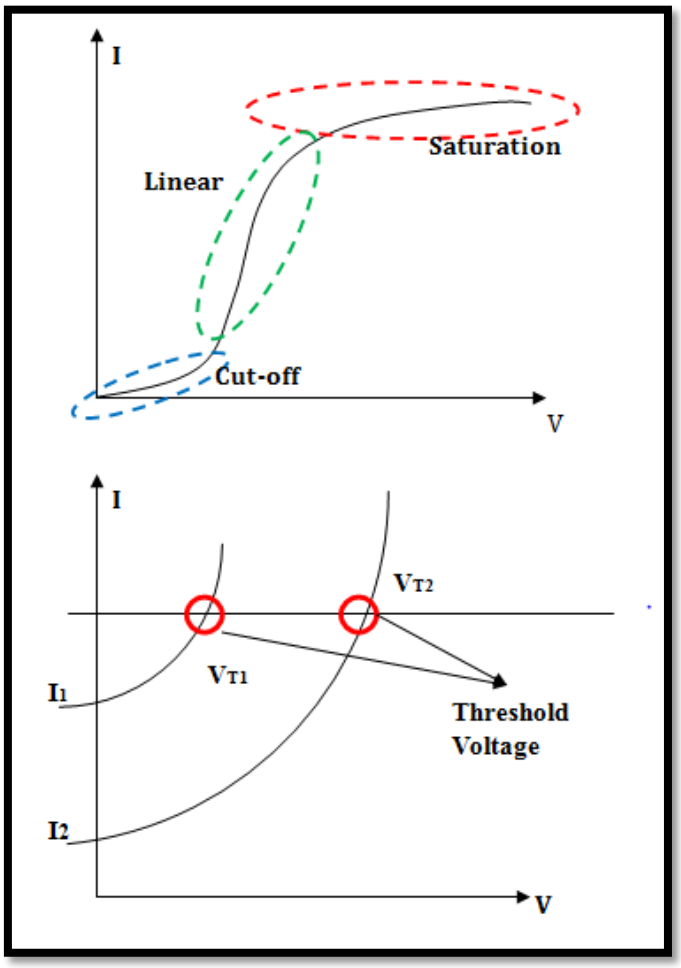


Figure 8 (a) Transistor Operating Regions

(b) The relationship between Threshold Voltage and Leakage Current in cut-off region

Low leakage transistor as mentioned before, is actually referred to high threshold voltage transistor which means that the transistor switched slower but leakage power is also lesser than others. However, there is also nominal transistor which is powered off faster than low-leakage transistor, but, at the same time leakage power also increase compared to low-leakage transistor. The following transistor type is high-speed transistor which is powered off even faster but leakage even higher compared to another two.

Basically, in a complete design, different type of transistors will be choosing for different applications based on the circuit requirement and must make a balancing between performance and power. Normally, in a complete CMOS design, low-leakage transistor is used for power gating purposes while nominal transistor is used for general logic circuit design for example AND, OR gate and so on. And for the high-speed transistor, it's mostly used in those critical paths which is requiring on timing and speed. Due to overall Vt variations throughout a full design has such a significant effect on performance and power dissipation, therefore choosing the right type of transistor is very important.

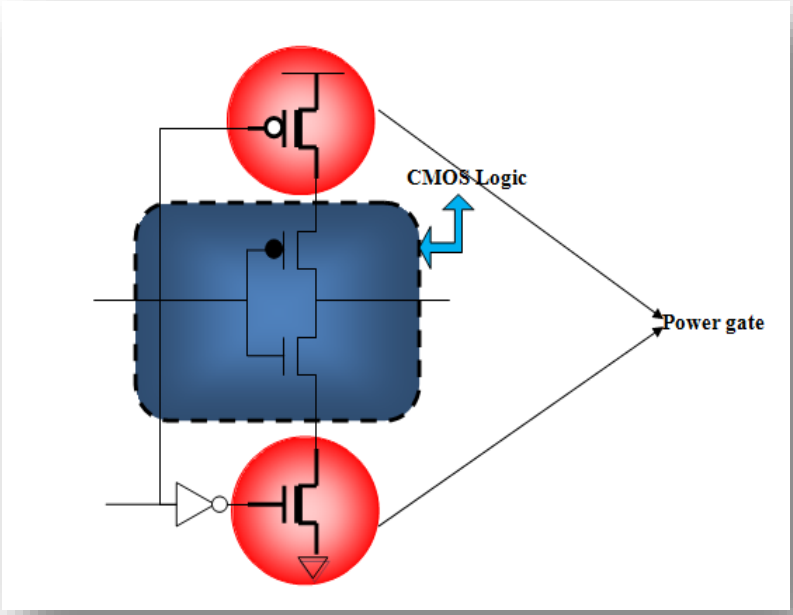


Figure 9 MT-CMOS

Let's assume the CMOS logic in Fig 7 is an inverter which is composed by one pmos and one nmos as shown in Fig 9. According to Fig 9, the power switches are both using low-leakage transistors to reduce static leakage power. While the CMOS logic in between them are using nominal transistors to achieve fast switching speed. Undoubtedly, this kind of transistor arrangement will eventually improve the overall speed and meanwhile reduce leakage power.

2.2 SRAM and Register File architecture

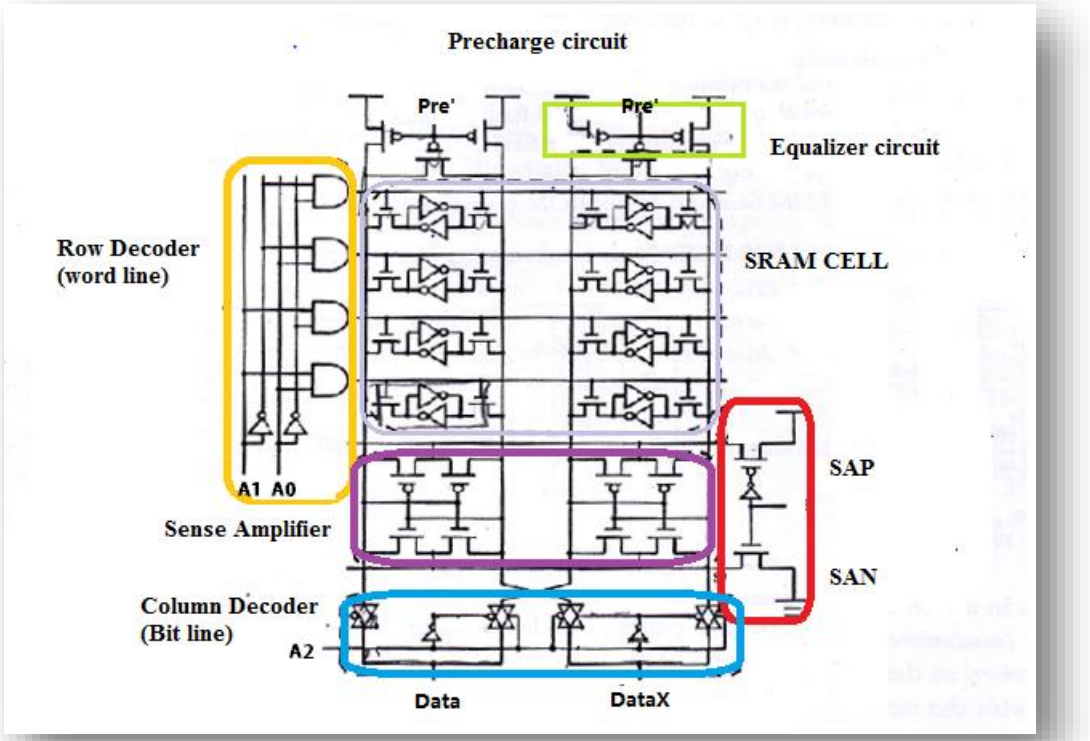


Figure 10 SRAM architecture [Adapted from: Reference [16]]

Basically, SRAM refers to Static Random Access Memory which is one of the volatile types of memory; it will lose its data after power is off. Compared to another type of memory, DRAM, SRAM is faster, but low density, high power consumption, and costly. Normally Static RAM will be using as cache memories for frequent used data or instructions storing. Typically, the general SRAM consists of few basic components which are SRAM cell array, decoder, sense amplifier, pre-charge circuit, equalizer circuit and also column circuitry.

First of all, memory array is composed by many single bit 6T SRAM cells. Each cell can only hold one bit at a same time, and it's for read and write operation. As shown in Fig 11 below, basically it's contains an back-to-back inverters in order to retain the data, one word line to activate read or write process, and two bit lines which is carrying complementary data value(input) Besides, in 6T SRAM cell, the read and write operation is through the same port.

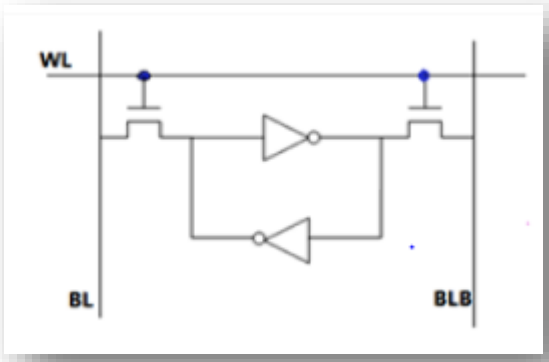


Figure 11 6T SRAM cell

Next one is the row decoder which is an address decoder with one-hot features to activate one row of memory array. One-hot means by among all of the outputs, only one chosen line will be asserted high while others asserted low. And the 'ON' line is to activate the word line for memory array to process read write operation. The address decode is actually using Binary Decoder which is 2^n decoder with n-input and 2^n outputs for example 2-to-4 (shown in Fig 12) or 3-to-8 decoder. As for the design with large amount of inputs, normally pre-decoder will be introduced. The advantages are save area, save wires and also shorter time delay.

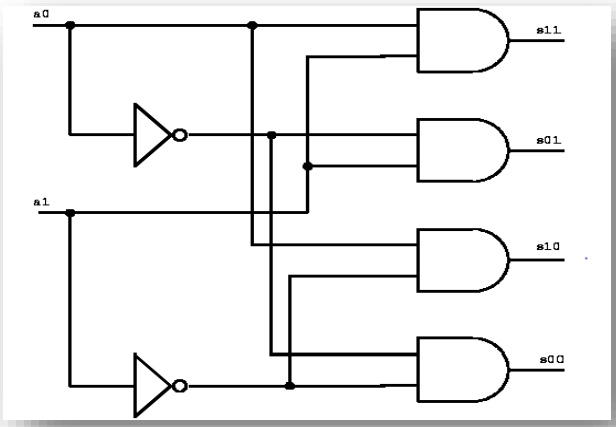


Figure 12 Binary Decoder

The following component is sense amplifiers which composed by two inverters connect back to back which can regenerative feedback. There are 2 type of sense amplifier (Fig 13), the first one is differential pair sense amplifier and the second one is latch-batch sense amplifier, the main difference between these two is that latch-based sense amplifier contains clock signal to control the connection to the power supply. The function of sense amplifier in SRAM design is to ensure fast and full rail-to rail transition of bit lines during read operation. In the full design as shown in Fig 10, noticed that there is a SAP and a SAN beside the sense amplifiers. Actually, SAP stands for Sense Amplifier Positive and N for negative, they function as the controller of the power supply to sense amplifier, which can used to temporary shut the sense amplifier down during pre-charge phase to ensure both bitlines could achieve same voltage level for data-reading purposes.

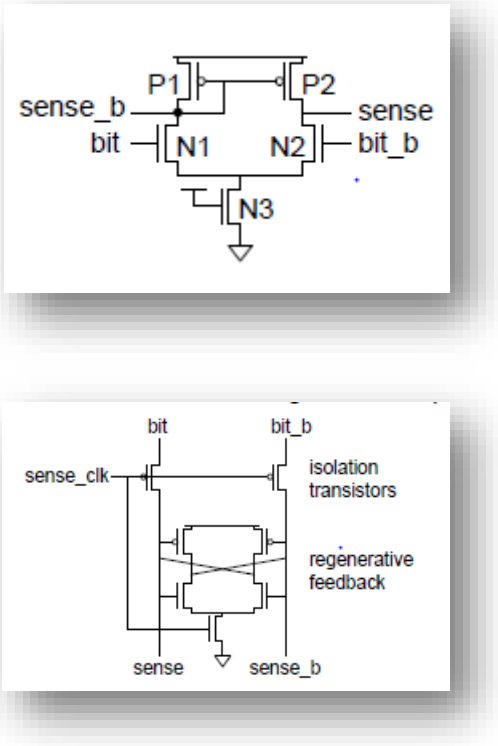


Figure 13 (a) Differential pair sense amp (b) latch-based sense amp.

Next one is the column select circuitry which is used to determine which column of memory array is activated for read or write operations. There are alternative ways to design for column circuitry for example tree decoder (fig 14), multiplexer with pass transistor (fig 15) or transmission gate, general decoder with pass transistor and so on. The column circuitry in Fig 10 is a multiplexer with transmission gate to choose between columns. This circuitry allows multiple bitline to share common amplifier.

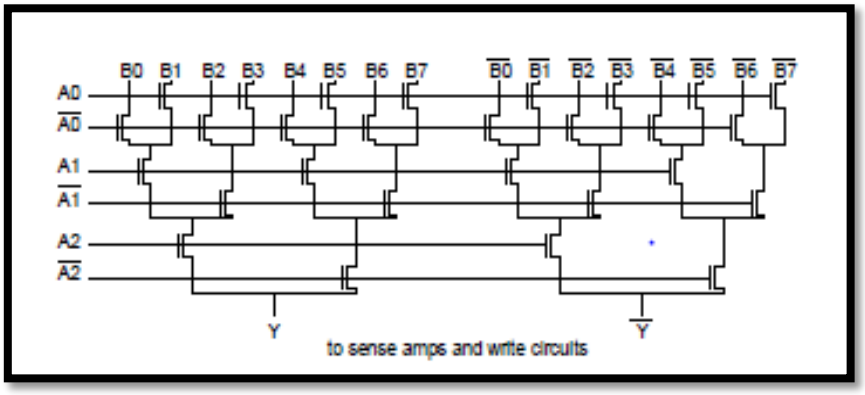


Figure 14 Tree Decoder Column Circuitry

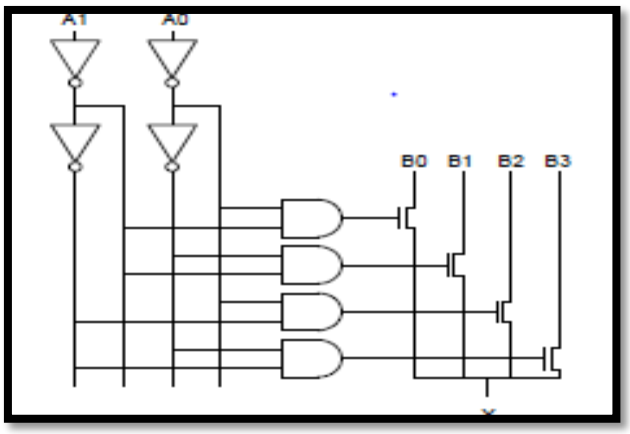


Figure 15 Simple Multiplexer with pass transistor

Next, following by the pre-charge circuit which is used to charge bit lines to 'high' especially read operations proceed, to make sure fast reading of bit 1. Lastly, the equalizer circuit is used to ensure that the voltage between both bitlines is exactly the same to minimize voltage variation for read purposes.

Thus, this is basically how it works, during read operations, pre-charge circuit will charge all bitlines to Vdd (high), equalizer circuit will make sure both bitlines are exactly the same voltage, next, output from decoder will cause one of the word lines asserted high, potential of bitline of the accused memory cell will be slowly pulled down until a defined level, The bitline capacitance will affect the ROC(rate of change) when the pull down operation during read process Then, column circuitry will select one of the rows, finally data will be output after amplifying by sense amplifier. The sense amplifier will actually differentiate and tell which cell to store a 1 or 0. The sensitivity of sense amplifier will directly affect the speed of read operations.

As for write operations, external data from write amplifier will cause a swing differential voltage on the bitlines. Only one bit line will go high, another bit line will be the inverse potential value. As similar to read operation, since Static RAM operate read and write process through the same port, one of the word lines will be activated. Bitlines will overwrite the value in the cell and stored inside the cross-coupled inverters until the new data comes in. Careful gate sizing of SRAM cell is very important for write operation because the value of bitline has to be stronger drive strengths in order to force the on-demand cell has the same logic with bitline.

From research paper reviewed, the author has proposed some solutions in order to improve the performance of SRAM architecture in terms of speed and also power economic. The first method that being introduced are circuit partitioning which divide the memory array into 2 parts and use same wordline driver for it, as compared to only one single core memory array, the capacitive and resistive load are reduced by half. The second method is fast sensing by using a latch type sense amplifier which is able to

detect a very small bitline difference and give a high gain factor. However, a problem rise up is that when the sense should be switched on after the detection of the bitline difference by considering also all other factors like temperature, voltage and so on, hence, in order to switch on the sense when the required bitline is obtained, the self-timing technique is introduced to maintain the required bitline difference. Lastly, in order to gain in speed, dual Vth usage is proposed which is implemented in such a way that assigns different threshold voltage to different part of circuits accordingly.

After the discussion on the SRAM architecture, register file is focused in this section. Basically, register file has the similar function with SRAM. The main difference between register file and SRAM is the read and write port. Ordinary SRAM processes read and write operation through the same port while register file has dedicated port for read and write operation respectively. Hence, register file architecture will not has read and write conflict. Moreover, register file tends to design in a smaller size than SRAM.

2.3 Memory Array Architecture

In order to discuss about memory array, the very beginning will start with the most basic unit of SRAM—a single bit cell. Basically the most typical memory cell is 6T memory cell which shown in Fig 16. It basically composed by 2 pull up PMOS and 2 pull down NMOS transistors as two cross-coupled inverters and 2 NMOS access transistors to access SRAM cell during read and write operations.

The cross-coupled connection is for retaining data purposes which will continuously create regenerative feedback that allow the SRAM cell to indefinitely store a single bit. This configuration is actually one R/W port which can be used for read/write process, but not both execute simultaneously. The write process is activated by asserting Write Word line (WL) while read process is activated when Read Word Line (RL) is asserted high. While both of the bit line (BL & BLB) are used to deliver write data or send out read data during read and write operation.

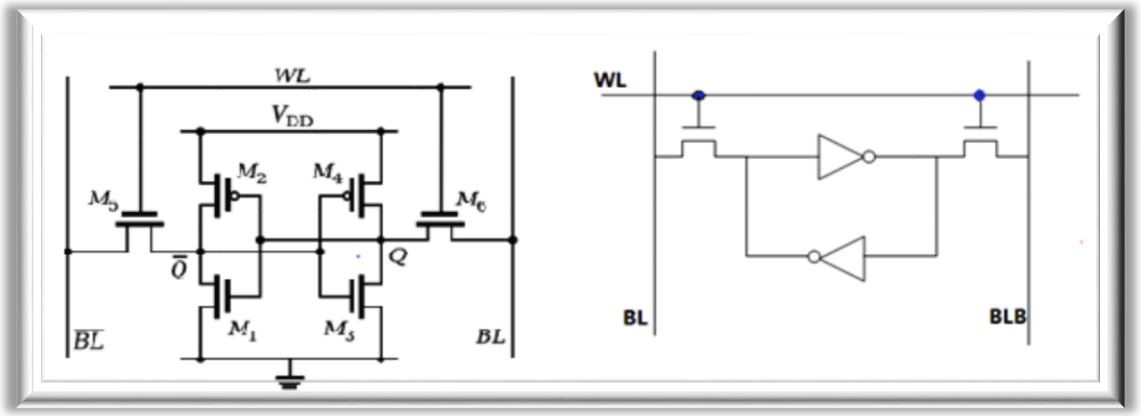


Figure 16 gate-level and transistor level for 6T SRAM cell

Nowadays, the memory cell used in industries today is the improved version of conventional structure 6T SRAM cell, which is 8T memory cell (refer to Fig 17). The 2 new extra transistors are actually the read port for each SRAM cell.

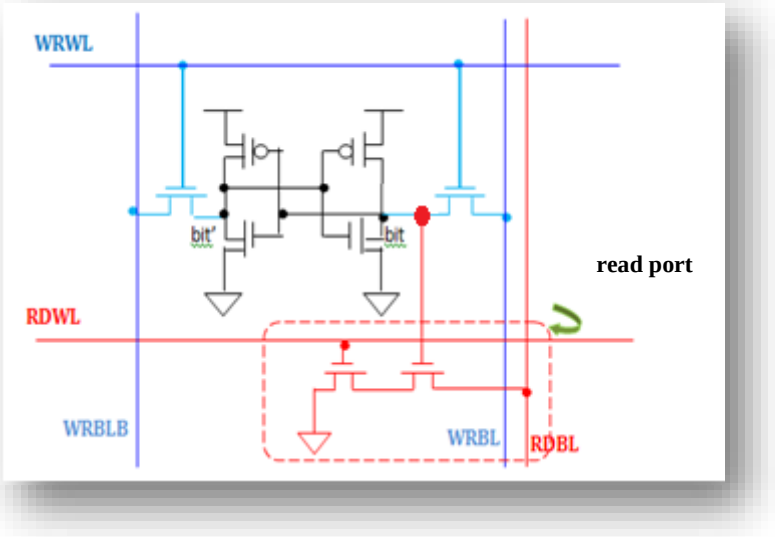


Figure 17 8T Memory Cell [Adapted from: Reference [11]]

Typically, the currently existing 8T memory cell, the sense amplifier (read port) has been dissolved into each cell, thus, providing a different path for read process as compared to write process. This design eventually will improve the performance on read operation but increase the amount of transistor compared to old structure which only contains one read port and shared by the same column of memory cells. Sense amplifier can be treated as a 'half inverter' which comprising only NMOS as a pull-down circuit, thus only be able to drive a strong signal 0 when bit line go high and provide signal high-impedance when bit line go low. The output from read port is connected to the read bit line which will send and activate the next circuits.

Different from other industries, the well-known Intel processor design is actually using 10T SRAM cell. Here is the concept of stack transistors technology brings in which is also considered as one of the low power techniques. Stack transistors mean using 2 or more PMOS connected in series. As compared to 8T memory cell, 10T may uses up more area throughout whole circuit and cause redundancy issue, however, the arrangement of 2 PMOS connected in series is actually helps reduce the power dissipation.

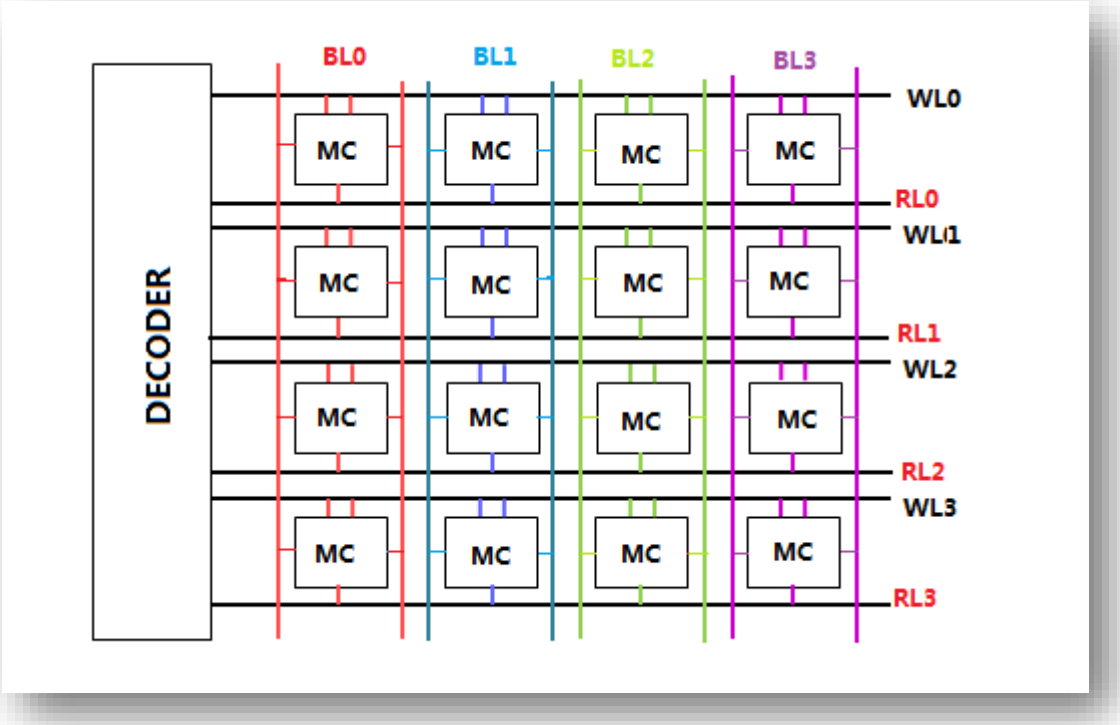


Figure 18 Memory Array

To support the operation of register file, a group of single bit data SRAM cells has to be connected together (as shown in Fig 18). Each memory cell are connected to the row's word line (WL) and the column's bitline (BL). WL in this register design is used to control when the entry is accessed for read or write operation. Both write and word lines are actually controlled by decoder.

When one of the word line (WL) for example WL0 asserted high, all the memory cells that connected to that word line will be activate. For the write process, the access transistors that connect to the WL0 are enabled. External valid data will force the memory cell to have same logic value with the bitlines. New data is being written inside, while the WL0 word line de-asserted, the value inside will follow the previous data and retaining in pair of inverters, act like a hold function.

While for data-reading process, read word line (RL) must be asserted high to enable read port, basically the pull down circuit in read port will output a 0 and force read bit line (RDBL) to go low and the following operation will be controlled and accomplished by Domino Multiplexer together with pre-charge and keeper circuit.

From research paper reviewed, the author proposed the solutions in reducing leakage power without degrading the performance of SRAM. The author stated that the design of 6T memory array involve complex trade-off between 6 factors which is minimize cell area, obtain good cell stability with minimum voltage, goof soft error immunity, high cell read current to minimize access time, minimum word line pulse and low leakage current. There are many interactions between those factors, hence, when the solutions that come up fix some of them, another problems such as add cost in power

and so on rise up. Indeed, another method 8T is being introduced which definitely provide better minimum voltage and faster access time compared to previous 6T methodology. However, the leakage power consumption is much higher due to the 2 extra nMOS which located in read port if the stored data is 1.

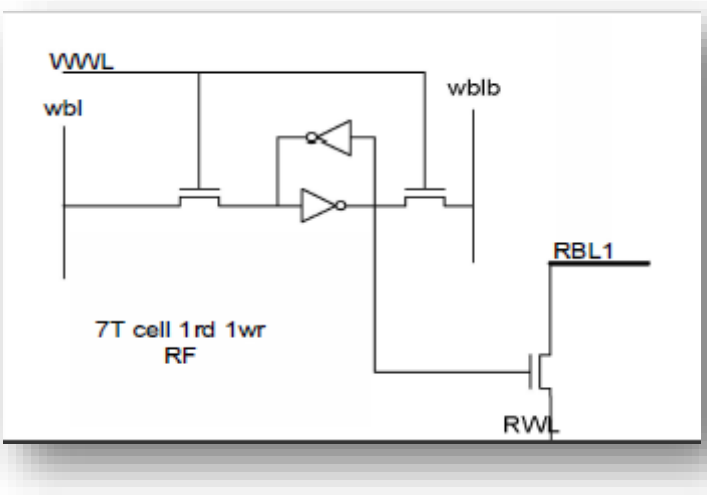


Figure 19 7T memory cell [Adapted from: Reference [17]]

Hence, in this research paper, the author proposed 7T based solution in order to strike a balance between lower power consumption and acceptable performance. In order to eliminate read port leakage power, the memory cell is proposed to design in such a way that shown in figure 19, which eliminate one of the nMOS in read port, and cause the read word line and read bit line has same voltage level during ideal mode. The author used Hspice to check and validate the functionality of proposed solution and result shows that the leakage power saving compared to 8T cell is data dependant which ranged from 30% to 50% for the same technology and same threshold voltage used in both methods, but it saves up to 12% area compared to 8T memory cell.

Chapter 3: Methodology

As mentioned in the project objective and scope, generally, the solutions that proposed to solve those problems is by using power gating techniques and Drowsy mode. These 2 modes will be enabled by considering the on-demand and validity of data. Data validity is implemented by adding a valid bit to identify empty cell which refer to the entries with empty data.

Now, let's consider the 2 conditions, on-demand and data validity. Obviously, data validity has higher priority than on-demand. If entries with data and the cell is currently accessed, normal Vdd turn on. However, if entries with valid data, but the memory cells are not currently accessed, will be switched to drowsy mode, in other words, low-Vdd will turn on. When the data is invalid, memory cell will be powered down. Table 3.1 shows how the conditions affect the way to enable nominal Vdd and low-Vdd.

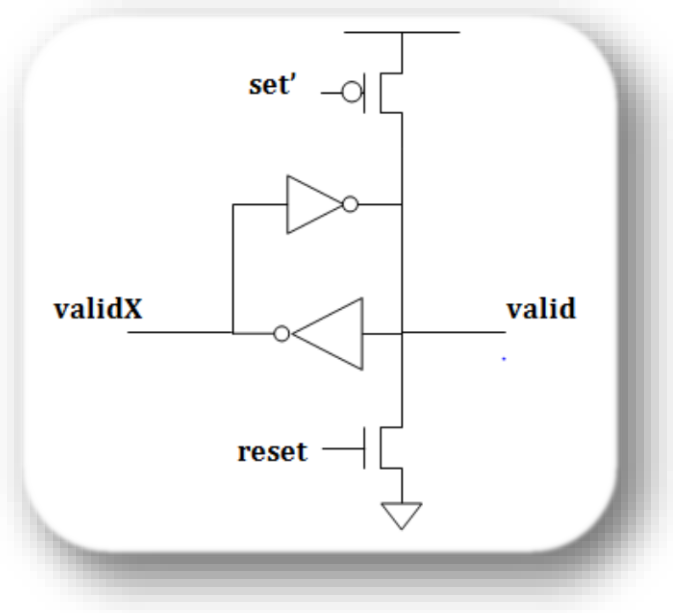
Conditions	LowVdd	Vdd
Data Valid & On Demand	Off	On
Data Valid & Not On Demand	On	Off
Data Invalid & don't care	Off	Off

Table 3.1

3.1 Valid bit

In order to implement power gating in the design, the most basic term is the power switching control signal as shown in Fig 7 before, which is used to activate header/footer power switch. Hence, in this proposed solution, valid bit is the control signal throughout the whole register file design which is generated by memory array. Basically, the valid bit is implemented by simply adding one bit to the data that being written into the memory array. In this proposed solution, the valid bit generator circuitry is controlled by set and reset and eventually, it will output to memory array, address decoder and also domino multiplexer to activate power gating.

Valid bit generator circuitry can be designed as follow.



The general idea is: when set Vdd will be going into the conventional structure and Vss will be providing a 0 when reset. Thus, if set is 1 reset is 0, PMOS is turned on, and

Vdd output a 1 to valid while after inverter, validX will be a 0. But, what if set and reset happen simultaneously? There's a problem of contention which causing a direct path from Vdd to Vss. A better solution has been introduced in Fig 19 which can make sure there is only one power source either Vdd or Vss can turned on at a same time.

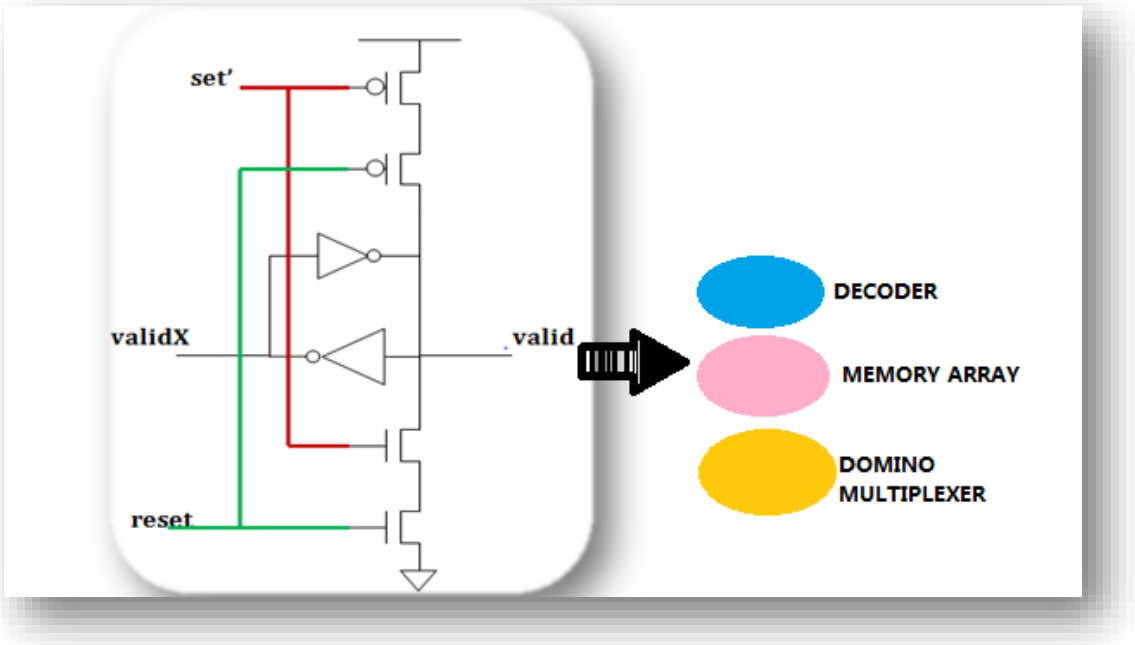


Figure 20 Valid Bit Flag

From Fig 20, if set is asserted high, and reset is asserted low, 2 PMOS above will be turned on, provide a 1 to valid and a 0 to validX. On the contrary, if now circuit intend to be reset which set is asserted low, reset asserted high, 2 NMOS in the bottom will be turned on and provide a 0 to valid and vice versa to validX. Still, as mentioned before, the valid bit will connect to decoder, memory array and also Domino Multiplexer.

3.2 Power gating

Typically, there are 3 modes in this proposed solution, which consists of drowsy mode, powered down and active mode. This section shows the way to activate and implement them.

Drowsy mode is actually sleep mode, which just need to provide low power to retain the data that stored inside the memory cell. Active mode is when read or writes process is required by the user. Lastly, powered-down mode enabled when the memory cell has no valid data which it definitely doesn't need any power supply. Thus, nominal Vdd still will include as similar to the older structure, but now low-Vdd comes in, which will provide a value lower than nominal Vdd but higher than threshold voltage.

For power gating, PMOS acts as a header switch, as the figure shown below (Fig 21a), header switch in this solution will be using to choose between nominal power supply and low power supply.

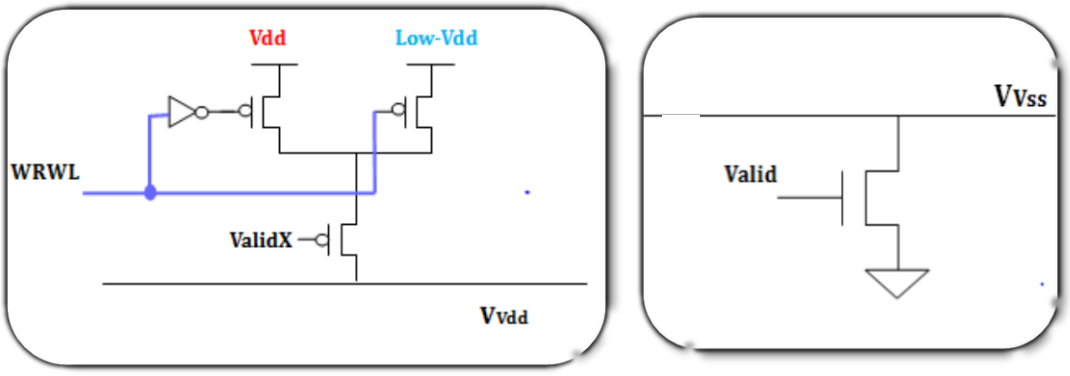


Figure 21 (a) Header Switch (b) Footer Switch

For header power switch, besides the valid bit, write word line also will be one the of control signals. While for footer NMOS power switch will be an NMOS connected ground, controlled by valid bit (as shown in Fig 21b).

3.3 Proposed Solutions

Due to the power gate and valid bit discussed earlier in order to solve power-efficiency problem, an older structure 8T memory cell will be modified into Fig 22, which use back 6T SRAM cell structure, but, the inverters inside instead of directly connect to nominal Vdd, the PMOS will connect to Virtual Vdd in Fig 22. While at the same time the same row of memory cells that connecting to the same word line will be connected to a same power gate (Fig 22) togther to share the Virtual Vdd. Moreover, footer power switch will be either added to each of the memory cell respectively(fig 22) or the same row memory cells share only one footer but the footer switch NMOS must be very large gate size in order to drive a strong signal (fig 23).

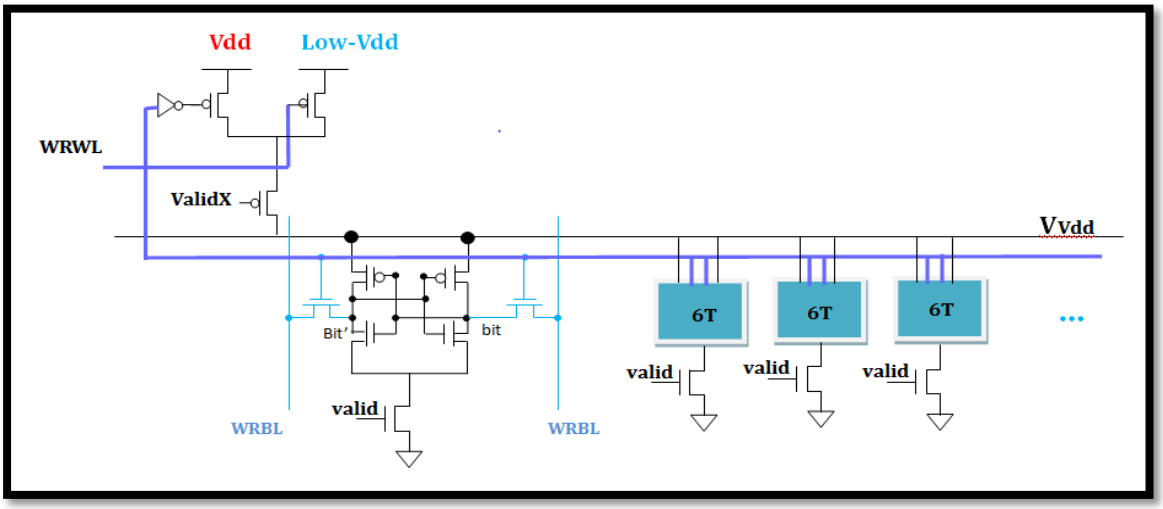


Figure 22 One single row of memory array

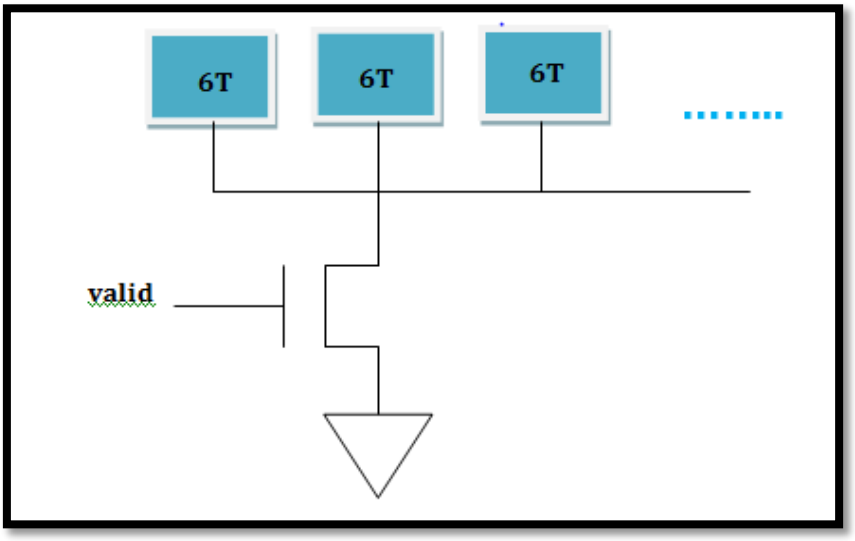


Figure 23 shared footer power switch

When WRWL asserted high, means that there is a new data ready to be written inside the memory cell and replace the previous data, thus we need to provide nominal Vdd to the targeted memory cell in order the accomplish the data-writing operation. Since PMOS only can be activated by a 0, hence, an inverter needs to add right before the transistor, the PMOS gate opens, Vdd flows in. Footer switch will drive a 0 to the circuit also. If valid is asserted high, means that validX is a 0, thus, output a 1 to the virtual Vdd. Memory cells activated, data are written inside. That's the case for on-demand and valid data.

However, for those not on-demand cells, the write word line from decoder will be in low state which will activate the gate for low-Vdd and deactivated the gate for Vdd. If there is data valid, similar to the operation before, low Vdd will be output to the virtual Vdd which will supply power to the memory cell, same case goes to footer switch which

will provide a 0 to Virtual Vss. This proposed solution solve the problem in current design which cause high loss on leakage power for supplying those memory cells which is not for write/read purposes but only need to retain the data inside.

Furthermore, the entries with empty data will be identified by valid bit, when data is invalid, valid bit output a 0, PMOS and NMOS power switches turn off, whole memory cell will be shutting down thus can reduce a lot of power consumption. It is because when those unused cells are powered-down, their leakage powers are considered 0.

The following case is the data-writing process. As the target is to reduce write power, the solution proposed here is momentarily powered-off the targeted cell. The protocol is targeted memory cell go offline (reset valid bit) → write data ready → write word line activated → set valid bit, valid data write inside the memory cell. Initially the momentarily power off is to let the data which stored inside the target memory cell previously float between 0 and 1(as shown in Fig 24). Immediately, we turn it on again, now the value swing in between, it will take almost smaller amount of power go to either 0 or 1 instead of using more power switch to 0 or 1 when the signal change from 0 to 1 or 1 to 0. This solution can reduce the write power expecially for the case that intend to write the data which totally inverse with the previous data such as 1100 → 0011.

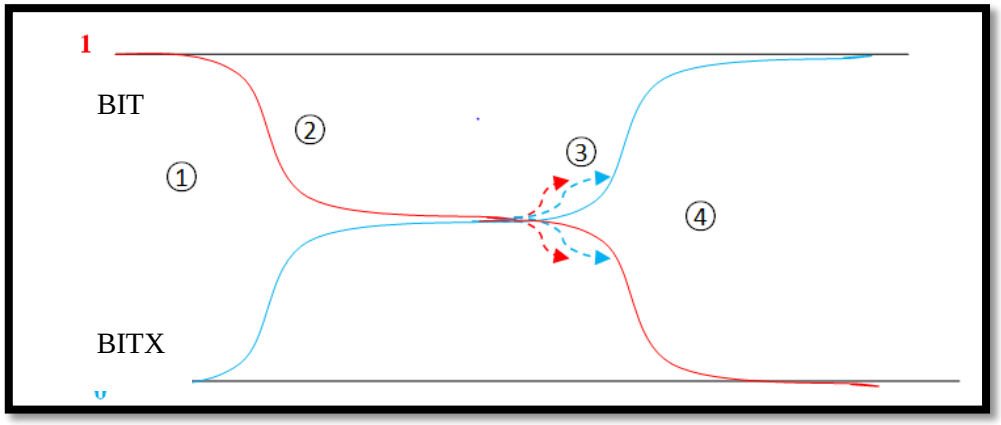


Figure 24 Momentarily pre-write powered down

Phase 1: Full Vdd (data stored and active)

Phase 2: Valid bit reset (bit &bitX depleted)

Phase 3: Write data (bit & bitX stored the same data)

Phase 4: Valid bit set (bit &bitX restored to rail-to-rail signal)

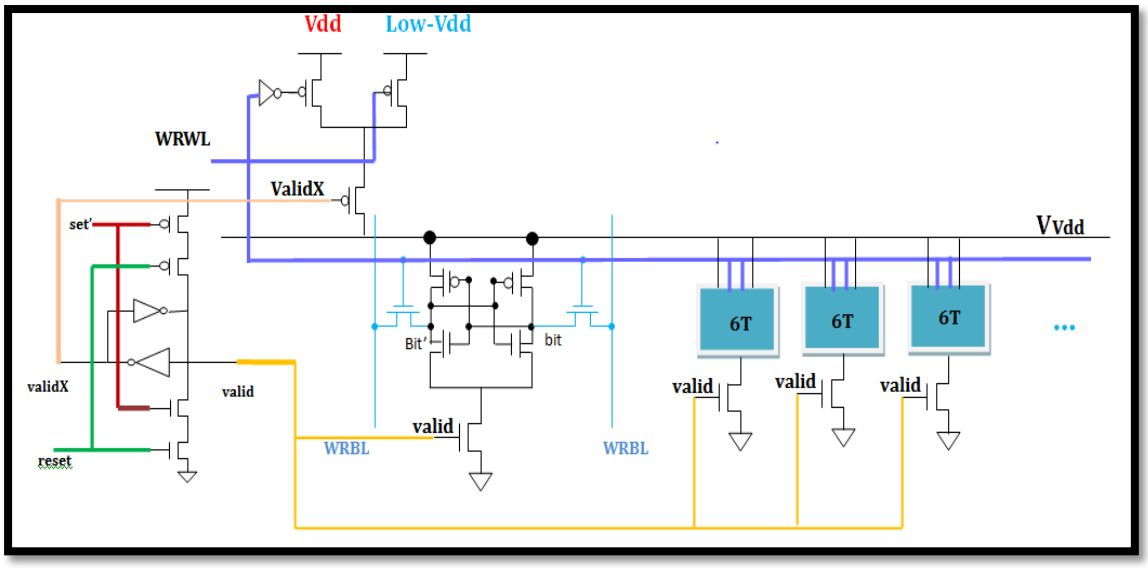


Figure 25 Memory Array with Low-Vdd and Valid bit

3.4 Expected Output

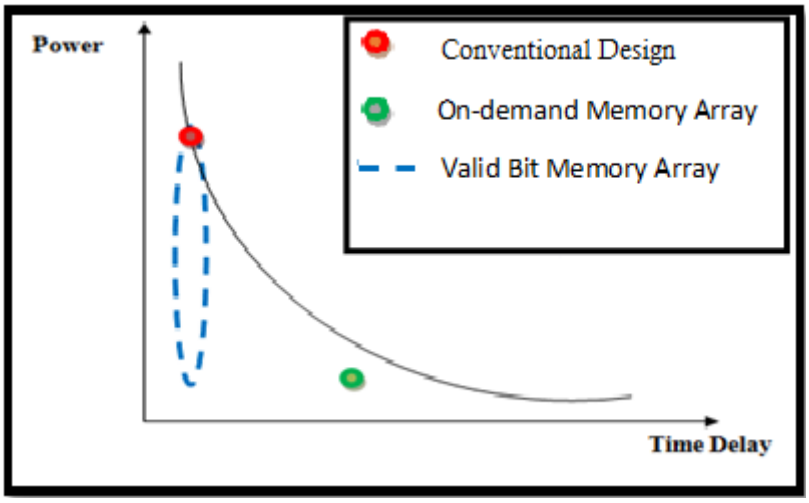


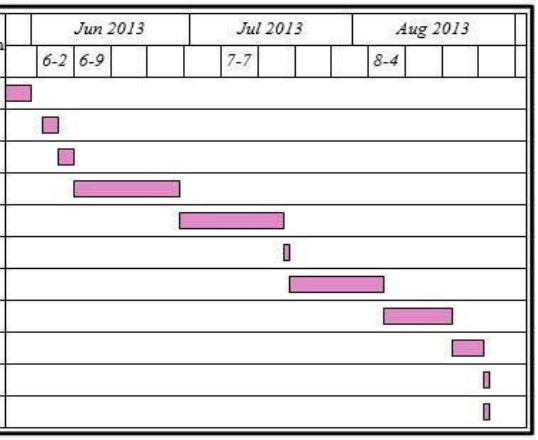
Figure 26 Expected output for proposed schemes

The main objective in this proposed solution is to study the reduction of power dissipation versus time delay. The red point shows existing conventional memory array which is very efficient in terms of time delay but, dissipate a lot of power. The green point shows the memory array that proposed with the first condition On-demand, which is always limit to only one row due to the reason where WL is from decoder which main feature is one-hot decoding, only one input will be asserted high among all of the word lines. Lastly, valid bit, the second condition, which will ouptut result that ranging from the best case to the worst case. Best case is that only one row of memory cells is filled with data which means valid, while, the worst case is defined as when all rows of memory cells have no empty cell, which means that all cells are in active mode or drowsy mode. But still, the worst case will still consume less power than existing design because among all valid cells, only one row of memory cells is currently accessed, while others are all in drowsy mode which will only supplied by low Vdd. The on-demand will introduce a longer delay than valib bit is because it first need to read the address from decoder.

3.5 Timeline

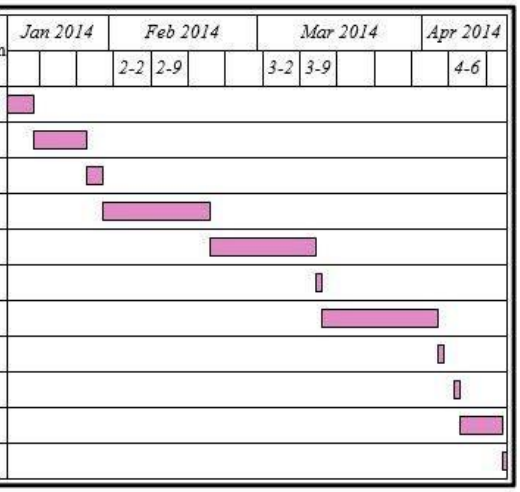
3.5.1 Timeline 1(Project 1)

ID	Task Name	Start	Finish	Duration
1	Discussion on the topic	27-May-13	31-May-13	5d
2	Formulation project objective	03-Jun-13	05-Jun-13	3d
3	Discussion of the methdologies	06-Jun-13	08-Jun-13	3d
4	Research and literature review	09-Jun-13	28-Jun-13	20d
5	Preliminary Report	29-Jun-13	18-Jul-13	20d
6	Submission of Preliminary Report	19-Jul-13	19-Jul-13	1d
7	Enhancement of Project 1	20-Jul-13	06-Aug-13	18d
8	Finalization of Project 1 Report	07-Aug-13	19-Aug-13	13d
9	Poster Preparation	20-Aug-13	25-Aug-13	6d
10	Oral Presentation of Project 1	26-Aug-13	26-Aug-13	1d
11	Poster Submission	26-Aug-13	26-Aug-13	1d



3.5.2 Timeline 2 (Project 2)

ID	Task Name	Start	Finish	Duration
1	Discussion on project scale and design	13-Jan-14	17-Jan-14	5d
2	Implementation Proposed Design circuit	18-Jan-14	27-Jan-14	10d
3	Combination and Testing with other parts	28-Jan-14	30-Jan-14	3d
4	Implementation project on larger scale	31-Jan-14	19-Feb-14	20d
5	Power and time analysis	20-Feb-14	11-Mar-14	20d
6	Submission of Draft report	12-Mar-14	12-Mar-14	1d
7	Enhancement and finalize Project 2	13-Mar-14	03-Apr-14	22d
8	Turnitin check	04-Apr-14	04-Apr-14	1d
9	Submission of Project 2	07-Apr-14	07-Apr-14	1d
10	Preparation for Presentation and Poster	08-Apr-14	15-Apr-14	8d
11	Oral presentation and Poster Submission	16-Apr-14	16-Apr-14	1d



Chapter 4: Implementation & Analysis of Proposed Solutions

Before moving into the memory array section, to prove that the proposed design is working perfectly fine, the figure of whole Register file is included which is shown in figure 27. As mentioned before this proposed RF design has split into 3 different part which is Address Decoder, Memory Array and Domino Mux and these 3 parts are in-charged by 3 different person respectively, the proposed RF is shown in the figure below.

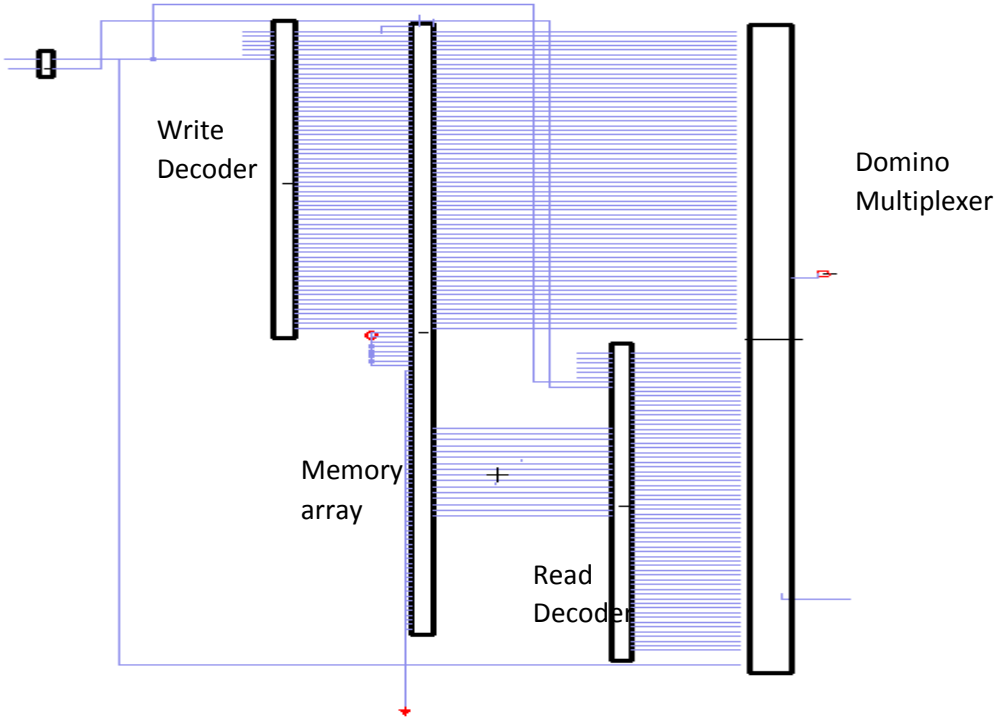


Figure 27 Proposed RF

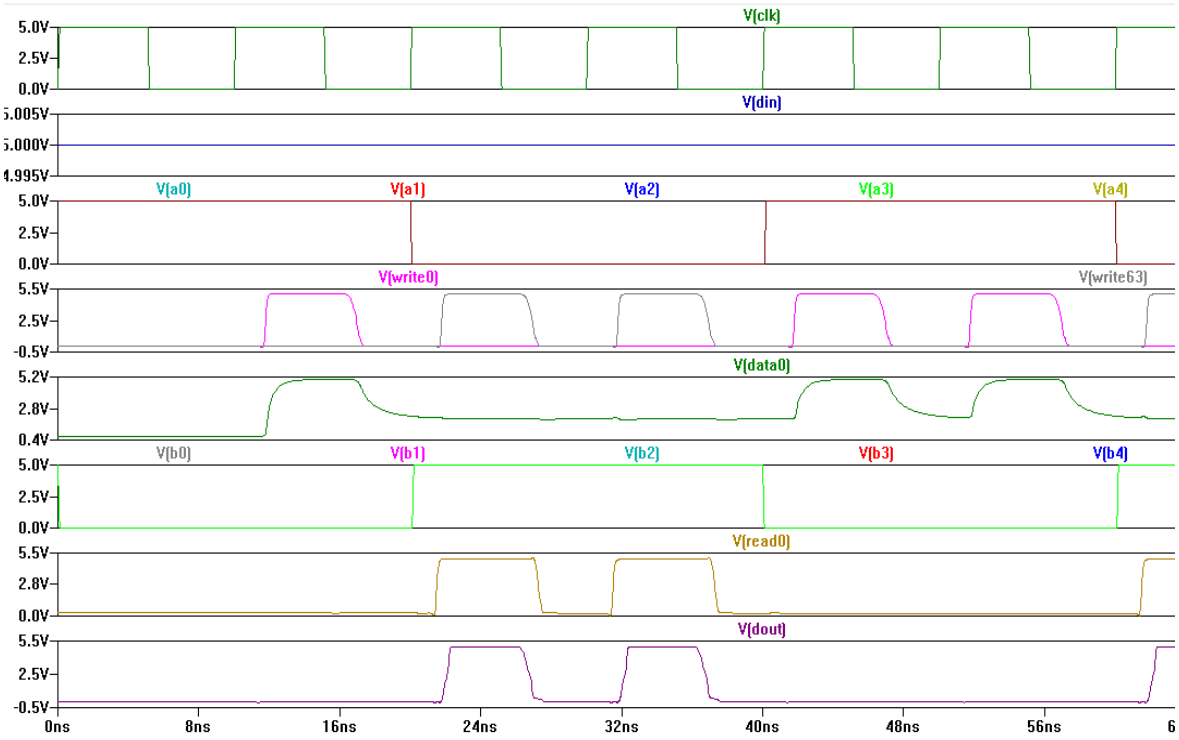


Figure 28 Timing diagram of RF

Figure 28 shows that when the input for write and read decoder is 000000 time which the write WL0 and read WL0 will be activated, when write WL0 is activated, data input which is '1' will be written into the first row of memory array and store the '1' inside, so when read WL0 is being activated time, the storage inside the memory array will be output a '1'by following the clock.

Now, let's look into memory array of the proposed design. Implementations and testing of the design of memory array in proposed solutions earlier will be shown and explained in this part. As what I've mentioned in the technology involved section before, Electric VLSI version 9.03 will be the circuit level design tools, LTSpiceIV will be the simulator for checking waveform on voltage, current/power.

4.1 Valid Bit Flag

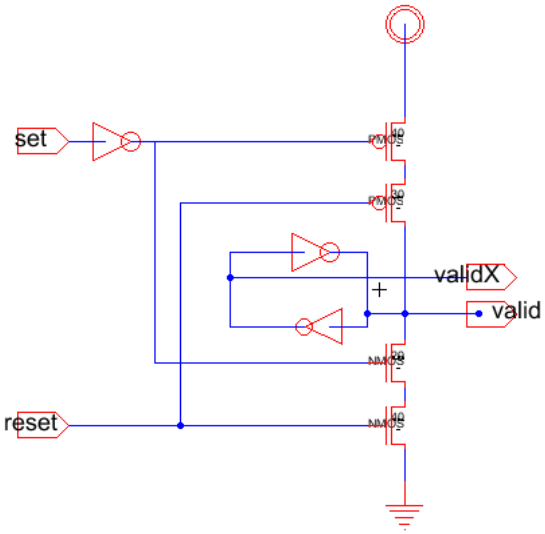


Figure 29 Transistor level view of Valid bit flag

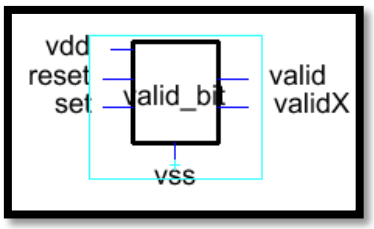


Figure 30 Icon view of Valid bit flag

So, this valid bit flag will be used by programmer to check whether the particular cell contains valid data, besides that, another usage of this valid bit flag is to prevent wrong

data write into the wrong cells, for example now the system initially tends to write to address 0001 which is the second entry of memory array, however there is something wrong with the decoder which it unconciously produce more than one ‘1’to memory array, where this could be activate more than one entry in memory array, so by using this valid bit flag which when data writing time we can pre-set those not currently accessed cells to invalid, therefore, although the WLs for first row memory cells are activated, but with the invalid signal, data won’t be able to write into wrong memory cells also.

As shown in the timing diagram(figure 31) below, set and reset must be the incerse signal, where the circuit will produce two outputs which is valid and validX (invalid). According to the transostor level of the circuit when set is provided a ‘1’, ‘0’ will definitely being assigned to reset signal, when set become a ‘1’, after an inverter ,it will activate the pmos on the top, and disable the nmos on the bottom, while, reset with a ‘0’ will activate the pmos on the second top, while disable the nmos, which Vdd will flow into the circuit and output valid as ‘1’, validX as ’0’.

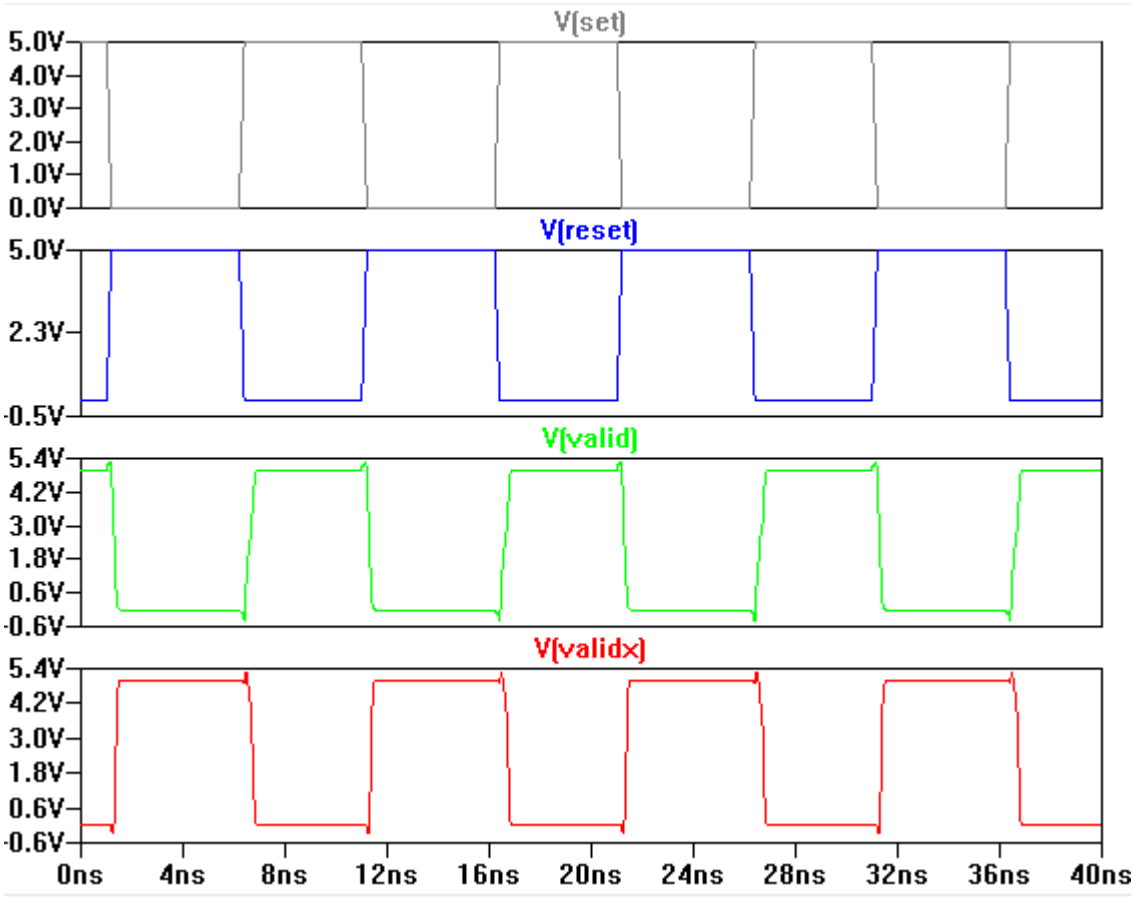


Figure 31 Timing diagram of valid bit flag

4.2 Shared-P memory array

What means by shared-P memory array? Basically P is stand for power source, which means by the same rows of memory cells which shared the same write WL & read WL will share the same power source (Vdd) as what proposed in the section before.

4.2.1 Shared power supply Vdd Topology

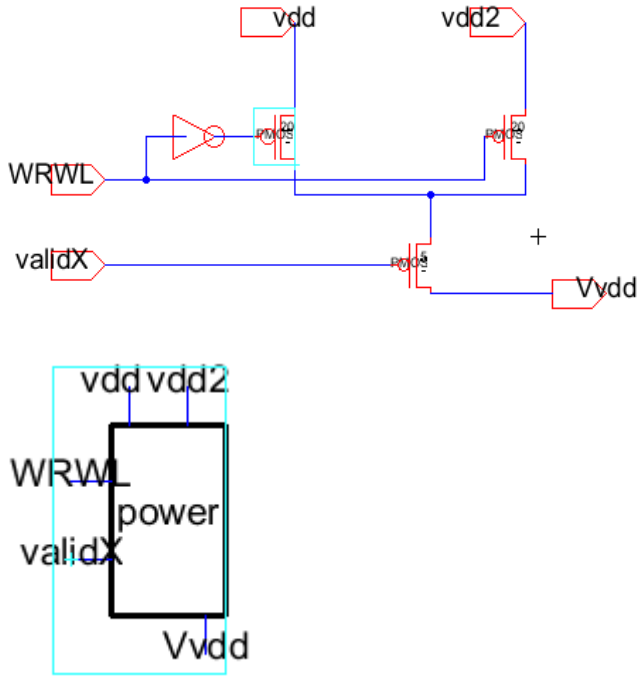


Figure 32 (a) Transistor level of share power source (b) Icon view

Figure 32(a) shows the transistor level of power source, which the control signal is write WL and validX respectively, and form a 2-level power control source. Vdd will be provided of 5V, while vdd2 which is low Vdd, will be a 2V signal in this modified design. The upper layer is controlled by WRWL, which is when decoder tend to write to the current memory cell, decoder will provide a '1', which after the inverter will

produce a 0 to turn on the pmos of vdd, while 1 will turn off the pmos of vdd2, hence compare to original design, the proposed solutions has two different vdd power supply which in charged of different conditions. When it comes to second layer, the valid signal which generated by valid bit flag before, if the satais valid to read to the cell is valid to write, signal will be provided in order to turn on the pmos accordingly. This kind of design is actually using the idea of power-gating which introduced in the early part before. This will be the header switch with the power switching control signals, WRWL and validX.

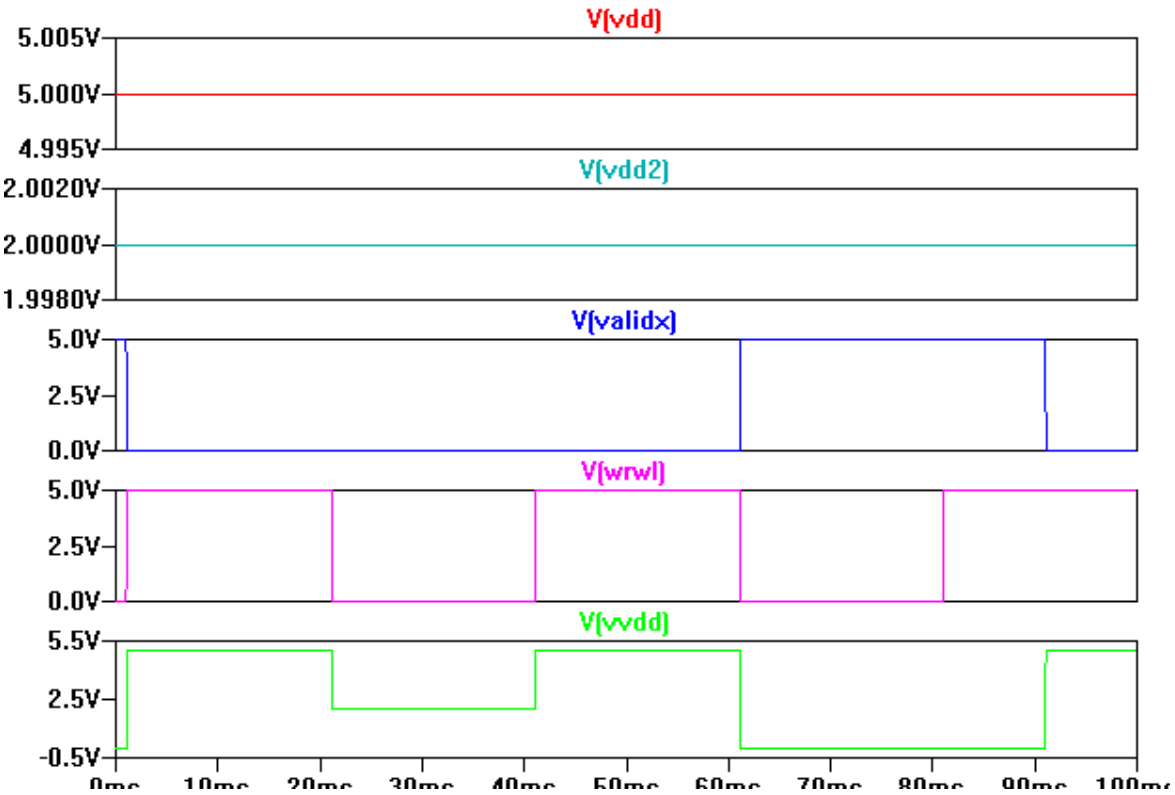


Figure 33 Timing diagram of shared Vdd

As what shown in the timing diagram above, the Virtual Vdd which is the output of this topology, will switch between 5V and 2V because of the of Vdd and Vdd2(low Vdd) provided that the entry is valid to read or write. If it is invaid, the signal is high impedence 'Z' which will swing and float between 0 and 5.

4.2.2 Shared-P memory cell

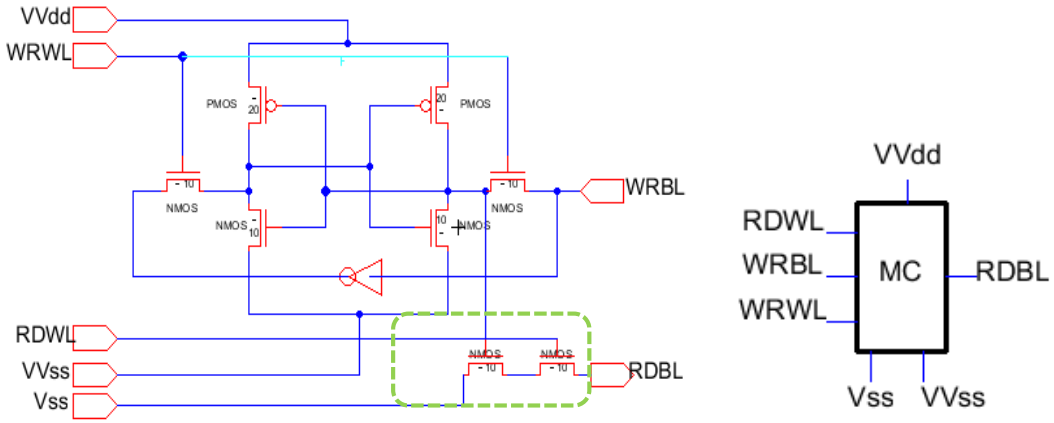


Figure 34 (a) Transistor level of shared-p memory cell (b) Icon view

Figure 34(a) is the 1-bit memory cell which consists of 6T SRAM cell and read port, as shown in the figure, the virtual Vdd (VVdd) is an input instead of just directly connect to a nominal Vdd, same case for the ground, virtual Vss (VVss) will be another power-gating to control the Vss power supply for the memory cell which will dicuss further in the diagram later. Therefore, as what shown in figure 35, after we connect up valid bit flag with the shared-p power source and also the shared-p memory cell, the proposed shared-P memory array is formed. As what mentioned, VVss virtual ground will be gated by an nmos which is the footer of power gating. The power control switching signal is valid which is also generated by valid bit flag.

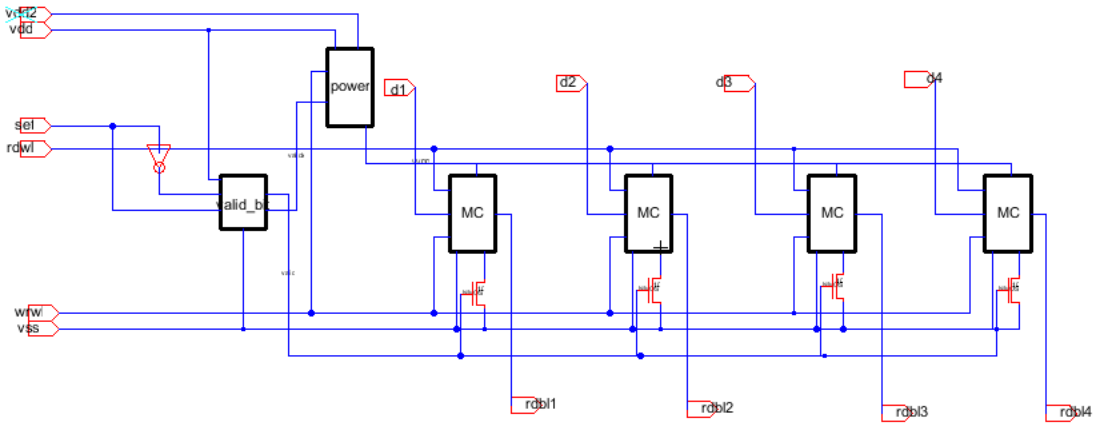


Figure 35 1x4 (1 entry 4 data) memory array

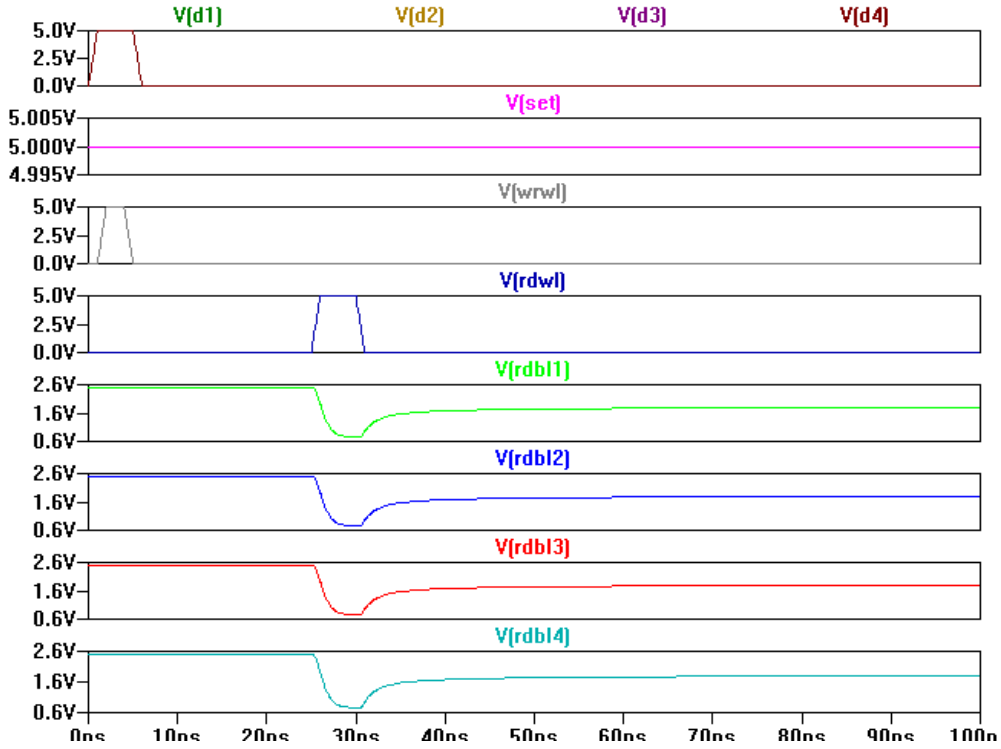


Figure 36 Timing diagram of 1-entry memory array

4.3 Testing and result of the proposed solutions

In this part, the main technology for circuit simulation that will be invoked is LTSpiceIV, which is a high performance SPICE simulator, schematic capture and waveform viewer with enhancements and models for easing the simulation of switching regulators. Hence, in order to verify the power efficiency of the proposed solutions in this projects, variant tests will be conducted in order to compare the power consumption between proposed solutions and current design.

Basically, during the tests are conducting, the input data has been pre-defined to 4 bit for each of the tests while changing the number of entries in order to observe the power consumption. The reason to pre-define the data input size is to assure the reliability of the tests so that the power can be observed with varying memory size. Besides that, since the proposed solutions has 2 main conditions that can used to control the powered-on or powered-off of the circuit, which is Validity and On-demand, therefore these two conditions will be taken into the main considerations during the tests are conducting. Basically, this is how the test are going to be carry out, the power supply which is Vdd and Vss in the whole circuit will be pulled out and connect together to a main Vdd and main Vss respectively in order to observe the power dissipation.

Before showing the tested results, three different modes for memory cells will be introduced as what mentioned in the earlier section which are active mode, drowsy mode and sleep mode. Active mode will be supplied by 5V vdd and 0V vss which means the cell is currently being access, while drowsy mode will be supplied by 2V vdd and 0v vss which means that the memory cell is not being used currently but it

contains valid data inside the bi-stable element, therefore low power need to be supplied to the circuit in order to retain the storage inside to preventing data loss. Lastly, sleep mode which refer to invalid cell, there will be no power supply to the current circuit, in others words, the circuit is completely powered down.

4.3.1 Verification on static power dissipation

The results first shown below are tested on static power dissipation for three different cases between current basic design and proposed design which are 1 entry, 4 entries and 8 entries with 4 data input size memory array.

4.3.1.1 1-entry-4-data static power comparison

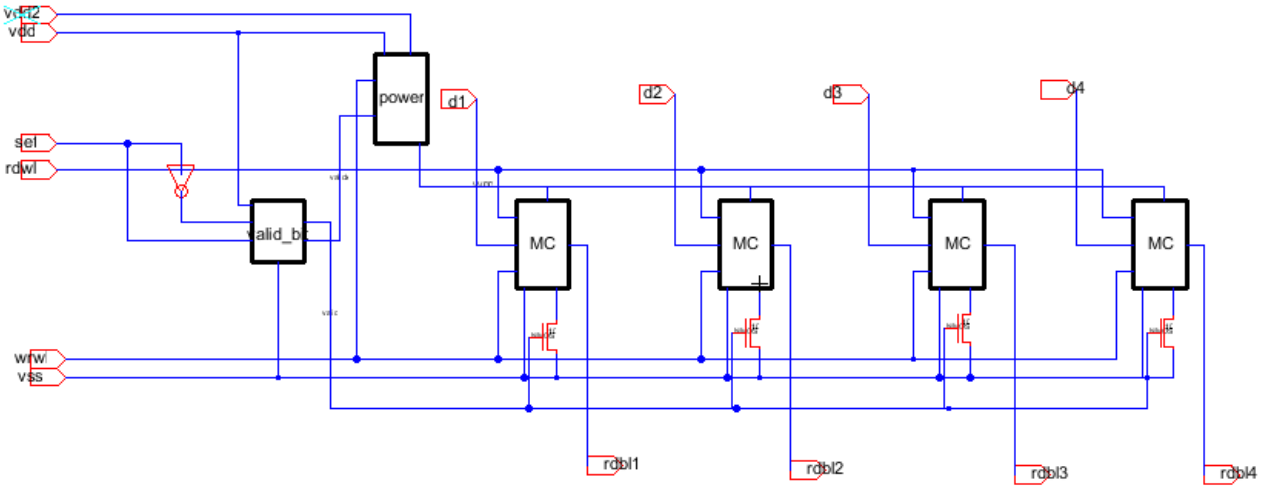


Figure 37 1-entry memory array

Conventional design	data	ivdd(pA)	ivss(pA)	total leakage
I entry 4 data	1	100	16	116
	0	100	16	116

Table 1 leakage of conventional design

Proposed design	Entry's state	data	Ivdd (pA)	Ivdd2 (pA)	Ivss (pA)	total leakage
MC (I entry 4 data)						
valid, on-demand	Active mode	0	133.35	3.01	6.71	143.07
		1	113.3	3.01	15.06	131.37
valid, off-demand	Drowsy mode	0	141.55	33.67	18	193.22
		1	121.36	35.08	20.06	176.5
Not valid, on-demand	Sleep mode	0	126.38	3.01	6.05	135.44
		1	84.56	3.01	6.05	93.62
Not valid, off-demand	Sleep mode	0	127.9	12.04	6.05	145.99
		1	107.86	12.04	6.05	125.95

Table 2 leakage of proposed design

4.3.1.2 4-entries-4-data static power comparison

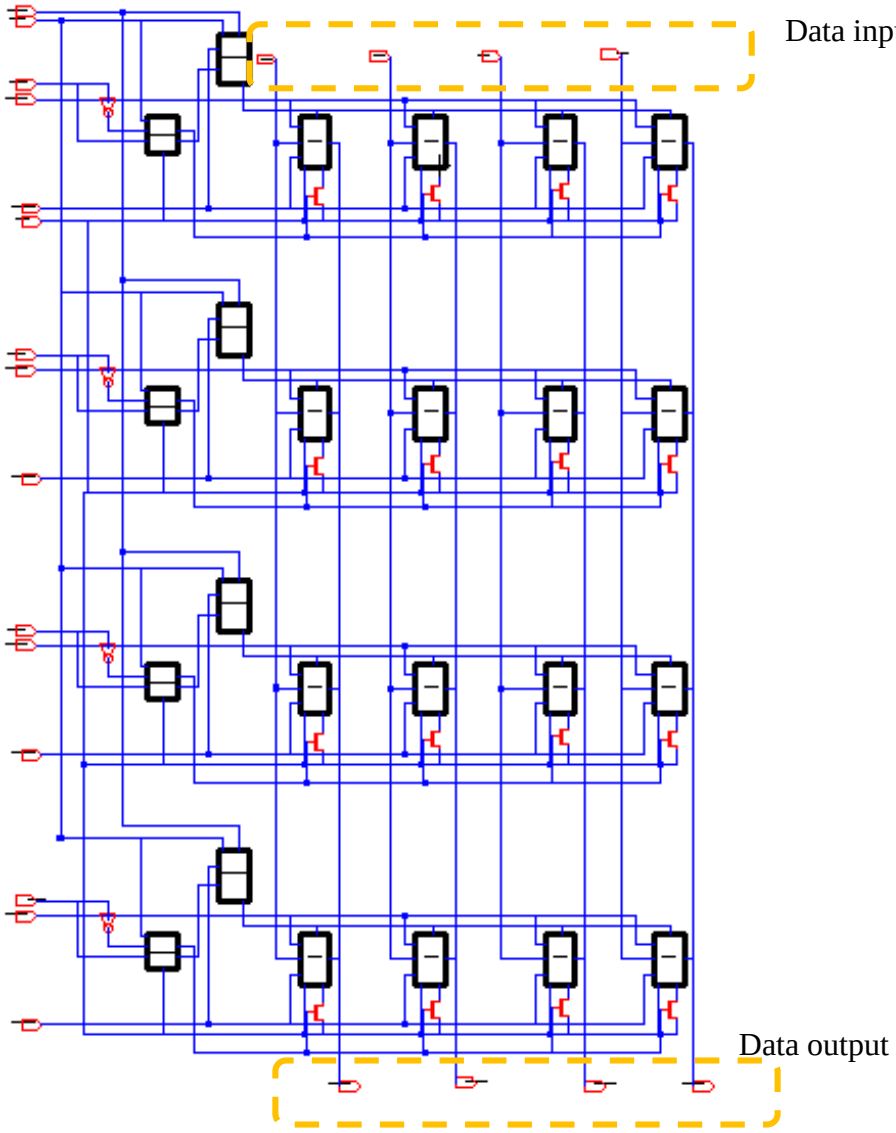


Figure 38 4 entries memory array

Inside 4 entries memory array, there will be 4 different write and read word lines (WL) which are provided from dedicated read and write decoder for each row of memory cells, the same row of memory cells will be connected to the same word line to control the data in and out. However, the data output from the read ports which located in the

same column will be drive to a same output which named as read bit line (RDBL), this signal will eventually send to domino multiplexer for data reading purposes. In our case, there will be 4 read bit line due to the 4-data input size.

Conventional design	data	ivdd(pA)	ivss(pA)	total leakage
MC (4 entry 4 data)				
1 entry on-demand	0	400.9	70.2	471.1
	1	320.75	80.26	401.01
2 entries on-demand	0	400.9	60.18	461.08
	1	320.75	80.26	401.01
all cells off-demand	0	400.9	80.22	481.12
	1	320.75	80.26	401.01

Table 3 leakage of 4-entry conventional design

Proposed design	MC state	data	ivdd (pA)	ivdd2 (pa)	Ivss (pA)	total leakage
1 valid 1 on-demand	1 entry-> active mode	0	517.09	39.13	24.9	581.12
(same entry)	Others->sleep mode	1	417.33	39.13	33.21	489.67
2 valid 2 on-demand	1 entry-> active mode 1 entry-> drowsy mode	0	530.6	61.6	39.66	631.86
(Rn W diff cell)	Others ->sleep mode	1	450.38	62.18	47.22	559.78
2 valid 1 on-demand	1 entry-> active mode	0	530.6	61.2	39.78	631.58
	1 entry-> drowsy mode Others-> sleep mode	1	450.58	59.1	50.56	560.24
all valid 1 on-	1 entry-> active mode	0	557.93	105.97	287.7	951.6
demand	Others-> drowsy mode	1	477.63	103.53	394.16	975.32
all not valid 1 on-	All entries-> Sleep mode	0	510.11	39.13	24.2	573.44
demand		1	408.15	39.13	24.2	471.48
all not valid all off-	All entries-> sleep mode	0	511.65	48.16	24.2	584.01
demand		1	499.12	48.16	24.2	571.48

Table 4 leakage of 4-entry proposed design

4.3.1.3 8-entries-4-data static power comparison

Inside this 8 entries memory array there will be 8 read and write word lines which came from read and write decoder respectively.

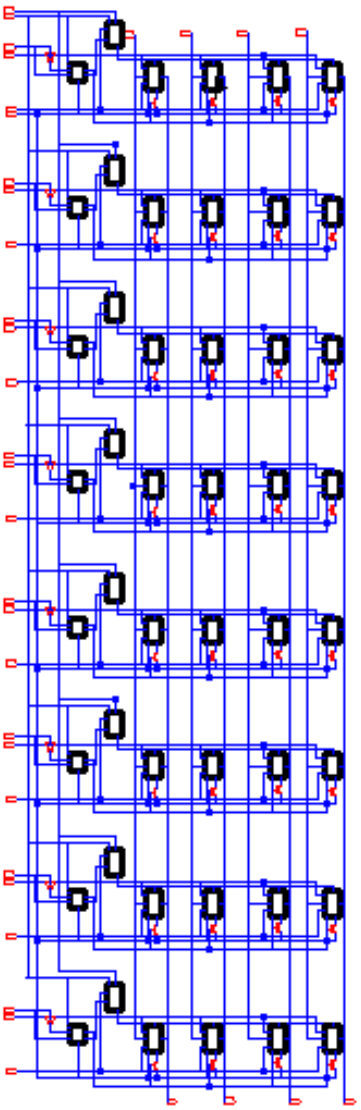


Figure 39 8-entry memory array

Conventional design	data	ivdd (pA)	ivss(pA)	total leakage
MC (8 entry 4 data)				
1 entry on-demand	0	801.8	150.4	952.2
	1	641.49	160.53	802.02
2 entries on-demand	0	801.8	150.4	952.2
	1	641.49	160.53	802.02
all entries off-demand	0	801.8	160.43	962.23
	1	641.5	160.53	802.03

Table 5 leakage of 8-entry conventional design

Proposed design	Entry status	data	ivdd (pA)	ivdd2 (pa)	Ivss (pA)	total leakage
1 valid 1 on-demand	1 entry->active mode	0	1028.7	87.29	49.06	1165.05
(same cell)	Others-> sleep mode	1	868.33	87.29	57.41	1013.03
2 valid 2 on-demand	1 entry->active mode 1 entry-> drowsy mode	0	833.62	109.1	64.58	1007.3
(Rn W diff cell)	Others-> sleep mode	1	881.83	110.34	71.42	1063.59
4 valid 2 on-demand	2 entries-> active mode 2 entries-> drowsy mode	0	1069.7	155.98	516.66	1742.34
	Others-> sleep mode	1	908.83	156.43	99.45	1164.71
all valid 1 on-demand	1 entry-> active mode	0	1119.5	224.782	937.27	2281.552
	Others-> drowsy mode	1	949.65	222.11	937.27	2109.03
all not valid	All entries-> sleep mode	0	1023.3	96.32	48.4	1168.02
All off-demand		1	862.9	96.32	48.4	1007.62
all not valid	All entries-> sleep mode	0	1022.7	87.29	48.4	1158.39
1 on-demand		1	839.78	87.29	48.4	975.47

Table 6 leakage of 8-entry proposed design

Theoretically, the power dissipation in proposed design should be reduce as what discussed in expected results section, that is because the power gates that added inside act as an controller of the power supply of the whole circuit which can turn on or off the power supply by considering two conditions which is data validity and on-demand, thus when the circuit is powered off, the power dissipation should be decreased.

However, those tables above clearly show that the proposed design not only couldn't archieve as what expected, but also increase the power dissipation by average 20%.

As we know, leakage power consists of a few different types, in our case, for nanometer device or circuit, leakage power is mainly dominated by sub-threshold leakage and gate oxide tunneling current. The sub-threshold current (power) which refer to the current flow from drain to source when the transistor is not completely off. In the past, the leakage current remain small when the transistor is being turned off. However, nowadays with the technology scaling, supply voltage has been scaled down in order to maintain the device reliability and reduce dynamic power dissipation. Relatively, this reduction in supply voltage also requires the scaling of the Vth which the value should stay between ground and supply voltage. The reduction of Vth indicated that there are lesser gate voltage will be swing below threshold in order to turn off the transistor. Hence, we can conclude that the sub-threshold leakage current increases exponentially to the reduction of threshold voltage.

Talk about the second one, gate oxide tunnelling leakage. The gate oxide which is known as the insulator between the gate and channel. The device scaling in nanometer increases short channel effects which will limit the electron drift characteristics. To control the short channel effects, gate oxide thickness become thinner and thinner to increase the channel conductivity and performance when the device is ON and reduce the sub-threshold leakage when the device is powered-off. But somehow,scaling down the oxide thickness brings pros and cons, the advantages is give rise to high electric field, resulting in a high direct-tunnelling current through transistor gate insulator, relatively leading to high leakage power consumption.

There are a few potential problems which caused this unexpected results. Firstly, limitation of online design models which can apply in Electric VLSI, the semiconductor C5 model 330nm technology which is used as the library in Electric VLSI is not the ideal model to evaluate and verify the leakage power, the reason is that in 300nm C5 models, leakage power brings not much impact to the overall performance for both designs.

Secondly, lack of choices for transistor type, as mentioned before in a complete circuit design, variant transistor type with different threshold voltage will be apply in different parts in order to reduce the power dissipation. Low leakage transistor which refer to the transistor with high threshold volatage, low speed and relatively low power consumption, is actually the best type to use as the transistor for power gate in the proposed desgin. However, the design tool, Electric VLSI doesn't provide different type of transistors for user to choose, therefore, throughout the whole design, we only can apply the one and only one transistor type. Besides that, the number of transistors also increase compared to the conventional design, and there is no low-leakage transistor can be applied as power gate, under these circumstances, relatively the power consumed also increase.

Moreover, noticed that Electric VLSI is also not the ideal design tools to evaluate power consumption due to the reason that EVLSI don't even has any way or method to observe the overall dissipated power so we can only pull out the power source Vdd and Vss in order to observe the power changes in both design.

4.3.2 Verification on static power dissipation between 1-entry-4-data shared-footer memory array and seperated-footer memory array

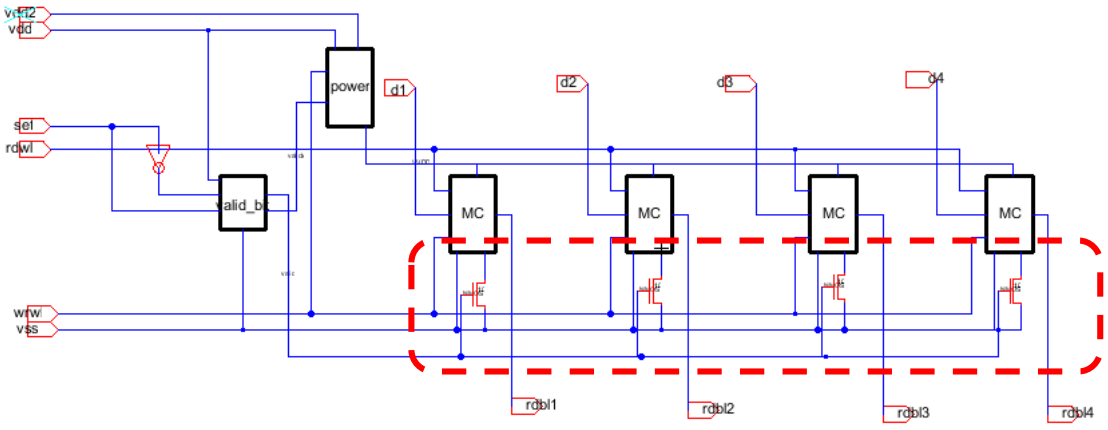


Figure 40 Separated-footer power switch

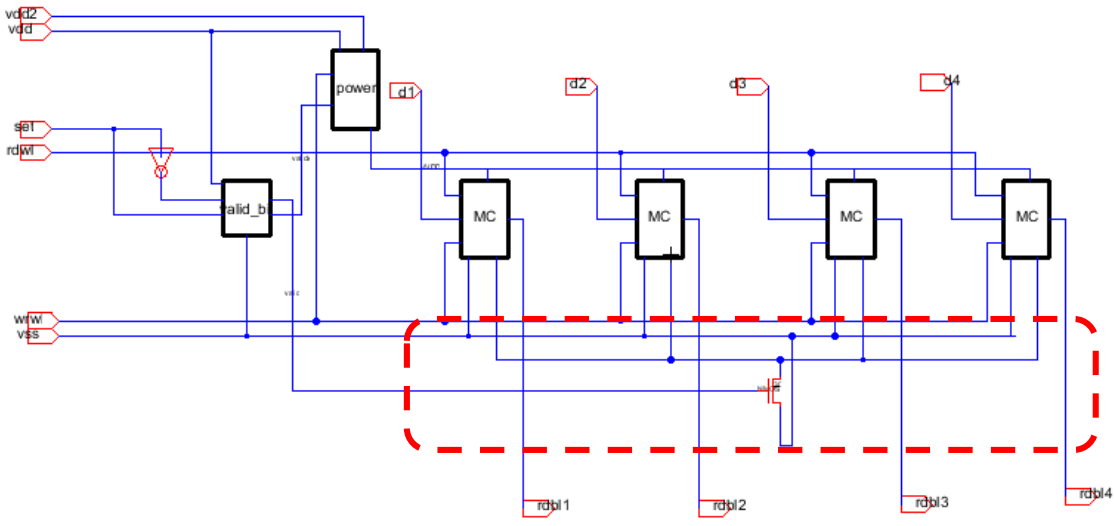


Figure 41 Shared-footer power switch

Proposed design	Entry's state	data	Ivdd (pA)	Ivdd2 (pa)	Ivss (pA)	total leakage
MC (I entry 4 data)						
valid, on-demand	Active mode	0	133.35	3.01	6.71	143.07
		1	113.3	3.01	15.06	131.37
valid, off-demand	Drowsy mode	0	141.55	33.67	18	193.22
		1	121.36	35.08	20.06	176.5
Not valid, on-demand	Sleep mode	0	126.38	3.01	6.05	135.44
		1	84.56	3.01	6.05	93.62
Not valid, off-demand	Sleep mode	0	127.9	12.04	6.05	145.99
		1	107.86	12.04	6.05	125.95

Table 7 leakage of separated-footer power switch

Proposed design	Entry's state	data	Ivdd (pA)	Ivdd2 (pa)	Ivss (pA)	total leakage
MC (I entry 4 data)						
valid, on-demand	Active mode	0	130.34	3.01	6.39	142.74
		1	111.3	3.01	14.53	130.84
valid, off-demand	Drowsy mode	0	139.4	34.1	17.8	194.3
		1	121.4	35.07	20.07	176.54
Not valid, on-demand	Sleep mode	0	123.38	3.01	6.05	135.44
		1	84.56	3.01	6.05	93.62
Not valid, off-demand	Sleep mode	0	126.4	12.04	6.1	144.54
		1	106.35	12.04	6.1	124.49

Table 8 leakage of shared-footer power switch

Ideally, the 2nd design(figure 40) should be lesser leakage compared to 1st design (figure 41) due to the reduction of the number of nmos. However, from the tables above, it shows that there is not much different in terms of power consumption. Why does this happen? First, for seperated-footer switch, each of the nmos aspect ratio is set to 5, while in the 2nd design which is with shared-footer switch, due to the sharing problem, the AR(aspect ratio) for nmos have to set to a relatively larger value in order to assure

that the driven current is big enough to supply each of the memory cells which is set to 10 in this case. Although the AR in 1st design is smaller compared to 2nd desgin, but overall the power comsumption is only reduced by the most 0.02%, which can conclude as not much difference, the reason is that there are total 4 nmos with smaller AR in 1st design, but there's only 1 nmos with larger AR exists in 2nd design, so in other words, their static power dissipation are almost the same.

Besides this, as mentioned before, leakage power doesn't bring any big difference under this 300nm C5 design enviroment, some more there is no low-leakage transistor to use as the power switch, so power dissipation for both desgin cannot evaulate accurately due to the limitation of tools.

4.3.3 Verification on dynamic power dissipation for writing process

As we know, for writing process, especially when the next data that need to be written inside is the totally opposite data of the current storage, for example when 1 write to 0 or when 0 write to 1, it will consume a lot of dynamic power. Therefore, in order to reduce high dynamic power dissipation, valid bit has been utilized to overcome this problem.

As mentioned in the methodology part before, the concept is momentarily powered-off the targeted memory cell/array which prior to writing process. The steps are first reset the cells, then next get the write data ready, activate write wordline then only set the cells to valid cell as shown in figure 24. Those diagrams and tables shown below are the results that tested on 1 bit memory cells and also 1-entry-4-data memory array.

4.3.3.1 Comparison between current and proposed 1 bit memory cell

conventional design	**transition time(ns)**	**dynamic power**	
Signal changes		**ivdd**	**ivss**
0 -> 1	0.5989	23.46pA -> 1.38mA	5.02pA -> 434.3uA
1 -> 0	0.4804	21.8pA -> 1.5mA	5.78pA -> 561.4uA

Table 9 Dynamic power dissipation of conventional design

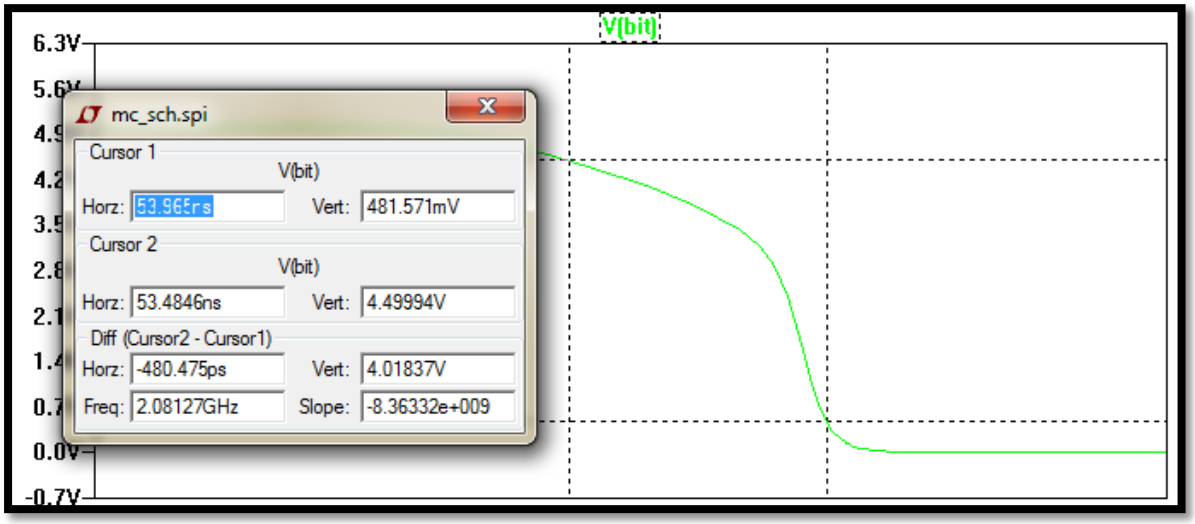


Figure 42 Output signal transition from 1 to 0

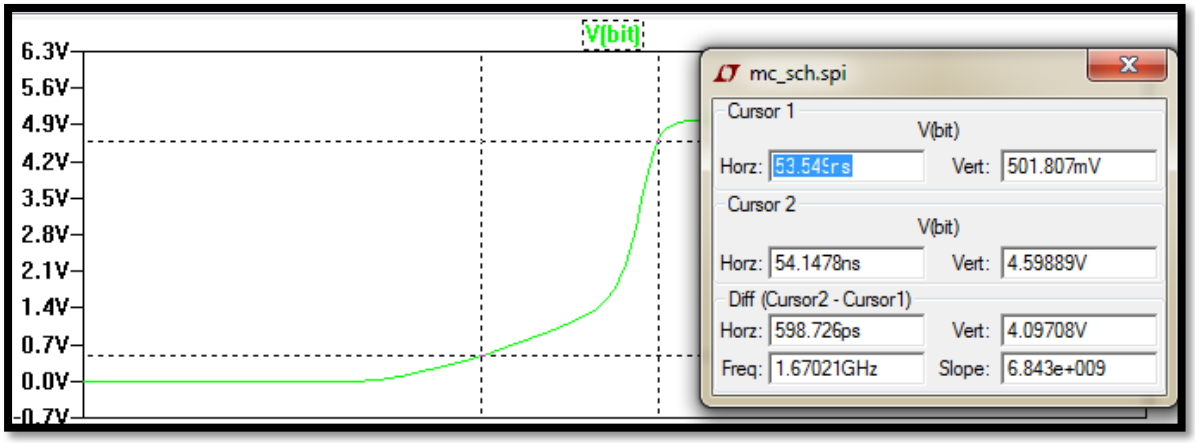


Figure 43Output signal transition from 0 to 1

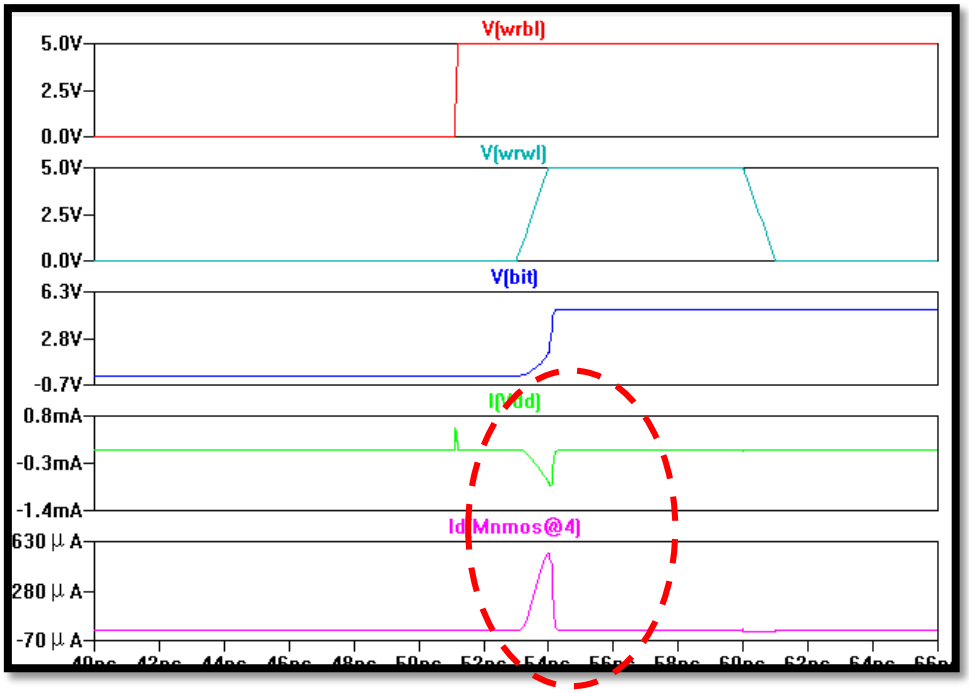


Figure 44 Timing diagram of 1 bit basic memory cell

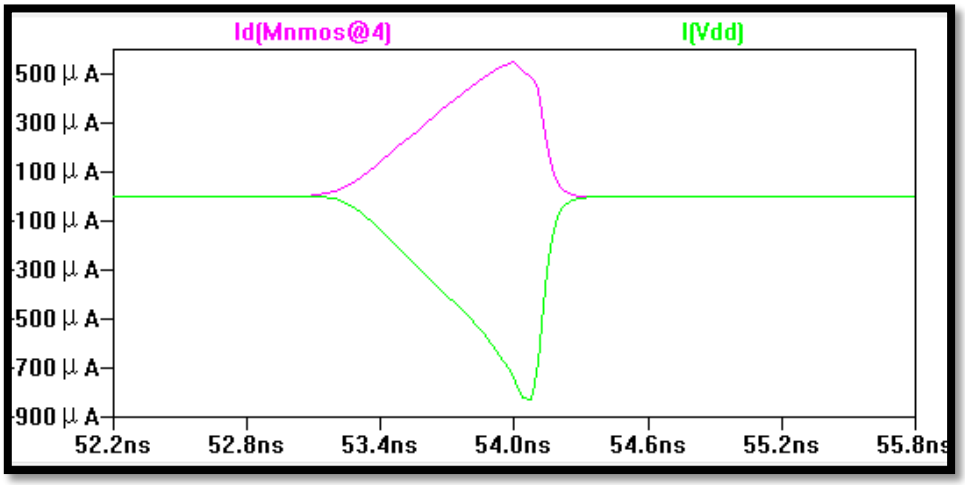


Figure 45 Dynamic power (ivdd and ivss)

However, in proposed design with valid bit control bit, it is possible to shut down the memory cells temporarily which prior to writing, in a sense that it can minimize the dynamic current. So first, how does the dynamic current occur? Dynamic power is the power consumed when signal changes, means that when signal from 0 change to 1 or from 1 change to 0, the current especially for ivdd and ivss will spike because they need to fight with another power source in order to produce a full rail signal.

proposed design	**power before reset**			**power after reset**			**transition time(ns)**	**dynamic power**	
signal changes	**ivdd**	**ivdd2**	**ivss**	**ivdd**	**ivdd2**	**ivss**		**ivdd**	**ivss**
0 -> 1	953.7pA	3pA	16.2pA	170.8pA	3pA	118pA	0.3357	170.8pA -> 537uA	118pA -> 83uA
1 -> 0	950.88pA	3pA	96.8pA	120.6pA	3.02pA	118pA	0.1748	120pA -> 1.3mA	118pA -> 15.78uA

Table 10 Dynamic power dissipation of proposed design

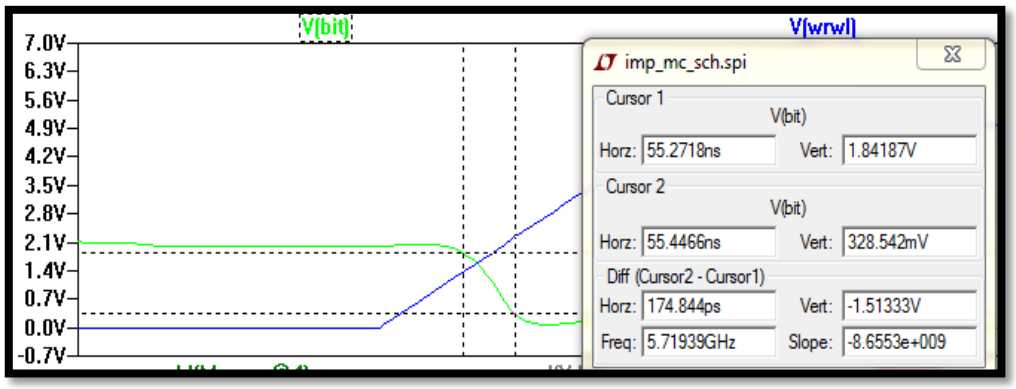


Figure 46 Output signal transition from 1 to 0

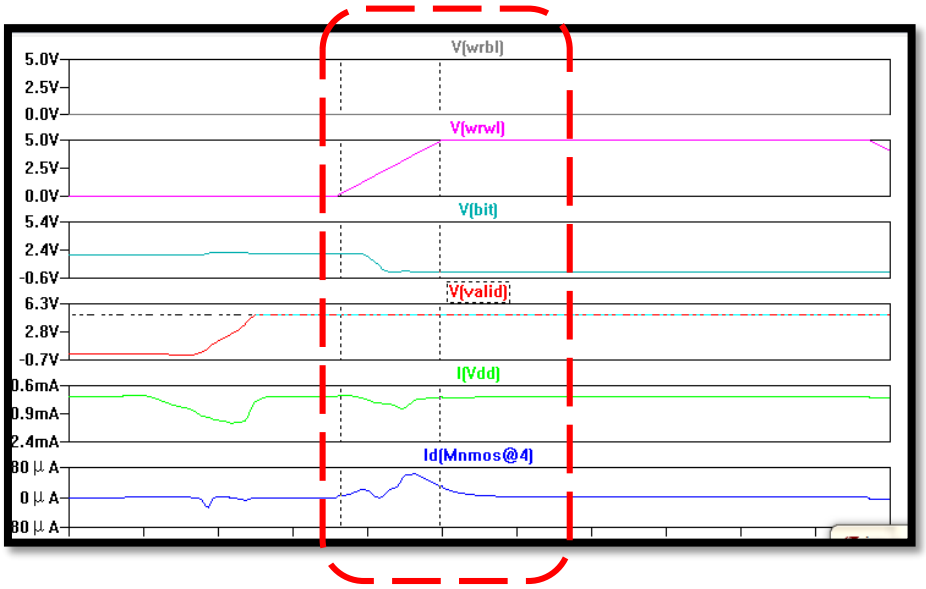


Figure 47 Timing diagram of 1 bit proposed memory cell (1 -> 0)

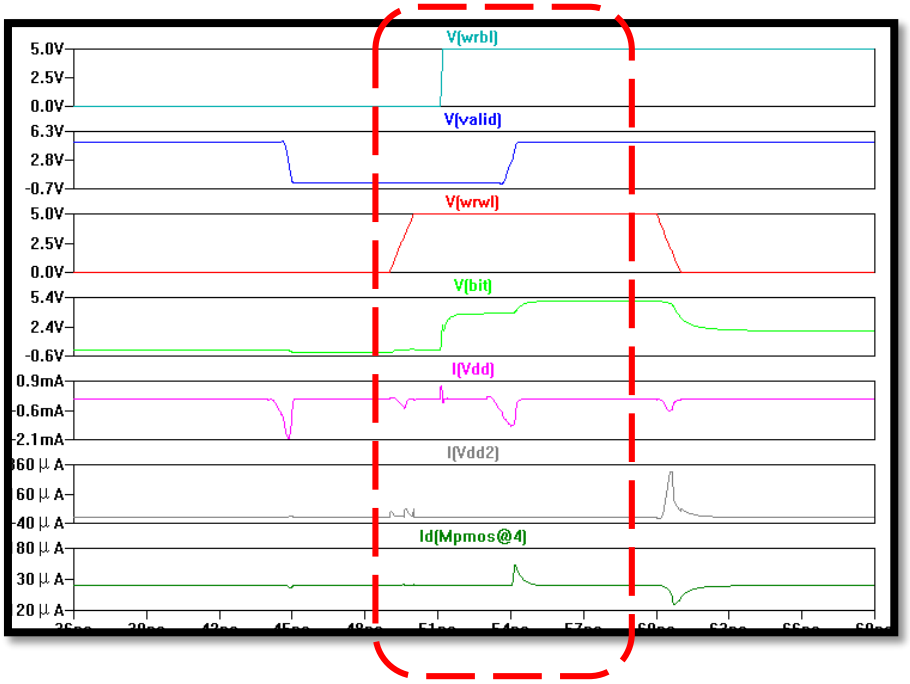


Figure 48 Timing diagram of 1 bit proposed memory cell (0 -> 1)

4.3.3.2 Comparison between current and proposed 1 entry memory array

memory array	power before reset			power after reset			dynamic power	
signal changes (0 -> 1)	ivdd	ivdd2	ivss	ivdd	ivdd2	ivss	ivdd	ivss
basic memory array	-	-	-	-	-	-	80.19pA -> 3.5mA	3pA -> 2.6mA
proposed memory array	1.7nA	1.27nA	1.23nA	303.4pA	12pA	201pA	303pA -> 504uA	201pA ->55uA

Table 11 Dynamic power dissipation of 1x4 memory array

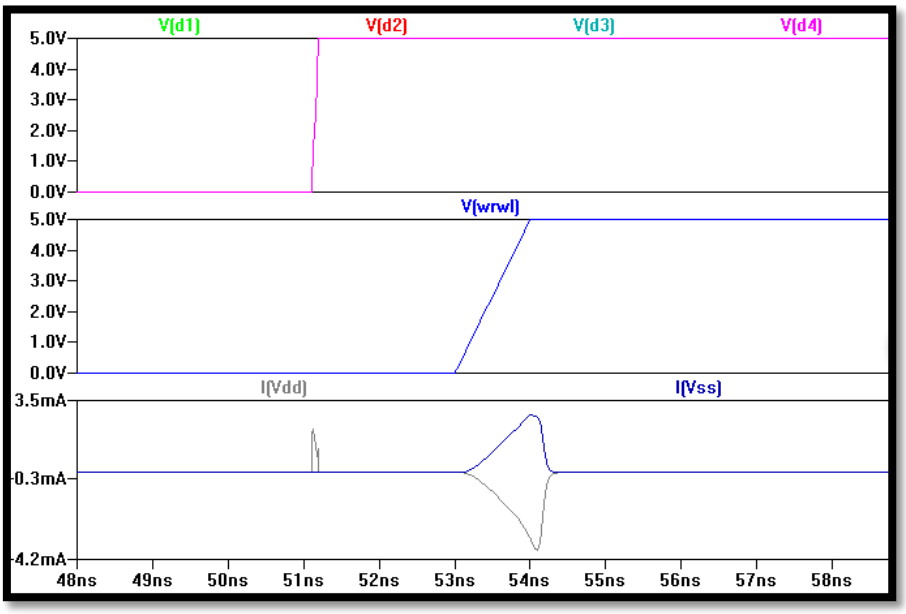


Figure 49 Timing diagram of basic memory array

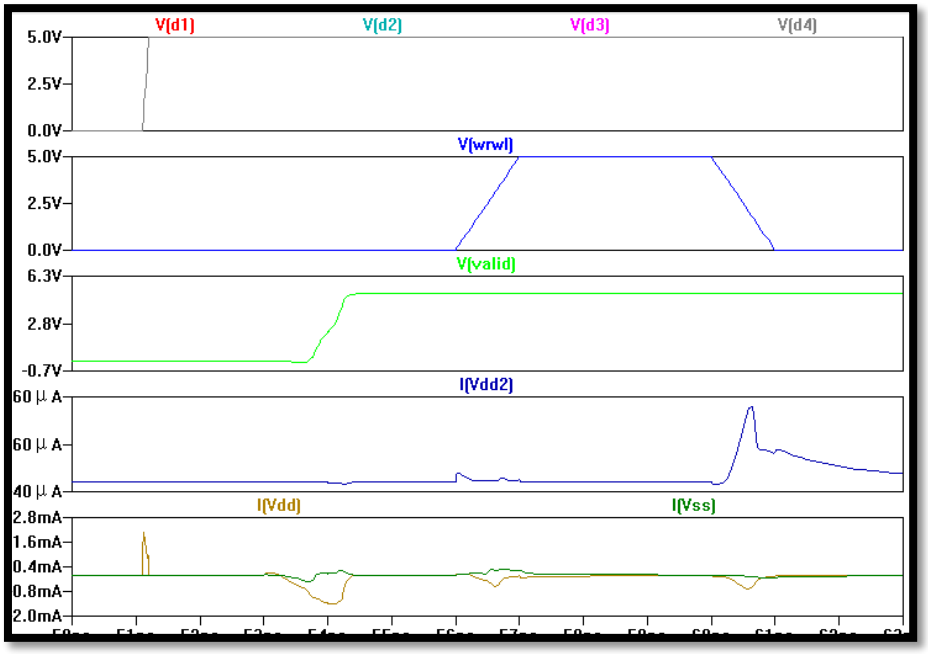


Figure 50Timing diagram of proposed memory array

After the tests are conducted between modified design and current design, the results show that the modified design is consumed lesser dynamic power than the current design, means that when output signal change, the dynamic current (ivdd and ivss) spike lesser than the conventional design. In other words, the modified design need lesser power to produce full rail signal. That's because of the momentarily reset, the whole cell will be shutting down, there is no signal changes which means that there is also no power will be consumed, ivdd and ivss will swing in the middle, after the cell is set to valid, the cell will be powered up again, that time when a '1' need to be written inside, ivdd don't have to fight so hard with ivss in order to produce a full rail signal, this same goes to writing a '0' case. Therefore, it is proven that the modified design consumed lesser dynamic power than the conventional design.

In terms of speed, which can be observed from transition time from table 10 and table 11, proposed design need lesser time in order to write a '1' or '0'. However, don't forget about the time for resetting the memory cell, in this case, the cell has been reset about 2-5ns in order to let the vdd and vss flow randomly in between 0V and 5V so that the design dissipated lesser dynamic power after the design powered up in order to write new data into the bi-stable element (SRAM cell) during writing process. Therefore, the proposed design will be slower to produce the output

Chapter 5: Conclusion

Typically, this proposal is to verify the static and dynamic power dissipation of the memory array which is a portion of register file between the proposed design and the current conventional design. One new memory cell's state has been introduced in this proposal, drowsy mode, during this mode the memory cells will be supplied by lower vdd which the value will be smaller than nominal Vdd. This mode will be implemented by taking two conditions which is data validity and on demand into considerations in order to control the power supply throughout the whole design. The original intention is to use these techniques to improve the power efficiency problem.

First of all, the verification on the dynamic power for the writing process has improved as what expected, which the valid bit enables the proposed design to consume lesser dynamic power than the conventional design. However, it may slower down the speed of the writing process due to the reason the design need some extra time to reset the memory cells first before writing new data. Nowadays, a perfect balance that need to be taken between speed and power dissipation are the critical problem for IC manufacturer, hence, we shall explore more into details for this part in future in order to come out with a low dynamic power dissipation memory array without degrading the performance of the memory array.

However, unfortunately for the verification on static power consumption, the proposed design didn't produce the result as what expected, on the contrary increase the power dissipation. The potential problems has been discussed in the section before. Firstly will be the lack of available design model for Electric VLSI, what used in this proposal is 300nm C5 models. Secondly, there is no low leakage transistor type available in

Electric VLSI to use as power gate in the proposed design. Moreover, lack of online open source for circuit designing and evaluating tools, Electric VLSI is the only open source that could be found for circuit designing, however, it is definitely not the ideal one.

Therefore, in order to improve the design, some modifications on the proposed design is necessary to bring into future work. Firstly, 90nm or even smaller design models need to be included. Next, a proper tool for circuit-level design entry is a must in order to evaluate and observe the power dissipation accurately. Besides that, due to overall Vt variations throughout a full design has significant effect on performance and power dissipation, the tools that going to be applied must contain various transistor types, at least two so that low-leakage can used in non-critical path especially for the power gate which is the heater and footer transistor which we added inside proposed design while nominal transistor can be used for the rest of the part in whole circuit. Besides all these, others low-power techniques for example stacked transistors also should be carried out in future so that the best techniques could be found after doing all the research and analysis.

In conclusion, due to the highly concern towards power efficiency of register file, there are still a lot of modifications and improvements need to be made in the proposed design which focus on the memory array section in order to achieve power reduction without performance penalties.

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