LOW-POWER RF DESIGN:
SELECTIVE POWER-GATED DOMINO MULTIPLEXER

By

ONG ZI YONG

A REPORT

SUBMITTED TO

Universiti Tunku Abdul Rahman

In partial fulfilment of the requirements

For the degree of

BACHELOR OF INFORMATION TECHNLOGY (HONS)

COMPUTER ENGINEERING

Faculty of Information and Communication Technology

(Perak Campus)

JAN 2014

DECLARATION OF ORIGINALITY

I declare that this report entitled "LOW-POWER RF DESIGN: SELECTIVE POWER-GATED DOMINO MULTIPLEXER" is my own work except as cited in the references. The report has not been accepted for any degree and is not being submitted concurrently in candidature for any degree or other award.

Signature : _____

Name : Ong Zi Yong

Date : 7th April 2014

ACKNOWLEDGEMENTS

I would like to express my most sincere thanks to Universiti Tunku Abdul Rahman for providing me an opportunity to participate and work in this project. Besides that, I gratefully acknowledge UTAR facilities such as library and Intel microprocessor lab which provide me a convenience during completing my project.

Besides that, I would like to express my sincerely appreciation to my supervisors, Mr Kuek Chian Shiun for his guidance and help. Mr Kuek Chian Shiun shows his patience and intelligent when guiding me to complete this project, without his patience and unconditional support, this project would not be completed successfully.

Last but not least, my friends, Moon Jia Min and Chiang Jia Yeong are also the people that help me a lot in this project. Thank for their suggestion, opinion, and willing to share their knowledge with me during the time I completing this project

ABSTRACTS

A register file acts an important role in a computer's central processing unit (CPU) which is memory storage. Nowadays, reduction of the power consumption is prior consideration in CPU design due to the high power consumption of CPU. In this project, some selective power-gated domino multiplexer design will be introduced which used in low-power register and expected to reduce the power consumption of register file. On top of that, selective power-gated and drowsy memory and selective-power-gated address decoder have to develop and work with the selective power-gated domino multiplexer to construct a low power register file. Furthermore, the register file with power-gated technique is able to maintain its operation when some part in address decoder, memory array and domino multiplexer is powered off which mean the power consumption of the register file is expected to be reduced. Therefore, a low power register file can directly save the power consumption of CPU.

TABLE OF CONTENT

LIST OF FIGURE

LIST OF ABBREVIATIONS

CPU	Central Processing unit
TDP	Thermal Design Power
VLSI	Very Large Scale Integration
LBL	Local Bit-line
GBL	Global Bit-line
RDWL	Read Word-line
SRAM	Static Random Access Memory
LCR	Leakage Current Replica

Chapter 1: Introduction

1.1 Project Background

A register file is a means of memory storage within a computer's central processing unit (CPU). Modern integrated circuit-based register files are usually implemented by way of fast static RAMs with multiple ports. With fast static RAMs, there are many bits of memory that are labeled according to binary code. The status of each memory bit is labeled with a zero or one, indicating an active or inactive state. Nowadays, a lot of high technology products in human life are containing the central processing unit (CPU) such as tablets, computer, smart phone and so on.

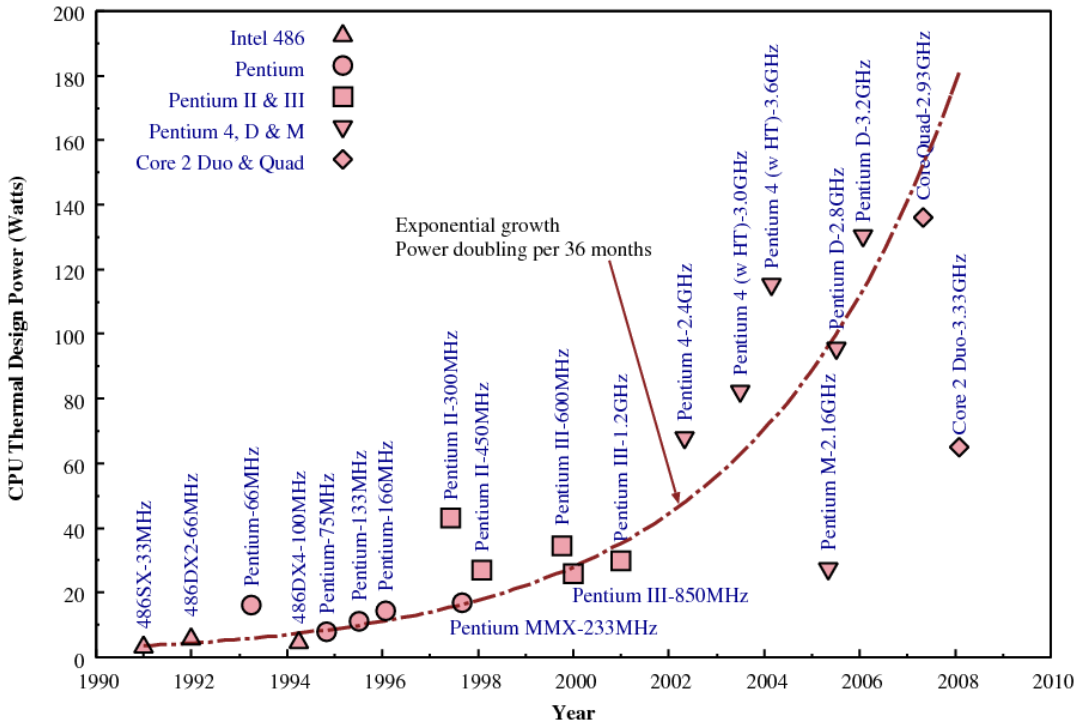

Fig 1 Power Trend from 1990 to 2010. Figure adapted from http://arch.naist.jp/Files/2011/energy_efficiency_arch.html

Fig 1 shows the power trend from 1990 to 2010. This can be seemed that the power consumption of the CPU is getting high and higher from 1990 to 2010. However, the power trend was change after 2008 year. The manufacture of CPU such as Intel is starting focus on the power consumption issue and promoted less power consumption but high speed processor. For example, the Intel Core 2 Duo processor has a lower power consumption compare to Intel Pentium 4 processor. The maximum TDP (Thermal Design Power) of Intel Core 2 Duo processor is only between 65w but TDP of Intel Pentium 4 is about 115w. Nowadays, the maximum TDP of newest CPU with Haswell architecture, 4th Generation Intel Core i7 processors is only 65w but it have much better performance compare to other 2 old version processor. Therefore, reduction of power consumption is nowadays becoming the first consideration in CPU design while the first consideration of CPU design is on power reduction but with the consideration that performance of the CPU must be maintaining or upgrading. For this project, it is going to study on the power consumption of the domino multiplexer which located inside register.

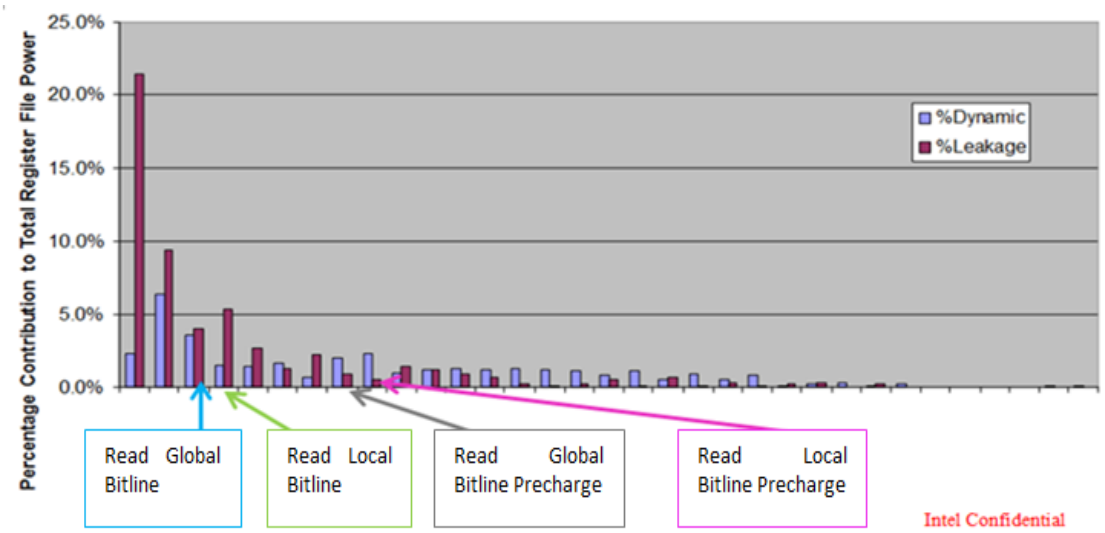

Fig 2 percentage contribution of total register file power

Generally, almost all the IC manufacturers of mobile, hand-held devices, computer is facing the power consumption issue and they have come out a lot of method to solve this problem. For example, the register file that located inside Intel Haswell processor. Register file is consuming about 27% from the overall power consumption of Haswell processor while the domino multiplexer consume the power when read process which is Read Local Bitline, Read Global Bitline, Read Local Bitline(LBL) Precharge and Read Global Bitline(GBL) Precharge. In addition, the domino multiplexer consumes highest leakage power when Read Local Bitline process is carried. Therefore, this project will study the reduction of the power of domino multiplexer. A low power methodology is proposed for the domino multiplexer used in register file which is selective power-gated domino multiplexer.

1.2 Problem Statement

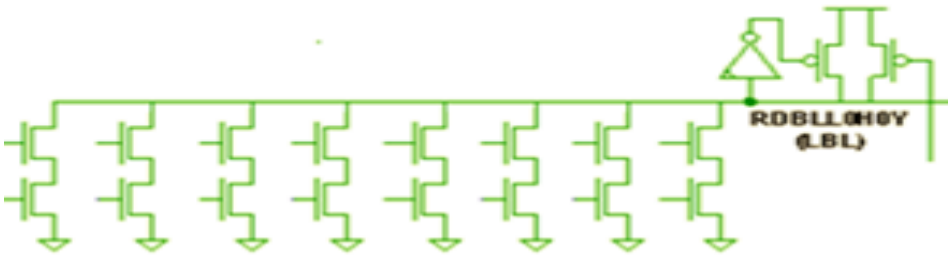

Fig 3 Circuit structure of domino multiplexer in register file.

Fig 3 is a circuit structure of domino multiplexer in register file. According to the circuit structure above, local bitline (LBL) of the circuit will keep at level '1' (on) by the keeper circuit when it is not being access. However, there will be a large leakage power because there have a large pull down network even all of the LBL is in off-stage.

However, Intel invented a method that able solve this problem which called on-demand precharge. The advantage of this method is it able to turn off the precharge circuit when the LBL is not being access in order to save the leakage power. Nevertheless, this will come out another problem when the charge-down or/and charge-up process happens too frequently as the dynamic power in that situation may surpass the leakage power.

As a conclusion, there have few problem existing before and after the on-demand precharge being implemented. Therefore, this project is going to study and evaluate these problems by propose 2 power-gated schemes for the conventional domino multiplexer design which existing in register file nowadays.

1.3 Project Scope & Objectives

1.3.1 Project Objective

The general objective of this project is **to study and verify the power efficiency of existing conventional domino multiplexer which used in register file** by comparing power consumption and time delay of proposed design and existing conventional domino multiplexer design.

The first objective of the project is to **compare the strength and weakness of 2 proposed power-gated schemes for domino multiplexer**. 2 power-gated scheme for domino multiplexer are naming as single LBL float with complex gate isolation and double LBL and read-merge float with isolation MOS. The Power-gated is control by the RDWLs (read word-line) which are output of the decoder and it will gate the precharge and keeper circuits which are not being access.

The second objective is **examining the efficiency of power reduction when domino multiplexer is gated based on on-demand and block validity** (block is empty or with data). The selective power-gated domino multiplexer only operates when required to perform read operation and it will be in rest mode (floating state) when not being accessed. This project is to study and evaluate the leakage power consumption of selective power-gated domino multiplexer which included a low power methodology, power gating. Moreover, the block validity and on-demand are the condition that decides the mode of selective power-gated domino multiplexer domino multiplexer either operate or rest mode.

1.3.2Project Scope

This project is to study the power efficiency of the proposed selective power-gated domino multiplexer by analyzing their power consumption and time delay. This selective power-gated domino multiplexer is designed base on a low power methodology called power-gate. There are few developments will be carried on selective power gated domino multiplexer.

1. Compare the strength and weakness of 2 power gated scheme for domino multiplexer in term of power saving and time delay.

2. Take on-demand and block validity as a case study to examine the efficiency of power reduction of the power-gated domino multiplexer.

1.4 Innovation / Contribution

The main contribution of this project is to study the power efficiency of the conventional design after this project proposes two different power-gated schemes for domino multiplexer. These 2 different power-gated schemes are expected to reduce the power consumption of conventional domino multiplexer design. The reduction of the power consumption of the domino multiplexer is directly affect the overall power consumption of whole CPU. In order to design a new high technology product, power reduction is one of the important aspect that designer must consider. The reduction of power also provide a chance to CPU designer, they can increase the performance of previous version CPU with less power consumption.

This project is to study the power consumption and time delay of register file's domino multiplexer which included power-gated technology. The advantage of the power-gated domino multiplexer is the only one domino multiplexer which is valid and being access will be in operation mode and the other domino multiplexers in

register file which are not being access will be in rest mode (floating state).

The floating state in the LBL of the domino multiplexer is that the state in LBL is neither '1' nor '0'. The domino multiplexer will be powered down and in a floating state if it is not being access. However, the LBL will be reset automatically from '1' to '0' due to the leakage power and this process is expected to consume minimal power because the LBL is pulled down to '0' after leakage of existing charge.

1.5 Methods / Technology Involved

In this project, a technology is involved to ensure the project is successfully completed, which is semiconductor C5 mocmos 300nm models design environment. All the schematics design in this project is created based on C5 mocmos 300nm model design environment.

An Electric design automation tools is also involved in this project which is Electric VLSI Design System. Electric VLSI is used to draw the schematics of the conventional domino multiplexer design and two proposed selective power-gated domino multiplexer design.

In addition, a SPICE simulator is used in this project which is LTspice IV. LTspice IV is a high performance SPICE simulator, schematic capture and waveform viewer. The timing delay and power consumption of the schematic are observed by using LTspice IV.-

Lastly, the base domino multiplexer design is come from some conventional design which existing in register files nowadays and it will be the reference and benchmark for the proposed selective power-gated domino multiplexer

Chapter 2 Literature Review

2.1 Low Power Techniques

This project is going to reduce the power consumption of the domino multiplexer that located inside register file. There are few existing low power techniques that have been successfully reduces the power consumption of the CPU.

Transistor sizing is one of the existing methods to reduce the power consumption. Transistor sizing reduces the width of transistors in order to reduce their dynamic power consumption. However, reduction of the width also cause the transistor's delay become longer and thus the transistor lie away from the critical paths of a circuit are most suitable for this technique. In order to applying this technique, the suitable transistor will be the transistor with tolerable delay which varies depending on how close that transistor to the critical path .Then, each transistor will be sizing to be as small as possible without violating its tolerable delay.

Transistor reordering is other methods to reduce the power consumption. The arrangement of transistors in a circuit will affect the power consumption.

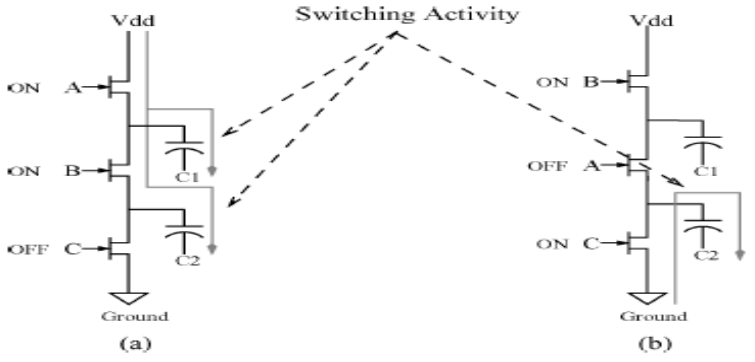

Fig 4 Transistor Reordering. Figure adapted from Venkatachalam, V. et al. 2005

Fig 4 shows 2 type of transistor ordering of same circuit that differs only in the position of transistor A and B. Suppose that transistor A and B is on and the transistor C is off, the current is able flow from VDD and charge the capacitor C1 and C2. Now the condition is change, assume that transistor A is off, while transistor B and C is on. In fig 4(a), the current from ground will flow through transistor B and C and discharge the both capacitor C1 and C2. On the other hand, in fig 4(b), the current from ground only flow through transistor C and discharge the capacitor C2 only but not both as in fig 4(a). Thus the implementation in fig 4(b) cause the more reduction power compared to fig 4(a). Transistor reordering is to rearranges the position of transistors in order to minimize their switching activity. One of the guiding of this principles is to place transistor which switching frequently closer to the circuit's output in order to prevent domino effect where the switching activity from one transistor affect other transistor in the circuit and causing power dissipation. Therefore, this technique requires determining which transistor has the most frequently switching activity.

Half swing clocks is one of the methods that fulfill low power design.

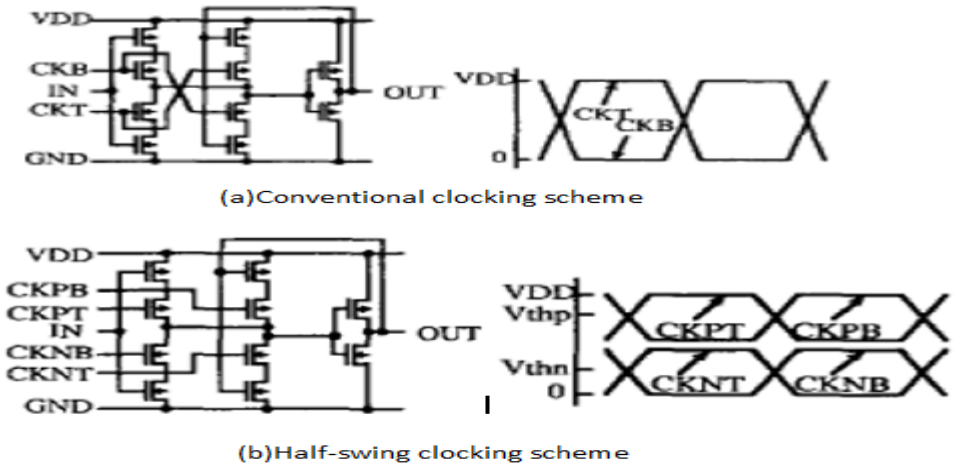

Fig 5 Half-swing clocking scheme. Figure adapted from Kachhara, D. et al. 2012

Half swing clock allows us to reduce power consumption of clocking circuitry but is retained for all other circuit in the chip. Fig5 show the half swing clocking scheme compared to the conventional clocking scheme. In conventional clocking scheme, a conventional latch is gated by 2 full swing clocks. To decrease the clocking power, the half swing clocking scheme use 2 separate clock signals for NMOS and PMOS respectively. For the NMOS, the clock is swing from zero to half VDD and the clock of PMOS is swing from VDD to half VDD. This technique is able to reduce the power consumption in clocking circuitry.

Gate level power optimization is one of the existing methods that able to reduce the power consumption and cell sizing is an example of gate level power optimization. For **cell sizing**, the tool cans selectively increase and decrease cell drive strength throughout the critical path to achieve timing and minimize the dynamic power. Besides, **buffer insertion** is other example of gate level power optimization. In buffer insertion, a buffers insert is better than increasing the drive strength of the gate itself.

Multi supply voltage (Vdd) is other existing methods to lower the power consumption. Reducing supply voltage is the most effective way for dynamic power reduction. By considering power consumption and performance tradeoff, we may apply different supply voltage to different block of a chip based on their performance requirements.

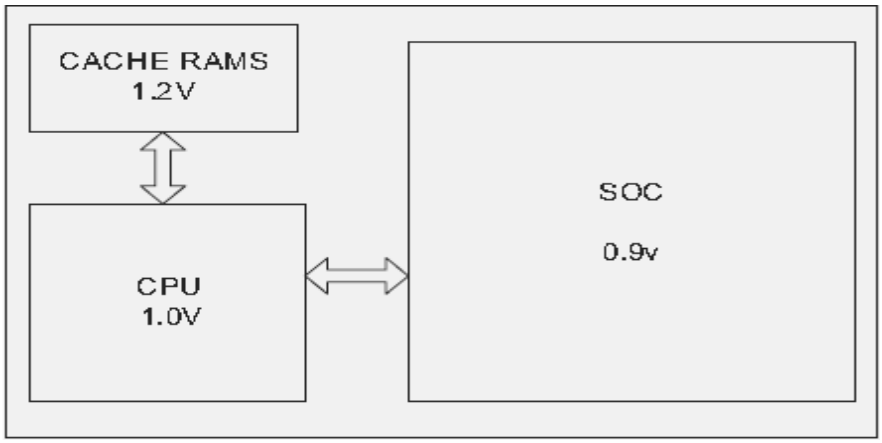

Fig 6 Multi-Volatege Architecture. Figure adapted from Flynn, D. et al. *2009.*

Fig 6 is the example for multi Vdd. In architecture, the cache RAMS are taking the highest voltage because they are on the critical timing path. On the other hand, the CPU runs at high voltage because system performance is determined by CPU performance. However, CPU need lower voltage compare to cache because the overall CPU subsystem performance is determined by the cache speed. The rest of the chip can run at low voltage will not impacting the overall system performance. Therefore, each major component of the system is running at the lowest voltage consistent with fulfilling system timing. This technique can save the power of a system.

Last but not least, **clock gating** is another technique to reduce the power consumption. Clock gating can save dynamic power for both of the register being gated and the clock network between clock gated cell and the registers. A block usually needs clocking only when required and the clock could be gated off in stand-by/ sleep mode when the scheduled task are completed. The challenges of this technique are to identify suitable control signal for the clock gating and have a good

clock management. Besides, the engineers should use clock buffer with proper driving strength in order to avoid unnecessary power consumption of clock network.

2.2 Power-gating

There are several type of transistor in the industry nowadays such as high spend transistor, nominal transistor and low-leakage transistor. Each type of transistor has strength and weakness respectively. Table 1 is going to show the difference between these 3 type transistors.

	High Speed	Nominal	Low-leakage
Speed	Fast	Normal	Slow
Leakage power of the transistor	High	Normal	Low

Table 1

According to table 1, high speed transistors have the fastest speed but highest leakage power. Therefore this type of transistor is suitable implemented at the circuits which give priority on time-delay. On the other hands, the nominal transistors have the moderate speed and leakage power. So that, this type of transistor normally will be implemented in the logic gate because logic gate usually need the balance between time-delay and power consumption. Lastly, low-leakage transistors have the lowest leakage power but it has the longest time delay. Therefore, this type of transistor is suitable for the circuits which give priority on the power saving such as power-gating.

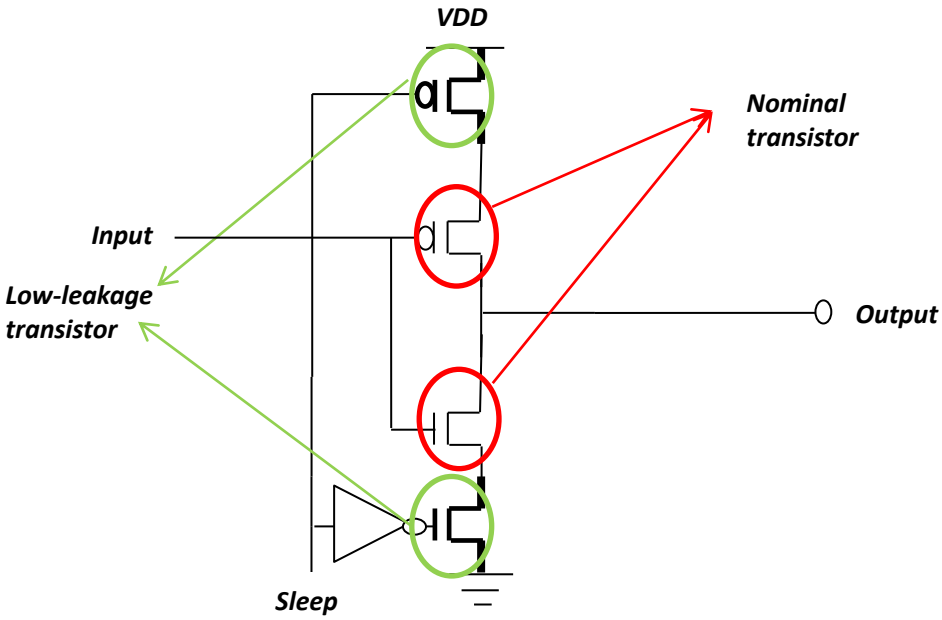

Fig 7 The example of implementation of transistors that mentioned.

Fig 7 show that a power-gated inverter's circuit structure. The power-gated transistor is implemented by using low-leakage transistor to save the power consumption. On the other hand, the inverted is implemented by use nominal transistor in order to get the balance between power consumption and time delay.

In fact, reducing power consumption has become very important issue in nowadays due to increase in transistor density and clock frequency as well as consumer trends in high performance, portable and embedded application. In addition, the leakage power significantly increases due to the high transistor density, oxide thickness and reduced voltage. Fortunately, power-gating is a technique that allows us to saving leakage power and it is effective in reducing leakage power.

Power gating is a technique that designed to reduce the leakage power by shutting off the idle block and shutting on the active block. Basically, the power gating circuit will separate the pull-up network and the pull-down network of the idle block from the Vdd and Vss by using additional transistors, called sleep transistor. The sleep transistors are turned on when the block is in active mode and turn off when the block is in idle mode. This technique able to reduce the leakage power is due to the disconnection of the circuit from the Vdd and/or Vss when it is in idle mode.

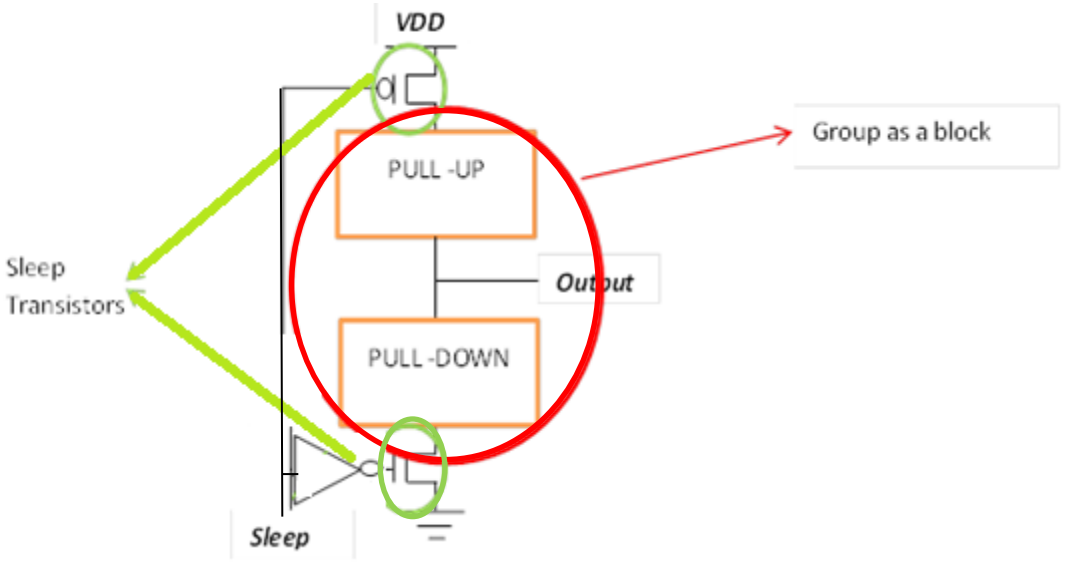

Fig 8 General circuit structure of power gating

Fig 8 show that the basic example for power gated circuit. In fig 8, supposes Sleep = 0, then the circuit is work normally. However, if the Sleep =1, then the block will be separate from Vdd and ground. This will causing the state in the block become floating and finally automatically reset to 0 due to leakage.

There is 1 challenge that need faced by power gating design which is the output from the power gated block will ramp off slowly. This will causing large crowbar current in the always powered on block due to these output spend more time at floating state. To solve this problem, isolation cell are introduced. The isolation cell placed between the outputs of the power gated block and the input of the always powered on block. The function of this isolation cell is to ensure the always on block do not have crowbar current when one of the input is at floating state due to the power gated block is powered off and this isolation cell receive the control signal from power gating controller.

The basic way to solve the floating output of the powered down blocks is to use an isolation cell to make the output to either '1' or '0'. One of the isolation techniques is using logic gate which is AND and OR gate as the isolator. In active high logic, the most common way is using an AND gate to make the output to '0'. For active low logic, the most common way is using an OR gate to make the output to '1'.

Fig 9 Isolation cells by using logic gate. Figure is adapted from Flynn, D. et al.2009.

In fig 9(a), an AND gate is used as the isolator. When the active low isolate signal "ISOLN" is '1', the signal pass to the output while the 'ISOLN' is '0', the output is forced to '0'. For fig 9(b), a OR gate is used as the isolator. When the active high

isolate signal “ISOL” is “1”, the output is forced to “1” while the “ISOL is’0’, the signal pass to the output.

An alternative isolation method is using pull-up or pull-down transistor instead of logic gate. However, this method is requiring careful sequencing to prevent contention in the output.

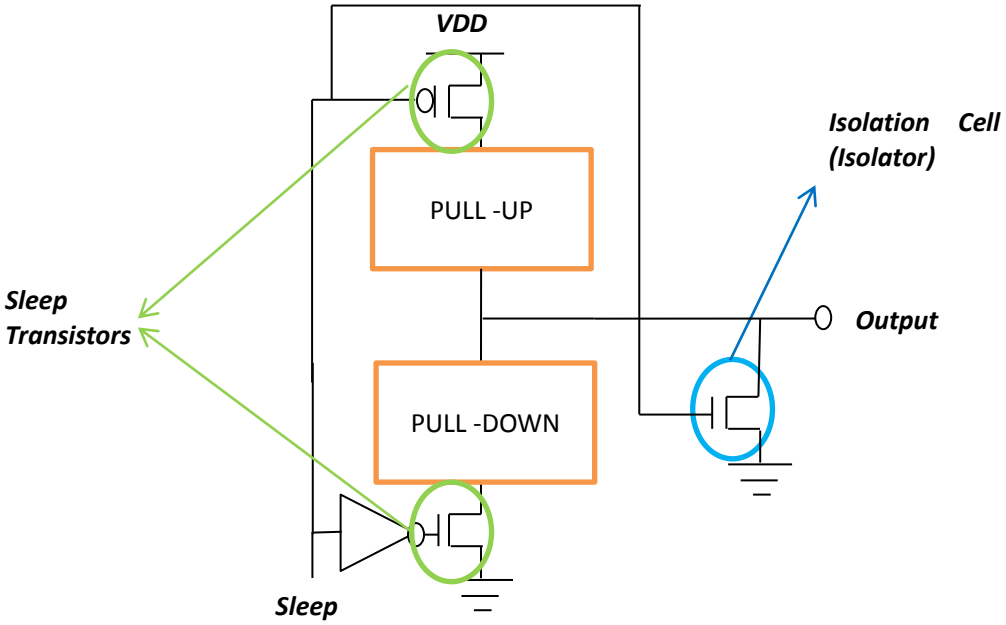

Fig 10 Isolation cell by using pull-down transistor

Fig 10 is an example of additional pull-down transistor in a power gating circuit. The isolation cell able to solve the floating output issue by pulling the signal to ‘0’. However, if there is necessary to make it output is ‘1’, the isolation cell can be built by PMOS and connected to Vdd.

2.3 Register File Architecture

Before discuss about register file, a close cousin of the register file will be introduced first which is Static Random Access Memory (SRAM). Nowadays, SRAM is the fundamental and important technology for memory design. The advantages of using SRAM are high speed, robust and easily implemented in standard logic processes.

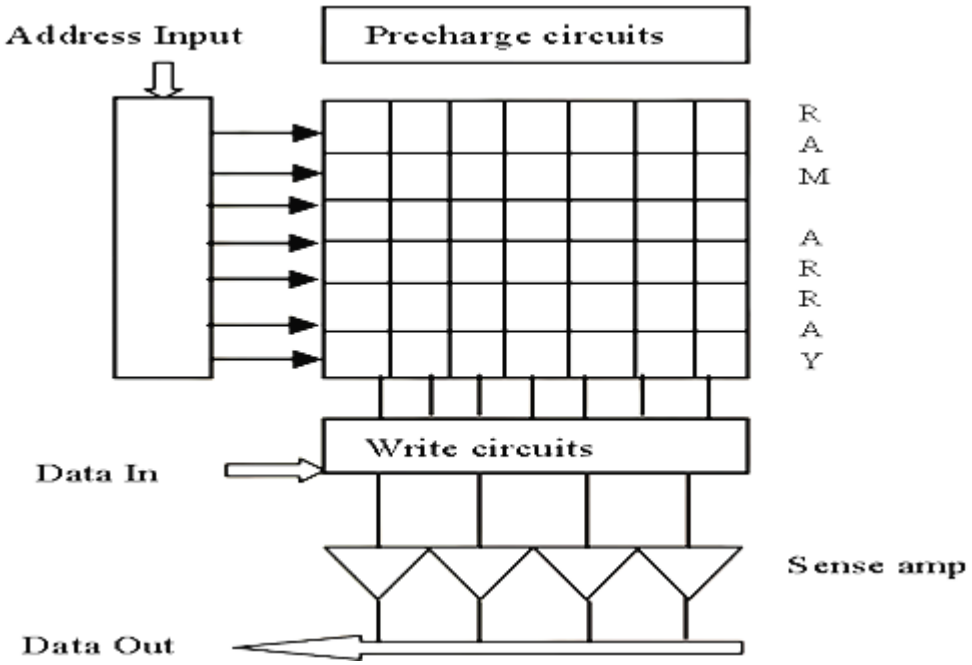

Fig 11 General SRAM Architecture. Figure adapted from Santhi Swaroop, V.G. et al, 2012.

Fig 11 show the general SRAM architecture diagram. Generally, a SRAM formed by row decoder, SRAM array, sense amplifier and precharge circuits. For the SRAM array, it consists of a group of SRAM cells and each column of SRAM cell share the same bitline.

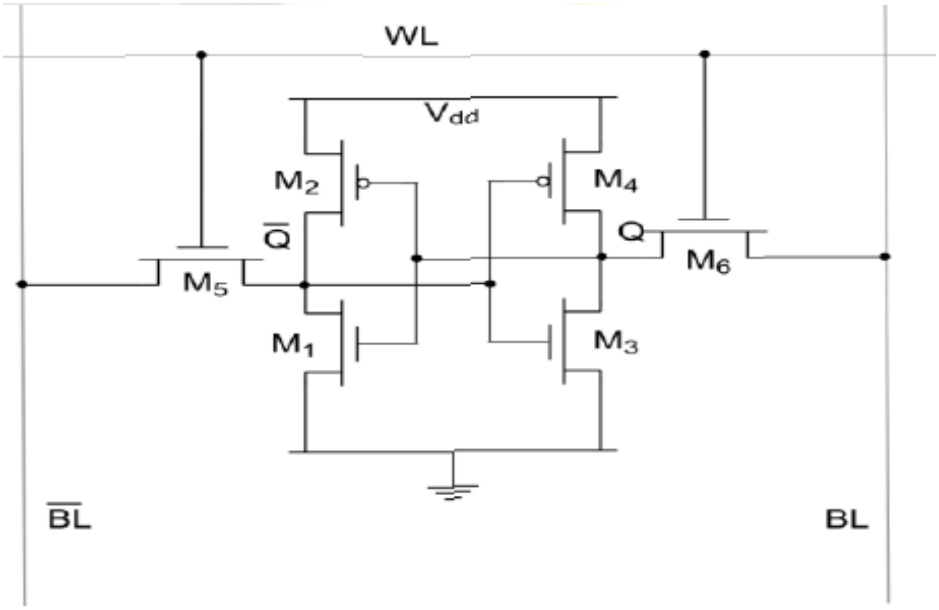

Fig 12 6T SRAM cell. Figure adapted from Santhi Swaroop, V.G. et al, 2012.

Fig 12 show the transistor level circuit of 6T SRAM cell. It has a two cross coupled inverters (Bi-stable Element) which consists of 2 PMOS and 2 NMOS. Besides, 2 NMOS as a access transistor to access the SRAM cell during Read and Write operation. For both of the bitlines (BL and BL'), their functionality is to transfer the data during Read and Write operation in a differential manner. The data and inversed data is provided to BL and BL' respectively to have a better noise margin. The data is stored as bi-stable state in two cross coupled inverters.

Before read operation, the bitlines are precharged to '1' by a precharge circuit. For the precharge circuit, it is implemented base on dynamic logic and the dynamic logic will be discussed later

In addition, the row decoders are used to active the specific row in the array. The decoder decodes the input address and active the wordline. Only one of the rows in SRAM array will be active in Read or Write operation. Fig 13 is an example for 3-5 decoder.

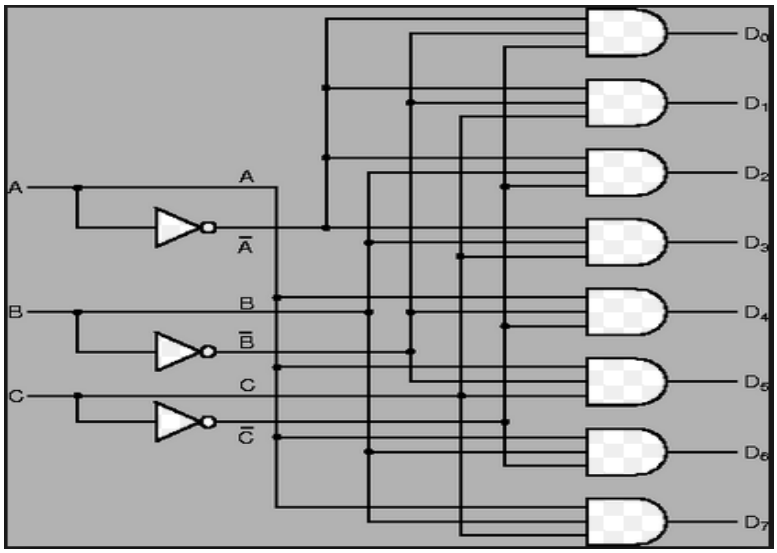

Fig 13 3-to-8 decoder.

Depending on the mode of operation, SRAM cells are connected go both bitlines either sense amplifier read the content in the cell or content in the cell is overwrite by coming data. A sense amplifier is used to read the content in the cell. In addition, it helps the SRAM chip perform faster and reduce the power consumption of SRAM chip by sensing a voltage different on the bitlines. Fig14 is the example of sense amplifier

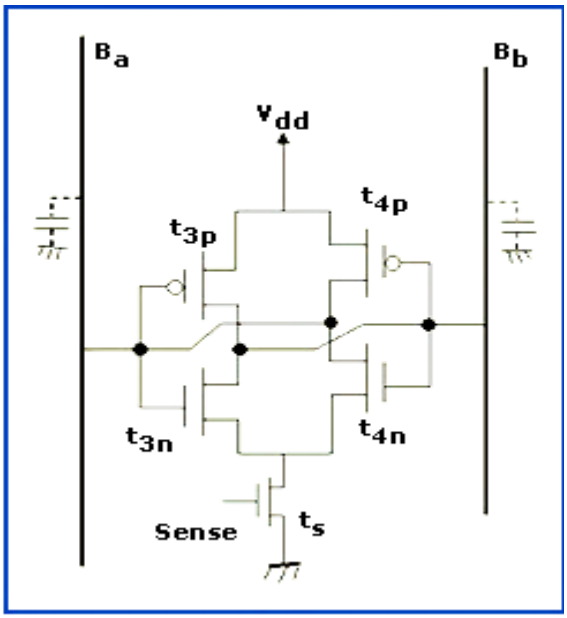

Fig 14 Sense amplifier. Figure adapted from http://www.ami.ac.uk/courses/ami4407_dicdes/u03/

For the register file, it can perform read and write operation in the same time due to separated read port and write port. However, SRAM not able to perform read and write operation in the same clock cycle.

Nowadays, all the processors contain a bank of register which is register file. The function of the register is to provide on-chip memory for the processor in order to prevent the long delay that occurs when the memory of the chip is accessed.

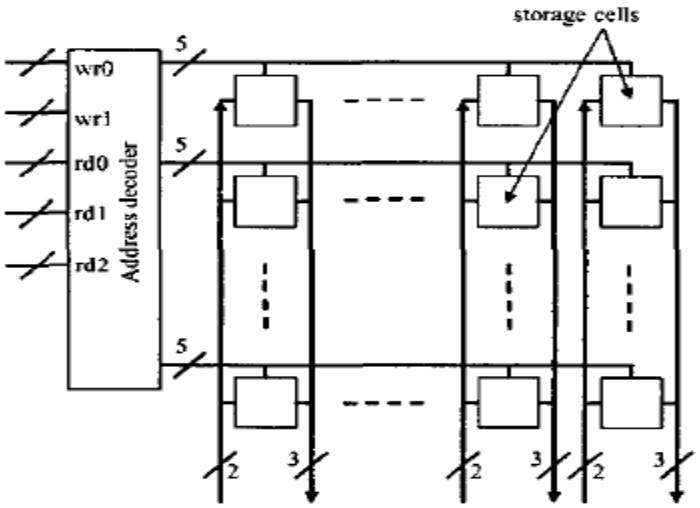

Fig 15 schematic diagram of small multiport register file. Figure adapted from Burgess, N. 2003

There are many way to construct a register file. Fig 15 is an example for the register file architectures that introduced by Neil Burgess. This register file contain 3 read address ports (rd0, rd1, rd2) which the memory address are input through rd0-rd2 and this allow the data in memory array can be available on any of the 3 output buses. This register file also contains 2 write address ports (wr0, wr1) which the memory address are input through wr0, and wr1. These features of this register file allow the register file to read and write multiple data simultaneously.

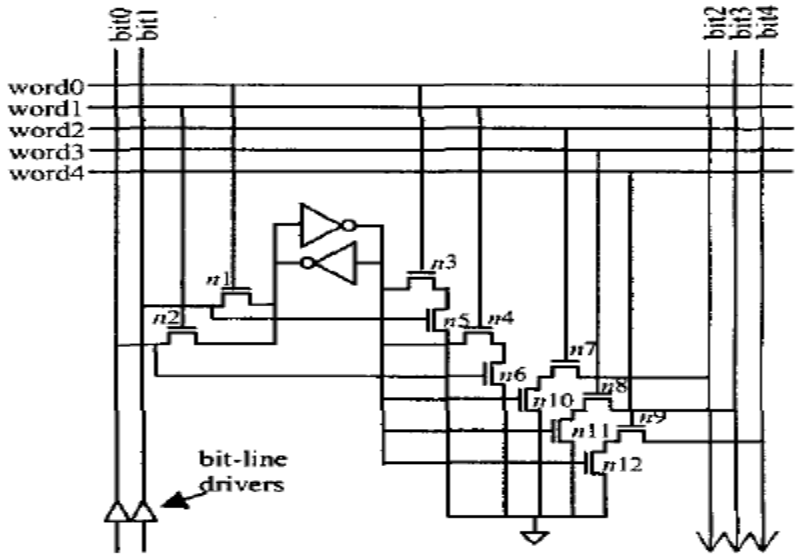

Fig 16 Transistor diagram of the storage cell. Figure adapted from Burgess, N. 2003

Fig 16 is the transistor diagram of the storage cell that used in multi-port register file. The word-lines (word0-4) address individual register in the file while to read or write data to or from the register cells is using the bit-lines (bit2-4).

In read operation, an address will be send to one of the read address port (rd0, rd1, rd2) and the address will be decoded by the address decoder in order to activate one of the word lines, word2-word4. The address is decoded by address decoder and the selected word-line active high. In the same time, the bit-lines, bit2-bit4 (read bitline) precharged to '1'. After that, if the content in the selected register cell is '1', the bit-line will be forced to '0' through one of the n-FET stacks n7-n10 , n8-n11 , or n9-n12; otherwise the bit-line remain '1'. After that, the bit-line pass through read access logic and output the result that is same with the content in register cell. In fact, this is only one of the basic structures of the register cell; there are many variation of structure for register cell.

For the write operation, an address will be send to one of the write address port (wr0,wr1) and the address will be decoded by the address decoder in order to activate one of the word lines, word0-word1. When the access transistor pair (n1-n3 or n2-n4) has been turned on, data will be stored in to the bi-stable element (cross-coupled inverter). If the data is '1', the right hand node of the bi-stable element is pulled to '0' through n3-n5 or n4-n6, otherwise, the left hand node of the bi-stable element is pulled to '0' through n1 or n2.

Generally, read and write operation occur on different phases of the same clock cycle. For example, write operation occurring on the first phase of a cycle to avoid the hazard of a write operation corrupting the read operation which occurring on the second phase. On the other hand, read then write operation is also acceptable due to the write operation in second phase have time to charge lengthy interconnect tracks routed back to the register file location.

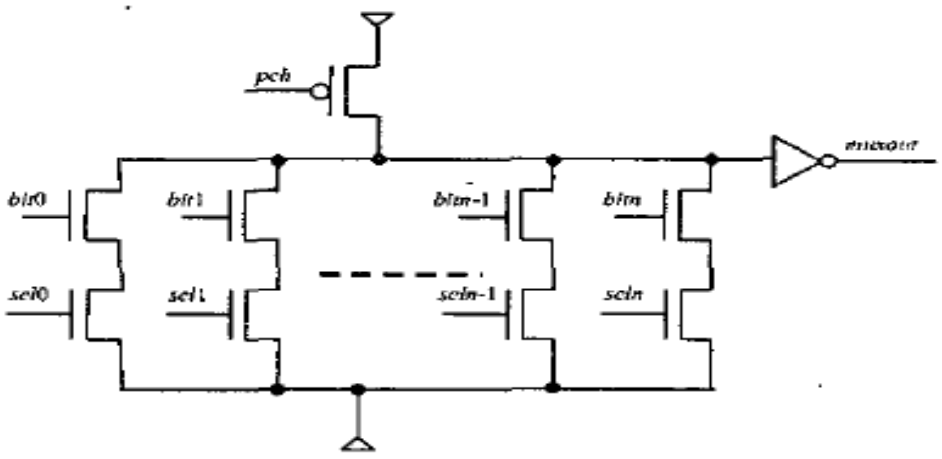

Fig 17 Dynamic logic multiplexer (domino multiplexer). Figure is adapted from Burgess, N. 2003

Finally, the read access logic of this register file is implemented as a multi-input dynamic logic multiplexer (domino multiplexer) which show in fig 17

2.4 Domino Multiplexer Architecture

The concept of dynamic logic is important before going into domino multiplexer. Dynamic logic is one of the design methodologies in combinatorial logic circuit, especially for those implemented in MOS technology. In order to minimize the capacitance of the logic gate input, dynamic logic only implemented in either Pull-down network (PDN) or Pull-up network (PUN). Generally, the dynamic logic circuit is operates in 2 phase which is Precharge phase and Evaluation phase.

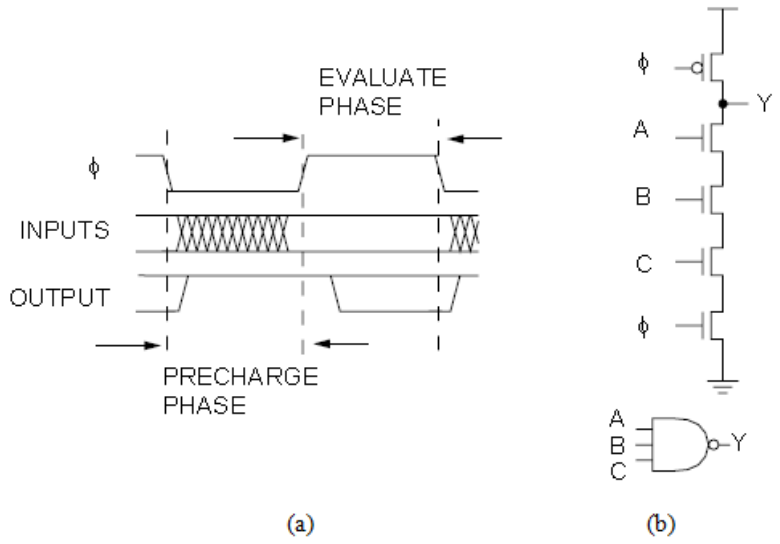

Fig 18 (a) Timing diagram showing the precharge and evaluation phase **Fig 18(b)** Simple dynamic NOR gate. Figure adapted from Jacob, B. et al, 2008

Fig 18(b) show a simple example of the implementation of dynamic logic. In the precharge phase, ϕ is '0'. Therefore .the PMOS precharge transistor that connected to Vdd will precharges the output Y to '1'. However, NMOS precharge transistor is turned off to avoid the possible inadvertent early discharge of the output and contention. For the evaluation phase, ϕ is '1' and NMOS precharge transistor is turned on. Therefore, if the right combination of the input signals exists, the output node will be reset to '0'. Fig 18(a) show the timing diagram for precharge and evaluation phase. The input of the dynamic gates must designed not to inadvertently discharge the output node and turn on PMOS precharge transistor and NMOS precharge transistor at the same time.

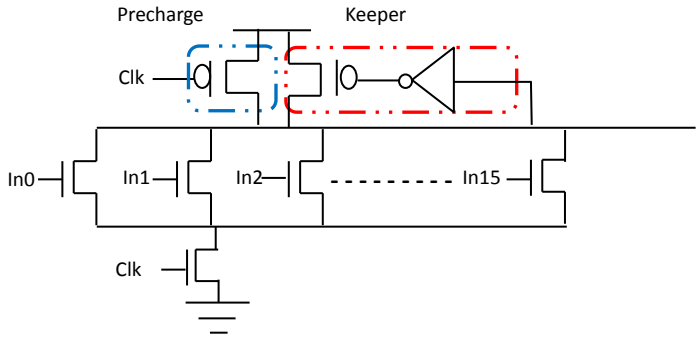

Fig 19 Example of implementation of NOR16 gate using dynamic logic

The advantage of dynamic circuit is fast and compact. Therefore, it is a preferred choice to implement in a large logic cell. Fig 19 is the example of implementation of NOR16 gate using dynamic logic. The keeper circuit is to hold the '1' after precharge phase, but it must be weak enough not to fight with evaluation.

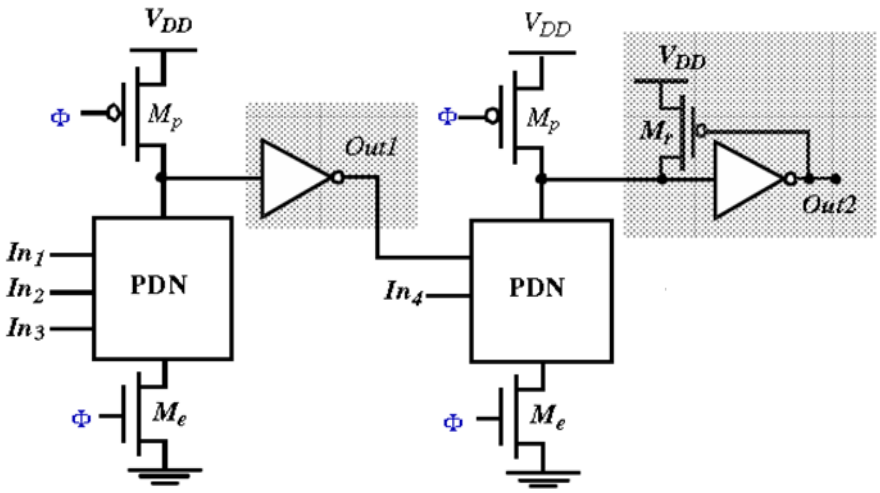

Fig 20 General structure of domino circuit.

Fig 20 shows a basic structure of domino circuit. Domino circuit is a dynamic logic that connected in series. Each of the dynamic circuit is trigger next one and the connected dynamic circuits is evaluate sequentially but precharge in the same time. In addition, domino multiplexer in register file is designed base on domino circuit.

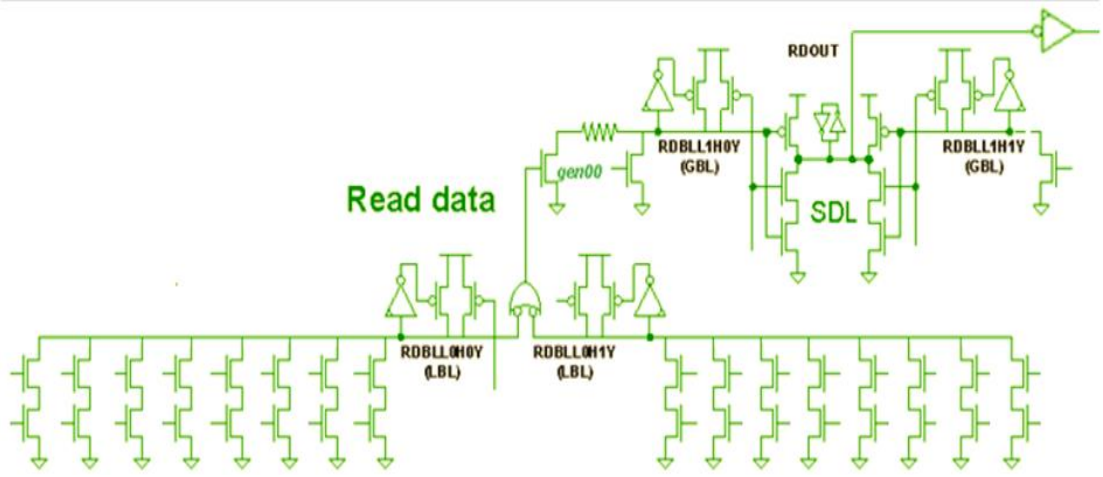

Fig 21 The structure of domino multiplexer in register file.

Fig 21 show that the basic structure of domino multiplexer in a register file. The domino multiplexer is constructed base on domino logic concept. For the domino multiplexer in register file, the local bitline (LBL) and global bitline (GBL) are domino circuit. Both of them are precharged at the same time. However, LBL will evaluate first then the result will pass through the read-merger which is same function with the inverter between two dynamic logics in fig15. After that, the read-merger will output a correct result to GBL, and GBL will operate to output the data that same as the content of the particular memory cell which selected to read.

Domino multiplexer is indispensable for constructiong a high-speed OR and AND-OR gates in CMOS. It need keeper to maintain a '1' during evaluation phase. A conventional keeper is a pFET pull-up network which it must satisfy 2 conditions. First, for the slow-pFET/fast-nFET (sPfN) process corner, the keeper must source sufficient current to overpower the leakage current of nFET logic. Second, for the fast-pFET/slow-nFET (fPsN) process corner, the keeper must be weak enough so that it will not fight with evaluation as a single nFET leg can pull the dynamic node quickly enough. These conditions are contradictory in that increasing the margin for one reduces the margin for the other. As the size of a domimo multiplexer increase, finally a point of zero margins for both constraints is reached. This mean the maximum possible size of domino multiplexer is reached.

Therefore, Lih.Y and his partners who are Tzartzanis.N, and W.Walker.W had introduced a structure of domino multiplexer which is different with conventional structure of domino multiplexer. They present a new keeper which call leakage current replica (LCR) keeper. This LCR keeper is a circuit that addresses the short-comings of the conventional keeper. The LCR keeper using a conventional analog current mirror that able to tracks any process corner as well as voltage and

temperature. However, the random on-die variation is the only variation that LCR keeper cannot track. A single current mirror structure can be shared among more than one domino multiplexer.

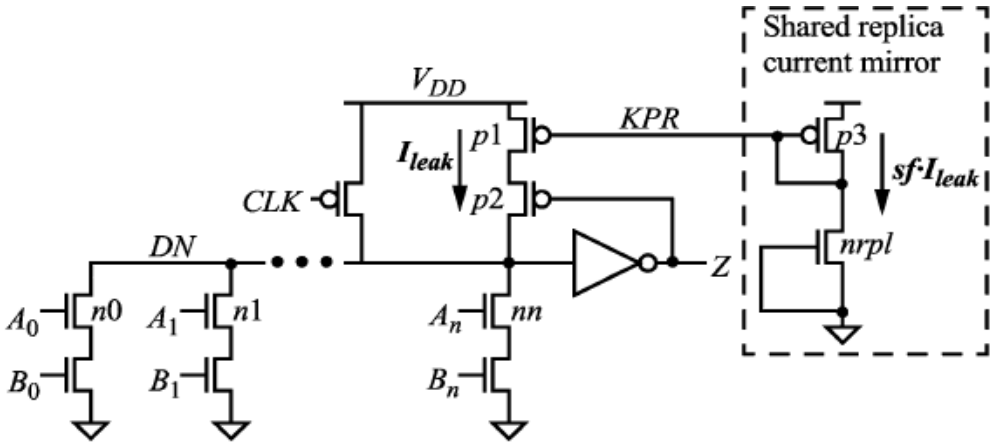

Fig 22 The topology of LCR keeper domino multiplexer. Figure adapted from Lih.Y et al, 2007

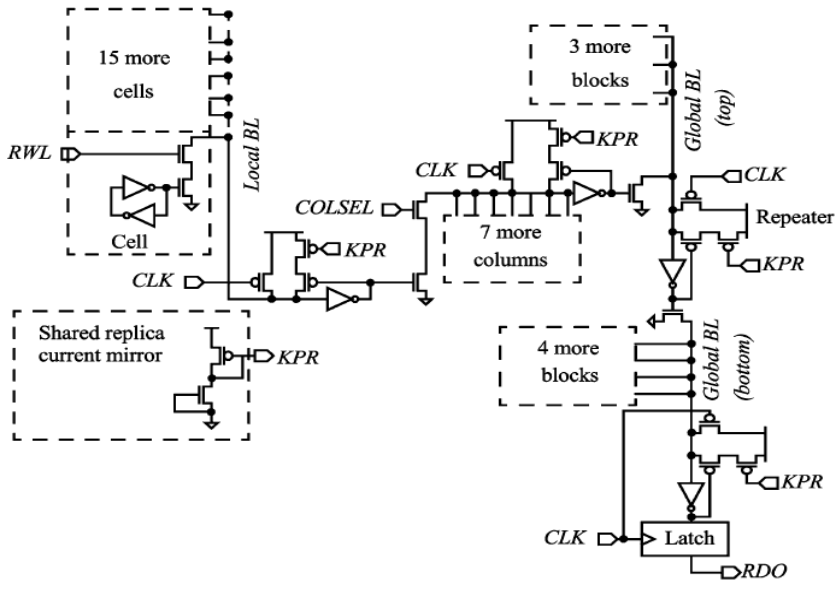

Fig 23 SRAM single-ended four-stage domino read port.. Figure adapted from Lih.Y et

al, 2007

Fig 23 four-stage domino read port from read word line RWL to latched output RD0, which is entirely conventional except for the LCR keepers. In Fig 23, local bit lines (Local BL) connect 16 cells through an AND-OR domino multiplexer. For 2nd stage, it is an eight-leg AND-OR dynamic multiplexer used for column select with local bit line inputs coming from opposing sub blocks. For 3rd stage, it is an OR domino multiplexer to select one of four top blocks. For 4th stage, it is a five-input dynamic OR gate with one of the inputs fed from the top global bit line and the other four fed from the bottom blocks.

Delay Path	Conventional	LCR	Change
CLK → RWL	631ps		same
RWL → RDO	415ps	336ps	-19%
CLK → RDO	1046ps	967ps	-7.6%

Fig 24 Simulated SRAM Access Time, Conventional vs LCR. Figure adapted from Lih.Y et al, 2007

From Fig 24, the result show that the LCR keeper have faster access time compare to conventional keeper. However, the LCR keeper cannot track the random on-die variation which still must be addressed using conventional margining.

Chapter 3 Methodology

3.1 Proposed Power-gated Schemes

This project is going to study the strength and weakness of 2 power-gated scheme for domino multiplexer and evaluate the efficiency of power reduction when domino multiplexer gated by power-gate methodology which depend on on-demand and block validity (block is empty or with data). This methodology is expected to improve the power efficiency of the domino multiplexer that existing in current conventional design. Therefore, the proposed power-gated schemes are expected to reduce the power consumption of the existing conventional domino multiplexer design that used in register file nowadays.

One of the purpose that selective power-gated domino multiplexer is proposed is to improve the limitation of the on-demand precharge which is Intel design nowadays. The power-gate is control by signal from the decoder and it will shut down the precharge and keeper circuit of the domino multiplexer which not being accessed. In addition, two different circuit structures will be proposed which is single LBL float with complex gate isolation and double LBL and read-merge float with isolation MOS.

First proposed power-gated scheme is called single LBL float with complex gate isolation.

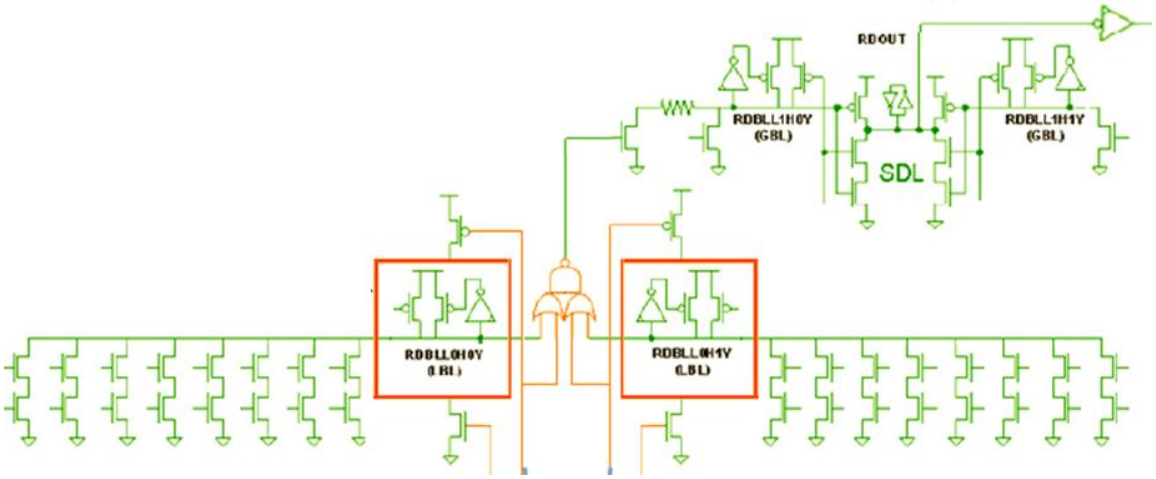

Fig 25 Circuit structure of single LBL float with complex gate isolation

Second proposed power-gated scheme is called double LBL and read-merge float with isolation MOS.

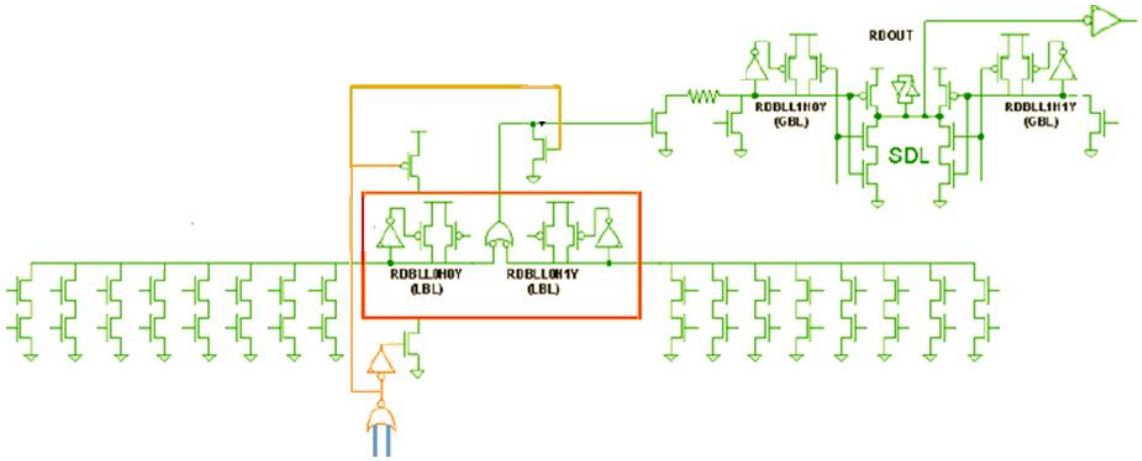

Fig 26 Circuit structure of double LBL and read-merge float with isolation MOS

For single LBL float with complex gate isolation, the basic approach is the LBL will be left to floating state when the domino multiplexer is not being access instead of charging down and charging up the LBL. By the way, LBL will automatically being reset to level '0' due to the leakage power and this process is expected to consume less power because the LBL is pulled to '0' after the existing charge is removed due to leakage power. However, the NAND2 read-merger needs to modify and become a complex gate read-merger in order to solve the floating LBL issue and this complex gate read-merger is expected to output a longer read time-delay because the NAND2 read merge is modified to 4-input complex gate read merge.

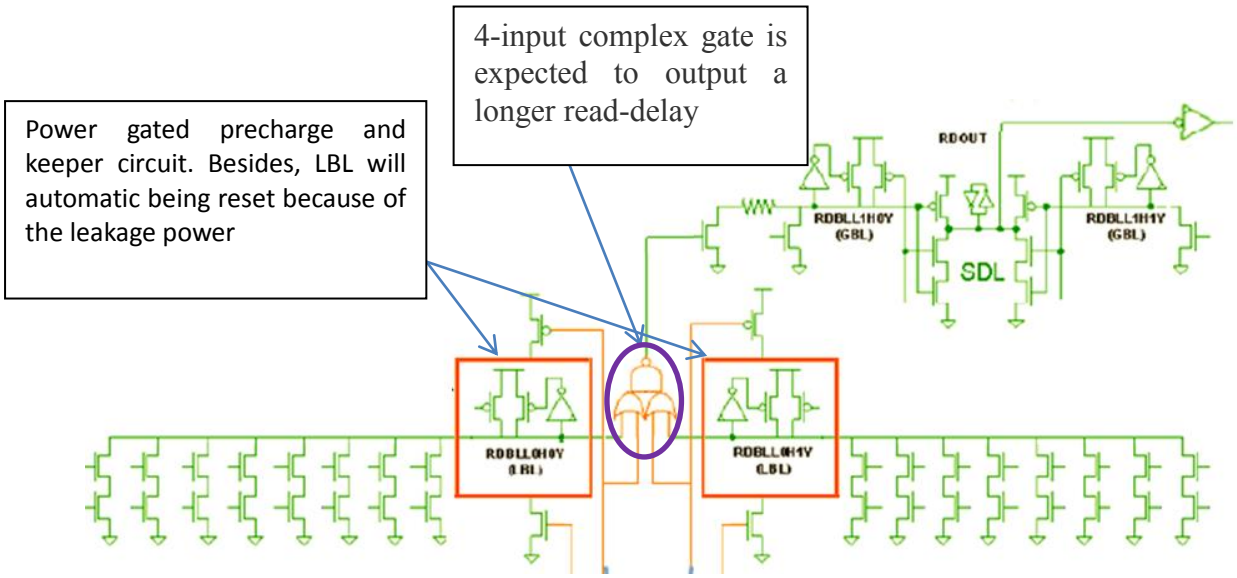

Fig 27 Feature of single LBL float with complex gate isolation

For double LBL and read-merge float with isolation MOS, the basic approach is gating the precharge, keeper circuit and the read-merger as a block. This approach is expected to avoid the longer time delay problem. In addition, a power isolator is added to solve the issue of floating output from read-merger in order to ensure the read-merger will output a '0' signal to the global bitline (GBL) while the domino multiplexer is shut down. Nevertheless, this scheme is less flexibility compared to first proposed power-gated scheme because this scheme needs to turn on/ off double LBL. Turn on/off double LBL in the same time will reduce the power-saving prospect due to the double LBL leakage.

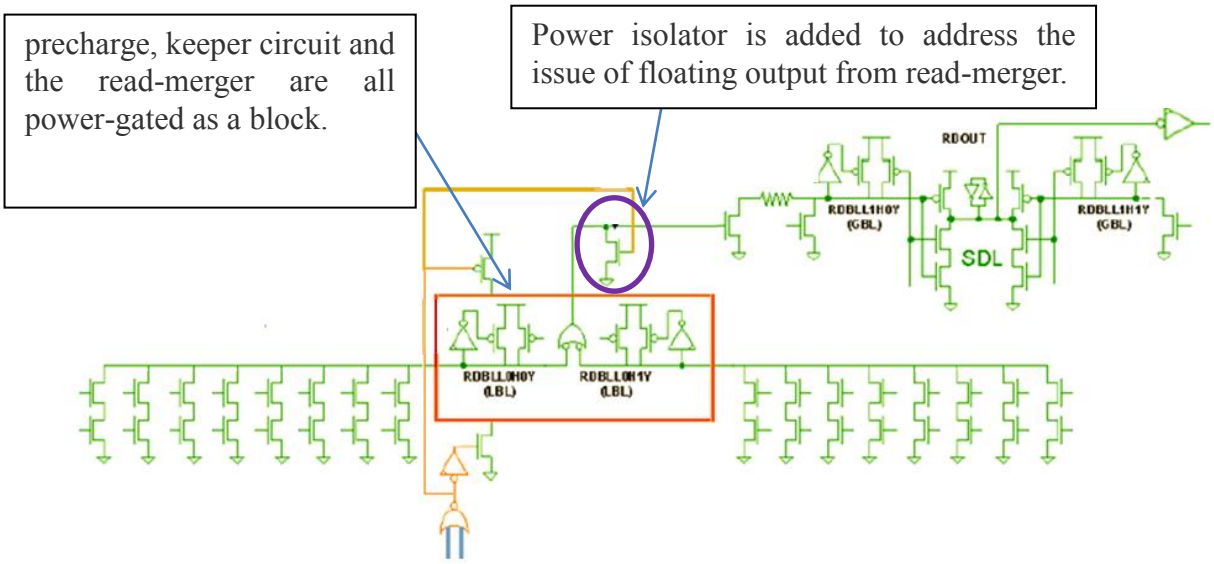

Fig 28 Feature of double LBL and read-merge float with isolation MOS

3.2 On-demand and Block validity

One of the objectives of this project is to examine the efficiency of power reduction when domino multiplexer is gated based on on-demand and block validity. The on-demand power-gated domino multiplexer is powered off when it is not being access, this will causing the reduction of the power but there will be longer time delay. Furthermore, the block validity power-gated domino multiplexer is power-gated domino multiplexer those handle the valid block will be power on. Otherwise, the power-gated domino multiplexer will be power off.

For example, a register file with 32 locations, 5 bits address width and 1 bit of data width is on the read process. The user wants to read the data from memory address 00001. The 32 locations are divided to 4 blocks with 8 locations per block. The register file will take the upper 2 bit of the input memory address to control the validity of the entire blocks. Since the upper 2bit of the input memory address is 00. Therefore the block with the upper address 01, 10, and 11 will be set to invalid, only the block with upper address 00 will be set to valid. After that, the mode of power-gated multiplexers is whether active mode or ideal mode are depending the validity of the block that it handle. In this example, the 1st power-gated multiplexer will be powered on.

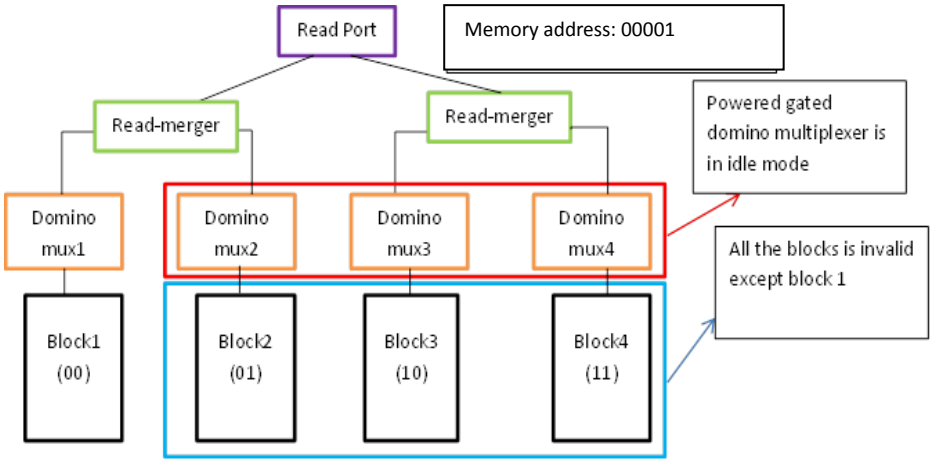

Fig 29 Example of on-demand.

Suppose there are same register file with same specification doing the same process. In block validity, the block is invalid if the storage of all the location in block is invalid. Therefore, the entire domino multiplexer inside the register file is in idle mode.

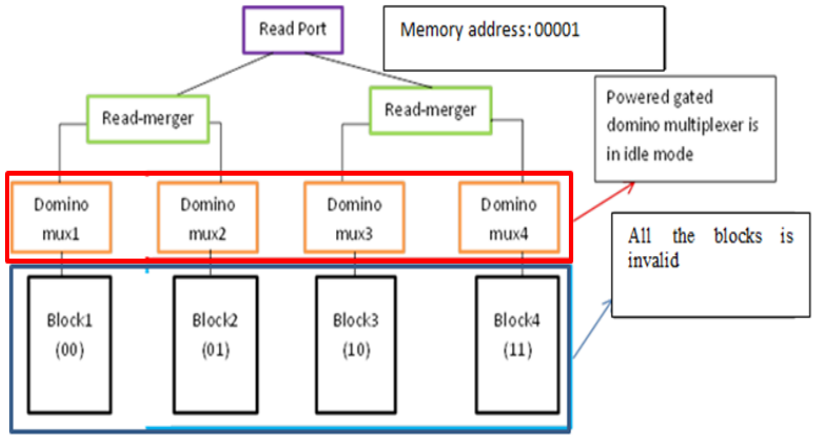

Fig 30 Example 2 of block-validity

3.3 Expected Outcome

Generally, the relationship between power consumption and time delay is inversely proportional. Power consumption become lower, as the time delay will also become longer.

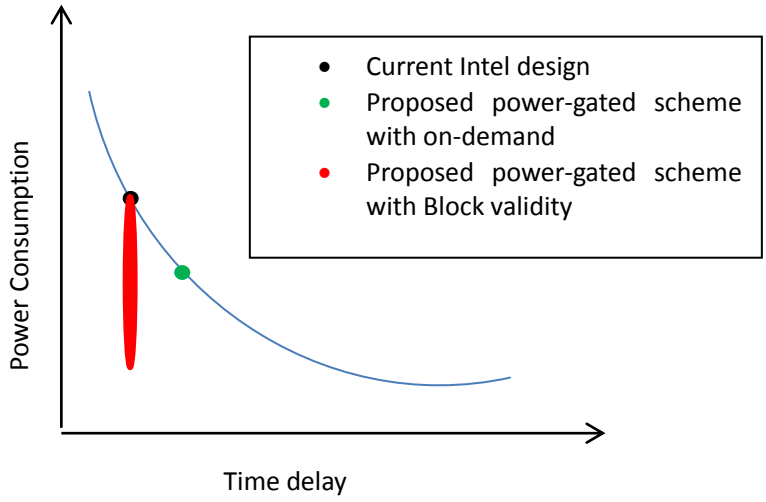

Fig 31 Expected Outcome for proposed power-gated schemes

Base on the Fig30, the expected result is the on-demand power-gated scheme is expected to have lowest power consumption. However, it also expected have longest time delay because input address will be analysis before precharge in order to determine which domino multiplexer will be powered on. For block validity proposed power-gated scheme, the power consumption and time delay is depending on how many block is valid. If there is only one block is valid, the power consumption will be minimize. However, if the entire blocks are valid, the power consumption of the power-gated domino multiplexer will not be reduced which same with the power consumption of the domino multiplexer existing in current Intel design.

Besides that, as what discussed before this, the proposed design 1 which called single LBL float with complex gate isolation is expected have longer read time-delay but

more power reduction compared to the proposed design 2 which called double LBL and read-merge float with isolation MOS. The reason that cause longer time delay on design 1 is because the NAND2 read merge is replaced by a complex gate read merge. In addition, the reason for the design 1 has more power reduction is because the flexibility of LBLs. Design 1 can turn on/off the LBLs independently, while Design 2 only able to turn on/off both LBL in the same time.

3.4 Time Line

3.4.1 Project 1 Time Line

ID	Task Name	Start	Finish	Duration
1	Discussion Topic	27/5/2013	31/5/2013	5d
2	Problem Statement and Project Objective	3/6/2013	5/6/2013	3d
3	Discussion of the methodology	6/6/2013	8/6/2013	3d
4	Preliminary Report (Include Finding Research Paper)	9/6/2013	18/7/2013	40d
5	Submission of Preliminary Report	19/7/2013	19/7/2013	1d
6	Enhancement of Project 1	20/7/2013	17/8/2013	29d
7	Finalization of Project 1	18/8/2013	18/8/2013	1d
8	Poster Preparation	20/8/2013	24/8/2013	5d
9	Oral Presentation of Project 1	26/8/2013	26/8/2013	1d
10	Poster Submission	26/8/2013	26/8/2013	1d

Fig 32 Gantt chart of Project 1

3.4.2 Project 2 Time Line

ID	Task Name	Start	Finish	Duration
1	Set up Electric VLSI Design Environment	13/1/2014	17/1/2014	5d
2	Build Schematic	20/1/2014	28/1/2014	9d
3	Testing Functionally of Domino Multiplexer	10/2/2014	18/2/2014	9d
4	Testing Functionality of Register File	24/2/2014	27/2/2014	4d
5	Evaluation on Speed and Power Consumption	28/2/2014	14/3/2014	15d
6	Documentation and draft report	15/3/2014	21/3/2014	7d
7	Finalization of Project 2 report	22/3/2014	3/4/2014	13d
8	Turnitin check	4/4/2014	6/4/2014	3d
9	Project 2 Report Submission	7/4/2014	7/4/2014	1d
10	Presentation and Poster Preparation	7/4/2014	13/4/2014	7d
11	Poster Submission and Presentation	16/4/2014	16/4/2014	1d

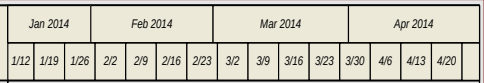

Fig 33 Gantt chart of Project 2

Chapter 4 Implementation & Analysis of Proposed Solutions

4.1 Design and Verification Plan

In project II, the schematics design of conventional domino multiplexer and two proposed selective power-gated domino multiplexer are drew and analyzed by using Electric VLSI. In this project, not only power consumption will be analyzed, but also time delay. All the schematics design in this project is based on C5 mocmos 300nm design environment. Before carry out the analysis on all the schematics, these schematics have been combined with decoder and memory array to ensure all the domino multiplexer schematics design have the correct functionality.

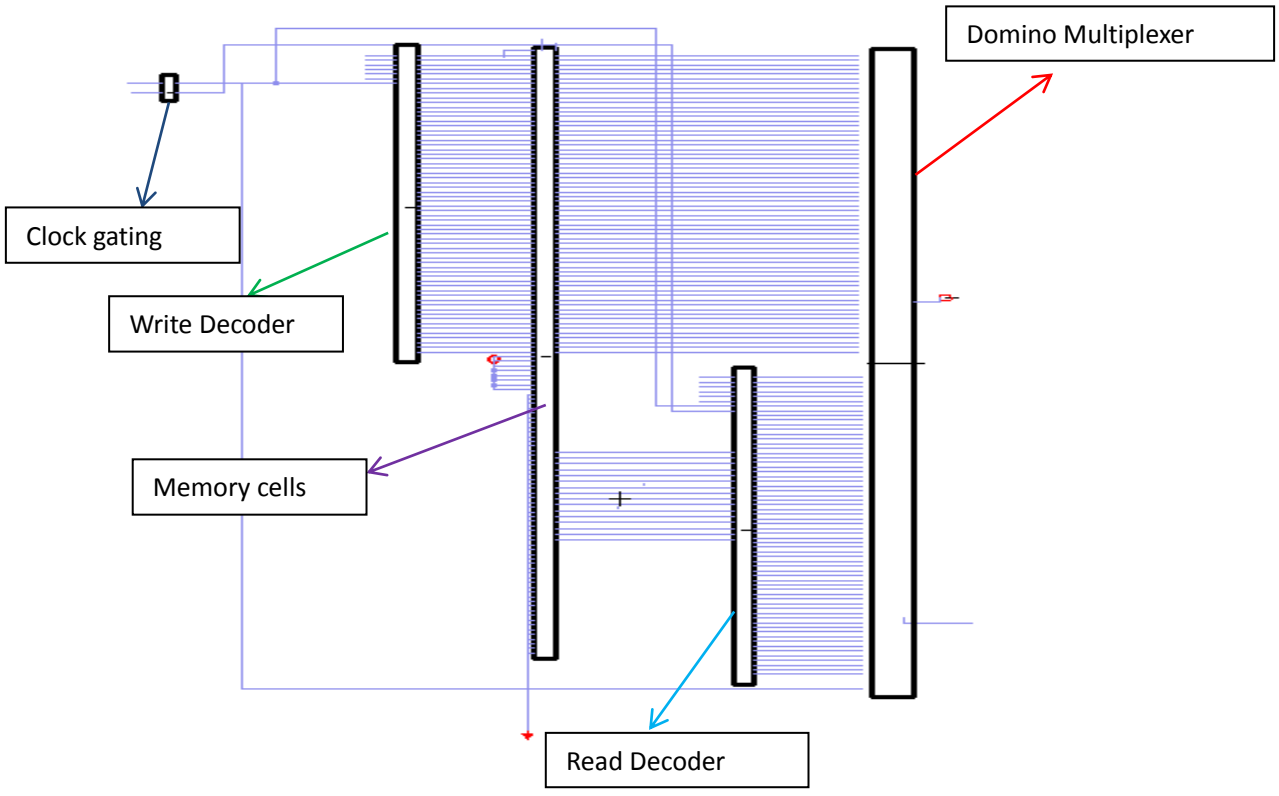

Fig 34 Register File

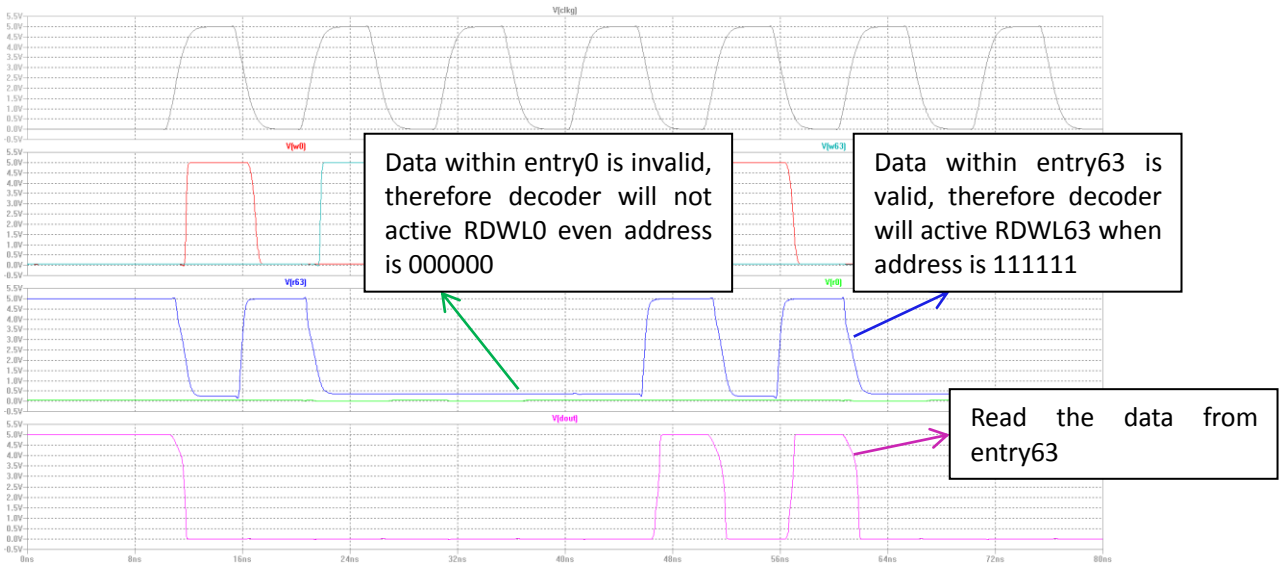

Fig 35 Timing diagram of register file

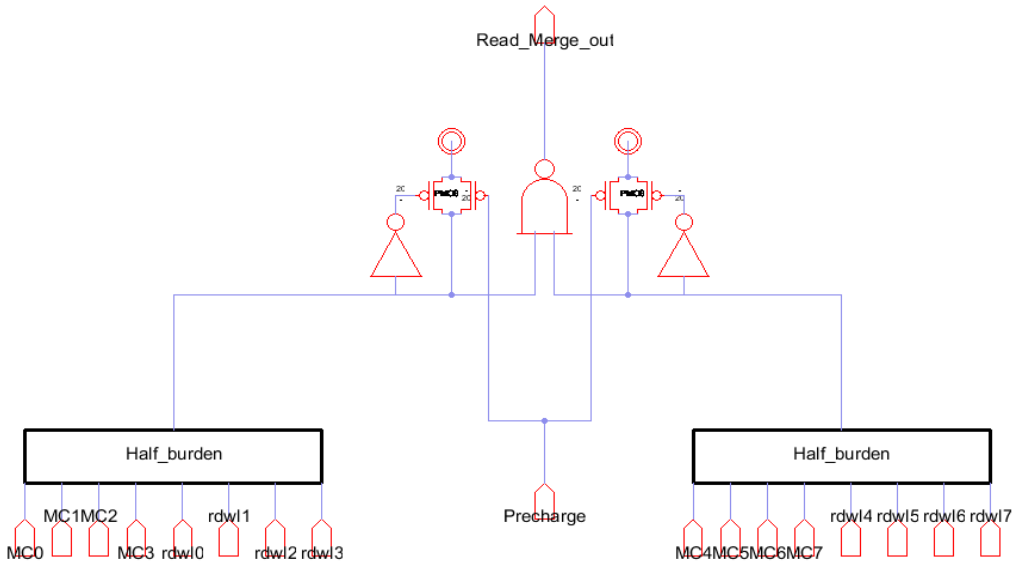

Fig 36 Schematic of conventional domino multiplexer

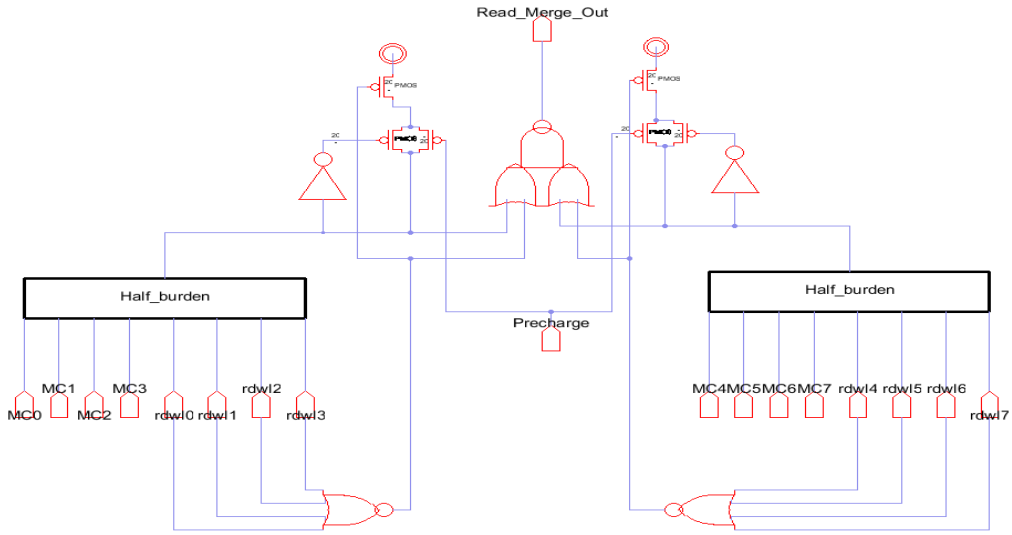

Fig 37 Schematic of single LBL float with complex gate isolation

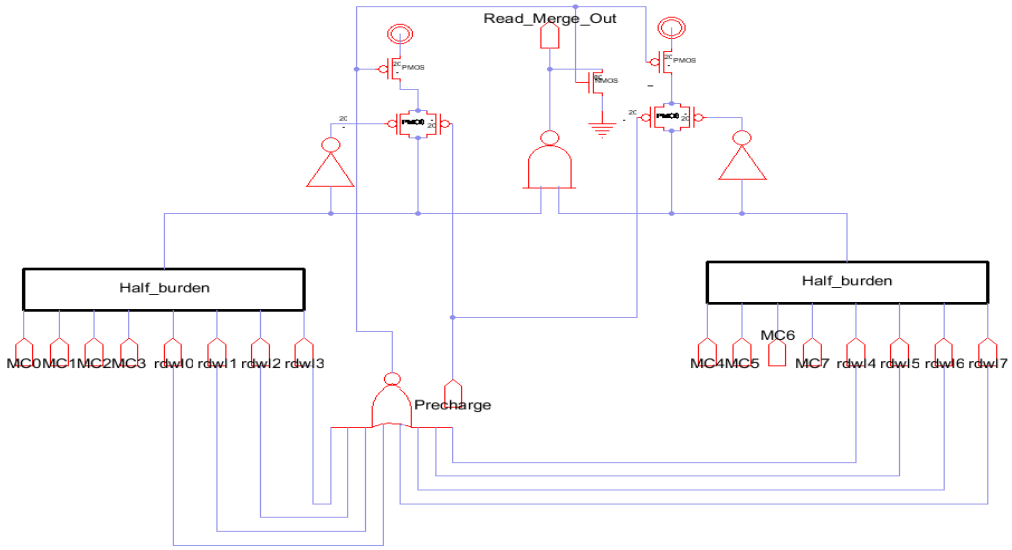

Fig 38 Schematic of double LBL and read-merge float with isolation MOS(with Nor-8)

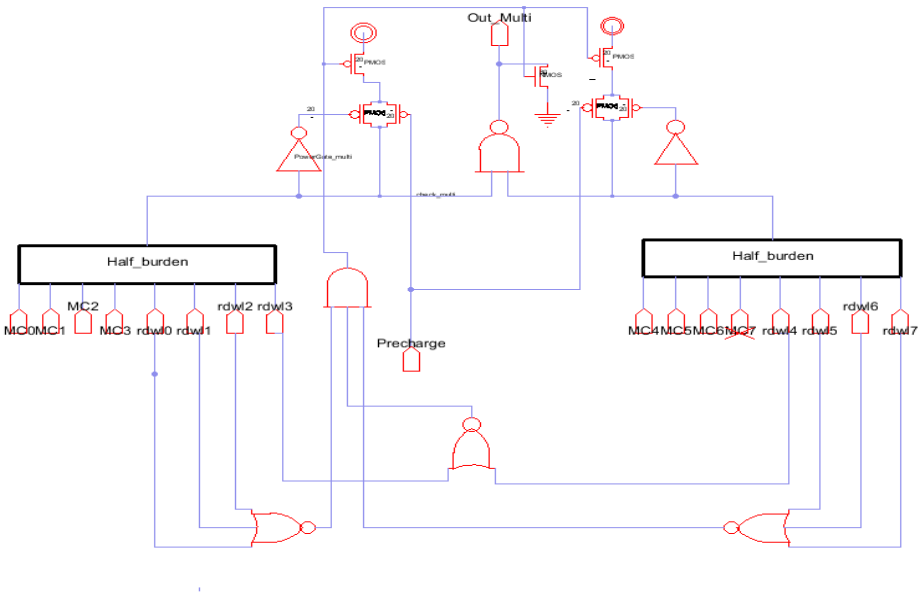

Fig 39 Schematic of double LBL and read-merge float with isolation MOS(with multi-gate)

In addition, the on-demand and block validity are combined together as a condition to power on/off the selective power-gated domino multiplexer. The read word lines (RDWL) from decoder will produce the control signal to control the power gate after pass through some gates. In single LBL float with complex gate isolation (design1), the local bit lines (LBL) can work independently. Therefore, only two NOR-4 gates are required to produce the control signal for each half burden. However, the LBL for double LBL and read-merge float with isolation MOS must turn on/off at the same time to prevent floating output. Thus, all the RDWL must gather together to produce a control signal for whole selective power-gated domino multiplexer. There are two way can be applied in order to produce a correct control signal. First, implement a NOR-8 gate to gather all the RDWL and second is implementing two NOR-3 gate and an AND-3 gate (multi-gate).

4.2 Analysis

4.2.1 Analysis on Time Delay

All the schematic design of domino multiplexer compared with each other in term of time delay. In the read operation, the rising time and falling time of each schematic design will be recorded in order to carry out the analysis among all schematics design.

Comparison among proposed design

First of all, the schematic of double LBL and read-merge float with isolation MOS (Desgin2) has two way to produce the correct control signal for power gate which is NOR-8 gate , and multi-gate (combination of two NOR-3 gate and an AND-3 gate. Therefore, there are total three power-gated schematic design to compare with each other in term of time delay which are single LBL float with complex gate isolation, NOR-8 double LBL and read-merge float with isolation MOS and multi-gate double LBL and read-merge float with isolation MOS.

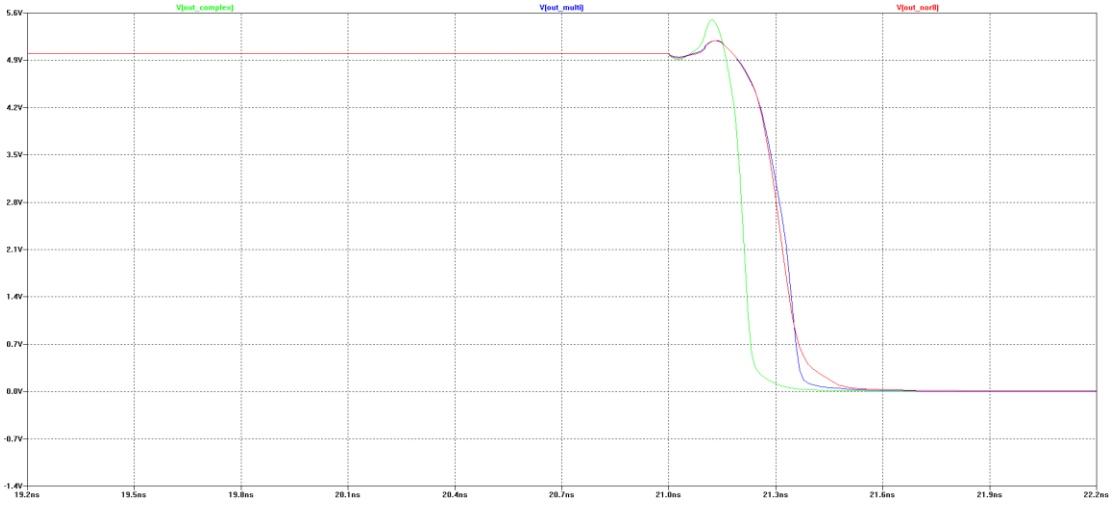

Fig 40 Falling time for the outputs of three power-gated schematic design

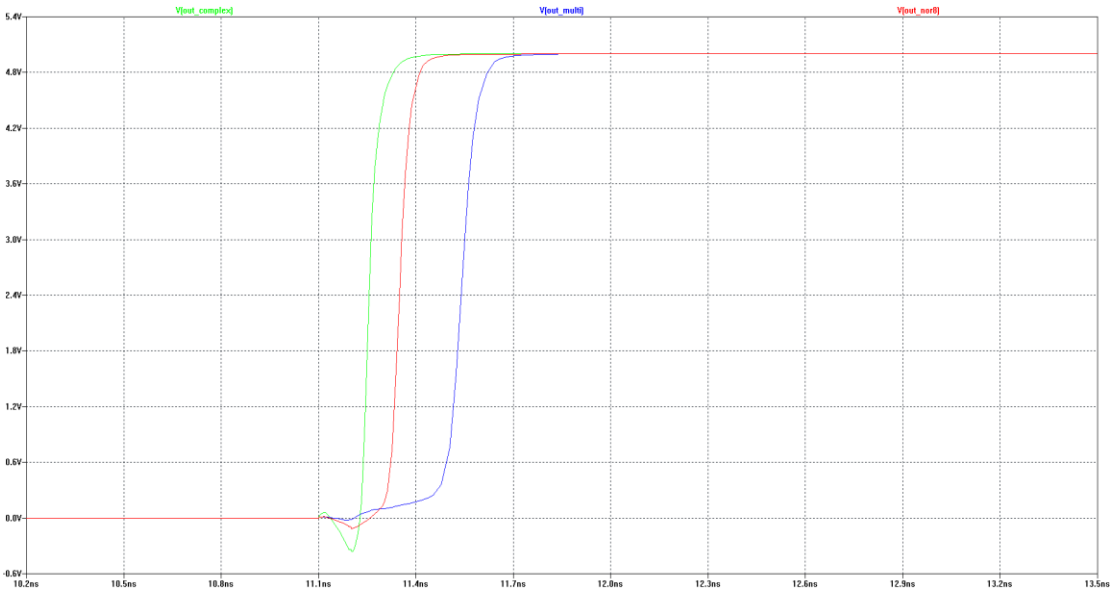

Fig 41 Rising time for the outputs of three power-gated schematic design

Fig 40 and fig 41 shows the timing diagram for the outputs of single LBL float with complex gate isolation, NOR-8 double LBL and read-merge float with isolation MOS and multi-gate double LBL and read-merge float with isolation MOS. Green color represent single LBL float with complex gate isolation (Design 1). Blue color represent multi-gate double LBL and read-merge float with isolation MOS (Design 2 with multi-gate) while red color represent NOR-8 double LBL and read-merge float with isolation MOS (Design 2 with NOR-8).

From the timing diagrams above, it clearly show that the single LBL float with complex gate isolation (Design 1) has the shortest time delay among all the design. For the double LBL and read-merge float with isolation MOS (Design2), the way using NOR-8 to gather all the RDWL is faster than using multi-gate.

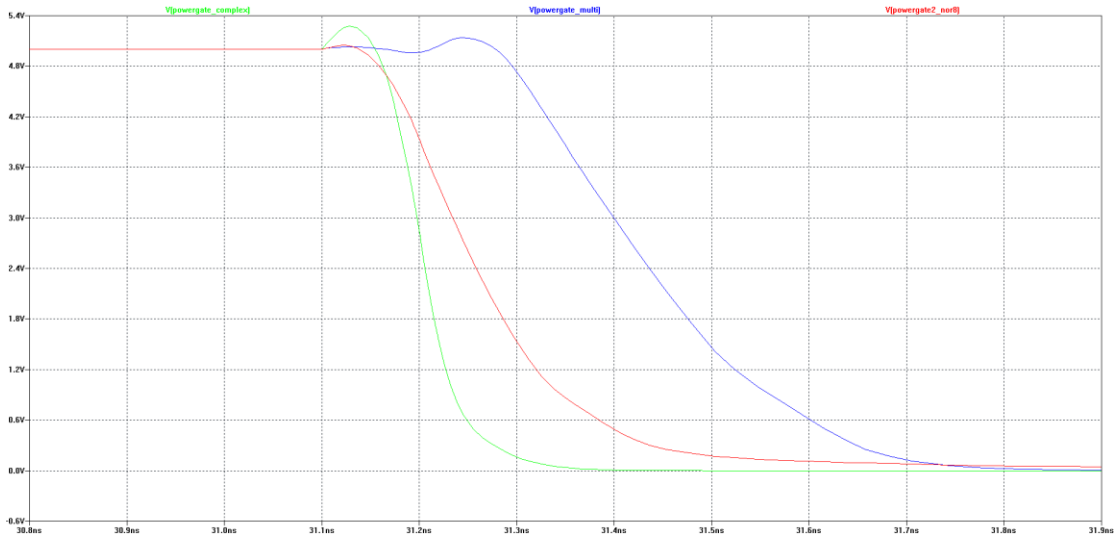

Fig 42 Falling time for the control signals of three power-gated schematic design

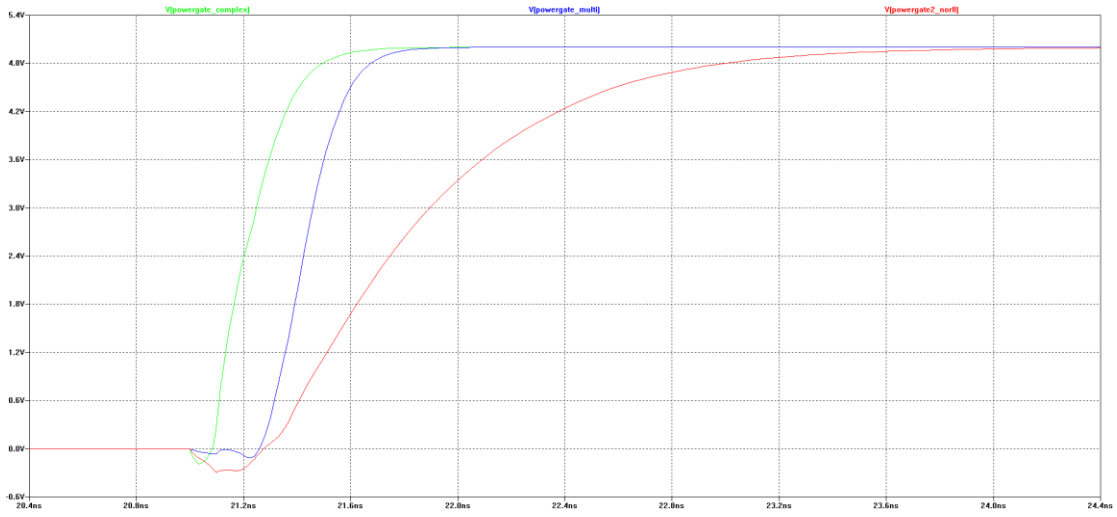

Fig 43 Rising time for the control signals of three power-gated schematic design

Initially, the expected result is NOR-8 will has longer time delay due to the fan-in problem and the difficulty to get the data '1' which used to power off the domino multiplexer. However, the simulation result is different with expected result. Although NOR-8 is much slower to product a '1' compare to multi-gate, but it is much faster to product a '0' compare to multi gate. This mean that NOR-8 double LBL and read-merge float with isolation MOS (Design 2 with NOR-8) is faster for power on, while multi-gate double LBL and read-merge float with isolation MOS (Design 2 with multi-gate) is faster for power off . After analyze the output of both double LBL and read-merge float with isolation MOS, the NOR-8 double LBL and read-merge float with isolation MOS (Design 2 with NOR-8) is better than multi-gate double LBL and read-merge float with isolation MOS (Design 2 with multi-gate) due to much shorter delay for power on but very minimum degradation on the speed for power off.

Comparison among conventional design and proposed designs

After comparison among all the power-gated schematics design, now discuss about the result about the comparison between the two proposed power-gated designs and the conventional design. Initially, the conventional design is expected to have the shortest time delay compare to other 2 proposed power-gated design. Nevertheless, the ~~simulation~~ result is different with expected result after carry out the simulation.

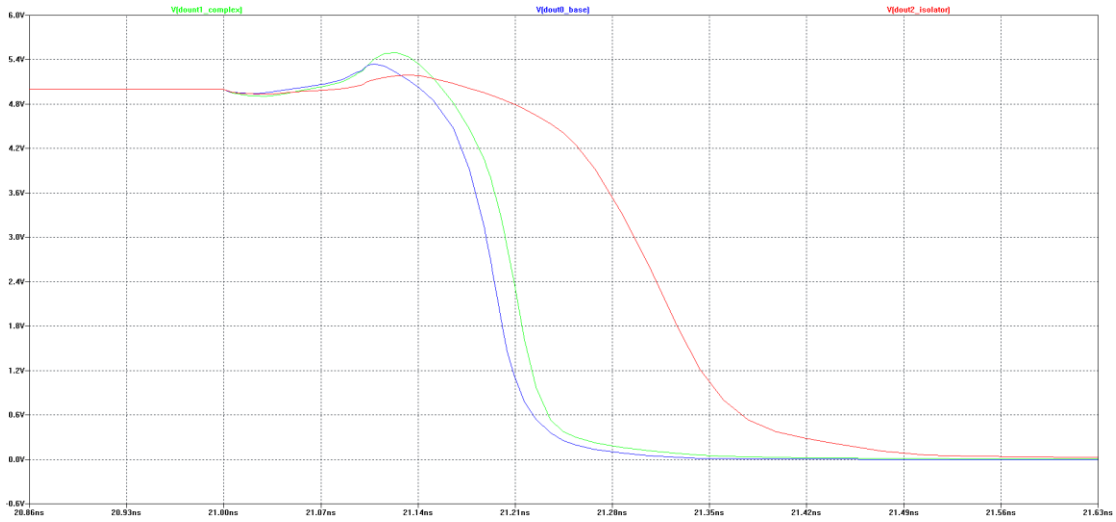

Fig 44 Falling time for the outputs of conventional design, and two power-gated design

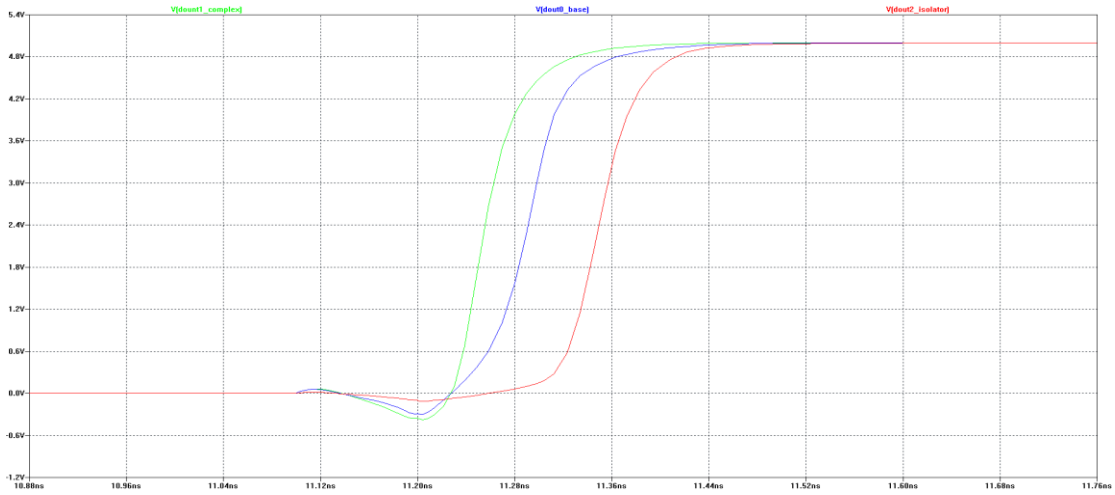

Fig 45 Rising time for the outputs of conventional design, and two power-gated design

In fig 44 and 45 show the timing diagram for the outputs of conventional design, and two proposed power-gated design. Green color represent single LBL float with complex gate isolation (Design1). Blue color represent conventional design while red color represent double LBL and read-merge float with isolation MOS (Design2). From the timing diagrams above, it clearly show that Design1 has fastest rising time among three domino multiplexer designs followed by conventional design and Design 2. On the other hand, conventional design has fastest falling time followed by Design1 and Design2.

In expected result, the reason for conventional design is expected to have shortest time delay is because there have no power-gated in conventional design and it can save the time to output a control signal for power gate. However, by refer to simulation result, Design 1 is faster than conventional design and Design 2 in term of rising time.

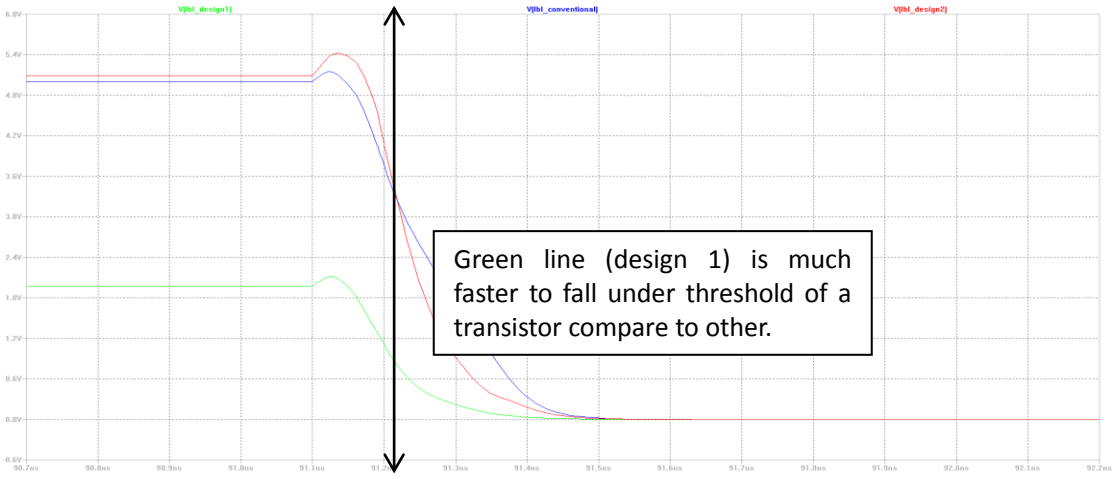

Fig 46 Falling time for LBL of conventional design, and two proposed power-gated design

Fig 47 Rising time for LBL of conventional design, and two proposed power-gated design

The factor that causes Design 1 faster than conventional design in term of rising time is the floating voltage level of local bitline (LBL). In Fig 46 and 47, green color represents the LBL of Design1. From the both fig, it clearly show that the Design1 has a lower voltage level in '1' compare to Design2 and conventional design. But the voltage level is able to overshoot the threshold voltage of a 300nm transistor.

The reason will cause different voltage level among 3 schematics design is the delay of power control signal. First of all, the control signal for power gate is come from the RDWL which output from read decoder. For the read decoder, it only enabled and produces the RDWL to domino multiplexer during evaluation phase. Therefore, all the RDWL will be '0' during precharge and this cause the control signal go to '1' and shut off the power gate. Since the LBL cannot directly connect to VDD source during precharge, floating state will be occur and the voltage level unable to reach VDD but

almost half VDD. For the Design 1, the power gate control able to produce a quickly signal with minimum delay during precharge. Thus, the floating LBL will exist. However, the power gate control of Design 2 has a signal with longer delay and this allow its LBL have sufficient time to raise closer to VDD. Therefore, the voltage level of Design 2 is different and higher compared to Design 1 and this is one of the limitations that cause the simulation result of this project is out of expectation.

In rising time of LBL, 3 of them can switch on nmos at the same time. Thus, the falling time of their outputs is depending on the delay of power gate control signal. In this case, conventional will have the faster falling time because it does not has power gate control signal. However, there is different story for falling time of LBL. For falling time of LBL, Design1 has a fastest speed to switch on pmos and the NOR-4 that used in Design 1 able to produce a '0' control signal easily. Therefore, Design 1 able to turn on the pmos in complex gate faster than the other two designs to turn on the pmos in their read-merge (NAND).

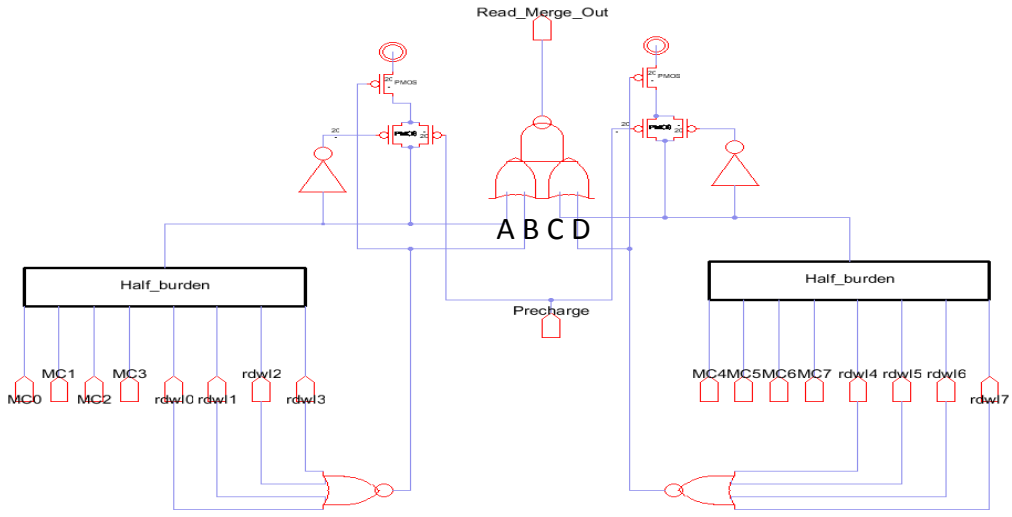

Fig 48 single LBL float with complex gate isolation (Design 1)

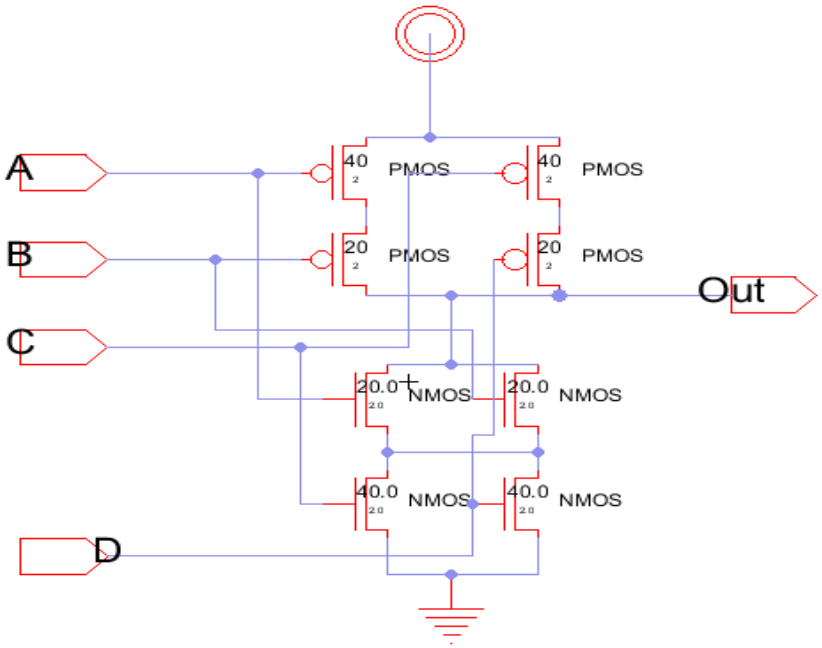

Fig 49 Complex Gate

From fig 48 and 49, they clearly show that the input of a complex gate. The inputs B/D are able to receive a '0' very fast due to the parallel nmos in NOR-4. The inputs A/C are receiving signal from LBL and they can switch on a pmos in a shorter delay due to the low-voltage level in LBL of Design 1. With these conditions, Design1 able to have the shortest delay in rising time of the outputs among three designs.

4.2.2 Analysis on Power

After analyze the functionality and the time delay of all the schematic design of domino multiplexer, the power consumption of all the schematic design also had analyzed. First of all, all the VDD source and VSS source in the each schematic are

connected to a main VDD source and main VSS source respectively in order to measure the power consumption of each design.

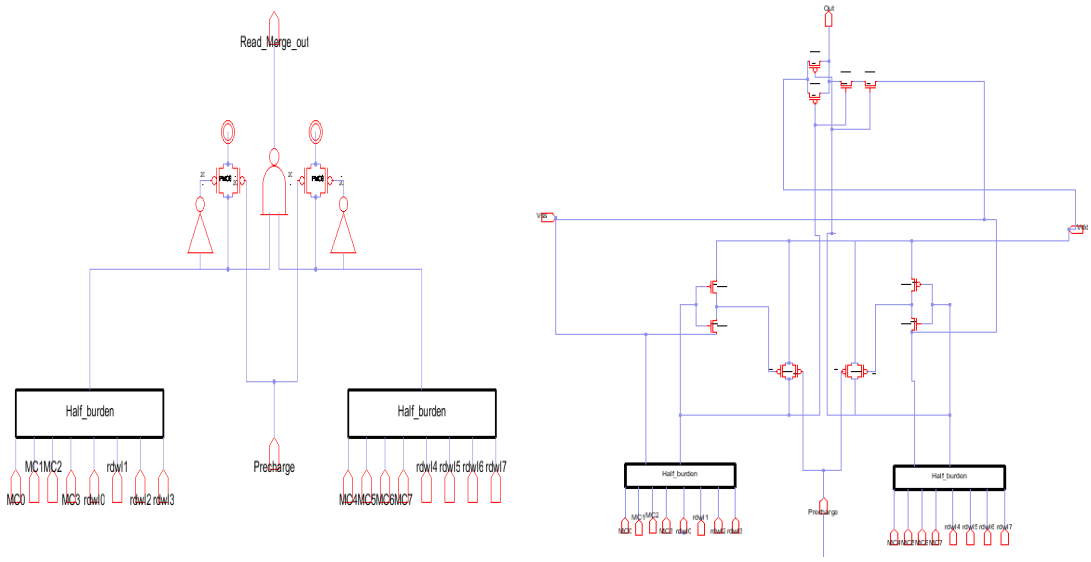

Fig 50 Schematic of Conventional Design in power analysis

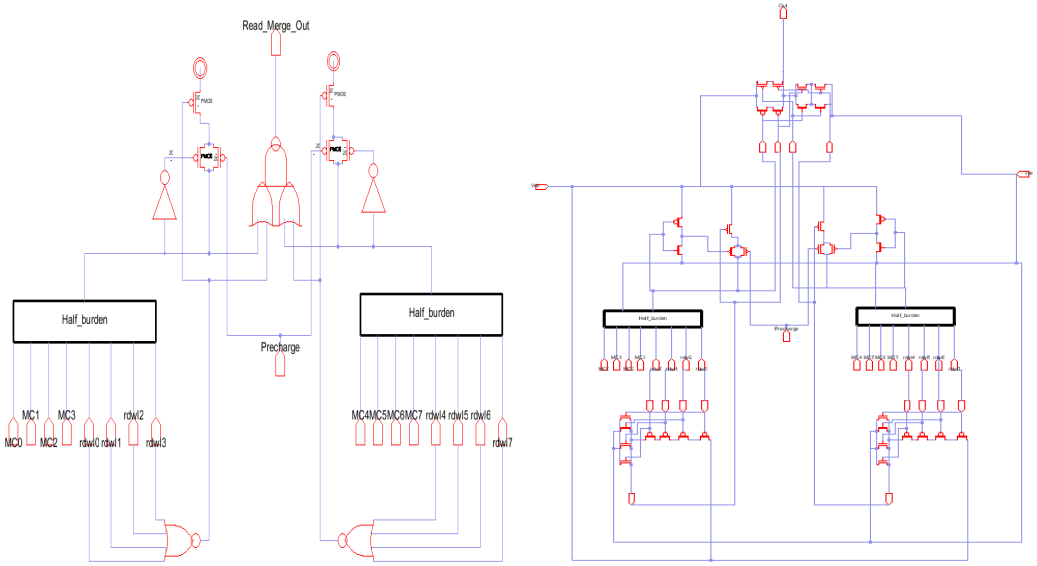

Fig 51 Schematic of Design 1 in power analysis

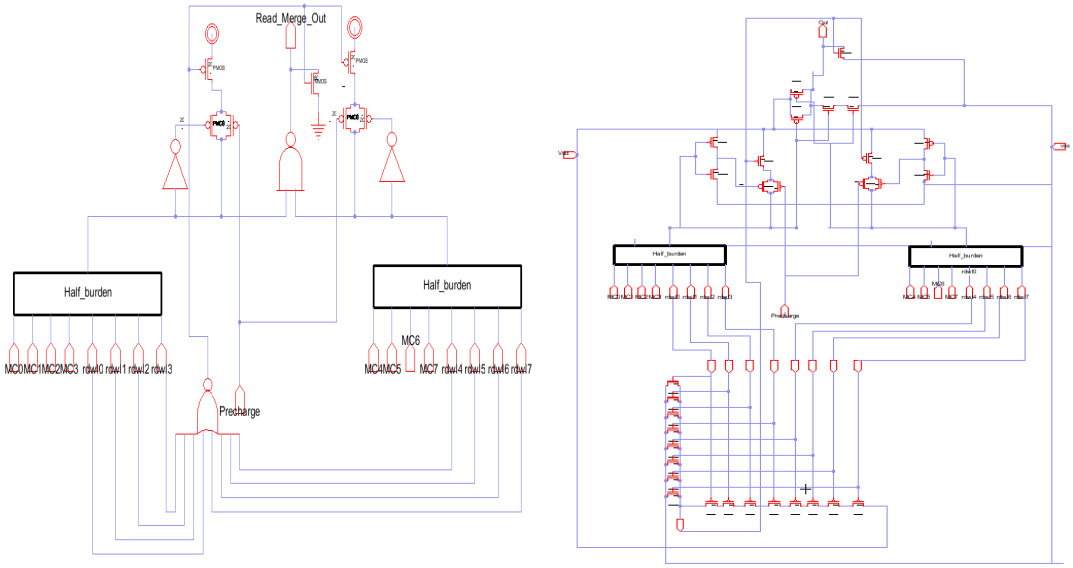

Fig 52 Schematic of Design 2 in power analysis

In expected result, Design1 has lower of power consumption compare to conventional design and Design2. Design1 is implementing power-gated low power technology and contains a complex gate to provide the flexibility in order to ensure the LBL can work independently. Design2 is implementing power-gated low power technology and contains an isolator to ensure no floating output. These two proposed design is expected to reduce the power consumption of conventional design because the proposed design can be power off when it is not being access or the data is invalid.

However, the simulation result is out of the expectation. From the simulation result, both proposed design not only unable to reduce the power consumption as what expected, but increase a lot of power consumption. Therefore, the proposed power-gated domino multiplexer is consider fail to reduce the power consumption and couldn't archieve the expected result.

Number of block	Type of DMUX	Ivdd(pA)				Ivss(pA)			
		Not being Access		Accessed		Not being Access		Accessed	
		Pre=0	Pre=1	Pre=0	Pre=1	Pre=0	Pre=1	Pre=0	Pre=1
1	Base	60.4832	60.4832	3547.3	45.2784	60.4832	60.4832	3541.94	45.2784
	Design 1	748.441x10^6	617.458x10^6	608.288x10^6	308.833x10^6	748.441x10^6	617.458x10^6	608.288x10^6	308.833x10^6
	Design 2	1.57264x10^9	1.24949x10^9	81.1002	56.5375	1.57264x10^9	1.24949x10^9	81.1002	56.5375
2	Base	120.967	120.967	3612.79	105.762	120.967	120.967	3612.79	105.762
	Design 1	1.49688x10^9	1.23491x10^9	1.35695x10^9	926.448x10^6	1.49688x10^9	1.23491x10^9	1.35695x10^9	926.448x10^6
	Design 2	3.14529x10^9	2.49898x10^9	1.57278x10^9	1.24996x10^9	3.14529x10^9	2.49898x10^9	1.57278x10^9	1.24996x10^9
4	Base	241.933	241.933	3728.76	226.728	241.933	241.933	3738.94	226.728
	Design 1	2.99376x10^9	2.46981x10^9	2.85392x10^9	2.16167x10^9	2.99376x10^9	2.46981x10^9	2.85392x10^9	2.16167x10^9
	Design 2	6.29058x10^9	4.99796x10^9	4.71833x10^9	3.74941x10^9	6.29058x10^9	4.99796x10^9	4.71833x10^9	3.74941x10^9
8	Base	483.866	483.866	3973.8	468.661	483.866	483.866	3973.8	468.661
	Design 1	5.98751x10^9	4.93961x10^9	5.84795x10^9	4.63212x10^9	5.98751x10^9	4.93961x10^9	5.84795x10^9	4.63212x10^9
	Design 2	12.5812x10^9	9.99593x10^9	11.0094x10^9	8.74849x10^9	12.5812x10^9	9.99593x10^9	11.0094x10^9	8.74849x10^9

Fig 53 Analysis on power consumption among three schematics design

In order to measure the power consumption, all the VDD source and VSS source in each schematic design are connected to a main VDD source and main VSS source respectively and the Ivdd and Ivss will be measure which is the leakage current in the schematic. Besides, the power consumption of all schematic design is measured under 4 different conditions. They are accessed precharge phase, accessed evaluation phase, non-accessed precharge phase, and non-accessed evaluation phase. In addition, this power analysis is carried out in 1, 2, 4, and 8 unit of schematic design which represent 8 entries, 16 entries, 32 entries, and 64 entries. From fig 52, the analysis result shows that the highest power consumption is from Design2 followed by Design1 and conventional design. From the analysis, it shows that Design1 have about 10^6 times power consumption and Design2 have about 10^9 times power consumption compared to conventional design.

Potential Problems

There few potential problems that cause the simulation result is different with expected result. First, C5 model 330nm technology which used as library in Electric VLSI is not the most ideal technology for this project to evaluate and verify the power consumption. The reason is because the leakage current for 300nm C5 models transistor does not affect much on overall power consumption.

Second problem is the number of transistor in proposed power-gated schematic design. The number of transistor in proposed power-gated schematic is more than conventional design. Each transistor will contribute some leakage current and end up the leakage current from each transistor become a significant amount of power consumption.

Third problem is about lack of choices for transistor type. As mention in chapter2, there are several type of transistor in the industry nowadays such as high spend transistor, nominal transistor and low-leakage transistor. Different type of transistor will be applied in different parts of schematic in order to reduce the power consumption and time delay. Low leakage transistor which refer to the transistor with high threshold volatage, low speed and low power consumption. Actually the most ideal way is the sleep transistors in the power gate (transistors that connected to source either VDD or VSS) should be using the low leakage transistor. However, the sleep transistors in this project are using the normal transistor which has higher leakage current compare to low leakage transistor. The reason why this project is using normal transistor instead of low leakage transistor is the C5 300nm model does not provide different type of transistor, and only normal transistor is provided in this library.

Lastly, limitation of tool, Electric VLSI is also one of the potential problems too. This tool is not the ideal design tool to evaluate power consumption. Therefore, it can only show limited information regarding power consumption.

The four problems above are the potential problems that may affect the result of this project. Therefore, more analysis should be carried out in future work in order to improve the accuracy of the result and find out the solutions to solve the existing problems. In the conclusion, the proposed power-gated selective domino multiplexer is unsuccessful to reduce the power consumption of the existing conventional design domino multiplexer.

Chapter 5 Conclusion

Nowadays, reduction of the power consumption is prior consideration in CPU design. In order to reduce the leakage power of the domino multiplexer used in register file, Intel had come out a technique called on-demand-precharge to solve the problem. Nevertheless, the on-demand precharge is not perfectly solving the problem. This project is to to study and verify the power efficiency of existing conventional domino multiplexer which used in register file by propose two different power gated scheme for domino multiplexer. The selective power gated domino multiplexer is able to power off when it is not being access and this feature is expected to reduce the power consumption.

Unfortunately, after the verification and analyse, the proposed solutions are consider fail to archive the reduction on power consumption of existing conventional domino multiplexer which used in register file nowadays. There are few problems that affect the result and cause the simulation result is out of initially expectation. For example, technologies used in this project are not the most ideal technology, number of transistors in the schematics design is increasing, lack of choices for transistor type in design library that used in this project, limitations of designing tool and etc. Therefore, solutions to overcome these problems should be figure out in future work in order to increase the accuracy of result.

However, some modifications and improvements can be implemented on this project in future work in order to improve the accuracy and performance of the design. Firstly, 90nm or even smaller transistor models should be implemented in the project instead of 300nm. Secondly, use the proper electric design automation tool which can evaluate and calculate the power consumption accurately. In addition the electric

design automation tool should contain multiple type of transistor in order to allow the user can apply the ideal transistor type for the design. For example, the low-leakage transistor can be applied as sleep transistor (transistors that connected to source either VDD or VSS) in power gate to reduce the leakage power while normal can be applied as general logic circuit in order to reduce the time delay. Last but not least, this project may include other low-power techniques in order to get the best techniques to get the best trade-off between power consumption and time delay.

In conclusion, the journey to duel with power efficiency is very long. There are still a lot of modifications, improvements, and developments need to carry out on this project in order to fully achieve the expected results of this project which are successfully reduce the power consumption of existing conventional domino multiplexer that used in register file and able to get the best trade-off between power consumption and time-delay.

Bibliography

Bruce Jacob, Spencer W. Ng, David T. Wang (2008). Memory Systems: Cache, DRAM, Disk. Morgan Kaufmann.

Keating, M. Flynn, D. Aitken, R. Gibbons, A. Shi, K. (2007). Low Power Methodology Manual: For System-on-Chip Design. Springer.

Meher , P. & Mahapatra, K.K. 2011. Ultra Low-Power and Noise Tolerant CMOS Dynamic Circuit Technique. IEEE Conference Publication.

Shi-Hao Chen & Jiing-Yuan Lin. 2008. Experiences of Low Power Design Implementation and Verification. IEEE Conference Publication.

Shirai, T. & Usami, K. 2008, Hybrid Design of Dual Vth and Power Gating to Reduce Leakage Power under Vth Variation. IEEE Conference Publication.

Ortega, C., Tse, J., & Manohar, R. 2010. Static Power Reduction Technique for Asynchronous Circuits. IEEE Conference Publication.

Hailin Jiang, Marek-Sadowsha, M., & Nssif, S.R. 2005. Benefits and Costs of Power Gating technique. IEEE Conference Publication.

Venkatachalam, V., & Franz, M.Power Reduction Techniques For Microprocessor Systems. Univeersity of California. Irvine.

Jae Wong Chun, & Chen, C.Y.R. 2010. A Novel Leakage Power Reduction Technique for CMOS Circuit Design. IEEE Conference Publication.

Burgess, N. 2003. Logical Effort Analysis of Multi-port Register File Architectures. IEEE Conference Publication.

Bernstein, K., & Furman, Anatol. 1984. Multiport Register File Architecture. IEEE Conference Publication.

Lih, Y., Tzartzanis, N., & Walker, W.W. 2007. 'A Leakage Current Replica Keeper for Dynamic Circuits'. IEEE Journals & Magazines. Vol. 42, no. 1, pp. 48-55.

Li Ding, & Mazumber, P. 2004. 'On Circuit Techniques to Improve Noise Immunity of CMOS Dynamic Logic', IEEE Journals & Magazines. vol. 12, no. 9, pp. 910-925

Agrawal, R. & Ladhake, S.A. 2012. 'Systematic Design of High-Speed and Low Power Domino Logic', International Journal of Advanced Research in Computer Science and Software Engineering. vol. 2, no. 3.

Kachhara, D., Prasad, R., Agarwal, R. & Maheshwari, M. 2002.' Power Saving in CMOS Using a Half-Swing Clock Scheme', International Journal of Engineering Research and Apllication(IJERA). vol. 2, no. 2,pp. 815-819

Swaroop, V.G.S, Krishana, B.M., Bhaskar M.V., & Kanth, B.R. 2012. 'Design Of Low Power 8 Bit SRAM Architecture Using Leakage Feed Back With Stack & Sleep Stack with Keeper', International Journal of Engineering Research and Apllication(IJERA). Vol. 2, no.2, pp. 192-201.

Morizio, J.(No State). Dynamic Combinational Circuit. [ONLINE] Available at: http://people.ee.duke.edu/~jmorizio/ece261/classlectures/ dynamicCMOS.pdf. [Accessed 16 July 2013]

Register File Characterization. Available from: http://www.ecse.rpi.edu/frisc/ theses/CampbellThesis/chapter3.html. [Accessed 16 July 2013]

Desktop Processors. Available from http://ark.intel.com/. [Accessed 16 July 2013]

Dynamic logic (digital electronics). Available from: http://en.wikipedia.org/wiki/Dynamic_logic_(digital_electronics) . [Accessed 16 July 2013]

Digital Integrated Circuit Design. Available from: http://www.ami.ac.uk/courses/ami4407_dicdes/u03/. [Accessed 16 July 2013]