STUDY OF THE HIGH TEMPERATURE SOLID STATE HYDROGEN SENSOR BASED ON WIDE BANDGAP SEMICONDUCTOR MATERIAL

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By

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ABSTRACT

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CHONG SIR CONG

The growing need for reliable, efficient, high temperature hydrogen (H_2) and hydrocarbon monitoring has fueled research into novel structures for gas sensing. The aim of this project is to develop a robust solid state hydrogen gas sensor that can withstand and operated in high temperature environment, especially for automotive hydrogen safety applications in fuel cell and hydrogen-powered vehicles. Here, Silicon Carbide (SiC)-based H_2 sensors have attracted much attention due to application in harsh environments. SiC is a wide bandgap semiconductor that can withstand harsh conditions, such as high temperature, strong radiation and chemical reactive environments. With its wide bandgap (~3.2 eV, 4H-SiC), high strength and low intrinsic carrier concentrations, the working temperature of 4H-SiC can reach 1200^{o}C. A solid state SiC-based H_2 sensor is suitable for the automotive industries, since the component is small size and compact, can withstand high temperatures without the need for extra cooling

system, have low power consumption and the ability to be easily interfaced with standard electrical connector bus to the on-board electronic control systems. Currently, only Silicon (Si)-based H_2 sensors are available in the market nowadays wherein the operating temperature is limited to 180^{o}C or lower. Such low temperatures are restrictive to the locations where the sensor can be installed. Therefore, SiC-based H_2 sensors can be a serious contender for the automobile and as well as other industries applications in H_2 gas sensing, which is the motivation for this project. With the distinctive and superiority of these kind of SiC-based H_2 sensors, it promote a brilliant landscape of future green technology in concluded. In this dissertation, the characteristic of SiC-based MOS capacitor H_2 sensor is conferred in detail. Three material systems (Pd/SiO_2, Pt/SiO_2, Mo/SiO_2) have been tested in our experiment. MOS capacitor H_2 sensor devices with low interface state density (10^9 $cm^{-2}eV^{-1}$) have been fabricated and their performances under high temperature environment have been measured. The results are very promising. More than 0.3V flat band voltage shift (show in C-V curve) has been observed for the devices produced using Pt/SiO_2 and Pd/SiO_2 systems when they are exposed to low hydrogen concentration (~0.2%) and high temperature (~480^{o}C) environment. However, the Mo/SiO_2 devices show no response. It is believed that this is due to the low solubility of H_2 gas in Mo.

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APPROVAL SHEET

This thesis entitled "**STUDY OF THE HIGH TEMPERATURE SOLID STATE HYDROGEN SENSOR BASED ON WIDE BANDGAP SEMICONDUCTOR MATERIAL**" was prepared by CHONG SIR CONG and submitted as partial fulfillment of the requirement for the degree of Master of Engineering Science at Universiti Tunku Abdul Rahman.

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SUBMISSION OF FINAL YEAR PROJECT /DISSERTATION/THESIS

It is hereby certified that **CHONG SIR CONG** (ID No: **09 UEM 05597**) has completed this dissertation entitled "**STUDY OF THE HIGH TEMPERATURE SOLID STATE HYDROGEN SENSOR BASED ON WIDE BANDGAP SEMICONDUCTOR MATERIAL**" under the supervision of Dr. Lew Kim Luong (Supervisor) from the Department of Electrical and Electronic Engineering, Faculty of Engineering and Science (FES), and Dr. Yong Thian Khok (Co-Supervisor) from the Department of Electrical and Electronic Engineering, Faculty of Engineering and Science (FES).

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I hereby declare that the thesis is based on my original work except for citations and quotations which have been duly acknowledged. I also declare that it has not been previously and concurrently submitted for any other degree or award at UTAR or other institutions.

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CHAPTER 1

INTRODUCTION

1.1 Background and Motivation

Nowadays, with the increasingly serious environmental pollution and raised of the awareness in environmental conservation in many countries, many scientists and engineers are making efforts in producing green products which are environmentally friendly. Looking for a clean, renewable energy source becomes an urgent need to overcome the conundrum. The shortage and polluted impacts of fossil fuels has reinvigorated interest in the advancement of its alternatives. Hydrogen (H_2), the most abundant gases element in natural, is one of the most promising candidates. Much attention has been paid towards H_2 as one of the economical, non-conventional and clean energy source/carrier for the many industrial applications. For example, H_2 can become efficiency energy carriers for use in fuel cells and combustion engines.

It's being much doubts about H_2 gas safety have prevented it from fulfilling its potential as a fuel source. H_2 is a highly active and flammable chemical element in concentrations ranging from 4% to 90% by volume which depend on the temperature of environment (see Fig. 1.1). Its lowest explosion limit being 4.1% makes the need for placing H_2 sensors near high concentration storage facilities essential. For optimal operations and safety issues, the use of H_2 in advanced power

production will required a real-time monitoring of the H_2 concentrations via an online gas sensing system that is reliable and can survive the harsh operating conditions (such as the environment within the combustion engines). H_2 gas sensors would form an integral part of such systems incorporating H_2 as a fuel. These electronic devices are important in various applications for safety reasons. It is of great attention mainly for detection of H_2 leakages. The desired gas sensors must function at temperatures up to 400°C with long operating lifetime in the presence of gases containing significant amounts of H_2. High sensitivity, selectivity, reliability and fast response time for real-time monitoring, long-term stability, low H_2 concentrations workable, and cost effectiveness are additional essential factors for the sensing system.

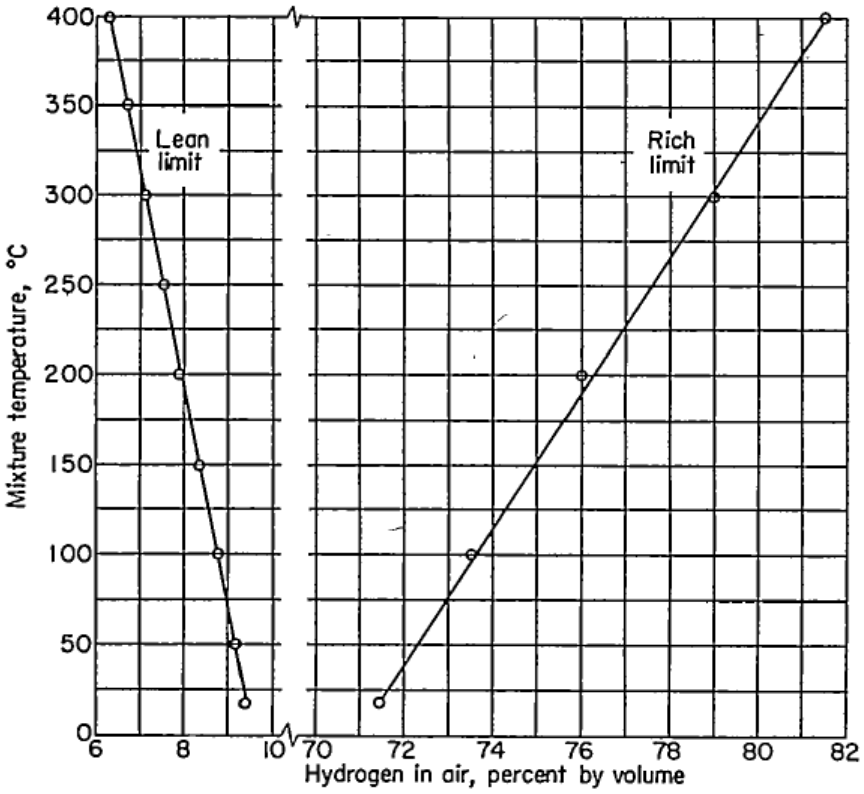


Figure 1.1: Effect of temperature on flammability limits of H_2 in air for downward propagation.

Harsh environment, in general, is termed as extreme environment, hostile environment, rough environment or "unfriendly" environment. These environments are always referred to the situation involving high temperature, high power, intense vibrations, erosive flows, and as well as high aggressive media exposure. In addition, harsh environment is related to the condition which is likely to cause significant corrosion-related degradation. Typically, harsh environment applications are related to those heavy or large-scale industries especially in automotive. In this industry, not only the operational temperatures are high but also the inability to provide cooling system. Field effect H_2 gas sensors based on Si substrates have operating temperatures limited to below 200 $^{\circ}$C (Ghosh et al. 2001). Thus, this would cause conventional pure Si-based H_2 sensing electronic systems to fail. Consequently, there is a need for semiconductors with good thermal stability and wide bandgap for stable electronic properties at elevated temperatures. Soo et al. (2001) and Pitts et al. (2001) investigated that Silicon Carbide (SiC) is able to deal with this harsh environment application when we used it as a substrate to develop electronic devices. These wide bandgap semiconductors offer great potential to fabricate active high-temperature electronics and micro-systems for applications in very-high-temperature regimes (more than 300°C). SiC has additional attractive features compared with other wide bandgap semiconductors. SiC substrates are commercially available, it has known device processing techniques that very similar with Si and it has an excellent ability to grow a good quality of thermal oxides. As a result, SiC is now in the forefront of high voltage and high power electronic devices research. SiC has a lot of different poly-types (polymorphism). For each of them, the bandgap ranges from 2.2 eV for the cubic

configuration to 3.3 eV for the hexagonal configuration. This range of wide bandgap allows high temperature operation up to 1000°C. This property of SiC allows H_2 sensors based on this material to be integrated with high-temperature electronic devices on the same chip. Furthermore, these wide bandgap semiconductors may offer additional advantages in terms of high power and high accuracy applications (Loloee et al. 2008). Therefore, development of SiC-based H_2 sensor is of strong concern.

Most of the SiC-based H_2 sensors are grouped into field effect devices, which properties are determined largely by the effect of an electric field on a region within the devices. The unique working principle of SiC field effect devices makes it as a gas sensor with high sensitivity and good selectivity towards H_2 gas sensing. Furthermore, these SiC-based devices are able to perform rapid response over a broad range of temperature, where the response is in the order of milli-seconds (ms). Gas sensors of this structure have a great stability and reliability for harsh environment applications (Lundström et al. 1976). Among these field effect devices, metal-oxide-semiconductor (MOS) SiC-based H_2 sensor is preferred. MOS capacitive H_2 sensors are very simple to fabricate. They consist of junctions of metal, insulating and semiconducting materials. Direct measurements of capacitance is made as a function of bias voltage, and from them the changes in their electrical field distribution due to the H_2 gas could be monitored (Soo et al. 2001).

1.2 Research Objectives

The main objective of this project is to fabricate a MOS SiC-based H_2 sensor for the automotive industries which could operate under high temperature environment (>300 ^oC). These sensors must respond to the presence of H_2 well before the explosive limit (> 4% H_2 in air) is reached. This requirement dictates that a premium is placed on detecting small quantities of H_2 (0.5% or smaller) in the ambient atmosphere. Thus, our devices with varieties metal gate material (Palladium (Pd), Platinum (Pt) and Molybdenum (Mo)) will be tested under 480 ^oC and they should respond to low concentrations of hydrogen gas (0.2% H_2 in air). The minimum flat band voltage shift should be 0.1V. By using the workstation that provide by Keithley (software include), we are able to study the characteristics of those samples by analyzed the Capacitance vs Voltage C-V curve that generates from the Keithley semiconductor characterization system.

1.3 Thesis Organization

The thesis comprises of six chapters. Chapter 1 gives the background study and detailed development of solid state hydrogen sensors over the years. The motivation and the objectives behind this work are also discussed in this chapter. The literature review on hydrogen sensors is presented in Chapter 2. The basic operation principle of MOS capacitor is introduced in Chapter 3. The hydrogen sensing mechanism is also discussed in this chapter. Chapter 4 gives the fabrication

process technology that is employed for the fabrication of the solid state hydrogen sensors. The data collection procedures, analysis and the measurement instruments used in the study are also discussed in this chapter. In Chapter 5, the author discusses the experimental results obtained under high temperature environment. Chapter 6 summarizes the research works presented in this thesis. Recommendations for further research is also presented in Chapter 6

CHAPTER 2

LITERATURE REVIEW

Metal oxide semiconductor (MOS) devices employing a catalytic metal layer have emerged as one of the leading H_2 sensing platforms due to their high sensitivity and inherent capability for signal amplification. The limited operating temperature of such devices make use of silicon (Si) as the semiconductor layer has led research efforts to focus on replacing them with devices based on other semiconductor materials. Wide bandgap material, Silicon Carbide (SiC), has emerged as one of the leading candidate.

According to Trinchi et. al (2008), SiC consists of light atoms held together by strong forces. This high strength of Si–C bond produces many extreme properties such as chemical inertness and low diffusion coefficients. SiC is not easily eroded by most acids and can only be etched by alkaline hydroxide basics (i.e. KOH) at molten temperatures (> 600°C). SiC has well-known outstanding mechanical properties, in especially hardness and wears resistance. In terms of hardness, SiC has a Mohs hardness of 9. In terms of wear resistance, SiC has a value of 9.15. Moreover, SiC has a high thermal conductivity (better than Copper, Cu), and for some poly-types (notably 4H and 6H), a high critical electric field (in excess of 2 MV cm^{-1}), which can withstand an electric field one order of magnitude higher than Si. Since SiC has a higher breakdown voltage, its on-resistance is drastically reduced when compared with Si devices.

Compared with other wide-bandgap material, there is the other desired property of SiC as a substrate due to its ability to grow as a good quality of thermal oxide. The surface of SiC can be passivated by the formation of thermal SiO_2 but the oxidation rate is very slow when compared with Si. The good electronic and mechanical properties of SiC coupled with high temperature stability of the material are the underlying rational for investments in SiC technology and they offer new possibilities for more challenging applications than those impossible with Si devices, especially in high temperature environment applications such as the future automobile that uses hydrogen as its on-board fuel for motive power. There are various types of hydrogen fuel-cells that could apply to the car engine. Table 2.1 shows the list of different types of fuel-cells and their properties (Kumar and Majhi). It is found that fuel-cells for medium and large power application normally have very high operating temperature. Sensors that bulk with SiC are quite suit for it because of it advance characteristics that stated on above (Hübert et al, 2011).

Table 2.1: Types of fuel-cells and their applications (Kumar and Majhi).

Fuel Cell Type	**Operating temp.**	**Applications**
Alkaline (AFC)	50-200°C	Used in space vehicle, eg. Apollo, Shuttle
Proton Exchange Membrane (PEMFC)	30 -100°C	Vehicles and mobile applications and for lower power, CHP systems
Direct methanol (DMFC)	20-90°C	Suitable for portable electronic systems of low power
Phosphoric acid (PAFC)	220°C	Large numbers of 200KW CHP in use
Molten carbonate	650°C	Suitable for medium to large scale CHP systems.
Solid Oxide (SOFC)	500-1000°C	Suitable for all sizes of CHP systems

Polytypism (one-dimensional polymorphism) is one of the most unique features of SiC. There are approximately 250 SiC poly-types that have been discovered. The most common poly-types that are of greatest interest are 6H-SiC, 4H-SiC and the cubic form, 3C-SiC. The application of 4H- and 6H-SiC is usually restricted to electronic devices. Presently, 4H- and 6H-SiC electronic devices are the most promising due to the availability and quality of reproducible single-crystal wafers in these poly-types. According to Pitts et. al. (2001), 4H-SiCs' substantially higher carrier mobility compared to 6H-SiC should make it the poly-type of choice for most SiC electronic devices, provided that all other device processing, performance, and cost-related issues play out as being roughly equal between the two poly-types. This is due to the overall superior material properties. Its wide bandgap dramatically reduces the number of electron–hole pairs formed from thermal activation across the bandgap, which allows high temperature operation of SiC electronic devices. Thus, the H_2 sensors studied in this project are 4H-SiC-based devices.

The first field effect based hydrogen gas sensor is proposed by Lundstrom et al. (1976). The sensor belongs to the MOS family of devices. These device structure consist of a catalytic metal (generally group VIII transition metal) deposited on an oxide layer. The metal and oxide layers are in turn deposited onto the semiconductor substrate. The device reported by Lundstrom et al. more than 30 years ago was Pd-SiO_2-Si device. Nevertheless, the major of work on MOS based hydrogen sensors still concerned Pd/SiO_2 system although other material system such as Pd/Al_2O_3 system (Okuyama et al. 1997), Ni/SiO_2 system (Lu and Chen, 2010) and Rh/SiO_2 system (Ali M. 2007) were also investigated. Hence, the Pd-

SiO_2-SiC devices will be the main interest in this project. However, it is found that Pd will be embrittled easily by H_2 and deteriorate the device durability (Olsen, 2004). To overcome such issue, Pt has been proposed by other researchers. The Pt/SiO_2 material system with a 0.9V voltage shift under 1% H_2 gas condition has been reported by Ghosh et al. 2006. Thus, the Pt-SiO_2-SiC devices will also be fabricated and tested in our laboratory under 0.2% H_2 gas condition. Pt is known to have sticking issue on oxide layer and may peel off from MOS structure. A special sticking layer is needed for the Pt/SiO_2 material system and this could increase the cost of production and affect the sensing performance as well (Yoshimori, 1998). Although Pd/SiO_2 and Pt/SiO_2 material systems have showed acceptable results, both of them have some vulnerable issues which may affected their sensitivity, durability and reliability. To overcome these disadvantages, we would like to try new material system such as Mo/SiO_2. As a typical transition metal like Pd and Pt, Mo (in group VI) can also serve as metal catalyst. In addition, from our past fabrication experience, the adhesion between Mo and SiO_2 is much better compare with that of Pt. Thus, the Mo/SiO_2 material system which has never been tried by other researcher will also be attempted.

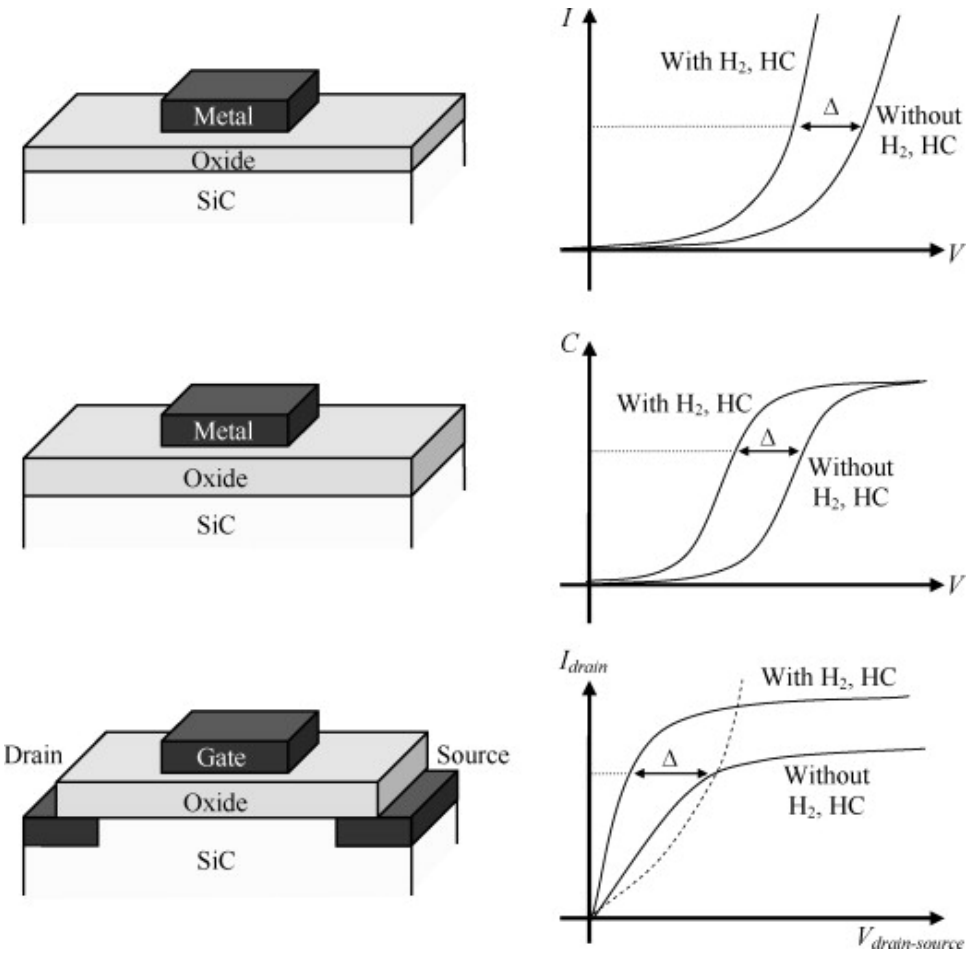


Figure. 2.1: Configurations of SiC based field effect hydrogen sensors. Their typical responses is also shown: *Top*: Schottky diode, *middle*: capacitor, *bottom*: field effect transistor. (Trinchi et al. 2008)

The field effect based hydrogen gas sensors have three different configurations as shown in Fig. 2.1. In each configuration, exposure to H_2 could alter the electric field distribution within the devices, causing a change in the current, capacitance or conductance. The first structure shown in Fig 2.1 is a Schottky diode. It is a two terminal device where the terminals are placed on the metal and semiconductor. In general, a several atomic layers thick oxide layer is grown before metal are deposited on the semiconductor. Shift in the diode current-voltage characteristics is monitored in the presence of H_2 gas. The second structure shown in Fig 2.1 is a MOS capacitor. The device structure of MOS capacitor is

similar to that of the Schottky diode where the terminals are also placed on the metal and semiconductor. However, the oxide layer thickness is much larger than for the diode's. This oxide layer is formed to prevent current conduction. Thus, charge can be accumulated on either of its sides. Shift in the device capacitance-voltage characteristics is monitored in the presence of H_2 gas. The third structure shown in Fig.2.1 is a MOS field effect transistor (MOSFET). It is a three terminal device. The current flowing through the two metal terminals (drain and source) is modulated by the electric field distribution in the oxide layer. Shift in the transistor conductance-voltage characteristics is monitored in the presence of H_2.

Among the three field effect based hydrogen gas sensors configurations, MOSFET H_2 sensor draws much attention due to the superior characteristics owned. However, in laboratory based research works, this structure requires many sophisticated equipment and technologies. Thus, MOS capacitor H_2 sensor is preferred in our research works because it is much more simple and sleazy in comparison. We believe that the results obtained may be similar to the corresponding MOSFET structure H_2 sensor. Moreover, the MOS capacitor is very sensitive to low gas concentrations and it is a simple, compact structure that can be economically mass-produced via microelectronic fabrication techniques. The development of the MOS capacitor was also pushed by researchers as a powerful tool to investigate semiconductor surface and oxide properties, as surface passivation for junction diodes and bipolar transistors, as an effective diffusion mask, and for electrical isolation (Terman 1962; Snow, Grove and Deal 1965; Nicollian and Brews 1982; Goetzberger and Sze. 1969). In conclusion, MOS capacitor has almost all the advantage that lies between the Schottky Diode and MOSFET configuration of H_2 sensor, which as good as in producing a hydrogen

leakage alarm system.

Hübert et al. (2011) shows that a typical MOS structure capacitive type H_2 sensor should be able to detect H_2 gas on the range of up to 5% of concentration in air. According to Ghosh, Tobias and Golding (2003), SiC based H_2 sensors that are able to operate at temperature up to 1000K are achievable. It is also expected that certain specific configuration of sensors could have response time in order of mili-second and sensitivity until 0.1%. In a paper submitted to Sensors and Actuators B, Dr. Lundstrom has reported his 25 years of field effect gas sensor research work (Lundstrom et al. 2007). It is found that a 0.2~0.3V voltage shift is expected when a Pd MOS Si based device is tested under 1% H_2 gas condition. We are expecting the same result from our SiC devices since both devices share the same H_2 sensing mechanism.

CHAPTER 3

THEORETICAL BACKGROUND

3.1 Operation principal of Metal-Oxide-Semiconductor capacitor

A MOS capacitor is the simplest MOS device with a catalytic metal electrode. The MOS capacitor consists of an oxide film sandwiched between a P- or N-type semiconductor (here, Silicon is used for illustrated) substrate and a metal plate called gate as shown in Fig 3.1. The study of the behavior of this capacitor under varying biased that applied between substrate and gate is a powerful way to investigate the quality of the oxide layer and the quality of the oxide-semiconductor interface. For this type of structure, the terminals are placed on the metal and semiconductor substrate. The oxide layer must be insulating. Hence, its thickness must be large enough to prevent tunneling between the metal and semiconductor.

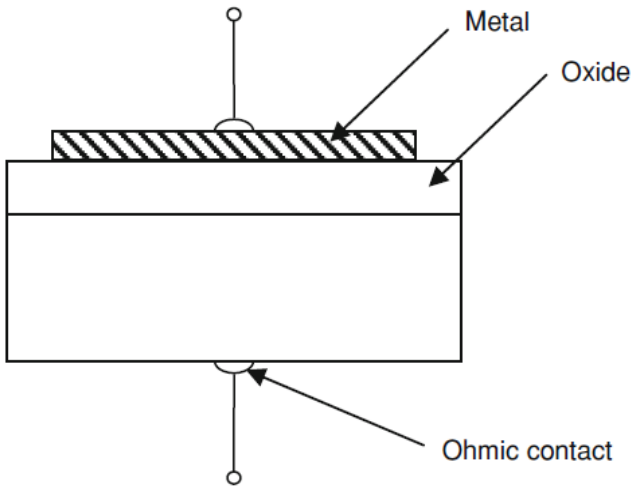


Figure 3.1: Cross-sectional view of a MOS structure.

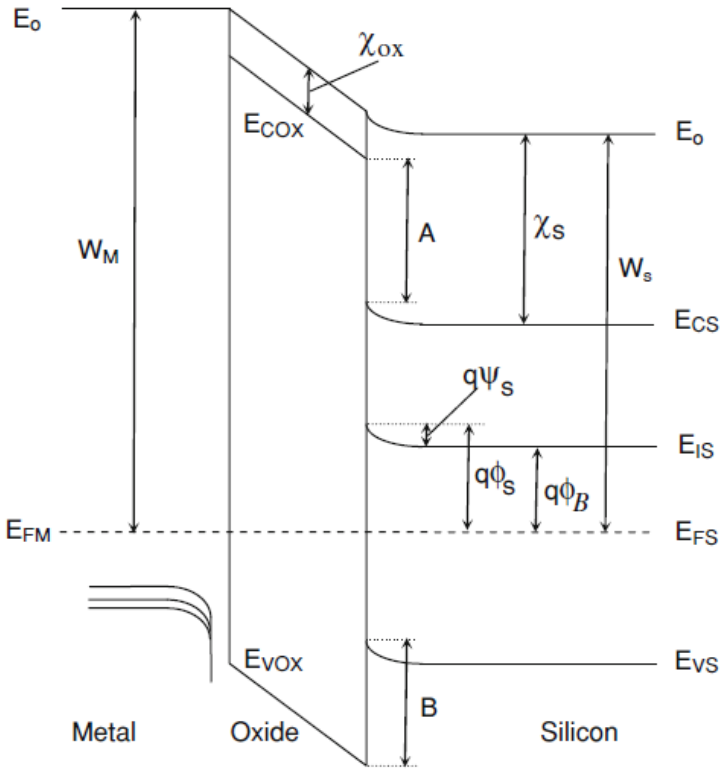


Figure 3.2: Energy band diagram of unbiased real MOS structure (Grove 1967).

Fig 3.2 shows the energy band diagram of an unbiased MOS structure when the work function of the metal W_M and work function of semiconductor W_S are different. The diagram shows the position of the different energy levels such as Fermi level in the gate (E_{FM}) and in the semiconductor (E_{FS}). In this figure, χ_S represents the electron affinity for the semiconductor and χ_{ox} for the oxide. Fig 3.2 also shows that certain energy barriers exist between the metal and the oxide as well as between the semiconductor and the oxide. For example, an energy $(W_M – q\chi_{ox})$ would be needed to move an electron from the Fermi level of the metal E_{FM} to the lowest unoccupied states in the oxide, and $A + (E_{CS}–E_{VS})$ would be needed to move an electron from the semiconductor valence band to the lowest unoccupied states in the oxide, where W_M is the work function of metal, E_{CS} and E_{VS} the bottom

of conduction band and top of valence band of the semiconductor, respectively. ‘‘A’’ represents the difference between the bottom level of the conduction bands of oxide and semiconductor at the semiconductor–oxide interface and q is the electron charge. The importance of these energy barriers is that they prevent the free flow of carriers from the metal to the semiconductor or vice versa. Some typical values for such a structure are shown in Table 3.1.

Table 3.1: Typical values in the energy bands of a MOS structure (Hübertet et al. 2011)

Metal	Oxide	Silicon
$W_M = 4.8$ eV (Au)	$\chi_{ox} = 0.9$ eV	$\chi_S = 4.1$ eV
$W_M = 4.1$ eV (Al)	$E_{COX}–E_{VOX} = 8.1$ eV	$E_{CS}–E_{VS} = 8.1$ eV
	$A = 3.2$ eV	$4.1\text{ eV} < W_S^* < 5.2$ eV
	$B = 3.8$ eV	

*W_S varies with doping concentration and temperature

Fig 3.2 shows the various potentials. The potential may be defined by the following equation,

$$q\phi = E_F - E_i(x). \tag{3.1}$$

where E_F is the extrinsic Fermi level and E_i is the intrinsic energy level in the semiconductor. The potential $\phi(x)$is called the bulk potential ϕ_B in the bulk ($x\rightarrow\infty$) and the surface potential ϕ_S at the surface (x = 0). Location of any other energy level e.g. an interface trap level within the semiconductor band gap may be specified by stating its distance in electron volt (eV) from the intrinsic level. The band bending $\psi(x)$ is defined as:

$$\psi(x) = \phi(x) - \phi_B. \tag{3.2}$$

where $\psi(x)$ represents the potential at any point x in the depletion layer with respect to its value in the bulk. In particular, the barrier height $\psi_S = \phi_S - \phi_B$ is the total band bending.

The MOS structure is called ideal if the following two conditions are met:

i. The work function of metal W_M and work function of semiconductor W_S are equal, $W_M = W_S$, which implies that in the three materials, all energy levels are flat, when no voltage applied to the structure. This case is illustrated in Fig 3.3.

ii. There exists no extra charge in the oxide and at the semiconductor-oxide interface, which implies that the electric field is zero everywhere in the absence of any applied voltage.

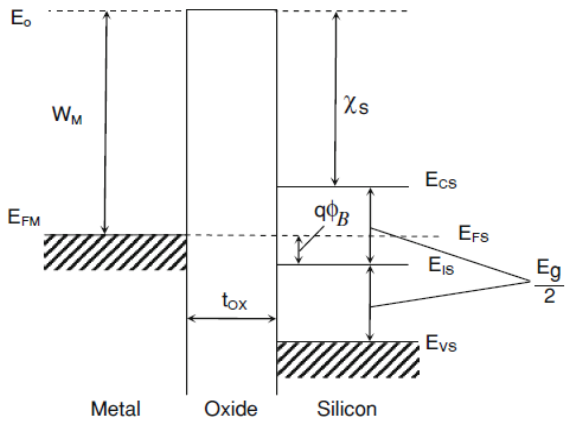


Figure 3.3: Energy band diagram of unbiased ideal MOS structure (Grove 1967, Sze 1981)

MOS capacitance will vary with the applied gate to substrate voltage. The capacitance versus voltage characteristics (C-V curve) of MOS capacitors that result from the modulation of the width of the surface space charge layer (SCL) by the gate field have been found to be extremely useful in the evaluation of the electrical properties of oxide-semiconductor interfaces which will further discussed on section 3.2. There are three regions of interest, namely as - accumulation, depletion and inversion in the C–V characteristics of the MOS capacitor (see section 3.2, Fig. 3.8). A MOS capacitor fabricated on a P-type substrate is the case treated here.

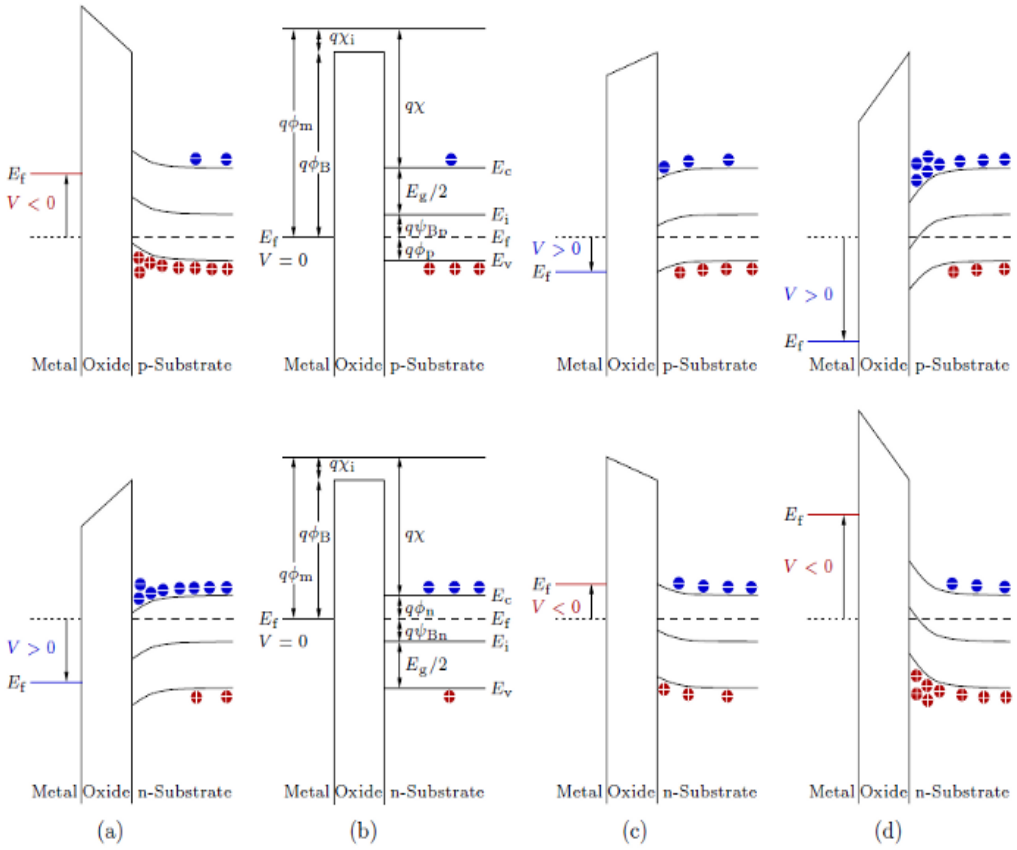


Figure 3.4: The energy band diagrams for ideal MOS-capacitors under different bias conditions: (a) accumulation, (b) flatband, (c) depletion, and (d) inversion.

3.1.1 Accumulation

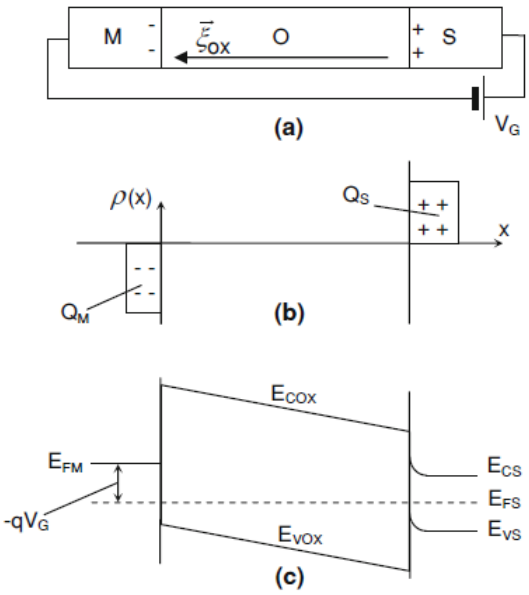


Figure 3.5: Schematic representation of P-MOS structure under bias resulting in accumulation mode, (a) biasing condition, (b) charge distribution, (c) energy band diagram (Grove 1967, Sze 1981).

When an external voltage V_G is applied to the semiconductor surface in MOS capacitor, the carrier densities change accordingly in its surface region. With large negative bias applied to the gate, holes are attracted by the negative charges to form an accumulation layer (Fig 3.5). The high concentration of these holes will form the second electrode of a parallel plate capacitor with first electrode at the gate. Since the accumulation layer is an indirect ohmic contact with the P-type substrate, the capacitance of the structure under accumulation conditions must be approximately equal to the capacitance of the oxide,

$$C_{\text{ox}} = \frac{\varepsilon_o \varepsilon_{ox}}{t_{\text{ox}}} \tag{3.3}$$

where ε_o is the permittivity of the free space, ε_{ox} the relative permittivity of oxide, and t_{ox} the oxide thickness. This capacitance is always expressed per unit gate area [F cm^{-2}]. It does not vary with bias V_G as long as the structure is maintained in accumulation mode. At the same time, it is also independent of the frequency as long as the motion of the majority carriers, which contribute to substrate charge ΔQ_S, can keep pace with the incremental speed of gate charge ΔQ_M. This is true if the frequency of the applied small signal is smaller than the reciprocal of the dielectric time constant of silicon, i.e. 10^{11} Hz. Under this condition, the Fermi level near the silicon surface will move to a position closer to the valance band edge as shown in Fig 3.5(c).

3.1.2 Depletion

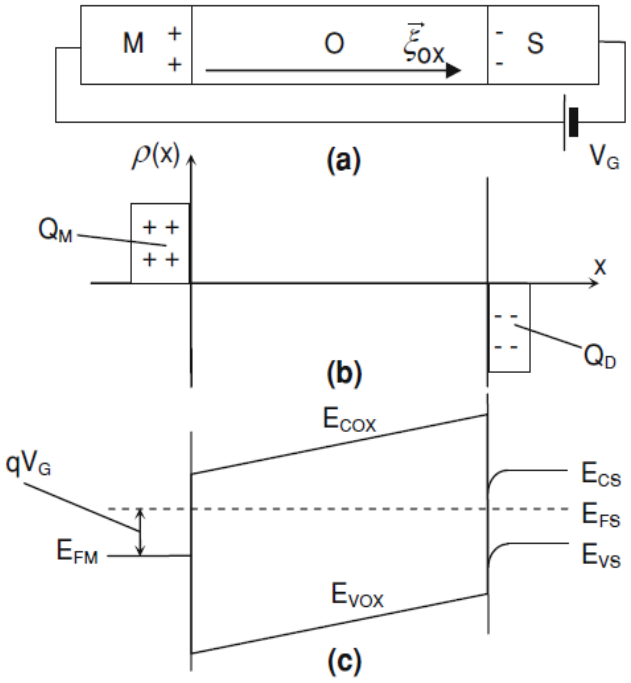


Figure 3.6: Schematic representation of P-MOS structure under bias resulting in depletion mode, (a) biasing condition, (b) charge distribution, (c) energy band diagram (Grove 1967, Sze 1981).

When negative charges are removed from the gate, holes leave the accumulation layer until the semiconductor will be neutral everywhere. This applied gate bias is called the flat band voltage. As the bias on the gate is made more positive with respect to flat band, holes are repelled and a region is formed at the surface which is depleted of carriers (Fig 3.6[b]). Under depletion conditions, the Fermi level near the semiconductor surface will move to a position closer to the center of the forbidden region as illustrated in Fig 3.6(c). Increasing the positive voltage V_G will tend to increase the width of the surface depletion region X_D, the capacitance from the gate to the substrate associated with MOS structure will decrease, because the capacitance associated with the surface depletion region will add in series to the capacitance across the oxide. Thus the total capacitance per unit area from the gate to substrate under depletion conditions is given by

$$C(V_{\mathrm{G}}) = \left(\frac{1}{C_{\mathrm{ox}}} - \frac{1}{C_{\mathrm{S}}(V_{\mathrm{G}})} \right)^{-1}, \tag{3.4}$$

Where C_S is the Si capacitance per unit area, is given by

$$C_{\mathrm{S}}(V_{\mathrm{G}}) = \frac{\varepsilon_o \varepsilon_S}{X_{\mathrm{D}}}, \tag{3.5}$$

and,

$$X_{\mathrm{D}} = \sqrt{\frac{2\varepsilon_o \varepsilon_S \psi_S}{qN_{\mathrm{A}}}}. \tag{3.6}$$

where the relation between the applied gate voltage V_G and the total band bending w_S can be written as

$$V_G = \psi_S + \frac{\sqrt{2\varepsilon_o \varepsilon_S q N_A \psi_S}}{C_{ox}} \tag{3.7}$$

Since only minority carriers contribute to the substrate charge ΔQ_D, the capacitance is independent of frequency.

3.1.3 Inversion

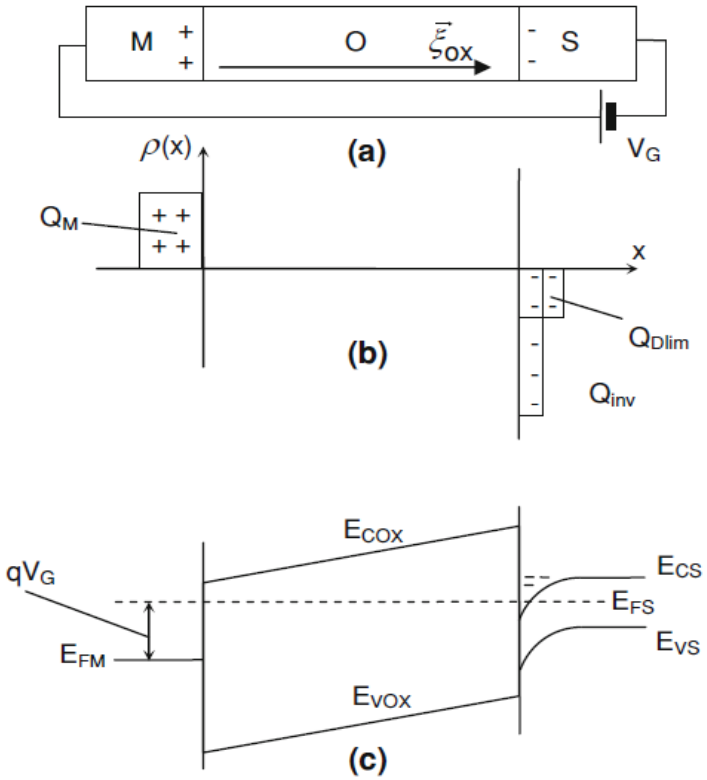


Figure 3.7: Schematic representation of P-MOS structure under bias resulting in inversion mode, (a) biasing condition, (b) charge distribution, (c) energy band diagram (Grove 1967, Sze 1981).

With increasingly applying positive voltage, the surface depletion region will continue to widen until the onset of surface inversion is observed (n-type), an inversion layer is formed, and the Fermi level near the silicon surface will now lie close to the bottom of conduction band (Figure 3.7). This inversion layer is very

thin (1–10 nm) and separated from the bulk of semiconductor by the depletion layer. The buildup of inversion layer is a threshold phenomenon. The threshold condition marks the equality of the concentration of minority carriers to the doping concentration. At the onset of inversion, the depletion layer width reaches a limit, X_{DLim} as shown in Fig 3.7(b). Since the charge density in the inversion layer may or may not be able to follow the ac variation of the applied gate voltage, it follows that the capacitance under inversion conditions will be a function of frequency.

3.1.4 Low and High Frequency Capacitance

At first we consider the low frequency case, as illustrated in Fig.3.8. It corresponds to the thermal equilibrium in which the increase in the gate charge δQ_M is balanced by the substrate charge δQ_{inv}: It arises when the frequency of the small signal is sufficiently low (typically less than 10 Hz). The low frequency capacitance of the structure, C_{LF}, is equivalent to that of the oxide layer, just as in accumulation mode,

$$C_{\mathrm{LF}} = C_{\mathrm{ox}}. \tag{3.8}$$

When the frequency of applied small signal is high (typically above 10^5 Hz), the increase of charge in the metal-side δQ_M is now balanced by the substrate charge δQ_D, since the minority carriers can no longer adjust their concentrations. The charge modulation δQ_D occurs at distance X_{DLim} of the semiconductor–oxide interface. It follows that the high frequency capacitance of the MOS structure, C_{HF}, is given,

$$\frac{1}{C_{HF}} = \frac{1}{C_{ox}} + \frac{1}{C_{D\,lim}}. \tag{3.9}$$

where

$$C_{D\,lim} = \frac{\varepsilon_o \varepsilon_S}{X_{D\,lim}}, \tag{3.10}$$

and,

$$X_{D\,lim} = \sqrt{\frac{4\varepsilon_o \varepsilon_S kTLn\left\langle \frac{N_A}{n_i} \right\rangle}{q^2 N_A}}. \tag{3.11}$$

As a result, the capacitance is practically independent of positive or negative bias for both high frequency inversion and low frequency inversion.

3.2 Capacitance-Voltage Characteristics

Capacitance-Voltage curve or, in simply, C-V curve plotting is a common electrical technique for investigating information on the electrical properties of insulating materials and charge phenomena in MOS structures. Below, some of the characteristics of the C-V plot will be reviewed, and how it is used to identify and characterize yield and process integration problems will be discussed.

3.2.1 Ideal MOS

Fig. 3.8 shows a high and low-frequency C-V plot of an ideal MOS structure. The solid line denotes the high frequency curve, while the dashed line denotes the low frequency curve. The capacitance is high when the structure is in accumulation, decreases toward the flat band condition at zero volt applied to the structure, and decreases further toward C_{min}, the steady state high frequency condition. In the low frequency condition, the capacitance begins to rise again at a voltage called the match point. As the voltage increases, the capacitance increases to a level similar to that in accumulation. This is sometimes referred to as a quasi-static C-V measurement, and is measured using the voltage ramp method. In the voltage ramp method, the voltage is ramped very slowly at a given rate typically less than 50 mV/sec. When the frequency is considered to be low, the generation of electron-hole pairs keeps up with the signal. When the frequency is high, only majority carriers can follow the signal. At low frequencies, the charge exchange with the inversion minority carriers is in step with the varying signal. The small signal response dQ to dV appears at the surface (inversion) rather than that at the depletion boundary. As the inversion layer forms, the capacitance increases back to $C_{max} = C_{ox}$.

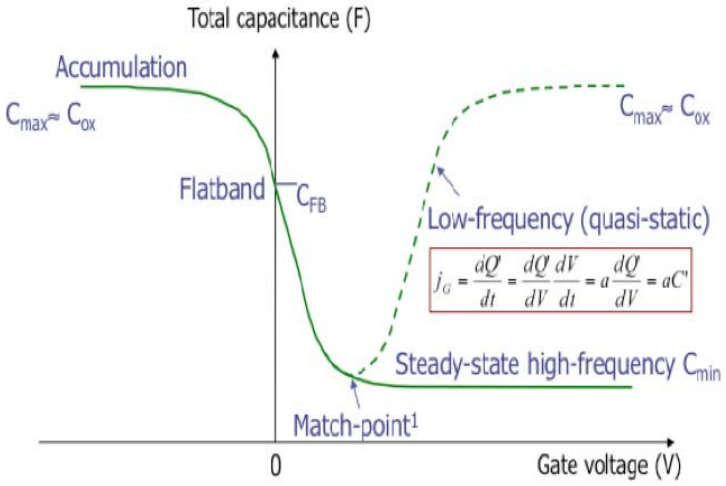


Figure 3.8: High and Low Frequency Capacitance-Voltage plot of an ideal MOS structure (p-type). (Henderson C, 2011)

Fig.3.9 shows a high-frequency C-V plot of an ideal MOS structure. High frequency measurements allow the user to hide the effects of minority carriers since minority carriers cannot react fast enough to follow the signal. The capacitance is high, approximately that of the ideal capacitance across the oxide, when the voltage is negative. When the voltage is negative, the MOS structure is in accumulation, so the surface holes concentration increases, raising the capacitance. At flatband, the capacitance should be equal to the ideal capacitance for the flatband condition. As the voltage goes positive, the MOS structure goes into depletion. The surface electrons concentration (minority carries) increases, but remains at a level which too low to offset the decrease in surface holes concentration. In weak inversion, the surface electrons concentration is higher than the surface holes concentration, causes the depletion width (x_d) increases, lowering the capacitance further. In strong inversion, the surface electrons concentration equals the surface holes concentration at flatband, and the depletion width reaches its maximum. The capacitance reaches its minimum at this value as well. The steady-state condition is

reached when sufficient electrons are supplied to the surface mechanisms like electron-hole pair generation.

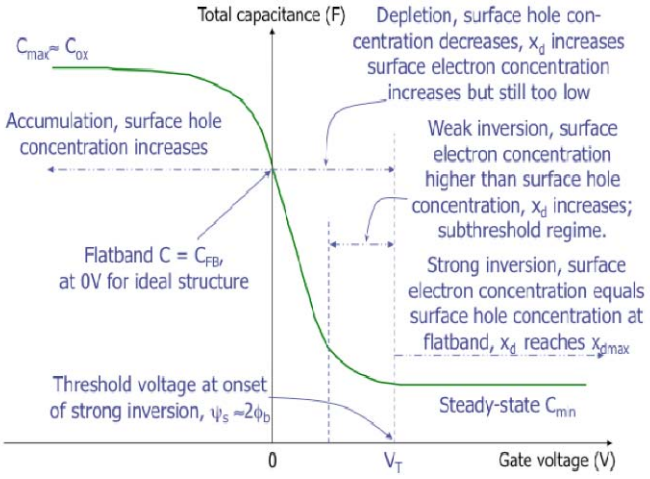


Figure 3.9: Details of C-V plot at high frequency of an ideal MOS (p-type). (Henderson C, 2011)

Nevertheless, an ideal MOS device does not agree with experimental results, and this difference is due to the presence of the oxide charges and the work function difference that exists in practice (non-ideal) but was not taken into account in the theoretical treatment of an ideal MOS capacitor. Early studies of the MOS devices showed that the threshold voltage V_{Th} and the flat band voltage V_{FB} could strongly be affected by charges store in the oxide layer. The understanding of the origin and nature of these charges is very important if they are to be controlled or minimized during device processing. The net result of the presence of any charges in the oxide is to induce a charge of opposite polarity in the underlying semiconductor.

3.2.2 Non-ideal MOS

In the real MOS structure, the work function of the metal and the work function of the semiconductor are different. For this reason, there exists an electric field in the oxide and in the top layer of the semiconductor even in the absence of an applied voltage. To obtain the flat band conditions, $\psi_S = 0$, a bias on the gate must be applied relative to the substrate, which can be written as

$$\Delta V_{\mathrm{FB1}} = \frac{W_{\mathrm{MS}}}{q}. \tag{3.12}$$

As an example, for Al–SiO_2–Si structure, a typical value of ΔV_{FB1} is 0.3 V for an n-type Si substrate and 0.8 V for a p-type. The effect of a work function difference may cause a shift of the actual C–V curve with respect to the ideal one. The flat-band-voltage shift ΔV_{FB1} occurs along the voltage axis as illustrated in Fig. 3.10.

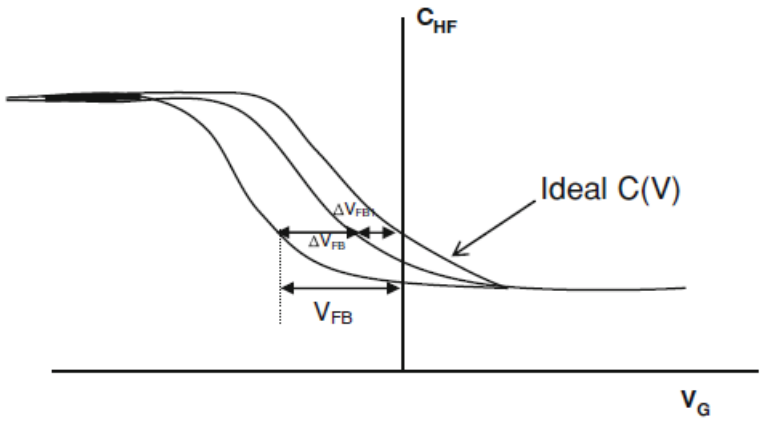


Figure 3.10: The C–V curves of a P-type MOS structure showing the flat band voltage shifts introduced by work function difference and oxide charges.

Whether mobile ions or other types of oxide charges are distributed unevenly in the bulk, their density $\rho(x)$ varies with distance (and with time in case of time-dependent stress). To study the influence of oxide charges distribution on the properties of the MOS structure, at first, the effect of only those charges, which are located within a layer between x and $x + dx$, is calculated. The origin of the x-axis is taken at the metal-oxide interface as shown in Fig. 3.10. In a second step, the effect of the various layers from zero to t_{ox} is added. Using Gauss's law, the electric field in the oxide ζ_{ox} exhibits a discontinuity $\delta\zeta_{ox}$ when crossing this charge layer. This discontinuity is given by

$$\delta\zeta_{\mathrm{ox}} = \frac{\rho(x)dx}{\varepsilon_o \varepsilon_{ox}}. \tag{3.13}$$

For ensuring flat band condition in the Si, ζ_{ox} must be zero on the right hand side of the discontinuity. Thus, the profile of the electric field should be as shown in Fig. 3.10(b) and the corresponding gate voltage that ensures the flat band condition is given by:

$$\delta V_{\mathrm{FB}} = \frac{-\rho(x)xdx}{\varepsilon_o \varepsilon_{ox}} \tag{3.14}$$

Using a classical result of electrostatics, namely the superposition theorem, the effects of all layers comprised between zero and t_{ox} are added and the gate

voltage shift ΔV_{FB}, which is necessary to ensure a flat-band condition at the semiconductor–oxide interface, is found to be

$$\Delta V_{\mathrm{FB}} = -\int_{\grave{a}}^{t_{ox}} \frac{\rho(x)xdx}{\varepsilon_o \varepsilon_{ox}}. \tag{3.15}$$

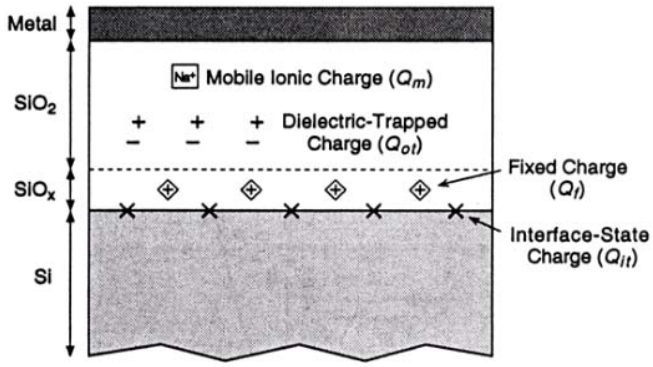


Figure 3.11: Four different charges in MOS structures (Grove 1967, Sze 1981).

Normally, there are four different types of charges in MOS structures

(i) Mobile ion charge, Q_m

Elements such as sodium (Na) or other alkali ion are mobile within the oxide under raise temperature (e.g.>100℃) and high-electric field operation will cause the stability problem in the entire device.

(ii) Fixed-oxide charge, Q_f

The fixed-oxide charges, O_f is located within approximately 3nm of the oxide-semiconductor interface. This charge is fixed and cannot be charged or discharged over a wide variation of surface potential. Generally, Q_f is positive and depends on the oxidation and annealing conditions. It has been

suggested that when the oxidation is stopped, some ionic semiconductor atoms are left near the interface. It may result in the positive interface charge Q_f. Typical fixed-oxide charges densities for a carefully treated SiO_2-Si interface system are about $10^{10}cm^{-2}$ for a <100> surface and about $5x10^{10}cm^{-2}$for a <111> surface.

(iii) (Dielectric) Oxide-trapped charge, Q_{ot}

Oxide-trapped charges are associated with defect in the oxide layer. These charges can be created, for example, by X-ray radiation or high-energy electrons bombardment. The trap is distributed inside the oxide layer. Most of process-related oxide trapped charges can be removed by low-temperature annealing.

(iv) Interface-trapped charge, Q_{it}

It is due to the oxide-semiconductor interface properties and dependent on the chemical composition of this interface. The interface trap density is orientation dependent. For Si sample, the interface trap density in <100> orientation is about an order of magnitude smaller than that in <111> orientation. By the treatment of 450℃ H_2 annealing, the value of Interface-trapped charges for <100> orientation Si can be as low as $10^{10}cm^{-2}$.

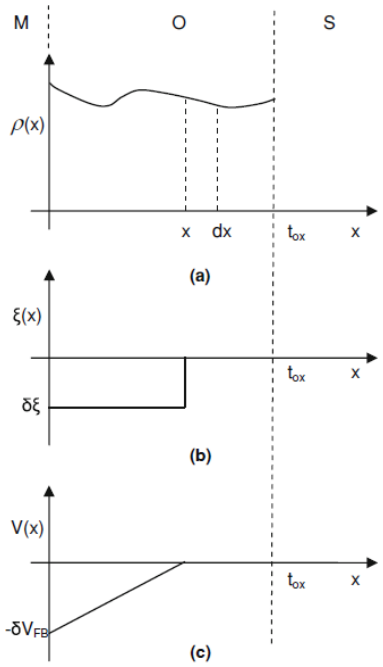


Figure 3.12: Distribution of (a) oxide charges, (b) electric field and (c) voltage within the oxide of MOS structure

3.3 Hydrogen Sensing Mechanism

Hydrogen sensors based on the capacitor structures were first reported by Lundström and DiStefano in 1976. When the MOS capacitor is exposed to H_2, the H_2 molecules will dissociate on the metal surface because of catalytic behavior of the metal. Part of this dissociation H_2 atoms are adsorbed on the metal surface. Some of the H_2 atoms consequently diffuse from the metal film until they reached and adapted at the metal–dielectric interface (Fig. 3.13). These H_2 atoms are polarized that creates a bipolar layer, due to the reduction of metal–dielectric work function difference in H_2. Hence, there is a change in electric charge that gives rise to an extra electric field in insulator. As a result, this causes concentration of mobile carriers in semiconductor layer to change and create a decrease of the flat

band voltage of the MOS capacitor (as shown in Fig. 3.14). The resulting H_2 atoms diffuse through the metal within microseconds to dielectric surface. It can occur at temperatures as low as 150°C. Besides, the speed at which it occurs may increase followed by increasing in temperature. It is apparent that this type of sensor is sensitive to H_2. Nevertheless, extra carriers due to electron-hole pairs generation by light sources (nature or man-made) also have significant effect on the output of sensors. The sensing principle of a typical hydrogen-sensitive MOS capacitor is illustrated in Fig. 3.14.

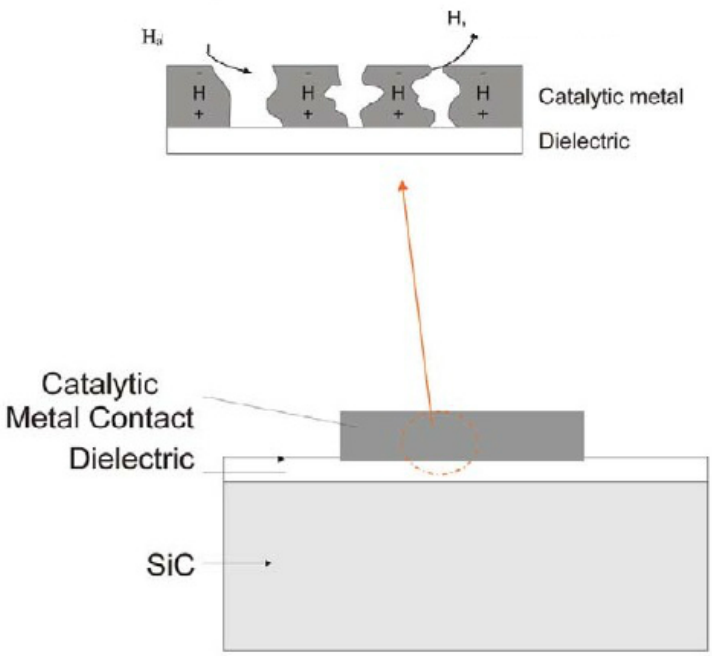


Figure 3.13: Dissociation and association of hydrogen gas molecules at metal surface. (Wright, Horsfall and Vassilevski 2008)

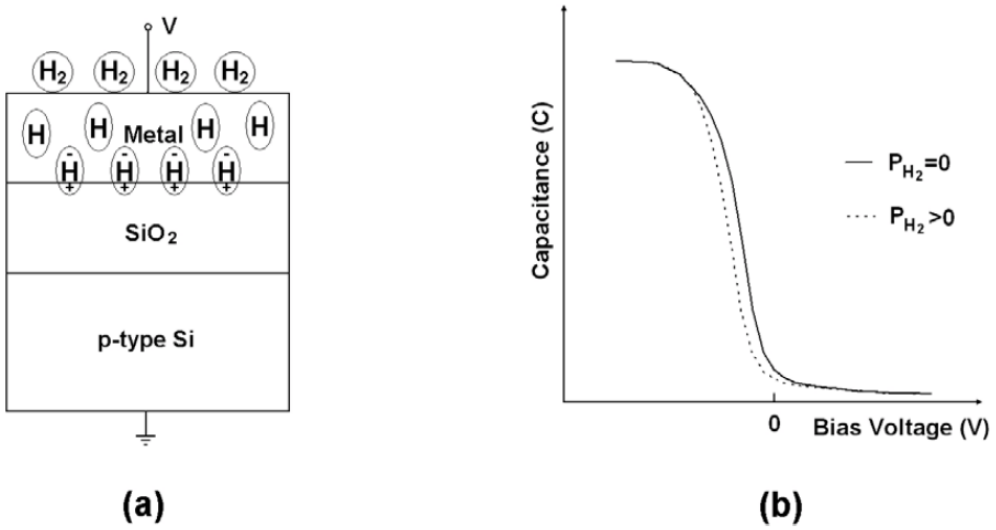
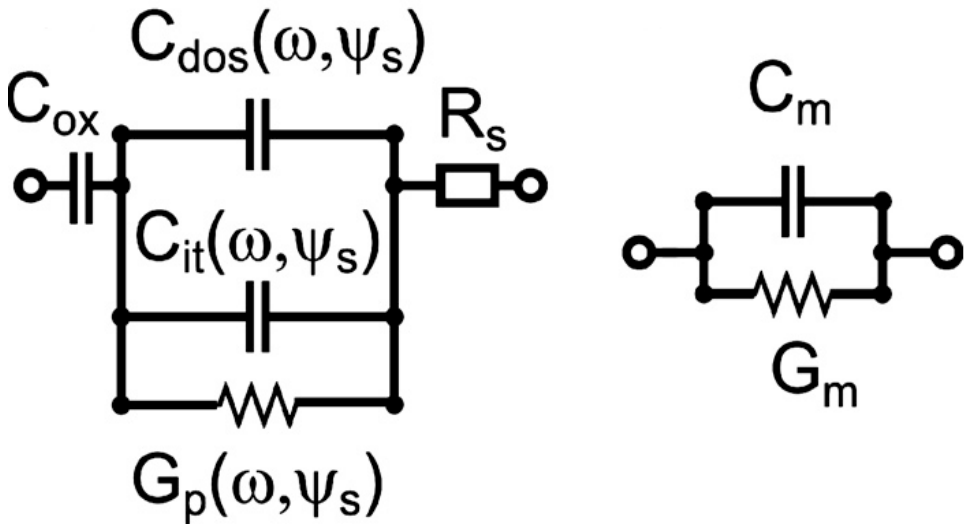


Figure 3.14: Sensing principle of a typical hydrogen-sensitive MOS capacitor. (a) Device scheme and the formation of a dipole layer of hydrogen atoms at the metal/SiO_2interface. (b) Shift of the C-V curve due to the introduction of H_2

3.4 Extraction of Interface Trap Properties

From section 3.3, it is found that a low interface trap density in oxide layer is essential for the MOS capacitor type H_2 sensor. Thus, it is important for us to study the interface trap properties of the testing sample before the H_2 sensing experiment is conducted. Nicollian and Brew (1982) first proposed that these trap density can be deduced from *G*-ω measurements, which is one of the most sensitive methods to determine D_{it}, interface trap density of 10^9 cm^{-2} $eV^{-1}$and lower. This section briefly describes the relation between the measure admittance of the MOS capacitor and interface trap properties. The trap density is not measured directly. It can be extracted from measured admittance using an equivalent circuit. The equivalent circuit of the MOS capacitor is shown in Figure 3.15.



(a) (b)

Figure 3.15: Equivalent circuit of the MOS capacitor. (a) It showing the oxide capacitance C_{ox}, the semiconductor capacitance C_{dos} (ω, ψ_s), the equivalent parallel interface trap capacitance C_{it} (ω, ψ_s), the equivalent parallel interface trap conductance G_p (ω, ψ_s) and a series resistance R_s. (b) C_m and G_m are measured capacitance and conductance of equivalent circuit of impedance analyzer.

Compared with the standard equivalent circuit shown in a lot of text books, an equivalent parallel interface trap capacitance C_{it} (ω, ψ_s) is added to the circuits. It is introduced to the circuits to reflect the fact that an energy loss can arise when recombination or generation through the interface trap occur. By using the impedance analyzer, we can measure C_m and G_m. The parallel conductance (G_p) is related to the measured impedance by equation 3.16

$$G_p = \frac{\omega^2 C_{ox}^2 G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2}. \tag{3.16}$$

The G_p versus angular frequency(ω) curve is plot and the peak value of G_p/ω can be obtained. Interface traps in the proximity of Fermi level can change their occupancy. Their frequency dependent response depends on the trap time constant given by

$$\tau = \frac{\exp[\Delta E/k_B T]}{\sigma v_{th} D_{dos}},$$

$$= 2\pi/\omega \qquad (3.17)$$

where ΔE is the energy difference between trap level E_T and majority carrier band edges (E_{CB} or E_{VB}, respectively), σ, the capture cross section of the trap, v_{th} , the average thermal velocity of the majority carriers and D_{dos}, effective density of state.

Maximum loss occurs when interface traps are in resonance with the applied ac signal ($\omega\tau$=1). Assuming that surface potential fluctuations can be neglected, the trap density, D_{it} is estimated from the normalized parallel conductance peak, $(G_p/\omega)_{max}$:

$$D_{it} \approx \frac{2.5}{Aq}\left(\frac{G_p}{\omega}\right)_{\max}, \qquad (3.18)$$

where A is the device area and q is the electron charge.

CHAPTER 4

CAPACITORS FABRICATION PROCESS AND MEASUREMENT SET UP

4.1 MOS Fabrication Techniques

The 4H-SiC wafers used in this project were made by Cree. It is an *n*-type substrate with resistivity of 0.02 Ω-cm. A thin 0.50 μm *n*-type buffer layer (doping density of 1×10^{18} cm^{-3}) and a 10.4 μm thick lightly-doped *n*-type epilayer (doping density of ~$1x10^{15}$ cm^{-3}) were grown on it. Then, the wafers were sliced into 1 cm x 1 cm square pieces for MOS capacitor fabrication. Before the samples go for thermal oxidation, the standard Radio Corporation of America (RCA) cleaning procedure was adopted to clean it. This cleaning process consisted of two stages (standard cleaning-1 and standard cleaning-2). A high pH alkaline mixture (NH_4OH : H_2O_2 : DI-water = 1:1:5) was used in SC-1 and a mixture of (HCl, H_2O_2 and DI-water) in the ratio of (1:1:6) is used in SC-2.

After the cleaning process, the samples were put in a horizontal oxidation furnace for thermal oxidation. The Schematic diagram of horizontal oxidation furnace is shown in Fig.4.1. The oxide (SiO_2) layer was grown in pure oxygen at 1150^{o}C for around nine hours. The thickness of the oxide layer is 120nm. After the oxide layer was formed, it was annealed in pure nitric oxide (NO) for two hours to improve the interface quality. Then, the top metal contact (Pt, Pd or Mo) was deposited. The metallization was done by sputtering method. The diameter of the

contact is around 700μm. Back oxide was then removed with buffered oxide etch. After the MOS capacitor was fabricated, it was tested under three difference concentrations of hydrogen gas (0.2%, 1% and 2%). The measurement is done under 480^{o}C temperature environment.

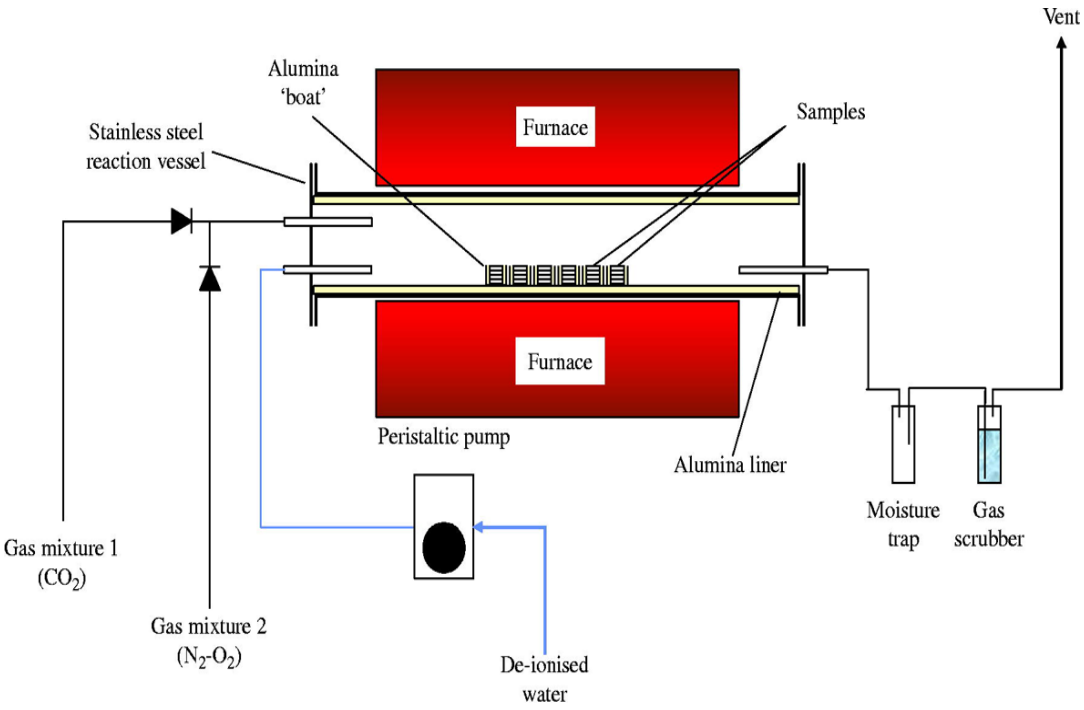


Figure 4.1: Schematic diagram of horizontal oxidation furnace.

4.2 C-V measurements set-up

We were using these C-V measurements in studying the mechanisms and qualities of the MOS capacitor H_2 sensors, especially at the gate-oxide interface in detail. A scheme of the sample and the setup is shown in the Fig. 4.2 below.

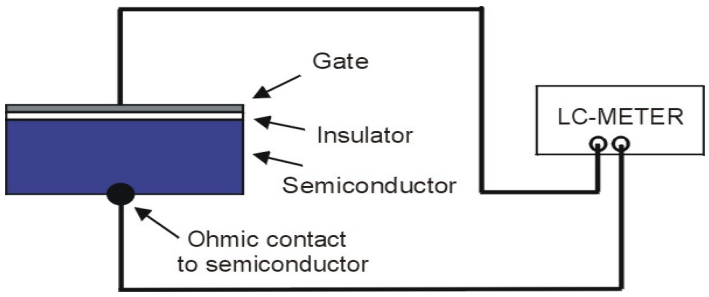


Figure 4.2: An illustrated configuration of C-V measurements on MOS structure sample.

By definition, capacitance is the change in charge (Q) in a device that occurs when it also has a change in voltage (V):

$$C \equiv \frac{\Delta Q}{\Delta V} \tag{4.1}$$

One general practical way to implement this is to apply a small AC voltage signal (mV range) to the device under test, and then measure the resulting current. Integrate the current over time to derive Q and then calculate C from Q and V. C-V measurements in a semiconductor device are made using two simultaneous voltage sources: an applied AC voltage signal (dV_{ac}) and a DC voltage (V_{dc}) that is swept in time, as illustrated in Fig. 4.3.

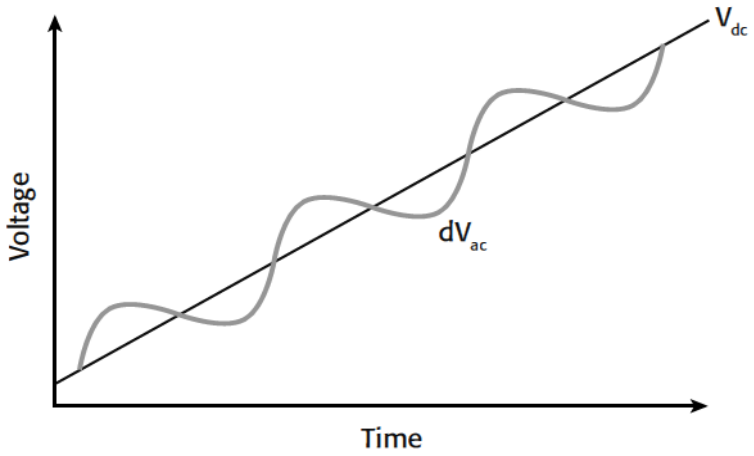


Figure. 4.3: AC and DC voltage of C-V Sweep Measurement.

The magnitude and frequency of the AC voltage are fixed; the magnitude of the DC voltage is swept in time. The purpose of the DC voltage bias is to allow sampling of the material at different depths in the device. The AC voltage bias provides the small signal bias so the capacitance measurement can be performed at a given depth in the device.

Essentially, as we have already discussed in chapter 2 and 3, the MOS capacitor is just an oxide placed between a semiconductor and a metal gate. The semiconductor and the metal gate are the two plates of the capacitor. The oxide functions as a dielectric. The area of the metal gate defines the area of the capacitor. The MOS-C can be fabricated directly on the semiconductor substrate and the backside of the substrate is used as one of the two electrical contacts needed for a C-V test (see Fig 4.4).

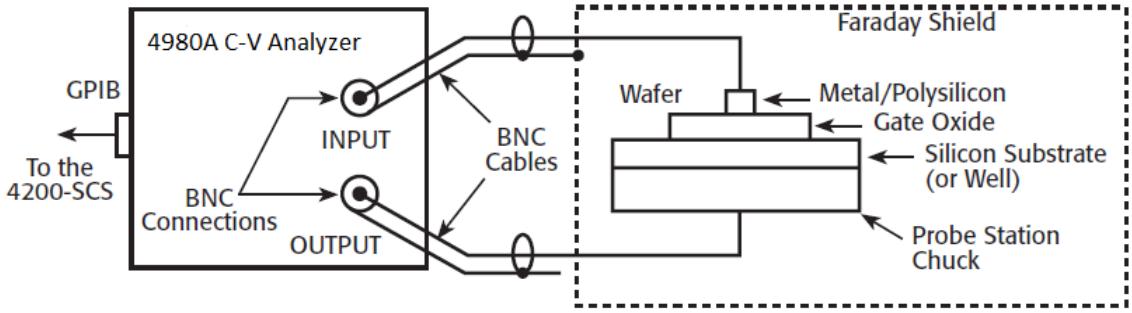


Figure 4.4: MOS-CC-V analyzes instrument connection.

To measure MOS-C C-V curve, the MOS-C is typically connected to a C-V analyzer. The Agilent 4980A Precision LCR meter was used in our laboratory testing. The C-V analyzer applies a high frequency (1 MHz or 100 kHz) drive signal to the backside of the substrate, via the chuck of a prober. (The prober chuck must be "floating" electrically to avoid diverting the drive signal to ground.) This high frequency AC drive signal is superimposed on a relatively slow DC bias sweep. The signal is picked up through the gate via the manipulator or probe needle. (**Note:** If the polarity of the measurement is reversed — the drive signal is applied to the gate via the probe needle, and the signal is measured at the substrate — the additional capacitance of the chuck on which the substrate rests complicates interpretation of the results. Additionally, the chuck acts as an antenna, picking up RF noise from the environment.) Sometimes, as with a MOS-C on a production wafer, the substrate-to-oxide interface is replaced with a well-to-oxide interface. In such cases, a conductor is available at the top of the wafer that connects to the well. The analyzer drive signal is applied to the well through this conductor, and the signal is measured at the gate as usual. The sensor performance testing configuration in our lab is shown in Fig. 4.5.

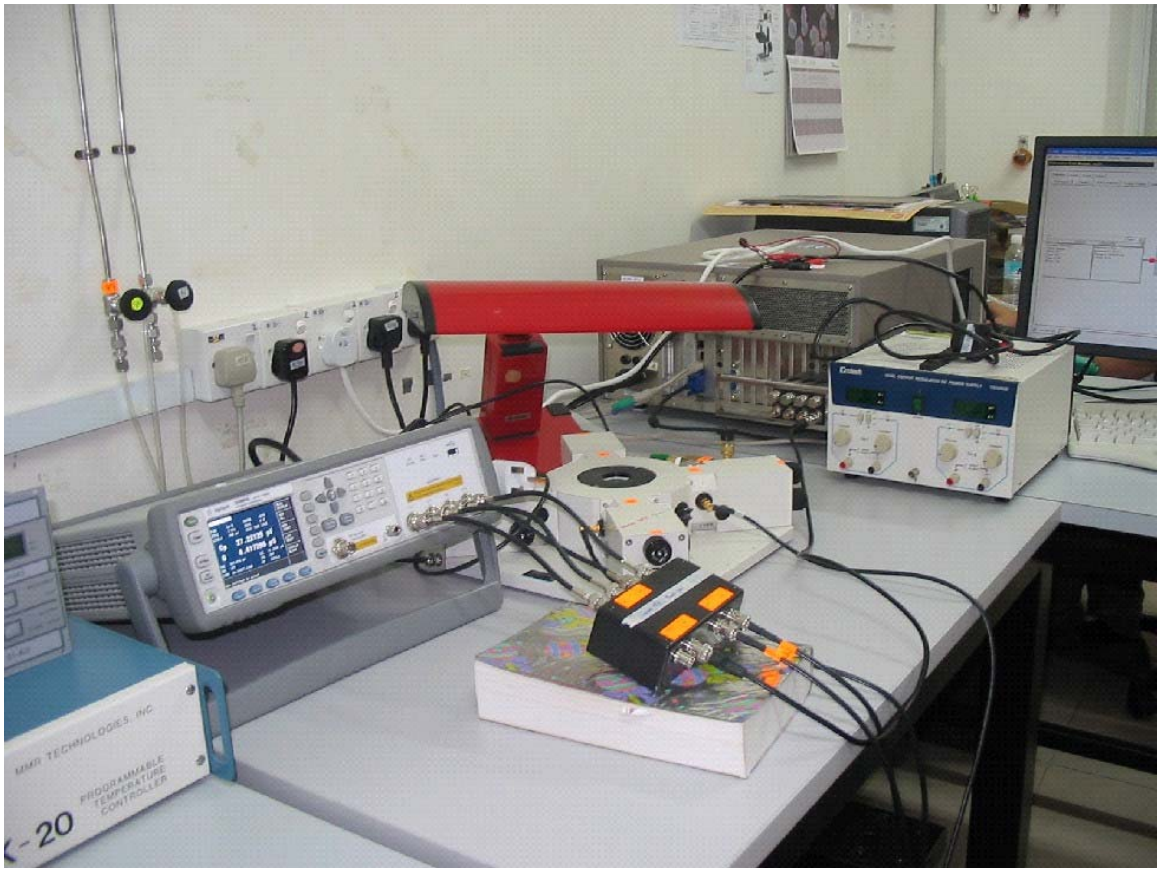


Figure 4.5: Sensor performance testing configuration

Beside the Agilent 4980A Precision LCR meter, a Keithley Model 4200-SCS Semiconductor Characterization System equipped with the 4200-CVU Integrated C-V Option was also used to carry out the C-V measurement. The Keithley system is an integrated measurement system that can include instruments for both I-V and C-V measurements, as well as software, graphics, and mathematical analysis capabilities. The Keithley Test Environment Interactive (KTEI) software that controls the Model 4200-SCS incorporates a list of a dozen test projects specific to C-V testing. Each project is paired with the formulae necessary to extract common C-V parameters, such as oxide capacitance, oxide thickness, doping density, depletion depth, Debye length, flatband capacitance,

flatband voltage, bulk potential, threshold voltage, metal-semiconductor work function difference, and effective oxide charge.

To simplify testing, a project (CVU_MOScap) has been created for the 4200-SCS that makes C-V measurements on our MOS capacitor and extracts measurement parameters such as oxide thickness, flatband voltage and threshold voltage. Figure 4.6 is a screen shot of the project. Figure 4.7 illustrates a C-V sweep generated with the (CVSweep_ MOScap) test module. This test performs a capacitance measurement at each step of a user-configured linear voltage sweep. A C-V graph is generated from the acquired data, and several device parameters are calculated using the Formulator which is a tool in the 4200-SCS's software that provides a variety of computational functions, common mathematical operators, and common constants. Figure 4.8 shows the window of the Formulator. These derived parameters are listed in the Sheet Tab of the Test Module.

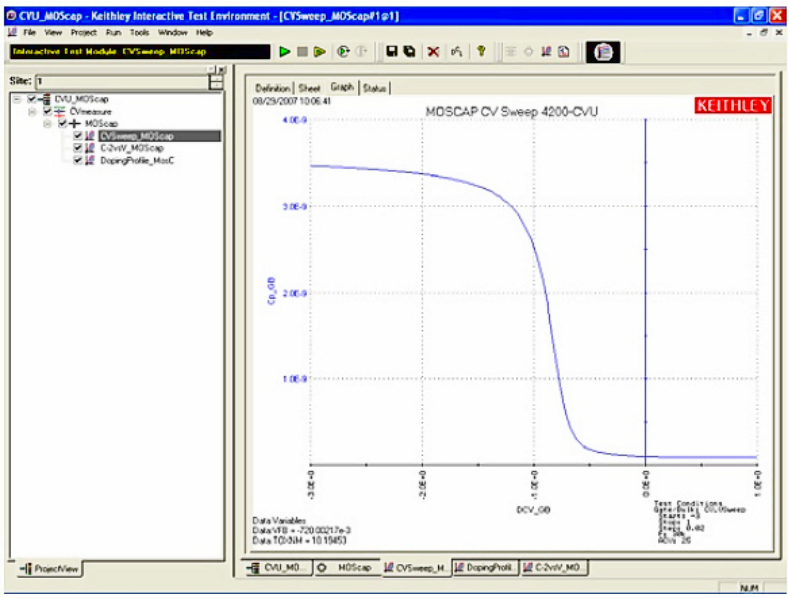


Figure 4.6: C-V Sweep created with MOScap project for the 4200

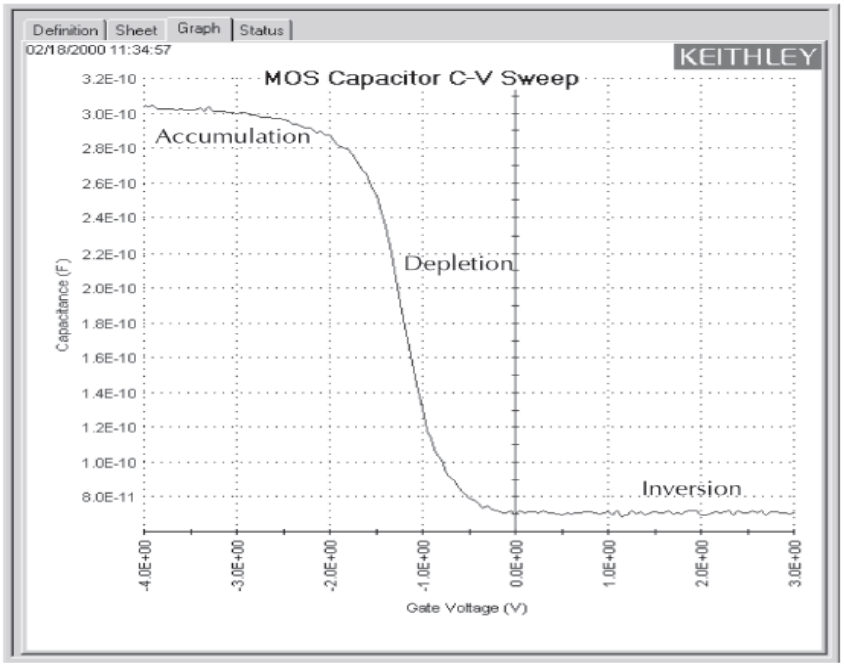


Figure 4.7: C-V curve of a p-type MOS capacitor measured with the 4200-CVU

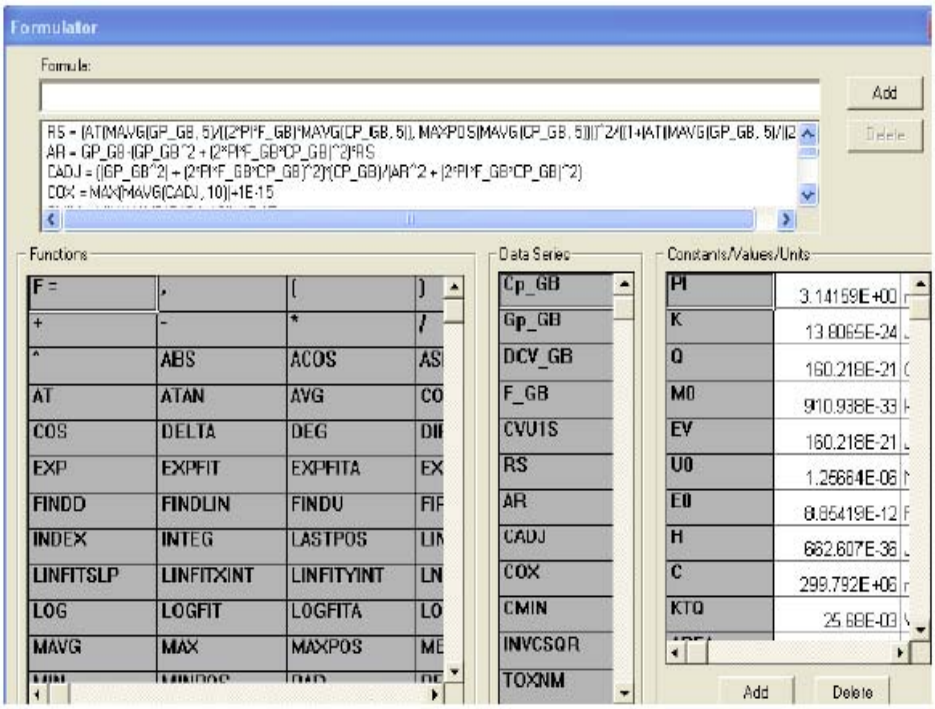


Figure 4.8: Formulator window with parameters derived.

CHAPTER 5

RESULTS AND DISCUSSION

5.1 Interface State Density Profiling of the Thermal Oxide

For MOS structure, it is found that passivation of oxide and interface traps by nitridation is an effective way to improve the interface quality. The passivation can be done by post-oxidation annealing in nitric oxide (NO) or nitrous oxide (N_2O) gas (Jamet, Dimitrijev and Tanner 2001, Cheong et al 2003, Cheong, Bahng and Kim 2007). This section will present a study on the distribution of interface state density as a function of energy within the *n*-type 4H-SiC bandgap at the thermal oxide-SiC interface for our MOS samples underwent post-oxidation NO anneal.

The density of states profiling of our sample is deduced from *G*-ϕ measurements that have been introduced in chapter 3. The voltages applied on the gate of our MOS sample ranges from 2 V to 3 V. This range covered from depletion to flat-band condition. The method is only applicable when majority carriers do not contribute much to the conductance loss. It is found that the conductance measured below 2 V was too noisy and therefore discarded. The Fermi level was found to be 0.23 eV below the conduction band for the given doping density. Hence, the energy range that could be probed was from the Fermi level to midgap. The parallel conductance (G_p), the conductance of the semiconductor in the equivalent circuit, was calculated from the measured impedance, G_m and C_m. The G_p versus ω curve was plotted and it is used to deduce the interface state

densities. Figure 5.1 shows the results of our test MOS samples. The interface state densities in these samples is $1x10^{11}$ $cm^{-2}eV^{-1}$ around 0.2 eV below the conduction band. The interface state densities is around two orders smaller ($1x10^{9}$ $cm^{-2}eV^{-1}$) at 0.9 eV below the conduction band. Since the interface state densitiy was acceptably low, these samples may be used for hydrogen gas sensor.

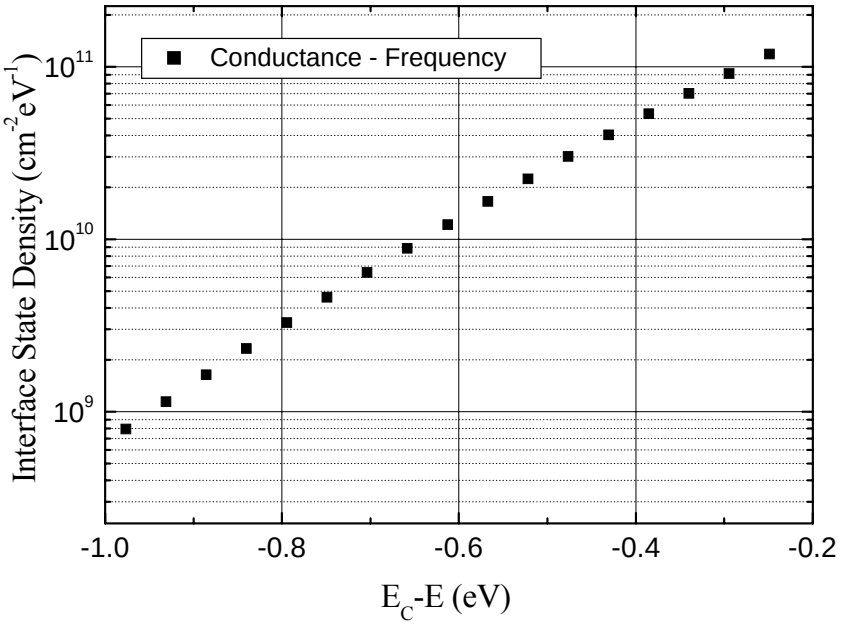


Figure 5.1: Interface state density as deduced from *G*-ω measurements

5.2 Hydrogen Sensing Results

Three material systems are studied in this project. They are Pd/SiO_2, Pt/SiO_2 and Mo/SiO_2. They are tested under three difference concentrations of hydrogen gas (0.2%, 1% and 2%). The measurement is done under 480°C

temperature environment.

Fig. 5.2 shows the results obtained from the Pd/SiO_2/SiC MOS capacitor. Around 0.4V shift in the device flat band voltage is observed when our sample is exposed to H_2 gas. A strong response (~0.42V) is seen even under very low H_2 concentration. These results demonstrate that Pd/SiO_2/SiC is a promising material system for high temperature H_2 gas sensing application.

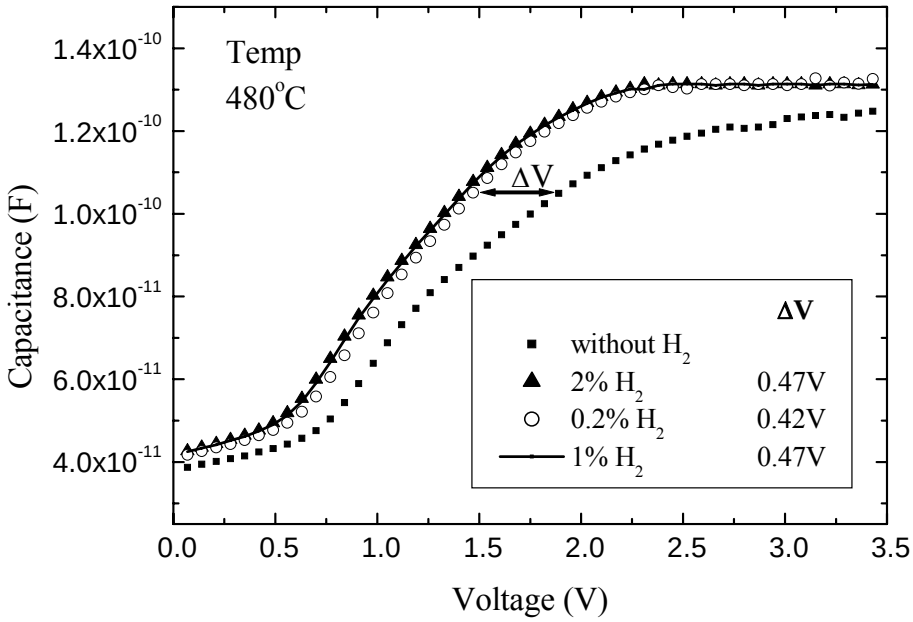


Figure 5.2: High-frequency (1 MHz) capacitance of the Pd/SiO_2/SiC sample measured in difference hydrogen concentration.

Fig. 5.3 shows the results obtained from the Pt/SiO_2/SiC sample. The flat band voltage shift is lower compared to that of Pd/SiO_2/SiC devices. 0.29 V voltage shift is observed when our sample is exposed to gas with 0.2% H_2 concentration. The Pt/SiO_2/SiC material system is another good candidate for high temperature H_2 gas sensor.

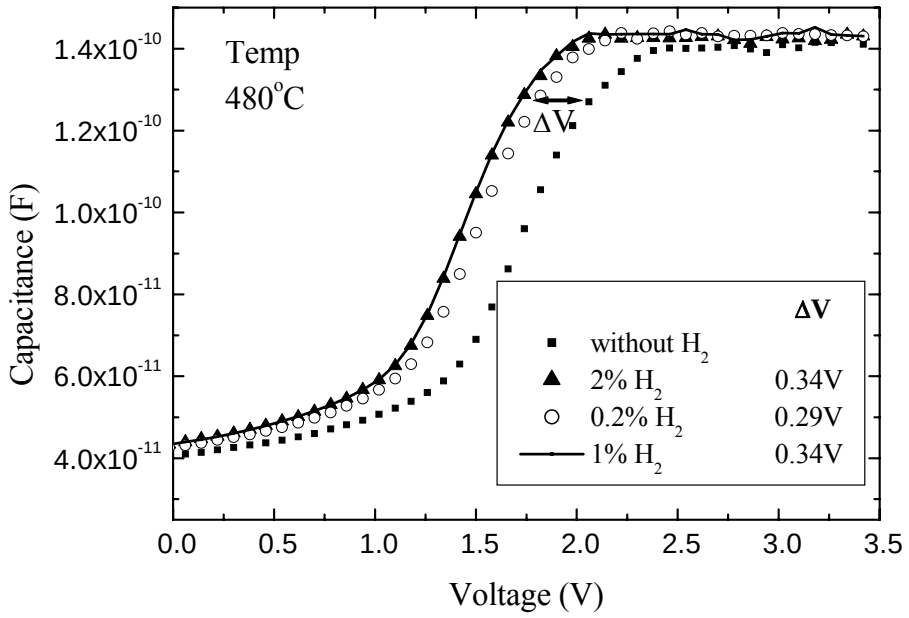


Figure 5.3: High-frequency (1 MHz) capacitance of the Pt/SiO_2/SiC sample measured in difference hydrogen concentration.

The third material system we have tried in this project is Mo/SiO_2/SiC. Their results are shown in Fig. 5.4. Obviously, this material system is not working. The response is so weak that it is hard to tell whether the voltage shift is due to measurement error or H_2 gas. Our results show that both Pd/SiO_2 and Pt/SiO_2 material systems are good candidate for high temperature H_2 gas sensor. Compared to Pt/SiO_2 material system, Pd-SiO_2-SiC sensor showed larger voltage shift. Nevertheless, the respond (~0.4V for Pd, ~0.3V for Pt) of both systems to 0.2% H_2 gas are acceptable good and meet our requirement. While for Mo/SiO_2 material system, we get a very disappointed result. It is believed that the poor performance of Mo-SiO_2-SiC sensors are due to the low solubility of H_2 gas in Mo. Fig 5.5 shows the H_2 solubility in the three metal contacts as a function of temperature. From Fig. 5.5, it is found that Mo has the lowest H_2 adsorption rate. Among the

tested material systems, Pd-SiO_2-SiC sensor showed largest voltage shift since there is highest solubility of H_2 gas in Pd.

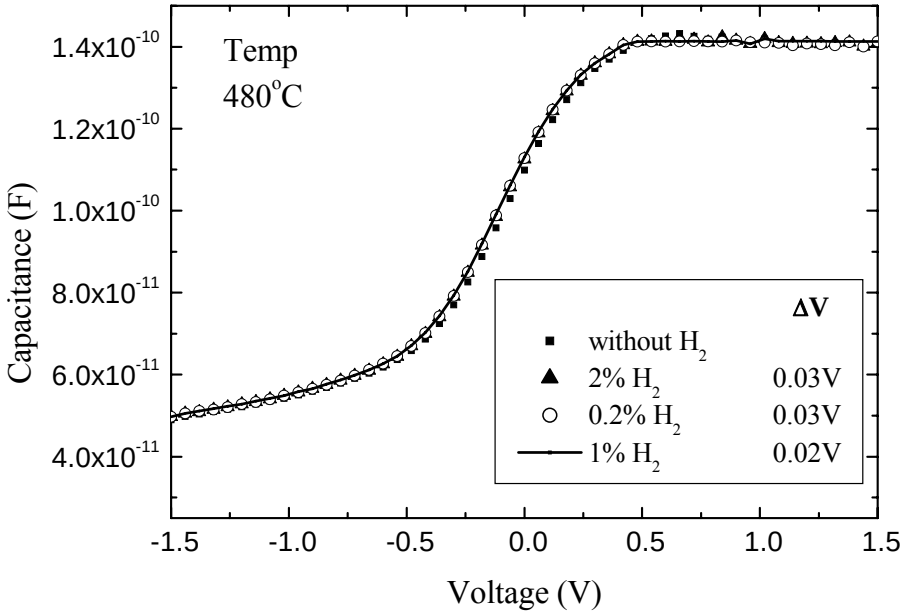


Figure 5.4: High-frequency (1 MHz) capacitance of the Mo/SiO_2/SiC sample measured in difference hydrogen concentration.

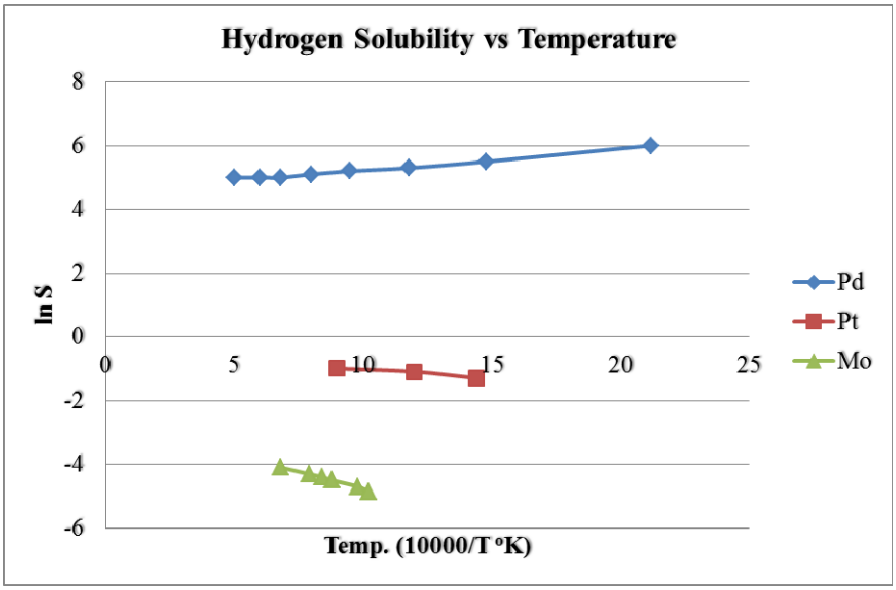


Figure 5.5: *wt*% of hydrogen dissolved in 100 g of metal at 1 atm as a function of temperature (Sax 1975, Axel 1998, DCS U. Padova).

CHAPTER 6

CONCLUSION AND RECOMMENDATIONS FOR FURTHER RESEARCH

6.1 Conclusion

In this project, SiC-based MOS capacitor type hydrogen sensors with low interface state density have been made. To passivate the oxide and interface traps in the sensors oxide layer, post-oxidation annealing in nitric oxide (NO) gas has been carried out. Our results show that the passivation of oxide and interface traps by nitridation are effective and a low interface state density of approximately $1x10^{9}$ $cm^{-2}eV^{-1}$ has been achieved in our devices. Three material systems (Pd/SiO_2, Pt/SiO_2 and Mo/SiO_2) have been used to fabricate the SiC-based hydrogen sensors. We found that Mo/SiO_2 system is not suitable for hydrogen sensing application. The $Mo/SiO_2/SiC$ sensors show very weak response to hydrogen gas. The other two devices, $Pd/SiO_2/SiC$ and $Pt/SiO_2/SiC$ sensors show promising result under high temperature condition. Around 0.3V voltage shift in their C-V characteristics is observed under 0.2% hydrogen gas concentrations and $480^{o}C$ environment.

6.2 Recommendations for Further Research

According to the results that presented in this thesis, the use of Silicon

Carbide (SiC) as the bulk material for high temperature hydrogen gas sensor applications is very promising. In order to make further progress in this direction, some outstanding items and issues, listed below, need to be further investigated.

(i) The SiC–SiO_2 interface-state density (D_{it}) is a significant aspect that affected the voltage different or shifted in C-V characterization if its density is higher than the order of 10^{11} $cm^{-2}eV^{-1}$. Although nitridation processes can reduce D_{it}, it is still has the limitation on remove some other interface-state that is believe to be due to the carbon (C) clusters that accumulated at the interface. One another suggestion for lowering D_{it} is to grow gate oxides with nitridation process and simultaneously illuminating with ultra-violet (UV) light on the SiC. It has been demonstrated that by using pre-oxidation UV–Ozone (O_3) cleaning, the accumulated carbon clusters can be dissociated. By combining nitridation process with UV illumination during oxide-growing process, some carbon clusters generated during oxidation process could be broken down into smaller carbon compounds by the UV light. Simultaneously, the nitrogen from the nitridation process can more effectively remove the smaller carbon compound.

(ii) Other catalytic metals, especially from the group of VIIIB and IB, which are nearby with Palladium (Pd) and Platinum (Pt) are also quite suitable on building the metal contact. Further study and production of H_2 gas sensors that based on these metals stuffs with giving some more promising on sensing performance of current H_2 gas sensors.

(iii) The thickness of gate oxides used in this research was around 120 nm. It is essential to investigate the quality of ultra-thin sized of gate oxides, which are thinner than 10 nm. For silicon (Si), ultra-thin gate oxides are the trend of current hydrogen (H_2) gas sensors and other semiconductor technologies and the same trend would be followed in the development of SiC-based MOS devices in term of improving the sensing performance.

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