DEVELOPMENT OF PHOTOVOLTAIC ARRAY EMULATOR (PVAE)

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May 2011

DECLARATION

I hereby declare that this project report is based on my original work except for citations and quotations which have been duly acknowledged. I also declare that it has not been previously and concurrently submitted for any other degree or award at UTAR or other institutions.

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I certify that this project report entitled "DEVELOPMENT OF PHOTOVOLTAIC ARRAY EMULATOR (PVAE)" was prepared by SEE HUI MING has met the required standard for submission in partial fulfilment of the requirements for the award of Bachelor of Engineering (Hons.) Electrical And Electronic Engineering at Universiti Tunku Abdul Rahman.

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ACKNOWLEDGEMENTS

In this section, I would like to thank for the people who had provides me any kind of helps in the process of developing the PVAE.

First of all, I would like to thank my project supervisor, Mr Chua Kein Huat, who had given me a lot of precious opinions and feedbacks for my project. During each project meeting with Mr. Chua, we discussed both the development of the system and also the writing of the report. Mr. Chua always motivates me whenever I faced problems in developing the system. When it comes to the report writing part, he advised me what kind of contents should be included and giving feedbacks after read through my report.

I would also like to thank my project partners, Siew Yeu Wen. We always discuss about the development of the project, updating each others with our own progress, and hence able to understand each other's part more clearly. Besides, he also provides me many helps and ideas during the project development and also the report writing. Without any of his helps, the project would certainly become more difficult or even impossible for me.

Finally, I must say thanks to my mother and my siblings for their love, support and continuous encouragement throughout the course.

DEVELOPMENT OF PHOTOVOLTAIC ARRAY EMULATOR (PVAE)

ABSTRACT

Photovoltaic (PV) inverter is a device to convert the solar energy into electrical energy by using solar cells. The PV inverter emits zero CO₂; hence, it is a environmental friendly resources. However, the photovoltaic array systems are inherently dependence on weather changes. Due to this limitation, an emulator call Photovoltaic Array Emulator (PVAE) is proposed. The main objectives of PVAE are to perform difference PV energy production system test under many situation without depending on weather and to perform PV energy production system test without large system and cost. The supply DC voltage to the inverter to invert it into AC voltage using PWM method, the PWM signal is generated by triangle wave compare with the sine wave phase angle based on grid network. After that, controller is used to control the voltage input of the inverter so that it can produce an output that is similar to the real PV array output. So, from the result, when the time is increase, the power from the PVAE system is increase from low power to high power and come back to low power. A PVAE simulation result is proposed. Besides that, it is also have to test about the relationship between PV and load at the three phase system. It is found when the PV is located with the unbalanced load at the heavy loaded phase in the three phase unbalanced load, it is able to reduce the voltage unbalance.

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LIST OF SYMBOLS / ABBREVIATIONS

Ι	current flowing into the load
U	across voltage of a solar cell
I_{sc}	short-circuit current
I_o	saturation current
Q	electron charge (1.6×1019C)
R_s	series parasitic resistance
Ν	junction constant
Κ	Boltzman constant (1.38×10-23J/K)
Т	PN junction temperature
R_{sh}	shunt parasitic resistance
c_p	specific heat capacity, J/(kg·K)
h	height, m
K_d	discharge coefficient
Μ	mass flow rate, kg/s
Р	pressure, kPa
P_b	back pressure, kPa
R	mass flow rate ratio
Т	temperature, K
ν	specific volume, m ³
α	homogeneous void fraction
η	pressure ratio
ρ	density, kg/m ³
ω	compressible flow parameter
ID	inner diameter, m
MAP	maximum allowable pressure, kPa

CHAPTER 1

INTRODUCTION

1.1 Overview

The demand of the electric power in Malaysia is keep increasing in the rate of 5.7% per year. In recent year, oil and gas are the main energy source in Malaysia. However, the oil reservation is estimated to last for another 19 years and gas reserves another 33 years. In order to prevent the energy crisis happen in Malaysia, Malaysia government need to strengthen the role of renewable energy as the fifth cornerstone of energy generation [1].

Photovoltaic is an array of cells containing a solar photovoltaic material that can converts solar radiation into direct current electricity. It is the method to generate the electric power by using solar cells to convert the sun light into the electricity. The process of convert ion will not cause any pollution. As a result, the photovoltaic sole is increasingly 110% per year by whole world [2]. However, the photovoltaic array systems are inherently dependence on weather changes. It is not available at night and less available in cloudy weather condition from conventional photovoltaic technologies. Typically, the output of any PV module is reduced to 5-20% of its full sun output when it operation under cloudy condition.

Photovoltaic Array Emulator (PVAE) is the system who able to represent electrically similar with the PV arrays but without depending on the weather conditions

and capable to emulate PV array systems. That can make a possible to perform difference PV energy production system test under many situation and without depending on weather or much more expensive and large systems. Photovoltaic inverters are required to know the efficiency of their Maximum Power Point Tracking Systems (MPPTS) and the quality of the energy injected in the utility under different situation of irradiation. Therefore, PVAE becomes vital to have appropriate test equipments for manufacturers and laboratories dedicated to PV inverter's R&D [3].

In Malaysia, the statutory limit of voltage unbalance factor is 1% by set from the Tenaga Nasional Berhad (TNB). PV across the phases of the network and without PV is determine, to figure out the limitation that allow the PV volumes to be accommodated on the networks before the voltage unbalance factor at any points on the network exceed the limits. For the purpose of this project, PV across the phase of the network case when PV is connects to the phase. Without PV describe the case when PV connections is open circuit with the phase.

1.2 Problem Statement

The problem statements of the proposed project address the problems and challenges faced by the development of applications on the related field. The problem statements for the PVAE are as following:

- 1. All of the photovoltaic array system is inherently dependence on weather changes. It cannot be performing the different PV power production in many conditions, such as at the night or at the raining day. It is a serious problem for the testing in manufacturers and laboratories.
- 2. In order to eliminate atmospheric dependency, previous test equipment used lamps to simulate the solar irradiation with its consequent need of huge power for testing equipments having a power bigger than 1kW but only produce a low

output power. Other ones tried to simulate the sun by a current source and a diode chain, as it is usually represented a photovoltaic panel by its electrical scheme. However, the equipment had thermal stability problems and was limited by its diode chain's fill factor.

1.3 Project Objective

The main objective of the proposed project is to emulate characteristic of a PV array energy production system under many situations and without depending on weather or much more expensive and large systems.

1.5 Project Flow Chart

Figure 1.1 shown as the flow chart of the project. It is separate to two sections; the first section more focus on doing the research related with the topic. The second section is focus on design and testing of the project.

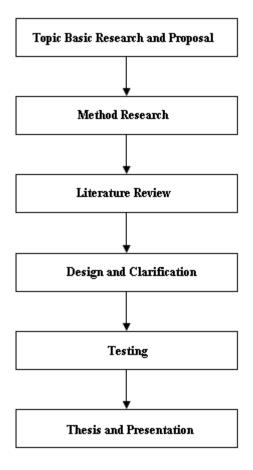


Figure 1.1: Flow Chart of the project

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

This chapter is about the research of the proposed project, photovoltaic array emulator (PVAE). Sources of the read materials are mainly from internet articles, e-books and so on. This research aims to investigate and to be clear about how to build a PVAE. Besides, examination and comment is made on the literature relevant to the area of the proposed project research.

2.2 Overview

In this section, the focus point will be onto few papers that are related to the Photovoltaic Array Emulator. The reviewed papers are listed below:

- i. Development of a Photovoltaic Array Emulator System based on a Full-Bridge Structure
- ii. Single-Phase Inverter Design
- iii. Modeling of a Single-phase Photovoltaic Inverter
- Daily Load Profiles for Residential, Commercial and Industrial Low Voltage Consumers
- v. PV Panel Model Based On Datasheet Values

Besides, some of the parts and components that build up the PVAE will also be discussed at this chapter.

2.2.1 Development of a Photovoltaic Array Emulator System based on a Full-Bridge Structure

In this paper, they believe that the photovoltaic industry is growing exponentially and PVAE is becoming an essential tool for manufactures and laboratories dedicated to PV inverter's R&D. It is required to know the efficiency of their Maximum Power Point Tracking Systems (MPPTS), the quality of the energy injected in the utility under different situations of irradiation, and specially the performance of the different anti-islanding methods in solar inverters under large penetration of PV. Therefore, it is important to have appropriate test equipments for manufacturers and laboratories dedicated to PV inverter's R&D. In this paper, a photovoltaic array emulator has been presented and its static and dynamic response evaluated.

A wide range of array simulators or emulators have been proposed and developed few years ago. For example, some of them without galvanic isolation, some based on structures with low frequency, some using PWM principle and so on. In this paper, they proposed developing PVAE based on full-bridge structure.

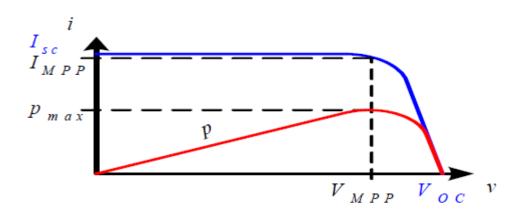


Figure 2.1: Current-Voltage characteristic of PV-module

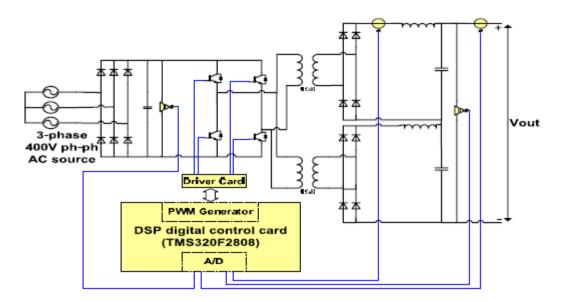


Figure 2.2: Electrical scheme of PV converter

Figure 2.1 shows the I-V curve of the PV whereas figure 2.2 shows the scheme of PV converter. From the figure 2.1, the curve is obtained in ideal conditions with a given temperature, solar irradiation and cell's material. In the figure 2.2, the proposed PVAE is formed by a full-bridge structure with high-frequency transformers and PWM principle. It is used to drive the IGBT at the full-bridge inverter part. However, the proposed project is to develop a PVAE in single phase but on this paper, the PVAE is using 3-phase converter. So that, some of the parts in this article as a reference to developing the PVAE. [2]

2.2.2 Single Phase Inverter Design

Inverter is used in PVAE to invert DC voltage into AC voltage. In this paper, Prof. Ali proposed how to design a PWM inverter. When design an inverter, there are three basic schemes to convert the fuel cell plus boost module's DC energy into AC.

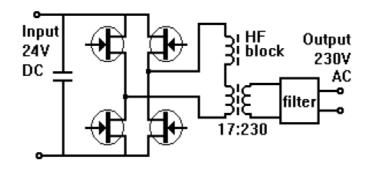


Figure 2.3: Circuit topology of a chop and transform inverter

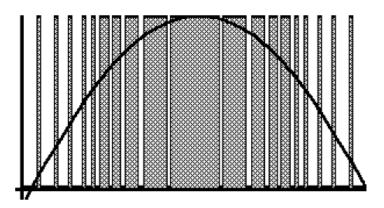


Figure 2.4: Sine Waveform

Figure 2.3 is the type to converts the low voltage DC into a low voltage AC, after that only converts the low voltage AC into the wanted AC voltage. The advantages are the low voltage operation is safe, the insulation from the grid after the inverter, the ease with which it makes sine-wave which feeds into the transformer and the most important in many aspects, which is reliability due to the low number of semiconductors in the power path. However, the disadvantage of this inverter is slightly lower efficiency, typically 92%. Figure 2.3 shows as a good approximation of a sine wave, all type of equipment will run on this signal. The sine wave is approximated by a high-frequency chopping plus filtering. This chopping is also known as PWM. This is the only waveform allowed to be grid-connected, when the inverter is capable of synchronization to the grid.

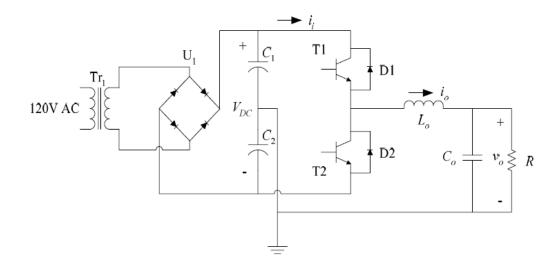


Figure 2.5: Single Phase Inverter

Figure 2.4 shows single phase inverter. U_1 is used to invert the AC voltage source into DC voltage. In this type of inverter, due to low output voltage and power, the voltage rating of a power switch does not affect its cost and volume significantly, while less number of the power switches leads to simpler control, higher reliability and lower cost. The L_0 and C_0 is the filter for the output from harmonic response. [6]

2.2.3 Modeling of a Single-phase Photovoltaic Inverter

In this paper, they are present the design of a single-phase photovoltaic inverter and simulation. The concept of this inverter is representing an AC power based on the main power distribution. This paper also has provided some technical information for the inverter design and circuit used. In technical information section, they are using controlling the power angle or the difference voltage magnitude to control the inverter. In this paper, I am more focus on how to coupling of the two circuits, which is PV circuit connect to the grid network.

As we know, to connect two different AC network circuits, it has to make the AC voltage waveform of two circuits have been similar. It is possible to achieve by using technique phase-locked-loop (PLL). This technique is used a replicate of a grid

sinusoidal voltage source to pass through a zero-crossing detector (ZCD) to convert into a square pulse of frequency 50 Hz and magnitude 230V rms. The ZCD, as its name implies detects zero crossing on the input waveform and triggers at each zero crossing. Once the detector detect a zero crossing, it triggers to a pre-set value and detect a second zero crossing, it will triggers back to zero. In this way can easy convert a sinusoidal input into a square waveform. After that, the ZCD output was used as the input of triggering block. The triggering pulse will produce a square wave output that will be in phase with the grid voltage. This phase comparison is shown in Figure 2.6.

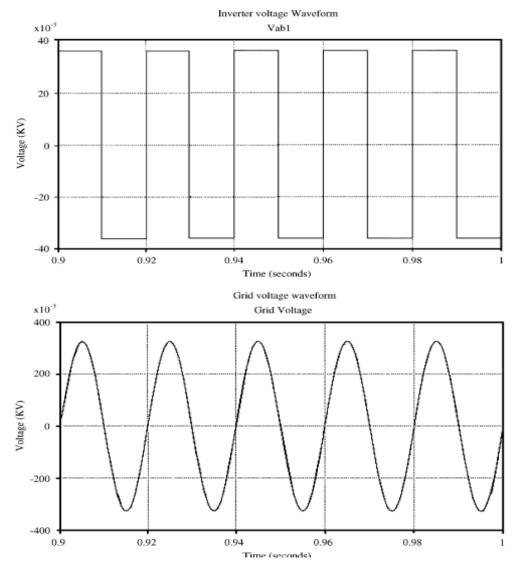


Figure 2.6: Inverter output and grid voltage waveform

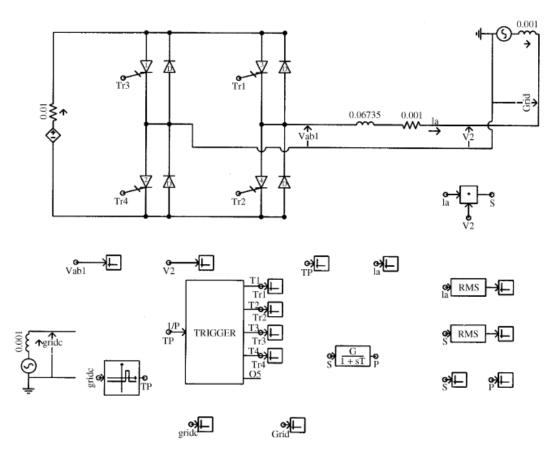


Figure 2.7: The complete network

The circuit show as above is the circuit to generate the PWM signals who able to connect with the grid network. The phase power of the grid is taking as the input reference for the PWM. This paper also have discuss about the relationship between the phase angle and power output. From this paper, when phase angle is slightly increase 2° , the rms value of current was increase from 1.3*A* to 1.6*A*, the output power is increase. When the phase angle is slightly decrease 2° , this slight shift in latter case reactive power was flowing from the grid toward the inverter, the power is show as negative. [7]

2.2.4 Daily Load Profiles for Residential, Commercial and Industrial Low Voltage Consumers

In this paper, they are represents the result of the study carried out from the determination of the industrial, commercial and residential consumer's daily load. The

paper proposes the customers representative daily load curve are defined statistically form.

For the residential consumer's daily load, the maximum demand is during at night between 9pm to 12am. The high standard deviation values are due to the diversity in the use of electric appliance mainly the shower. For the commercial consumer's daily load, the maximum demand is during business hours which are between 8am to 6pm. The measurements corresponding to weekdays were considered. Both of the consumer's daily load are show as below.

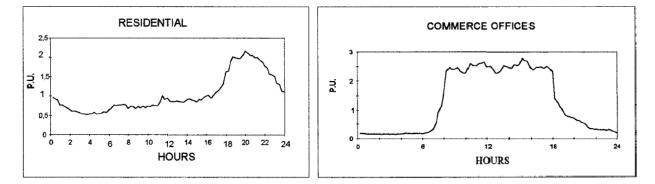


Figure 2.8 shown as the residential and commercial consumer's daily load

From this paper, a statistic analysis of residential and commercial consumers load curves applied to a sample of consumers to recommendation of the representative curves of consumers by consume range in the residential and by type of activity in the commercial sector. it can let us more understand about the load different residential and commercial. It also helps us to decide which load should be used to test this project. [8]

2.2.5 PV Panel Model Based On Datasheet Values

A model for photovoltaic panels, based exclusively on datasheet parameters has been developed and implemented. In this paper, there are presented some numerous methods, for extracting the panel parameters. The most common methods that we use are based on measurement of the I-V curve or other characteristic of the panel. A photovoltaic panel model, can based on the value provide by the manufacturer's data sheet.

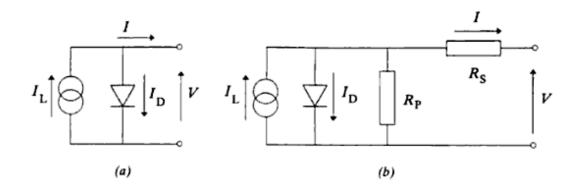


Figure 2.9: Equivalent circuit of a PV cell

The circuit of figure 2.9(a) shows that equivalent circuit of an ideal device. However, in real solar cell there exist other effects. These affect the external behavior of the cell. We consider at least two of these extrinsic effects, which is the series resistance and current leaks proportional to the voltage. These effects are distributed throughout the device and cannot always be represented by a resistance of constant value. The relationship between the series and parallel resistance, when the value of parallel resistance is small, it will reduce the open circuit voltage and fill factor, the short circuit current is not affect by it. For the series resistance, when the value is large, it will reduce the fill factor and short circuit current, but will not affecting the open circuit voltage.

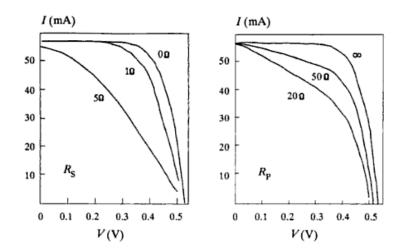


Figure 2.10: The effect of series and parallel resistance on the I-V characteristic of solar cell

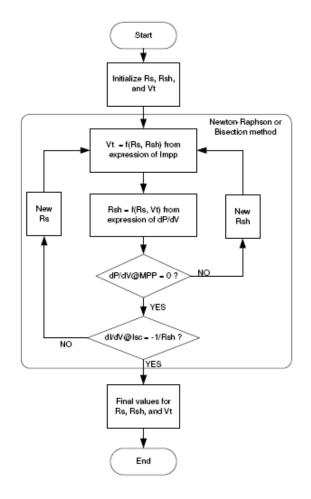


Figure 2.11: Flow Chart of determination of the PV model parameters

Figure 2.10 is show that the process of finding the value of series and parallel resistance. By solving this, we can get three equations, there equations do not allow separating the unknowns and solving them analytically, they are solved by using numerical methods. The equation is shown as: [9]

$$I_{mpp} = I_{sc} - \frac{V_{mpp} + I_{mpp}R_s - I_{sc}R_s}{R_{sh}} - \left(I_{sc} - \frac{V_{oc} - I_{sc}R_s}{R_{sh}}\right)e^{\frac{V_{mpp} + I_{mpp} - V_{oc}}{n_s V_t}} - (1)$$

$$\frac{dP}{dV} = I_{mpp} + V_{mpp} \left[\frac{\frac{(I_{sc}R_{sc} - V_{oc} + I_{sc}R_{s})e^{\left(\frac{V_{mpp} + I_{mppR_{s} - V_{oc}}{n_{s}V_{t}}\right)}{n_{s}V_{t}R_{sh}} - \frac{1}{R_{sh}}}{1 + \frac{R_{s}}{R_{sh}} + \frac{(I_{sc}R_{sh} - V_{oc} + I_{sc}R_{s})e^{\left(\frac{V_{mpp} + I_{mppR_{s} - V_{oc}}{n_{s}V_{t}}\right)}{n_{s}V_{t}R_{sh}}}}{n_{s}V_{t}R_{sh}} \right] - (2)$$

$$-\frac{1}{R_{sh}} = \frac{-\frac{(I_{sc}R_{sh} - V_{oc} + I_{sc}R_{s})e^{\left(\frac{I_{sc}R_{s} - V_{oc}}{n_{s}V_{t}}\right)}}{n_{s}R_{sh}V_{t}} - \frac{1}{R_{sh}}}{1 + \frac{R_{s}}{R_{sh}} + \frac{(I_{sc}R_{sh} - V_{oc} + I_{sc}R_{s})e^{\left(\frac{I_{sc}R_{s} - V_{oc}}{n_{s}V_{t}}\right)}}{n_{s}V_{t}R_{sh}}} - (3)$$

CHAPTER 3

METHODOLOGY

3.1 Introduction

This chapter describe about the method use design of the proposed for the PVAE. The overall system model is also included in this chapter together with a flow diagram show as below. Each module and also its processes will be described and illustrated more detailed on how it operates and achieving its individual tasks. From the figure show as below, it can separate in two parts, which is PV inverter and PWM generator process. PV inverter is the DC sources connect with the inverter and invert the DC power to AC power. After that, it will supply to the grid network. The PWM generator process is get the phase information from the grid network, combine the phase that control by the user and make this phase become a sine wave. After that, this sine wave will send to compare with the triangle wave and generate out a PWM signal. This PWM signal is send to inverter to control the inverter.

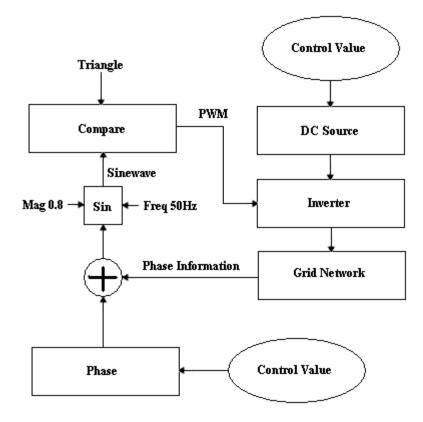
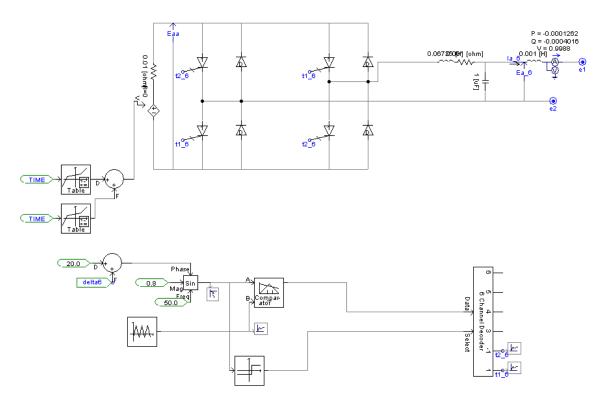


Figure 3.1 Block Diagram of Proposed System

3.2 System Overview

DC voltage is a source of this PVAE, also is a controller of this PVAE to control the total power deliver out from the PVAE. Inverter is used to invert the DC voltage to AC voltage, the reason use inverter because on the gird network is using AC power. Inverter need requires a PWM waveform to perform the invert performance. To generate the AC power that able to supply into the grid network, it is required the PWM signal who able to connect with grid network and frequency must be same as $50H_Z$. To achieve this task, grid phase information is provided and adds with the phase angle that setting by user. This phase angle can adjust and affect the output power performance of PVAE. After add in phase signal, the signal need to transfer to sine wave which magnitude 0.8 and frequency $50H_Z$. Then it will compare with triangle waveform and deliver the PWM

signal. Sine wave acts as the DC level for the comparison. In this project, I am going to design a PVAE that able to connect with the grid network by using simulation.



3.3 **PV Inverter**

Figure 3.2: single-phase photovoltaic inverter

Figure 3.2 show as a single phase photovoltaic inverter, it is modeled in the distribution network by using PSCAD program. PV inverter is installed at any of the three phases in the customer's premises. The inverter circuit is using four gate-turn-off (GTO) thyristor to perform a H-bridge inverter. GTO is control by the PWM signal which is generate by compare between the triangle waveform and sine waveform. The inverter is connected to one of the three phases, before connect with the grid network, it is have a coupling circuit consisting of a resistor and inductor, this is to make sure the voltage of PV is 239.6*V*.

3.3.1 DC Source

A DC voltage, such as battery, outputs a constant voltage over time. DC is the unidirectional flow of electric charge. In this project, a DC supply is used as the sources of PVAE and also is the control power output of the PVAE. The figure below show as the DC sources for PVAE in PSCAD.

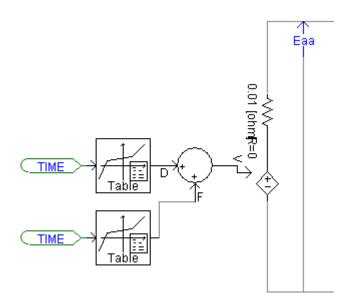


Figure 3.3 shown as the voltage and control in PSCAD

From the figure above, DC sources is set as external input method, so it can be decided how much voltage that be generate from DC battery. Two lookup tables are used to give the control signal for the DC battery. The lookup table value is show as below.

Time		Time	
<i>(s)</i>	Output	<i>(s)</i>	Output
0.50	0.00	5.0	2.00
1.00	0.25	5.5	1.75
1.50	0.50	6.0	1.50
2.00	0.75	6.5	1.25
2.50	1.00	7.0	1.00
3.00	1.25	7.5	0.75
3.50	1.50	8.0	0.50
4.00	1.75	8.5	0.25
4.50	2.00	9.0	0.00

Table 3.1: Lookup table Value

For the DC sources for the PSCAD, when it is setting as external input method, signal 1 is will generated 2500V from the DC sources.

3.3.2 Inverter

In order to generate AC voltage from DC voltage, it can use electronic switches to reverse the polarity of the electricity supplied to the load periodically. In this project, an H-bridge circuit is required to generate the DC to AC voltage, figure 3.4 shows as an H-bridge inverter that build in PSCAD.

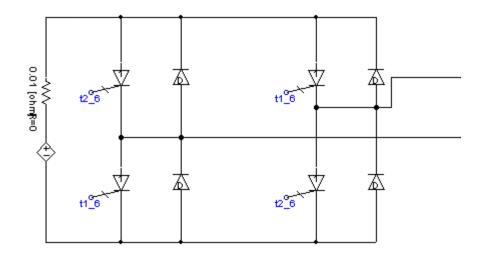
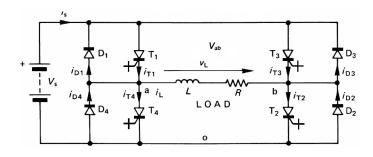


Figure 3.4 shown as an H-bridge inverter circuit

From the figure 3.4, four thyristor GTO is requires for this H-bridge circuit. Gate turn-off (GTO) is a type of thyristor, a high-power semiconductor device, it is a fully controllable switches which can be turned on and off by their gate. It can be turned on by a gate signal and can also be turned off by a gate signal of negative polarity. The turned on and turned off time of the GTO is very important because it have to generated the sine wave power by PWM.

To perform invert DC to AC power, the four switches in H-bridge, which are T_{1_6} , T_{2_6} . In order to generate a square wave in first one half cycles, closing the T_{2_6} , open another two which is T_{1_6} . To generate the next half cycles, closing the T_{1_6} , open the T_{2_6} . Both conditions are show as below.



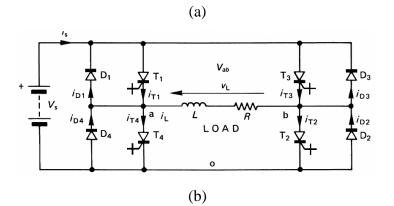


Figure 3.5: Operation of H-bridge

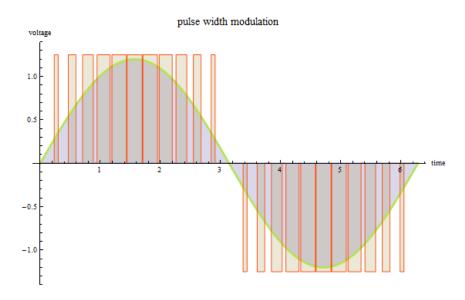


Figure 3.6 shown as Pulse Width Modulations

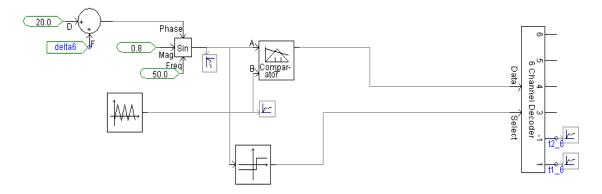


Figure 3.7 shown as PWM generator in PSCAD

From the figure 3.7, delta 6 is the phase from grid network. 20° is the phase that controllable by the user to affect the output power from PVAE. After adding two phase, it will send to sine wave generator to generate a sine wave based on 0.8 amplitude, 50 Hz and the phase that user selected. After that, it will compare this sine wave signal with the triangle signal to get the PWM signal. Single input comparator is help decoder select which switch have to open and close. PWM signal is also send though decoder to control the switch to invert DC power to AC power.

3.4.1 Phase Angle

Phase in waves is the fraction of a wave cycle which has elapsed relative to an arbitrary point. In this part, there have two types of phase is generated. First phase is the phase of gird network, which is generated by grid system. The second phase is the phase set by user; this phase can be effect the output power of the PVAE. For example, take a look at figure 3.7. The upper side plot shows a 1 kHz sine wave starting with a phase of 0 radians. The peak amplitude is 1V. The middle side plot shows as add one period of 1 kHz sine wave starting with a phase of 45 °. Peak amplitude also is 1V. If these two wave are add together, the result shown on the bottom, is one period of 1 kHz sine wave with a different peak amplitude and starting phase. When two phases add together and get a increasing amplitude, it is means the PVAE can be injected power into the grid

system. If after two phases add together and get decreasing amplitude, it is means the PVAE will start inject back the power from grid system.

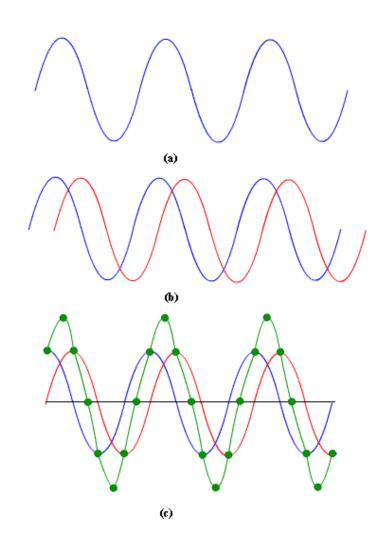


Figure 3.8 shown as the add two phase

3.4.2 PWM Signal

PWM stands for pulse width modulation. It is a powerful technique to control analog circuit with a processor's digital outputs, such as microcontroller. A simple PWM generator can be made by using triangle wave generator together with an analog

comparator. The magnitude of the triangle wave is compare with the sine wave. The figure 3.8 is show as the sine sawtooth PWM.

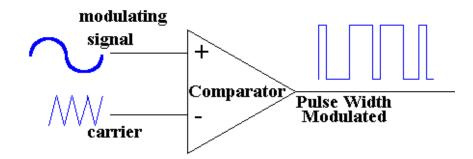


Figure 3.9 shown as sine sawtooth PWM

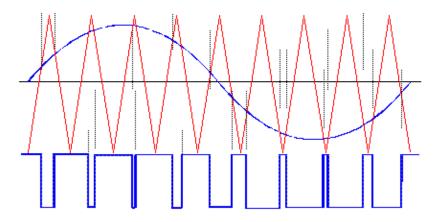


Figure 3.10 shown as PWM generator

3.4.3 Load

Beside simulate a PVAE; in this project also have simulated the relationship between PV and load in each phase. Load will affects the performance of circuits that output current and voltage.

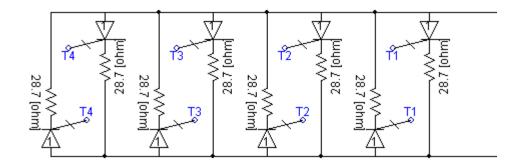


Figure 3.11 shown as the variable load

When no load, which is open circuit terminals, all of the current cannot be across to the output, so Vout is equal with Vs and current equal to zero. However, when put the load resistance, this load will makes a closed circuit and allows current to flow. So the value of power across the load will be change. Voltage drop across load resistance, so in the result, voltage output terminal is not same as Voltage input. The output voltage can be determined by the voltage division rule:

$$V_{OUT} = V_S \times \frac{R_L}{R_L + R_S} \qquad -(4)$$

The power taken by the load is:

$$P = \frac{V_{OUT}^2}{R_L} \qquad -(5)$$

The reason use bidirectional of load because of the power at grid network is sine wave, but the GTO only can accept one direction waveform, so it is requires have two direction of GTO to complete this task. The figure show as below is the idea of load circuit.

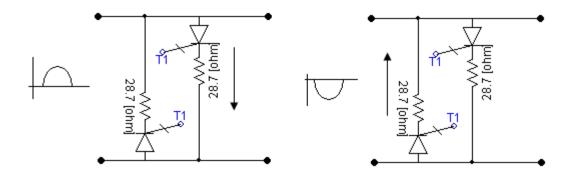


Figure 3.12 shown as the how the load work at sine wave

By using figure 3.12, the power can be always passing though the same value of resistor. If not, the power can pass though will be decrease half base on half cycle current cannot pass though of the load.

In this variable load, all the resistor value have been same, the reason of this is because if use many different value of resistor, user may confuse. Besides that, it is also because of the capability of resistor, when the total amount of power passes though the resistor is very large power. The price of resistor will be very expensive. So in order to solve this problem, the way that use in this project is build a parallel resistor, this way can be separate the power passes though each resistor when total amount of power is very high. For example, has two case of testing, first case is a resistor value 14.35 Ω , another is case is two resistor with value 28.7 Ω . The power passes through 4kW. In first case, the total power pass though of the resistor is 4kW, For the second case, two resistors total handle 4kW power, means each resistor just handle 2KW power. The price of the resistor is based on the total amount of power. It will be increase the price when the resistor need handle more power.

CHAPTER 4

RESULT AND DISCUSSION

4.1 Introduction

This chapter presents the results of the implemented project "Photovoltaic Array Emulator" and also discussions regarding the testing. The purpose of performing tests on the implemented project is to test whether the project is working correctly, and the results are achieving the objectives as stated in the first chapter.

The simulation result is tested on PSCAD program. The testing conditions are separated into two, Photovoltaic Array Emulator and Relation between PV and Load. On the first part of testing, it is help to choose which solution can be use to perform a photovoltaic array emulator. The second part of testing is to understand the relationship between PV and load and how they affect the voltage unbalance.

4.2 Photovoltaic Array Emulator

In this project, I have tried many testing on it. First, to generate the PV output, I have test to change the input voltage and also try for the phase angle. Both of them also can affect the output power of the PV.

4.2.1 Phase Angle

For PWM generator, phase angle is very important. Phase angle can be affect to the power output of PV. The input voltage is set as 550V and changing the phase angle from 0° to +360°. The output power of PV is shown as below.

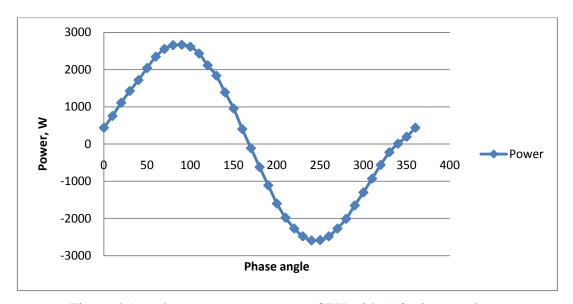


Figure 4.1 as shown as output power of PV with 550V input voltage

According to the graph above, we can see that when the phase is 90°, the output power is reach to maximum and when phase -270°, the output power is decrease to minimum. When the phase angle change to 90°, the power that deliver out from the PV is maximum which is about 2667*W*, when the angle is continue increase, the output power will be start drop down until reach the minimum point which is -2270W. The output is show as a sine wave form. However the phase of maximum point and minimum point will be slightly change if the input voltage is change to too big or too small. For example, when the input power is change to 5500*V*, the maximum point of output power will be at 60° and minimum point at -240°, besides that, maximum power is 34950*W* and minimum power is appeal when the input voltage is high. The graph of 5500*V* input power is show as below.

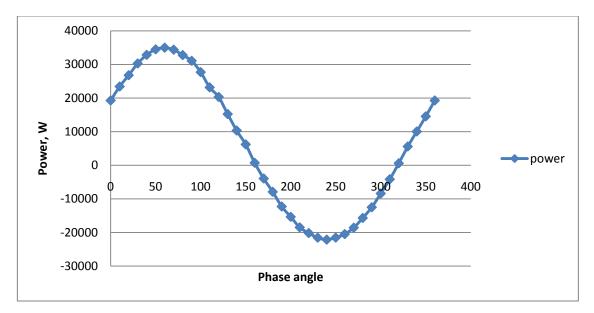


Figure 4.2 shown as output power of PV with 5500V input voltage

4.2.2 Input Voltage

The DC input of PV is the main sources of photovoltaic array emulator. Besides that, DC input also can act as battery in simulation. Changing the value of DC input can direct affect the output power of PVAE. In this case, the difference input voltage will give how much of the impact to the output power will be tested, which is show as a dynamic input voltage and fix phase.

The phase angle of first case is set as 0° and second case of phase angle is set as 50°, input voltage will change according to the time, which is the table 4.1 as shown as below.

Time, (s)	Vin (V)
0	0
0.5	2625
1	6250
1.5	10625
2	12500
2.5	12000
3	6750
3.5	5000
4	3625
4.5	1875

Table 4.1: The time and Vin.

The result of output power is show as below; figure 4.3 is shown as the comparison between phases is set as 0° and phase is set as 50° .

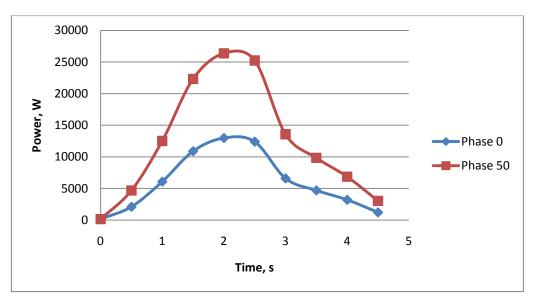


Figure 4.3 shown as comparison between phase 0 ° and phase 50 ° output power.

From the figure 4.3, the different input voltage will direct change the output power. Besides that, the phase also will affect the output power. Just like the previous

testing, the output power of PV at phase 50 $^\circ$ is higher than the output power at PV at phase 0 $^\circ$.

4.2.3 Select the Method of using for Photovoltaic Array Emulator.

When tested above two tests which are the phase angle of PV and input voltage of PV, now it is ready to generate the output of PV which is similar as the real PV output. At this part, two methods of simulation will be use to generate the PV output, which is changing the phase angle and changing the input voltage. Both of the methods only generate the output power which is following the shape of real PV output power. Figure of Real PV output power as shown as below.

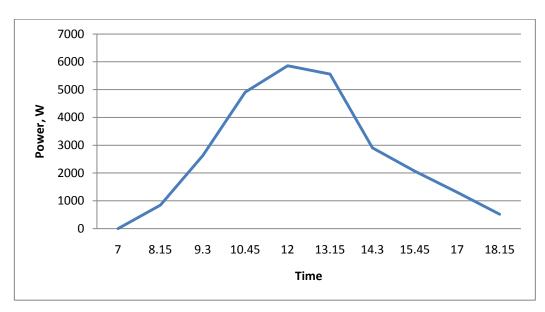


Figure 4.4 shown as power output of real PV.

1. Phase angle

In this method, to generate PV output as changing the phase angle, the input voltage of PV is fixed, set as 550V, the result is shown as below.

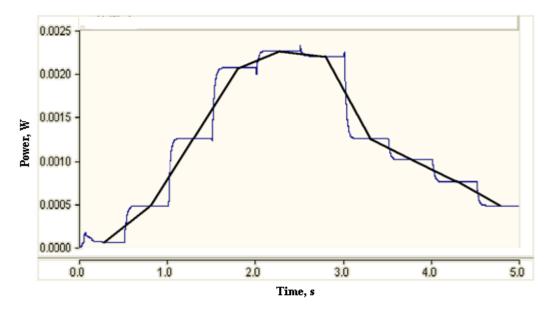


Figure 4.5 shown as output power of phase change.

Time in simulation	Real	Phase	
(s)	time	()	Output power (W)
0	7	-20	30.9
0.5	8.15	0	450
1	9.3	30	1304
1.5	10.45	60	2098
2	12	90	2250
2.5	13.15	70	2180
3	14.3	30	1304
3.5	15.45	20	1030
4	17	10	786
4.5	18.15	0	450

Table 4.2: The power generate by change Phase angle.

From the result, the shape of output power for PV is same as the real PV output power; however, the maximum output power of this case is only 2250W. This is because have a limitation of phase angle changing. From the previous testing, it is show out one of the information which is the maximum output

power can be deliver out from the PV by using different phase angle is 90°. The main reason that this method is not considered is because of above limitation.

2. Input Voltage

Under this method, it is generate the PV output power by using changing input voltage. In this part, phase angle of PV is fixed which is set as 0° . The result is shown as below.

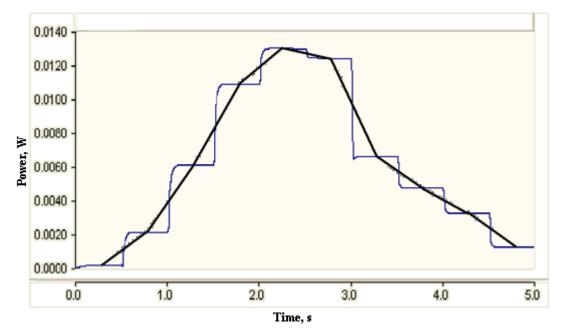


Figure 4.6 shown as output power of voltage change.

Time in simulation	Real		
(s)	time	Vin (V)	Output power (W)
0	7	0	133
0.5	8.15	2625	2092
1	9.3	6250	6063
1.5	10.45	10625	10881
2	12	12500	12966
2.5	13.15	12000	12389
3	14.3	6750	6583
3.5	15.45	5000	4686
4	17	3625	3194
4.5	18.15	1875	1211

Table 4.3: The power generate by change input voltage.

From the result, the shape of output power of PV is similar with the real PV output power. On this case, there is no limitation for the maximum output power. When the input voltage is higher, the output that can be delivering out also can be higher. This method is selected to use because of easy to control and no limitation of maximum power that can be delivered out.

4.2.4 Simulation of Photovoltaic Array Emulator

From the previous testing, the second method is confirmed be use which is changing input voltage to control and generate the PVAE output power. The data of PVAE generated is show as below.

DC input (V)	AC output (W)
0	145
250	110
500	851
750	2072
1000	3242
1250	4376
1500	5492
1750	6596
2000	7697

DC input (V) AC output (W)

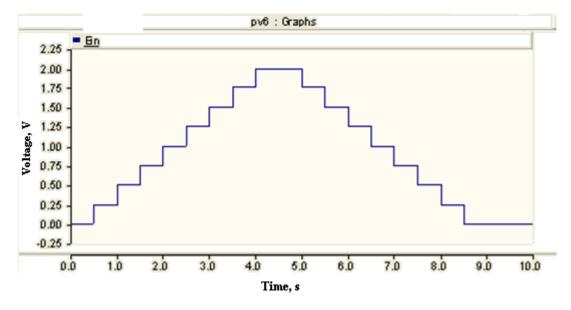


Figure 4.7 shown as DC input

Table 4.4 PVAE input voltage and output power

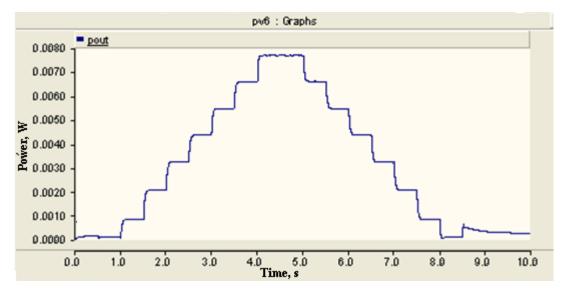


Figure 4.8 shown as PVAE output.

From the figure 4.8 and table 4.4 that show as above, the voltage input is change 250V per 0.5 second. This output consider by real PV output power. For the real PV output power, the power will start increasing from morning until noon. When noon, the output power should be reach the maximum if do not have any other weather condition. The maximum output condition should be remaining between 12pm to 2pm. After that, the output power should be start drop until the sunlight is fully disappearing. So, from the result, PVAE is show out the result that similar with the real PV output. The output power will keep increasing until reach the maximum which is the time at 4 second. After reach maximum point, it will stay at the maximum value until the time at 5 second, then it only will start drop down until time at 8.5 second. The table as below can be explaining more clearly about the time of simulation vs real time.

Time in simulation		
(s)	Time in day	Output Power (W)
0.0	7.06 am	145
0.5	7.48 am	110
1.0	8.30 am	851
1.5	9.12 am	2072
2.0	9.54 am	3242
2.5	10.36 am	4376
3.0	11.18 am	5492
3.5	12.00 pm	6596
4.0	12.42 pm	7697
4.5	1.24 pm	7697
5.0	2.06 pm	6596
5.5	2.48 pm	5492
6.0	3.30 pm	4376
6.5	4.12 pm	3242
7.0	4.54 pm	2072
7.5	5.36 pm	851
8.0	6.18pm	110
8.5	7.00 pm	228

Table 4.5: Time simulation vs real time

4.2.5 Comparison of the Simulation Result and Laboratory Result

The Grid-tied PV is used device that is Grid PV Inverter Sunteams 1500. There has some limitation for this device. Input DC voltage must between 100V to 450 V, and maximum output AC power is1650W. When the input DC voltage is small than 150V, the inverter will auto come to standby mode, because of this limitation, to make sure the inverter is operation, the input voltage must greater than 150V. Car battery is used on this part as the input voltage of PV inverter, total number of car battery that use for this

project is 15 pcs. 15 pcs car battery is the maximum batter that can be use for this project because out of the battery.

Number of car		
battery	Input Voltage, V	Output Power, W
12	151	1180
13	164.4	1270
14	176.3	1377
15	185.8	1472

Table 4.6: Output power from PV inverter

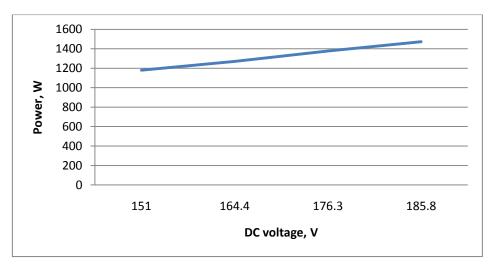


Figure 4.9: Output Power vs Input Voltage for the PV inverter

Minimum of 12 pcs car battery are used for this project, this is because of the limitation for the PV inverter. When the car battery is less than 12 pcs, the Voltage will be less than 150V, which will make PV inverter under standby mode. The maximum of car battery that use for this project is 15 pcs due to the number of battery that we have. Each car battery can supply about 12V. From the result, when 12 pcs of car battery is used, output power that can deliver out from the PV inverter is about 1180W. Because 12 pcs car battery is only provide a DC voltage 151V. So we can probably know that the minimum power generate by PV inverter is about 1180W. When increase 1 more car battery for the system, the output power is increase about 100W until the maximum

number of car battery which is 15pcs, the output power is about 1472*W*. The result is same as the simulation, when increase the input voltage, the output power will be increase. Figure 4.10 shown as the switch for the PV inverter that we build out, and figure 4.11 shown as the circuit design of switch for PV inverter.



Figure 4.10 shown as switch for the PV inverter

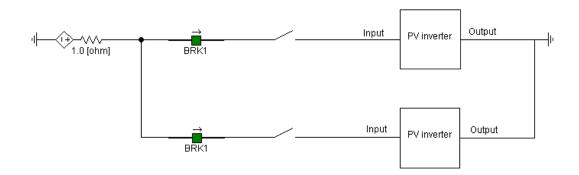


Figure 4.11 shown as the circuit design of switch for PV inverter

4.3 Relation between PV and Load

PV will increase the voltage unbalance for the grid network, the reason of that is because when installing the PV in the network, PV will change the voltage profile in the network, causing the three phase system voltage profile amplitudes to differ more from each other and hence a high voltage unbalance. In this paper, an analysis has been carried out to investigate how PV installations, their location and power generation capacity can cause of voltage unbalance increasing.

$$\operatorname{VUF}(\%) = \frac{V^{-}}{V^{+}} \times 100 \tag{6}$$

4.3.1 Load

Total have three types of load conditions have been tested. First is balanced load, second is unbalanced load, and third is variable load. In balanced load conditions, load for the three phase system is set as same value, which is from 0W load to 10kW load. For unbalanced load, load for the three phase system is set as different value.

1. Balanced load

From this case, no PV is connect to the load, the percents of voltage unbalance is get zero for each condition, means that in each of the conditions, the current taken from each side of the system is equal and the power factors also as equal.

Phase A	Phase B	Phase C	
(<i>W</i>)	(<i>W</i>)	(<i>W</i>)	%VUF
0	0	0	0
2000	2000	2000	0
4000	4000	4000	0
6000	6000	6000	0
8000	8000	8000	0
10000	10000	10000	0

Table 4.7: Balanced load

2. Unbalanced load

Beside simulate for the balanced load, unbalanced load also be tested. The reason to test the unbalanced load is want to more understand about the load at each phase will give how much effect of the whole system. There have two type conditions have been tested for unbalanced load, which is unbalanced load at phase A, the second condition of unbalanced load is three phase with different load. The result is shown as below.

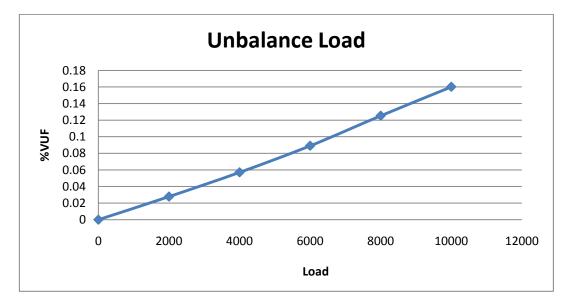


Figure 4.12 shown as the voltage unbalance for the unbalance load at phase A.

When unbalance load at phase A, voltage unbalance will keep increasing. That is because the current taken from each side is difference.

Phase A	Phase B	Phase C	
(W)	(<i>W</i>)	(<i>W</i>)	%VUF
0	2000	4000	0.045940528
0	4000	6000	0.068235622
0	6000	8000	0.100296711
0	8000	10000	0.133773672
0	10000	10000	0.15052055
2000	10000	4000	0.115616599

Table 4.8: Three phase with unbalance load

From the table 4.8, when the value of load for each phase is bigger different, the voltage unbalance will become bigger, if the different is small, then the voltage unbalance become smaller.

3. Variable load

In this case, values of load have been change due to the time change. To generate a 2kW load, based on the equation,

$$P = \frac{V^2}{R} - (7)$$

$$2000 = \frac{239.6^2}{R}$$

$$R = \frac{239.6^2}{2000}$$

$$R = 28.7\Omega$$

To get the second value of load, this is 4kW, the way that use in this project is parallel two 28.7 Ω resistors.

$$R_{T} = R_{1} \parallel R_{2} - (8)$$

$$R_{T} = \left[\frac{1}{28.7} + \frac{1}{28.7}\right]^{-1}$$

$$R_{T} = 14.35\Omega$$

$$P = \frac{239.6^{2}}{14.35}$$

$$P = 4000W$$

Table 4.9: The load power

Time, s	Load, Ω	Power, W
0	infinite	0
1	28.7	2000
2	14.35	3995
3	9.57	5984
4	7.175	7967
5	9.57	5984
6	14.35	3995
7	28.7	2000
8	infinite	0

4.4 Photovoltaic Array Connect with Load

In this part, the PV will be connect to the single phase load, four types of methods will be tested in this part, which is fixed PV with fixed load, variable PV with load, fixed PV with variable load and variable PV with variable load.

4.4.1 Fixed PV with fixed load

In this method, the PV output is fixed as 4 types, which are 2072*W*, 4151*W*, 5491*W* and 7035*W*. Each types of PV output will be test for the balanced load, unbalanced load.

1. Balanced load

From the result, the voltage unbalanced did not change much when increase the load. That is because from the previous testing, it is show the voltage unbalance for balance load is zero. So the voltage unbalance from this figure 4.3 is because of PV. The current pass though each phase will become bigger different when PV output power is increase. This is the reason show that voltage unbalance is high when PV output power is 7035*W*. When the PV output power is small, which is 2072*W*, the percents of voltage unbalance is small. When the PV output power is reach to 7035*W*, the percents of voltage unbalance is large. It is also prove as the hardware device. The figure below show as voltage unbalance of PV inverter for the simulation result and laboratory result when connect with balanced load.

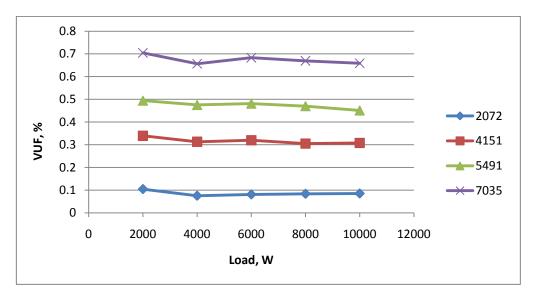


Figure 4.13 shown as VUF vs Load for PV connect with balance load

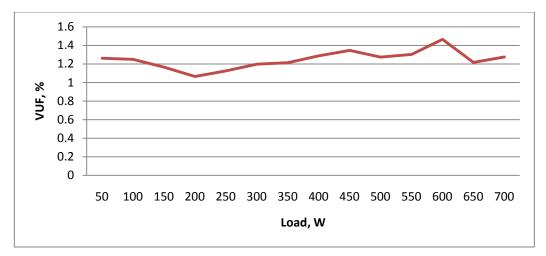


Figure 4.14 shown as VUF vs load for PV inverter

2. Unbalance load

In this case, unbalance load will separate to two sections. First section is PV connect with same phase of unbalance load, second section is PV connect with different phase of load.

Under this section, PV is connecting at phase A and unbalance load also connect at phase A, other two phase set as 0W load. Figure below show as PV connect with same phase of unbalanced load

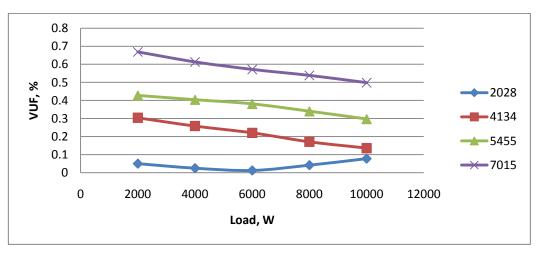


Figure 4.15 shown as VUF vs load for PV connect at same phase of unbalance load

From the result, the voltage unbalance is decrease when the load is increase. In this case, when the load is increase, mean it will requires more power and make the three phase system unbalance, but when PV is connect on the same phase, the PV output power will cover the power that load requires from the system, to make the voltage unbalance of three phase decrease. This result also proves by the hardware PV inverter, when PV inverter and load is connecting at the same phase, the voltage unbalance is decrease.

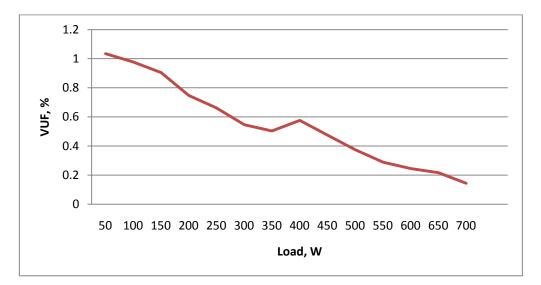


Figure 4.16 shown as VUF vs load for same phase with PV

In this part, PV is connecting at A and unbalance load is connecting at phase B and phase C. Figure show as below is PV connect with different phase of unbalance load

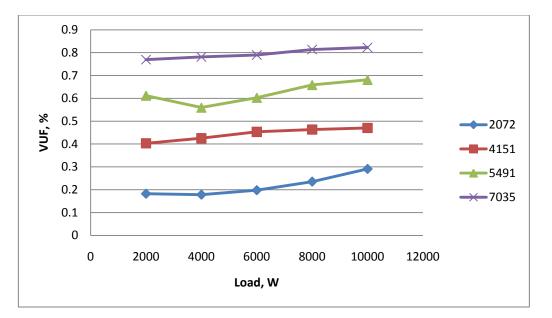


Figure 4.17 shown as VUF vs load for PV connect to different phase of unbalance load

From the result, voltage unbalance is increasing by increase load. The reason of voltage unbalance increase is because two reason, first reason is when the load increase, it will requires more power from the network, this will make the voltage unbalance increase. Second reason is when the PV supply is increase, it will inject more power to the system, and it will also make the three phase system more unstable and voltage unbalance increasing. This result also prove by using PV inverter connect with the different phase of unbalanced load. The result is show as below.

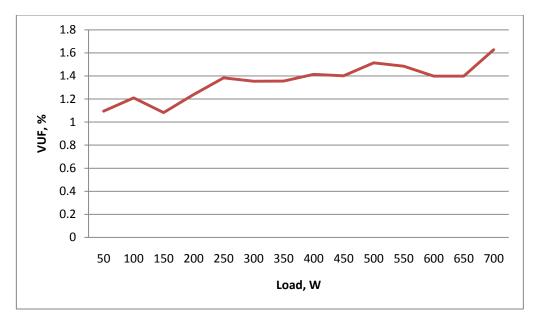


Figure 4.18 shown as VUF vs load for different phase with PV.

4.4.2 Variable PV with fixed load

In this part, the variable PV output power is show as figure 4.8; load is set as 2kW, 4kW, 6kW, 8kW and 10kW. The test is same as previous, which will separate in two sections, which is balance load and unbalance load.

1. Balanced load

From this result, the voltage unbalance will start drop at the beginning until 0.5 second, after that it will increase to maximum which is about 2 and 2.5 second. When reach the maximum point, it will start drop back until 3.75second then only increase back. The reason of front part and behind part is high because when PV output power is zero, the power will be inject into PV system and it will make the voltage unbalance increase. Same as the previous testing, the balanced load will not make voltage unbalance increase; the reason of voltage unbalance increase on this case is the PV output power increase. The PV output power injects into the network and makes the current of each phase unstable. The result is making the voltage unbalance increase. The result is shown as below.

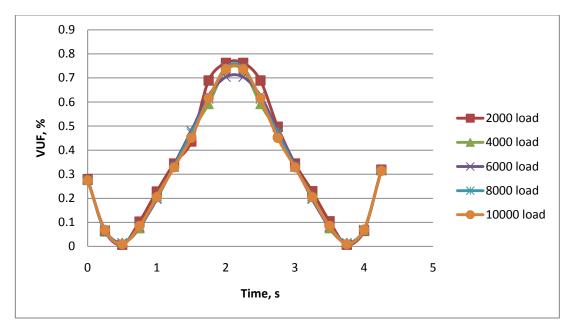


Figure 4.19 shown as VUF vs time for PV connect with balance load

2. Unbalance load

Two different conditions of unbalance load will be test on this situation, which is variable PV connecting with the same phase of unbalance load and variable PV connecting with the different phase of unbalance load.

Variable PV is connecting at phase A, and the unbalance load is also providing at phase A. The figure show as below is PV connects with same phase of unbalance load.

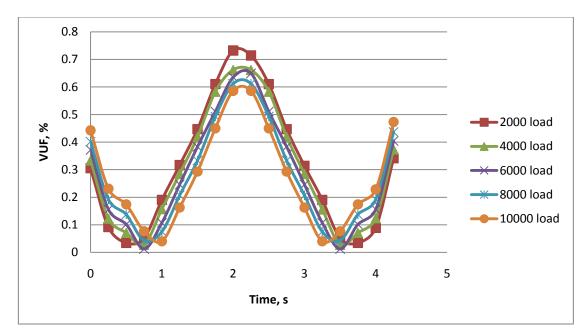


Figure 4.20 shown as VUF vs time for PV connect at same phase of unbalance load

From the figure 4.20, voltage unbalance is lower than the PV connecting with balanced load. At the front part, 2kW load will have a lower voltage unbalanced and 10kW load will have a higher voltage unbalanced because of the power requires for the difference load value. At 2kW load, power requires from the system is most lower, that is the reason it can get the lower voltage unbalanced. For 10kW load, the power requires from the system is higher, so it will make the system more unstable than 2kW load. However, when the time is increase, the output power of PV will be increase, it will make the voltage unbalance at 10kW lower than 2kW load at overall graph. The reason of that result is because when PV provides more power to network, the load can direct get the power from PV and less requires from network.

Under this situation, the variable PV is connecting at phase A. Unbalance load connecting at phase B and phase C. The figure show as below is PV connects with different phase of unbalance load.

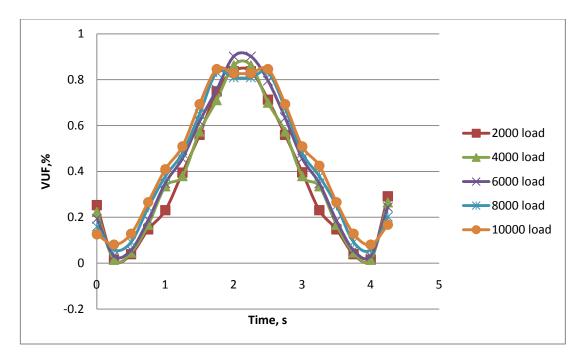


Figure 4.21 show as VUF vs time for the variable PV and different phase of unbalance load.

In this result, the overall value of voltage unbalanced is higher than previous two conditions which balanced load and same phase with unbalanced load. This is because two reason of making increase voltage unbalance also occurs together. First reason is unbalance load and second reason is PV supply. The unbalance load at phase B and phase C will make current pass though each phase becomes more difference. When the PV supply to network, it will also make the three phase network more unstable and increase the voltage unbalance.

4.2.3 Fixed PV and variable load

In this case, PV output power is fixed as 4 values which are 2072W, 4151W, 5491W and 7035W. Variable load is set as start from 0W load until 8kW load in time 4.5second, every 0.5second increase 2kW until time 2second reach the maximum and decrease 2kW every 0.5second after time 2.5second. Same as the previous test, it will separate into two parts which is balanced load and unbalanced load.

1. Balanced load

For balanced load, the three phase load also set as variable load to increase load power in the same time. The result is show as below.

From the figure below, the voltage unbalance is not much change for each type of value of PV. The reason to get this result is because under balanced load, the voltage unbalance is very less, near to zero. The only effect voltage unbalance for this simulation is PV output power, when output power more high, the voltage unbalance more high.

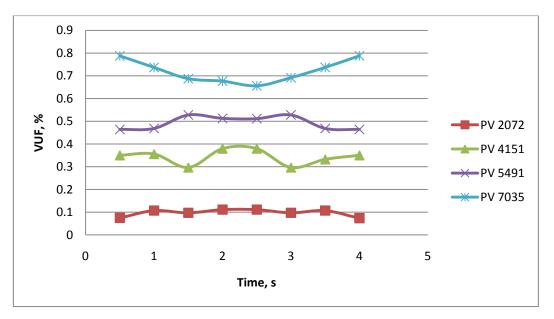


Figure 4.22 shown as VUF vs time in balanced variable load

2. Unbalance load

For unbalance load part, same as previous testing, it will separate in two parts which is PV connecting with the same phase of unbalance load and PV connecting to the difference phase of unbalanced load.

Under this situation, PV is connecting at phase A and unbalance variable load is also connecting at phase A. Figure 4.23 show as PV connect with the same phase of unbalance load

From the result shown as below, the voltage unbalance will be decrease when the time is increase until the time 2.5 second, then it will increase back until time 4 second. The reason of this result is because when the time is increase, the value of load will be increase, this will make the voltage unbalance drop due to the PV connect with the same phase of load. After time 2.5 second, the voltage unbalance will start increase back because the load will be decrease after that time. When the load is increase at the same phase of PV supply, the power requires from the load will be decrease due to the power is receive by PV.

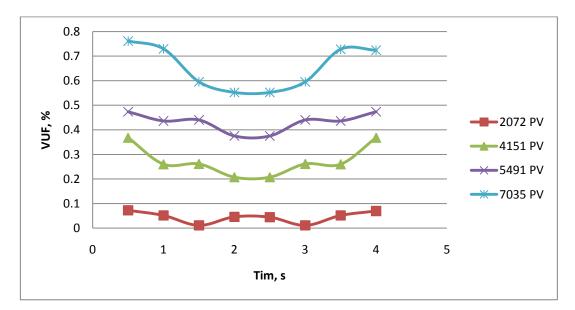


Figure 4.23 shown as VUF vs time with PV connect with same phase unstable variable load

Under this situation, PV is connecting at the phase A and unbalanced variable load is connecting at phase B and phase C. Figure 4.24 shown as below is PV connects with the difference phase of unbalance load.

From the figure show as above, the overall value of voltage unbalance is higher. The reason of high voltage unbalance is difference phase of PV supply and variable load. When the PV supply more power to network, the distance between three phase of current pass though will become bigger. When the time is increase, the power requires for the load also increase based on the value of load is increase. This will also increase the voltage unbalance for the system.

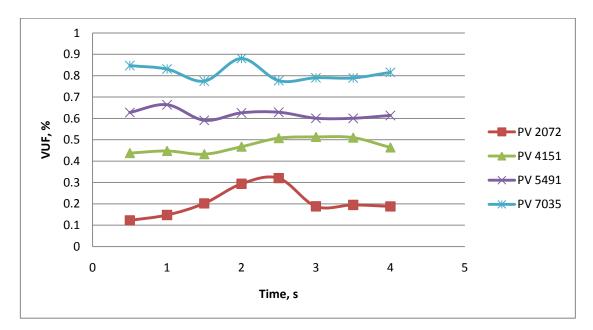


Figure 4.24 shown as VUF vs time with PV connect with difference phase unstable variable load

4.2.4 Variable PV and variable load

Under this case, both of the PV and load also will change during the time difference. The variable PV is act as real PV, change the power output during time. The variable load is act as real commercial network, change the load power requires during time. It will test three types of conditions which is balanced load, unbalanced load with same phase and unbalanced load at difference phase. The result is show as below.

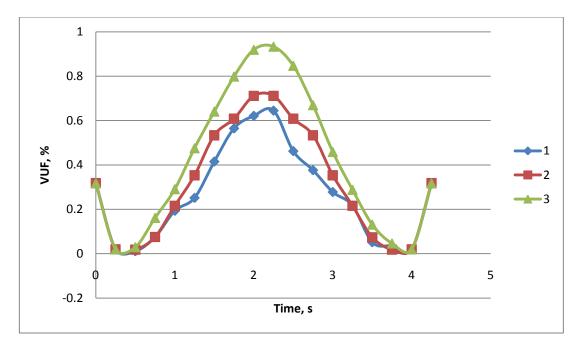


Figure 4.25 shown as VUF vs time

From the figure above, 1 is show as unbalance load with same phase, 2 is show as balanced load, 3 is show as unbalance load with different phase. The higher value of voltage unbalance is when unbalance load with different phase and lower value of voltage unbalance is when unbalancing load with same phase.

4.5 Conclusion

In conclusion, the proposed "Photovoltaic Array Emulator" is tested and a lot of testing is presented in this chapter. From the result, photovoltaic array emulator is more suitable control by using DC input voltage. However, when using software simulation, idea case will not give any limitation of the output power of PVAE. But when using hardware to operate PV inverter, there will have limitation for the input voltage and output power. Besides that, PV is more suitable connect to the load which will have high load requires at the day time.

CHAPTER 5

CONCLUSION AND RECOMMENDATION

5.1 Introduction

In this chapter, an overall conclusion of the proposed system "Photovoltaic Array Emulator" will be made. This chapter will give a summary of all the previous chapters; briefly discuss the proposed project's challenges, objectives; the literature reviews on several related journal and conference papers; system design; all the testing data characteristics and lastly, the result of proposed system. Beside all the contents mentioned above, this chapter will also state the recommendation of the simulation photovoltaic array emulator.

The "Photovoltaic Array Emulator" is proposed based on the facts that electrical demand of Malaysia is keep increasing every \year and the main energy source use for Malaysia is non renewable source. To prevent energy crisis happen in Malaysia, Malaysia government is strengthening the role of renewable energy as the fifth cornerstone of energy generation. PVAE are the system who able to represent electrically similar with the PV arrays but without depending on the weather conditions and capable to emulate PV array systems. That can make a possible to perform difference PV energy production system test under many situation.

Some reviews had been done on the field related to Photovoltaic Array Emulator. Five papers are studied and each of them proposed some methods with certain key features for PVAE system. The purpose of reviewing previous work is to give a better idea on how on implement the similar system.

The PVAE can be separate in several parts; all part should be combining together at the last to perform the electrically similar with the PV arrays. First part is DC battery part, in simulation, the value of battery should be controllable for decided the output power from the PVAE. After that it is requires an inverter to invert the DC power to AC power, the inverter of this project is use H-bridge inverter. The switch of inverter is control by PWM signal generator, which is compare between sine wave and triangle wave. The sine wave is generated by phase of grid network and triangle wave is generated by a triangle signal generator.

In the system development period, unit testing is performance on each individual module. The tests took place in two parts, which is PVAE and PVAE connect with grid network. This is to make sure the system can be fully use and functions correctly. However, after testing, from the result, power output from the PVAE can be adjust though DC voltage sources and the phase angle set for the PWM. When PVAE connect with the load, it is more suitable use for the load at the same phase, the voltage unbalance will be less if comparing with the load not same phase with PVAE.

In conclusion, PVAE simulation result is proposed. There are many scenarios that may cause the high voltage unbalance. In this project, only some scenario are consider, where in the case PV and Load in the same phase, when load increase, the voltage unbalance drop, for other the case of balanced load, the voltage unbalance will maintain at same position for the balance load, cannot be decrease. Most bad condition is unbalance load with PV connect in difference phase with load, this case will increase the voltage unbalance. From the result and comparison, it can be say most best location for the PV is use for the commercial based on the load higher and PV output higher at the same timing.

5.2 Recommendation

Since the complete PVAE is consist so many parts of device which can became the structure of the proposed system, thus improvements from any of the part can be increase the overall performance or make it more accurate in the result. The future improvements that can be done as show as follows.

5.2.1 Practical device

In this simulation, all the part of the circuit inside PVAE is using the idea case device. It does not consider any environment condition, device limitation and so on. So the result of simulation will be difference with the practical result. The component use in simulation also not consider on price, so it is hard to calculate how much cost requires if build out. The result of this part is improving the simulation more near with the real practical result.

5.2.2 Inductance and Capacitance Load

The relation between Load and PV is tested in this project. However, the capacitance load and inductance load is not consider under in testing. Capacitance load and inductance load will affect the power factor. If the power factor is low, it will also affect the voltage unbalance for the whole network system. It can be more complete for the PVAE on testing all situations.

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APPENDICES

Balar	nce Lo	ad	Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
0	0	0	239.54	239.54	239.54	239.54	0	0	0	0
2k	2k	2k	239.44	239.44	239.44	239.44	0	0	0	0
4k	4k	4k	239.34	239.34	239.34	239.34	0	0	0	0
6k	6k	6k	239.24	239.24	239.24	239.24	0	0	0	0
8k	8k	8k	239.13	239.13	239.13	239.13	0	0	0	0
10k	10k	10k	239.02	239.02	239.02	239.02	0	0	0	0

Balanced load without PV

Unbalanced load without PV

Unbalano Load	ce		Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
0	0	0	239.54	239.54	239.54	239.54	0	0	0	0
2000	0	0	239.44	239.53	239.55	239.51	0.066667	0.023333	0.043333	0.027835
4000	0	0	239.33	239.52	239.55	239.47	0.136667	0.053333	0.083333	0.057071
6000	0	0	239.22	239.52	239.56	239.43	0.213333	0.086667	0.126667	0.089099
8000	0	0	239.09	239.51	239.57	239.39	0.3	0.12	0.18	0.125319
9999	0	0	238.96	239.5	239.57	239.34	0.383333	0.156667	0.226667	0.16016

Unba	alance	Load	Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
0	2000	4000	239.53	239.46	239.33	239.44	0.09	0.02	0.11	0.045941
0	4000	6000	239.53	239.36	239.21	239.37	0.163333	0.006667	0.156667	0.068236
0	6000	8000	239.53	239.26	239.08	239.29	0.24	0.03	0.21	0.100297
0	8000	9999	239.53	239.16	238.94	239.21	0.32	0.05	0.27	0.133774
0	9999	9999	239.53	239.04	238.94	239.17	0.36	0.13	0.23	0.150521
2000	9999	4000	239.55	239.02	239.32	239.3	0.253333	0.276667	0.023333	0.115617

PV with Balanced load

PV supply = 2072W

Balar	nce Loa	d	Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
0	0	0	239.99	239.58	239.52	239.7	0.293333	0.116667	0.176667	0.122377
2000	2000	2000	239.82	239.49	239.4	239.57	0.25	0.08	0.17	0.104354
4000	4000	4000	239.61	239.36	239.32	239.43	0.18	0.07	0.11	0.075179
6000	6000	6000	239.53	239.25	239.23	239.34	0.193333	0.086667	0.106667	0.080779
8000	8000	8000	239.43	239.13	239.13	239.23	0.2	0.1	0.1	0.083602
9999	9999	9999	239.32	239.02	239.01	239.12	0.203333	0.096667	0.106667	0.085035

PV supply = 4151W

Balar	nce Loa	d	Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
0	0	0	241.8	239.61	239.56	240.32	1.476667	0.713333	0.763333	0.61445
2000	2000	2000	240.67	239.55	239.35	239.86	0.813333	0.306667	0.506667	0.339091
4000	4000	4000	240.45	239.36	239.29	239.7	0.75	0.34	0.41	0.312891
6000	6000	6000	240.4	239.28	239.22	239.63	0.766667	0.353333	0.413333	0.319933
8000	8000	8000	240.22	239.13	239.12	239.49	0.73	0.36	0.37	0.304814
9999	9999	9999	240.12	239.04	238.99	239.38	0.736667	0.343333	0.393333	0.307735

PV supply = 5491W

Balar	ice Loa	d	Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
0	0	0	242.86	239.65	239.6	240.7	2.156667	1.053333	1.103333	0.895985
2000	2000	2000	241.25	239.56	239.38	240.06	1.186667	0.503333	0.683333	0.494314
4000	4000	4000	241.06	239.4	239.3	239.92	1.14	0.52	0.62	0.475158
6000	6000	6000	240.98	239.28	239.22	239.83	1.153333	0.546667	0.606667	0.480903
8000	8000	8000	240.83	239.17	239.11	239.7	1.126667	0.533333	0.593333	0.470025
9999	9999	9999	240.63	239.04	238.98	239.55	1.08	0.51	0.57	0.450845

Balar	nce Loa	d	Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
0	0	0	243.98	239.7	239.64	241.11	2.873333	1.406667	1.466667	1.191727
2000	2000	2000	242.02	239.62	239.34	240.33	1.693333	0.706667	0.986667	0.704597
4000	4000	4000	241.7	239.41	239.26	240.12	1.576667	0.713333	0.863333	0.656607
6000	6000	6000	241.72	239.32	239.2	240.08	1.64	0.76	0.88	0.683106
8000	8000	8000	241.55	239.19	239.09	239.94	1.606667	0.753333	0.853333	0.669603
9999	9999	9999	241.39	239.06	238.98	239.81	1.58	0.75	0.83	0.658855

Unbalanced load with PV at the same phase

PV supply = 2072W

Balance L	oad		Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
0	0	0	240.03	239.55	239.54	239.71	0.323333	0.156667	0.166667	0.134887
2000	0	0	239.72	239.52	239.56	239.6	0.12	0.08	0.04	0.050083
4000	0	0	239.63	239.52	239.56	239.57	0.06	0.05	0.01	0.025045
6000	0	0	239.51	239.52	239.56	239.53	0.02	0.01	0.03	0.012525
8000	0	0	239.39	239.51	239.57	239.49	0.1	0.02	0.08	0.041755
9999	0	0	239.26	239.5	239.58	239.45	0.186667	0.053333	0.133333	0.077958

PV supply = 4151W

Balance L	oad		Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
0	0	0	241.38	239.57	239.56	240.17	1.21	0.6	0.61	0.50381
2000	0	0	240.64	239.53	239.56	239.91	0.73	0.38	0.35	0.304281
4000	0	0	240.47	239.51	239.57	239.85	0.62	0.34	0.28	0.258495
6000	0	0	240.35	239.53	239.58	239.82	0.53	0.29	0.24	0.220999
8000	0	0	240.16	239.51	239.58	239.75	0.41	0.24	0.17	0.171011
9999	0	0	240.03	239.5	239.58	239.7	0.326667	0.203333	0.123333	0.13628

PV supply = 5491W

Balance L	oad		Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
0	0	0	241.69	239.62	239.49	240.27	1.423333	0.646667	0.776667	0.592397
2000	0	0	241.09	239.51	239.59	240.06	1.026667	0.553333	0.473333	0.427665
4000	0	0	240.99	239.5	239.57	240.02	0.97	0.52	0.45	0.404133
6000	0	0	240.93	239.52	239.6	240.02	0.914333	0.495667	0.418667	0.380947
8000	0	0	240.78	239.52	239.59	239.96	0.816667	0.443333	0.373333	0.34033
9999	0	0	240.62	239.51	239.59	239.91	0.713333	0.396667	0.316667	0.297338

Balance L	oad		Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
0	0	0	243.16	239.69	239.49	240.78	2.38	1.09	1.29	0.988454
2000	0	0	241.98	239.54	239.6	240.37	1.606667	0.833333	0.773333	0.668405
4000	0	0	241.79	239.53	239.63	240.32	1.473333	0.786667	0.686667	0.61308
6000	0	0	241.64	239.55	239.61	240.27	1.373333	0.716667	0.656667	0.571587
8000	0	0	241.5	239.53	239.59	240.21	1.293333	0.676667	0.616667	0.538425
9999	0	0	241.35	239.52	239.59	240.15	1.196667	0.633333	0.563333	0.498293

Unbalanced load with PV at the difference phase

PV supply = 2072W

Ba	lance L	oad	Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
0	0	0	239.99	239.58	239.52	239.7	0.293333	0.116667	0.176667	0.122377
0	2000	2000	240.12	239.65	239.28	239.68	0.436667	0.033333	0.403333	0.182185
0	4000	4000	239.99	239.49	239.21	239.56	0.426667	0.073333	0.353333	0.178102
0	6000	6000	239.95	239.46	239.02	239.48	0.473333	0.016667	0.456667	0.197653
0	8000	8000	239.89	239.42	238.81	239.37	0.516667	0.046667	0.563333	0.235337
0	9999	9999	240.06	239.31	238.72	239.36	0.696667	0.053333	0.643333	0.29105

PV supply = 4151W

Ba	lance L	oad	Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
0	0	0	241.8	239.61	239.56	240.32	1.476667	0.713333	0.763333	0.61445
0	2000	2000	240.88	239.68	239.18	239.91	0.966667	0.233333	0.733333	0.402923
0	4000	4000	240.86	239.71	238.95	239.84	1.02	0.13	0.89	0.425284
0	6000	6000	240.82	239.55	238.83	239.73	1.086667	0.183333	0.903333	0.453281
0	8000	8000	240.76	239.48	238.71	239.65	1.11	0.17	0.94	0.463175
0	9999	9999	240.63	239.25	238.63	239.5	1.126667	0.253333	0.873333	0.470418

PV supply = 5491W

Ba	lance L	oad	Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
0	0	0	242.86	239.65	239.6	240.7	2.156667	1.053333	1.103333	0.895985
0	2000	2000	241.67	239.85	239.08	240.2	1.47	0.35	1.12	0.61199
0	4000	4000	241.34	239.7	238.95	240	1.343333	0.296667	1.046667	0.55973
0	6000	6000	241.39	239.63	238.81	239.94	1.446667	0.313333	1.133333	0.60292
0	8000	8000	241.49	239.55	238.69	239.91	1.58	0.36	1.22	0.65858
0	9999	9999	241.44	239.43	238.55	239.81	1.633333	0.376667	1.256667	0.681104

Ва	lance L	oad	Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
0	0	0	243.98	239.7	239.64	241.11	2.873333	1.406667	1.466667	1.191727
0	2000	2000	242.23	239.89	239.02	240.38	1.85	0.49	1.36	0.769615
0	4000	4000	242.14	239.89	238.76	240.26	1.876667	0.373333	1.503333	0.781087
0	6000	6000	242.06	239.72	238.71	240.16	1.896667	0.443333	1.453333	0.78974
0	8000	8000	242.01	239.62	238.54	240.06	1.953333	0.436667	1.516667	0.813697
0	9999	9999	241.89	239.45	238.41	239.92	1.973333	0.466667	1.506667	0.822508

Dynamic PV with balanced load

Load = 0

PV output	Bala	nce l	oad	Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
145	0	0	0	235.52	236.26	236.18	235.9867	0.466667	0.273333	0.193333	0.197751
110	0	0	0	239.51	239.52	239.53	239.52	0.01	2.84E-14	0.01	0.004175
851	0	0	0	239.6	239.51	239.59	239.5667	0.033333	0.056667	0.023333	0.023654
2072	0	0	0	240.07	239.57	239.53	239.7233	0.346667	0.153333	0.193333	0.144611
3242	0	0	0	240.63	239.59	239.51	239.91	0.72	0.32	0.4	0.300113
4376	0	0	0	241.14	239.57	239.5	240.07	1.07	0.5	0.57	0.445703
5492	0	0	0	241.94	239.62	239.55	240.37	1.57	0.75	0.82	0.65316
6596	0	0	0	242.66	239.67	239.51	240.6133	2.046667	0.943333	1.103333	0.850604
7697	0	0	0	243.03	239.62	239.47	240.7067	2.323333	1.086667	1.236667	0.965214
7697	0	0	0	243.03	239.62	239.47	240.7067	2.323333	1.086667	1.236667	0.965214
6596	0	0	0	242.66	239.67	239.51	240.6133	2.046667	0.943333	1.103333	0.850604
5492	0	0	0	242.09	239.63	239.57	240.43	1.66	0.8	0.86	0.69043
4376	0	0	0	241.14	239.57	239.5	240.07	1.07	0.5	0.57	0.445703
3242	0	0	0	240.63	239.59	239.51	239.91	0.72	0.32	0.4	0.300113
2072	0	0	0	240.07	239.57	239.53	239.7233	0.346667	0.153333	0.193333	0.144611
851	0	0	0	239.6	239.51	239.59	239.5667	0.033333	0.056667	0.023333	0.023654
110	0	0	0	239.53	239.54	239.55	239.54	0.01	0	0.01	0.004175
228	0	0	0	238.39	239.53	239.53	239.15	0.76	0.38	0.38	0.317792

PV								Vdev	Vdev		
output	Baland	ce load		Va	Vb	Vc	Vage	а	b	Vdev c	%VUF
				235.1	236.1	236.0					0.27989
145	2000	2000	2000	4	7	9	235.8	0.66	0.37	0.29	8
				239.1	239.4	239.4					0.06267
110	2000	2000	2000	9	2	1	239.34	0.15	0.08	0.07	2
				239.4	239.4	239.4	239.443	0.01333	0.01666	0.00333	0.00696
851	2000	2000	2000	3	6	4	3	3	7	3	1
				239.8			239.573	0.24666	0.07333	0.17333	0.10296
2072	2000	2000	2000	2	239.5	239.4	3	7	3	3	1
				240.2	239.4	239.4	239.723	0.54666	0.27333	0.27333	0.22804
3242	2000	2000	2000	7	5	5	3	7	3	3	1
				240.6	239.4	239.4	239.863	0.82666	0.37333	0.45333	0.34464
4376	2000	2000	2000	9	9	1	3	7	3	3	1
				241.2	239.5	239.8	240.213	1.04666	0.65333	0.39333	0.43572
5492	2000	2000	2000	6	6	2	3	7	3	3	4
				241.9	239.5	239.4	240.333	1.65666	0.74333	0.91333	
6596	2000	2000	2000	9	9	2	3	7	3	3	0.68932
				242.2	239.6	239.3	240.386	1.83333	0.76666	1.06666	
7697	2000	2000	2000	2	2	2	7	3	7	7	0.76266
				242.2	239.6	239.3	240.386	1.83333	0.76666	1.06666	
7697	2000	2000	2000	2	2	2	7	3	7	7	0.76266
				241.9	239.5	239.4	240.333	1.65666	0.74333	0.91333	
6596	2000	2000	2000	9	9	2	3	7	3	3	0.68932
				241.2	239.5	239.3	240.066	1.19333	0.50666	0.68666	0.49708
5492	2000	2000	2000	6	6	8	7	3	7	7	4

1					240.6	239.4	239.4	239.863	0.82666	0.37333	0.45333	0.34464
	4376	2000	2000	2000	9	9	1	3	7	3	3	1
					240.2	239.4	239.4					0.22943
	3242	2000	2000	2000	7	5	4	239.72	0.55	0.27	0.28	4
					239.8	239.4						0.10435
	2072	2000	2000	2000	2	9	239.4	239.57	0.25	0.08	0.17	4
					239.4	239.4	239.4	239.443	0.01333	0.01666	0.00333	0.00696
	851	2000	2000	2000	3	6	4	3	3	7	3	1
					239.2	239.4	239.4	239.363	0.15333	0.07666	0.07666	0.06405
	110	2000	2000	2000	1	4	4	3	3	7	7	9
					238.2	239.4	239.4	239.053	0.76333	0.37666	0.38666	0.31931
	228	2000	2000	2000	9	3	4	3	3	7	7	5

PV								Vdev	Vdev		
output	Baland	ce load		Va	Vb	Vc	Vage	а	b	Vdev c	%VUF
				235.0	236.0	235.9					0.27577
145	4000	4000	4000	5	6	9	235.7	0.65	0.36	0.29	4
				239.0	239.3	239.3					0.06687
110	4000	4000	4000	8	2	2	239.24	0.16	0.08	0.08	8
				239.2	239.3	239.3	239.316	0.03666	0.01333	0.02333	0.01532
851	4000	4000	4000	8	3	4	7	7	3	3	1
				239.6	239.3	239.3					0.07517
2072	4000	4000	4000	1	6	2	239.43	0.18	0.07	0.11	9
				240.0	239.3	239.3					
3242	4000	4000	4000	9	6	2	239.59	0.5	0.23	0.27	0.20869
				240.5	239.3		239.716	0.79333	0.37666	0.41666	0.33094
4376	4000	4000	4000	1	4	239.3	7	3	7	7	6
				241.0							0.47515
5492	4000	4000	4000	6	239.4	239.3	239.92	1.14	0.52	0.62	8
				241.4	239.3						0.59159
6596	4000	4000	4000	5	4	239.3	240.03	1.42	0.69	0.73	3
				241.9	239.4	239.2					0.73263
7697	4000	4000	4000	9	3	7	240.23	1.76	0.8	0.96	1
				241.9	239.4	239.2					0.73263
7697	4000	4000	4000	9	3	7	240.23	1.76	0.8	0.96	1
				241.4	239.3						0.59159
6596	4000	4000	4000	5	4	239.3	240.03	1.42	0.69	0.73	3
				241.0							0.47515
5492	4000	4000	4000	6	239.4	239.3	239.92	1.14	0.52	0.62	8
				240.5	239.3		239.716	0.79333	0.37666	0.41666	0.33094
4376	4000	4000	4000	1	4	239.3	7	3	7	7	6
				240.0	239.3	239.3					
3242	4000	4000	4000	9	6	2	239.59	0.5	0.23	0.27	0.20869
				239.6	239.3	239.3					0.07517
2072	4000	4000	4000	1	6	2	239.43	0.18	0.07	0.11	9
				239.2	239.3	239.3	239.316	0.03666	0.01333	0.02333	0.01532
851	4000	4000	4000	8	3	4	7	7	3	3	1
					239.3	239.3					0.06687
110	4000	4000	4000	239.1	4	4	239.26	0.16	0.08	0.08	3
					239.3	239.3	238.956	0.75666	0.37333	0.38333	0.31665
228	4000	4000	4000	238.2	3	4	7	7	3	3	4

Load = 6000

PV								Vdev	Vdev		
output	Baland	e load		Va	Vb	Vc	Vage	а	b	Vdev c	%VUF
				234.9	235.9	235.8					0.27589
145	6000	6000	6000	5	6	9	235.6	0.65	0.36	0.29	1
				238.9	239.2	239.2	239.133	0.16333	0.07666	0.08666	0.06830
110	6000	6000	6000	7	1	2	3	3	7	7	2
				239.1	239.2	239.2	239.223	0.03333	0.00666	0.02666	0.01393
851	6000	6000	6000	9	3	5	3	3	7	7	4
				239.5	239.2	239.2	239.336	0.19333	0.08666	0.10666	0.08077
2072	6000	6000	6000	3	5	3	7	3	7	7	9
				239.9	239.2	239.2					0.19626
3242	6000	6000	6000	4	5	2	239.47	0.47	0.22	0.25	7
				240.4	239.2	239.2	239.656	0.81333	0.38666	0.42666	0.33937
4376	6000	6000	6000	7	7	3	7	3	7	7	4
				240.9	239.2	239.2					0.47950
5492	6000	6000	6000	8	9	2	239.83	1.15	0.54	0.61	6
				241.5	239.3		240.006	1.50333	0.69666	0.80666	0.62637
6596	6000	6000	6000	1	1	239.2	7	3	7	7	1
				241.7	239.2	239.1					0.70396
7697	6000	6000	6000	6	6	9	240.07	1.69	0.81	0.88	1
				241.7	239.2	239.1					0.70396
7697	6000	6000	6000	6	6	9	240.07	1.69	0.81	0.88	1
				241.5	239.3		240.006	1.50333	0.69666	0.80666	0.62637
6596	6000	6000	6000	1	1	239.2	7	3	7	7	1
				240.9	239.2	239.2					0.47950
5492	6000	6000	6000	8	9	2	239.83	1.15	0.54	0.61	6
				240.4	239.2	239.2	239.656	0.81333	0.38666	0.42666	0.33937
4376	6000	6000	6000	7	7	3	7	3	7	7	4
				239.9	239.2	239.2					0.19626
3242	6000	6000	6000	4	5	2	239.47	0.47	0.22	0.25	7
				239.5	239.2	239.2	239.336	0.19333	0.08666	0.10666	0.08077
2072	6000	6000	6000	3	5	3	7	3	7	7	9
				239.1	239.2	239.2	239.223	0.03333	0.00666	0.02666	0.01393
851	6000	6000	6000	9	3	5	3	3	7	7	4
				238.9	239.2	239.2	239.153	0.16333	0.07666	0.08666	0.06829
110	6000	6000	6000	9	3	4	3	3	7	7	6
					239.2	239.2	238.853	0.75333	0.36666	0.38666	0.31539
228	6000	6000	6000	238.1	2	4	3	3	7	7	6

PV								Vdev	Vdev		
output	Balar	nce load	b	Va	Vb	Vc	Vage	а	b	Vdev c	%VUF
				234.8	235.8	235.7	235.493	0.65333	0.35666	0.29666	0.27743
145	8000	8000	8000	4	5	9	3	3	7	7	2
				238.8	239.1	239.1	239.036	0.14666	0.07333	0.07333	0.06135
110	8000	8000	8000	9	1	1	7	7	3	3	7
				239.0	239.1	239.1	239.113	0.03333	0.00666	0.02666	
851	8000	8000	8000	8	2	4	3	3	7	7	0.01394
				239.4	239.1	239.1					0.08360
2072	8000	8000	8000	3	3	3	239.23	0.2	0.1	0.1	2
				239.8	239.1	239.1					0.20052
3242	8000	8000	8000	5	4	2	239.37	0.48	0.23	0.25	6
				240.3	239.1	239.1	239.523	0.79666	0.39333	0.40333	0.33260
4376	8000	8000	8000	2	3	2	3	7	3	3	5
				240.8	239.1	239.1	239.703	1.12666	0.53333	0.59333	0.47002
5492	8000	8000	8000	3	7	1	3	7	3	3	5
				241.3	239.1	239.0					0.61283
6596	8000	8000	8000	4	8	9	239.87	1.47	0.69	0.78	2

1		1		241.8	239.1	239.0	240.026	1.78333	0.84666	0.93666	0.74297
7697	8000	8000	8000	1	8	9	7	3	7	7	3
				241.8	239.1	239.0	240.026	1.78333	0.84666	0.93666	0.74297
7697	8000	8000	8000	1	8	9	7	3	7	7	3
				241.3	239.1	239.0					0.61283
6596	8000	8000	8000	4	8	9	239.87	1.47	0.69	0.78	2
				240.8	239.1	239.1	239.703	1.12666	0.53333	0.59333	0.47002
5492	8000	8000	8000	3	7	1	3	7	3	3	5
				240.3	239.1	239.1	239.523	0.79666	0.39333	0.40333	0.33260
4376	8000	8000	8000	2	3	2	3	7	3	3	5
				239.8	239.1	239.1					0.20052
3242	8000	8000	8000	5	4	2	239.37	0.48	0.23	0.25	6
				239.4	239.1	239.1					0.08360
2072	8000	8000	8000	3	3	3	239.23	0.2	0.1	0.1	2
				239.0	239.1	239.1	239.113	0.03333	0.00666	0.02666	
851	8000	8000	8000	8	2	4	3	3	7	7	0.01394
				238.8	239.1	239.1	239.046	0.16666	0.08333	0.08333	0.06972
110	8000	8000	8000	8	3	3	7	7	3	3	1
				237.9	239.1	239.1	238.746	0.75666	0.36333	0.39333	0.31693
228	8000	8000	8000	9	1	4	7	7	3	3	3

PV								Vdev	Vdev		
output	Baland	ce load		Va	Vb	Vc	Vage	а	b	Vdev c	%VUF
				234.7	235.7	235.6	235.386	0.64666	0.35333	0.29333	0.27472
145	9999	9999	9999	4	4	8	7	7	3	3	5
				238.7	238.9		238.913	0.16333	0.07666	0.08666	0.06836
110	9999	9999	9999	5	9	239	3	3	7	7	5
				238.9	239.0	239.0	239.003	0.02333	0.00666	0.01666	0.00976
851	9999	9999	9999	8	1	2	3	3	7	7	3
				239.3	239.0	239.0	239.116	0.20333	0.09666	0.10666	0.08503
2072	9999	9999	9999	2	2	1	7	3	7	7	5
				239.7	239.0						0.20479
3242	9999	9999	9999	5	3	239	239.26	0.49	0.23	0.26	8
				240.1	239.0	238.9	239.403	0.78666	0.37333	0.41333	0.32859
4376	9999	9999	9999	9	3	9	3	7	3	3	5
				240.6	239.0	238.9					0.45084
5492	9999	9999	9999	3	4	8	239.55	1.08	0.51	0.57	5
				241.2	239.0	238.9	239.763	1.47666	0.69333	0.78333	0.61588
6596	9999	9999	9999	4	7	8	3	7	3	3	5
				241.6	239.0	238.9	239.903	1.76666	0.84333	0.92333	0.73640
7697	9999	9999	9999	7	6	8	3	7	3	3	8
				241.6	239.0	238.9	239.903	1.76666	0.84333	0.92333	0.73640
7697	9999	9999	9999	7	6	8	3	7	3	3	8
				241.2	239.0	238.9	239.763	1.47666	0.69333	0.78333	0.61588
6596	9999	9999	9999	4	7	8	3	7	3	3	5
5 402	0000	0000	0000	240.6	239.0	238.9	220 55	1.00	0.54	0.57	0.45084
5492	9999	9999	9999	3	4	8	239.55	1.08	0.51	0.57	5
4376	9999	9999	9999	240.1 9	239.0 3	238.9 9	239.403 3	0.78666 7	0.37333 3	0.41333	0.32859
4376	9999	9999	9999	-	-	9	3	/	3	3	5
2242	9999	0000	9999	239.7 5	239.0	220	220.20	0.40	0.22	0.20	0.20479 8
3242	9999	9999	9999	239.3	3	239	239.26	0.49	0.23	0.26	0.08503
2072	9999	9999	9999	239.3	239.0 2	239.0 1	239.116 7	0.20333	0.09666 7	0.10666	0.08503
2072	3333	3333	9999	238.9	239.0	239.0	239.003	0.02333	0.00666	0.01666	0.00976
851	9999	9999	9999	238.9	239.0	239.0	239.003	0.02333	0.00666	0.01666	0.00976
100	3333	2229	2223	238.7	239.0	239.0	238.936	0.16666	0.08333	0.08333	0.06975
110	9999	9999	9999	238.7	239.0	239.0	238.936	0.16666	0.08333	0.08333	0.06975
110	5555	5555	5555	237.8	2	239.0	/	/	5	5	0.31428
228	9999	9999	9999	237.8	239	239.0	238.64	0.75	0.36	0.39	0.31428
220	3333	2223	2223	9	239	5	230.04	0.75	0.30	0.39	L

Dynamic PV with Unbalanced load at same phase

PV											
outp											
ut	Unbal	ance	load	Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
											0.30526
145	2000	0	0	235.14	236.25	236.19	235.86	0.72	0.39	0.33	6
											0.09189
110	2000	0	0	239.18	239.5	239.52	239.4	0.22	0.1	0.12	6
054	2000	0	0	220.42	220 52	220 50	239.503	0.0000000	0.026667	0.05666	0.03479
851	2000	0	0	239.42	239.53	239.56	3	0.083333	0.026667	7	4
2072	2000	0	0	220 72	239.52	239.55	239.596 7	0 1 2 2 2 2 2	0.076667	0.04666 7	0.05147 5
2072	2000	0	0	239.72	239.52	239.55	239.753	0.123333	0.076667	0.19333	0.19047
3242	2000	0	0	240.21	239.49	239.56	239.753	0.456667	0.263333	0.19333	0.19047
J242	2000	0	0	240.21	233.43	235.50	5	0.430007	0.203333	5	0.31675
4376	2000	0	0	240.69	239.54	239.56	239.93	0.76	0.39	0.37	0.51075
	2000	Ű		210105	200101	200100	240.086	0.70	0.00	0.49666	0.44706
5492	2000	0	0	241.16	239.51	239.59	7	1.073333	0.576667	7	1
							240.263			0.78333	0.61044
6596	2000	0	0	241.73	239.58	239.48	3	1.466667	0.683333	3	1
											0.73208
7697	2000	0	0	242.17	239.55	239.51	240.41	1.76	0.86	0.9	3
							240.413			0.87333	0.71404
7697	2000	0	0	242.13	239.57	239.54	3	1.716667	0.843333	3	8
							240.263			0.78333	0.61044
6596	2000	0	0	241.73	239.58	239.48	3	1.466667	0.683333	3	1
							240.086			0.49666	0.44706
5492	2000	0	0	241.16	239.51	239.59	7	1.073333	0.576667	7	1
4276	2000	0	0	240.00	220 54	220 50	239.926	0 750000	0.200007	0.36666	0.31398
4376	2000	0	0	240.68	239.54	239.56	7 239.753	0.753333	0.386667	7 0.19333	5 0.19047
3242	2000	0	0	240.21	239.49	239.56	239.753	0.456667	0.263333	0.19333	
5242	2000	0	0	240.21	239.49	239.50	239.596	0.450007	0.205555	0.04666	4 0.05147
2072	2000	0	0	239.72	239.52	239.55	239.590	0.123333	0.076667	0.04666	0.05147
2072	2000	0	0	255.12	233.32	237.33	239.503	0.123333	0.070007	0.05666	0.03479
851	2000	0	0	239.42	239.53	239.56	235.503	0.083333	0.026667	0.05000	4
	_,,,,	Ű	Ŭ				239.423			0.11666	0.08910
110	2000	0	0	239.21	239.52	239.54	3	0.213333	0.096667	7	3
							239.116			0.41333	0.34153
228	2000	0	0	238.3	239.52	239.53	7	0.816667	0.403333	3	5

PV	Unbal	ance									
output	load			Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
							235.82			0.36333	0.33357
145	4000	0	0	235.04	236.25	236.19	67	0.786667	0.423333	3	8
							239.36			0.16666	0.12254
110	4000	0	0	239.07	239.49	239.53	33	0.293333	0.126667	7	7
											0.07099
851	4000	0	0	239.28	239.51	239.56	239.45	0.17	0.06	0.11	6
							239.58			0.02333	0.02782
2072	4000	0	0	239.65	239.54	239.56	33	0.066667	0.043333	3	6
							239.73			0.17333	0.15711
3242	4000	0	0	240.11	239.53	239.56	33	0.376667	0.203333	3	9
							239.89			0.31666	0.28484
4376	4000	0	0	240.58	239.53	239.58	67	0.683333	0.366667	7	5

							240.05			0.46333	0.41935
5492	4000	0	0	241.06	239.51	239.59	33	1.006667	0.543333	3	1
											0.58275
6596	4000	0	0	241.64	239.49	239.59	240.24	1.4	0.75	0.65	1
											0.66164
7697	4000	0	0	241.9	239.51	239.52	240.31	1.59	0.8	0.79	5
											0.66164
7697	4000	0	0	241.9	239.51	239.52	240.31	1.59	0.8	0.79	5
											0.58275
6596	4000	0	0	241.64	239.49	239.59	240.24	1.4	0.75	0.65	1
							240.05			0.46333	0.41935
5492	4000	0	0	241.06	239.51	239.59	33	1.006667	0.543333	3	1
							239.89			0.31666	0.28484
4376	4000	0	0	240.58	239.53	239.58	67	0.683333	0.366667	7	5
							239.73			0.16666	0.15572
3242	4000	0	0	240.11	239.53	239.57	67	0.373333	0.206667	7	6
							239.58			0.02333	0.02782
2072	4000	0	0	239.65	239.54	239.56	33	0.066667	0.043333	3	6
											0.07099
851	4000	0	0	239.28	239.51	239.56	239.45	0.17	0.06	0.11	6
							239.38			0.16333	0.12392
110	4000	0	0	239.09	239.52	239.55	67	0.296667	0.133333	3	8
							239.08			0.45666	0.37364
228	4000	0	0	238.19	239.52	239.54	33	0.893333	0.436667	7	9

PV	Unbala	nce									
output	load			Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
							235.766			0.40333	0.37183
145	6000	0	0	234.89	236.24	236.17	7	0.876667	0.473333	3	7
							239.323			0.20666	0.15599
110	6000	0	0	238.95	239.49	239.53	3	0.373333	0.166667	7	5
							239.413			0.14666	0.10163
851	6000	0	0	239.17	239.51	239.56	3	0.243333	0.096667	7	7
											0.01252
2072	6000	0	0	239.51	239.52	239.56	239.53	0.02	0.01	0.03	5
		_	_				239.663			0.10333	0.10709
3242	6000	0	0	239.92	239.51	239.56	3	0.256667	0.153333	3	5
											0.24600
4376	6000	0	0	240.42	239.5	239.57	239.83	0.59	0.33	0.26	8
5 402	6000	0	0	240.02	220 5	220 50	240	0.02	0.5	0.42	0.38333
5492	6000	0	0	240.92	239.5	239.58	240	0.92	0.5	0.42	3
6596	6000	0	0	241.38	239.51	239.57	240.153 3	1.226667	0.643333	0.58333 3	0.51078 5
0590	6000	0	0	241.38	239.51	239.57	240.323	1.220007	0.043333	0.71333	0.63525
7697	6000	0	0	241.85	239.51	239.61	240.323	1.526667	0.813333	0.71333	0.03525
7057	0000	0	0	241.05	235.51	235.01	5	1.520007	0.015555	5	5
7697	6000	0	0	241.9	239.51	239.61	240.34	1.56	0.83	0.73	0.64908
							240.153			0.58333	0.51078
6596	6000	0	0	241.38	239.51	239.57	3	1.226667	0.643333	3	5
											0.38333
5492	6000	0	0	240.92	239.5	239.58	240	0.92	0.5	0.42	3
				- · - · -							0.24600
4376	6000	0	0	240.42	239.5	239.57	239.83	0.59	0.33	0.26	8
	6006					222 5 5	239.663	0.05000	0.450000	0.10333	0.10709
3242	6000	0	0	239.92	239.51	239.56	3	0.256667	0.153333	3	5
2072	6000		•	220 51	220 52	220 50	220 52	0.00	0.01	0.00	0.01252
2072	6000	0	0	239.51	239.52	239.56	239.53	0.02	0.01	0.03	5
051	6000	0	0	220 17	220 E1	220 56	239.413 3	0 242222	0.006667	0.14666	0.10163
851	6000	0	0	239.17	239.51	239.56	239.343	0.243333	0.096667	0.20666	0.15598
110	6000	0	0	70 000	220 E1	220 55	239.343	0 272222	0 166657	0.20666	
110	6000	U	U	238.97	239.51	239.55	3	0.373333	0.166667	/	2

Ì								239.046			0.50333	0.40438	l
	228	6000	0	0	238.08	239.51	239.55	7	0.966667	0.463333	3	4	

PV	Unbal	ance	5								
output	load			Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
											0.40156
145	8000	0	0	234.8	236.23	236.21	235.7467	0.946667	0.483333	0.463333	1
											0.19224
110	8000	0	0	238.82	239.48	239.54	239.28	0.46	0.2	0.26	3
851	8000	0	0	239.04	239.5	239.57	239.37	0.33	0.13	0.2	0.13786 2
001	8000	0	0	235.04	239.5	239.37	239.37	0.55	0.13	0.2	0.04314
2072	8000	0	0	239.38	239.51	239.56	239.4833	0.103333	0.026667	0.076667	8
		-	-								0.07511
3242	8000	0	0	239.81	239.51	239.57	239.63	0.18	0.12	0.06	6
											0.20713
4376	8000	0	0	240.28	239.5	239.57	239.7833	0.496667	0.283333	0.213333	1
- 100			•							0.07	0.33341
5492	8000	0	0	240.74	239.51	239.57	239.94	0.8	0.43	0.37	7 0.49277
6596	8000	0	0	241.32	239.52	239.57	240.1367	1.183333	0.616667	0.566667	0.49277
0350	8000	0	0	241.52	233.32	235.57	240.1307	1.1055555	0.010007	0.500007	0.61178
7697	8000	0	0	241.75	239.52	239.57	240.28	1.47	0.76	0.71	6
											0.61178
7697	8000	0	0	241.75	239.52	239.57	240.28	1.47	0.76	0.71	6
											0.49277
6596	8000	0	0	241.32	239.52	239.57	240.1367	1.183333	0.616667	0.566667	5
F 402	0000	0	0	240 74	220 54	220 57	220.04	0.0	0.42	0.27	0.33341
5492	8000	0	0	240.74	239.51	239.57	239.94	0.8	0.43	0.37	7 0.20713
4376	8000	0	0	240.28	239.5	239.57	239.7833	0.496667	0.283333	0.213333	0.20713
4570	0000	0	0	240.20	233.5	235.57	235.7035	0.450007	0.203333	0.215555	0.07511
3242	8000	0	0	239.81	239.51	239.57	239.63	0.18	0.12	0.06	6
											0.04314
2072	8000	0	0	239.38	239.51	239.56	239.4833	0.103333	0.026667	0.076667	8
											0.13786
851	8000	0	0	239.04	239.5	239.57	239.37	0.33	0.13	0.2	2
110	8000	0	0	238.84	220 5	239.56	239.3	0.46	0.2	0.26	0.19222 7
110	8000	U	U	238.84	239.5	239.30	239.3	0.46	0.2	0.26	0.43653
228	8000	0	0	237.96	239.5	239.55	239.0033	1.043333	0.496667	0.546667	0.43055

PV	Unbal	ance	9								
output	load			Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
											0.44268
145	9999	0	0	234.64	236.23	236.18	235.6833	1.043333	0.546667	0.496667	4
											0.23129
110	9999	0	0	238.68	239.48	239.54	239.2333	0.553333	0.246667	0.306667	4
851	9999	0	0	238.91	239.5	239.57	239.3267	0.416667	0.173333	0.243333	0.1741
											0.07656
2072	9999	0	0	239.26	239.5	239.57	239.4433	0.183333	0.056667	0.126667	6
											0.04034
3242	9999	0	0	239.68	239.5	239.57	239.5833	0.096667	0.083333	0.013333	8
											0.16268
4376	9999	0	0	240.12	239.5	239.57	239.73	0.39	0.23	0.16	3

											0.29318
5492	9999	0	0	240.6	239.51	239.58	239.8967	0.703333	0.386667	0.316667	2
											0.44983
6596	9999	0	0	241.17	239.52	239.58	240.09	1.08	0.57	0.51	1
											0.58551
7697	9999	0	0	241.65	239.51	239.57	240.2433	1.406667	0.733333	0.673333	7
											0.58551
7697	9999	0	0	241.65	239.51	239.57	240.2433	1.406667	0.733333	0.673333	7
											0.44983
6596	9999	0	0	241.17	239.52	239.58	240.09	1.08	0.57	0.51	1
											0.29318
5492	9999	0	0	240.6	239.51	239.58	239.8967	0.703333	0.386667	0.316667	2
											0.16268
4376	9999	0	0	240.12	239.5	239.57	239.73	0.39	0.23	0.16	3
											0.04034
3242	9999	0	0	239.68	239.5	239.57	239.5833	0.096667	0.083333	0.013333	8
											0.07656
2072	9999	0	0	239.26	239.5	239.57	239.4433	0.183333	0.056667	0.126667	6
851	9999	0	0	238.91	239.5	239.57	239.3267	0.416667	0.173333	0.243333	0.1741
											0.22848
110	9999	0	0	238.71	239.5	239.56	239.2567	0.546667	0.243333	0.303333	5
											0.47288
228	9999	0	0	237.83	239.49	239.56	238.96	1.13	0.53	0.6	2

Dynamic PV with unbalanced load at difference phase

PV	U	nbaland	ce								
output	lo	ad		Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
							235.826			0.25333	0.25301
145	0	2000	2000	235.23	236.17	236.08	7	0.596667	0.343333	3	1
							239.406			0.00333	0.01531
110	0	2000	2000	239.37	239.44	239.41	7	0.036667	0.033333	3	6
							239.476			0.07666	0.03897
851	0	2000	2000	239.57	239.46	239.4	7	0.093333	0.016667	7	4
							239.616			0.34666	0.14745
2072	0	2000	2000	239.97	239.61	239.27	7	0.353333	0.006667	7	8
							239.696			0.43666	0.23084
3242	0	2000	2000	240.25	239.58	239.26	7	0.553333	0.116667	7	7
							239.913			0.71333	0.39458
4376	0	2000	2000	240.86	239.68	239.2	3	0.946667	0.233333	3	7
							240.136			1.01666	0.55940
5492	0	2000	2000	241.48	239.81	239.12	7	1.343333	0.326667	7	4
6506	~	2000			222.04				0.54	4.95	0.74890
6596	0	2000	2000	242.15	239.81	239.09	240.35	1.8	0.54	1.26	8
7607	~	2000	2000	242.45	220.07	220.00	240.436	2 04 2 2 2 2	0.50007	1.44666	0.83736
7697	0	2000	2000	242.45	239.87	238.99	7	2.013333	0.566667	7	5
7697	0	2000	2000	242.45	239.87	238.99	240.436 7	2 012222	0.566667	1.44666 7	0.83736
7697	0	2000	2000	242.45	239.87	238.99	240.286	2.013333	0.500007	1.24666	5 0.71303
6596	0	2000	2000	242	239.82	239.04	240.286 7	1.713333	0.466667	1.24000	0.71303
0390	0	2000	2000	242	235.02	235.04	240.136	1.715555	0.400007	1.01666	0.55940
5492	0	2000	2000	241.48	239.81	239.12	240.130 7	1.343333	0.326667	1.01000	0.55540
5452	Ŭ	2000	2000	241.40	235.01	235.12	,	1.5455555	0.320007	,	0.39598
4376	0	2000	2000	240.86	239.73	239.14	239.91	0.95	0.18	0.77	2
	-						239.696			0.43666	0.23084
3242	0	2000	2000	240.25	239.58	239.26		0.553333	0.116667	7	7
	-						239.616			0.34666	0.14745
2072	0	2000	2000	239.97	239.61	239.27	7	0.353333	0.006667	7	8
							239.476			0.07666	0.03897
851	0	2000	2000	239.57	239.46	239.4	7	0.093333	0.016667	7	4

								239.426			0.00333	0.01531
	110	0	2000	2000	239.39	239.46	239.43	7	0.036667	0.033333	3	4
								239.086			0.34333	0.29138
	228	0	2000	2000	238.39	239.44	239.43	7	0.696667	0.353333	3	7

PV	U	nbalano	ce								
output	lo	ad		Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
							235.756			0.21333	0.22339
145	0	4000	4000	235.23	236.07	235.97	7	0.526667	0.313333	3	4
							239.326			0.03666	0.01532
110	0	4000	4000	239.34	239.35	239.29	7	0.013333	0.023333	7	1
851	0	4000	4000	239.5	239.34	239.33	239.39	0.11	0.05	0.06	0.04595
2072	0	4000	4000	239.95	239.52	239.18	239.55	0.4	0.03	0.37	0.16698
							239.766			0.66666	0.33504
3242	0	4000	4000	240.57	239.63	239.1	7	0.803333	0.136667	7	8
											0.37954
4376	0	4000	4000	240.67	239.55	239.06	239.76	0.91	0.21	0.7	6
5 400		1000					240.033	1.076667	0.000000	1.11333	0.57353
5492	0	4000	4000	241.41	239.77	238.92	3	1.376667	0.263333	3	1
6596	0	4000	4000	241.89	239.65	239.01	240.183 3	1.706667	0.533333	1.17333 3	0.71056 8
0590	0	4000	4000	241.09	259.05	259.01	240.386	1.700007	0.5555555	1.44666	o 0.86249
7697	0	4000	4000	242.46	239.76	238.94	240.380	2.073333	0.626667	1.44000	0.80249
1057	Ŭ	1000	1000	212.10	233.70	230.51	240.386	2.0755555	0.020007	1.44666	0.86249
7697	0	4000	4000	242.46	239.76	238.94	7	2.073333	0.626667	7	9
											0.69956
6596	0	4000	4000	241.83	239.76	238.86	240.15	1.68	0.39	1.29	3
							240.033			1.11333	0.57353
5492	0	4000	4000	241.41	239.77	238.92	3	1.376667	0.263333	3	1
											0.37954
4376	0	4000	4000	240.67	239.55	239.06	239.76	0.91	0.21	0.7	6
							239.766			0.66666	0.33504
3242	0	4000	4000	240.57	239.63	239.1	7	0.803333	0.136667	7	8
2072	0	4000	4000	239.95	239.52	239.18	239.55	0.4	0.03	0.37	0.16698
851	0	4000	4000	239.5	239.34	239.33	239.39	0.11	0.05	0.06	0.04595
							239.346			0.03666	0.01531
110	0	4000	4000	239.36	239.37	239.31	7	0.013333	0.023333	7	9
							239.013			0.30666	0.26497
228	0	4000	4000	238.38	239.34	239.32	3	0.633333	0.326667	7	8

PV	U	nbalano	ce								
output	lo	ad		Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
							235.686			0.17333	
145	0	6000	6000	235.23	235.97	235.86	7	0.456667	0.283333	3	0.19376
							239.246			0.07666	0.03204
110	0	6000	6000	239.32	239.25	239.17	7	0.073333	0.003333	7	5
							239.283			0.09333	0.05711
851	0	6000	6000	239.42	239.24	239.19	3	0.136667	0.043333	3	5
											0.18793
2072	0	6000	6000	239.89	239.41	239.02	239.44	0.45	0.03	0.42	9
							239.653			0.73333	0.34911
3242	0	6000	6000	240.49	239.55	238.92	3	0.836667	0.103333	3	5
							239.766			0.79666	0.45599
4376	0	6000	6000	240.86	239.47	238.97	7	1.093333	0.296667	7	9

1							239.986			1.11666	
5492	0	6000	6000	241.47	239.62	238.87	7	1.483333	0.366667	7	0.61809
							240.133			1.35333	0.75652
6596	0	6000	6000	241.95	239.67	238.78	3	1.816667	0.463333	3	4
							240.333			1.48333	0.90152
7697	0	6000	6000	242.5	239.65	238.85	3	2.166667	0.683333	3	6
							240.333			1.48333	0.90152
7697	0	6000	6000	242.5	239.65	238.85	3	2.166667	0.683333	3	6
											0.79513
6596	0	6000	6000	242.12	239.66	238.85	240.21	1.91	0.55	1.36	8
											0.63330
5492	0	6000	6000	241.53	239.59	238.91	240.01	1.52	0.42	1.1	7
							239.766			0.79666	0.45599
4376	0	6000	6000	240.86	239.47	238.97	7	1.093333	0.296667	7	9
							239.656			0.73666	
3242	0	6000	6000	240.49	239.56	238.92	7	0.833333	0.096667	7	0.34772
							239.436			0.41666	0.18515
2072	0	6000	6000	239.88	239.41	239.02	7	0.443333	0.026667	7	7
							239.286			0.09666	0.05572
851	0	6000	6000	239.42	239.25	239.19	7	0.133333	0.036667	7	1
							239.246			0.07666	0.03204
110	0	6000	6000	239.32	239.25	239.17	7	0.073333	0.003333	7	5
							238.903			0.25666	0.24417
228	0	6000	6000	238.32	239.23	239.16	3	0.583333	0.326667	7	1

PV	U	nbalanc	ce								
output	lo	ad		Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
-							235.606			0.12333	0.15987
145	0	8000	8000	235.23	235.86	235.73	7	0.376667	0.253333	3	1
											0.05853
110	0	8000	8000	239.3	239.14	239.04	239.16	0.14	0.02	0.12	8
											0.09196
851	0	8000	8000	239.44	239.15	239.07	239.22	0.22	0.07	0.15	6
2072	•			• • •				0.50	0.00	0.50	0.24225
2072	0	8000	8000	240	239.4	238.86	239.42	0.58	0.02	0.56	2
2242	0	8000	8000	240.49	220.45	220 70	239.573	0.006667	0 1 2 2 2 2 2	0.78333	0.37845
3242	0	8000	8000	240.48	239.45	238.79	3	0.906667	0.123333	3	1 0.47982
4376	0	8000	8000	240.82	239.36	238.83	239.67	1.15	0.31	0.84	0.47982
4370	0	0000	8000	240.02	235.50	230.03	233.07	1.15	0.51	0.04	0.65024
5492	0	8000	8000	241.47	239.52	238.74	239.91	1.56	0.39	1.17	4
0.01	Ū	0000	0000		200102	20007	240.143	1.00	0.00	1.51333	0.83144
6596	0	8000	8000	242.14	239.66	238.63	3	1.996667	0.483333	3	8
							240.016			1.40666	0.80966
7697	0	8000	8000	241.96	239.48	238.61	7	1.943333	0.536667	7	6
							240.016			1.40666	0.80966
7697	0	8000	8000	241.96	239.48	238.61	7	1.943333	0.536667	7	6
							240.143			1.51333	0.83144
6596	0	8000	8000	242.14	239.66	238.63	3	1.996667	0.483333	3	8
											0.67511
5492	0	8000	8000	241.58	239.47	238.83	239.96	1.62	0.49	1.13	3
4070		0000	8000	240.02	220.20	220.02	220 67	1 45	0.24	0.04	0.47982
4376	0	8000	8000	240.82	239.36	238.83	239.67	1.15	0.31	0.84	6
3242	0	8000	8000	240.48	239.45	238.79	239.573 3	0.906667	0.123333	0.78333 3	0.37845
3242	U	8000	8000	240.48	239.45	238.79	3	0.900007	0.123333	3	1 0.25059
2072	0	8000	8000	240.03	239.4	238.86	239.43	0.6	0.03	0.57	0.25059
2072	0	0000	0000	240.03	233.4	230.00	233.43	0.0	0.05	0.57	0.09196
851	0	8000	8000	239.44	239.15	239.07	239.22	0.22	0.07	0.15	6
110	0	8000	8000	239.32	239.16	239.06	239.18	0.14	0.02	0.12	0.05853

											3
							238.863			0.21666	0.20234
228	0	8000	8000	238.38	239.13	239.08	3	0.483333	0.266667	7	7

PV	U	nbaland	ce								
output	lo	ad		Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
							235.526			0.07333	0.12595
145	0	9999	9999	235.23	235.75	235.6	7	0.296667	0.223333	3	9
							239.056			0.14666	0.08087
110	0	9999	9999	239.25	239.01	238.91	7	0.193333	0.046667	7	3
							239.133			0.20333	0.12824
851	0	9999	9999	239.44	239.03	238.93	3	0.306667	0.103333	3	1
							239.296			0.63666	0.26605
2072	0	9999	9999	239.91	239.32	238.66	7	0.613333	0.023333	7	7
											0.40920
3242	0	9999	9999	240.47	239.35	238.65	239.49	0.98	0.14	0.84	3
											0.50922
4376	0	9999	9999	240.8	239.25	238.69	239.58	1.22	0.33	0.89	4
							239.836			1.23666	0.69352
5492	0	9999	9999	241.5	239.41	238.6	7	1.663333	0.426667	7	8
											0.84576
6596	0	9999	9999	242.05	239.56	238.45	240.02	2.03	0.46	1.57	3
7607	~	0000	0000	244.00	220.25	220.47	239.903	4 000007	0 553333	1.43333	0.82811
7697	0	9999	9999	241.89	239.35	238.47	3	1.986667	0.553333	3	1
707	~	9999	9999	241.00	220.25	220 47	239.903	1.000007	0 552222	1.43333	0.82811
7697	0	9999	9999	241.89	239.35	238.47	3	1.986667	0.553333	3	1 0.84576
6596	0	9999	9999	242.05	239.56	238.45	240.02	2.03	0.46	1.57	0.84576
0390	0	9999	9999	242.05	259.50	230.45	239.836	2.05	0.40	1.23666	0.69352
5492	0	9999	9999	241.5	239.41	238.6	239.830	1.663333	0.426667	1.23000	0.09352
5452	0	5555	5555	241.5	233.41	230.0	,	1.005555	0.420007	,	0.50922
4376	0	9999	9999	240.8	239.25	238.69	239.58	1.22	0.33	0.89	0.30922
	-						239.523		1.50	0.76333	0.42445
3242	0	9999	9999	240.54	239.27	238.76	3	1.016667	0.253333	3	4
							239.296			0.63666	0.26605
2072	0	9999	9999	239.91	239.32	238.66	7	0.613333	0.023333	7	7
							239.133			0.20333	0.12824
851	0	9999	9999	239.44	239.03	238.93	3	0.306667	0.103333	3	1
							239.076			0.14666	0.08086
110	0	9999	9999	239.27	239.03	238.93	7	0.193333	0.046667	7	7
											0.16751
228	0	9999	9999	238.38	239.01	238.95	238.78	0.4	0.23	0.17	8

Dynamic Load with PV

PV supply = 2072W

Unbalance	e Lo	ad	Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
0	0	0	240.08	239.52	239.52	239.7067	0.373333	0.186667	0.186667	0.155746
2000	0	0	239.8	239.55	239.53	239.6267	0.173333	0.076667	0.096667	0.072335
4000	0	0	239.72	239.53	239.54	239.5967	0.123333	0.066667	0.056667	0.051475
6000	0	0	239.52	239.52	239.56	239.5333	0.013333	0.013333	0.026667	0.011133
8000	0	0	239.38	239.51	239.58	239.49	0.11	0.02	0.09	0.045931
8000	0	0	239.38	239.51	239.57	239.4867	0.106667	0.023333	0.083333	0.04454

6000	0	0	239.52	239.52	239.56	239.5333	0.013333	0.013333	0.026667	0.011133
4000	0	0	239.72	239.53	239.54	239.5967	0.123333	0.066667	0.056667	0.051475
2000	0	0	239.79	239.55	239.53	239.6233	0.166667	0.073333	0.093333	0.069554
0	0	0	240.12	239.55	239.55	239.74	0.38	0.19	0.19	0.158505

PV supply = 4151W

Unbalance	e Lo	ad	Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
0	0	0	241.5	239.54	239.48	240.1733	1.326667	0.633333	0.693333	0.552379
2000	0	0	240.89	239.55	239.58	240.0067	0.883333	0.456667	0.426667	0.368045
4000	0	0	240.46	239.49	239.56	239.8367	0.623333	0.346667	0.276667	0.259899
6000	0	0	240.48	239.56	239.52	239.8533	0.626667	0.293333	0.333333	0.261271
8000	0	0	240.29	239.55	239.54	239.7933	0.496667	0.243333	0.253333	0.207123
8000	0	0	240.29	239.55	239.54	239.7933	0.496667	0.243333	0.253333	0.207123
6000	0	0	240.48	239.56	239.52	239.8533	0.626667	0.293333	0.333333	0.261271
4000	0	0	240.46	239.49	239.56	239.8367	0.623333	0.346667	0.276667	0.259899
2000	0	0	240.89	239.55	239.58	240.0067	0.883333	0.456667	0.426667	0.368045
0	0	0	241.53	239.57	239.51	240.2033	1.326667	0.633333	0.693333	0.55231

PV supply = 5491W

Unbalance	e Lo	ad	Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
0	0	0	242.52	239.61	239.51	240.5467	1.973333	0.936667	1.036667	0.820354
2000	0	0	241.24	239.51	239.56	240.1033	1.136667	0.593333	0.543333	0.473407
4000	0	0	241.11	239.53	239.55	240.0633	1.046667	0.533333	0.513333	0.435996
6000	0	0	241.13	239.53	239.56	240.0733	1.056667	0.543333	0.513333	0.440143
8000	0	0	240.89	239.54	239.54	239.99	0.9	0.45	0.45	0.375016
8000	0	0	240.89	239.54	239.54	239.99	0.9	0.45	0.45	0.375016
6000	0	0	241.13	239.53	239.56	240.0733	1.056667	0.543333	0.513333	0.440143
4000	0	0	241.11	239.53	239.55	240.0633	1.046667	0.533333	0.513333	0.435996
2000	0	0	241.24	239.51	239.56	240.1033	1.136667	0.593333	0.543333	0.473407
0	0	0	242.54	239.63	239.53	240.5667	1.973333	0.936667	1.036667	0.820285

Unbalance	e Lo	ad	Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
0	0	0	243.51	239.63	239.52	240.8867	2.623333	1.256667	1.366667	1.089032
2000	0	0	242.31	239.6	239.53	240.48	1.83	0.88	0.95	0.760978
4000	0	0	242.2	239.59	239.55	240.4467	1.753333	0.856667	0.896667	0.729198
6000	0	0	241.67	239.51	239.54	240.24	1.43	0.73	0.7	0.595238
8000	0	0	241.53	239.48	239.6	240.2033	1.326667	0.723333	0.603333	0.55231
8000	0	0	241.53	239.48	239.6	240.2033	1.326667	0.723333	0.603333	0.55231

e	5000	0	0	241.67	239.51	239.54	240.24	1.43	0.73	0.7	0.595238
4	1000	0	0	242.2	239.6	239.55	240.45	1.75	0.85	0.9	0.727802
2	2000	0	0	242.15	239.56	239.52	240.41	1.74	0.85	0.89	0.723764
	0	0	0	243.53	239.65	239.54	240.9067	2.623333	1.256667	1.366667	1.088942

Dynamic Load with PV at Balanced load

PV supply = 2072W

balar	nce Loa	ıd	Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
0	0	0	240.15	239.56	239.54	239.75	0.4	0.19	0.21	0.16684
2000	2000	2000	239.68	239.47	239.35	239.5	0.18	0.03	0.15	0.075157
4000	4000	4000	239.77	239.46	239.31	239.5133	0.256667	0.053333	0.203333	0.107162
6000	6000	6000	239.57	239.33	239.11	239.3367	0.233333	0.006667	0.226667	0.097492
8000	8000	8000	239.5	239.23	238.97	239.2333	0.266667	0.003333	0.263333	0.111467
8000	8000	8000	239.5	239.23	238.97	239.2333	0.266667	0.003333	0.263333	0.111467
6000	6000	6000	239.57	239.33	239.11	239.3367	0.233333	0.006667	0.226667	0.097492
4000	4000	4000	239.77	239.46	239.31	239.5133	0.256667	0.053333	0.203333	0.107162
2000	2000	2000	239.68	239.48	239.35	239.5033	0.176667	0.023333	0.153333	0.073764
0	0	0	240.17	239.59	239.56	239.7733	0.396667	0.183333	0.213333	0.165434

PV supply = 4151W

balar	nce Loa	d	Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
0	0	0	241.72	239.62	239.49	240.2767	1.443333	0.656667	0.786667	0.600696
2000	2000	2000	240.65	239.52	239.26	239.81	0.84	0.29	0.55	0.350277
4000	4000	4000	240.64	239.45	239.27	239.7867	0.853333	0.336667	0.516667	0.355872
6000	6000	6000	240.28	239.34	239.09	239.57	0.71	0.23	0.48	0.296364
8000	8000	8000	240.53	239.27	239.06	239.62	0.91	0.35	0.56	0.379768
8000	8000	8000	240.53	239.27	239.06	239.62	0.91	0.35	0.56	0.379768
6000	6000	6000	240.28	239.34	239.09	239.57	0.71	0.23	0.48	0.296364
4000	4000	4000	240.53	239.48	239.19	239.7333	0.796667	0.253333	0.543333	0.332314
2000	2000	2000	240.65	239.52	239.26	239.81	0.84	0.29	0.55	0.350277
0	0	0	241.67	239.58	239.56	240.27	1.4	0.69	0.71	0.582678

PV supply = 5491W

balan	nce Loa	d	Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
0	0	0	242.68	239.66	239.48	240.6067	2.073333	0.946667	1.126667	0.861711
2000	2000	2000	241.02	239.46	239.24	239.9067	1.113333	0.446667	0.666667	0.464069
4000	4000	4000	241	239.37	239.26	239.8767	1.123333	0.506667	0.616667	0.468296
6000	6000	6000	241.19	239.41	239.17	239.9233	1.266667	0.513333	0.753333	0.527946
8000	8000	8000	241.02	239.29	239.06	239.79	1.23	0.5	0.73	0.512949

8000	8000	8000	241.02	239.3	239.06	239.7933	1.226667	0.493333	0.733333	0.511552
6000	6000	6000	241.19	239.41	239.17	239.9233	1.266667	0.513333	0.753333	0.527946
4000	4000	4000	241	239.37	239.26	239.8767	1.123333	0.506667	0.616667	0.468296
2000	2000	2000	241.02	239.46	239.24	239.9067	1.113333	0.446667	0.666667	0.464069
0	0	0	242.7	239.7	239.51	240.6367	2.063333	0.936667	1.126667	0.857448

PV supply = 7035W

balar	balance Load		Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
0	0	0	243.96	239.67	239.62	241.0833	2.876667	1.413333	1.463333	1.193225
2000	2000	2000	242.27	239.55	239.31	240.3767	1.893333	0.826667	1.066667	0.787653
4000	4000	4000	242	239.49	239.2	240.23	1.77	0.74	1.03	0.736794
6000	6000	6000	241.71	239.45	239.02	240.06	1.65	0.61	1.04	0.687328
8000	8000	8000	241.56	239.27	238.98	239.9367	1.623333	0.666667	0.956667	0.676567
8000	8000	8000	241.46	239.32	238.88	239.8867	1.573333	0.566667	1.006667	0.655865
6000	6000	6000	241.7	239.45	238.97	240.04	1.66	0.59	1.07	0.691551
4000	4000	4000	242	239.49	239.2	240.23	1.77	0.74	1.03	0.736794
2000	2000	2000	242.27	239.55	239.31	240.3767	1.893333	0.826667	1.066667	0.787653
0	0	0	243.98	239.7	239.64	241.1067	2.873333	1.406667	1.466667	1.191727

Dynamic load with PV at the difference phase

PV supply = 2072W

Ur	Unbalance Load		Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
0	0	0	240.15	239.56	239.53	239.7467	0.403333	0.186667	0.216667	0.168233
0	2000	2000	239.81	239.48	239.26	239.5167	0.293333	0.036667	0.256667	0.122469
0	4000	4000	239.76	239.38	239.08	239.4067	0.353333	0.026667	0.326667	0.147587
0	6000	6000	239.85	239.35	238.9	239.3667	0.483333	0.016667	0.466667	0.201922
0	8000	8000	240.1	239.26	238.83	239.3967	0.703333	0.136667	0.566667	0.293794
0	8000	8000	240.17	239.22	238.82	239.4033	0.766667	0.183333	0.583333	0.320241
0	6000	6000	239.83	239.29	239.02	239.38	0.45	0.09	0.36	0.187986
0	4000	4000	239.96	239.44	239.08	239.4933	0.466667	0.053333	0.413333	0.194856
0	2000	2000	240.06	239.46	239.31	239.61	0.45	0.15	0.3	0.187805
0	0	0	240.17	239.59	239.58	239.78	0.39	0.19	0.2	0.162649

PV supply = 4151W

Ur	Unbalance Load		Va	Vb Vc		Vage	Vdev a	Vdev b	Vdev c	%VUF
0	0	0	241.49	239.62	239.47	240.1933	1.296667	0.573333	0.723333	0.539843
0	2000	2000	240.96	239.5	239.27	239.91	1.05	0.41	0.64	0.437664
0	4000	4000	240.88	239.51	239.03	239.8067	1.073333	0.296667	0.776667	0.447583

0	6000	6000	240.73	239.41	238.94	239.6933	1.036667	0.283333	0.753333	0.432497
0	8000	8000	240.65	239.26	238.68	239.53	1.12	0.27	0.85	0.467582
0	8000	8000	240.87	239.23	238.86	239.6533	1.216667	0.423333	0.793333	0.507678
0	6000	6000	240.92	239.33	238.82	239.69	1.23	0.36	0.87	0.513163
0	4000	4000	241.12	239.48	239.09	239.8967	1.223333	0.416667	0.806667	0.509942
0	2000	2000	241.06	239.58	239.2	239.9467	1.113333	0.366667	0.746667	0.463992
0	0	0	241.8	239.61	239.56	240.3233	1.476667	0.713333	0.763333	0.61445

PV supply = 5491W

Ur	Unbalance Load		Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
0	0	0	242.66	239.67	239.5	240.61	2.05	0.94	1.11	0.852001
0	2000	2000	241.64	239.56	239.2	240.1333	1.506667	0.573333	0.933333	0.627429
0	4000	4000	241.7	239.57	239.05	240.1067	1.593333	0.536667	1.056667	0.663594
0	6000	6000	241.25	239.41	238.84	239.8333	1.416667	0.423333	0.993333	0.590688
0	8000	8000	241.27	239.24	238.8	239.77	1.5	0.53	0.97	0.6256
0	8000	8000	241.27	239.28	238.74	239.7633	1.506667	0.483333	1.023333	0.628397
0	6000	6000	241.3	239.43	238.85	239.86	1.44	0.43	1.01	0.60035
0	4000	4000	241.39	239.52	238.94	239.95	1.44	0.43	1.01	0.600125
0	2000	2000	241.64	239.66	239.2	240.1667	1.473333	0.506667	0.966667	0.613463
0	0	0	242.82	239.67	239.58	240.69	2.13	1.02	1.11	0.884956

Ur	Unbalance Load		Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
0	0	0	243.96	239.67	239.62	241.0833	2.876667	1.413333	1.463333	1.193225
0	2000	2000	242.45	239.57	239.22	240.4133	2.036667	0.843333	1.193333	0.847152
0	4000	4000	242.3	239.55	239.06	240.3033	1.996667	0.753333	1.243333	0.830894
0	6000	6000	242.01	239.39	239.05	240.15	1.86	0.76	1.1	0.774516
0	8000	8000	242.11	239.32	238.56	239.9967	2.113333	0.676667	1.436667	0.880568
0	8000	8000	241.79	239.24	238.75	239.9267	1.863333	0.686667	1.176667	0.776626
0	6000	6000	241.94	239.39	238.8	240.0433	1.896667	0.653333	1.243333	0.790135
0	4000	4000	242.16	239.67	238.96	240.2633	1.896667	0.593333	1.303333	0.789412
0	2000	2000	242.3	239.56	239.16	240.34	1.96	0.78	1.18	0.815511
0	0	0	243.98	239.7	239.64	241.1067	2.873333	1.406667	1.466667	1.191727

PV	unba	lance	load	Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
145	0	0	0	238.33	239.47	239.47	239.09	0.76	0.38	0.38	0.317872
110	0	0	0	239.61	239.53	239.55	239.5633	0.046667	0.033333	0.013333	0.01948
851	2000	2000	2000	239.44	239.49	239.41	239.4467	0.006667	0.043333	0.036667	0.018097
2072	2000	2000	2000	239.68	239.47	239.35	239.5	0.18	0.03	0.15	0.075157
3242	4000	4000	4000	240.09	239.39	239.24	239.5733	0.516667	0.183333	0.333333	0.215661
4376	4000	4000	4000	240.6	239.48	239.18	239.7533	0.846667	0.273333	0.573333	0.353141
5492	6000	6000	6000	241.2	239.39	239.17	239.92	1.28	0.53	0.75	0.533511
6596	6000	6000	6000	241.43	239.39	239.09	239.97	1.46	0.58	0.88	0.608409
7697	8000	8000	8000	241.64	239.29	238.87	239.9333	1.706667	0.643333	1.063333	0.711309
7697	8000	8000	8000	241.64	239.29	238.87	239.9333	1.706667	0.643333	1.063333	0.711309
6596	6000	6000	6000	241.43	239.39	239.09	239.97	1.46	0.58	0.88	0.608409
5492	6000	6000	6000	241.2	239.39	239.17	239.92	1.28	0.53	0.75	0.533511
4376	4000	4000	4000	240.6	239.48	239.18	239.7533	0.846667	0.273333	0.573333	0.353141
3242	4000	4000	4000	240.09	239.39	239.24	239.5733	0.516667	0.183333	0.333333	0.215661
2072	2000	2000	2000	239.68	239.48	239.35	239.5033	0.176667	0.023333	0.153333	0.073764
851	2000	2000	2000	239.44	239.49	239.41	239.4467	0.006667	0.043333	0.036667	0.018097
110	0	0	0	239.61	239.53	239.55	239.5633	0.046667	0.033333	0.013333	0.01948
228	0	0	0	238.39	239.53	239.53	239.15	0.76	0.38	0.38	0.317792

Dynamic Load with dynamic PV with Balanced load

Dynamic Load with dynamic PV with Unbalanced load at same phase

PV	unbalanc	e lo	ad	Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
145	0	0	0	238.34	239.48	239.48	239.1	0.76	0.38	0.38	0.317859
110	0	0	0	239.61	239.53	239.55	239.5633	0.046667	0.033333	0.013333	0.01948
851	2000	0	0	239.51	239.55	239.55	239.5367	0.026667	0.013333	0.013333	0.011133
2072	2000	0	0	239.81	239.52	239.56	239.63	0.18	0.11	0.07	0.075116
3242	4000	0	0	240.25	239.56	239.55	239.7867	0.463333	0.226667	0.236667	0.193227
4376	4000	0	0	240.43	239.52	239.53	239.8267	0.603333	0.306667	0.296667	0.251571
5492	6000	0	0	241.04	239.48	239.61	240.0433	0.996667	0.563333	0.433333	0.415203
6596	6000	0	0	241.58	239.6	239.49	240.2233	1.356667	0.623333	0.733333	0.564752
7697	8000	0	0	241.8	239.49	239.63	240.3067	1.493333	0.816667	0.676667	0.621428
7697	8000	0	0	241.85	239.47	239.58	240.3	1.55	0.83	0.72	0.645027
6596	6000	0	0	241.21	239.59	239.5	240.1	1.11	0.51	0.6	0.462307
5492	6000	0	0	240.9	239.52	239.57	239.9967	0.903333	0.476667	0.426667	0.376394
4376	4000	0	0	240.55	239.54	239.56	239.8833	0.666667	0.343333	0.323333	0.277913
3242	4000	0	0	240.33	239.56	239.54	239.81	0.52	0.25	0.27	0.216838
2072	2000	0	0	239.71	239.52	239.53	239.5867	0.123333	0.066667	0.056667	0.051478
851	2000	0	0	239.41	239.54	239.53	239.4933	0.083333	0.046667	0.036667	0.034796
110	0	0	0	239.61	239.53	239.55	239.5633	0.046667	0.033333	0.013333	0.01948

228 0 0 0 238.4 239.53 239.53 239.1533 0.753333 0.376667 0.376667	0.315
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PV	un	balance	e load	Va	Vb	Vc	Vage	Vdev a	Vdev b	Vdev c	%VUF
145	0	0	0	238.33	239.47	239.47	239.09	0.76	0.38	0.38	0.317872
110	0	0	0	239.61	239.53	239.55	239.5633	0.046667	0.033333	0.013333	0.01948
851	0	2000	2000	239.53	239.48	239.4	239.47	0.06	0.01	0.07	0.029231
2072	0	2000	2000	239.98	239.47	239.33	239.5933	0.386667	0.123333	0.263333	0.161385
3242	0	4000	4000	240.32	239.46	239.09	239.6233	0.696667	0.163333	0.533333	0.290734
4376	0	4000	4000	240.94	239.43	239.03	239.8	1.14	0.37	0.77	0.475396
5492	0	6000	6000	241.4	239.31	238.88	239.8633	1.536667	0.553333	0.983333	0.640643
6596	0	6000	6000	241.95	239.45	238.7	240.0333	1.916667	0.583333	1.333333	0.7985
7697	0	8000	8000	242.24	239.33	238.53	240.0333	2.206667	0.703333	1.503333	0.919317
7697	0	8000	8000	242.24	239.38	238.38	240	2.24	0.62	1.62	0.933333
6596	0	6000	6000	242.08	239.45	238.61	240.0467	2.033333	0.596667	1.436667	0.847058
5492	0	6000	6000	241.58	239.48	238.86	239.9733	1.606667	0.493333	1.113333	0.669519
4376	0	4000	4000	240.91	239.5	239.02	239.81	1.1	0.31	0.79	0.458696
3242	0	4000	4000	240.29	239.41	239.1	239.6	0.69	0.19	0.5	0.28798
2072	0	2000	2000	239.84	239.49	239.25	239.5267	0.313333	0.036667	0.276667	0.130814
851	0	2000	2000	239.62	239.45	239.46	239.51	0.11	0.06	0.05	0.045927
110	0	0	0	239.61	239.53	239.55	239.5633	0.046667	0.033333	0.013333	0.01948
228	0	0	0	238.39	239.53	239.53	239.15	0.76	0.38	0.38	0.317792

Dynamic Load with dynamic PV with unbalanced load at difference phase