CIRCUIT UNDER PAD PROGRAMMABLE AND SLEW RATE CONTROLLED OUTPUT BUFFER DESIGN

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CIRCUIT UNDER PAD PROGRAMMABLE AND SLEW RATE CONTROLLED OUTPUT BUFFER DESIGN

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A project report submitted in partial fulfilment of the requirements for the award of the degree of Bachelor of Engineering (Hons) Electronic Engineering

Faculty of Engineering and Green Technology
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DECLARATION

I hereby declare that this project report is based on my original work except for citations and quotations which have been duly acknowledged. I also declare that it has not been previously and concurrently submitted for any other degree or award at UTAR or other institutions.

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APPROVAL FOR SUBMISSION

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CIRCUIT UNDER PAD PROGRAMMABLE AND SLEW RATE CONTROLLED OUTPUT BUFFER DESIGN

ABSTRACT

The use of resistive, capacitive or inductive external loads will make the integrated circuits more susceptible to the output ringing problem if more than one output is switching simultaneously. In order to reduce this signal swing problem, limitation of the maximum rate of change of output voltage, which is also known as output slew rate, is preferred. Therefore, the purpose of this study is to design the output buffer as an interface between the integrated circuit and external loads for controlling the slew rate with slow, mid-range and fast slew rate design. The output buffer with slew rate controlled must act fast enough to meet the speed requirement of the system while minimizing the noise problems. Besides, the output loading condition may vary for different types of applications. This introduces different drive strengths used to drive different capacitive loads. In view of this, the project is also focusing on the design of output buffer such that it is featured with programmable drive strength to enable the users to select the desired operating mode that best suits their applications. The drive strength capability is designed for 2-mA, 4-mA, 6-mAand 8-mA. The designs are featured with circuit under pad structure and using SilTerra C18G process with 0.18µm low power process technology. The performances of C.U.P. programmable and slew rate controlled output buffers are evaluated.

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LIST OF SYMBOLS / ABBREVIATIONS

V_{GS}	gate-to-source voltage, V
V_{THN}	NMOS threshold voltage, V
V_{THP}	NMOS threshold voltage, V
V_{DS}	drain-to-source voltage, V
I_D	drain current, mA
SR	slew rate, V/μs
f	signal frequency, Hz
V_p	peak output voltage, V
L	inductance, mH
$\frac{di}{dt}$	rate of current change, mA/μs
C	capacitance, pF
K	trans-conductance parameter
C'_{ox}	oxide capacitance per area, F/cm^2
μ_n	mobility of electron
μ_p	mobility of hole
W	width of the transistor, μm
P	power dissipated, W
R	resistance value, Ω

CMOS	complementary metal oxide semiconductor
NMOS	n-channel metal oxide semiconductor
PMOS	p-channel metal oxide semiconductor
PCB	printed circuit board
DC	direct current
GND	ground
IC	integrated circuit

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CHAPTER 1

INTRODUCTION

1.1 Background of Study

According to Moore's law, the invention of transistor caused the occurrence of semiconductor miniaturization trajectory where the density of components per area was increased at reduced cost. Gordon Moore observed that the number of transistors on a single microchip of the lowest manufacturing cost was doubling every 18 months and this pace would likely continue into the near future. In view of this, the phenomenon led to the small scale integrated circuit (SSI) in the late-1950s, soon followed by medium scale integration (MSI) of the mid-1960s, then large scale integration (LSI) of the early-1970s, very large scale integration (VLSI) of the 1980s and ultra large scale integration (ULSI) of the 1990s (Schaller, 1996).

Output buffers are found important in those integrated circuits (IC) to provide an interface for driving resistive, capacitive or inductive external loads. A resistive load is normally a pull-up or pull-down resistor on a bus line. The capacitive load is generally comprised of the gate-to-channel input capacitance and parasitic capacitance due to the pin, bonding wire and conductor on the printed circuit board (PCB). On the other hand, inductive load is usually the parasitic inductance formed by the power and ground line of the output buffer with the external power source and ground rail on the PCB (Garcia *et al.*, 1998).

However, these types of loads will make the ICs more susceptible to the output ringing problem, such as voltage spikes on the power line or ground bounces, if more

than one output is switching simultaneously. The magnitude of power noise will then have a significant impact on the circuit operation and performance. In order to reduce the signal swing, limitation of the maximum rate of change of output voltage, which is also known as output slew rate, is preferred. There are many papers published about the design of slew rate controlled output buffer. A simple approach is to use resistor or capacitor to slow down the turn-on time of the output buffer. Nonetheless, this solution increases the propagation delay and larger area is required (Garcia *et al.*, 1998). Therefore, a full standard CMOS transistor circuit that can act as a slew rate controlled output buffer is proposed.

Besides, there is always a need for different drive strengths used to drive capacitive loads based on the preferences of the user. Higher drive strength is needed to drive several loads and eliminate the use of external buffers while lower drive strength improves the signal integrity and reduces electromagnetic interference (SiTime, 2015). Therefore, most of the input/output (I/O) standards in today's fast-paced design world comprised of the programmable drive strength feature for all single-ended drivers. It enables the users to select the preferable drive strength and achieve their design goals more effectively. In view of this, an output buffer that is capable of providing different drive strengths is proposed to meet the requirements of the users.

1.2 Problem Statement

As CMOS IC technology approaches sub-micron process, the slew rate of the output buffer with unacceptable current spikes during the simultaneous switching of many output buffers can no longer be ignored. This issue presents challenges for I/O designers. Therefore, the purpose of this study is to design the output buffer for controlling the slew rate.

Besides, the output loading condition may vary for different types of applications. This becomes interesting if the output buffer is featured with programmable drive strength that enables the users to select the operating mode that best suits their

applications. In view of this, the output buffer is also designed such that it is capable of operating in either a 1.8V or 3.3V environment, with programmable drive strength capability of 2-mA, 4-mA, 6-mA and 8-mA.

The designs of the output buffers are based on the literature and information that are published and in public domain. These designs are featured with circuit under pad (C.U.P.) structure and using SilTerra C18G process with 0.18µm low power process technology. HSPICE and Custom WaveView tool featured in Synopsys will be used to implement the designs. Also, Cadence Virtuoso tool is used with the target to improve the reliability and flexibility of the circuit performance. This work is in collaboration with Shanghai SZGC and using their license for the tool.

1.3 Goal and Objectives

The overall goal of this project is to work on the output buffers for circuit improvement.

The objectives of this work are: -

i. To design the C.U.P. slew rate controlled output buffer to solve the problem of unacceptable current spikes during the simultaneous switching of many output buffers.
ii. To design the C.U.P. programmable drive strength output buffer to drive different loads.
iii. To compare the performance of the C.U.P. output buffers without programmable drive strength and slew rate controlled with the C.U.P. programmable and slew rate controlled output buffers.

1.4 Project Outcomes

The outcomes of this project are:

i. The slew rate of the output buffer is controlled such that the resulting transition time is constant over a large range of output switching condition.
ii. A low noise design is achieved in which the problems of simultaneous switching noise (SSN) and output ringing are minimized.
iii. The output buffer is capable to operate in different drive strengths capability.
iv. The performances of the circuits are improved by the designs of programmable drive strength and slew rate controlled output buffers.

1.5 Outline of Report

1.5.1 Introduction

Chapter 1 consists of background of study, problem statement, goal and objectives as well as the project outcomes. In fact, the background of study is to describe the focus of this project and some relevant issues related to it. Then, problem statement will clarify the scope of the project with the technology process used. It is followed by the section of goal and objectives to identify the strategies or implementation steps that used to achieve the focus of the project. The project outcomes are listed to declare the results and achievements of the project. Lastly, the outline of report illustrates on the order of the topics.

1.5.2 Literature Review

Chapter 2 covers the literature review of the project. The information related to the area of study are gathered, summarized and evaluated to give a theoretical base for the research.

1.5.3 Methodology

The methodology of Chapter 3 describes the methods and particular procedure adopted in this project for the design work. This includes the flowchart and project milestone.

1.5.4 Results and Discussions

Chapter 4 will discuss the results obtained from the simulation. Result analysis will be performed and compared in this chapter.

1.5.5 Conclusion and Recommendation

The last chapter concludes all the task performed and result obtained. This chapter will clarify again the outcomes of the project. Also, some recommendations are suggested for future work.

CHAPTER 2

LITERATURE REVIEW

2.1 Device Structure and Physical Operation of Buffer

2.1.1 n-channel MOSFET

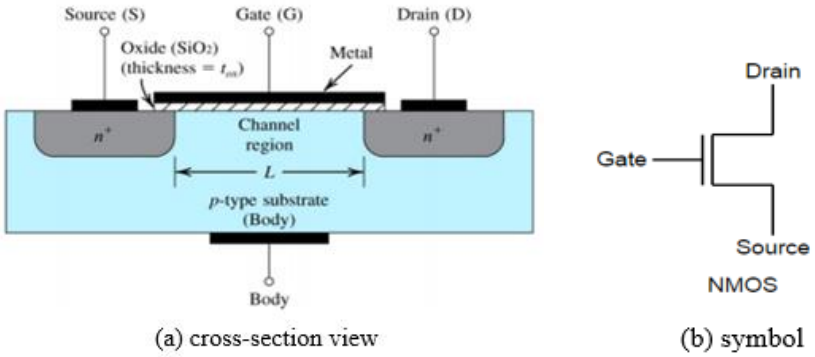
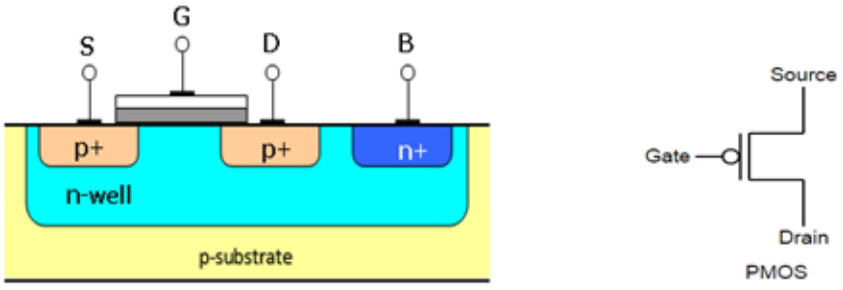


Figure 2.1: Physical structure and symbol of the enhancement-type NMOS transistor

An n-channel metal oxide semiconductor field effect transistor (n-MOSFET or NMOS) is a four terminal device of source (S), gate (G), drain (D) and body substrate (B). The source and drain are two heavily doped n-type regions implanted into a moderately doped p-type substrate. There is a narrow region called the channel, formed between these two regions. The typical value for channel length is in the range of 0.1µm to 3µm with the width of 0.2µm to 100µm (Stiles, 2008). A thin insulating layer of silicon dioxide (SiO_2) is grown on the surface substrate to cover the channel. The poly-silicon, or gate electrode, rests on top of the oxide layer and therefore, there is essentially zero DC current flowing from the gate to channel.

In operation, the flow of electrons from the source to drain is regulated by the voltage applied to the gate. When a positive voltage with respect to the source and the substrate is applied to the gate (V_{GS}), an electric field is generated across the substrate and free electrons are attracted towards the interface between the gate oxide and the semiconductor. If the gate voltage is sufficiently larger than the threshold voltage (V_{THN}), such that $V_{GS}>V_{THN}$, the electric field is strong enough to induce a conducting channel between the source and the drain. Then, a small positive drain-to-source voltage (V_{DS}) will cause the drain current (I_D) to flow through the induced channel and the NMOS is conducting now (Weste, 1993, p.43).

2.1.2 p-channel MOSFET



(a) cross-section view (b) symbol

Figure 2.2: Physical structure and symbol of the enhancement-type PMOS transistor

A p-channel metal oxide semiconductor field effect transistor (p-MOSFET or PMOS) is fabricated similarly to the NMOS. The only difference is it contains p-type source and drain regions in the n-well, and is fabricated on a p-substrate. This yields a p-type channel between the source and drain regions when the hole carrier are attracted to the surface of semiconductor by a negative gate voltage. Since the threshold voltage (V_{THP}) for a PMOS is negative, the gate voltage with respect to the source (V_{GS}) must be more negative than threshold voltage ($V_{GS}<V_{THP}$) to induce the conduction path. Then, a negative drain voltage (V_{DS}) causes the holes to flow from the source to the drain through the channel, resulting in a negative drain current (I_D).

2.1.3 Complementary MOSFET

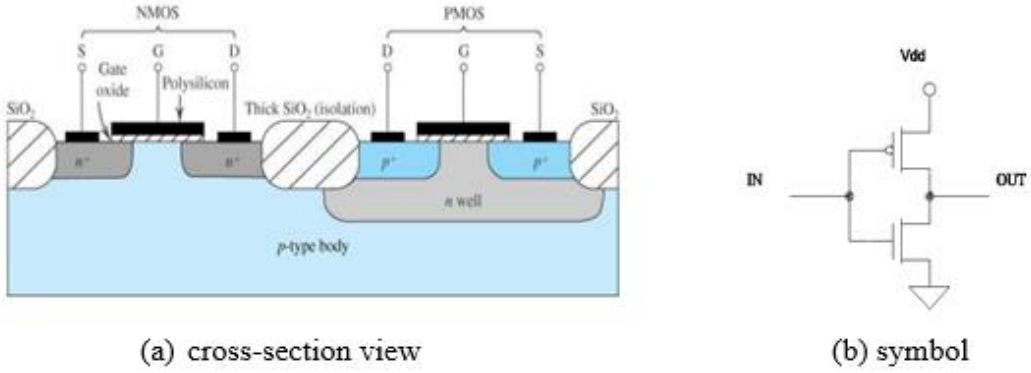


Figure 2.3: Physical structure and symbol of the CMOS transistor

By combining both of the NMOS and PMOS transistors, a complementary metal oxide semiconductor field effect transistor (CMOS) is formed as shown in Figure 2.3. The substrate and the well will be connected to the voltage which reverse bias the p-n junctions for device isolation. Also, a thick region of SiO_2 that functions as an insulator is used to isolate the PMOS from NMOS. The following table is used to derive the DC-transfer characteristics for the CMOS (Weste, 1993, p.62). Both gates of the PMOS and NMOS transistors are connected to a single input line while the output line links the drains of both transistors together.

Table 2.1: Various Operations of the NMOS and PMOS to form a CMOS

	Cutoff region (off)	**Linear region (lin)**	**Saturation region (sat)**
PMOS transistor	$V_{GS}>V_{THP}$	$V_{GS}<V_{THP}$ $V_{IN}<V_{THP}+V_{DD}$	$V_{GS}<V_{THP}$ $V_{IN}<V_{THP}+V_{DD}$
	$V_{IN}>V_{THP}+V_{DD}$	$V_{DS}>V_{GS}-V_{THP}$ $V_{OUT}>V_{IN}-V_{THP}$	$V_{DS}<V_{GS}-V_{THP}$ $V_{OUT}<V_{IN}-V_{THP}$
NMOS transistor	$V_{GS}<V_{THN}$	$V_{GS}>V_{THN}$ $V_{IN}>V_{THN}$	$V_{GS}>V_{THN}$ $V_{IN}>V_{THN}$
	$V_{IN}<V_{THN}$	$V_{DS}<V_{GS}-V_{THN}$ $V_{OUT}<V_{IN}-V_{THN}$	$V_{DS}>V_{GS}-V_{THN}$ $V_{OUT}>V_{IN}-V_{THN}$

Based on the table, the relationship between the output (V_{OUT}) and input (V_{IN}) of the CMOS can be illustrated as in Figure 2.4. The CMOS simply works as an inverter by noting that V_{OUT} is inversely proportional to V_{IN}. High V_{IN} will result in low V_{OUT} while low V_{IN} gives high $V_{OUT.}$

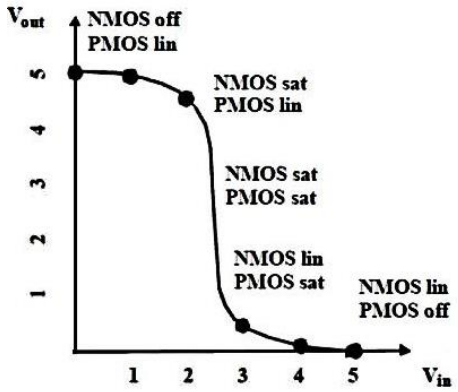


Figure 2.4: Transfer function of CMOS transistor

By cascading two CMOS together such that the output from one CMOS is fed into the input of another CMOS, the double inversion functions will cancel out each other and thus, V_{OUT} follows the value of V_{IN}. This forms a buffer, which is used to boost the signal or introduce delay in the circuit. Sometimes, the signal starts to degrade after travelling through a certain distance inside the circuit. Such degradation may cause error or noisy output and therefore, signal needs boosting. A weak signal source can be boosted by means of buffer. The logic level is unchanged, but the capability of current sourcing or sinking is now sufficient to drive the output load. Figure 2.5 shows the symbol and characteristics of a basic buffer. In the case of this study, a buffer functions as an isolation between two different circuitries to eliminate the unwanted noise problems.

Input	Output
0	0
1	1

Figure 2.5: Symbol and characteristics of a basic buffer

The CMOS technology consumes less power while producing the designed function with less noisy output. It becomes the fundamental to construct any logic gate. For example, NAND or NOR gates can be used to create a buffer too. However, a full NAND or NOR buffer implementation requires total of 8 transistors while the inverter design only uses 4 transistors. Larger number of transistors means to increase the circuit area. For this reason, the CMOS inverter is preferred in the design of the buffer (Barnes, 2009).

2.2 System on a Chip

The rapid scaling of CMOS technology with the advanced chip manufacturing process gives rise to the System on a Chip (SoC). SoC refers to the integration of multiple components with different functionalities, such as main processor, memories, interfaces, timers, converters or amplifiers, embedded on a single chip (Von Rosen *et al.*, 2015). While a computer has all the mentioned components connected together in a motherboard, the SoC technology is used in small and portable electronic devices such as smart phones and tablets. Due to its higher level of integration and shorter wiring, the power consumption of the SoC is also considerably lower compared to that of a computer (Anthony, 2012).

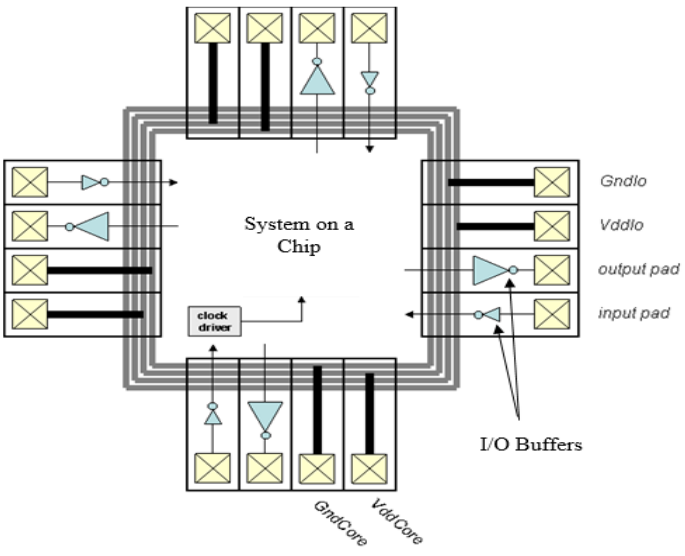


Figure 2.6: Simplified diagram of SoC with the buffers as I/O interface

The design of SoC comprises the hierarchical placement and routing of the components with the power supply and ground distribution networks. External power must be sufficiently supplied to the system through the I/O pad. Also, external clock and I/O data transfer are accessed through the I/O pins. In view of this, buffer provides single ended I/O interface for the SoC to the external devices. Figure 2.6 shows the simplified diagram of SoC with the buffers as I/O interface.

2.3 Controlled Slew Rate Output Buffer

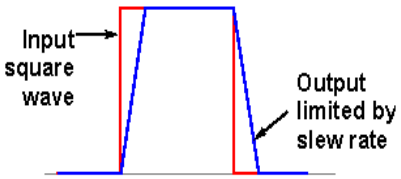


Figure 2.7: Slew rate illustration

In general, the output of a circuit is required to change from one level to another quickly in order to achieve high circuit performance. However, the switching of the output will never be an ideal case in real-life applications due to the limited drive current. The limitation at which the maximum output voltage can change per unit time is called the slew rate, as shown in Figure 2.7. It is a large signal characteristic of amplifiers and drivers, which helps to set the desired rise and fall time of the output with the equation as shown below (Gilbert, 2008). The value of the slew rate must be large enough for the maximum frequency and the voltage amplitude.

$$SR = 2\pi f \times V_p \tag{2.1}$$

where

SR = slew rate, V/μs

f = highest signal frequency, Hz

V_p = peak output voltage, V

With the conventional output buffer architecture, a tapered inverter chain, the transistor sizing is enforced by DC interfacing constraints such as the required driver strength, process, voltage and temperature ranges. Gradually increase in drive capability causes the last inverter to have largest size to drive the external load. This leads to the problem of unacceptable current spikes during the simultaneous switching of many output buffers. When the current passes through the parasitic inductance and capacitance, it subsequently brings out the serious problems of (i) simultaneous switching noise, (ii) output ringing and (iii) electromagnetic interference (Yang and Yuan, 2005).

(i) Simultaneous switching noise (SSN)

When several output buffers are switching simultaneously, the source voltage V_{DD} is dropped in the power distribution while the ground voltage V_{GND} of the internal circuit is raised relative to the system ground. This ground bounce voltage is also known as SSN and is primarily caused by the serial inductance modeled along the transmission line between the power pads of the circuit and the system power supply (Microsemi Corporation, 2012). It is given by the equation as shown below. The ground bounce voltage accumulates in magnitude with the number of simultaneously switching output.

$$V = L\frac{di}{dt} \qquad (2.2)$$

where

V = ground bounce voltage, V

L = inductance, mH

$\frac{di}{dt}$ = rate of current change, mA/μs

(ii) Output ringing

For high drive current capability, the impedance mismatch that resulted from the driving of transmission line with different parasitic impedances by the low impedance output buffer creates unwanted output ringing. Overshoot arises at the rising edge while undershoot occurs at the falling edge. Output ringing degrades the signal waveform and causes the problems of false triggering, missing pulses and

double clocking. Therefore, the effective impedance of the output buffer must be controlled to reduce output ringing problem during the signal transition (Leung, 1988).

(iii) Electromagnetic interference (EMI)

As the switching speed is increased, the output buffer generates faster rise and fall time for the output signal. These fast edges, however, produce a considerable amount of energy at high frequencies that can cause EMI. It is also known as radio frequency interference (RFI), which is a type of disturbance that causes reflection from parasitic impedance onto the transmitting channel. Subsequently, the effective performance of the circuit is degraded (Hesener, 2011). Hence, the output switching edges must be slow down in order to mitigate the effect of EMI.

There are many proposed low noise designs to solve those problems, such as current controlled buffer or slew rate controlled buffer. For current controlled technique, the driving current is kept nearly constant by adjusting the current capability of the pre-driver (Yang and Yuan, 2005). However, the drawback of this method is the increasing of rise time and propagation delay of the buffer. On the other hand, the idea of slew rate controlled buffer is to divide the output stage into several sub-stages that are connected in parallel (Leung, 1988) (Jou*et al.*, 2001). Each stage turns on in sequence by the signal from the pre-driver after some delay. This switching mechanism decreases the slew rate of the output transition and therefore, the impact of noise can be mitigated.

The slew rate must be carefully selected so as to match the output current to the load. Fast slew rate is needed for high speed devices but at the same time, may undergo output ringing problem. Slower slew rate can help to limit the noise problem in many cases but may not reach the desired output level when it needs to. So, the output buffer with slew rate controlled must act fast enough to meet the speed requirement of the system while minimizing the noise problems. When designing the output buffer for certain speed, worst case of process variables, supply voltage and temperature (PVT) are considered.

2.4 Programmable Drive Strength Output Buffer

Drive strength is the capability of current that can be drawn to drive the output loads by changing the output impedance of the buffer. It does not refer to the maximum current or current limit that can be drawn from the buffer, but the current strength that is guaranteed to deliver at the switching thresholds of an I/O standard (Cook, 2015). In general, there are two output drives as illustrated in Table 2.2 (Fairchild Semiconductor, 1998). This output drive characteristics are depending on the environment or output load.

Table 2.2: Types of Output Drives

	Static Output Drive	**Dynamic Output Drive**
Output state	Not switching	Switching
Output current capacity	Available at steady state to maintain a DC voltage level of an output.	Available during the switching or transition of an output to provide sufficient switching strength for loaded environment.
Applications	Useful in applications that use resistive termination solutions.	Useful in applications to define the switching speed of a device.

The output load is normally comprised of the capacitive load, with the equation as shown below:

$$I = C\frac{dv}{dt} \tag{2.3}$$

where

I = output current, mA

C = capacitance, pF

$\frac{dv}{dt}$ = rate of output voltage change, V/μs

For smaller load capacitance, smaller drive strength is needed. On the other hand, greater drive strength is required for larger capacitive load, so that higher current can be drawn to the output and fast enough to charge or discharge the load. However, the drive capability of the output buffer is a tradeoff between the leakage and speed. If the drive strength is small, low leakage current is the advantage but the switching current may become too small to drive the load. Subsequently, the signal has not enough time for charging or discharging to reach a valid logic level. The resulting waveform does not swing rail-to-rail. Conversely, higher drive strength can obtain fast edge rates, but causes higher leakage current at the same time. The output signal swing may overshoot or undershoot, causing signal integrity problem (Xilinx, 2014). Therefore, it is important to consider the tradeoff in order to select the appropriate drive strength based on the load.

One of the techniques to increase the drive strength in programmable output buffer design is to increase the $\frac{W}{L}$ ratio. The current of an output buffer is directly proportional to the size of the transistor ($I \propto \frac{W}{L}$) as can be seen in the current-voltage equations below for both NMOS and PMOS (Sharma, 2013):

$$I_{D(LINEAR)} = \frac{K}{2} . \frac{W}{L} . [2 . (V_{GS} - V_T)V_{DS} - V_{DS}^2] \quad (2.4)$$

$$I_{D(SATURATION)} = \frac{K}{2} . \frac{W}{L} . [(V_{GS} - V_T)^2 . (1 + \lambda V_{DS})] \quad (2.5)$$

where

I_D = drain current, mA

K = trans-conductance parameter ($\mu_n C'_{ox}$ for NMOS and $\mu_p C'_{ox}$ for PMOS, where μ_n and μ_p is the mobility of electron and hole respectively while C'_{ox} is the oxide capacitance per area)

W = width of the transistor, µm

L = channel length between source and drain regions, µm

V_{GS} = gate-to-source voltage, V

V_T = threshold voltage, V

V_{DS} = drain-to-source voltage, V

In other words, the output current can be increased by increasing the $\frac{W}{L}$ ratio, with channel length (L) limited by the technology while bigger width (W) ensures higher conductivity. However, increases the width of individual transistor resulting in larger diffusion area and taller transistor. This forces the remaining transistors in the same row to follow the same height, which may waste a lot of spaces in the output buffer design (Edaboard, 2006).

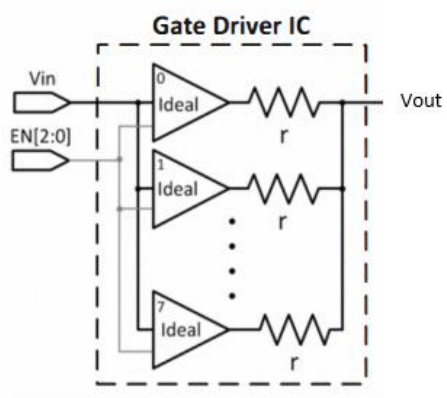


Figure 2.8: Topology of the programmable gate driver circuit

The issue can be solved by connecting multiple transistors in parallel for load adaptability function (Ruetz, 1992) (Schnizlein, 1997). This fingering technique in Figure 2.8 keeps the transistor in fixed size and several transistors are connected in parallel so as to increase the drive strength of the buffer (Ng and Shorten, 2011). The output of each transistor circuit is connected to a common output node of the output buffer. A control signal is then used to enable or disable the output buffers for the selection of weak, medium or strong current drive strength. Higher drive strength means to have more transistor circuits turning on with each output a predetermined amount of current to the common output node. The required drive current are summed up at the output node and delivered to the load. The output buffer architecture is assured with minimum drive strength for each drive setting.

The increase in current strength induces large power and ground noise when the output buffers are switching simultaneously. Therefore, a programmable drive strength output buffer is comprised of the slew rate controlled circuit. For a given

slew rate ($\frac{dv}{dt}$) as in the revised equation 2.3, the output driving capability is selected based on the capacitive load. The slew rate and drive strength are interrelated such that the drive strength indicates how much current is drawn to the load while the slew rate specifies how fast the current is delivered. Together, these two parameters determine the rising and falling time of the output signal (Altera Corporation, 2007).

2.5 Types of Output Buffers

The designs of programmable drive strength and slew rate controlled output buffer in this project are using 0.18µm low power process technology with the top metal layer of 5. The output buffer cells with 2-mA, 4-mA and 8-mA outputs provided in SilTerra C18G process are listed in Table 2.3. For the driver function, **OE** represents output enable, **In** represents data input and **P** represents pad. All of the output buffers have the same height and width, which is 210µm and 70µm respectively.

Table 2.3: Types of Output Buffers

Output Buffer	Functional Schematic	Cell Description	Driver Function		
			Input		Output
			OE	In	P
UTOC2A		2-mA direct output and output slew rate A.		0 1	0 1
UTOC4A		4-mA direct output and output slew rate A.		0 1	0 1
UTOC8A		8-mA direct output and output slew rate A.		0 1	0 1
UTOC8B		8-mA direct output and output slew rate B.		0 1	0 1
UTOC8C		8-mA direct output and output slew rate C.		0 1	0 1

The slew rate A, B and C have the functions as shown in Table 2.4.

Table 2.4: Types of Slew Rates

Slew Rate	Description
A	Slowest slew rate, low-noise pad.
B	Mid-range slew rate, medium-noise pad.
C	Highest slew rate, high-noise pad.

The buffers have the typical operating voltage conditions of 1.8V core supply and 3.3V I/O supply, with the voltage tolerance of 5V. The voltage across any two junction of an MOS transistor should never exceed 3.6V. This circuit is subjected to electrostatic discharge (ESD) if the voltage peak reaches a few kV during testing and handling. In view of this, a proper ESD protection circuit is provided in the output buffer cells.

2.6 Circuit under Pad (C.U.P.)

With the increasing of I/O pins in today's high performance SoC designs and the decreasing of die size without adding layers or manufacturing costs, the I/O ring designs and bond placements become more complicated. The area occupied by these bonding pads is getting bigger and therefore, a circuit under pad (C.U.P.) structure is investigated to shrink the chip size (Chen and Cheng, 2014). This technique arranges the ESD protection circuit and pad circuitry under the bonding pad to ensure that there is no additional space consumed on the die. However, the circuit would easily suffer extra mechanical stress during circuit probing and packaging processes. Extra care is needed such that the bonding and probing region are not overlapping to each other to reduce the pounding effect on the C.U.P. structure (Su*et al.*, 2007).

CHAPTER 3

METHODOLOGY

3.1 Project Overview

In this project, the C.U.P. output buffers listed in Table 2.3 are chosen in a selective manner to execute the designs of programmable drive strength and slew rate controlled. Due to the physical constraint, such as fixed size of transistors, the programmable drive strength and slew rate controlled output buffers are designed in separate ways. Otherwise, the design will consume a large amount of space, which is contradicting to the miniaturization of the IC chip market. The tools used for the simulation are HSPICE and Custom WaveView featured in Synopsys while Cadence Virtuoso is used for the implementation of the designs. Both of the software can be run in the CentOS Linux platform. In order to succeed, the project task has been well-planned and divided into several phases.

Phase 1: Go through the software training materials

The training materials and laboratory exercises for Synopsys tools are used to get familiar with the software environment and acquire the skills in simulating and debugging the designs, such as Synopsys VCS and Custom Designer. In the beginning, Custom Designer tool is planned to use for the project design. However, the foundry prefers to use Cadence Virtuoso and therefore, the designs of output buffers are shifted to the use of Cadence Virtuoso, which is also a platform for IC design and simulation.

Phase 2: Literature survey

Relevant information is reviewed and analyzed initially through the online public access catalog (OPAC) system of university library and Internet search engines. Self-knowledge is acquired and enhanced from the books, journal papers, datasheets and articles. To aid the search, several key words such as “design of slew rate controlled output buffer”, “design of programmable drive strength output buffer” and “circuit under pad” are formed and the range of information sources will be correlated with these terms.

Phase 3: Study the schematics and layouts of current buffer cells

Instead of schematic diagrams, only Spice netlist in .cdl format are provided. Therefore, the schematic diagrams of the output buffers are drawn manually based on the corresponding Spice netlist to have a better view in the transistors’ connections. The input stage, voltage level shifter and the output stage of the buffer are identified. In view of this, a selective study is performed to examine the schematics and layouts of current buffer cells. Output buffers in Table 2.3 will be concerned only in the case of the project study while the rest with drive strength greater than 8-mA will be ignored, due to the very large current capability that are not applicable to the design task.

The function of each output buffer is understood, including the ESD protection, use of the transistor model and various process layers from metal layer 1 to top metal layer 5 in the layout. The PMOS and NMOS transistors used for 1.8V are different from the transistors used for 3.3V. Also, metal layer 1 to metal layer 3 are generally used for routing purpose while metal layer 4 and top metal layer 5 serve as power bus. Although only the top metal layer 5 is needed to form the connection with the bonding wire, the bonding pad is actually created from all the metal layers stacked on top of each other and interconnected through appropriate vias. This arrangement gives rise to the connection from the core of a chip to the bonding pad and in turn, the outside world.

Phase 4: Study the C.U.P. modifications for buffer cells

The C.U.P. modifications are studied for the more standard output buffer cells. The layouts of the output buffers in the C.U.P. structure are compared with the current output buffers without C.U.P. modification. With the structure of C.U.P., the buffers have the advantage of more number of I/O can be used with optimal area utilization. HSPICE simulation is performed for both output buffers with and without C.U.P structure to observe any difference in the waveforms. Also, the C.U.P. output buffers are simulated to model all the best case and worst case corners of PVT. These are the environmental attributes that affecting the accuracy of design modeling. For typical case, the process used is typical PMOS and NMOS devices (tt). It is associated with the core supply voltage of 1.8V, I/O supply of 3.3V and room temperature of 27°C as shown in Figure 3.1.

```
******** Define Variables *********************************
.param v18 = 1.8
.param v33 = 3.3

.temp   27
.LIB "/home/cad/Synopsys/Silterra_new_pdk_mar15/models/hspice/c18e_core18_io33_header_hspice.modlib" c18e_hp_tt
.LIB "/home/cad/Synopsys/Silterra_new_pdk_mar15/models/hspice/c18e_core18_io33_header_hspice.modlib" c18e_to_tt
.LIB "/home/cad/Synopsys/Silterra_new_pdk_mar15/models/hspice/c18e_core18_io33_header_hspice.modlib" c18e_nat_tt
.LIB "/home/cad/Synopsys/Silterra_new_pdk_mar15/models/hspice/c18e_core18_io33_header_hspice.modlib" c18e_mvt_tt
.LIB "/home/cad/Synopsys/Silterra_new_pdk_mar15/models/hspice/c18e_core18_io33_header_hspice.modlib" c18e_nvar_tt
.LIB "/home/cad/Synopsys/Silterra_new_pdk_mar15/models/hspice/c18e_core18_io33_header_hspice.modlib" c18e_res_tt
.LIB "/home/cad/Synopsys/Silterra_new_pdk_mar15/models/hspice/c18e_core18_io33_header_hspice.modlib" c18e_diode_tt
.LIB "/home/cad/Synopsys/Silterra_new_pdk_mar15/models/hspice/c18e_core18_io33_header_hspice.modlib" c18e_mim_cap_tt
.LIB "/home/cad/Synopsys/Silterra_new_pdk_mar15/models/hspice/c18e_core18_io33_header_hspice.modlib"
c18e_finger_cap_tt
.LIB "/home/cad/Synopsys/Silterra_new_pdk_mar15/models/hspice/c18e_core18_io33_header_hspice.modlib" c18e_bjt_tt
```

Figure 3.1: Part of the HSPICE script for typical case simulation

On the other hand, the best case PVT analysis requires fast process (ff), maximum core supply and I/O supply of 1.98V and 3.63V and temperature of -40°C as shown in Figure 3.2. The maximum voltage is obtained from +10% of the nominal value.

```
******** Define Variables *********************************
.param v18 = 1.98
.param v33 = 3.63

.temp -40
.LIB "/home/cad/Synopsys/Silterra_new_pdk_mar15/models/hspice/c18e_core18_io33_header_hspice.modlib" c18e_hp_ff
.LIB "/home/cad/Synopsys/Silterra_new_pdk_mar15/models/hspice/c18e_core18_io33_header_hspice.modlib" c18e_to_ff
.LIB "/home/cad/Synopsys/Silterra_new_pdk_mar15/models/hspice/c18e_core18_io33_header_hspice.modlib" c18e_nat_ff
.LIB "/home/cad/Synopsys/Silterra_new_pdk_mar15/models/hspice/c18e_core18_io33_header_hspice.modlib" c18e_mvt_ff
.LIB "/home/cad/Synopsys/Silterra_new_pdk_mar15/models/hspice/c18e_core18_io33_header_hspice.modlib" c18e_nvar_min
.LIB "/home/cad/Synopsys/Silterra_new_pdk_mar15/models/hspice/c18e_core18_io33_header_hspice.modlib" c18e_res_min
.LIB "/home/cad/Synopsys/Silterra_new_pdk_mar15/models/hspice/c18e_core18_io33_header_hspice.modlib" c18e_diode_ff
.LIB "/home/cad/Synopsys/Silterra_new_pdk_mar15/models/hspice/c18e_core18_io33_header_hspice.modlib"
c18e_mim_cap_min
.LIB "/home/cad/Synopsys/Silterra_new_pdk_mar15/models/hspice/c18e_core18_io33_header_hspice.modlib"
c18e_finger_cap_min
.LIB "/home/cad/Synopsys/Silterra_new_pdk_mar15/models/hspice/c18e_core18_io33_header_hspice.modlib" c18e_bjt_min
```

Figure 3.2: Part of the HSPICE script for best case PVT simulation

This is followed by the worst case corner of PVT, which requires slow PMOS and NMOS devices (ss) for the process, minimum core supply voltage of 1.62V, minimum I/O supply of 2.97V and highest temperature of 125°C as shown in Figure 3.3. The minimum voltage is obtained from -10% of the nominal value.

```
******** Define Variables *********************************
.param v18 = 1.62
.param v33 = 2.97

.temp 125
.LIB "/home/cad/Synopsys/Silterra_new_pdk_mar15/models/hspice/c18e_core18_io33_header_hspice.modlib" c18e_hp_ss
.LIB "/home/cad/Synopsys/Silterra_new_pdk_mar15/models/hspice/c18e_core18_io33_header_hspice.modlib" c18e_to_ss
.LIB "/home/cad/Synopsys/Silterra_new_pdk_mar15/models/hspice/c18e_core18_io33_header_hspice.modlib" c18e_nat_ss
.LIB "/home/cad/Synopsys/Silterra_new_pdk_mar15/models/hspice/c18e_core18_io33_header_hspice.modlib" c18e_mvt_ss
.LIB "/home/cad/Synopsys/Silterra_new_pdk_mar15/models/hspice/c18e_core18_io33_header_hspice.modlib" c18e_nvar_max
.LIB "/home/cad/Synopsys/Silterra_new_pdk_mar15/models/hspice/c18e_core18_io33_header_hspice.modlib" c18e_res_max
.LIB "/home/cad/Synopsys/Silterra_new_pdk_mar15/models/hspice/c18e_core18_io33_header_hspice.modlib" c18e_diode_ss
.LIB "/home/cad/Synopsys/Silterra_new_pdk_mar15/models/hspice/c18e_core18_io33_header_hspice.modlib"
c18e_mim_cap_max
.LIB "/home/cad/Synopsys/Silterra_new_pdk_mar15/models/hspice/c18e_core18_io33_header_hspice.modlib"
c18e_finger_cap_max
.LIB "/home/cad/Synopsys/Silterra_new_pdk_mar15/models/hspice/c18e_core18_io33_header_hspice.modlib" c18e_bjt_max
```

Figure 3.3: Part of the HSPICE script for worst case PVT simulation

Phase 5: Extract parasitic of the modified C.U.P.output buffers

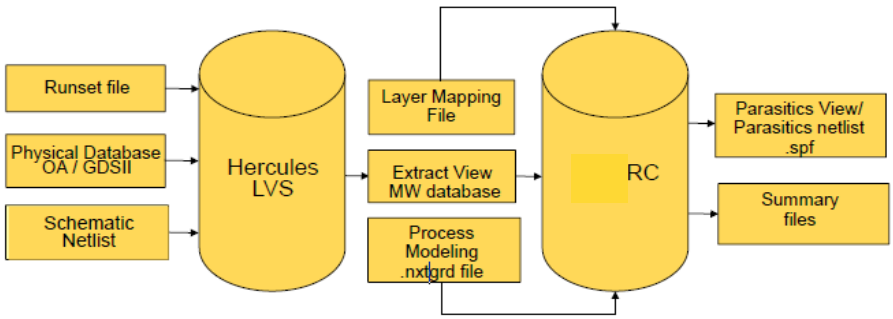


Figure 3.4: RC extraction flow

RC extraction is performed to extract the parasitic devices from layouts of the modified C.U.P. output buffers. Parasitic are unintentional devices of resistors, capacitors and inductors that are not schematic in the design. The extraction of RC parasitic can only be done if the layout design is clean from all violations. Then, the design is back annotated for netlist simulations and static time analysis (STA) where the propagation delay values are calculated for the cells in the netlist. All data path delays are checked against the timing constraints to ensure that if the constraints have

been met. By generating the parasitic netlist, HSPICE simulation is performed again to observe the difference in the waveforms.

Phase 6: Perform testing on the ready chip with C.U.P. structure

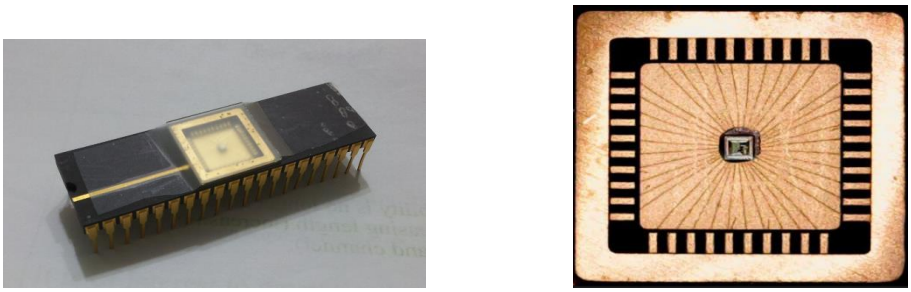


Figure 3.5: Ready chip with C.U.P. structure and the microscopic picture

In order to experience the whole IC design flow including the fabricated chip testing, some tests are carried out on the ready chip with C.U.P. structure as shown in Figure 3.5. There are two bidirectional I/O buffers (UTCCTU and UTCOC2A) and two input buffers (UTICU and UTICD) inside the chip. The descriptions of the buffers are summarized in Table 3.1 and the pin diagram is shown in Appendix A.

Table 3.1: Descriptions of the Buffers

I/O buffers	I/O types	Descriptions
UTCCTU	UTCCTU_2A input buffer	2-mA input buffer with CMOS input
	UTCCTU_2A output buffer	2-mA 3-state output buffer with pull up pad and slew rate A
	UTCCTU_8A input buffer	8-mA input buffer with CMOS input
	UTCCTU_8A output buffer	8-mA 3-state output buffer with pull up pad and slew rate A
UTCOC2A	UTCOC2A input buffer	2-mA input buffer with CMOS input
	UTCOC2A output buffer	2-mA n-channel open drain output buffer with slew rate A
UTICU	UTICU input buffer	Input buffer with CMOS input
UTICD	UTICD input buffer	Input buffer with CMOS input

First of all, the buffers are tested for the functionality. For input buffers, the input voltage is 3.3V while the output voltage is 1.8V. Conversely, the output buffers require 1.8V as the input voltage and produce 3.3V as the output voltage. The equipment used are listed in Table 3.2.

Table 3.2: Equipment Used for Functionality Testing

Equipment	Model name
DC Power Supply	MEGURO MP303-3 Triple Output DC Power Supply
Digital Multimeter	GW INSTEK GDM-8145 Digital Multimeter

After verifying the functionality, the buffers are tested for measuring the rise and fall time with different capacitor loads. When stimulated by a step input, the rise time is the time taken for the output voltage to rise from 10% to 90% of its final value. Fall time, on the other hand, is defined as the time required for the amplitude of output voltage to fall from 90% to 10% of the peak value. The equipment used are listed in Table 3.3.

Table 3.3: Equipment Used for Rise and Fall Time Measuring

Equipment	Model name
DC Power Supply	MEGURO MP303-3 Triple Output DC Power Supply
Function Generator	GW INSTEK SFG-830 30MHz Arbitrary Function Generator
Digital Storage Oscilloscope	TEKTRONIX TPS2014 Four Channel Digital Storage Oscilloscope 100MHz 1GS/s

The input frequency is set as 3MHz by using the function generator. The circuit connection of the buffer is illustrated in Figure 3.6. **C** refers to different capacitor loads used for investigating the relationship between the capacitor value with the rise and fall time measurement. The capacitor load **C** is increased until the output voltage drops from a fixed value. In other words, the drive strength of the buffer is no longer enough to support the capacitor load at that point.

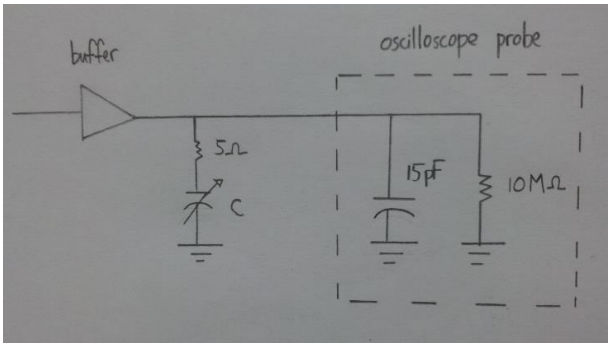


Figure 3.6: Circuit connection of the buffer

Note that an external pull up resistor of 10kΩ is required for UTCOC2A output buffer due to its open drain characteristics. Also, all of the unused pins of the chip must connect to ground as one of the precaution steps. This is demonstrated in Figure 3.7.

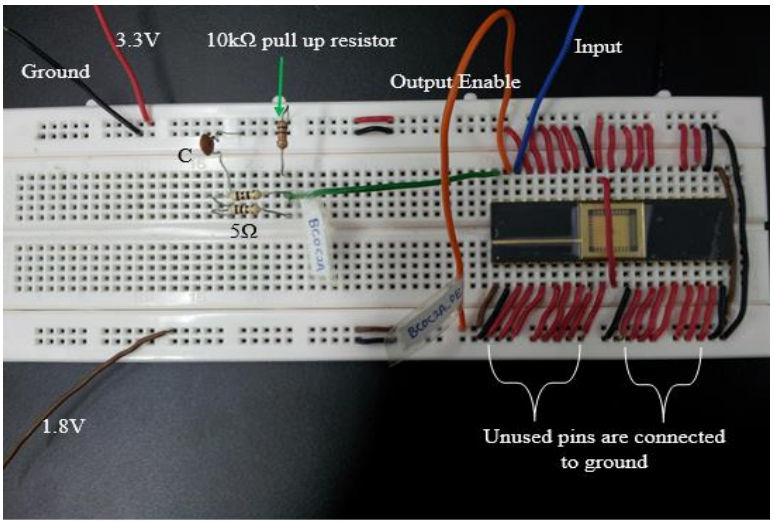


Figure 3.7: Circuit connection for UTCOC2A output buffer

Apart from that, the rise and fall time of the buffers are measured for the best case and worst case corners of PVT with the use of 3MHz input frequency and fixed capacitor value = 25pF (external capacitor of 10pF + intrinsic capacitance of 15pF from the oscilloscope probe). Due to the fixed process corner of the chip, only supply voltage and temperature will be changed for the PVT analysis. Fast corner requires high voltage and low temperature condition while slow corner needs low voltage and high temperature condition.

For fast corner to occur, the core supply voltage and I/O supply are set to 1.98V and 3.63V respectively. Low temperature is generated with the use of thermoelectric cooler in Figure 3.8. A thermoelectric cooler, or Peltier, is a solid state heat pump that creates a temperature differential on each side based on the concept of Peltier effect: by passing an electric current through two junctions, the temperature difference can occur in which one conductor side becomes hotter while the other side becomes cooler. If the current direction is reversed, the cold junction will get hot while the hot junction gets cold (Godfrey, 1996).

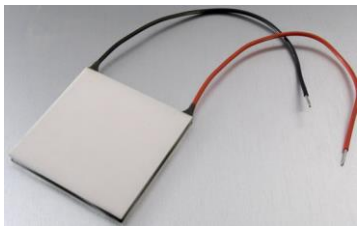


Figure 3.8: Thermoelectric cooler

The hot side of thermoelectric cooler is first attached to the heat sink with the use of thermal paste to remove the heat generated from the hot side when an electric current is applied to it. This is to ensure the cold side of thermoelectric cooler remains cold during the chip measurement. The thermoelectric cooler is tested for the temperature before attached to the chip. With two thermoelectric cooler connected in series, a supply voltage of 19V is found to give a stable minimum chip temperature of 11°C. The setup for generating low temperature condition is shown in Figure 3.9.

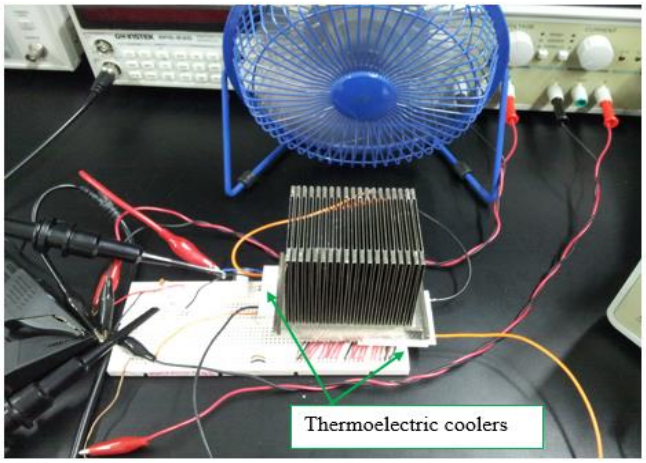


Figure 3.9: Setup for generating low temperature condition

The materials and equipment used are listed in Table 3.4.

Table 3.4: Materials and Equipment for Generating Low Temperature

Materials and Equipment	Model name	Quantity
DC Power Supply	MEGURO MP303-3 Triple Output DC Power Supply	2
Function Generator	GW INSTEK SFG-830 30MHz Arbitrary Function Generator	1
Digital Storage Oscilloscope	TEKTRONIX TPS2014 Four Channel Digital Storage Oscilloscope 100MHz 1GS/s	1
Digital Multimeter	TENMA 72-7730A Intelligent Digital Multimeter	1
Digital Multimeter	PRO'SKIT MT-1217 3 ¾ Auto Range Digital Multimeter	1
Thermoelectric Cooler	LAIRD TECHNOLOGIES ThermaTEC^{TM}Series HT8, 12, F2, 4040	2
Heat Sink	-	1
USB Mini Fan	-	1

On the other hand, for slow corner to occur, the core supply voltage and I/O supply are set to 1.62V and 2.97V respectively. High temperature is generated with the use of high power resistor in Figure 3.10.

Figure 3.10: High power resistor

The power resistor converts power dissipated to heat and increases the temperature of it when the current passes through it. The power dissipated by the power resistor can be found using the equation:

$$P = I^2R \tag{3.1}$$

where

P = power dissipated, W

I = current supplied to the resistor, A

R = resistance value, Ω

The high power resistor is first tested for the temperature before attached to the chip by using extension clamps. The temperature of the resistor will keep increasing until it reaches a point where the heat dissipated through the surrounding environment is same as the heat generated. With two power resistors connected in series that give a total of 20Ω, the supply voltage of 11V and supply current of 0.55A is found to give 6.05W power and a stable chip temperature of 80°C. The setup for generating high temperature condition is shown in Figure 3.11. The breadboard with the chip is covered by a box during the testing period to ensure a stable environmental temperature.

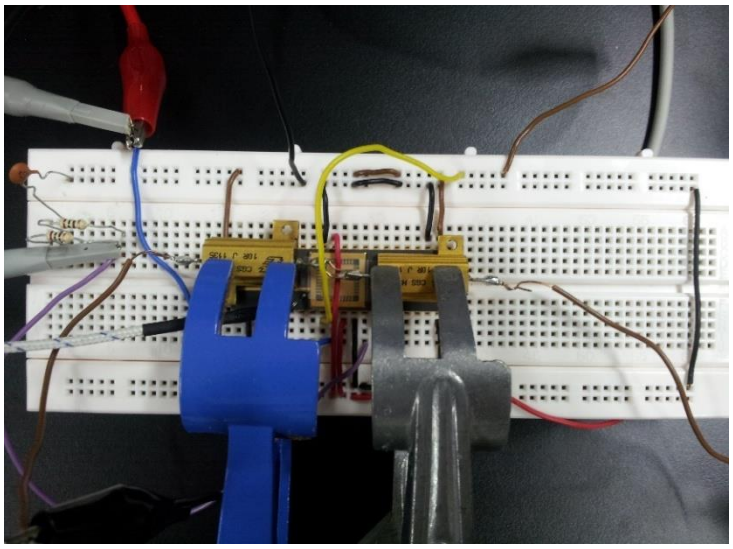


Figure 3.11: Setup for generating high temperature condition

The materials and equipment used are listed in Table 3.5.

Table 3.5: Materials and Equipment for Generating High Temperature

Materials and Equipment	Model name	Quantity
DC Power Supply	MEGURO MP303-3 Triple Output DC Power Supply	2
Function Generator	GW INSTEK SFG-830 30MHz Arbitrary Function Generator	1
Digital Storage Oscilloscope	TEKTRONIX TPS2014 Four Channel Digital Storage Oscilloscope 100MHz 1GS/s	1
Digital Multimeter	TENMA 72-7730A Intelligent Digital Multimeter	1
Digital Multimeter	PRO'SKIT MT-1217 3 ¾ Auto Range Digital Multimeter	1
High Power Resistor	TE CONNECTIVITY CGS HSA10 10R J 1135 Power Resistor	2
Extension clamp	-	2

Besides, three of the output buffers obtained in UTCCTU and UTCOC2A bidirectional I/O buffers are tested with different resistance values for measuring the DC drain current. By measuring the voltage across the resistor, the drain current can be found using Ohm's law:

$$V = IR \tag{3.2}$$

where

V = voltage across the resistor, V

I = drain current, A

R = Resistance value, Ω

The resistance value is increased until the output voltage reaches the saturation point, which is 3.3V in this case. There are two ways in measuring the current, either connecting the resistor from the output to the ground or to the I/O supply source

(3.3V). If the resistor **R** is connected from the output to the ground as shown in Figure 3.12, the PMOS transistor at the output stage of the buffer will be turned on.

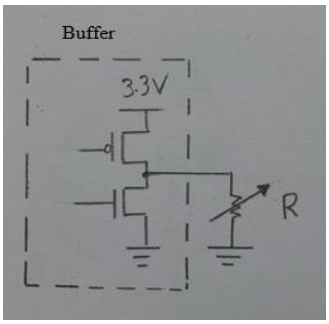


Figure 3.12: Resistor connection to the ground

Conversely, Figure 3.13 shows that if the resistor **R** is connected from the output to 3.3V DC power supply, the NMOS transistor at the output stage will be turned on.

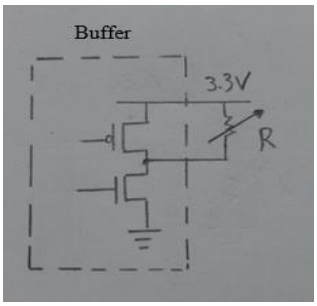


Figure 3.13: Resistor connection to the power supply

Decoupling capacitors of 10pF and 1µF are needed at the power supply pins and the output pin of the buffer respectively to filter the voltage spikes for producing smooth DC signal. The equipment used are listed in Table 3.6. The measured drain current is then compared with the simulated value. The simulated value is obtained by running HSPICE simulation for the output buffers. All the results are tabulated in Chapter 4.

Table 3.6: Equipment Used for DC Drain Current Measurement

Equipment	Model name
DC Power Supply	MEGURO MP303-3 Triple Output DC Power Supply
Digital Multimeter	PRO'SKIT MT-1217 3 ¾ Auto Range Digital Multimeter

Phase 7: Design the schematics of C.U.P. slew rate controlled output buffer

The output buffer with 8-mA drive current is decided to be used as the C.U.P. slew rate controlled design. This is because the current strength of 2-mA and 4-mA are considered too small and thus, excluded from the design. There are three different types of slew rates (slew rate A, slew rate B and slew rate C) required to be included in the 8-mA output buffer. The design is illustrated in Figure 3.14.

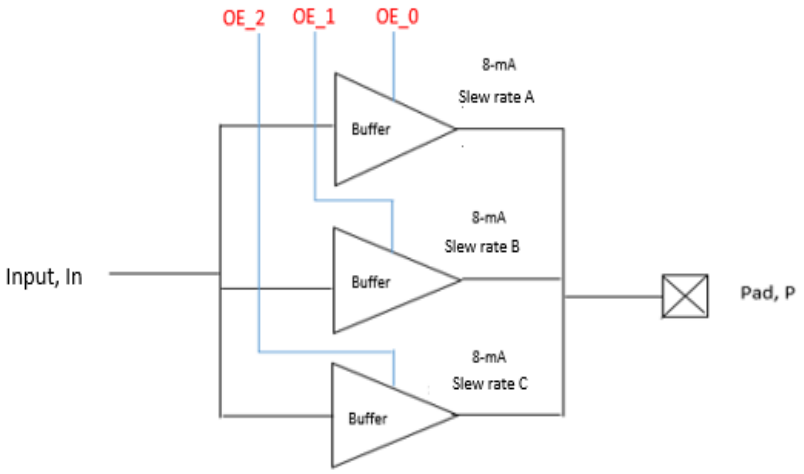


Figure 3.14: Illustration of slew rate controlled 8-mA output buffer design

From the figure, the output buffers with different slew rate A, B, and C are connected in parallel. The input is splitting into three branches to the inputs of the buffers while the output of each transistor circuit is connecting to a common node to the pad. Only one buffer is enabled each time to drive the load with the help of output enable signals (OE_0, OE_1 and OE_2). These control signals are used for selective enabling the slew rate. For example, an external capacitive load of 50pF is connected to the pad. The first output buffer is then turned on by enabling OE_0 to provide 8-mA current with slow slew rate (slew rate A) to drive the load. If the slew rate is too slow, the second or third output buffer instead of first buffer is turned on to provide medium (slew rate B) or fast slew rate (slew rate C) respectively.

By applying this idea into the schematics, the transistor circuits for different slew rates are designed and added at the output stage of the 8-mA buffer. This schematics

design is named as UTOC8ABC and is converted into the transistor netlist in .cdl format. HSPICE simulation is then performed on the design and the resulted waveforms are compared with that of the UTOC8A, UT0C8B and UTOC8C individual output buffers. The output waveforms of the designed buffer are expected to match with the waveforms generated by the three individual output buffers since they are 8-mA buffers with slew rate A, B and C.

Phase 8: Design the schematics of C.U.P. programmable drive strength output buffer

The programmable drive strength output buffer is designed such that it can operate for 2-mA, 4-mA, 6-mA and 8-mA drive currents. In view of this, the output buffer with 2-mA output and slew rate A is selected for the design since the minimum required drive strength is 2-mA. Four of the 2-mA buffers are then connected in parallel form since the maximum required drive strength is 8-mA. The design is illustrated in Figure 3.15.

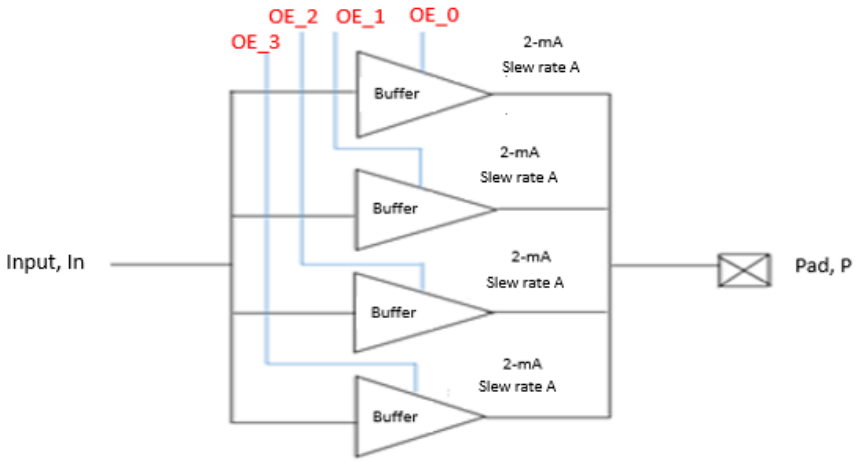


Figure 3.15: Illustration of programmable drive strength output buffer design

From the figure, the input is splitting into four branches to each input of the buffers while the output of each transistor circuit is connecting to a common node to the pad. By forming this type of parallel connection, the 2-mA current can be added up to the

desired drive strength at the output with the help of output enable signals (OE_0, OE_1, OE_2 and OE_3). These control signals are programmed to enable each of the output buffers in selecting a drive current output. For example, an external capacitive load of 50pF is connected to the pad. The first output buffer is then turned on by enabling OE_0 to provide 2-mA current to drive the load. If the drive strength is too weak, the second buffer is turned on too to deliver 4-mA current to the load. Similarly, the third and fourth output buffers will be turned on to give the drive strength of 6-mA and 8-mA respectively if the 4-mA drive strength is not enough to drive the 50pF load.

Based on this idea, the transistor circuits for different drive strengths are designed and added at the output stage of the buffer in the schematics. The schematics design is named as UTOC2468A and is converted into the transistor netlist in .cdl format. HSPICE simulation is then performed on the design and the resulted waveforms are compared with that of the UTOC2A, UT0C4A and UTOC8A individual output buffers. The output waveforms of the designed buffer are expected to match with the waveforms generated by the three individual output buffers since they can provide 2-mA, 4-mA and 8-mA drive current respectively.

Phase 9: Perform HSPICE simulation on both C.U.P. programmable and slew rate controlled output buffer designs for all best and worst case PVT corners

After the schematics of C.U.P. programmable drive strength and slew rate controlled output buffers are designed and converted into .cdl format successfully, HSPICE simulation is performed again to check for all of the best and worst case PVT corners against the design constraints. Same methods in Step 4 are applied.

Phase 10: Perform layout design of the programmable and slew rate controlled output buffers

By using the existing layouts of UTOC8A and UTOC2A output buffers in C.U.P. structure, the layouts of the programmable drive strength and slew rate controlled

output buffers are designed and added. This is done by adding the transistor layout one-by-one into the existing layout based on the design. The layout must perform Hercules design rule check (DRC) and Hercules layout versus schematic check (LVS) before adding the next transistor layout. DRC is performed to verify the completed design to manufacturing design rules specific to a technology. The layout data is analyzed for checking spacing, grid, length, area, size, enclosure and overlap. Also, LVS is checked to verify that the designed layout matches the electronic equivalent of the designed schematic netlist. LVS check extracts and verifies the connectivity between the device components before comparing the extracted information with the schematic netlist. All of the post layout checks are performed and fixed if there is any violation. Once DRC and LVS check are correct as shown in Figure 3.16 and Figure 3.17, next transistor layout can only be added and same steps are repeated again until all of the transistor circuits are completely added into the layout.

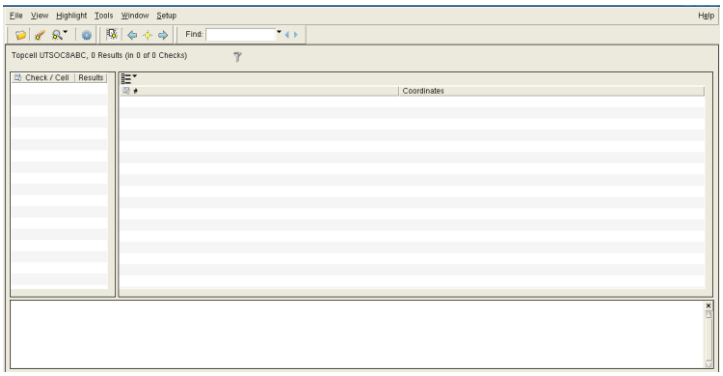


Figure 3.16: DRC is clean

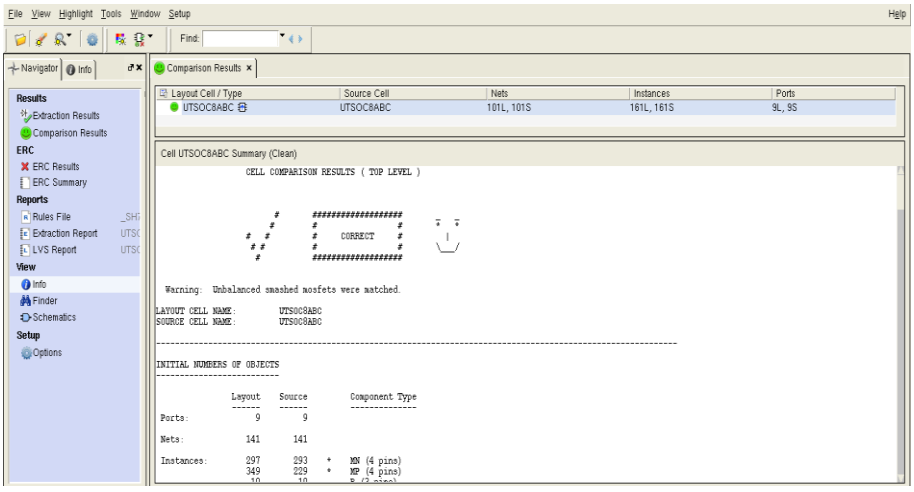


Figure 3.17: LVS check is correct

Phase 11: Extract parasitic of the designed C.U.P. programmable and slew rate controlled output buffers

The Star-RCXT extraction is performed again to extract the parasitic devices from layouts of the designed C.U.P. programmable and slew rate controlled output buffers. By using the generated parasitic netlist, HSPICE simulation is performed to observe the difference in the waveforms before and after RC extraction. Also, HSPICE simulation is executed again for the PVT corners analysis.

3.2 Flowchart of Circuit Level Design Flow

The design flow of C.U.P. programmable drive strength and slew rate controlled output buffers as described in sub-section 3.1 is simplified and illustrated in Figure 3.18 for better understanding.

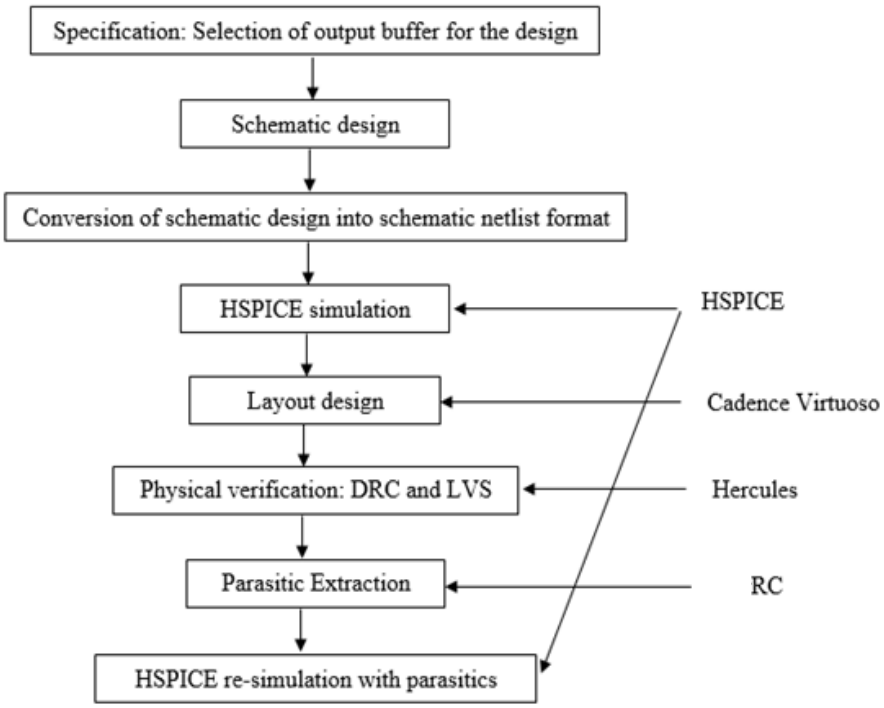


Figure 3.18: Flowchart of the output buffer designs

3.3 Project Milestone

Gantt chart for First Long Trimester (June 2015)

Week / Detail	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Project Selection														
Software tools learning														
Research and report writing														
Project work														
Progress report submission														
Oral presentation														

Gantt chart for Second Long Trimester (Jan 2016)

Week / Detail	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Project work																
Final report submission																
Poster presentation																
Oral presentation																
Hard bound submission																

CHAPTER 4

RESULTS AND DISCUSSIONS

4.1 Chip Testing

4.1.1 Functionality

Based on Table 3.1 in Chapter 3, the bidirectional and input buffers are tested for the functionality. The function of each buffer is tabulated in the corresponding table. The input voltage for input buffer is 3.3V. Due to the core supply of 1.8V, the input buffer will produce 1.8V only as the output voltage and is represented as logic '1' in the receiver function table. On the other hand, the output buffer requires 1.8V as the input voltage. Due to the voltage level shifter function inside the output buffer as shown in Figure 4.1, it will produce 3.3V as the output voltage and is represented as logic '1' in the driver function table.

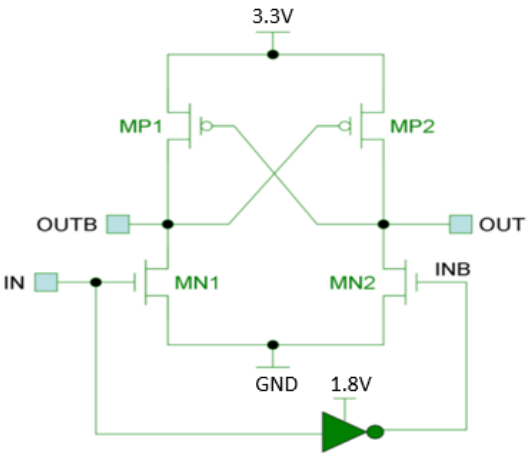


Figure 4.1: Voltage level shifter

When 1.8V is applied to IN of the voltage level shifter, INB is at GND value (0V) due to the inverter. Therefore, the NMOS MN1 is turned on while MN2 is off. The output signal OUTB is pulled to GND. This transition signal will then turn on the PMOS MP2 which pulls up the output OUT to 3.3V. Conversely, the input signal INB is at 1.8V when IN is at GND. This is an inverting function. MN1 will be turned off while MN2 will be turned on. Consequently, OUT signal is pulled to GND and MP1 is turned on. This makes MP1 to pull up the OUTB signal to 3.3V (Medhat, 2009).

For UTICU input buffer, the receiver function is shown in Table 4.1. **IE** represents input enable, **PU** represents weak pull up, **P** represents pad and **Out** represents the output of input buffer.

Table 4.1: Receiver Function of UTICU Input Buffer

Input Pin			**Output Pin**
IE	**PU**	**P**	**Out**
0	≍	≍	0
1	≍	0	0
1	≍	1	1
1	1	HR	1
1	HR	HR	1

When there is no **IE**, **Out** is always 0V regardless of the other input pins. When **IE** is connected to 1.8V, **Out** logic follows **P** logic. If **P** connects to nothing, which means high resistivity (HR), **Out** is always 1.8V for weak **PU**= logic 1 or HR.

For UTICD input buffer, the receiver function is shown in Table 4.2. **PD** represents weak pull down. When there is no **IE**, **Out** is always 0V regardless of the other input pins. When **IE** is connected to 1.8V, **Out** logic follows **P** logic. If **P** connects to nothing, weak **PD** of logic 1 causes **Out**= 0V but when **PD**= HR, **Out** equals to 1.8V.

Table 4.2: Receiver Function of UTICD Input Buffer

Input Pin			Output Pin
IE	**PD**	**P**	**Out**
0	≍	≍	0
1	≍	0	0
1	≍	1	1
1	1	HR	0
1	HR	HR	1

Apart from that, the receiver function of UTCOC2A input buffer is shown in Table 4.3. When there is no **IE**, **Out** is always 0V regardless of the other input pins. When **IE** is connected to 1.8V, **Out** logic follows **P** logic. If **P** connects to nothing, **Out** is at high impedance state (Z).

Table 4.3: Receiver Function of UTCOC2A Input Buffer

Input Pin		Output Pin
IE	**P**	**Out**
0	≍	0
1	0	0
1	1	1
1	HR	Z

If UTCOC2A is changed to become output buffer, the driver function is shown in Table 4.4. **OE** represents output enable while **In** represents data input.

Table 4.4: Driver Function of UTCOC2A Output Buffer

Input Pin		Output Pin
OE	**In**	**P**
0	≍	Z
1	0	0
1	1	Z
1	HR	0

This output buffer is tested without any external pull up resistor. As can be seen, **P** is always at high impedance state when **OE** is connected to ground or **In** is connected to 1.8V. If **OE** is enabled, **P** has logic 0 when **In** is connected to ground or nothing.

For UTCCTU_2A and UTCCTU_8A input buffers, the receiver function is shown in Table 4.5. The receiver functions of UTCCTU_2A and UTCCTU_8A input buffers are found to be same as UTICU input buffer.

Table 4.5: Receiver Function of UTCCTU_2A and UTCCTU_8A Input Buffers

Input Pin			**Output Pin**
IE	**PU**	**P**	**Out**
0	≍	≍	0
1	≍	0	0
1	≍	1	1
1	1	HR	1
1	HR	HR	1

If the bidirectional UTCCTU_2A and UTCCTU_8A are changed to become output buffers, the driver function is shown in Table 4.6. When **OE** is disabled, **P** is at high impedance state if **PU** is logic 0 or **P** becomes high resistive (3.3V) if **PU** is logic 1, regardless of the **In** value. When **OE** is turned on, **P** logic follows **In** logic.

Table 4.6: Driver Function of UTCCTU_2A and UTCCTU_8A Output Buffers

Input Pin			**Output Pin**
OE	**PU**	**In**	**P**
0	0	≍	Z
0	1	≍	HR
1	≍	0	0
1	≍	1	1

4.1.2 Rise and Fall Time Measurement

The input frequency is set as 3MHz in order to examine the rise and fall time of each buffer. The core supply voltage is set as 1.8V while the I/O supply voltage is set as 3.3V. The room temperature is 24°C. Due to the 15pF internal capacitance of oscilloscope probe, the buffers are tested with different external capacitance loads **C** plus 15pF. This total capacitance value is keep on increasing for the measurement until the output voltage of the buffer drops. The rise and fall time of one cycle of the input and output waveforms are measured automatically using the digital oscilloscope as shown in Figure 4.2 and Figure 4.3.

Figure 4.2: Rise time measurement of output buffer

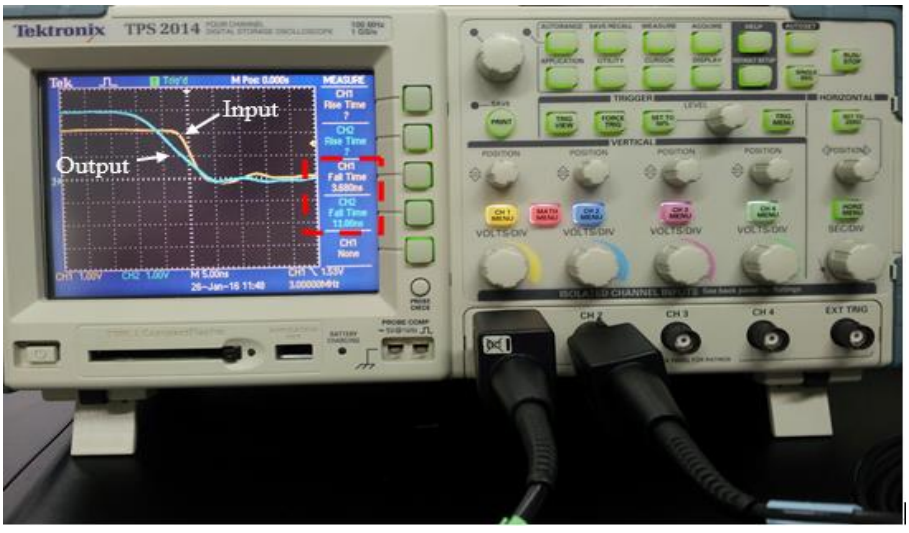


Figure 4.3: Fall time measurement of output buffer

The results are tabulated in the following tables.

Table 4.7: Rise and Fall Time Measurement for UTICU Input Buffer

	Input		Output	
Total capacitance (pF) = C+15pF	**Rise time (ns)**	**Fall time (ns)**	**Rise time (ns)**	**Fall time (ns)**
15 (intrinsic load)	8.4	9.6	17.2	5.6
25	8.4	9.6	22.4	7.6
35	8.4	9.6	25.6	10.0
48	8.4	9.6	31.2	12.8
62	8.4	9.6	39.2	16.0
103	8.4	9.6	57.6	23.6
130	8.4	9.6	72.8	31.2
262	8.4	9.6	113.0	50.0

Table 4.8: Rise and Fall Time Measurement for UTICD Input Buffer

	Input		Output	
Total capacitance (pF) = C+15pF	**Rise time (ns)**	**Fall time (ns)**	**Rise time (ns)**	**Fall time (ns)**
15 (intrinsic load)	8.8	10.0	16.8	5.6
25	8.8	10.0	23.2	7.2
35	8.8	10.0	26.8	9.6
48	8.8	10.0	32.0	12.0
62	8.8	10.0	39.2	15.6
103	8.8	10.0	62.8	23.6
130	8.8	10.0	73.2	30.8
262	8.8	10.0	114.0	47.6

As can be seen in the output column, the rise and fall time measurements for UTICU input buffer are approximately the same as the rise and fall time measurements for UTICD input buffer. This is due to the same buffer structure for both UTICU and UTICD input buffers, except the pull up and pull down transistor part.

Table 4.9: Rise and Fall Time Measurement for UTCOC2A Input Buffer

	Input		**Output**	
Total capacitance (pF) = C+15pF	**Rise time (ns)**	**Fall time (ns)**	**Rise time (ns)**	**Fall time (ns)**
15 (intrinsic load)	12.0	12.8	16.4	6.0
25	12.0	12.8	20.4	7.6
35	12.0	12.8	22.8	10.0
48	12.0	12.8	27.2	14.4
62	12.0	12.8	33.6	16.8
103	12.0	12.8	48.4	24.4
130	12.0	12.8	60.0	32.0
262	12.0	12.8	82.4	52.4
345	12.0	12.8	93.2	60.8

Table 4.10: Rise and Fall Time Measurement for UTCOC2A Output Buffer

	Input		**Output**	
Total capacitance (pF) = C+15pF	**Rise time (ns)**	**Fall time (ns)**	**Rise time (ns)**	**Fall time (ns)**
15 (intrinsic load)	10.04	10.84	64.8	12.12
25	10.04	10.84	74.2	15.2
35	10.04	10.84	83.2	19.6

An external pull up resistor of 10kΩ is connected from the pad of UTCOC2A output buffer to 3.3V due to its open drain characteristics.

Table 4.11: Rise and Fall Time Measurement for UTCCTU_2A Input Buffer

	Input		Output	
Total capacitance (pF) = C+15pF	**Rise time (ns)**	**Fall time (ns)**	**Rise time (ns)**	**Fall time (ns)**
15 (intrinsic load)	8.4	9.2	16.4	5.2
25	8.4	9.2	22.4	7.2
35	8.4	9.2	25.6	9.2
48	8.4	9.2	31.6	12.8
62	8.4	9.2	38.8	16.4
103	8.4	9.2	58.4	23.6
130	8.4	9.2	76.0	32.0
259	8.4	9.2	111.0	56.4

Table 4.12: Rise and Fall Time Measurement for UTCCTU_2A Output Buffer

	Input		Output	
Total capacitance (pF) = C+15pF	**Rise time (ns)**	**Fall time (ns)**	**Rise time (ns)**	**Fall time (ns)**
15 (intrinsic load)	10.8	11.2	5.4	5.0
25	10.8	11.2	9.4	7.8
35	10.8	11.2	16.4	12.0
48	10.8	11.2	21.6	16.4
62	10.8	11.2	28.0	22.8
103	10.8	11.2	36.8	30.6
130	10.8	11.2	46.4	39.0
365	10.8	11.2	94.4	90.2

Table 4.13: Rise and Fall Time Measurement for UTCCTU_8A Input Buffer

	Input		Output	
Total capacitance (pF) = C+15pF	**Rise time (ns)**	**Fall time (ns)**	**Rise time (ns)**	**Fall time (ns)**
15 (intrinsic load)	8.4	9.2	16.4	5.2
25	8.4	9.2	21.2	6.8
35	8.4	9.2	24.8	8.8
48	8.4	9.2	30.0	11.2
62	8.4	9.2	37.6	15.6
103	8.4	9.2	56.8	23.2
130	8.4	9.2	74.4	31.6
272	8.4	9.2	114.0	56.4

Table 4.14: Rise and Fall Time Measurement for UTCCTU_8A Output Buffer

	Input		Output	
Total capacitance (pF) = C+15pF	**Rise time (ns)**	**Fall time (ns)**	**Rise time (ns)**	**Fall time (ns)**
15 (intrinsic load)	8.4	10.0	4.8	4.0
25	8.4	10.0	5.6	4.8
35	8.4	10.0	6.4	6.0
48	8.4	10.0	10.8	5.6
103	8.4	10.0	15.2	8.0
130	8.4	10.0	20.4	13.2
325	8.4	10.0	23.2	18.8
2137	8.4	10.0	34.0	30.8

Based on the data, the fall time of the input waveform for all the buffers is greater than the rise time. This is due to the loading environment such as the environmental temperature and equipment impedances. In fact, the fall time should be smaller than

the rise timeas shown in the output waveforms for all buffers. This is because of the mobility of PMOS and NMOS. For charging period, the waveform rises from low level to higher level and this indicates that PMOS is turned on. If the waveform falls from high level to low level, NMOS will be turned on. Since PMOS hole mobility is smaller than the NMOS electron mobility, the charging time or rise time of the output will be definitely higher than that of the discharging time or fall time (Ash, 2013).

Also, the rise and fall time of the buffers are measured for the fast and slow corners of PVT with the use of 3MHz input frequency and fixed capacitance value of 25pF. For fast corner PVT to occur, the core supply voltage and I/O supply are set to 1.98V and 3.63V respectively. The low temperature is measured as 11°C. For slow corner PVT to occur, the core supply voltage and I/O supply are set to 1.62V and 2.97V respectively. The high temperature is measured as 80°C. The results are summarized in Table 4.15. Based on the data, the fast corner PVT contributes to faster rise and fall time while the slow corner PVT gives slower rise and fall time of the output waveform when compared with the original output waveform.

Table 4.15: Rise and Fall Time Measurement for PVT Corners

	Low Temperature (11°C) with C=25pF				Room Temperature (24°C) with C= 25pF				High Temperature (80°C) with C=25pF			
	Input		Output		Input		Output		Input		Output	
	Rise time (ns)	Fall time (ns)	Rise time (ns)	Fall time (ns)	Rise time (ns)	Fall time (ns)	Rise time (ns)	Fall time (ns)	Rise time (ns)	Fall time (ns)	Rise time (ns)	Fall time (ns)
UTICU input buffer	9.90	10.40	16.30	4.70	8.40	9.60	22.40	7.60	10.40	12.40	24.40	8.00
UTICD input buffer	10.04	10.08	17.76	4.24	8.80	10.00	23.20	7.20	9.56	10.04	24.80	8.30
UTCOC2A input buffer	10.40	10.56	15.20	4.10	12.00	12.80	20.40	7.60	10.20	10.50	21.50	8.10
UTCOC2A output buffer	10.32	10.52	56.70	10.76	10.04	10.84	74.20	15.20	11.52	12.48	80.51	18.60
UTCCTU_2A input buffer	10.50	11.32	17.70	4.48	8.40	9.20	22.40	7.20	10.80	11.60	28.40	10.40
UTCCTU_2A output buffer	10.32	11.56	8.60	4.92	10.80	11.20	9.40	7.80	10.40	12.00	26.40	18.40
UTCCTU_8A input buffer	10.40	10.70	16.84	4.36	8.40	9.20	21.20	6.80	10.80	11.60	25.60	10.00
UTCCTU_8A output buffer	10.08	10.80	4.37	3.68	8.40	10.00	5.60	4.80	10.80	11.60	6.40	5.20

4.1.3 DC Drain Current Measurement for Output Buffers

The output buffers of UTCOC2A, UTCCTU_2A and UTCCTU_8A are tested for DC drain current measurement. For PMOS transistor at the output stage of the buffer to turn on, the external resistor is connected from the pad to the ground. The resistance value keeps on increasing for the measurement until the voltage across the resistor reaches the saturation voltage of 3.3V. The results are tabulated in Table 4.16. The resistance is infinite when the output connects to nothing.

Table 4.16: Drain Current Measurement (PMOS is turned on)

	UTCCTU_2A output buffer		**UTCCTU_8A output buffer**	
Resistance (Ω)	**Measured V (V)**	**Measured I (mA)**	**Measured V (V)**	**Measured I (mA)**
infinite	3.3360	-	3.3680	-
5.400	0.1470	27.2222	0.2637	48.8333
9.900	0.2581	26.0707	0.4680	47.2727
0.984k	2.9380	2.9858	3.2580	3.3110
3.293k	3.2010	0.9721	3.3270	1.0103
4.280k	3.2470	0.7586	3.3320	0.7785
4.920k	3.2510	0.6608	3.3320	0.6772
9.840k	3.3000	0.3354	3.3430	0.3397
19.840k	3.3100	0.1668	3.3470	0.1687

The PMOS is fully turned on when the resistance is at the range of 5.4Ω to 9.9Ω. At this saturation point, most of the drain current can flow through the PMOS transistor at the output stage of the buffer. The saturation drain current of UTCCTU_8A is found 1.8 times larger than that of UTCCTU_2A output buffer. Theoretically, the drain current of UTCCTU_8A should be 4 times larger than the drain current of UTCCTU_2A output buffer due to the drive strength of 8-mA and 2-mA respectively. From 0.984kΩ onward, the measured voltage across the resistor is found constant for both UTCCTU_2A and UTCCTU_8A output buffers. This is because of the larger resistance load that causes the drain current is determined by the load resistance now.

For NMOS transistor at the output stage of the buffer to turn on, the external resistor is connected from the pad to 3.3V. The results are tabulated in Table 4.17.

Table 4.17: Drain Current Measurement (NMOS is turned on)

	UTCCTU_2A output buffer		UTCCTU_8A output buffer		UTCOC2A output buffer	
Resistance (Ω)	Measured V (V)	Measured I (mA)	Measured V (V)	Measured I (mA)	Measured V (V)	Measured I (mA)
infinite	3.336	-	3.368	-	-	-
5.400	0.158	29.2593	0.271	50.1852	0.162	30.0000
9.900	0.232	23.4343	0.464	46.8687	0.225	22.7273
0.984k	2.978	3.0264	3.286	3.3394	3.021	3.0701
3.293k	3.222	0.9784	3.329	1.0109	3.213	0.9757
4.280k	3.249	0.7591	3.335	0.7792	3.254	0.7603
4.920k	3.260	0.6626	3.340	0.6789	3.279	0.6665
9.840k	3.299	0.3353	3.344	0.3398	3.305	0.3359
19.840k	3.319	0.1673	3.349	0.1688	3.317	0.1672

The result of UTCOC2A output buffer is almost same as the result of UTCCTU_2A output buffer due to the same drive strength of 2-mA and slew rate A. Also, the overall results of UTCCTU_2A and UTCCTU_8A output buffer for NMOS to be switched on are similar to that for PMOS to be switched on. The NMOS is fully turned on when the resistance is at the range of 5.4Ω to 9.9Ω. At this saturation point, most of the drain current can flow through the NMOS transistor at the output stage of the buffer. The saturation drain current of UTCCTU_8A is found 1.7~2 times larger than that of UTCCTU_2A output buffer. From 0.984kΩ onward, the measured voltage across the resistor is found constant.

The theoretical calculation of DC drain current is also performed for the PMOS and NMOS of UTCCTU_2A and UTCCTU_8A output buffers at the saturation mode by using revised equation 2.5. Since it is theoretical case, $(1 + \lambda V_{DS})$ in the

equation will be ignored. The oxide capacitance per area C'_{ox} can be calculated using the equation:

$$C'_{ox} = \frac{\varepsilon_r \varepsilon_o}{t_{ox}} \tag{4.1}$$

where

C'_{ox} = oxide capacitance per area, F/cm^2

ε_r = relative permittivity

ε_o = permittivity of free space, F/cm

t_{ox} = oxide thickness, m

By using the given information, the calculations of C'_{ox} for PMOS and NMOS with the corresponding drain current for UTCCTU_2A and UTCCTU_8A output buffers are shown:-

<u>C'_{ox} for PMOS:-</u>

ε_r = 3.9

ε_o = 8.854 x 10^{-12} F/m

t_{ox} = 6.48 x 10^{-9} m

$$C'_{ox} = \frac{3.9 \; x \; 8.854 \; x \; 10^{-12} \; F/m}{6.48 \; x \; 10^{-9} \; m}$$

$$= 5.33 \; x \; 10^{-3} \frac{F}{m^2}$$

$$= 5.33 \; x \; 10^{-7} \frac{F}{cm^2}$$

<u>C'_{ox} for NMOS:-</u>

t_{ox} = 6.22 x 10^{-9} m

$$C'_{ox} = \frac{3.9 \; x \; 8.854 \; x \; 10^{-12} \; F/m}{6.22 \; x \; 10^{-9} \; m}$$

$$= 5.5515 \; x \; 10^{-3} \frac{F}{m^2}$$

$$= 5.5515 \; x \; 10^{-7} \frac{F}{cm^2}$$

I_D for UTCCTU_2A (PMOS is turned on):-

μ_p = 105 cm^2 /V.s

C'_{ox} = 5.33 x 10^{-7} F/cm^2

$\frac{W}{L} = 4\left(\frac{9.2u}{0.3u}\right)$

V_{GS} = -3.3V

V_T = -0.6184V

$$I_{D(SATURATION)} = \frac{105\ x\ 5.33\ x\ 10^{-7}}{2} \cdot 4\left(\frac{9.2}{0.3}\right) \cdot [-3.3 - (-0.6184)^2]$$
$$= 24.6866\ mA$$

I_D for UTCCTU_8A (PMOS is turned on):-

$\frac{W}{L} = 16\left(\frac{9.2u}{0.3u}\right)$

$$I_{D(SATURATION)} = \frac{105\ x\ 5.33\ x\ 10^{-7}}{2} \cdot 16\left(\frac{9.2}{0.3}\right) \cdot [-3.3 - (-0.6184)^2]$$
$$= 98.7321\ mA$$

I_D for UTCCTU_2A (NMOS is turned on):-

μ_n = 406 cm^2 /V.s

C'_{ox} = 5.5515 x 10^{-7} F/cm^2

$$\frac{W}{L} = \frac{1}{\left[\frac{1}{4\left(\frac{7u}{0.4u}\right)}\right] + \left[\frac{1}{4\left(\frac{7u}{0.4u}\right)}\right]}$$

V_{GS} = 3.3V

V_T = 0.715V

$$I_{D(SATURATION)} = \frac{406\ x\ 5.5515\ x\ 10^{-7}}{2} \cdot \frac{1}{\left[\frac{1}{4\left(\frac{7u}{0.4u}\right)}\right] + \left[\frac{1}{4\left(\frac{7u}{0.4u}\right)}\right]} \cdot [3.3 - (0.715)^2]$$
$$= 26.358\ mA$$

I_D for UTCCTU_8A (NMOS is turned on):-

$$\frac{W}{L} = \frac{1}{\left[\frac{1}{16\left(\frac{7u}{0.4u}\right)}\right] + \left[\frac{1}{16\left(\frac{7u}{0.4u}\right)}\right]}$$

$$I_{D(SATURATION)} = \frac{406\ x\ 5.5515\ x\ 10^{-7}}{2} \cdot \frac{1}{\left[\frac{1}{16\left(\frac{7u}{0.4u}\right)}\right] + \left[\frac{1}{16\left(\frac{7u}{0.4u}\right)}\right]} \cdot [3.3 - (0.715)^2]$$

$$= 105.432\ mA$$

The ratio of the drain current for UTCCTU_8A and UTCCTU_2A output buffers where PMOS is turned on is calculated as:

$$\frac{I_D\ (UTCCTU\_8A)}{I_D(UTCCTU\_2A)} = \frac{98.7321\ mA}{24.6866\ mA}$$

$$= 3.9994$$

$$\approx 4$$

The ratio of the drain current for UTCCTU_8A and UTCCTU_2A output buffers where NMOS is turned on is calculated as:

$$\frac{I_D\ (UTCCTU\_8A)}{I_D(UTCCTU\_2A)} = \frac{105.432\ mA}{26.358\ mA}$$

$$= 4$$

As can be seen, the drain current of UTCCTU_8A is 4 times larger than the drain current of UTCCTU_2A output buffer theoretically. However, the calculated value cannot be compared with the measured value as the calculated value shows the ideal case of maximum drain current calculation without any use of the resistor. In fact, the buffer circuit is comprised of a 636.219Ω resistor connected series to the pad. This makes the measured value smaller than the theoretical value. Therefore,

HSPICE simulation is performed for the comparison with the measured value. The HSPICE script is shown in Appendix B and the results are tabulated in Table 4.18.

Table 4.18: Drain Current Comparison for Measurement and Simulation

	UTCCTU_2A output buffer				UTCCTU_8A output buffer			
Resistance (Ω)	Measured V (V)	Measured I (mA)	Simulated V (V)	Simulated I (mA)	Measured V (V)	Measured I (mA)	Simulated V (V)	Simulated I (mA)
infinite	3.3360	-	3.3000	-	3.3680	-	3.3000	-
5.400	0.1470	27.2222	0.1390	25.8000	0.2637	48.8333	0.2940	55.4000
9.900	0.2581	26.0707	0.2530	25.6000	0.4680	47.2727	0.5390	54.4000
0.984k	2.9380	2.9858	2.9800	3.0300	3.2580	3.3110	3.2200	3.2700
3.293k	3.2010	0.9721	3.2000	0.9730	3.3270	1.0103	3.2800	0.9950
4.280k	3.2470	0.7586	3.2300	0.7540	3.3320	0.7785	3.2800	0.7670
4.920k	3.2510	0.6608	3.2300	0.6570	3.3320	0.6772	3.2800	0.6670
9.840k	3.3000	0.3354	3.2700	0.3320	3.3430	0.3397	3.2900	0.3350
19.840k	3.3100	0.1668	3.2800	0.1660	3.3470	0.1687	3.3000	0.1660

From the table, the simulated voltage and current values are similar to that of the measured values for UTCCTU_2A and UTCCTU_8A output buffers. The drain current saturation point is found at the resistance range of 5.4Ω to 9.9Ω. When the resistance load increases, the drain current will be eventually determined by the load instead of the transistor size.

4.2 Comparison of Output Buffers with and without C.U.P. Structure

Before starting the design, the layout of the output buffer with C.U.P. structure is compared with the output buffer without C.U.P. modification. The location of the I/O pad that acts as the intermediate structure for the connection of the core of integrated circuit to outside world becomes the key difference between the output buffers with and without C.U.P. modification. From Figure 4.4 and Figure 4.5, UTOC8A output buffer with C.U.P. structure saves a lot of spaces by relocating the pad area above the transistor circuits.

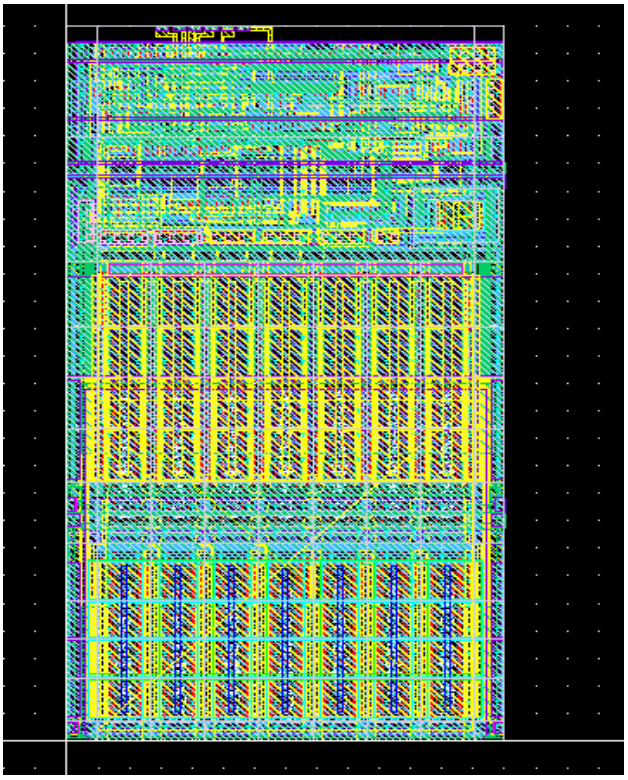


Figure 4.4: Layout of UTOC8A output buffer with C.U.P. structure

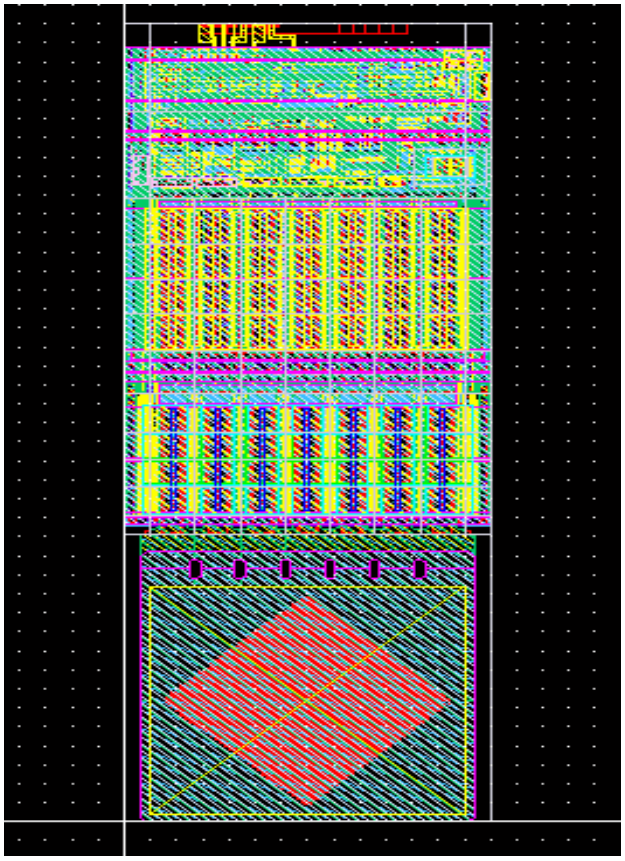


Figure 4.5: Layout of UTOC8A output buffer without C.U.P. structure

HSPICE simulation is then performed for both output buffers with and without C.U.P. modification to examine any difference in the waveform. Based on Figure 4.6, the output waveforms are the same for both output buffers, given the same input waveform. In other words, the output buffer with C.U.P. structure maintains the same transistor circuit connection but with the advantage of smaller space to be used.

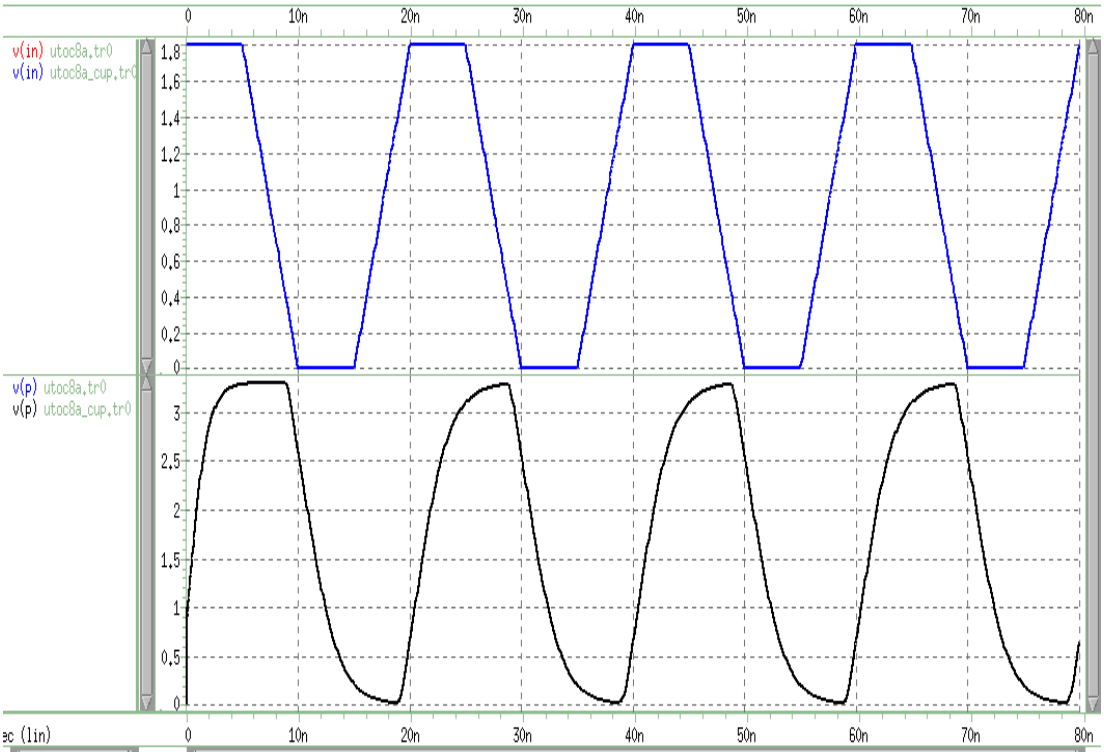


Figure 4.6: Waveforms comparison for UTOC8A output buffer with and without C.U.P. structure

4.3 Simulation of C.U.P. Output Buffer

The C.U.P. output buffer is simulated to model all the best case and worst case corners of PVT. The typical case requires typical process, core supply voltage of 1.8V, I/O supply of 3.3V and room temperature of 27°C. For best case corners of PVT, fast process is used together with core supply voltage of 1.98V, I/O supply of 3.63V and low temperature of -40°C. On the other hand, the worst case corners of PVT involves slow process, core supply voltage of 1.62V, I/O supply of 2.97V and high temperature of 125°C. The resulted waveform is shown in Figure 4.7.

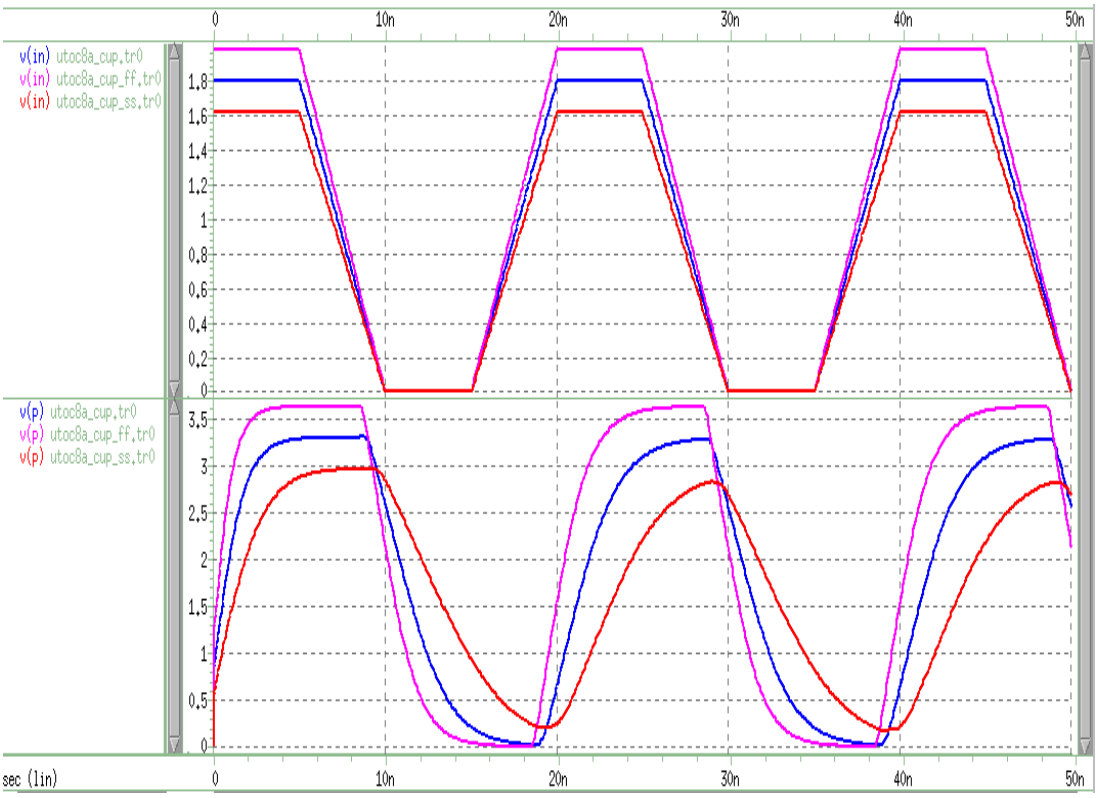


Figure 4.7: Waveform of C.U.P. UTOC8A output buffer for PVT corners

By comparing to the typical waveform (blue), the input and output waveforms with fast corners of PVT (magenta) give fastest rise and fall time and hence, it is known as best case PVT conditions. The input and output waveforms with slow corners of PVT (red), on the other hand, offer slowest rise and fall time among the three types of waveform simulation. Therefore, it is called worst case PVT conditions. The worst case PVT shows that the waveform does not swing rail-to-rail as the signal has not enough time for charging and discharging to reach the desired voltage levels.

After that, RC extraction is performed to extract the parasitic resistance and capacitance obtained from the output buffer layout as shown in Figure 4.8.

UTOC8A

No.	Layout Net	Source Net	R Count	C Total (F)	CC Total (F)	C+CC Total (F)
1	1	I1_I5_I1_15	39	1.64748E-15	5.71542E-15	7.36290E-15
2	2	I1_I5_I1_13	19	6.89830E-16	2.47056E-15	3.16039E-15

Figure 4.8: Part of the parasitic RC extraction from C.U.P. UTOC8A layout

At the same time, there are three parasitic netlist generated together with the RC extraction, with the extension format of .pex.netlist.UTOC8A.pxi, .pex.netlist.pex and .pex.netlist. The original CDL netlist included in the HSPICE script is replaced by these three parasitic netlist files so that HSPICE simulation can be performed again to observe the parasitic effect on the rise and fall time of the waveform.

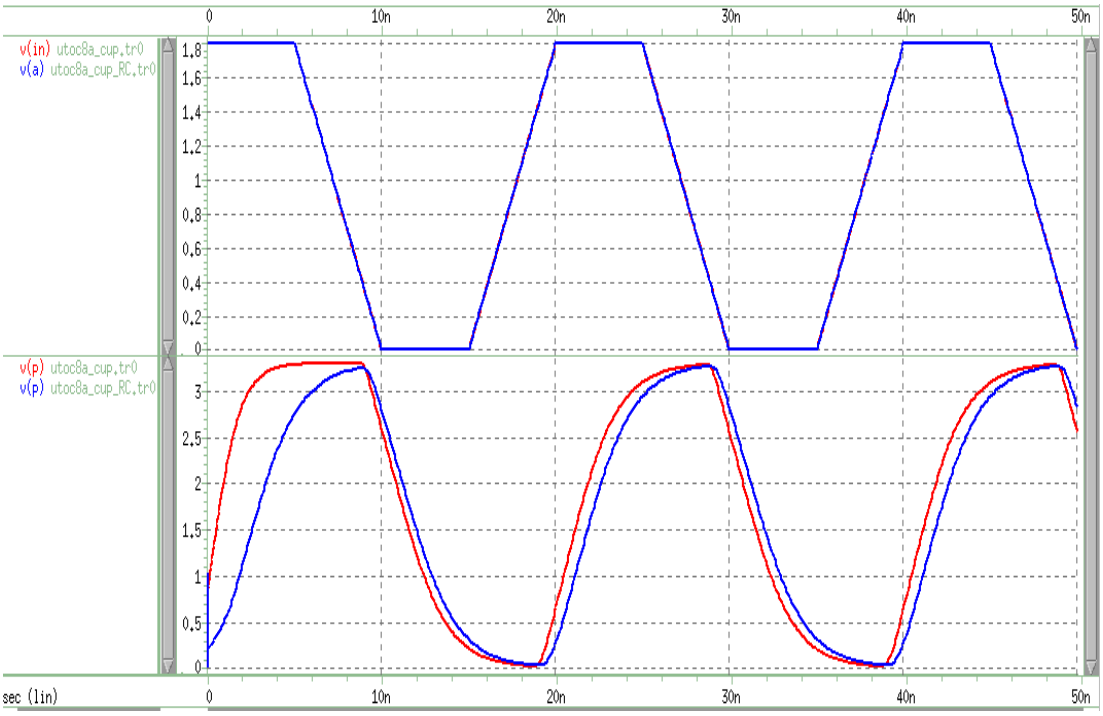


Figure 4.9: Comparison of waveforms for C.U.P. UTOC8A output buffer before and after RC extraction

Based on Figure 4.9, there is some delay between the output waveforms before and after RC extraction. This is due to the parasitic resistance and capacitance of the nets inside the layout that contribute to the delay. The delay is known as resistive-capacitive delay (RC delay).

4.4 Design of C.U.P. Slew Rate Controlled Output Buffer

4.4.1 Schematic Design

By referring to the original schematic diagram of UTOC8A output buffer, the input stage, voltage level shifter and output stage of the buffer are identified. Since the output buffer is comprised of the structure for slew rate A, the design of slew rate B and slew rate C are added parallel at the output stage of the buffer. The design of C.U.P. slew rate controlled output buffer is known as UTOC8ABC with the schematic design showed in Figure 4.10. The PMOS and NMOS at the output stage of the buffer are controlled independently by their own transistor circuit. There are three output enable pins, namely **OE_0**, **OE_1** and **OE_2**, for the selection of slew rate A, slew rate B and slew rate C respectively. The input pin is named as **In** while the output pin is named as **P**.

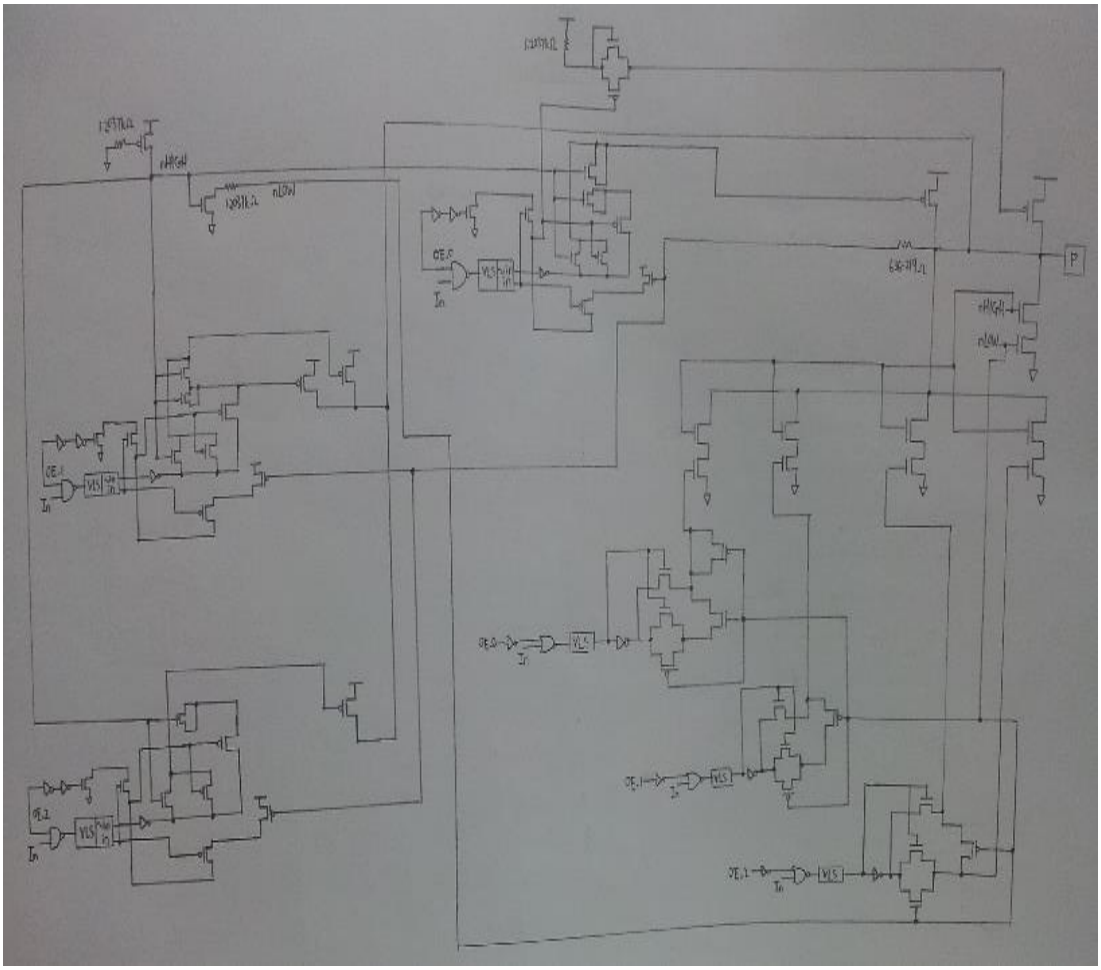


Figure 4.10: Schematic design of UTOC8ABC

4.4.2 HSPICE Simulation

Consequently, the drawn schematic design is converted into CDL netlist with the name of slew_rate_abc.cdl. By including this netlist file in HSPICE script as shown in Appendix C, the HSPICE simulation is performed on the design with the pull up resistor of 10kΩ and the capacitor load of 50pF. The generated waveforms with slew rate A, B and C are compared with that of the UTOC8A, UT0C8B and UTOC8C individual output buffers. Same steps are repeated from the schematic design to the HSPICE simulation for the modification until the output waveforms of UTOC8ABC matching with the waveforms generated by these three individual output buffers. The resulted output waveforms are shown in the following figures.

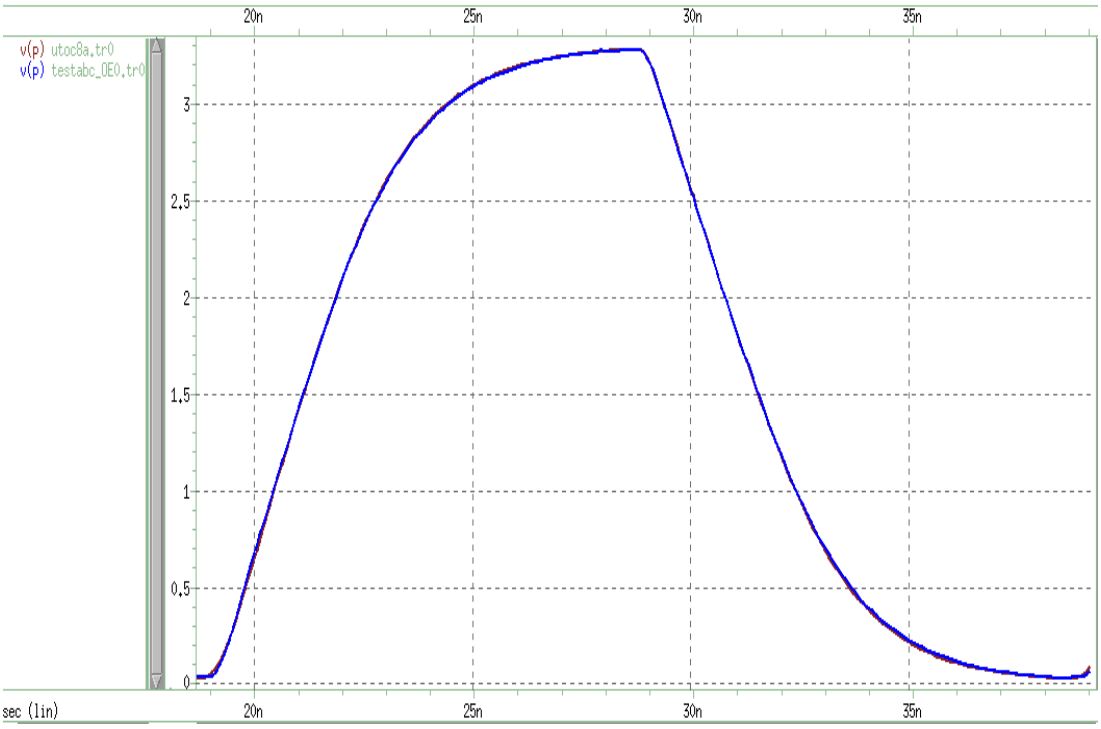


Figure 4.11: Comparison of waveforms for UTOC8A and UTOC8ABC (OE_0 is enabled)

When OE_0 pin of UTOC8ABC is enabled, the output buffer will provide drive strength of 8-mA with slew rate A for the 50pF capacitor load. This resulted waveform matches with the output waveform of the original UTOC8A output buffer.

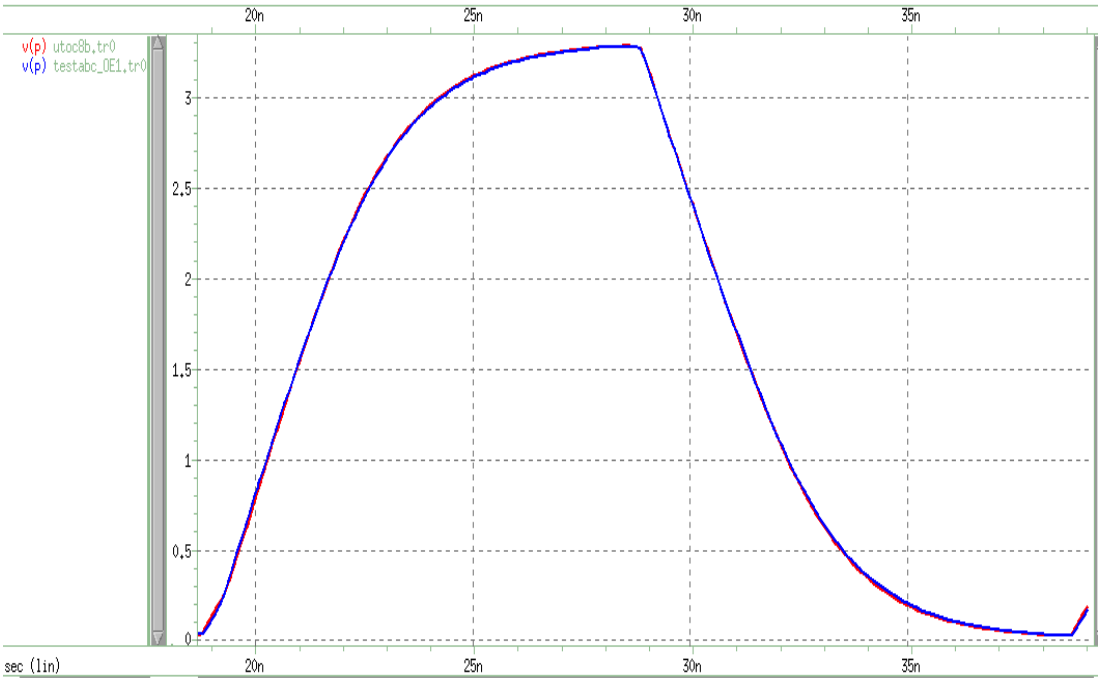


Figure 4.12: Comparison of waveforms for UTOC8B and UTOC8ABC (OE_1 is enabled)

When OE_1 pin of UTOC8ABC is enabled, the output buffer will provide drive strength of 8-mA with slew rate B for the 50pF capacitor load. This resulted waveform matches with the output waveform of the original UTOC8B output buffer.

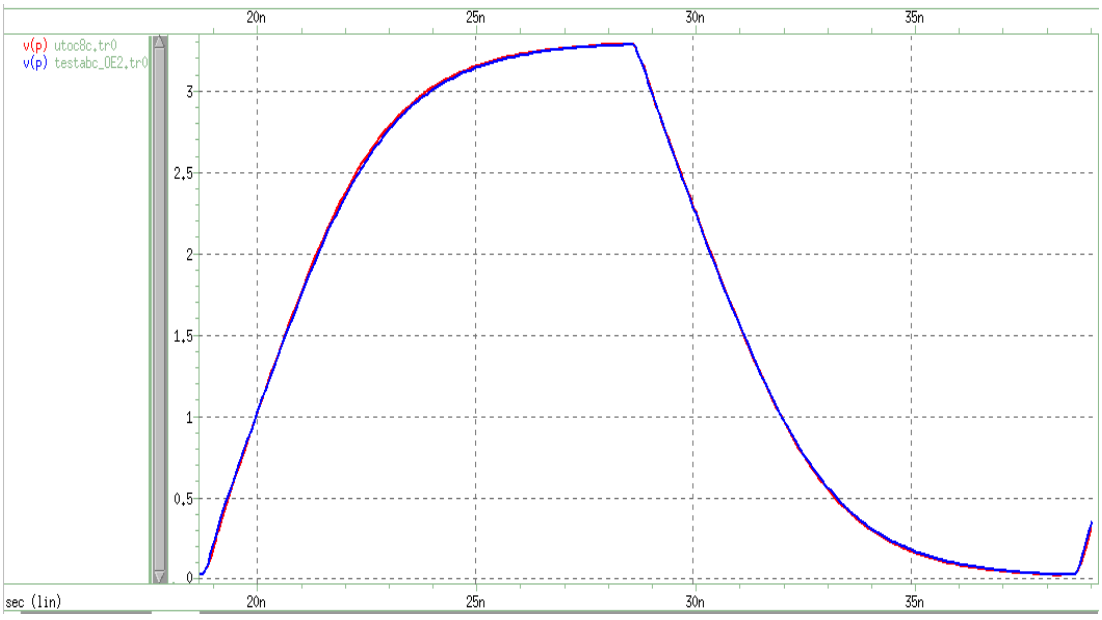


Figure 4.13: Comparison of waveforms for UTOC8C and UTOC8ABC (OE_2 is enabled)

When OE_2 pin of UTOC8ABC is enabled, the output buffer will provide drive strength of 8-mA with slew rate C for the 50pF capacitor load. This resulted waveform matches with the output waveform of the original UTOC8C output buffer.

The output waveforms are combined together for better view in Figure 4.14. Slew rate A, B and C are tested for the fixed capacitor load of 50pF. As can be seen, slew rate A (blue and magenta) contributes to the slowest slew rate; slew rate B (black and orange) gives mid-range slew rate; and slew rate C (purple and red) provides the fastest slew rate.

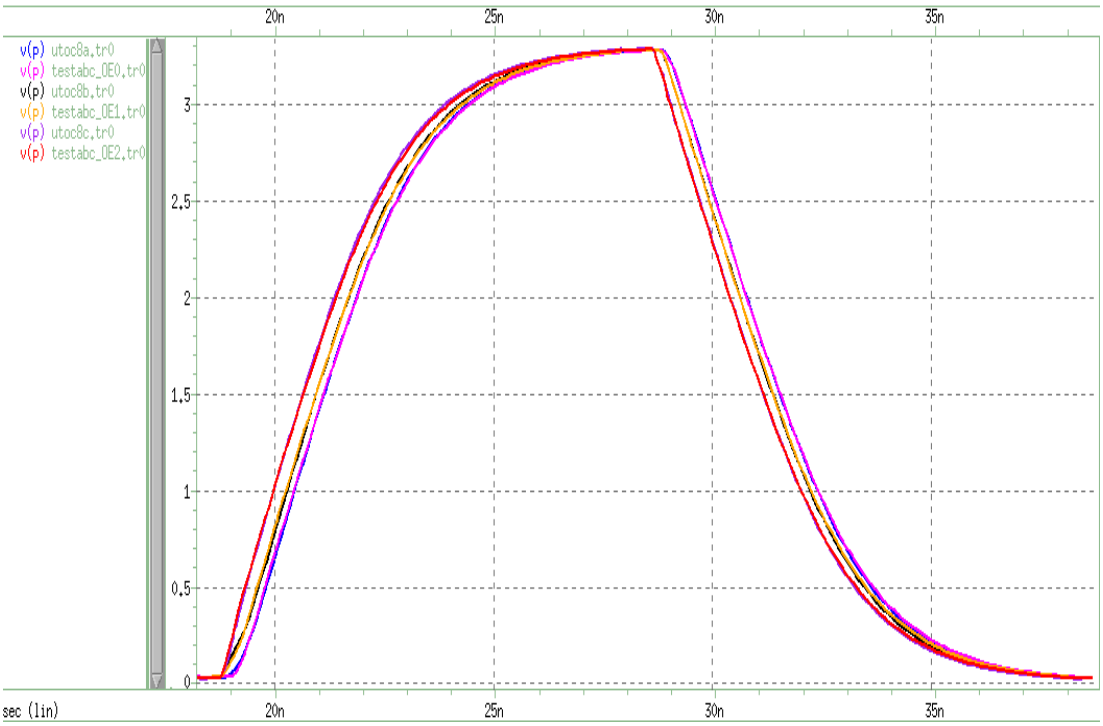


Figure 4.14: Combination waveforms of slew rate A, B and C for 50pF load

In order to determine the difference among the three slew rates A, B and C, the output waveforms undergo derivative function ($\frac{dV_P}{dt}$) to get the waveforms in terms of slew rate value. The result is shown in Figure 4.15. As can be seen, the beginning of the rising edge and the beginning of the falling edge of one cycle in the waveform give a bigger difference in the slew rate. However, the transition of the waveform shows that the slew rate is approximately the same with each other.

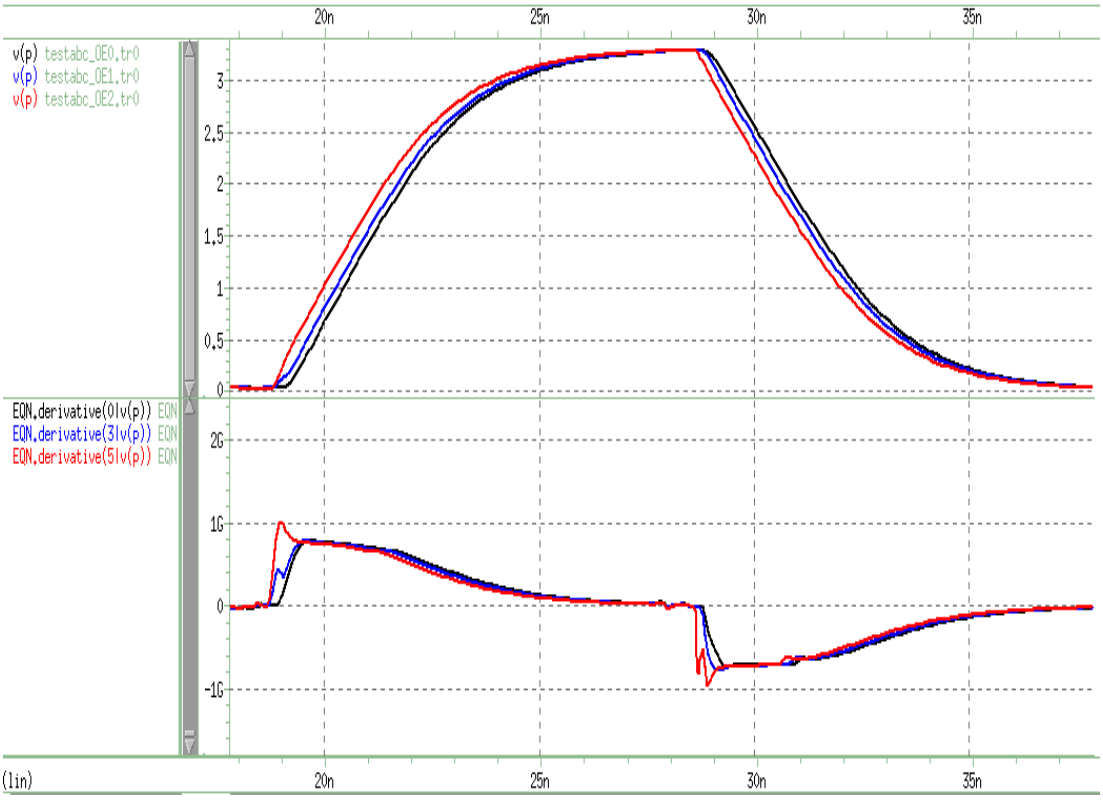


Figure 4.15: Slew rate waveforms with the corresponding derivative waveforms

Besides, HSPICE simulation is performed again to model all the best case and worst case corners of PVT. The results are shown in the following figures. The best case PVT conditions (black) give fastest rise and fall time while the worst case PVT conditions (red) show slowest rise and fall time if compared to the typical case (blue).

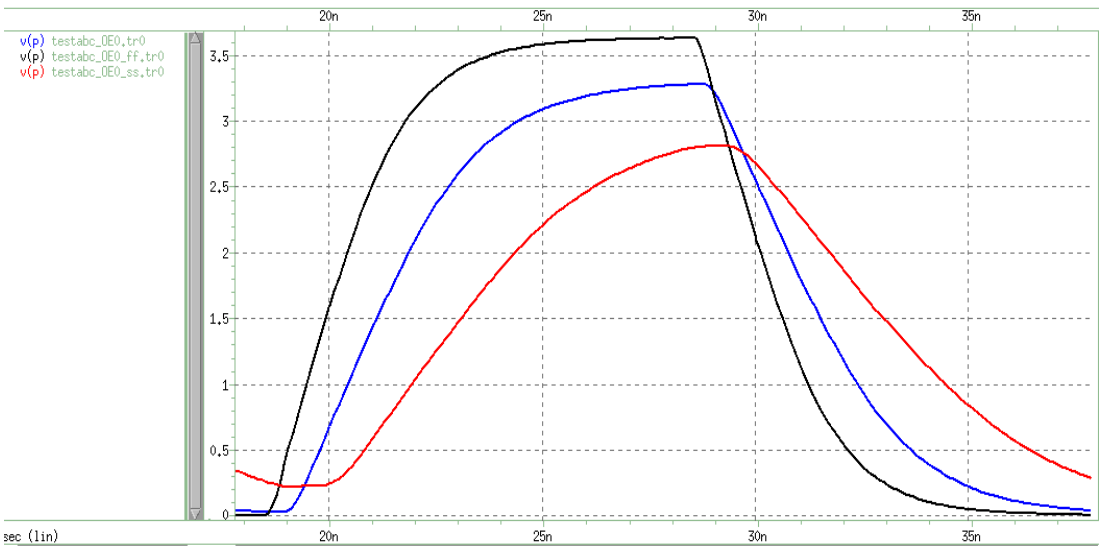


Figure 4.16: PVT waveform for slew rate A

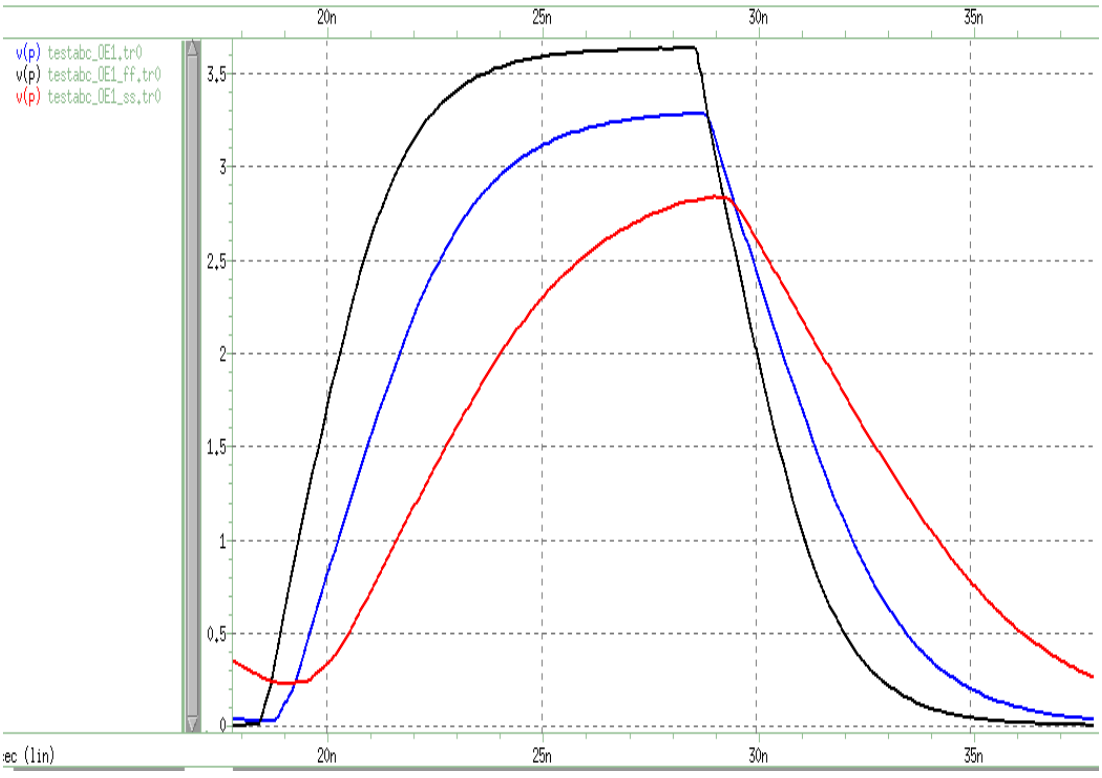


Figure 4.17: PVT waveform for slew rate B

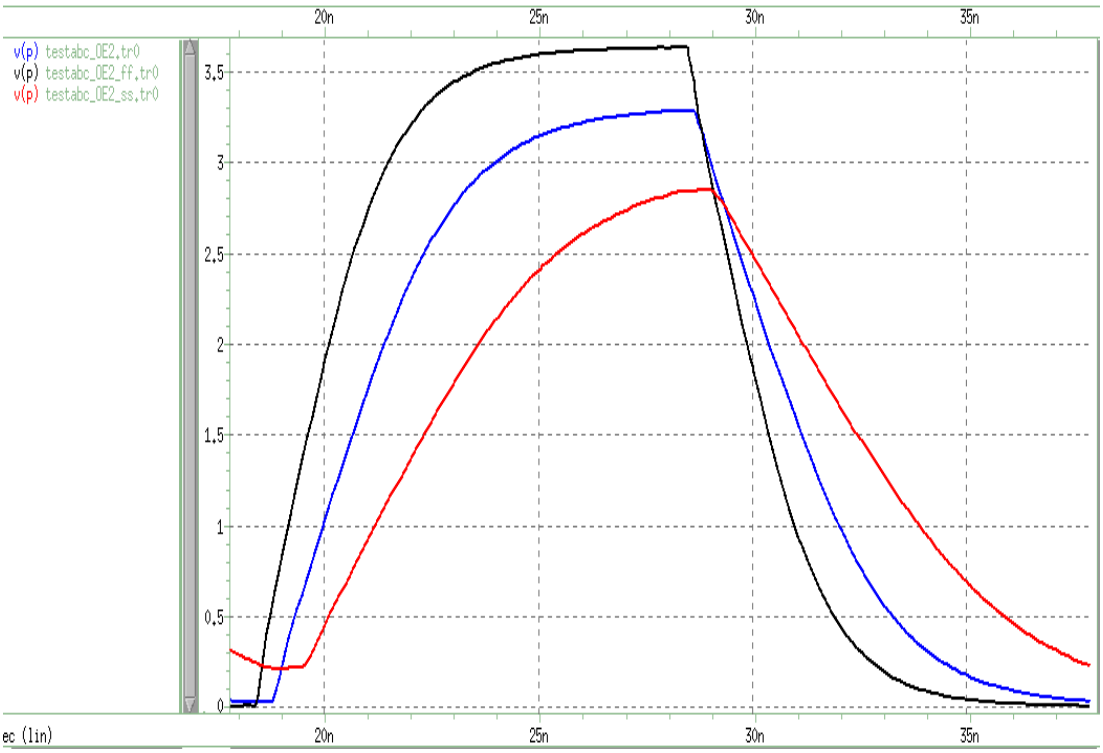


Figure 4.18: PVT waveform for slew rate C

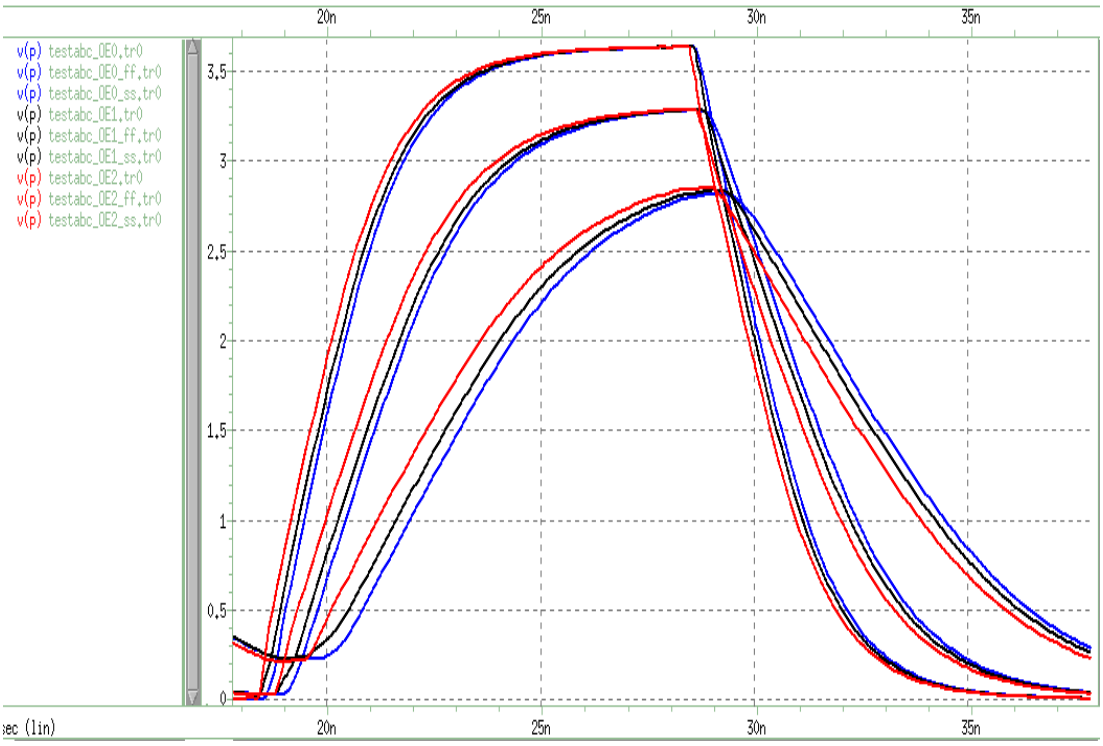


Figure 4.19: Combination of PVT waveforms for all slew rates

The waveforms of slew rate A (blue), slew rate B (black) and slew rate C (red) with their corresponding best and worst case PVT conditions are shown in Figure 4.19. In a nutshell, slower slew rate is required for smaller capacitive load while faster slew rate is needed for larger load. The output buffer with slew rate controlled is designed so as to act fast enough to meet the speed requirement but at the same time, minimizing the noise problem.

4.4.3 Layout Design and HSPICE Simulation

The layout of designed UTOC8ABC output buffer is presented in the n-well CMOS fabrication technology as shown in Figure 4.20. The guard rings are used for shielding purpose and formed by p-substrate with the use of substrate contacts to connect to the ground. This layout is checked for DRC and LVS to ensure that no violation occurs.

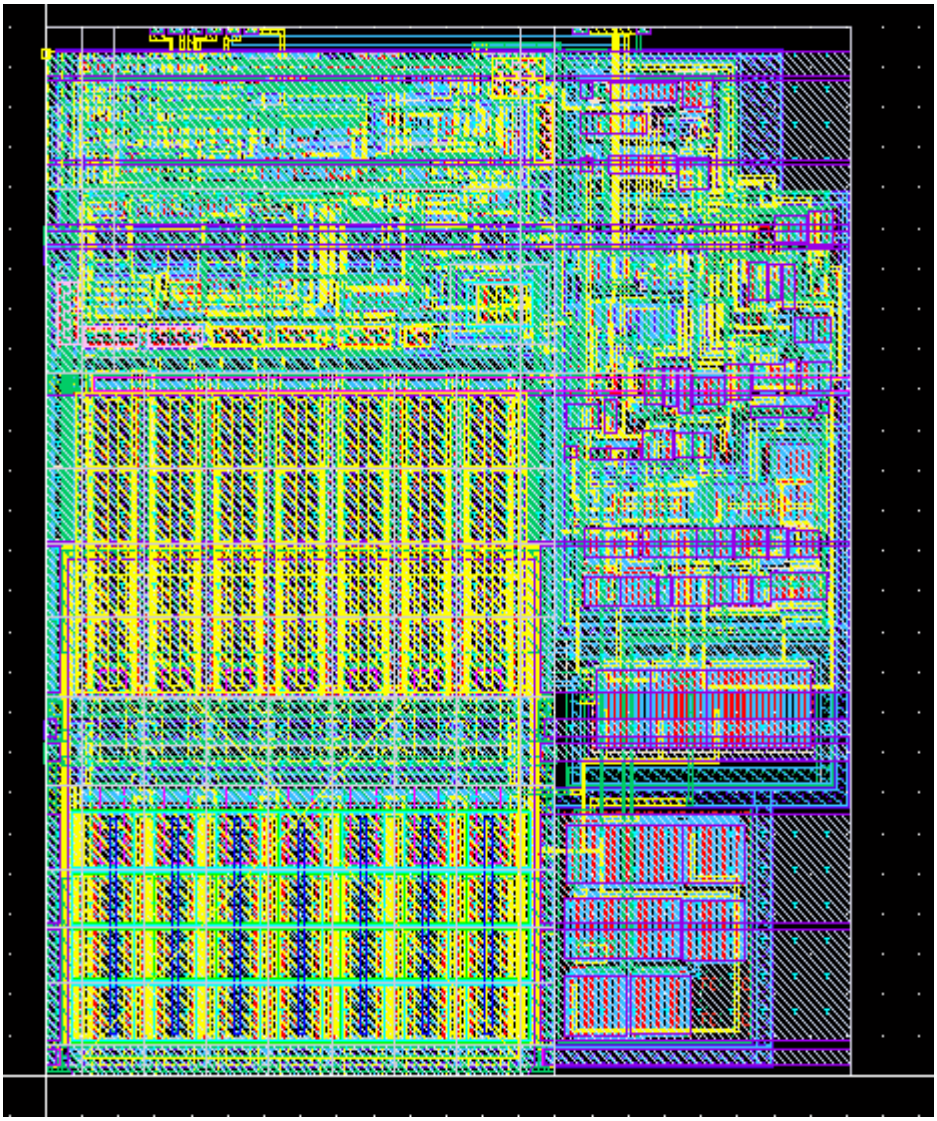


Figure 4.20: Layout of UTOC8ABC output buffer

After that, RC extraction is performed to extract the parasitic resistance and capacitance obtained from the layout. Subsequently, HSPICE simulation is performed again to observe the parasitic effect on the rise and fall time of the waveform. As in the following figures, the delay in the output waveforms after RC-extraction (black) is due to the parasitic effect.

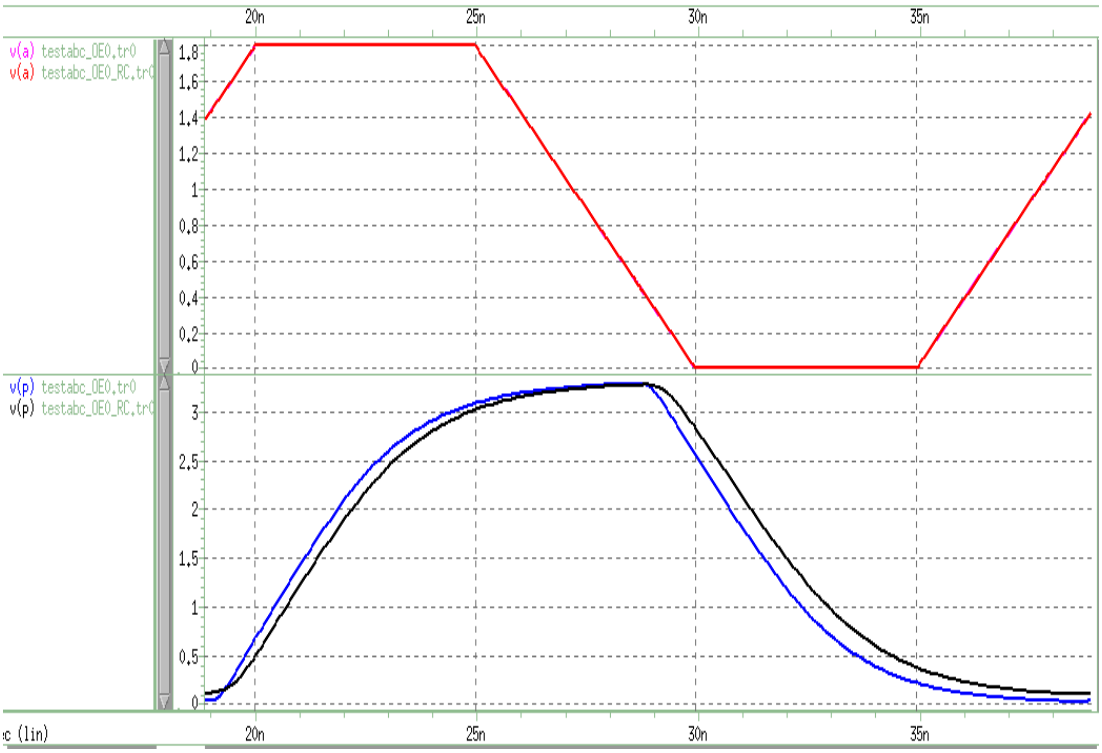


Figure 4.21: Comparison of waveforms for slew rate A before and after RC extraction

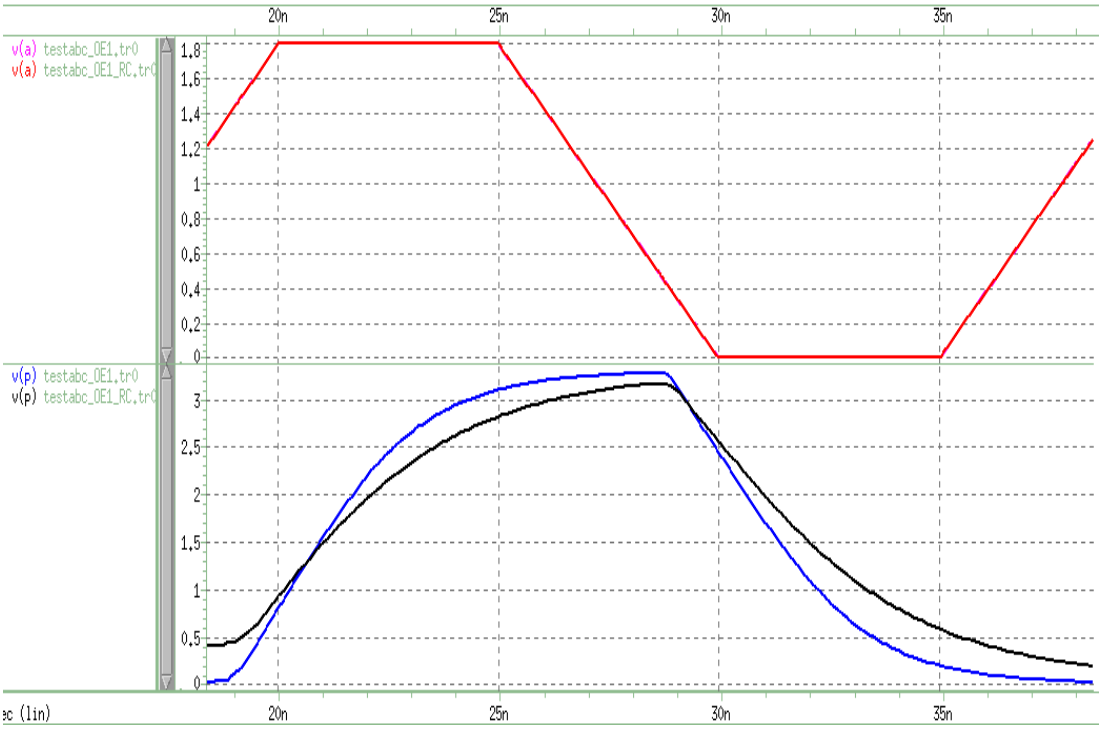


Figure 4.22: Comparison of waveforms for slew rate B before and after RC extraction

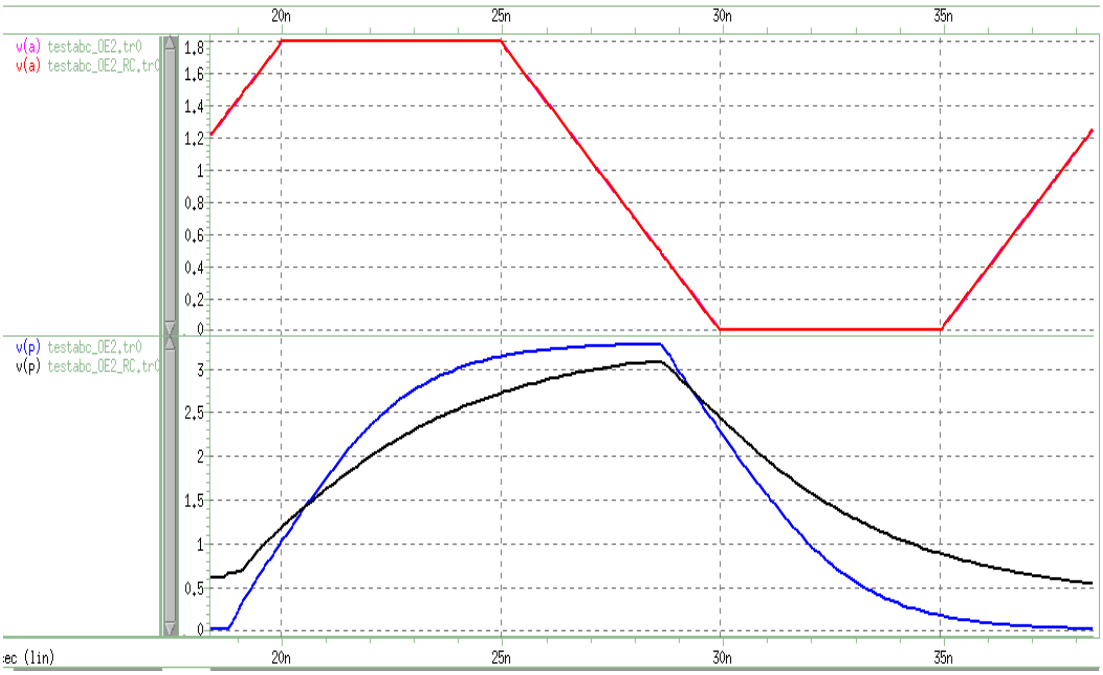


Figure 4.23: Comparison of waveforms for slew rate C before and after RC extraction

Also, UTOC8ABC output buffer is simulated to model all the best case and worst case corners of PVT after RC extraction as shown in the following figures. All of the waveforms after RC extraction (red) show the delay in rise and fall time when compared to the waveforms before RC extraction.

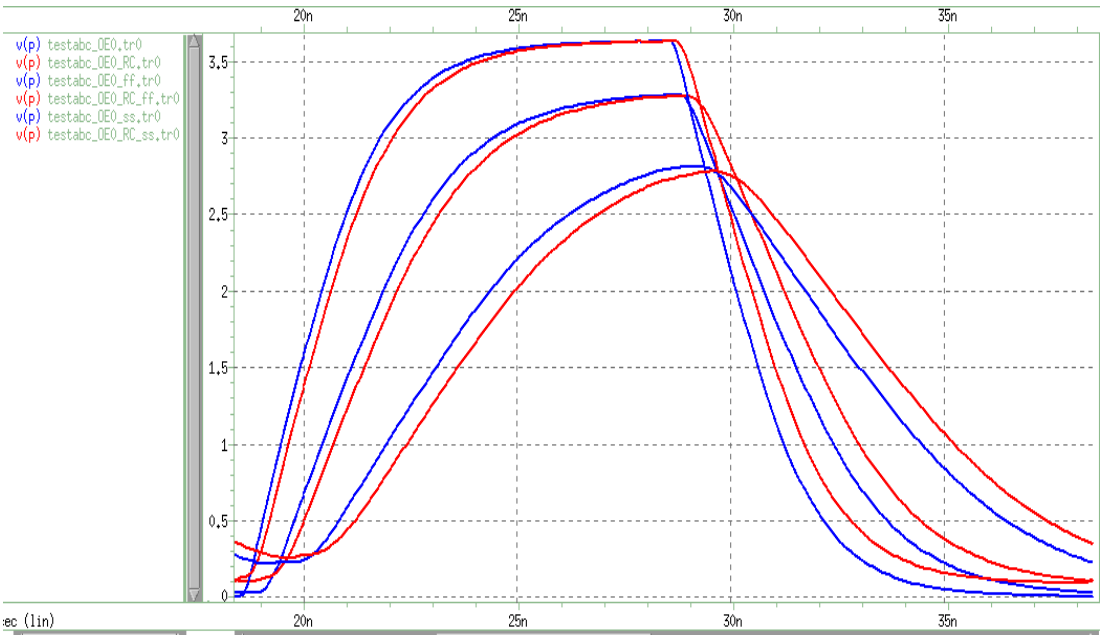


Figure 4.24: PVT waveforms for slew rate A before and after RC extraction

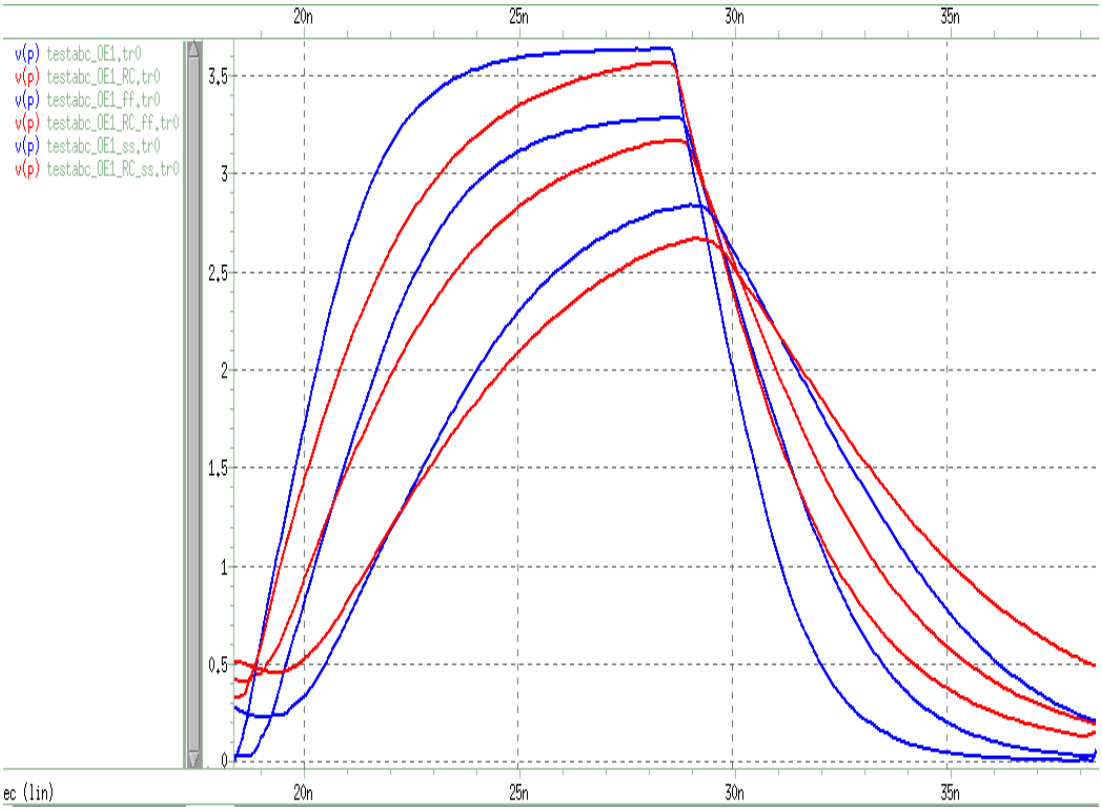


Figure 4.25: PVT waveforms for slew rate B before and after RC extraction

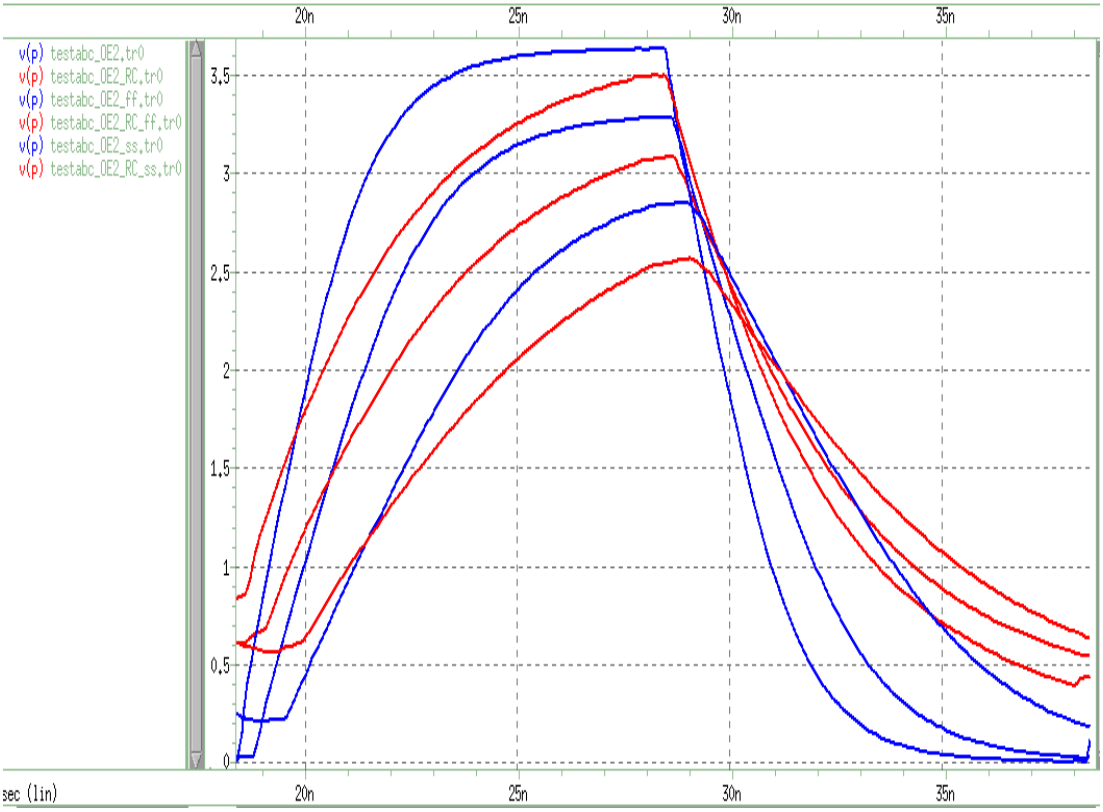


Figure 4.26: PVT waveforms for slew rate C before and after RC extraction

4.5 Design of C.U.P. Programmable Drive Strength Output Buffer

4.5.1 Schematic Design

By referring to the original schematic diagram of UTOC2A output buffer, the input stage, voltage level shifter and output stage of the buffer are identified. The design structure of 2-mA output drive current is repeated for four times and added parallel at the output stage of the buffer. The design of C.U.P. programmable drive strength output buffer is known as UTOC2468A with the schematic design showed in Figure 4.27. The PMOS and NMOS at the output stage of the buffer are controlled independently by their own transistor circuit. There are four output enable pins, namely **OE_0**, **OE_1**, **OE_2** and **OE_3**, for the selection of 2-mA, 4-mA, 6-mA and 8-mA respectively. The input pin is named as **In** while the output pin is named as **P**.

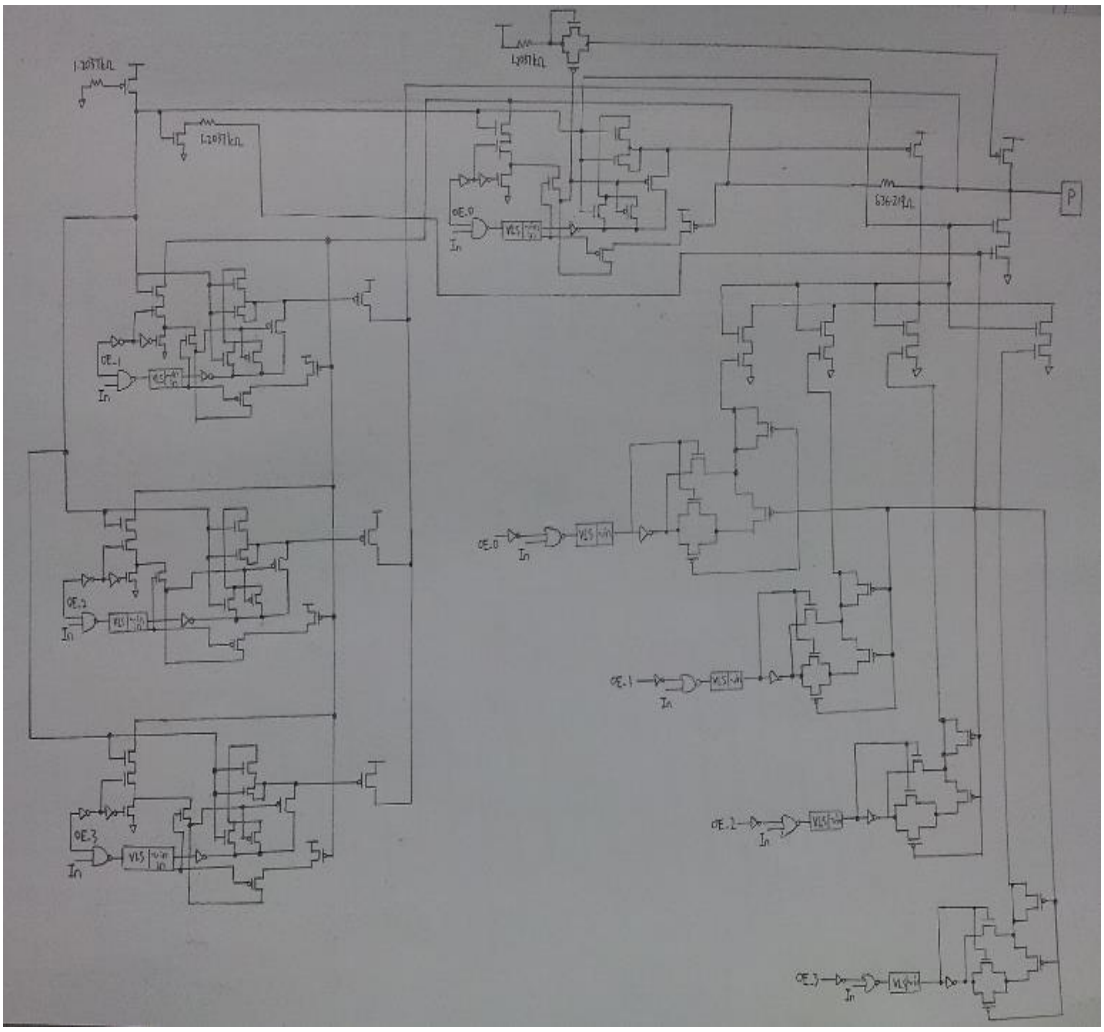


Figure 4.27: Schematic design of UTOC2468A

4.5.2 HSPICE Simulation

The completed schematic design is then converted into CDL netlist with the name of drivestrength_2468.cdl. By including this netlist file in HSPICE script as shown in Appendix D, the HSPICE simulation is performed on the design with the pull up resistor of 10kΩ and the capacitor load of 20pF. The generated waveforms with drive strength 2-mA, 4-mA and 8-mA are compared with that of the UTOC2A, UT0C4A and UTOC8A individual output buffers. Same steps are repeated from the schematic design to the HSPICE simulation for the modification until the output waveforms of UTOC2468A are matched with the waveforms generated by these three individual output buffers. The resulted output waveforms are shown in the following figures.

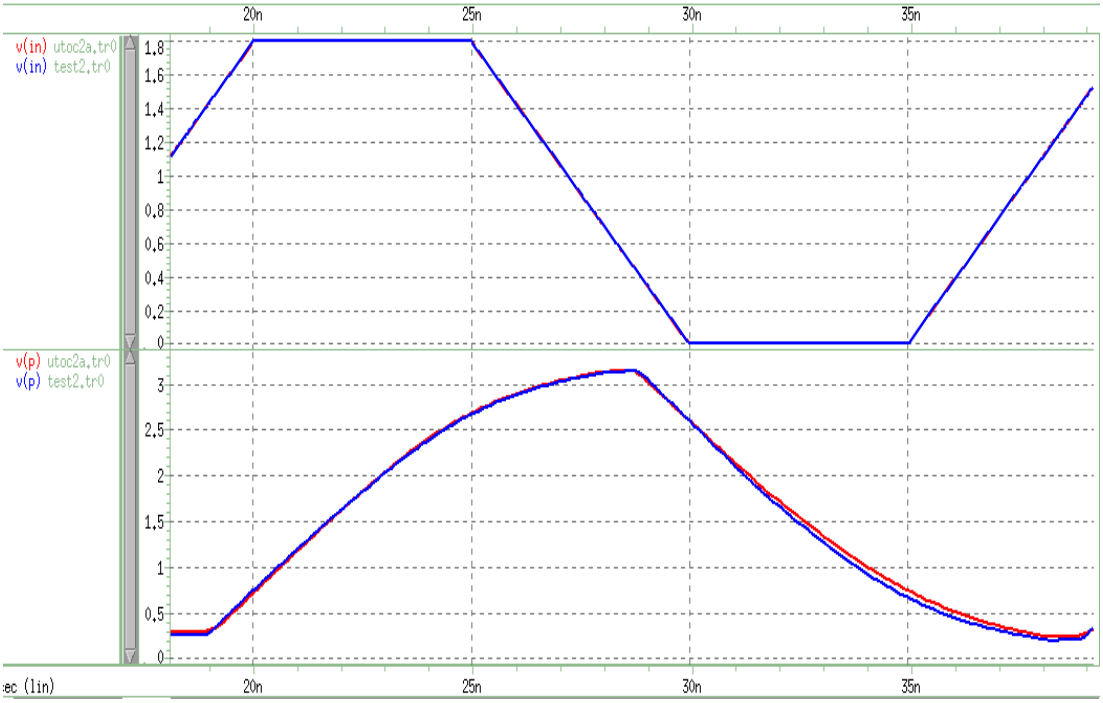


Figure 4.28: Comparison of waveforms for UTOC2A and UTOC2468A (OE_0 is enabled)

When OE_0 pin of UTOC2468A is enabled, the output buffer will provide drive strength of 2-mA with slew rate A for the 20pF capacitor load. This resulted waveform is approximately the same as the output waveform of the original UTOC2A output buffer.

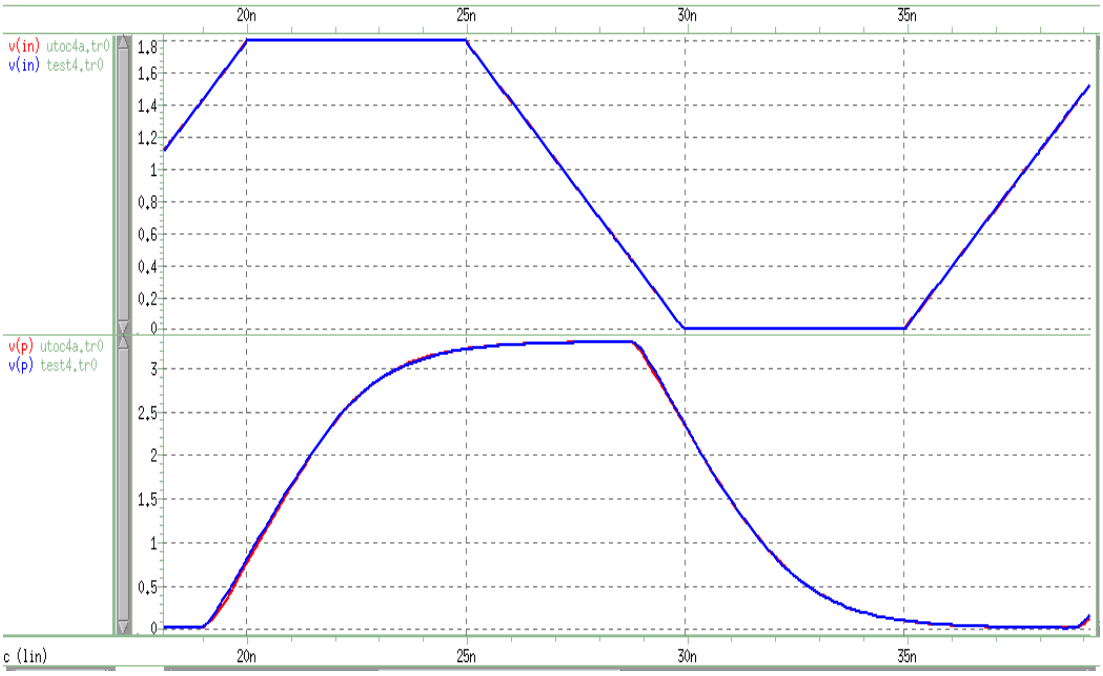


Figure 4.29: Comparison of waveforms for UTOC4A and UTOC2468A (OE_1 is enabled)

When OE_1 pin of UTOC2468A is enabled, the output buffer will provide drive strength of 4-mA with slew rate A for the 20pF capacitor load. This resulted waveform matches with the output waveform of the original UTOC4A output buffer.

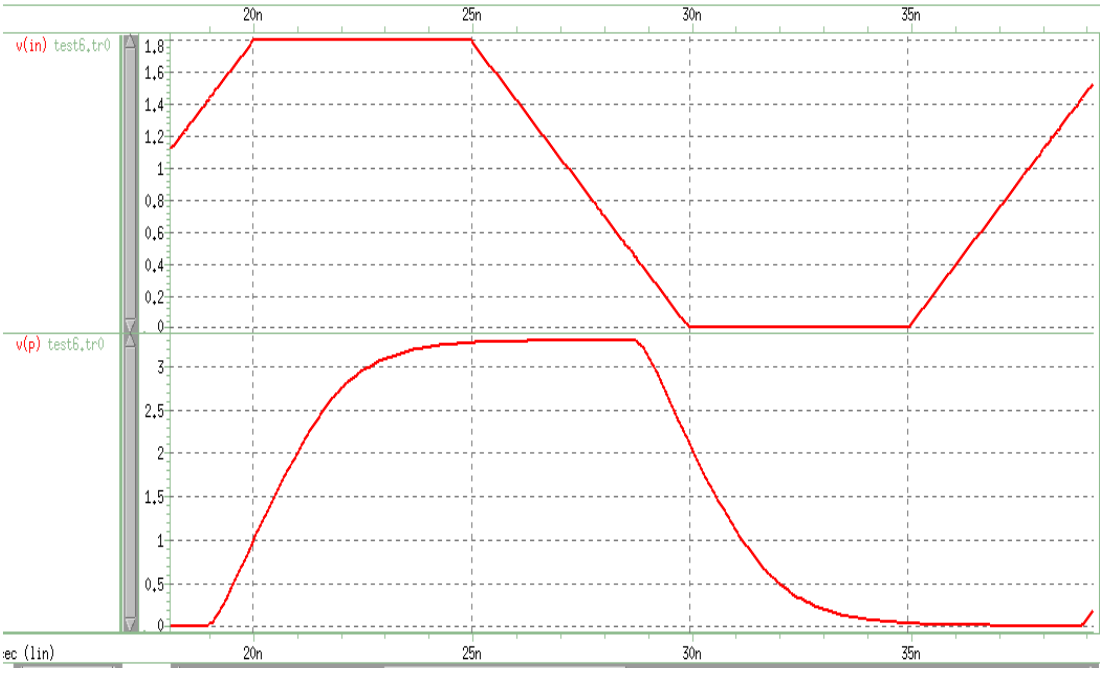


Figure 4.30: Waveform for UTOC2468A with OE_2 is enabled

When OE_2 pin of UTOC2468A is enabled, the output buffer will provide drive strength of 6-mA with slew rate A for the 20pF capacitor load.

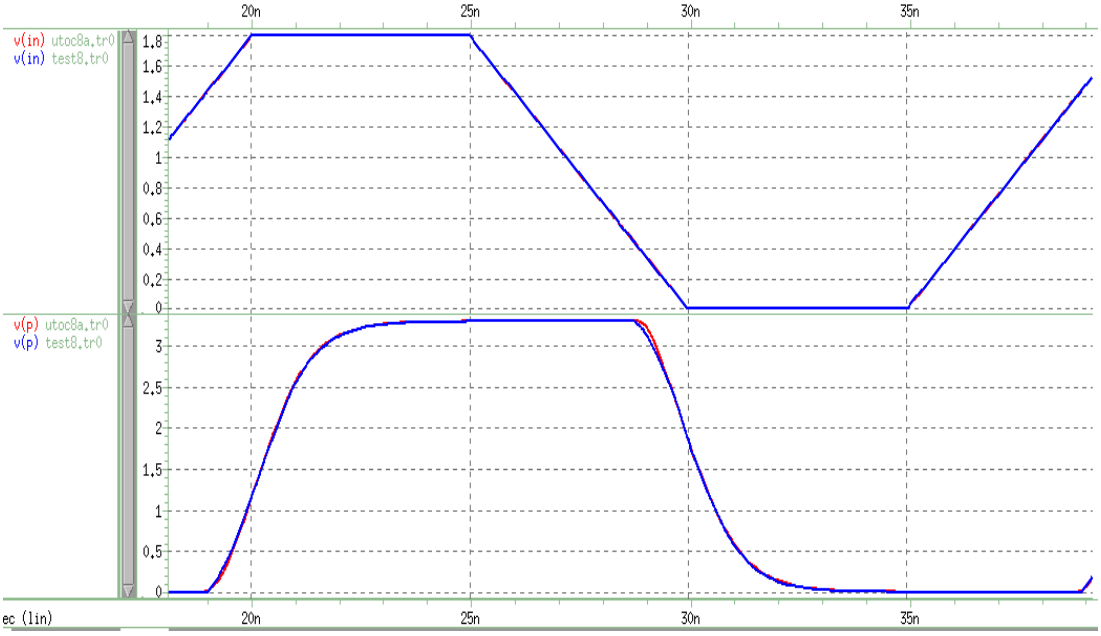


Figure 4.31: Comparison of waveforms for UTOC8A and UTOC2468A (OE_3 is enabled)

When OE_3 pin of UTOC2468A is enabled, the output buffer will provide drive strength of 8-mA with slew rate A for the 20pF capacitor load. This resulted waveform is approximately the same as the output waveform of the original UTOC8A output buffer.

The output waveforms are combined together in Figure 4.32. The drive current of 2-mA, 4-mA, 6-mA and 8-mA are tested for the fixed capacitor load of 20pF. As can be seen, drive current 2-mA (magenta) is not enough to drive the 20pF capacitor load while drive current of 4-mA (red), 6-mA (blue) and 8-mA (black) are enough to drive the load. However, 4-mA drive current is the best choice for driving 20pF load due to its ability for charging and discharging to reach a valid logic level but at the same time, it is not too fast to cause the output ringing problem.

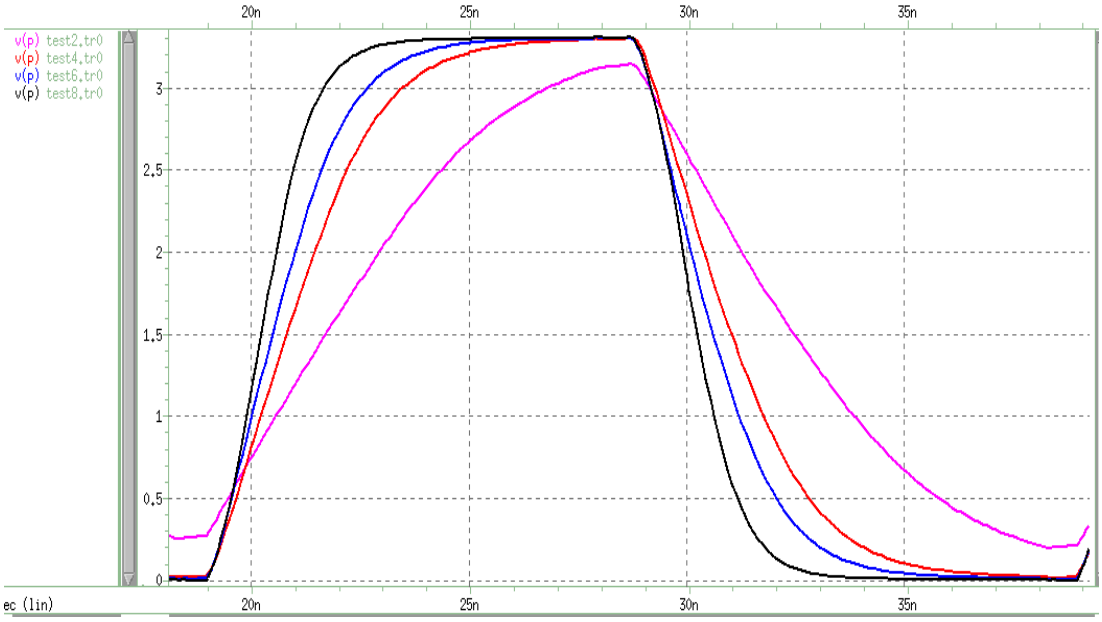


Figure 4.32: Combination waveforms of drive current 2-mA, 4-mA, 6-mA and 8-mA for 20pF

Apart from that, HSPICE simulation is performed again to model all the best case and worst case corners of PVT. The results are shown in the following figures. The best case PVT conditions (red) give fastest rise and fall time while the worst case PVT conditions (blue) show slowest rise and fall time if compared to the typical case (magenta).

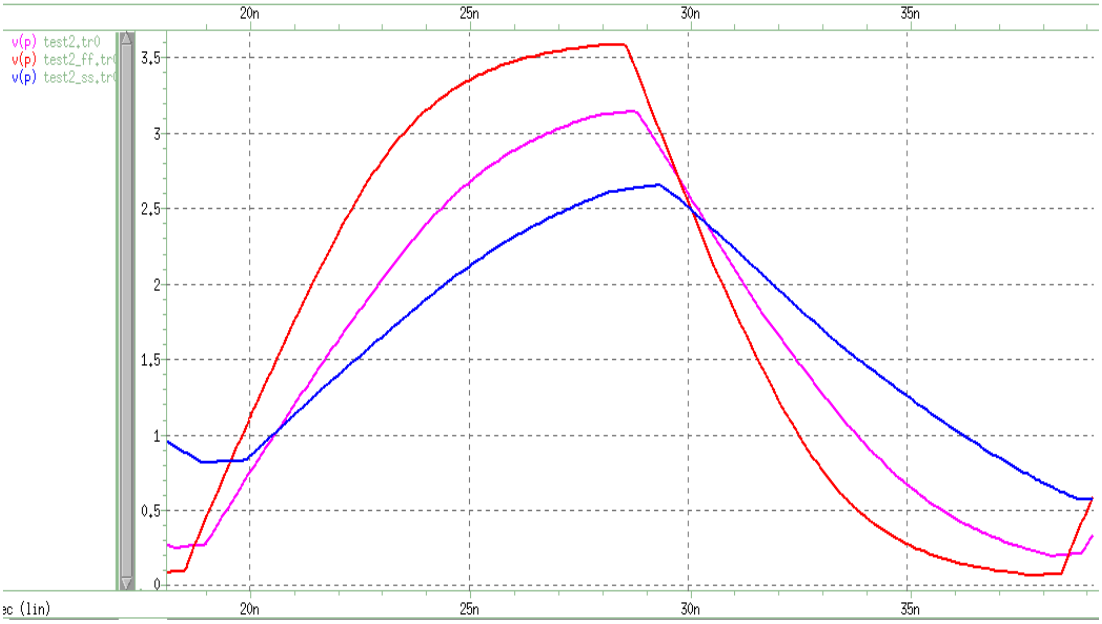


Figure 4.33: PVT waveform for 2-mA drive strength

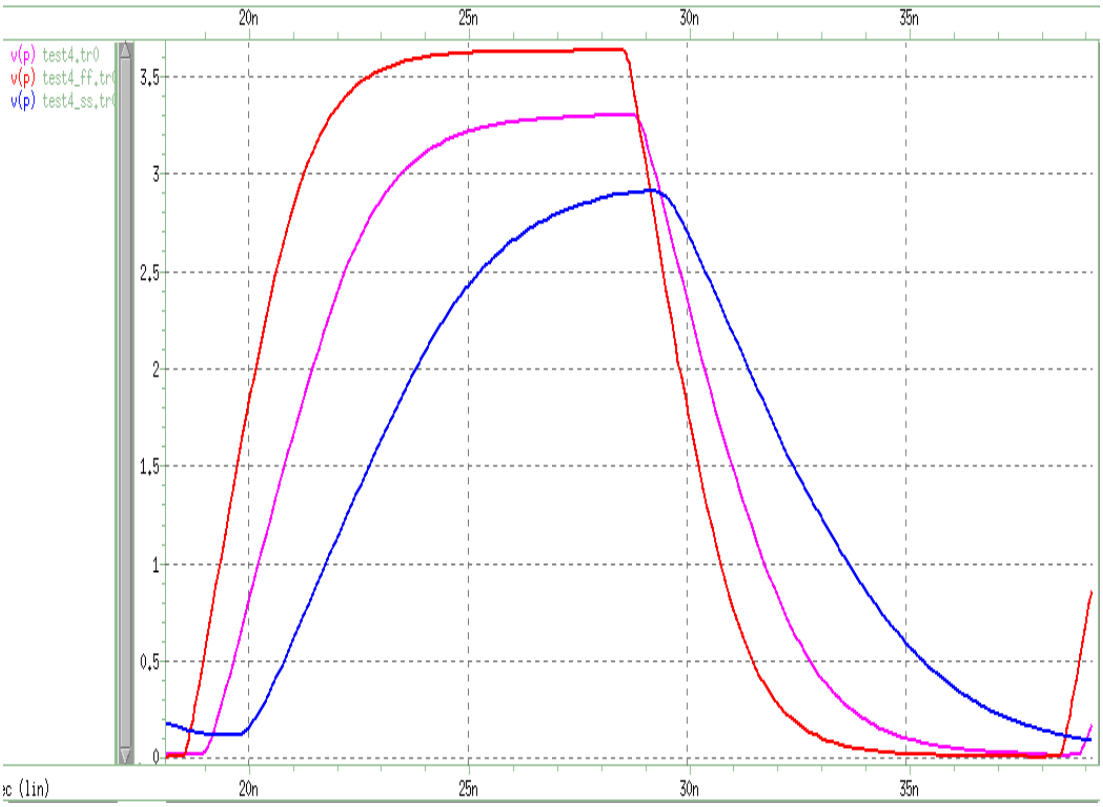


Figure 4.34: PVT waveform for 4-mA drive strength

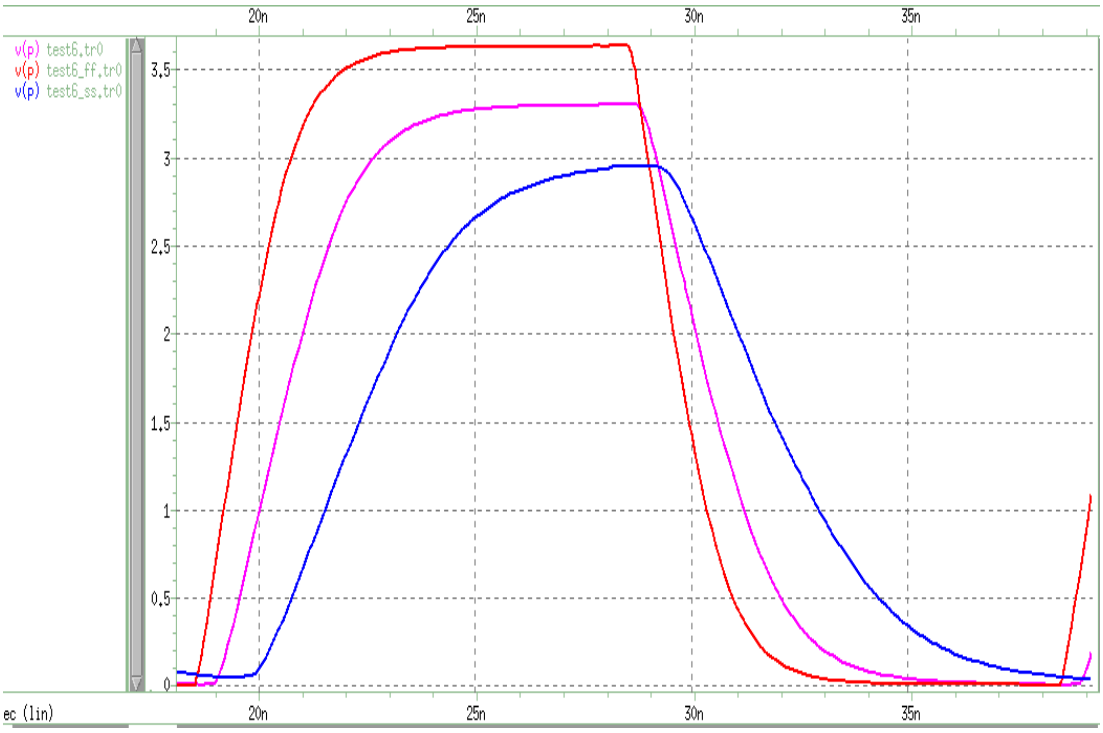


Figure 4.35: PVT waveform for 6-mA drive strength

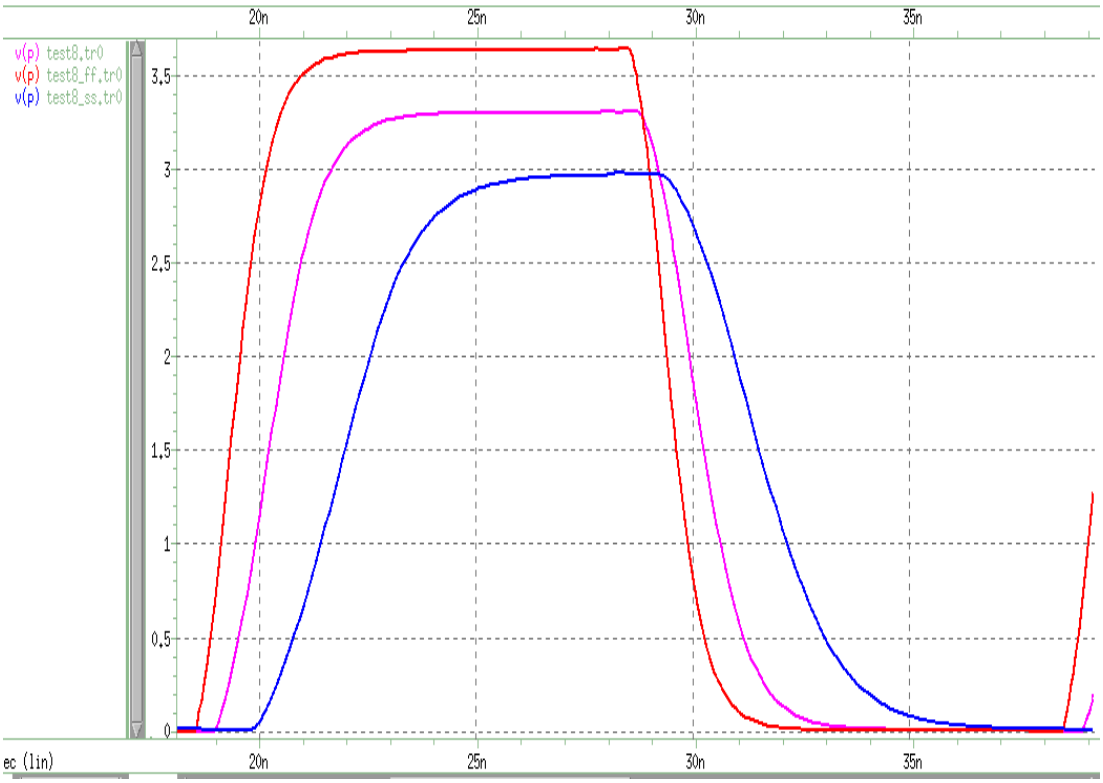


Figure 4.36: PVT waveform for 8-mA drive strength

In brief, smaller drive strength is required for smaller capacitive load while larger drive strength is needed for larger load. The output buffer with programmable drive strength design enables the user to select the correct drive strength for driving the load.

4.5.3 Layout Design and HSPICE Simulation

The layout of designed UTOC2468A output buffer is presented in the n-well CMOS fabrication technology as shown in Figure 4.37. The guard rings are used for shielding purpose and formed by p-substrate with the use of substrate contacts to connect to the ground. This layout is checked for DRC and LVS to ensure that no violation occurs.

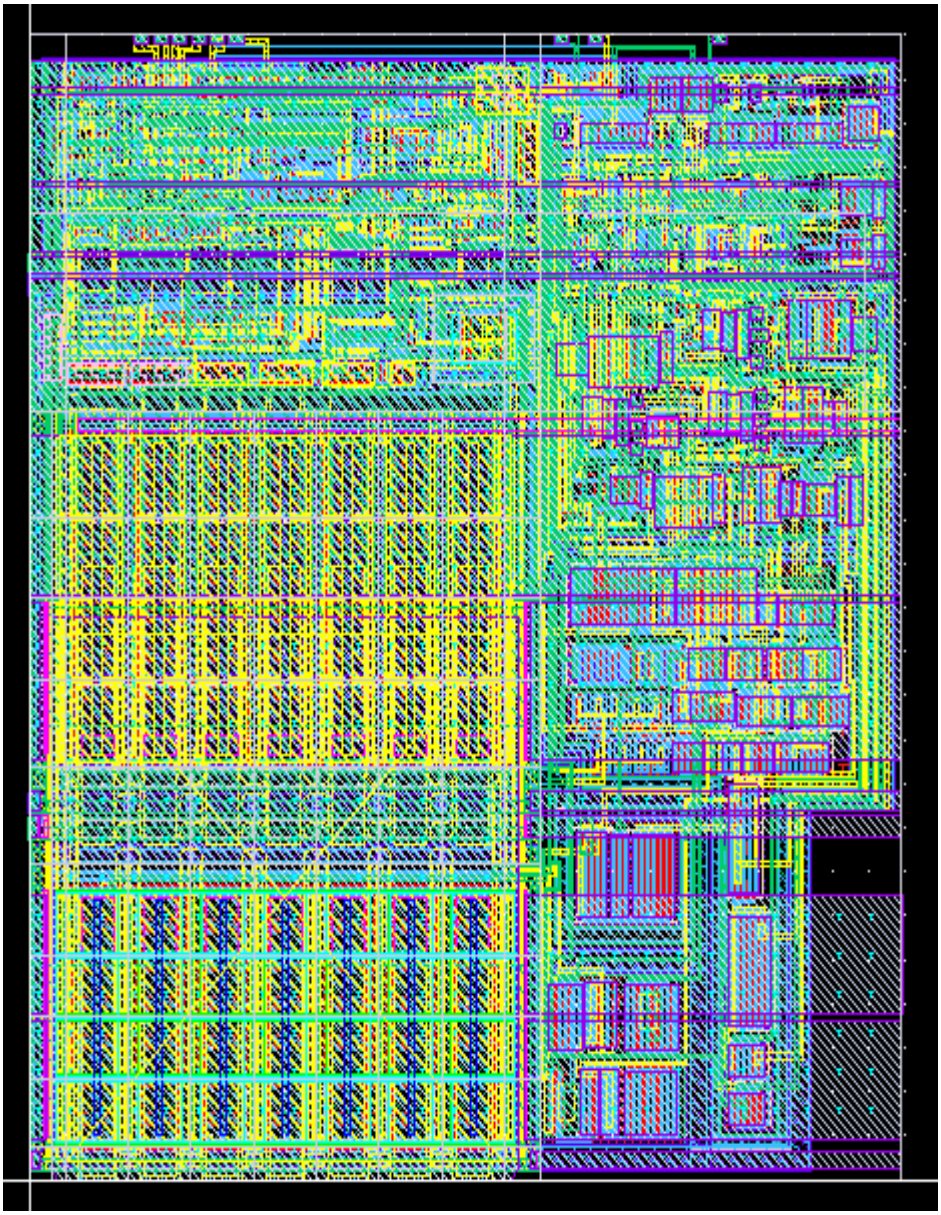


Figure 4.37: Layout of UTOC2468A output buffer

RC extraction is performed to extract the parasitic resistance and capacitance obtained from the layout. Subsequently, HSPICE simulation is performed again to observe the parasitic effect on the rise and fall time of the waveform. As in the following figures, the delay in the output waveforms after RC-extraction (red) is due to the parasitic effect.

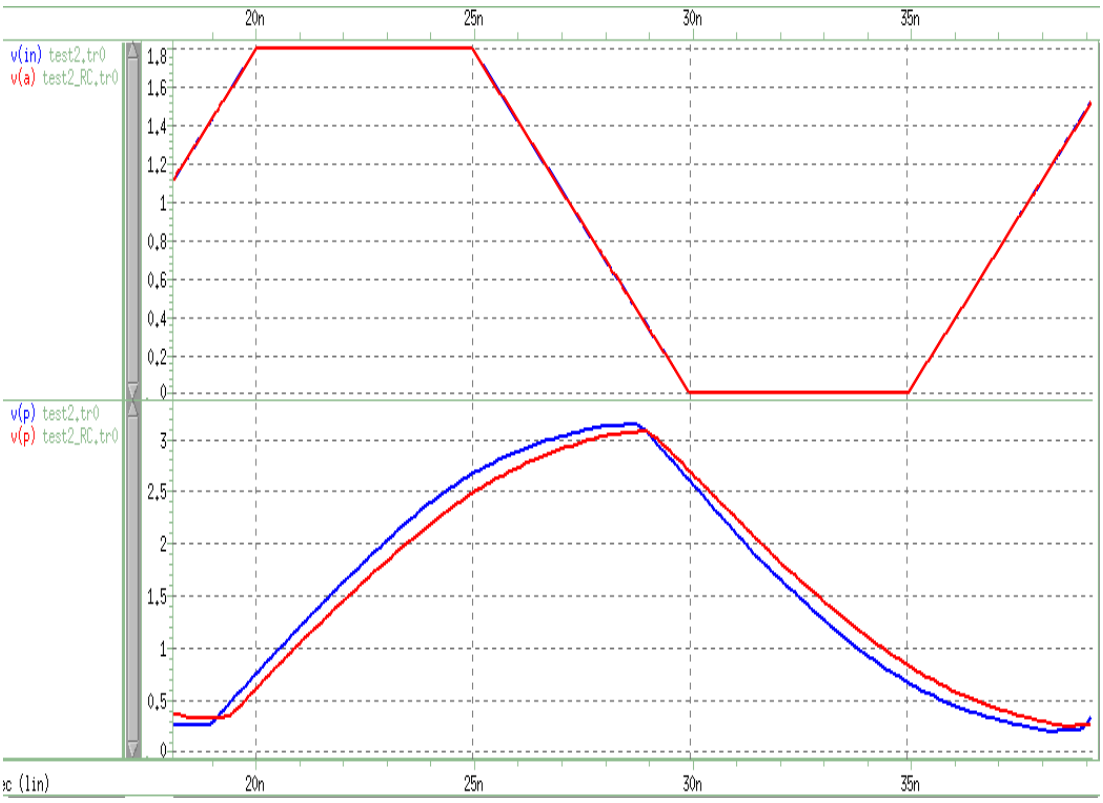


Figure 4.38: Comparison of waveforms for drive strength 2-mA before and after RC extraction

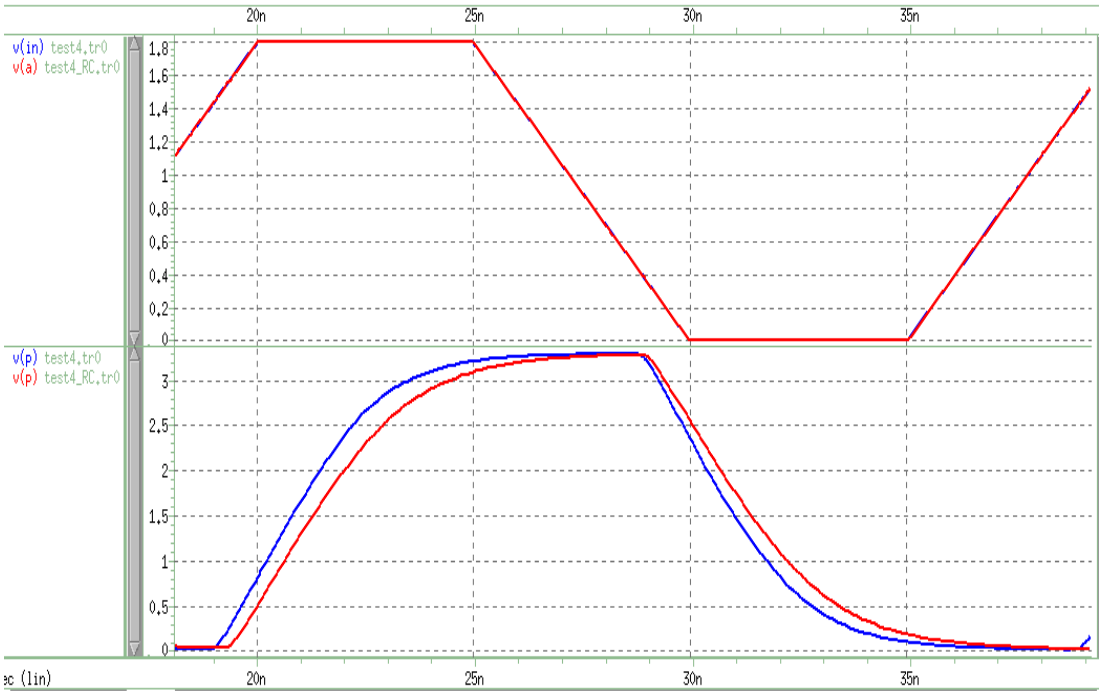


Figure 4.39: Comparison of waveforms for drive strength 4-mA before and after RC extraction

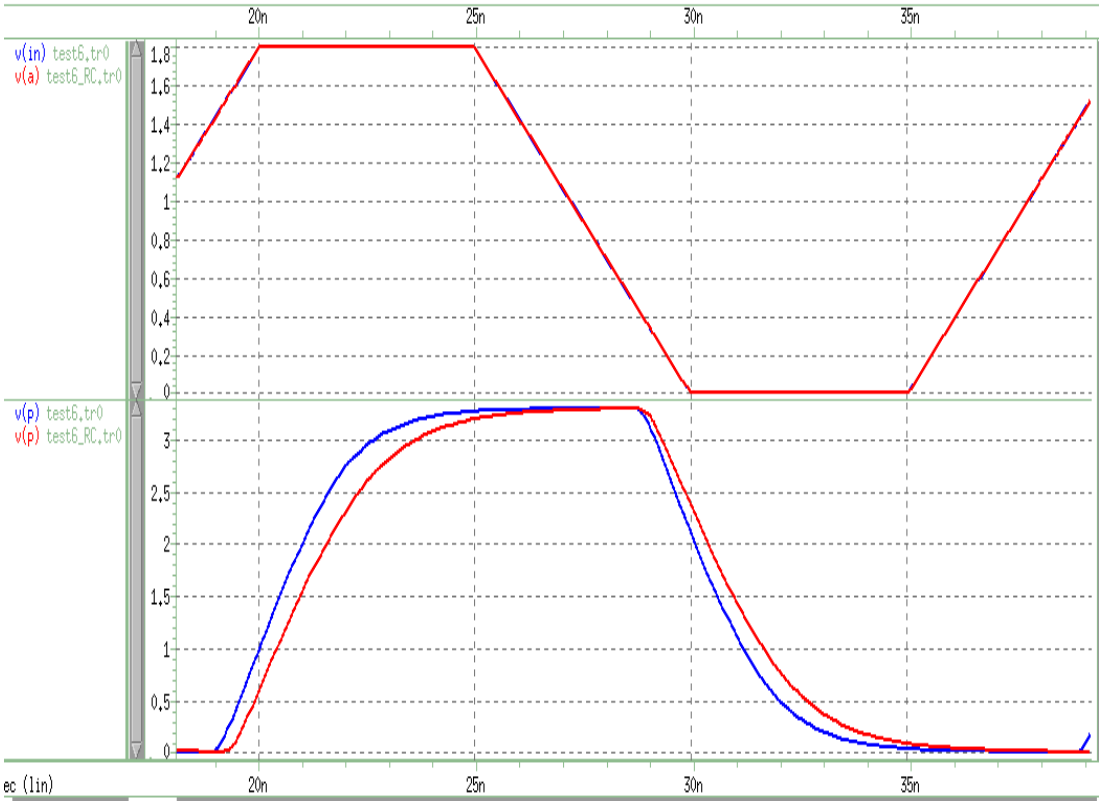


Figure 4.40: Comparison of waveforms for drive strength 6-mA before and after RC extraction

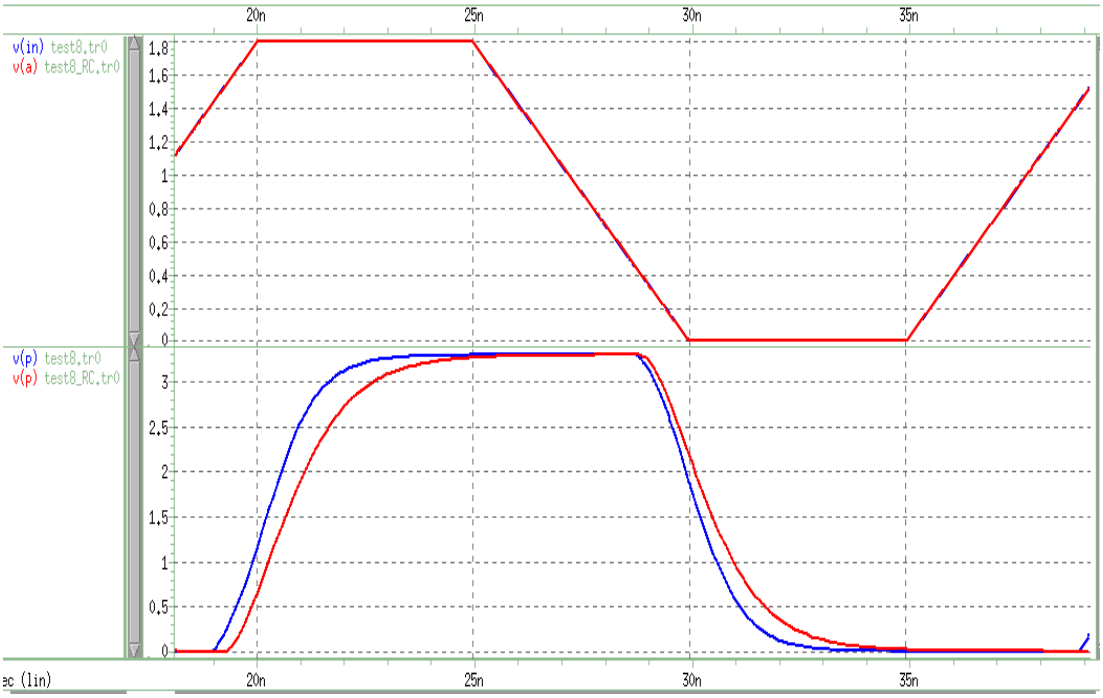


Figure 4.41: Comparison of waveforms for drive strength 8-mA before and after RC extraction

Also, UTOC2468A output buffer is simulated to model all the best case and worst case corners of PVT after RC extraction as shown in the following figures. All of the waveforms after RC extraction (red) show the delay in rise and fall time when compared to the waveforms before RC extraction.

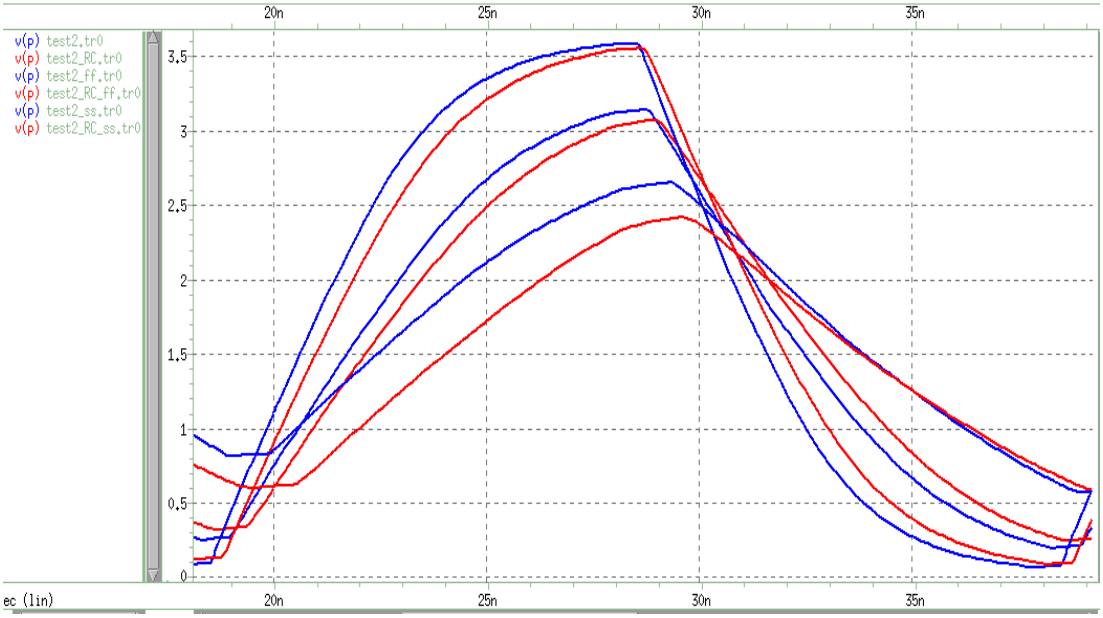


Figure 4.42: PVT waveforms for 2-mA drive strength before and after RC extraction

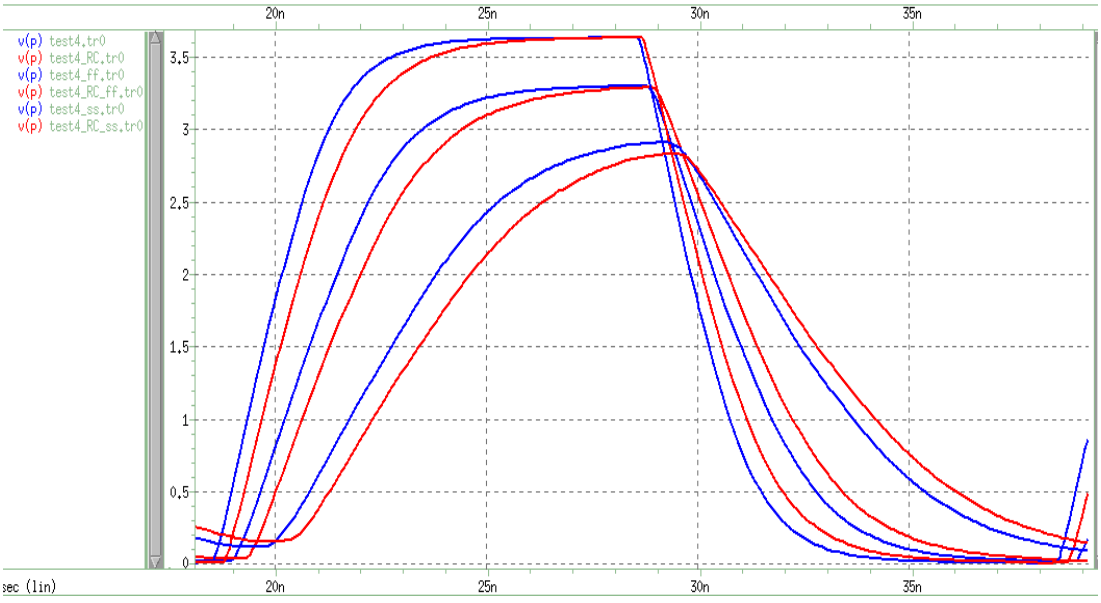


Figure 4.43: PVT waveforms for 4-mA drive strength before and after RC extraction

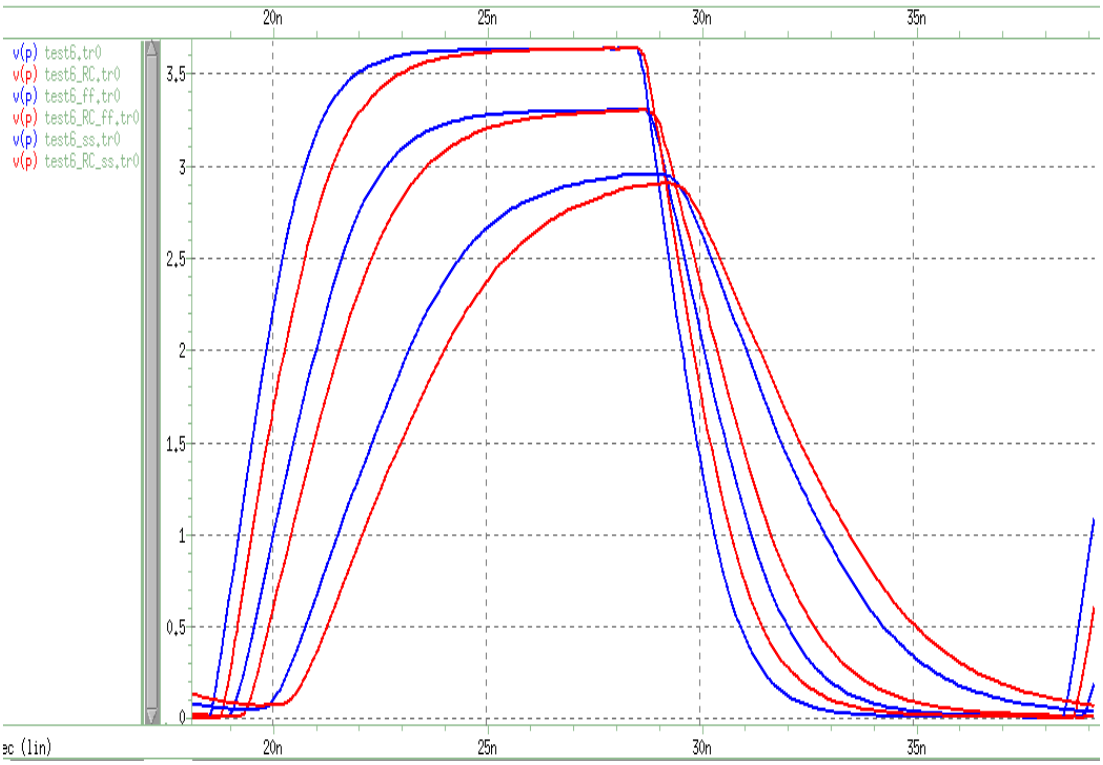


Figure 4.44: PVT waveforms for 6-mA drive strength before and after RC extraction

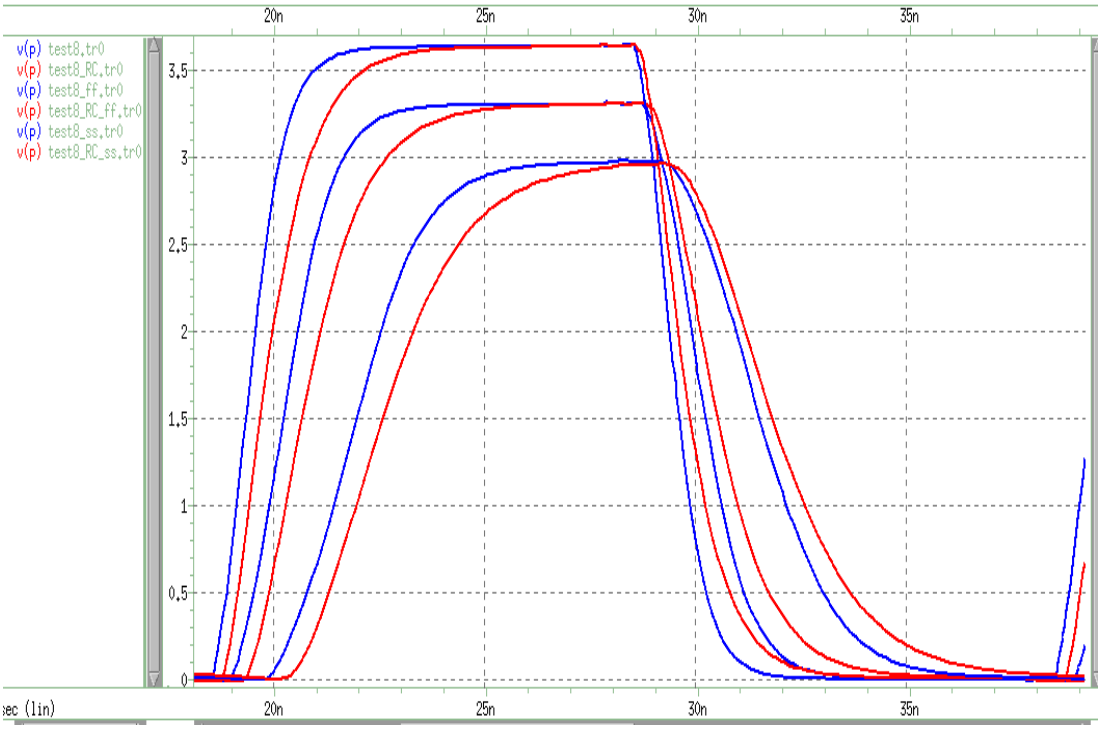


Figure 4.45: PVT waveforms for 8-mA drive strength before and after RC extraction

CHAPTER 5

CONCLUSION AND RECOMMENDATIONS

5.1 Conclusions

In conclusion, the objectives of this project have been fulfilled. First of all, the C.U.P. slew rate controlled output buffer is designed with slow, mid-range and fast slew rate. This output buffer can provide 8-mA drive strength. Based on the load requirement, the slew rate can be efficiently controlled such that the resulting transition time is constant over a large range of output switching condition. This can then solve the problem of unacceptable current spikes and other noise problems during the simultaneous switching of many output buffers.

Besides, the C.U.P. programmable drive strength output buffer is designed so as to drive different loads with 2-mA, 4-mA, 6-mA or 8-mA. This output buffer is featured with slow slew rate. The designed C.U.P. programmable drive strength output buffer enables the user to select the desired operating mode that best suits their applications.

Last but not least, the performance of the C.U.P. output buffers with programmable drive strength and slew rate controlled design are compared with the C.U.P. output buffers without such modifications. In terms of the waveform characteristics, the C.U.P. programmable drive strength and slew rate controlled output buffer contributes to the same rise and fall time as the individual output buffers without the design. However, the all-in-one combination of the slew rate in slew rate controlled output buffer and the all-in-one combination of the drive

strength in programmable drive strength output buffer increase the functionality. Besides, the designed buffers have smaller sizes compared to the total size of three individual output buffers. This follows the current trend of the IC technology, which requires the IC to be as small as possible.

5.2 Recommendations and Future Work

For the current design of C.U.P. slew rate controlled output buffer, the control of slew rate is occurred at the beginning of the rising and falling edge only. The slew rates at the transition state of the waveforms remain almost constant. This is because of the voltage spike and ground bounce problems that happen the most at the change of states from low to high logic or high to low logic. Therefore, the design of slew rate control is focused on the beginning of the rising and falling edge only to minimize the output ringing problem. However, this design can be further improved so that the transition states of the waveforms contribute to the difference in slew rate too.

In addition, the current layout designs of the C.U.P. programmable drive strength and slew rate controlled output buffers need to be improved in terms of the location of transistor circuit. The transistors in the layout can be relocated and re-routed for the optimization purpose. The optimized connection of the transistor circuit is important to avoid wasting space.

Lastly, the C.U.P. programmable drive strength and slew rate controlled output buffers can be taped out and fabricated with the ready designs and layout drawings. The fabricated chips can then be used for further testing and compared with the results of HSPICE simulation. Best case and worst case analysis of PVT corners can also be performed to test for the maximum and minimum voltage as well as the temperature.

REFERENCES

Altera, 2007. *Impact of I/O Settings on Signal Integrity in Stratix III Devices.* [Online]
Available at: https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/an/an476.pdf
[Accessed 18 August 2015].

Anthony, S., 2012. *SoC vs. CPU – The battle for the future of computing.* [Online]
Available at: http://www.extremetech.com/computing/126235-soc-vs-cpu-the-battle-for-the-future-of-computing
[Accessed 15 August 2015].

ARM Ltd., 1995. *Specialty I/O.* [Online]
Available at: http://www.arm.com/products/physical-ip/interface-ip/specialty-io.php
[Accessed 25 August 2015].

Ash, 2013. *PMOS, NMOS Sizing.* [Online]
Available at: https://allthingsvlsi.wordpress.com/2013/04/09/pmos-nmos-sizing/
[Accessed 11 April 2016].

Barnes, W., 2009. *CMOS Non Inverting Buffer.* [Online]
Available at: http://ee307w09-04.pbworks.com/w/page/8855348/FrontPage
[Accessed 13 August 2015].

Chen, S. & Cheng, Y., 2014. SIGNAL SENSING BY THE ARCHITECTURE OF EMBEDDED I/O PAD CIRCUITS. *INTERNATIONAL JOURNAL ON SMART SENSING AND INTELLIGENT SYSTEMS,* 7(1), pp. 196-213.

Cook, M., 2015. *Understanding Outputs.* [Online]
Available at:
http://www.thebox.myzen.co.uk/Raspberry/Understanding_Outputs.html
[Accessed 16 August 2015].

Edaboard, 2006. *in a CMOS circuit, what is meant by drive strength ?.* [Online]
Available at: http://www.edaboard.com/thread74140.html
[Accessed 18 August 2015].

Garcia, F., Coll, P. & Auvergne, D., 1998. Design of a Slew Rate Controlled Output Buffer. *ASIC Conference 1998. Proceedings. Eleventh Annual IEEE International,* pp. 147-150.

Gilbert, K., 2008. *slew rate explained.* [Online]
Available at: http://ken-gilbert.com/slew-rate-explained
[Accessed 20 August 2015].

Godfrey, S., 1996. *An introduction to thermoelectric coolers.* [Online]
Available at: http://www.electronics-cooling.com/1996/09/an-introduction-to-thermoelectric-coolers/
[Accessed 6 April 2016].

Hesener, A., 2010. Electromagnetic Interference (EMI) in Power Supplies. *Fairchild Semiconductor Power Seminar,* pp. 1-16.

Jou, S., Kuo, S., Chiu, J. & Lin, T., 2001. Low Switching Noise And Load-adaptive Output Buffer Design Techniques. *Solid-State Circuits, IEEE Journal,* 36(8), pp. 1239-1249.

Laird Technologies, 2008. *ThermaTEC™ Series HT8,12,F2,4040 Thermoelectric Modules.* [Online]
Available at: http://www.lairdtech.com/brandworld/library/THR-DS-HT8,12,F2,4040,11,W6.pdf
[Accessed 22 January 2016].

Lattice Semiconductor, 2015. *MachXO3 sysIO Usage Guide.* [Online]
Available at:
http://www.latticesemi.com/~/media/LatticeSemi/Documents/ApplicationNotes/MO/MachXO3sysIOUsageGuide.pdf?document_id=50125.
[Accessed 11 August 2015].

Leung, K., 1988. Controlled Slew Rate Output Buffer. *Custom Integrated Circuits Conference, 1988., Proceedings of the IEEE 1988*, pp. 1-4.

Medhat, D., 2009. *Easier cross-domain signal protection for mixed-signal SoCs.* [Online]
Available at: http://www.embedded.com/print/4018829
[Accessed 25 January 2016].

Microsemi, 2012. *Simultaneous Switching Noise and Signal Integrity.* [Online]
Available at: http://www.microsemi.com/document-portal/doc_view/130042-ac263-simultaneous-switching-noise-and-signal-integrity-app-note
[Accessed 20 August 2015].

Ng, W. & Shorten, A., 2011. Efficiency Enhancement and EMI Suppression via Dynamically Adjustable Gate Driving Strength. *Circuits and Systems (MWSCAS), 2011 IEEE 54th International Midwest Symposium on,* pp. 1-4.

Ruetz, J. E., 1992. *Programmable output drive circuit.* United States, Patent No. US5153450.

Schaller, B., 1996. *The Origin, Nature, and Implications of "MOORE'S LAW".* [Online]
Available at: http://research.microsoft.com/en-us/um/people/gray/moore_law.html
[Accessed 19 July 2015].

Schnizlein & Paul, G., 1997. *Programmable drive strength output buffer with slew rate control.* United States , Patent No. 5663664.

SiTime, 2015. *Programmable Features for Best Flexibility.* [Online]
Available at: http://www.sitime.com/technology/mems-oscillators/configurability
[Accessed 19 July 2015].

Stiles, J., 2008. *4.1 Device Structure and Physical Operation.* [Online]
Available at:
http://www.ittc.ku.edu/~jstiles/312/handouts/section_4_1_Device_Structure_and_Physical_Operation_package.pdf
[Accessed 11 August 2015].

Su, H. et al., 2007. *Circuit under pad structure and bonding pad process.* Taiwan, Patent No. US 20070123021 A1.

TE Connectivity , n.d. *Aluminium Housed Power Resistors Type HS Series.* [Online]
Available at: http://www.farnell.com/datasheets/1498243.pdf
[Accessed 27 January 2016].

Von Rosen, J. et al., 2015. A highly dependable self-adaptive mixed-signal multi-core system-on-chip architecture. *Integration, the VLSI Journal*, Volume 48, pp. 55-71.

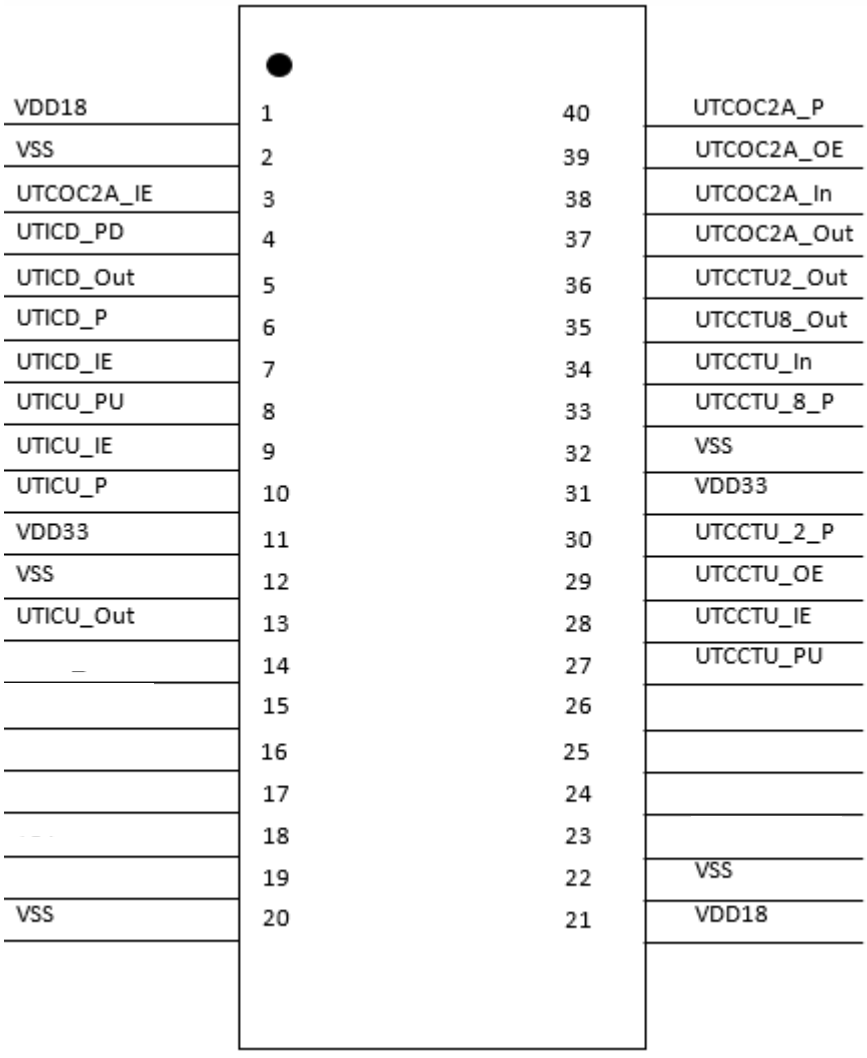
Weste, N. H. E. & Eshraghian, K., 1993. MOS TRANSISTOR THEORY. In: *Principles of CMOS VLSI Design: A Systems Perspective.* Boston: Addison-Wesley Publishing Company, pp. 43-62.

Xilinx, 2014. *Difference between Slew rate and Drive strength.* [Online]
Available at: http://forums.xilinx.com/t5/Virtex-Family-FPGAs/Difference-between-Slew-rate-and-Drive-strength/td-p/415933
[Accessed 17 August 2015].

Yang, L. & Yuan, J., 2005. Output Buffer Design for Low Noise and Load Adaptability. *Circuits, Devices and Systems, IEE Proceedings*, 152(2), pp. 146-150.

APPENDICES

APPENDIX A: Pin Diagram of Ready Chip with C.U.P. Structure



APPENDIX B: HSPICE Script of UTCCTU_2A Output Buffer

```
******** Design cell name: utcctu_2a ***************************
******** Design view name: schematic ***************************

.include original.cdl

******** GLOBAL Net Declarations ********************************
.global VDD18 VDD33 VSS

********* options ********************************************
.options post
.options probe
.option delmax = 0.0000000001   *MAXIMUM ALLOWED TIMESTEP SIZE

******** Define Variables ***************************************
.param v18 = 1.8
.param v33 = 3.3

.temp   27
.LIB "/home/cad/hspice/c18e_core18_io33_header_hspice.modlib" c18e_hp_tt
.LIB "/home/cad/hspice/c18e_core18_io33_header_hspice.modlib" c18e_to_tt
.LIB "/home/cad/hspice/c18e_core18_io33_header_hspice.modlib" c18e_nat_tt
.LIB "/home/cad/hspice/c18e_core18_io33_header_hspice.modlib" c18e_mvt_tt
.LIB "/home/cad/hspice/c18e_core18_io33_header_hspice.modlib" c18e_nvar_tt
.LIB "/home/cad/hspice/c18e_core18_io33_header_hspice.modlib" c18e_res_tt
.LIB "/home/cad/hspice/c18e_core18_io33_header_hspice.modlib" c18e_diode_tt
.LIB "/home/cad/hspice/c18e_core18_io33_header_hspice.modlib"
c18e_mim_cap_tt
.LIB "/home/cad/hspice/c18e_core18_io33_header_hspice.modlib"
c18e_finger_cap_tt
.LIB "/home/cad/hspice/c18e_core18_io33_header_hspice.modlib" c18e_bjt_tt

********* Define buffer ****************************************
Xutcctu2a IN IE OE P PU OUT VDD18 VSS VDD33 VSS UTCCTU2A

********* Define power source **********************************
VD18        VDD18           GND   v18
VD33        VDD33           GND   v33
VSS         VSS             GND   0
```

```
********** Define signal source **********************************
VsigIN IN GND v18
VsigOE OE GND v18
vsigPU PU GND 0v
vsigIE IE GND 0v

****** Define resistor load ************************************
Rload P GND 5.4

********* Transient analysis ************************************
.tran 0.1n 2u uic              *USE INITIAL CONDITION

********* Signals to be monitor *********************************
.probe tranv(VDD18) v(VDD33) v(VSS) v(IN) v(OUT) v(P) i(Rload)
.END
```

APPENDIX C: HSPICE Script of UTOC8ABC Output Buffer

```
******** Design cell name: utoc8abc ************************
******** Design view name: schematic ***********************

.include slew_rate_abc.cdl

******** GLOBAL Net Declarations ************************
.global VDD18 VDD33 VSS

********* options ***************************************
.options post
.options probe
.option delmax = 0.0000000001   *MAXIMUM ALLOWED TIMESTEP SIZE

******** Define Variables *********************************
.param v18 = 1.8
.param v33 = 3.3

.temp   27
.LIB "/home/cad/hspice/c18e_core18_io33_header_hspice.modlib" c18e_hp_tt
.LIB "/home/cad/hspice/c18e_core18_io33_header_hspice.modlib" c18e_to_tt
.LIB "/home/cad/hspice/c18e_core18_io33_header_hspice.modlib" c18e_nat_tt
.LIB "/home/cad/hspice/c18e_core18_io33_header_hspice.modlib" c18e_mvt_tt
.LIB "/home/cad/hspice/c18e_core18_io33_header_hspice.modlib" c18e_nvar_tt
.LIB "/home/cad/hspice/c18e_core18_io33_header_hspice.modlib" c18e_res_tt
.LIB "/home/cad/hspice/c18e_core18_io33_header_hspice.modlib" c18e_diode_tt
.LIB "/home/cad/hspice/c18e_core18_io33_header_hspice.modlib"
c18e_mim_cap_tt
.LIB "/home/cad/hspice/c18e_core18_io33_header_hspice.modlib"
c18e_finger_cap_tt
.LIB "/home/cad/hspice/c18e_core18_io33_header_hspice.modlib" c18e_bjt_tt

********* Define buffer *********************************
Xutoc8abc IN P OE_0 OE_1 OE_2 VDD18 VSS VDD33 VSS UTOC8ABC

********* Define power source ***************************
VD18        VDD18           GND   v18
VD33        VDD33           GND   v33
VSS         VSS             GND   0
```

```
********* Define transient signal source *********************
*pwl=piecewise linear relationship; r=repeated
VsigIN IN GND pwl 10p v18, 5n v18, 10n 0v, 15n 0v, 20n v18,r
VsigOE_0 OE_0 GND v18
VsigOE_1 OE_1 GND 0
VsigOE_2 OE_2 GND 0

****** Define resistor and capacitance load ******************
R VDD33 P 10k
Rload P wire_out 5
Cloadwire_out GND 50p

********* Transient analysis *****************************
.tran 0.1n 80n uic          *USE INITIAL CONDITION

********* Signals to be monitor ***************************
.probe tranv(VDD18) v(VDD33) v(VSS) v(IN) v(P) v(OE_0) v(OE_1) v(OE_2)
.END
```

APPENDIX D: HSPICE Script of UTOC2468A Output Buffer

```
******** Design cell name: utoc2468a **********************
******** Design view name: schematic **********************

.include drivestrength_2468.cdl

******** GLOBAL Net Declarations ***********************
.global VDD18 VDD33 VSS

********* options ***************************************
.options post
.options probe
.option delmax = 0.0000000001   *MAXIMUM ALLOWED TIMESTEP SIZE

******** Define Variables *********************************
.param v18 = 1.8
.param v33 = 3.3

.temp   27
.LIB "/home/cad/hspice/c18e_core18_io33_header_hspice.modlib" c18e_hp_tt
.LIB "/home/cad/hspice/c18e_core18_io33_header_hspice.modlib" c18e_to_tt
.LIB "/home/cad/hspice/c18e_core18_io33_header_hspice.modlib" c18e_nat_tt
.LIB "/home/cad/hspice/c18e_core18_io33_header_hspice.modlib" c18e_mvt_tt
.LIB "/home/cad/hspice/c18e_core18_io33_header_hspice.modlib" c18e_nvar_tt
.LIB "/home/cad/hspice/c18e_core18_io33_header_hspice.modlib" c18e_res_tt
.LIB "/home/cad/hspice/c18e_core18_io33_header_hspice.modlib" c18e_diode_tt
.LIB "/home/cad/hspice/c18e_core18_io33_header_hspice.modlib"
c18e_mim_cap_tt
.LIB "/home/cad/hspice/c18e_core18_io33_header_hspice.modlib"
c18e_finger_cap_tt
.LIB "/home/cad/hspice/c18e_core18_io33_header_hspice.modlib" c18e_bjt_tt

********* Define buffer *********************************
Xutoc2468a IN P OE_0 OE_1 OE_2 OE_3 VDD18 VSS VDD33 VSS UTOC2468A

********* Define power source ***************************
VD18        VDD18           GND   v18
VD33        VDD33           GND   v33
VSS         VSS             GND   0
```

```
********** Define transient signal source ********************
*pwl=piecewise linear relationship; r=repeated
VsigIN IN GND pwl 0n v18, 5n v18, 10n 0v, 15n 0v, 20n v18,r
VsigOE_0 OE_0 GND v18
VsigOE_1 OE_1 GND 0
VsigOE_2 OE_2 GND 0
VsigOE_3 OE_3 GND 0

****** Define resistor and capacitance load ********************
R VDD33 P 10k
Rload P wire_out 5
Cloadwire_out GND 20p

********* Transient analysis *******************************
.tran 0.1n 80n uic              *USE INITIAL CONDITION

********* Signals to be monitor ****************************
.probe tran v(VDD18) v(VDD33) v(VSS) v(IN) v(P) v(OE_0) v(OE_1) v(OE_2)
v(OE_3)
.END
```

APPENDIX E: Datasheet of Thermoelectric Cooler

Laird TECHNOLOGIES

Innovative **Technology** for a **Connected** World

ThermaTEC™ Series HT8,12,F2,4040
Thermoelectric Modules

The ThermaTEC™ Series of thermoelectric modules (TEMs) are designed to operate under cycling conditions or high temperature applications.

This product line is available in multiple configurations and is ideal for applications that require both heating and cooling mode (reverse polarity) or power generation. Assembled with proprietary solder construction, Bismuth Telluride semiconductor material and thermally conductive Aluminum Oxide ceramics, the ThermaTEC™ Series is designed for higher current and larger heat-pumping applications.

FEATURES

- Thermal Cycling Durability
- Power Cycling Reliability
- Precise Temperature Control
- Strong Lead Attachment
- RoHS Compliant
- Continuous Operation at High Temperatures

APPLICATIONS

- Analytical Instrumentation
- PCR Cyclers
- Thermal Test Sockets
- Electronic Enclosure Cooling
- Chillers (Liquid Cooling)
- Power Generation

PERFORMANCE SPECIFICATIONS		
Hot Side Temperature (°C)	25°C	50°C
Qmax (Watts)	72.9	80.0
Delta Tmax (°C)	63	75
Imax (Amps)	8.5	8.5
Vmax (Volts)	14.5	16.4
Module Resistance (Ohms)	1.58	1.78

SUFFIX	THICKNESS (PRIOR TO TINNING)	FLATNESS & PARALLELISM	HOT FACE	COLD FACE	Lead Length
11	0.131" ± 0.005"	0.002" / 0.0035"	Lapped	Lapped	6.0
TA	0.131" ± 0.001"	0.001" / 0.001"	Lapped	Lapped	6.0"
TB	0.131" ± 0.0005"	0.0005" / 0.0005"	Lapped	Lapped	6.0"

SEALING OPTION

SUFFIX	SEALANT	COLOR	TEMP RANGE	DESCRIPTION
R	RTV	White	-60 to 204 °C	Non-corrosive, silicone adhesive sealant
E	Epoxy	Black	-55 to 150 °C	Low density syntactic foam epoxy encapsulant

global solutions: local support™

Americas: +1 888.246.9050
Europe: +46.31.420530
Asia: +86.755.2714.1166

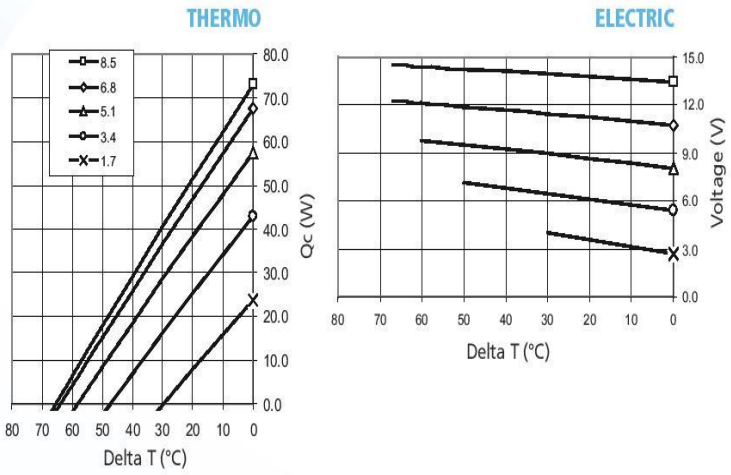
clv.customerpos@lairdtech.com
www.lairdtech.com

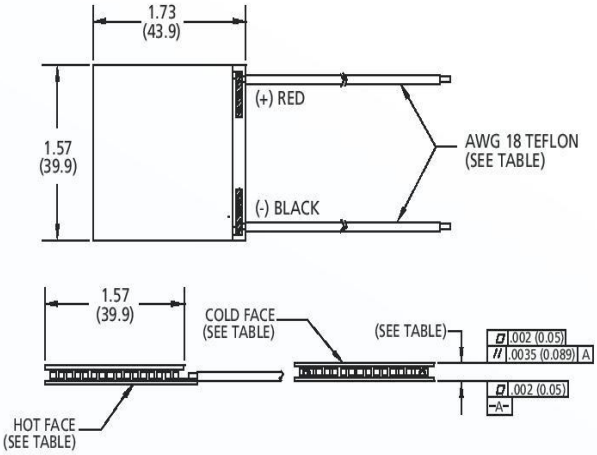
Laird TECHNOLOGIES

Innovative **Technology** for a **Connected** World

ThermaTEC™ Series HT8,12,F2,4040
Thermoelectric Modules

Performance Curves at Th = 25°C





Ceramic Material: Alumina (Al_2O_3)
Solder Construction: 271°C, Proprietary

OPERATING TIPS

- Max Operating Temperature: 175°C
- Do not exceed Imax or Vmax when operating module
- Reference assembly guidelines for recommended installation

THR-DS-HT8,12,F2,4040 0509

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Laird Technologies:
430160-502

APPENDIX F: Datasheet of Power Resistor

Aluminium Housed Power Resistors

Type HS Series

Key Features

- Established product with proven reliability
  - Leading the way with over 50 years of design and manufacturing experience
- 5 Watts to 300 Watts (500 Watt and 1000 Watt versions available)
  - Largest range on the market
- Versatile product
  - Bench mark in every industry
- Custom designs
  - Windings, terminations, mountings - We have a solution for your application
- Low resistance, low inductance and higher voltage versions available
  - Specialising the standard

Applications

- Braking Resistor
- Balancing Resistor
- Capacitor Charging & Discharging
- Crowbar
- Filter
- Electrical Machinery general use
- Available through Distribution

TE Connectivity are the leading European supplier of standard and custom designed aluminium housed resistors for general-purpose use, power supplies, power generation and the traction industry. The HS is a range of extremely stable, high quality wire wound resistors capable of dissipating high power in a limited space with relatively low surface temperature. The power is rapidly dissipated as heat through the aluminium housing to a specified heatsink.

The resistors are made from quality materials for optimum reliability and stability. TE can test resistors to conform to relevant international, MIL or customer specifications.

TE are happy to advise on the use of resistors for pulse applications and to supply information for high voltage use and low-ohmic value, alternative mountings and termination type.

Characteristics - Electrical
HSA & HSC - 5 Watts to 75 Watts

	HSA5	HSA10	HSA25	HSA50	HSC75
Dissipation @ 25°C with Heatsink (Watts):	10	16	25	50	75
Without Heatsink:	5.5	8	12.5	20	45
Ohmic Value Min (Ohms):	R01	R01	R01	R01	R05
Max:	10K	15K	36K	100K	50K
Max. Working Voltage (DC or ACrms) Volts:	160	265	550	1250	1400
Dielectric Strength (AC Peak) Volts:	1400	1400	2500	2500	5000
Stability (% resistance change, 1000 hours) (%):	1	1	1	1	2
Standard Heatsink - Area (mm²):	41500	41500	53500	53500	99500
Thickness (mm):	1	1	1	1	3
Number of Mounting Holes:	2 hole	2 hole	2 hole	2 hole	4 hole

Characteristics - Electrical
HSC - 100 Watts to 300 Watts

	HSC100	HSC150	HSC200	HSC250	HSC300
Dissipation @ 25°C with Heatsink (Watts):	100	150	200	250	300
Without Heatsink:	50	55	50	60	75
Ohmic Value Min (Ohms):	R05	R10	R10	R10	R10
Max:	100K	100K	50K	68K	82K
Max. Working Voltage (DC or ACrms) Volts:	1900	2500	1900	2200	2500
Dielectric Strength (AC Peak) Volts:	5000	5000	5600	5600	5600
Stability (% resistance change, 1000 hours) (%):	2	2	3	3	3
Standard Heatsink - Area (mm²):	99500	99500	375000	476500	578000
Thickness (mm):	3	3	3	3	3
Number of Mounting Holes:	4 hole	4 hole	6 hole	6 hole	6 hole

Dimensions are in millimeters and inches unless otherwise specified. Values in brackets are standard equivalents.

Dimensions are shown for reference purposes only. Specifications subject to change.

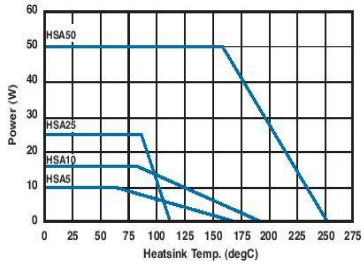
For email, phone or live chat, go to: **te.com/help**

Type HS Series

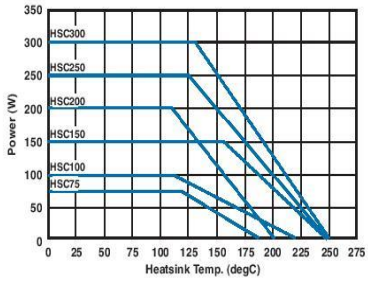
Characteristics - Electrical

Long Term Stability:	For improvements in long-term stability, resistors must be derated as follows; for 50% of stated ΔR maximum dissipation must not exceed 70% of rating; for 25% of stated ΔR maximum, dissipation must not exceed 50% of rating
Insulation Resistance:	Dry: 10,000MΩ minimum. After moisture test: 1000MΩ minimum.
Heat Dissipation:	Although the use of proprietary heat sinks with lower thermal resistance is acceptable, up rating is not recommended. The use of proprietary heat sink compound to improve thermal conductivity is recommended for optimum performance of all sizes but essential for HSC200, HSC250 & HSC300
Specification:	Temperature coefficient below 100R, 50ppm/°C Temperature coefficient above 100R, 30ppm/°C Tolerance, 5% standard: 10%, 3%, 2%, 0.5% & 0.25% available Tolerance for values below R10, 10% standard

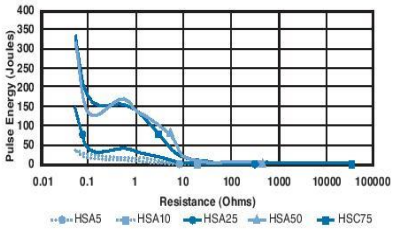
Derating Curve HSA5 to HSA50



Derating Curve HSC75 to HSC300



Pulse Energy HSA5 to HSC75

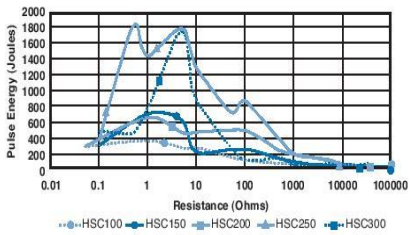


Dimensions are in millimeters and inches unless otherwise specified. Values in brackets are standard equivalents.

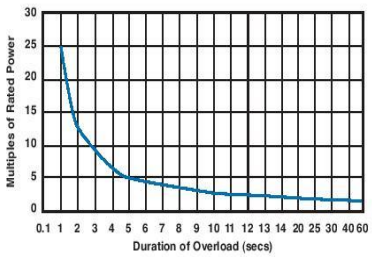
Dimensions are shown for reference purposes only. Specifications subject to change.

Type HS Series

Pulse Energy HSC100 to HSC300

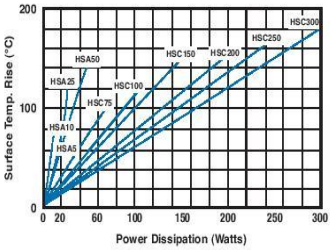


Power Overload



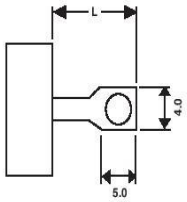
This graph indicates the amount that the rated power (at 20°C) of the standard HS Series resistor may be increased for overloads of 100mS to 60S

Surface Temperature Rise



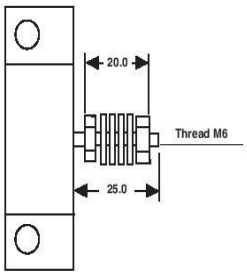
For resistor mounted on standard heatsink, related to power dissipation

Product Specifications - HSA5 - HSC150



Type	L
HSA5, 10	7
HSA25, 50	10
HSC75, 100, 150	8

HSC200 - HSC300



Dimensions are in millimeters and inches unless otherwise specified. Values in brackets are standard equivalents.

Dimensions are shown for reference purposes only. Specifications subject to change.

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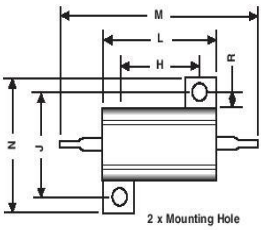
Type HS Series

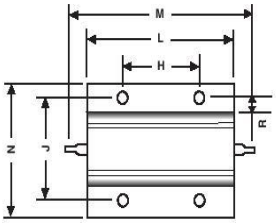
Dimensions - HSA5 - HSA50



2 x Mounting Hole

HSA5 - 2.4mm
HSA10 - 2.4mm
HSA25 - 3.3mm
HSA50 - 3.3mm

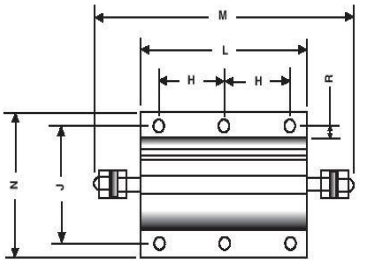
HSC75 - HSC150



4 x Mounting Hole

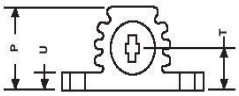
HSC75 - 4.4mm
HSC100 - 4.4mm
HSC150 - 4.4mm

HSC200+



6 x Mounting Hole

HSC200 - 5.3mm
HSC250 - 5.3mm
HSC300 - 6.5mm



Type	H±0.3	J±0.3	K±0.2	L Max	M Max	N Max	P Max	R Min	T±0.5	U Max
HSA5	11.3	12.4	2.4	17.0	30.0	17.0	9.0	1.9	4.3	2.5
HSA10	14.3	15.9	2.4	21.0	36.5	21.0	11.0	1.9	5.2	3.2
HSA25	18.3	19.8	3.3	29.0	51.0	28.0	15.0	2.8	7.2	3.2
HSA50	39.7	21.4	3.3	51.0	72.5	30.0	17.0	2.8	8.2	3.2
HSC75	29.0	37.0	4.4	49.0	71.0	47.5	26.0	5.0	11.5	3.5
HSC100	35.0	37.0	4.4	65.5	87.5	47.5	26.0	5.0	11.5	3.5
HSC150	58.0	37.0	4.4	98.0	122.0	47.5	26.0	5.0	11.5	3.5
HSC200	35.0	57.2	5.3	90.0	143.0	73.0	42.0	5.6	20.25	5.3
HSC250	44.5	57.2	5.3	109.0	163.0	73.0	42.0	5.6	20.25	5.3
HSC300	52.0	59.0	6.5	128.0	180.0	73.0	42.0	5.6	20.25	5.3

How to Order

HS	A	50	680R	J
Common Part	**Mounting Style**	**Power Rating**	**Resistance Value**	**Tolerance**
HS - Standard NHS - Low Inductance	A - Single Opposing mounting Feet B - Flange One Side C - Flange Two Sides	10 Watt = HSA5 16 Watt = HSA10 25 Watt = HSA25 50 Watt = HSA50 75 Watt = HSA75 etc	0.1ohm (100 mille ohms) R10 1ohm (1000 mille ohms) 1R0 1K (1000 ohms) 1KO	F - 1% G - 2% E - 3% J - 5% K - 10%