INTEGRATED CIRCUIT DESIGN OF A POWER MANAGEMENT UNIT FOR RADIO FREQUENCY IDENTIFICATION TRANSPONDER

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A project report submitted in partial fulfilment of the requirements for the award of Master of Engineering (Electronic Systems)

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April 2019

DECLARATION

I hereby declare that this project report is based on my original work except for citations and quotations which have been duly acknowledged. I also declare that it has not been previously and concurrently submitted for any other degree or award at UTAR or other institutions.

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APPROVAL FOR SUBMISSION

I certify that this project report entitled **"INTEGRATED CIRCUIT DESIGN OF A POWER MANAGEMENT UNIT FOR RADIO FREQUENCY IDENTIFICATION TRANSPONDER"** was prepared by **SARASWATHI** has met the required standard for submission in partial fulfilment of the requirements for the award of Master of Engineering (Electronic Sytems) at Universiti Tunku Abdul Rahman.

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In addition, I would also like to express my gratitude to my loving parents, husband, in laws and friends who had helped and given me encouragement along the way.

ABSTRACT

The target of this study is to structure a Power Management Unit (PMU) that creates distinctive control units from a steady input voltage. The reason for this unit is to drive the peripherals working at various levels and are installed in a single application. The structure of PMU bolsters the power spare mode activity, for example, the unit supplies voltage just when there is an interest for the activity to be performed by the control unit or solicitation from the peripheral. This task uses OrCAD programming as an EDA simulation device to reproduce the age display and investigate the heap profile. From the outcome, it demonstrates the model created is working effectively and the goal is accomplished. This study proposes a strategy to structure the PMU that holds the ability to produce four distinctive control units. This has been demonstrated with the mimicked outcomes created utilizing PSpice test system in OrCAD apparatus. The yield is created just when there is an activity required from the peripheral.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF SYMBOLS / ABBREVIATIONS

EDA	Ecteronic Design Automation
CAD	Computer-Aided Design
EMF	Electromagnetic Field
p.f	Power Factor
VAR	Variable Amplitude Regulator

LIST OF APPENDICES

CHAPTER 1

INTRODUCTION

1.1 Background of the Study

Ordinarily, an energy harvesting framework is made out of an electronic device that changes over the energy accessible in the earth in which it works into electrical energy (Matey et al., 2015) and a Power Management Unit (PMU) that concentrates and stores the energy from the converter and conveys it as a directed power supply to the heap. (Arunya et al., 2013) Energy harvesting methods from vibrations and movement have just been hailed as alluring power supply answers for web of-things gadgets (Sravya and Brahmaiah, 2017) and wearable remote sensors (Vijaya et al., 2014) . Energy harvesting frameworks can be utilized to energize batteries, which are a standout amongst the most well-known power hotspots for remote sensor modules. In addition, they can completely supplant batteries, in this manner making sensor modules free from the run of the mill intermittent upkeep of battery-powered frameworks and improving the self-sufficient activity of the detecting modules (Ker and Chen, 2006). This lined up with the current pattern of the present low electronic device which is self-supportability. Notwithstanding, restriction in power diminishes the number of capacities in a chip. Therefore, the requirements to join energy harvesting advancements into a battery-less remote correspondence framework.

For the deployed wireless micro-sensor networks, they are always expected to be functioning as long as possible. System lifetime is thus a very important metric to characterize the wireless micro-sensor networks. Here, the lifetime refers to the time until the micro-sensor network can no longer provide acceptable quality results (Chen, 1996), and usually the malfunction of the network is due to the death of part of the micro-sensor nodes. Extending the lifetime of the micro-sensor nodes is thus essential.

For the conventional micro-systems which are powered by the energy storage element, e.g. battery, the capacity of the energy storage element is a crucial factor that affects the device lifetime. The miniature volume of the devices would always constrain the capacity of the energy storage element (Chen, 1996). And the energy storage element will be quickly depleted after the devices operating for a while. For most of the micro-systems, especially micro-sensor nodes, they are required to be autonomously operating without human intervention, and it is impossible to return the

large numbers of nodes to the charging docks for charging. Moreover, for some devices, e.g., those being embedded in building infrastructure, it is impossible to get the devices out to replace the depleted batteries. The devices would become useless since then on.

Recently, the idea of “perpetual computation” was recommended which suggested using energy harvesting or scavenging techniques in the micro-system designs (Chao et al., 2007). Energy harvesting is the process by which energy is collected from the environment. The environmental energy source can be the solar, vibration, temperature gradients, and radioactive deterioration of substances, etc., and they can be transformed to electrical energy using diverse methods (Meninger et al., 2001). The harvested electrical energy at that moment is deposited in the energy buffer, e.g., super-capacitor, rechargeable battery, or directly used to power the micro-systems. Here, since the environmental energy be existent everywhere and typically, the energy volume can be boundless, the devices lifespan can thus be prolonged to virtual eternity.

So as to do as such, a synchronized circuit of numerous energy-harvesting plans and a PMU to deal with the sources is required. This venture, for the most part, will be on the structuring, reproduce and investigation of the PMU utilizing Mentor Graphics EDA instrument. Later on, this PMU can be possibly be interfaced with eager for power recipients, for example, RFID sensor transponder or any battery-less remote frameworks.

1.2 Problem Statement

Driven by the ever-growing power crisis, the design methodology of modern power management systems for multicore processors has shifted towards a cross-layer design methodology. This entails the development of the power management platform by jointly considering system level requirements. This enables modern power management systems to be tailored according to their load applications and corresponding operational environments.

As per mentioned earlier, the limitation in power reduces the number of functions in a chip. To move forward and to cater more functions, more power is required. This cannot be achieved with a single source of energy but required a multi-source of energy. In order to manage the multi-source of energy, PMU is very important. From the sources, the energy output varies with time since it is dependable on the environmental conditions. Besides that, power demands for any receiver are different and vary with time. Providing uniform control units to the circuitry would

result in high power density. Thus, we need an algorithm to allocate different power converter with time. A low power circuit to implement such algorithm is needed.

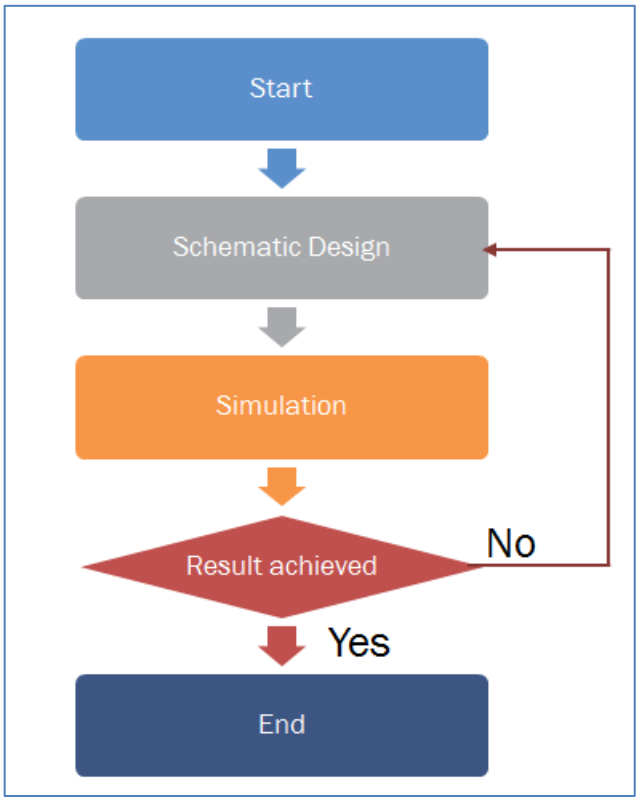
1.3 Objective of Project

The objectives of this project are to

- Design the PMU using EDA Tools
- Simulate the PMU to be able to produce multiple output

1.4 Scope of the Project

The proposed methodology of this project is using EDA tools. PMU blocks will be designed, simulated and analysed using EDA tools. Blocks will be designed from the transistor levels up to the final blocks and each stage simulation results will be generated and analysed as per below.



1.5 Contribution of the Study

This project will be helpful for any PMU utilization with single input and multiple output and also serves the energy saving mode.

CHAPTER 2

LITERATURE REVIEW

2.1 Power Management Unit (PMU)

Energy harvesting has an expanding enthusiasm to accomplish the independent task with the base intercession (Chiwandea et al., 2018) In any case, because of the variable energy accessible from energy sources, the power conveyed to the electronic device is likewise a factor. All things considered, won't probably play out the assignments with a similar exhibition consistently. Subsequently, a PMU is basic to deal with the power reaped, put away and conveyed to the implements (Vijaya et al., 2014). What's more, the PMU ought to convey the base power to the heap to play out the undertaking in the most productive manner. Figure 2.1 indicates distinctive dimensions where a PMU can be structured(Ker and Chen, 2006).As delineated in Figure 2.1, PMU can be executed in the transistor level to help dynamic voltage and recurrence scaling (DVFS) to lessen power utilization. Also, numerous voltage areas, power gating and check gating help in upgrading the general power utilization of devices. Further, a PMU can be actualized in the framework or the application level as a major aspect of the working framework. (Sravya and Brahmaiah, 2017)

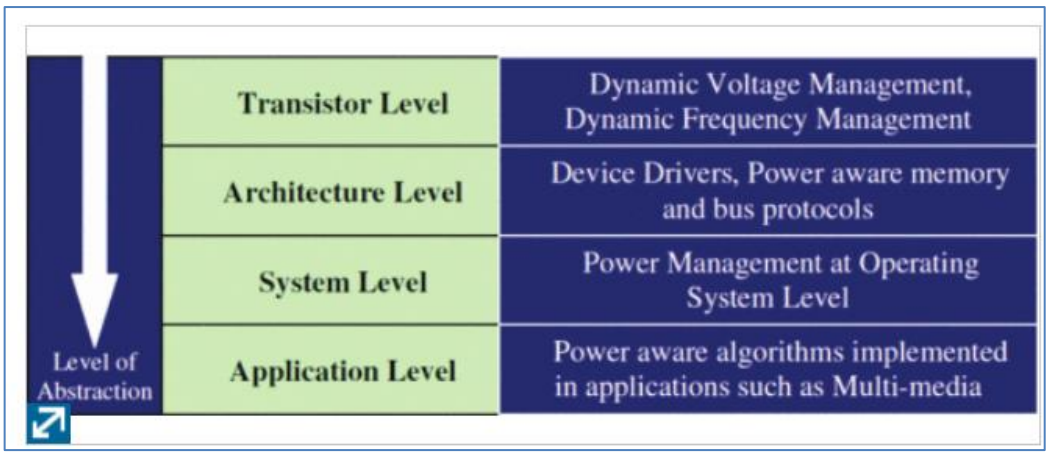


Figure 2.1: Power Management on Different Level of Abstractions (Sravya and Brahmaiah, 2017)

A couple of studies done beforehand on power management configuration, for example, PMU engineering for multi-source energy harvesting framework in wearable implements. The energy harvesting framework uses warm and vibration collectors as energy sources. Likewise, the PMU is intended to control the reaped energy just as to

deal with the power conveyed to an ECG processor. Further, the PMU creates diverse signs to empower and cripple the processor relying upon the accessible energy(Ker and Chen, 2006).

PMU is one of the crucial building blocks for energy harvesting systems. It should generate stable supply voltages for the other blocks inside the devices, but also adjust its operation behavior to extract extreme power from the energy transducer with the purpose of extend the device lifespan. For the energy harvesting structure with hybrid supplies, the power management system should also schedule and manage energy utilization among different energy sources. In the following chapters, we will take energy as an example of an energy source and propose different PMU designs for energy harvesting applications (Vijaya et al., 2014).

The majority of the works done before comprising of PMU overseeing two or single sources, with respect to this venture, the PMUs will deal with the energy gathered from numerous sources, for example, warm energy, sunlight-based energy, vibration energy, and furthermore RF/EM energy (Spies et al., 2007).

It is well-established practice to use reactive power compensation to increase the transmittable power in PMU. Fixed capacitors such as capacitor banks or precisely exchanged capacitors and reactors have for some time been utilized to build the relentless state power transmission by controlling the voltage profile along the lines. These implements are quicker than the precisely exchanged voltage controllers, for example, line tap changers (Chen and Rincón-Mora, 2007). Additionally, they are massive and dynamic control of matrix voltage sounds is beyond the realm of imagination (Torres et al., 2008). The majority of this hardware has a typical trademark in that the fundamental receptive power required for the remuneration is produced or consumed by a conventional capacitor or reactor banks and the thyristor switches are utilized just for the control of joined responsive impedance these banks present to the framework amid progressive times of a connected voltage. Thus, customary thyristor-controlled compensators present variable permission to the transmission organize and hence for the most part change the framework impedance (Roundy et al., 2004).

PMU has customarily utilized sorts of gear for receptive power trade at the purpose of normal coupling. These PMU can bolster voltages of basic burdens, improve transient strength and hoses the power motions (Jiang et al., 2005). PMU has similar abilities, yet with a higher control transmission capacity and the extra capacity

of giving higher flows at low voltage (Torres and Rincón-Mora, 2005). (Torres and Rincón-Mora, 2005)

PMU is a power device dependent on the voltage source converter standard (Austin et al., 1992). The innovation normally, being used is, contingent upon the power units and all-out rating, a few bit voltage source converter, constrained by advanced methods and associated with the power framework in shunt through a channel and perhaps a coupling transformer (Ker and Chen, 2006). Though it comprises of the thyristor-controlled reactor, and thyristor or precisely exchanged capacitors (Austin et al., 1992). It very well may be considered as a shunt impedance dictated by the parallel association of the capacitor and the powerful inductance of the thyristor-controlled reactor (Torres and Rincón-Mora, 2005).

In any case, when the PMU is utilized for responsive power age, the converter itself can keep the capacitor charged to the required power units. This is cultivated by controlling yield voltage fall behind air conditioning framework voltage by a little edge. Along these lines, the converter assimilates a little measure of genuine power from the air conditioner framework to meet its interior misfortunes and keep the capacitor voltage at the ideal dimension. A similar instrument can be utilized to increment or abatement the capacitor voltage. The receptive and genuine power trade between the PMU and the air conditioner framework can be controlled freely of one another. Any mix of genuine power age or retention with power age or assimilation is reachable if the PMU is outfitted with an energy amassing device of appropriate limit.

These power electronics devices are very vulnerable in terms of harmonic distortion. They inject harmonic currents in the grid and active control is very difficult for harmonic mitigation (Roundy et al., 2004).

2.2 Two Bit and Three Bit Voltage Source Converter

Single phase inverters can be designed in various ways namely two bit and mixed source converters for PMU. From the literature review point, this study focusing on 2-bit and 3-bit voltage source converters which have been discussed below:

2.2.1 Two Bit Inverters

The converters which produce a yield voltage or current with level either +ve/ -ve are known as worthless converters. In high power and high voltage applications, this no-

account inverter anyway has a few confinements in working at high recurrence primarily because of exchanging calamities and imperatives of implement rating.

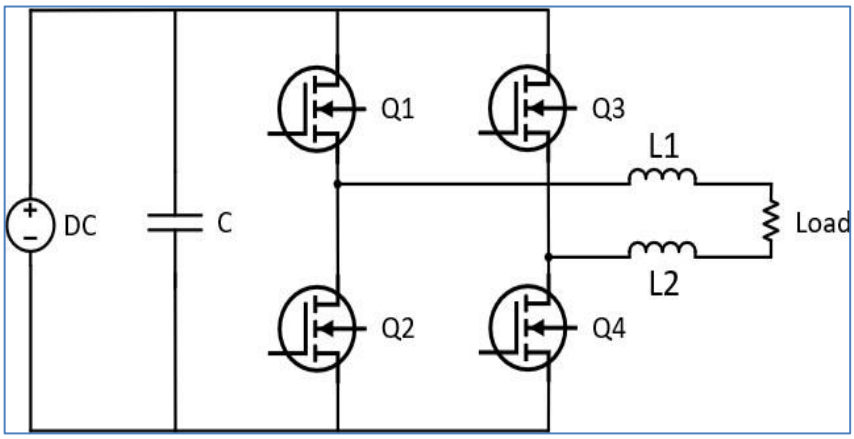


Figure 2.1: Two Bit Converter

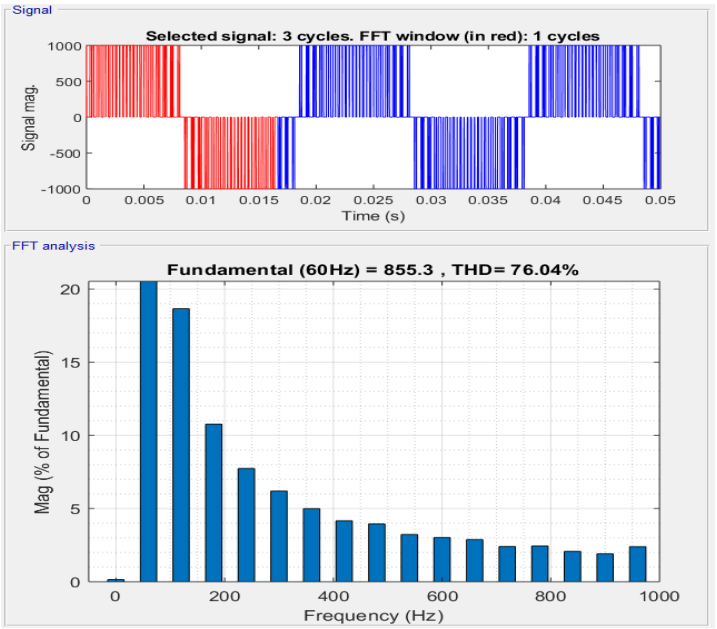


Figure 2.2: Two Bit Inverter Voltage Harmonics

2.2.2 Three Bit Inverters

In a multi-bit inverter, we create in excess of two control units which exhibits practically unadulterated sinusoidal yield voltage. Which has low dv/dt, low symphonious twists. In light of different power units s in the yield, the waveform moves toward becoming smoother however with expanding levels, the circuit turns out to be progressively intricate because of the expansion of the valves. Furthermore, an entangled control circuit is additionally required. For the getting reason, the circuit graph of a three bit inverter appears as follows. This plan looks like to the no good

inverter having just two extra switches and diodes are utilized and called as cinching diodes (Chiwandea et al., 2018) .

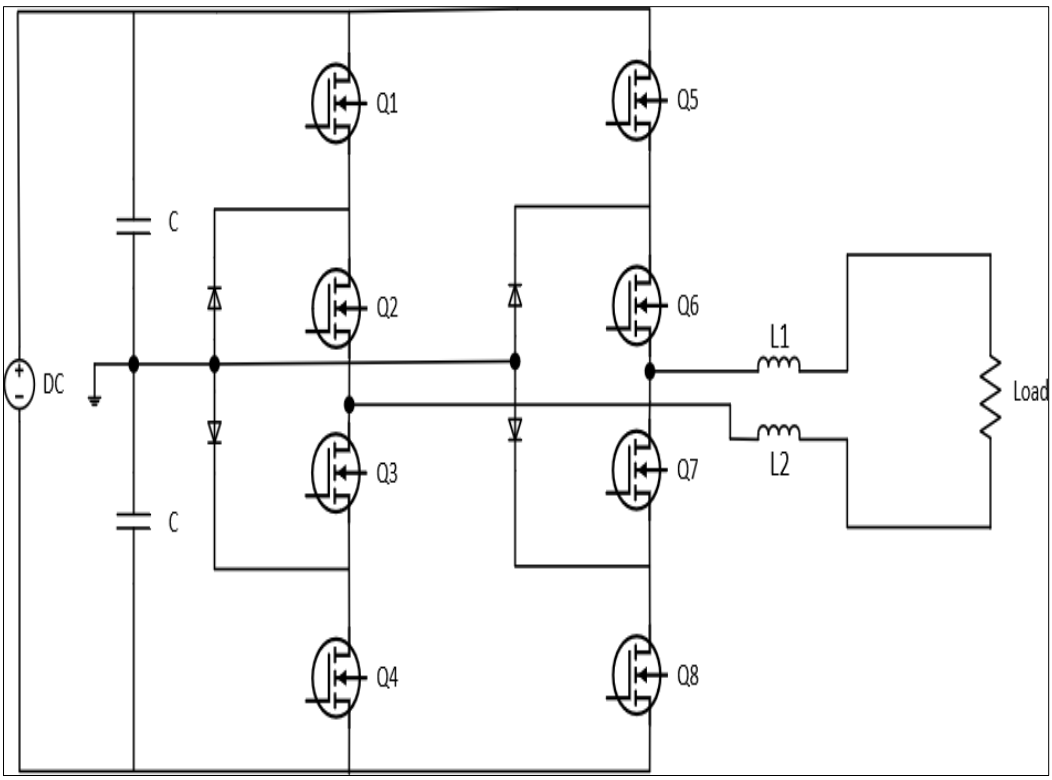


Figure 2.3: Three Bit Inverter

Switching current harmonics in a typical 3-bit inverter:

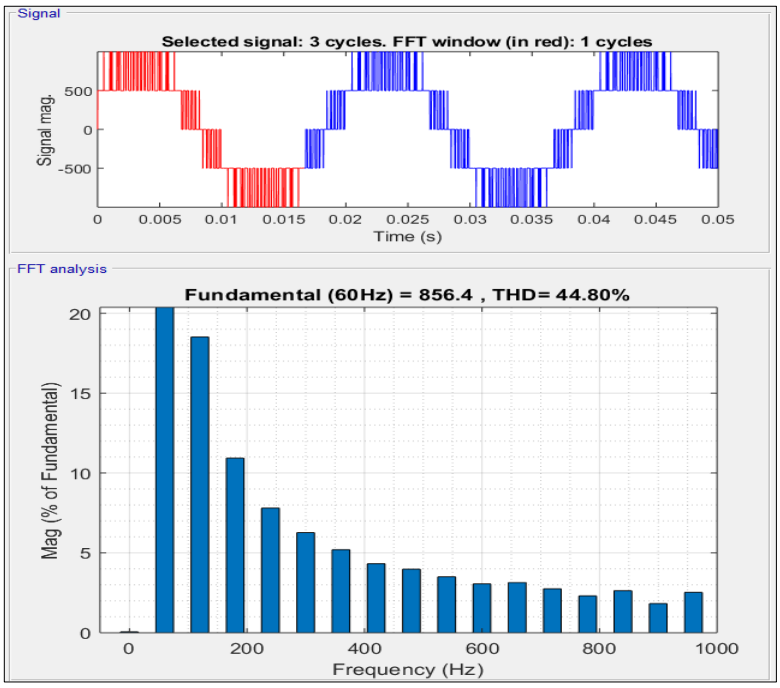


Figure 2.4: Three Bit Inverter Voltage (Arunya et al., 2013)

2.2.3 Comparison of Two Bit and Three Bit Inverters

The two-bit inverter will need high voltage semiconductor devices for high bus applications. Mixed voltage inverters, on the other hand, have better performance than the two bit inverter since they produce much better output voltage waveforms and they can operate at a lower switching frequency than two- bit inverters but magnetics need to be designed accordingly. They also can utilize low voltage semiconductor devices which are less expensive and faster in operation (Chen, 1996).

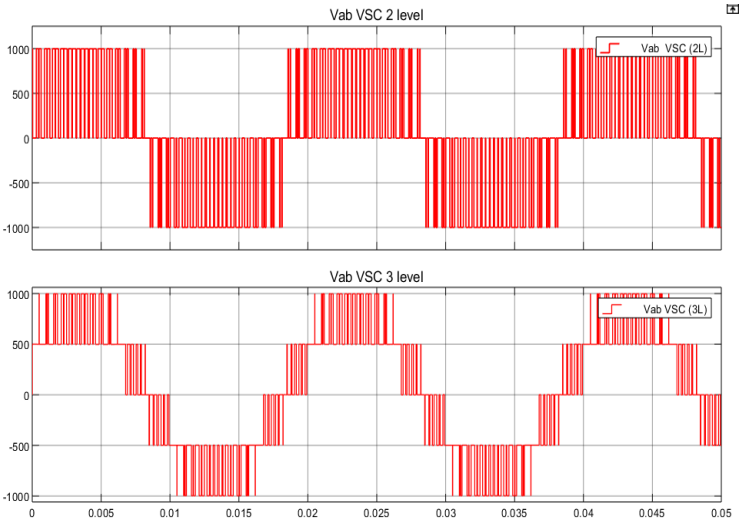


Figure 2.5: Two Bit and Three Bit Inverter Waveforms

The PMU is intended to create the voltage just when the activity is mentioned by power unit. The power is created when the yield empowers is dynamic and the information is exchanged amid empower period. Dissimilar to the other PMU that give the source consistently to the unit, the planned units ends up being a proficient power the executive devices(Aggarwal and Mehra, 2015).

CHAPTER 3

METHODOLOGY

3.1 Research Methods

The basic strategy for research for this theory was to fabricate a straightforward model of execution of PMU with PSPICE simulation. The PMU configuration is actualized in three phases, and it's a single supply with multiple output:

(i) Three bit inverter.

(ii) Two bit inverter.

(iii) Mixed voltage buffer.

The block diagrams are revealed in Figure 3.1. The purpose of every phase is additionally clarified in brief.

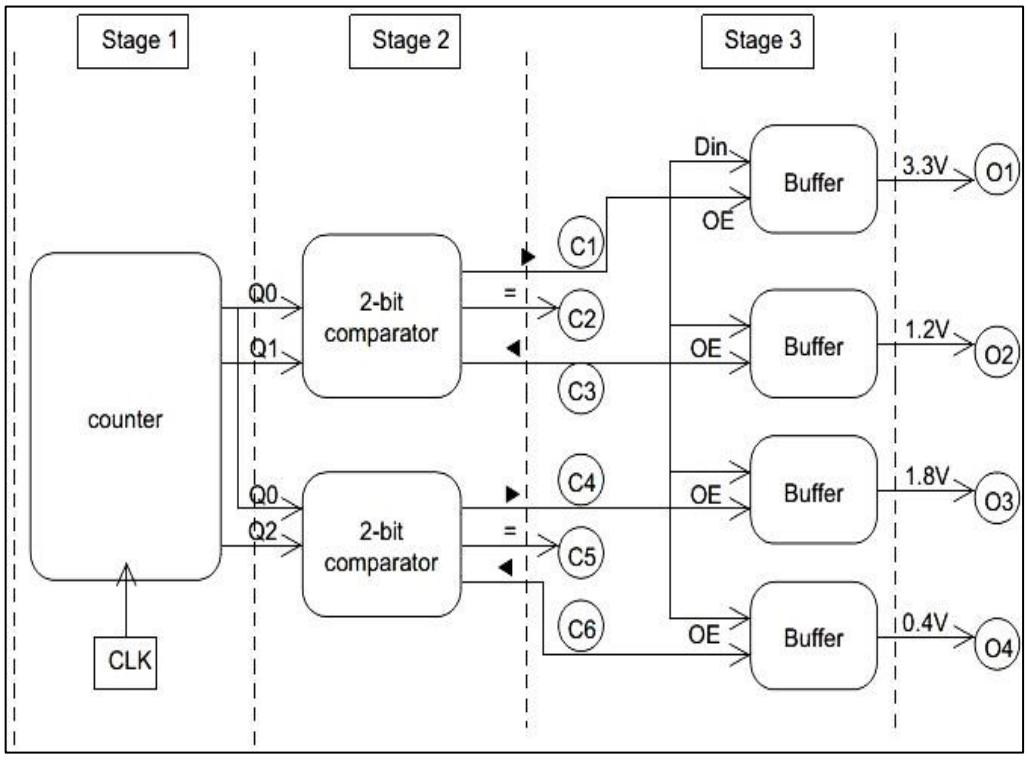


Figure 3.1: PMU Configuration

3.1.1 Three Bit Inverter

This is the principal phase of the plan. The inverter structure is executed utilizing D flip failure anywhere B is the digital contribution to inverter as appeared in Figure 3.2. The capacity of the inverter is up-tally from 0 to 7 at whatever point there is an ascent

in the digital control. The three harvests (Q0, Q1, and Q2) of the inverter are given as a contribution to the inverter arrange.

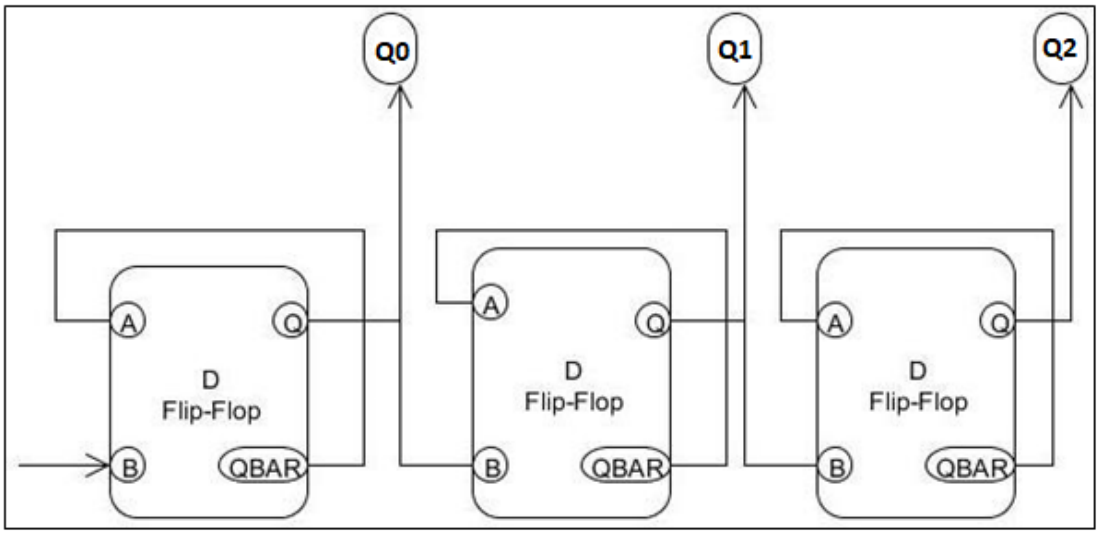


Figure 3.2: Blocks Diagram of Three Bit Inverter

Below is the truth table for the 3 bit inverter.

Table 3.1: Fact Table for the 3-bit Inverter

Present state			Next state			D flip-flop inputs		
Q2	Q1	Q0	Q2	Q1	Q0	D2	D1	D 0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	0
0	1	0	0	1	1	0	1	1
0	1	1	1	0	0	1	0	0
1	0	0	1	0	1	1	0	1
1	0	1	1	1	0	1	1	0
1	1	0	1	1	1	1	1	1
1	1	1	0	0	0	0	0	0

3.1.2 Two Bit Inverter

The inverter is structured as appeared in Figure 3.3. The inverter gets driven from the yield produced by the inverter. The motivation behind the inverter is to look at the yield of the inverter and create an empower flag to the following stage. The plan needs three inverters. The contribution of the inverter are In1 and In2 separately and produce yield is C1, and C2. Whereby C1 is created right at the moment where In1 is more prominent compared to In2.

Meanwhile C2 is produced at the time sum of the sources of info are equivalent created when In1 is under In2 blocks outline for the good for nothing inverter.

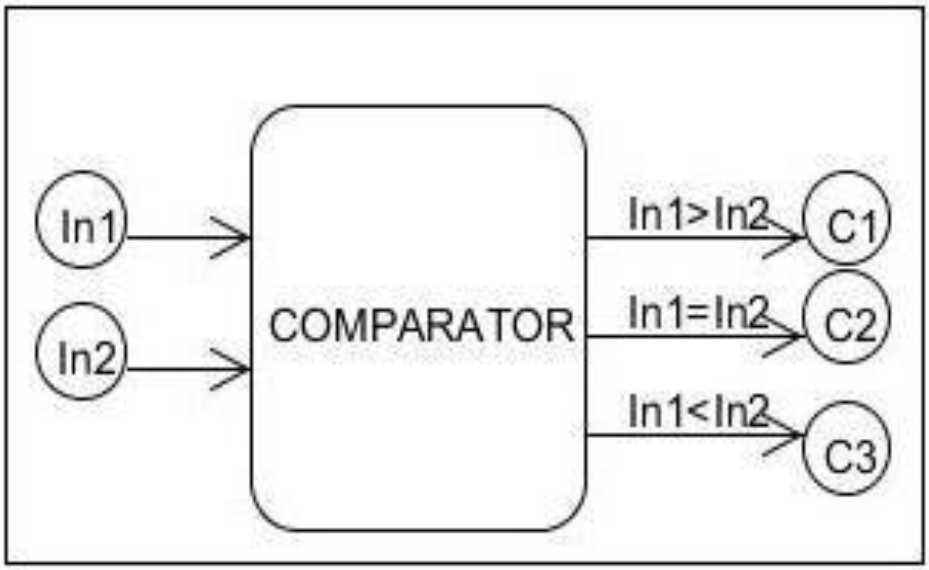


Figure 3.3: Two Bit Inverter Block Diagram

3.1.3 Mixed Voltage Buffer

The motivation behind the blended voltage support is to create distinctive power units with steady information voltage. This phase is determined by the yield of the inverter. The support has 2 data sources to empower and inverter data. The capacity of empowering the yield of the PMU and produce it just when the task is requested by the power unit is an inverter. So as to execute the PMU with four distinctive power units, it requires four blended flag cushions. Figure 3.4 demonstrates the schematic structure for a solitary stage blended voltage.

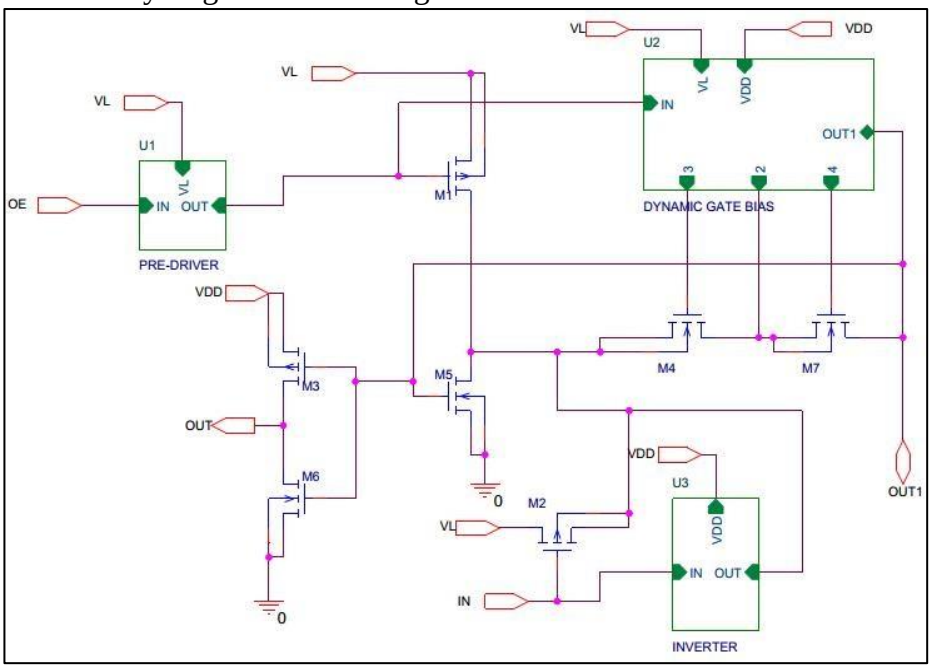


Figure 3.4: Schematic for Mixed Voltage Buffer

The planned schematic is actuality performed in OrCAD EDA tool CIS with the simulations of Pspice. The limits for both uMos and vMos are stable as below table

Table 3.2: Limits for uMOS and vMOS

Type	Vto (Edge Voltage)	Kp(Gain)	W= Width	L= Length
uMOS	1V	0.03m	2.3u	0.23u
vMOS	-1V	0.02m	6.23u	0.23u

In Figure 3.5, the CountSym blocks are the blend of inverter and inverter block. The inverter block accepts B as a digital data and produces 6 yields from 2 inverter blocks. The created yields are specified as contributions towards the voltage cushions.

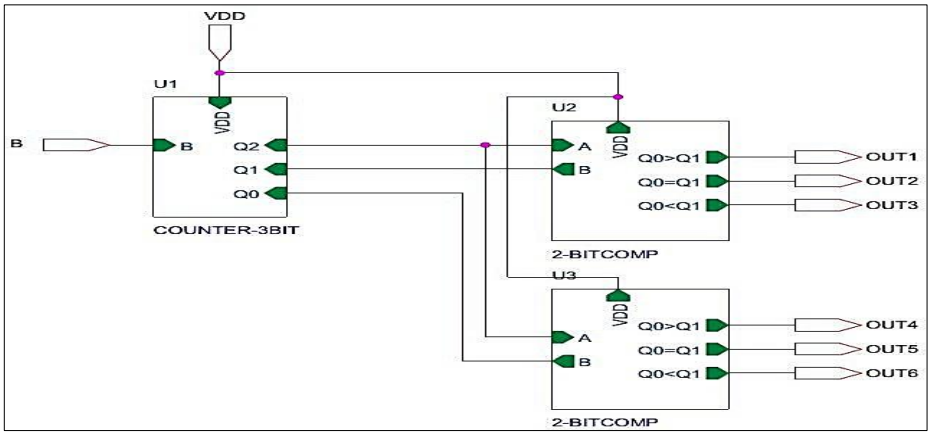


Figure 3.5: Diagram for CountSym Blocks

The supports generates yield dependent on information and empower signals. At that time yields are created at four diverse units (OT1, OT3, OT5, OT7) and their comparing rearranged supply levels (OT2, OT4, OT6, OT8) are distinctive postpone levels as appeared in Figure 3.6.

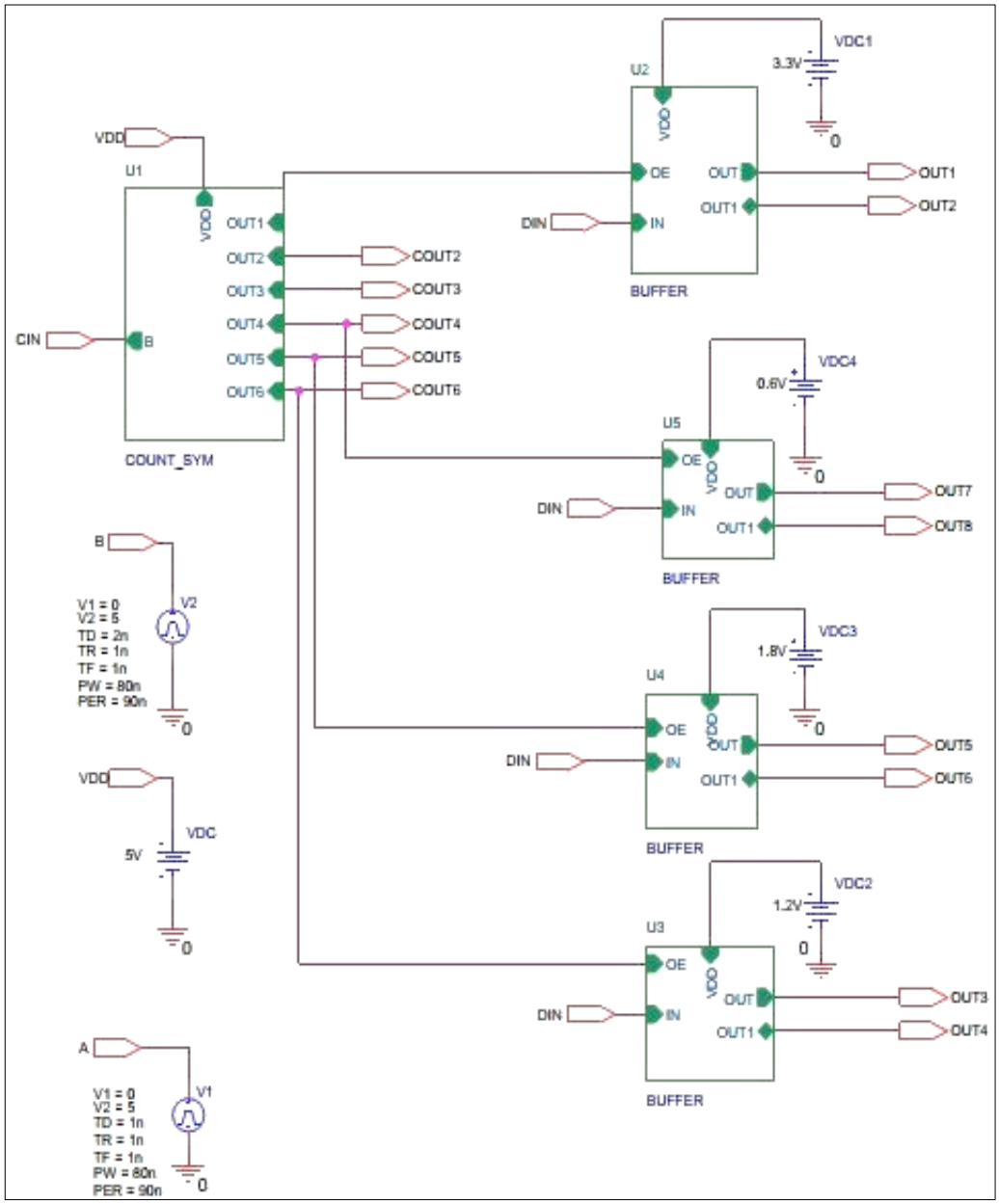


Figure 3.6: Schematic for PMU

CHAPTER 4

RESULTS AND DISCUSSIONS

4.1 Three Bit Inverter Simulation

In Figure 4.1, the digital flag is assumed as a contribution to B to start the inverter activity. The yield signs are seen at Q1, and Q2. The inverter begins its task when it gets activated the dwindling power. Q2 is the greatest substantial Bit & Q0 is minimum important Bit. A starter form of our support circuit was received with an alternate interconnect design in framework show based recreation conditions. Since the work isn't fit for performing DVFS tasks, the structure on the cushion controller interface was fairly fundamental for useful usage. In the interim, issues, for example, procedure and temperature varieties were not considered. The proposed buffering plan accomplishes versatile stream control by powerfully changing framework working conditions dependent on the quick traffic.

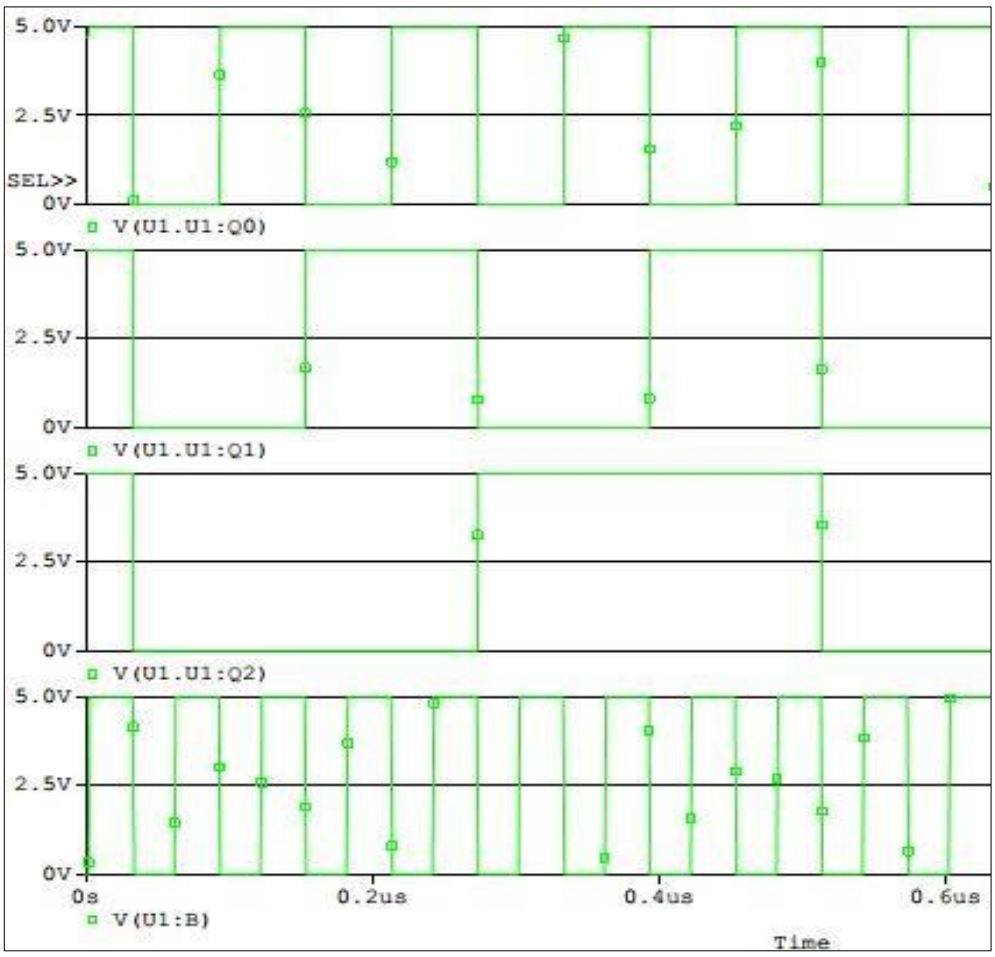


Figure 4.1: Simulated of Three Bit Inverter

4.2 Inverter Simulation

The information sources connected to the good for nothing comparison in Figure 4.2 are Q1. OUT2 empowered when Q2 equivalent and OUT3 is empowered when Q1 is more prominent than Q2.

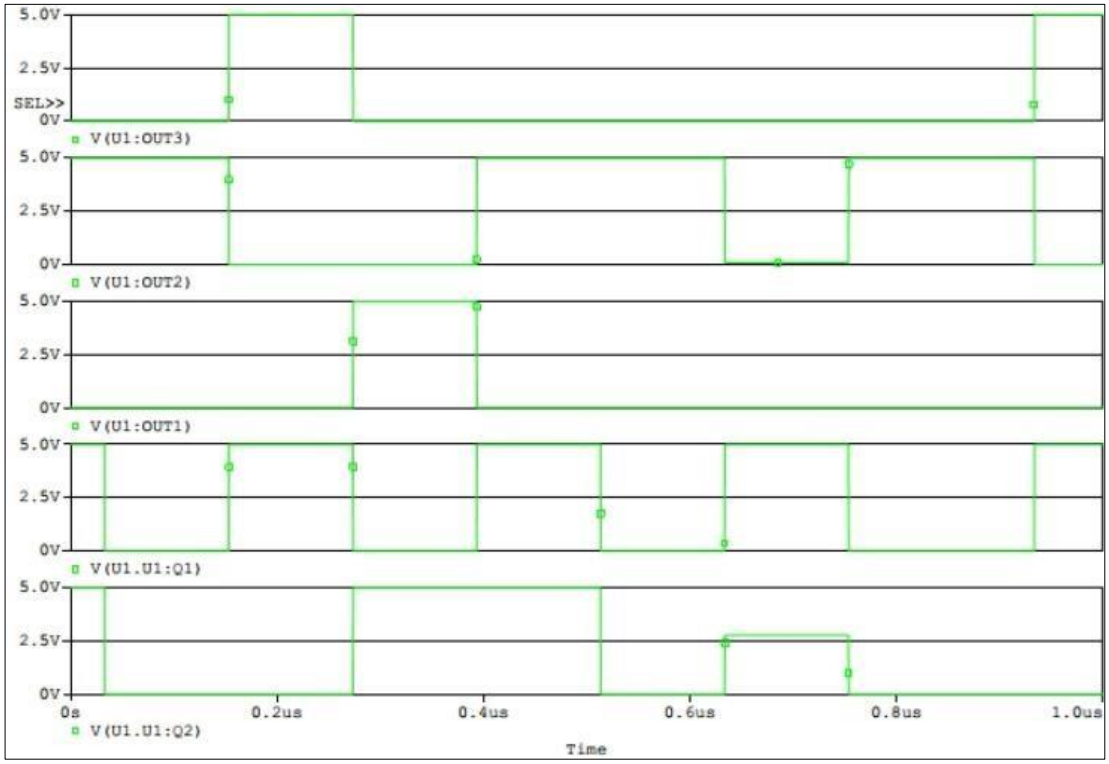


Figure 4.2: Simulated of Two Bit Inverter

4.3 Mixed Voltage Results

Mixed voltage buffer generates four different output voltage. Each output voltage simulation will be shown separately below. With single input, output of 3.3V, 1.8V, 1.2V and 0.4V are generated and the waveforms captured.

The 3.3 V source is produced from blended power as appeared in Figure 4.3. The information is linked at and empowers flag is OUT2. The yield is in Figure 4.4, A signal, OUT 9 allow signal and thus OUT4 generated 1.8V from the blocks.

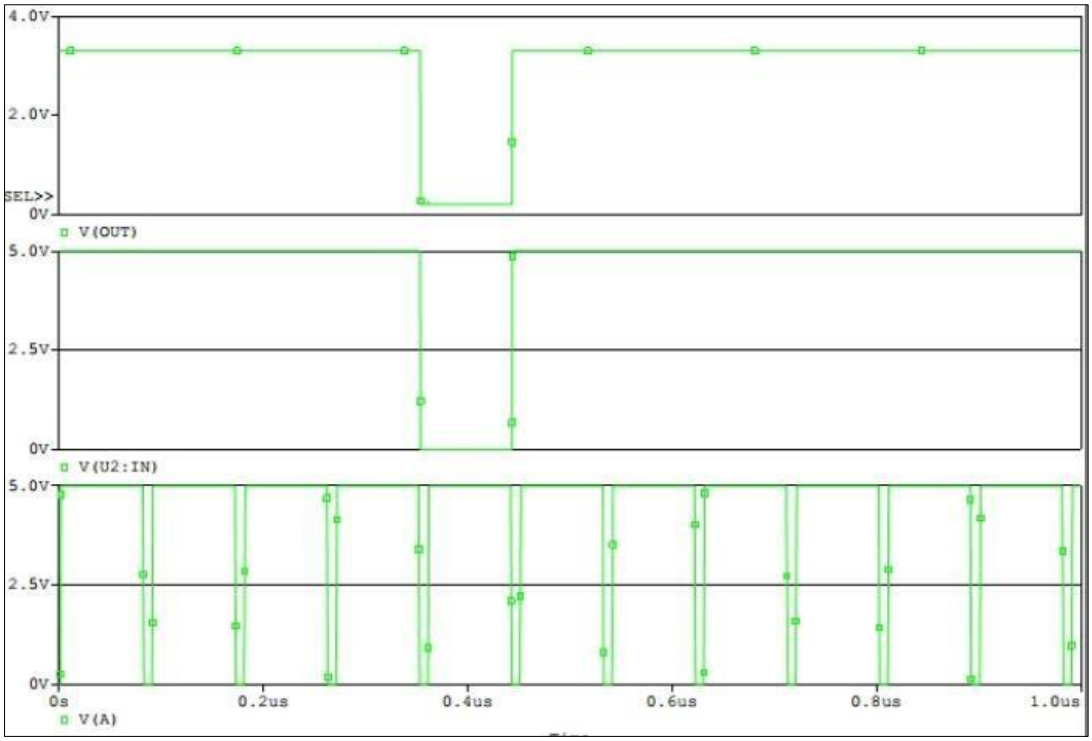


Figure 4.3: Simulated of 3.3V Mix Voltage

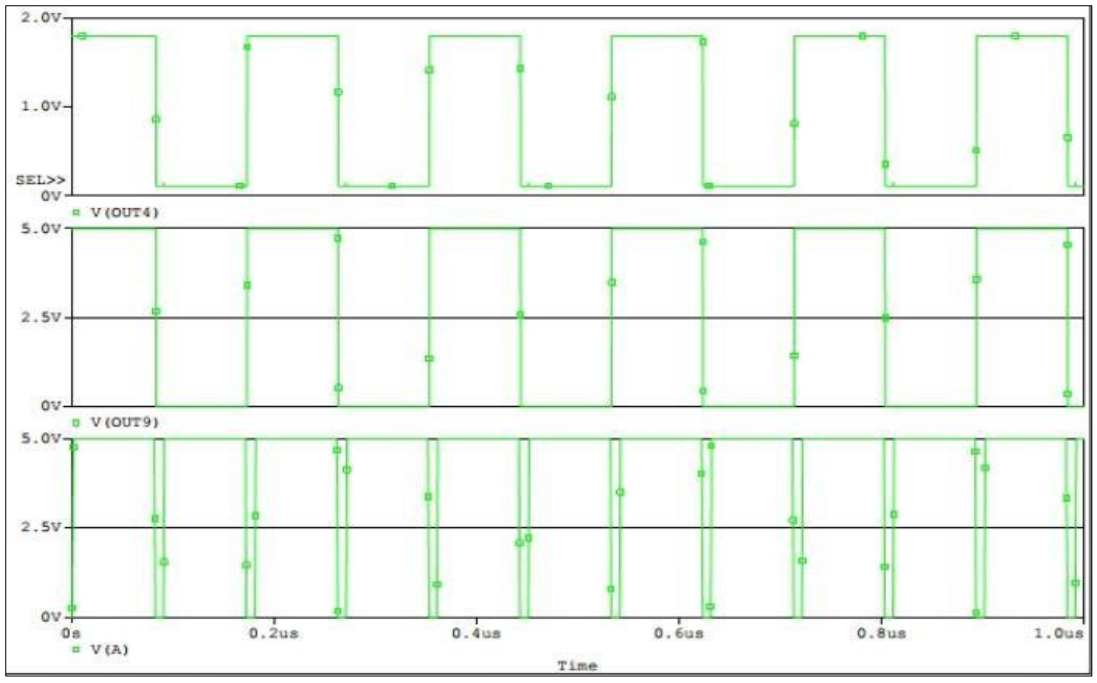


Figure 4.4: Simulation of 1.8V Mixed Voltage

In Figure 4.5, an information flag, OUT9 is the empowered flag and OUT4 is 1.2V output generated.

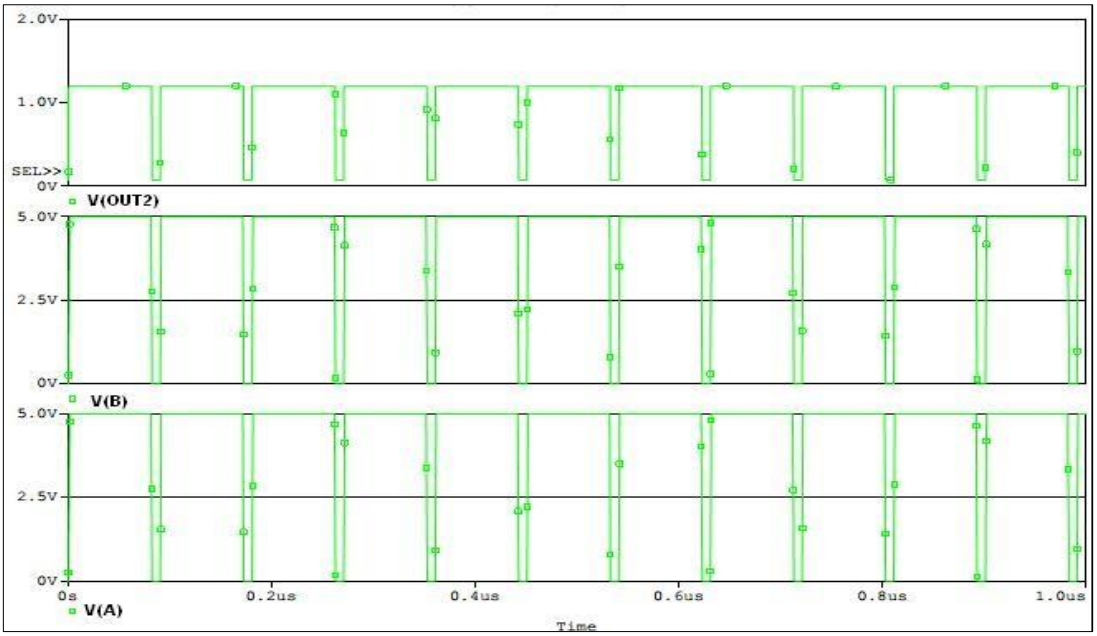


Figure 4.5: Simulation of 1.2V Mixed Voltage

In Figure 4.6, A is the information flag, B is the empower flag and OUT2 generated 0.4V.

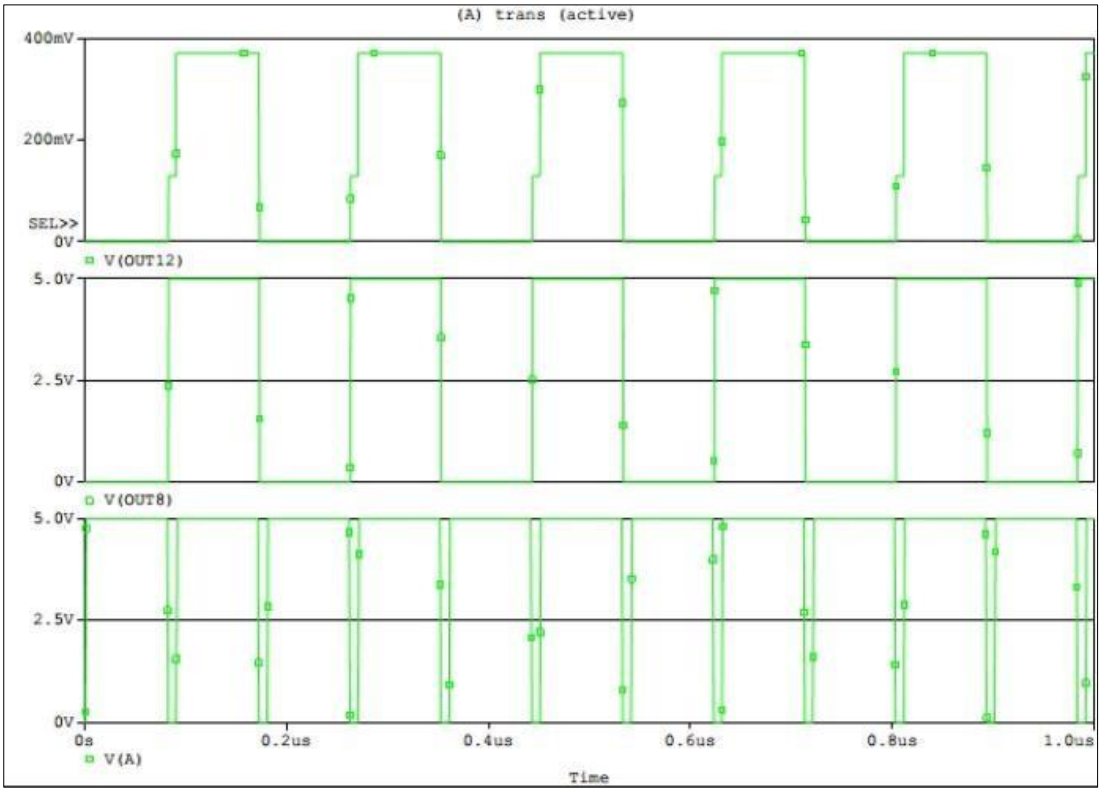


Figure 4.6: Simulation of 0.4V Mixed Voltage

4.4 Schematic Design for Each Blocks

Below shows the schematic diagram designed for each block in order to design an overall PMU that able to function with single input but generated multiple output.

4.4.1 1 Bit Inverter Application in OrCAD EDA Tool

The physical portrayal of 1-Bit inverter plan along the proposed D-Flip Flop support is appeared in Figure 4.7, which delineates a four-organize interface between two blocks. Amid blockage, the buffering plan utilizes defer control module that progressively reconfigured the repeater into tri-state supports.

In each cycle, the blockage control flag touches base at one support arrange, anticipating consequent transmission of information, which is rather the prompt phase of the structure. Data power continues just when the blockage flag is discharged, enabling the put away information to be ceaselessly transmitting to the switch. The control unit of every converter postpones the approaching clog motion by one clock cycle. This permits the buffering of information as they land at suitable moments of time.

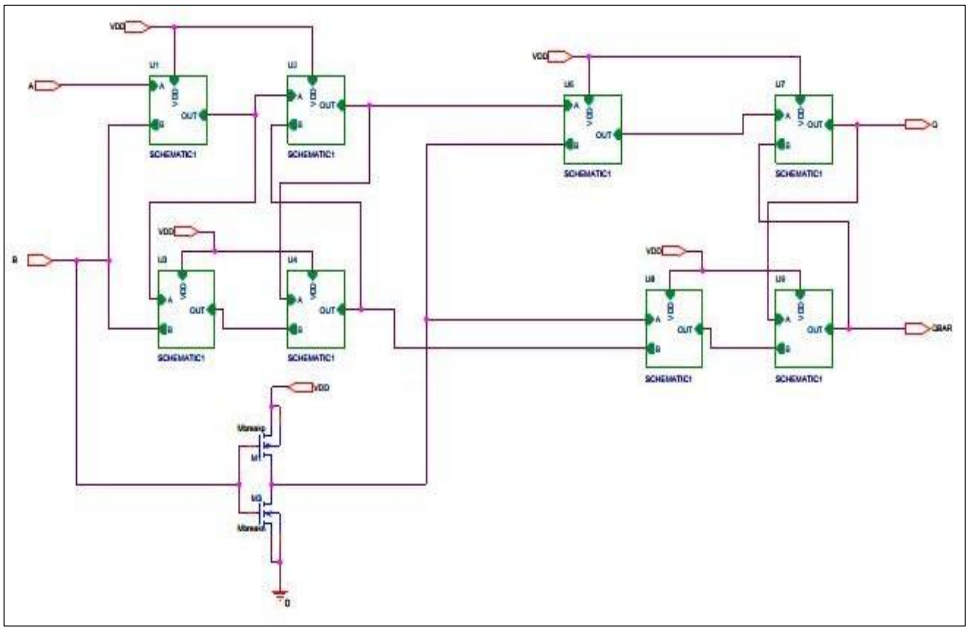


Figure 4.7: 1-Bit Inverter Design with D-Flipflop

4.4.2 Two Bit Inverter Implementation in OrCAD

The framework utilizes the consequences of control unit examination and reporting, directed at the submission layers, to give the fundamental power levels to the whole interconnect organize, with the network support. This appears in Figure 4.8, anywhere the projected 2-Bit inverter Design inverter is utilized to give voltages. The inverter additionally works intimately with the check producer contemporary in the recoverable data to give the important recurrence.

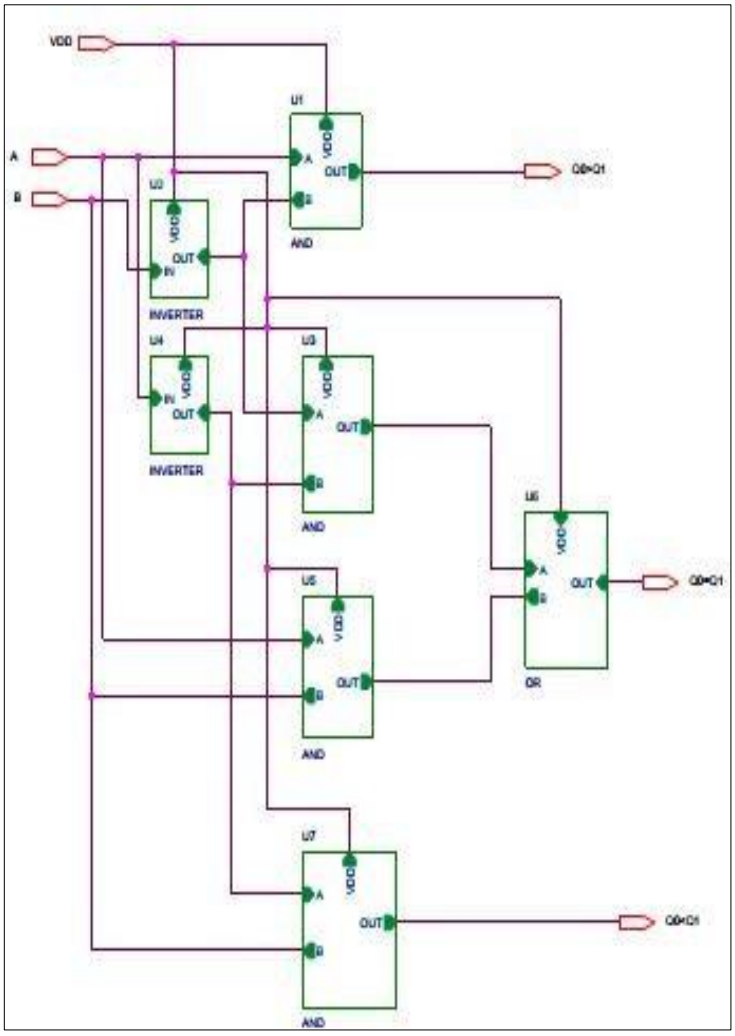


Figure 4.8: 2-Bit Inverter Design

4.4.3 Mixed Voltage Buffer

The detailed schematic design for mixed voltage buffer is as per shown in Figure 4.9. As shown, mixed voltage buffer uses a core block which is referred as dynamic gate bias. Purpose of the dynamic gate bias is depending on the activity situation, which is chosen by the framework remaining burden, organize traffic and timing for different processor centre errands. Source in the schematic is in pulse form in order to reflect that when there is no demand for supply, circuitry is in power saving mode.

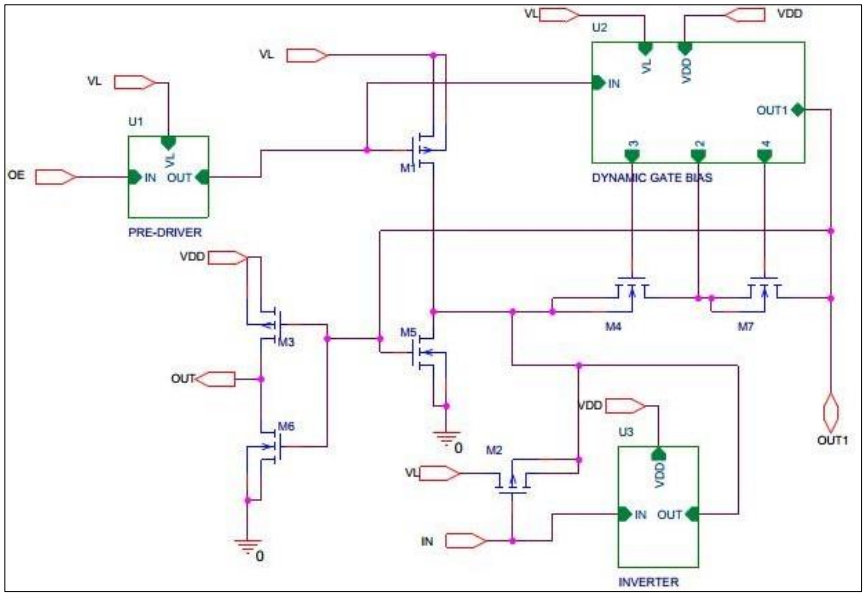


Figure 4.9: Inner Design of Mixed Voltage Buffer

Figure 4.10 shows the task of the Energetic Gateway Bias buffering plan at different modes. Amid states of the overwhelming remaining task at hand/traffic, the interconnect capacities at the working focus. So also, amid light traffic conditions. The Energetic Gateway Bias of the multicore design can likewise complete the accessibility of the power converter, to possibly work both the network buffering plan and different interconnect segments, in different modes.

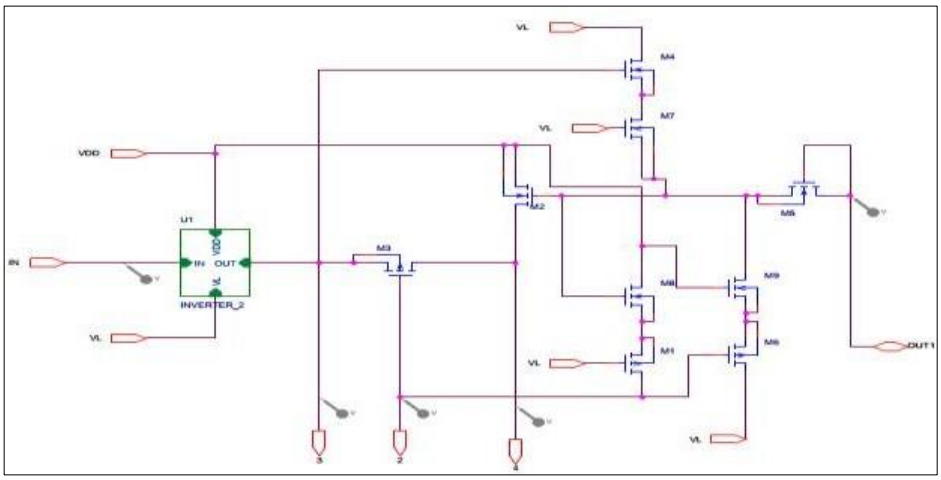


Figure 4.10: Schematic of Energetic Gateway Bias

The load resistance correlation with the generated output was not covered in this project scope but it will be one of the recommendation for any further studies or research done in the PMU. Theoretically load resistance will influence the output voltage and this can be also used to control the output value.

CHAPTER 5

CONCLUSIONS AND RECOMMENDATIONS

5.1 Conclusions

This study suggests a system to build the PMU that grasps the capacity of creating 4 individual blocks of power control units. This has been demonstrated with the reenacted outcomes created utilizing PSpice test system in OrCAD instrument. To dynamically respond to the power demands and to accurately control the power delivery to the mainframe cores. The yield is created just when there is an activity required from the blocks. The power management unit successfully able to generate four diverse voltage level from a continual input voltage. In additional the design is such where the PMU indirectly performing under power saving mode as it only functions when there is request for voltage supply.

5.2 Recommendations for future work

Power preparing and power management can possibly reclassify framework setup and configuration approaches, as it gives a more noteworthy level of plan adaptability. Subsequently, as they are basic for cutting edge multicore frameworks, the exploration work depicted in this thesis proposes a few power management strategies that attention on the joining of equipment programming co-plan systems, to interpret neighbourhood and constant power data onto the power management stage.

It has been demonstrated that power management techniques can also be employed to perform thermal monitoring and thermal management of modern IC systems. This is particularly basic for figuring frameworks, for example, multicore processors that can encounter sporadic events of warm hotspots, contingent upon the operational outstanding burden and can regularly prompt hopeless IC damage. Thus, the merging of effective thermal and power management techniques are also required to ensure that the multicore system always functions within the safe and reliable regions of operation. Hence, the development of a universal system that can minimize total power consumption and heat generation, while being implemented on a single common hardware platform, can revolutionize the design of future multicore and other computing systems.

A research challenge for power management systems for multicore processors is a result of the advancements in IC fabrication technology. As technologies continue to downscale transistor dimensions aggressively, due to reduced breakdown voltages and transistor failure mechanisms, the rated supply voltage has reduced. However, multicore architectures consist of a plethora of sub-systems, including analog circuit block such as voltage regulators, temperature sensors, amplifiers, and so on, which still operate at voltages that are higher than the breakdown voltage of the low-voltage digital process. Hence, the capability to provide large voltages is still essential in advanced semiconductor processes. However, as the converters that provide these supply voltages are required to operate at control units several times higher than transistor breakdown voltages, considerable design stress is placed on achieving reliable switching. Thus, future research into the development of robust power management circuit architectures that can safely supply large supply voltages, while still using advanced semiconductor processes, is highly essential. In addition to that, the correlation of the load resistance and PMU output can be further studied on to understand further what is the best or threshold value for the load resistance for a robust PMU.

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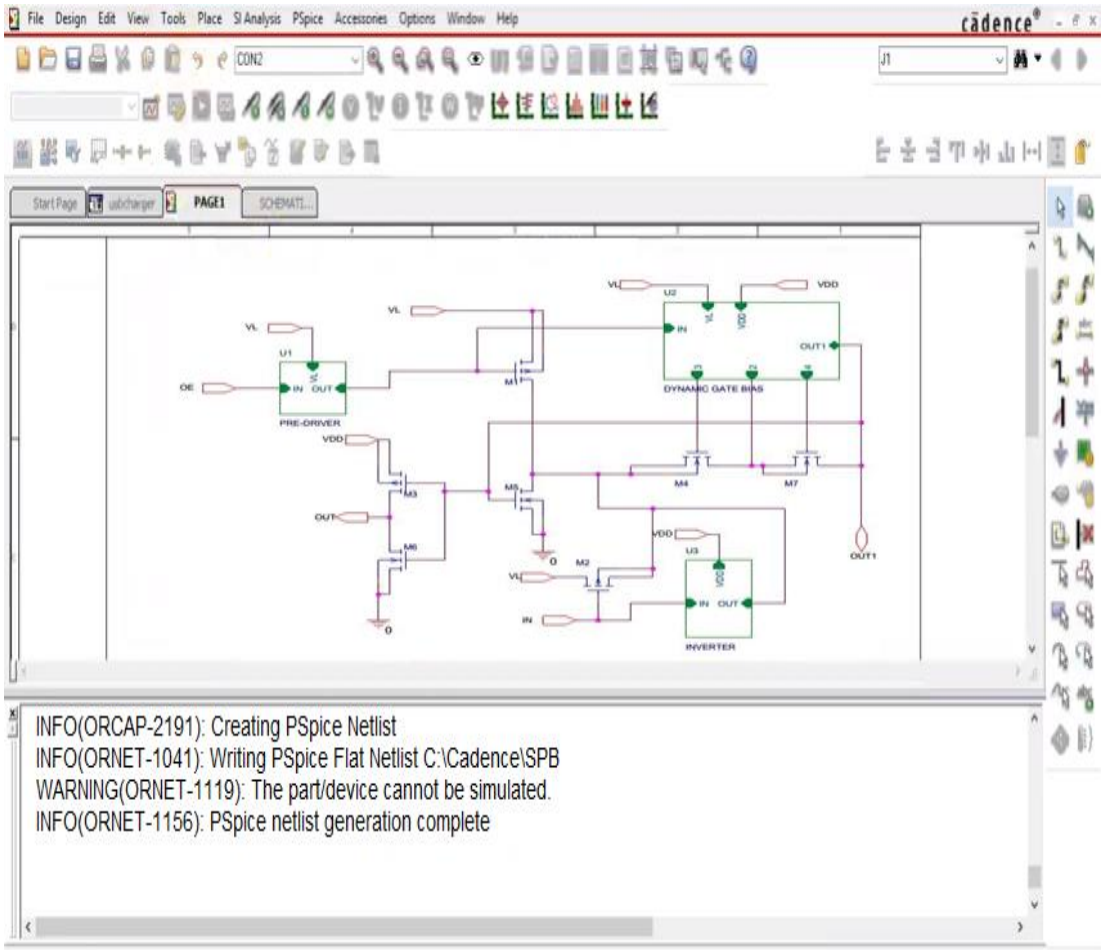
APPENDICES

APPENDIX A: Simulations



APPENDIX B: List of Errors