IMPROVEMENT OF POWERMITE PACKAGE CRACK AND CHIP DIE PROCESS OPTIMIZATION STUDY IN DIE ATTACH AND MOLDING PROCESS

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A project report submitted in partial fulfilment of the
requirements for the award of Master of Engineering (Electronic Systems)

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DECLARATION

I hereby declare that this project report is based on my original work except for citations and quotations which have been duly acknowledged. I also declare that it has not been previously and concurrently submitted for any other degree or award at UTAR or other institutions.

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APPROVAL FOR SUBMISSION

I certify that this project report entitled **"IMPROVEMENT OF POWERMITE PACKAGE CRACK AND CHIP DIE PROCESS OPTIMIZATION STUDY IN DIE ATTACH AND MOLDING PROCESS"** was prepared by **NUR AFIQQA BINTI RASHID** has met the required standard for submission in partial fulfilment of the requirements for the award of Master of Electronics at Universiti Tunku Abdul Rahman.

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Date : _____

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ABSTRACT

Powermite is a surface mount package with a low profile package technology, space saving and higher power dissipation surface mount diode. Since the package was introduced in the past few years, multiple occurrence of crack die reported which are severely impacting automotive customers quality and causing customer returns.

Vertical crack pattern contributes to 70% of the crack die which is the highest crack type compared to lateral crack and diagonal crack. The assembly high stress processes during die attach causing the initiation crack point propagates to reach die active area. The six sigma tools identified the root cause originates from die attach parameters not optimized. Design of Experiment (DOE) was performed to verify the hypothesis by assessing five die attach parameters and the parameters that are significantly causing crack die are then analysed to obtain the optimized die attach parameters.

The DOE concludes four out of five main parameters which are collet type, pick force, bond force and ejector needle settings significantly contribute to die crack issue. The association factor analysis concludes that the uses of rubber collet, lower bond force, pick force and ejector needle are the factors required to minimize crack die in die attach process. Future work for this project is to replicate this experiment through Taguchi method to find the best optimized parameter for die attach.

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LIST OF SYMBOLS / ABBREVIATIONS

IC	Integrated Circuit
Cu	Copper
DMAIC	Define, Measure, Analyze, Improve, Control
SIPOC	Supplier Input Process Output Customer
CTE	Co-efficient of thermal expansion
SEM	Scanning Electron Microscopy
BLT	Bond Line Thickness
ANOVA	Analysis of Variance
Pb	Lead
RBFA	Reject Bin Failure Analysis
TIM	Thermal interface materials
MSE	Mean Square Error
SSE	Sum Square error
SST	Sum square total

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CHAPTER 1

INTRODUCTION

1.1 Introduction

Integrated circuit chip (IC) technology was used in everyday life all the way from computers, cars, communication devices, industrial and electronics application. High demand for lower cost, smaller, faster, high power and good reliability of devices are the challenges which drive the competitive semiconductor industry to grow rapidly from the 1940's when contact point transistor was first invented by American physicists John Bardeen, Walter Brattain and William Shockley.

The basic operations involved in semiconductor manufacturing are divided into two which are front end and back end process. Front End process comprises of Crystal Production and Wafer Preparation, Masking Process and Wafer Fabrication whilst Back End process comprises of Packaging and Testing (Hitachi High-Technologies Corporation, 2019).

For the device to work reliably over time, it is important to protect the chip from internal and also external stress to the chip through packaging. Packaging refers to materials that encapsulate the circuit to protect the die from corrosion and mechanical damage and also to allow for electrical interconnection to the Printed Circuit Board. There are many types of IC packaging in the market. The design of the packaging is depending on the function, size, dimension, cost, electrical, mechanical, thermal properties and user friendliness of the end products and also their competitiveness in the market (Lee, Y.C. and Chen, W.T., 1998).As the packages become smaller and simpler, the complexity of the packages increases. New process was discovered to meet the market demand (Dexin Z., et. al., 2006).

Clip Bond is one of the packaging technologies for power devices that are acknowledged to have the least package resistance compared wire bonding and ribbon bonding (Kengen M., et al., 2009). Some high power packages and discrete devices for example, Insulated Gate Bipolar Transistors (IGBTs), Metal Oxide

Semiconductor Field Effect Transistor (MOSFETs) are using solder paste as direct materials to form Intermetallic Layer (IMC) to electrically connect the die, clip and lead frame. Some of the advantages are lower package resistance, good thermal transfer and fast switching performance due to small package dimension.

Crack die will affect the semiconductor device greatly and in some applications. The device failure can cause life threatening situation to the user like that application in aerospace. Although the devices was tested prior shipped to customer, the partially crack die might not necessarily fail immediately as the failure is still within passing margin. However, the partially defected device is facing serious reliability issue and eventually failed after continuous thermal stress and cause casualties to the user.

1.2 Crack die challenges

One of the challenges in semiconductor assembly packaging is to manage the thermal and mechanical stress to the die. There are many factors that could bring thermal and mechanical stress to the die that may cause the device failure. (Wang, K. P., et al., 2000). Studies have shown that crack die is caused by die attach parameters not optimized, silicon wafer incoming defect, solder void issue, Co-efficient of thermal expansion mismatch, mechanical stress, insufficient solder thickness and package stress.

1.2.1 Crack die due to die attach parameter not optimized

One of the cause of crack die is due to die attach parameter not optimized (Tan, Y. H. and Liau, W. S. 2018). The study explored on the type of machine, mechanical parts, die strength and the co-relationship between the impact force and crack die. It also suggested that surface defects such as micro crack that had existing in previous process, such as back grinding and wafer thinning have weaken the die and makes the die more susceptible to cracking in the subsequent process.

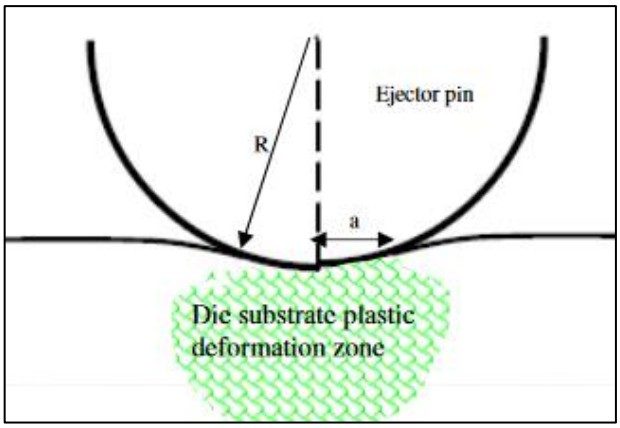


Figure 1.1: Ejector pin contact to surface of substrate (Fisher-Cripps, 2009 cited in Annaniah, L., 2016)

The crack formation is due to stress acting on the atomic bond exceeds the inter-atomic bond strength as illustrated in Figure 1.1 (Claeys, C. et al., 2011).

1.2.2 Crack die due to Silicon wafer crystal defect

A study had shown that crack die was happening only at specific die technology with a (100) crystallographic orientation plane. This concludes that the bond force and crystallographic orientation interaction is the contributing factor to crack die. (Annaniah, L. and Devarajan, M., 2016).

Crack die also might be caused by crystal defect in the wafer during wafer fabrication process. The two most commonly used technique for crystal growth are Czochralski or the crucible type method. Most common defect in the crystal growth are dislocation and swirls that may lead to reduction in the density of crystal growth. To reduce the crack die due to wafer fabrication issues, reduction of back side defects during wafer thinning and reduction in dicing defect during sawing (Ranjan, M., Gopalakrishnan, L., Srihari K., and Woychik, C., 1998)

1.2.3 Crack die due to solder void issue

Solder void degrades the performance of die by reducing the solder contact area. In addition, single big void also can cause high crack die possibility from subsequent

process at wire bond and mold (Yeo, S. M., Mahmood A. and Yazid, N. A. M., 2018).

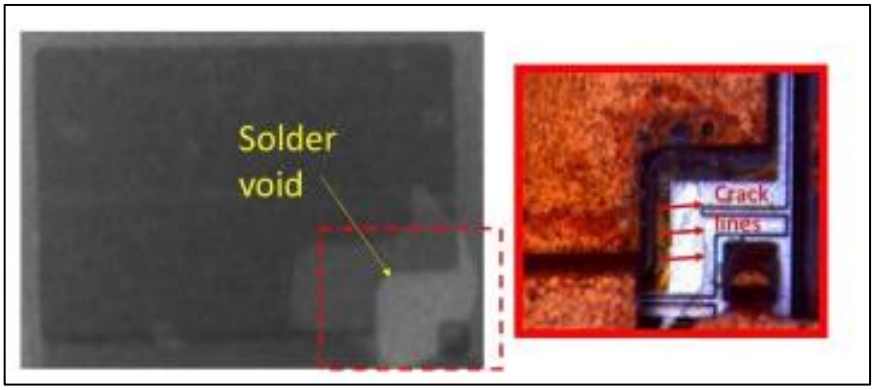


Figure 1.2: Crack die caused by mold compression with presence of solder void (Yeo, S. M., Mahmood A. and Yazid, N. A. M., 2018)

Void formation inside the solder joint influence the thermal resistance of devices. More solder voids increases the crack growth rate significantly (Hanss A., Liu, E., Schmid, M. and Elger, G., 2015).

1.2.4 Crack die due to Co-efficient of Thermal Expansion (CTE) mismatch

There are multiple researches that had proven CTE mismatch is one of the key factor of device performance. During designing stage, all factors must be taken into consideration such as material, package design, electrical performance, reliability and expected life span of a device. CTE mismatch will bring serious reliability issue when continuously being subjected to thermal loading and mechanical stress at consumer side.

A study conducted showed by reducing the mismatch of the CTE between multiple components of flip chip assembly, crack die could be reduced due to decrease of warpage of the package (Ranjan, M., Gopalakrishnan, L., Srihari K., and Woychik, C., 1998). Another CTE related study to crack die had proven that devices subject under 1000 cycles are prone to crack and chip. Modelling has verified that

the level of tensile stress is crucial to long life reliability compared to compressive stress (Pavio, J. and Hyde, D., 1991). A similar crack mechanism in Pb Free Flip Chip packaging from die bottom suggested that crack die occurs due to bending stress at the die backside from CTE mismatch of the Silicon die and the underfil fillet (Chen, K. M., 2009).

1.2.5 Crack die due to mechanical stress

Several studies had proven that mechanical stress can cause physical damage to the die. A study using external load is applied to the top of the packages and the damage at the Silicon layer was observed using ultrasonic scan and cross section (Su P., Khan B., and Ding M., 2010).

1.2.6 Crack die due to insufficient solder thickness

Solder thickness is crucial to cushioning of the stress subjected to the die during assembly processing. After solder reflow process, the dies was continuously subjected to many thermal and mechanical stress at the preceding assembly process. High lead solder was preferable in high-current-density discrete power packages due to its many advantages such as having low resistance, high thermal conductivity, ductility to accommodate thermal expansion mismatches between joining material and its high melting point to accommodate multiple reflow cycles in the subsequent process.

However, IMC interface Ag_3Sn layer spalling with discrete structure embedded in the Cu_3Sn IMC is undesirable. It may weaken the interface structure and make the joint harder and more brittle. The CTE mismatch and the stress from the mismatch strain lead to the crack of the Silicon. The study concludes that thinner BLT with larger IMC grain size at solder joint contributes to facilitate the crack growth at Si die and solder joint. The hardened solder also did not absorb the strain caused by CTE mismatch which later leads to crack die (Chiong, K., Zhang H., and Lim, S. P., 2016). Figure 2.4 shows the vertical crack initiated from bottom and propagate to die top through compression stress after cooling.

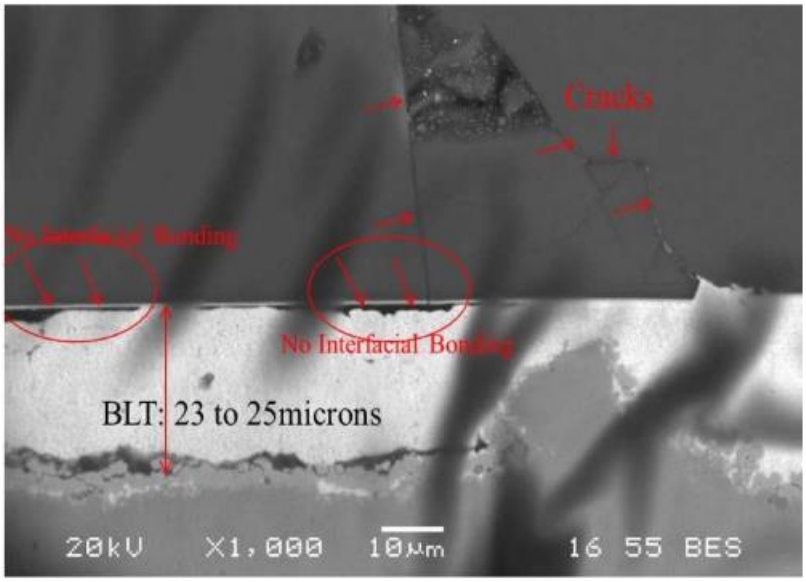


Figure 1.3: Vertical crack die at the no interfacial bonding area (Chiong, K., Zhang H., and Lim, S. P., 2016).

1.2.7 Crack die due to package stress

Finished products are also having the internal stress. A study had proven that the package design itself may cause crack die during molding process. The study compares several different packages with varied mask openings and die sizes were tested and the quantity of crack die was recorded. The outcome of the study shows that smaller die size has lesser stress compared with bigger die sizes (Vijayakumar, B. and Guo, Y., 2006).

1.2.8 Failure Analysis on Powermite package customer return unit

The customer return units shows solder seepage in between the crack line from die backside. This indicated that the crack had occur during die attach process when the solder is still in liquid form before solder reflow process as shown in Figure 1.4.

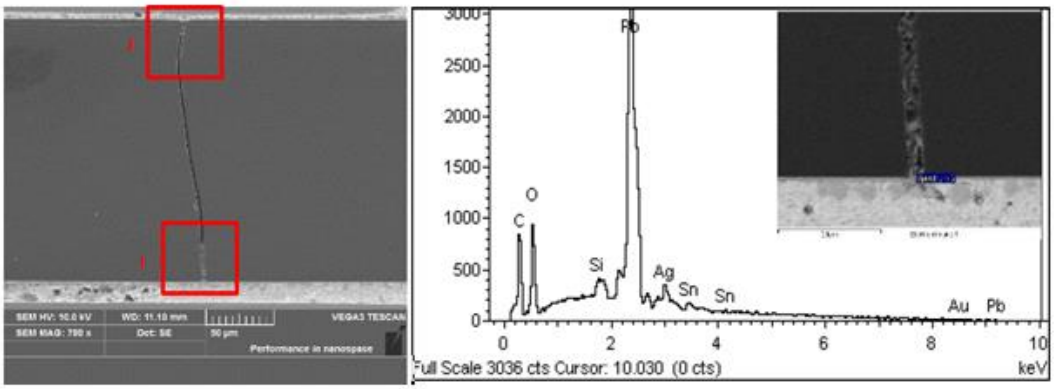


Figure 1.4: Solder seepage in between crack line.

1.3 Importance of the Study

Crack die has been the focus field of improvement since the introduction of semiconductor devices. For this package, the study will encompass three types of crack and chip which are lateral crack, vertical crack and chip die. This study can pose as a reference to another crack die study.

1.4 Problem Statement

All the surface mount package customer return is reported to have failed at board level. No external abnormalities can be observed on the Powermite package from field return device. However, after failure analysis conducted on the return units, found the die cracked into half. Those units having marginal crack at active area passes the final test electrical requirements.

In response to this problem, this study proposes to investigate the root causes through six sigma tools. One of six sigma tools which is Design of Experiment is used to study the significance of die attach parameters that contribute to crack die.

1.5 Aims and Objectives

This project aims to improve the surface mount package crack and chip die through process optimization study by using DOE approach in die attach parameters. The DOE was performed to verify the hypothesis by assessing five die attach parameters to identify parameters that are significantly causing crack die to obtain the optimized die attach parameters.

1.6 Scope and Limitation of the Study

The assembly process to analyse is at die attach process. For die attach machine, only Alphasem E3008 model will be used for study purpose. The studied parameter are die attach parameters - collet type, ejector needle height, bond force, pick force and separation time. Molding parameters are excluded from the study as they are not the contributing factors after investigation through failure analysis on the customer return units by Finite Element Analysis (FEA) and six sigma analysis.

1.7 Contribution of the Study

The findings of this study will serve as the reference document to other assembly process that are also facing crack dies issue. This would enable achieving zero defect products as expected by end user customer. The finding of this study also would serve the reference for future researcher who would work on optimization of die attach process.

1.8 Outline of the Report

This report contains 5 chapters. Chapter 1 contains the introduction, the importance of study, aims and objectives, scope and limitations of the study and also the contribution of the study.

Chapter 2 will contain the literature review on this research. It contains the tools of lean six sigma introduction, explanation of thermal transfer through solder

void of semiconductor packages and design of experiment's Analysis of Variance for five factors and two levels mathematical equation.

Chapter 3 will focuses on methodology and work plan on conducting the two levels five factors DOE for the die attach parameters which are identified by six sigma model analysis. The chapter also specific the plan of how the design of experiment is carried.

Chapter 4 presents the result, analysis and discussion of the outcomes of the experiments.

Lastly, Chapter 5 will summarise the conclusion and future recommendation.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

The literature review in this chapter will cover three subtopics which are six sigma method, thermal transfer through solder void in semiconductor packages and Design of Experiment. Six sigma methods explained about some of the tools incorporated in lean six sigma as root cause and problem solving tools. Improper heat transfer through solder void present causing high thermal resistance in semiconductor packages was visualized and studied in this chapter. Lastly, the Design of Experiment section will lists all the formula related to be used for Analysis of Variation.

2.2 Six Sigma Method

The continuous struggle by manufacturers wields tightly fixed process parameters as means to gain high yield. There are multiple methods introduced to bring improvement to the manufacturing process itself such as lean six sigma method. Six sigma was introduced by Motorola engineer Bill Smith in 1980's (Kaizen Consulting Group, 2019). Six sigma as applied by Motorola, is a drastic extension of the old idea of statistical control of a manufacturing process. Six sigma philosophy uses data and statistical tools to systematically improve process and sustain process improvements (Thomas P., 2019).

Six sigma methodologies comprises of five phases which are Define, Measure, Analyse, Improve, and Control (DMAIC). The Define phase contains the problem statement, Supplier Input Process Output Customer (SIPOC) mapping and Gantt chart of the project. Measure phase is to thoroughly understand the current state of the process and collect reliable data that will be used to expose the underlying causes of problem. All of the key processes input and output variables to be identified at the measure phase. Analyse phase is to pinpoint and verify causes affecting the key input and output variables tied to the project goals. The lists of

potential causes through usage of top down chart, Is and Is Not mapping, fishbone diagram was narrowed. Statistical analysis through the Design of Analysis was used to validate the significant factor and confirm the root cause (Michael L. G., et al., 2005)

2.3 Thermal transfer through solder void of semiconductor packages

Power package module was designed to withstand high thermal stress and electrical stress. Solder acts as interconnecting materials between clip and die and die to leadframe. Solder void, which may occur due to trapped gas during reflow, micro crack die, poor wettability at the joining interfaces will cause undesirable effect to the device functionality (Tran, Son, Dupont, Laurent and Khatir, Z., 2014).

The thermal resistance between packages with solder void and packages without solder void is different. Based on study conducted, the thermal resistance in package with large solder void is higher compared to packages with less solder void. Figure 2.2 shows a FEA simulation of heat transfer between Silicon/ Thermal Interface Materials and Thermal Interface Materials to copper. Example of thermal interface material is solder paste.

Solder interface materials (STIMs) are used to reduce the thermal resistance from the chip to the heat sink. However, voids formation in STIMs impedes heat transfer and results in increase in chip temperature. The package with larger solder voids results in higher thermal stress and will gradually formed a hot spot which later will contribute to the failure of a device. The excess heat melts the materials, warps and breaks the structure of semiconductor dies (Lakshminarayanan V., 1999).

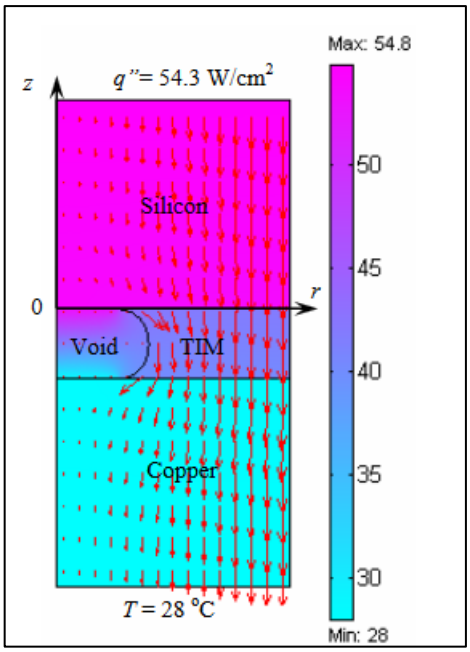


Figure 2.1: Simulated temperature distribution (colour) and arrows using FEA in cylindrical coordinates with a contact resistance of $1010^{-5}\ km^2/W$ at Silicon/TIM and TIM/copper interfaces (Xuejiao H., Linan J., Kenneth E.G., 2004).

A study on void percentage that contributes to thermal resistance has been successfully modelled by a research. The research has concluded that thermal resistance increases as the solder void increases in Figure 2.3 (Otiaba et al., 2011).

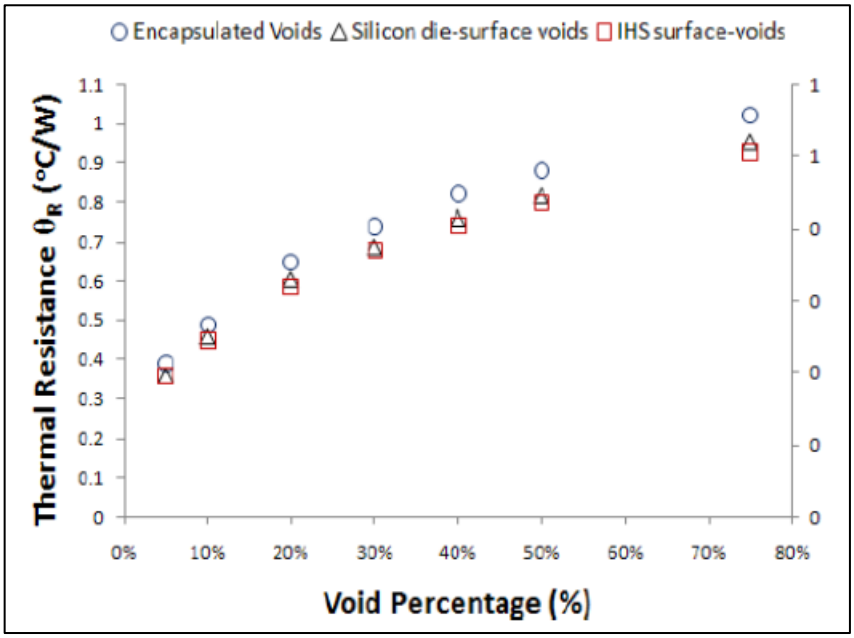


Figure 2.2: Thermal resistance due to different void styles (Otiaba et al., 2011).

2.4 Design of Experiment

By using designed experiment, the outcome of experiment can help to determine which of the process variables has the greatest influence on process performance. There are many ways to conduct an experiment. If the number of factors in a factorial experiment is too large, two levels for each factor is usually analysed which are the minimum and maximum effect. If there is *k*-factor set for two levels each, the total of experimental combinations is 2^k, which is called 2^k experimental design. The notations used to express the levels are "-1" to denote low and "+1" to denote high.

The interaction factors are called effect and calculated using formula $C^k{}_j = \frac{k!}{j!(k-j)!}$, where j denotes *j*-factor interaction. Table 2.1 shows the main and interaction factor, number of effects, and factor designator for *k* = 2, 3, 4 and 5.

Table 2.1: Main and interaction factor, number of effects, and factor designator for *k* = 2, 3, 4 and 5.

k Factor	No of effects 2^k -1	Main Factor	Two-factor Interaction	Three-factor Interaction	Four-factor Interaction	Five-factor Interaction
1	1	1	0	0	0	0
		A	-	-	-	-
2	3	2	1	0	0	0
		A, B	*AB*	-	-	-
3	7	3	2	1	0	0
		A, B, C	*AB, AC, BC*	*ABC*	-	-
4	15	4	6	4	1	0
		A, B, C, D	*AB, AC, AD, BC, BD, CD*	*ABC, ABD, ACD, BCD*	*ABCD*	-
5	31	5	10	10	5	1
		A, B, C, D, E	*AB, AC, AD, AE, BC, BD, BE, CD, CE, DE*	*ABC, ABD, ABE, ACD, ACE, ADE, BCD, BCE, BDE, CDE,*	*ABCD, ABCE, ABDE, ACDE, BCDE*	*ABCDE*

The total sum of squares SS_T is equal to $SS_T = \sum_{i=1}^{2^k} \sum_{k=1}^{n} y^2{}_{ik} - \frac{(\sum_{i=1}^{2^k} \sum_{k=1}^{n} yik)^2}{2^k n}$. This is because, each factor is set to two levels only. The degrees of freedom are $(2^k n - 1)$. The formula for calculating the sum of squares for every factor and sum of square of error is shown in equation 2.1.

$$\text{SS(any factor)} = \frac{(Sum\ of\ observation\ at\ "-"level)^2}{(Number\ of\ observation\ at\ -level)} + \frac{(Sum\ of\ observation\ at\ "+"level)^2}{(Sum\ of\ observation\ at\ "+"level)^2} - \frac{(Grand\ sum\ of\ all\ observations)^2}{(Total\ number\ of\ observations)}$$

Sum of Square of Error = Total sum of squares – Sum of squares for all factors

(2.1)

Where "-1" denotes low level of factor *j* and "+1" indicates high level of factor *j*. For any factors, its degrees of freedom is (2 -1). The total degrees of freedom is (2^kn-1), whilst the degrees of freedom for error is number of effect multiplied by number of duplicate. The formula to calculate Mean Square of any factor and Mean Square of error is as per equation 2.2 below.

$$\text{Mean Square (any factor)} = \frac{Sum\ of\ square\ of\ (any\ factor)}{Degreees\ of\ Freedom\ (any\ factor)}$$

$$\text{Mean Square (Error)} = \frac{Sum\ of\ square\ of\ error}{Degrees\ of\ freedom\ for\ error}$$

(2.2)

Calculated F-Value is per equation 2.3;

$$\text{Calculated F-Value} = \frac{Mean\ Square\ (any\ factor)}{Mean\ Square\ (Error)}$$

(2.3)

The analysis of variance ANOVA for all factors and the F-test matrix is summarizes per table 2.2.

Table 2.2: ANOVA table for five factor two level design

Factor	Sum of Square	Degrees of freedom	Mean Square	Calculated F-Value	F-value from statistical table
A . . . ABCDE	SS_A . . . SS_{ABCDE}	(2 – 1) . . . (2 – 1)	$SS_A/(2-1)$ . . . $SS_{ABCDE}/(2-1)$	MSA/MSE . . . MABCDE/MSE	F_α [(2-1),$(2^k n-1)-(2^k-1)$ . . . F_α [(2 – 1)(b-1)(c-1)(d-1)(e-1), abcde(n-1)]
ERROR	SS_E	$(2^k n)-(2^k-1)$	$MSE/(2^k n)-(2^k-1)$	-	-
TOTAL	SS_T	$(2^k n-1)$	-	-	-

($T_1 – T_2$) is called as contrast of the factor. T_1 indicates the "+1" value of factor while T_2 indicates the "-1" value of factor. Equation 2.4 shows the contrast value calculation. Thus, the contrast values for all the factors are tabulated per Table 2.3.

Contrast value (any factor) = Sum of T_1 – Sum of T_2 (2.4)

The associated effect of factor can be calculated per formula 2.5

$$\text{Associated Effect of any main factor or interaction} = 2(T_1\text{-}T_2)/2^k \quad (2.5)$$

Associated effect allows one to know the effect of the factor on the output response. A positive value means factor has direct effect on the output response while negative value means factor has negative effect on the output response.

CHAPTER 3

METHODOLOGY AND WORK PLAN

3.1 Introduction

This chapter contains the project timeline and experimental procedures conducted in this study. Six sigma tools have identified the possible root cause which are not optimized die attach parameter. DOE will be conducted to validate the root cause. The procedure of DOE will be explained further in this chapter.

3.2 Project Timeline

Table 3.1 shows the Gantt chart on the project progress.

Table 3.1: Gantt chart on project progress

Details	W3	W4	W5	W6	W7	W8	W9	W10	W11	W12	W13
Project Report selection											
Confirmation of Project Report											
Submission of Project Proposal											
Define Phase											
Problem statement and objective											
Measure phase											
SIPOC mapping											
Key Indicator (KPIV/KPOV)											
Analyze											
Top down chart											
Is and Is Not mapping											
Fishbone Diagram											
Design Of Experiment											

	In-Progress
	Completed
	Delay

3.3 DOE matrix and arrangement

The DOE was conducted using Alphasem E8003 die bonder and conducted on the morning shift. Listed in table 3.2 are the materials involved on this experiment;

Table 3.2: DOE setting at die attach area

Setting	Description
Lead Frame	Copper based lead frame
Solder Paste	PbSnAg
Collet	Rubber and Delrin collet
Input parameter	Pick force, bond force, needle height, separation time and post ejection delay
Sample size	6 units per run

Table 3.3 shows severity guidelines for the crack die analysis for DOE.

Table 3.3: Severity rating based on value

Value	Justification
100	Vertical crack line same as customer return pattern
85	Vertical crack line from bottom
70	Lateral Crack
60	Shell chip at die bottom
30	Random chipping at die bottom (big size)
20	Corner Chip
5	Random chipping at die bottom (small size)
0	No crack and chip die

3.4 Design of Experiment method

The design of experiment designed using five factor two level experiment. Table 3.4 contains all two level five factors die attach parameters to be performed in the DOE full factorial plan with 6 selected sample. The parameter limit setting is set using current die attach setting limit.

Table 3.4: Full factorial DOE five factor two levels

Factor	Low	High
Collet type A	Rubber	Delrin
Separation time B	20ms	80ms
Pick Force C	0.6N	1.0N
Bond Force D	0.6N	1.0N
Ejector needle height E	0.6mm	0.9mm

Table 3.5 shows the full factorial DOE plan. Table 3.6 lists all possible interaction factors from the main factors. The notations used to express the levels are "-1" to denote low and "+1" to denote high. Note that 31 interaction factor column in Table 3.6 is a product of all combination of A,B, C, D, E. To estimate an effect, a table of plus and minus which indicates high and low levels of factor A, B, C, D and E can be used through multiplication.

Table 3.5: Full factorial DOE plan

Run	Factor					Duplicate						Sum of Experiment
	A	B	C	D	E	1	2	3	4	5	6	
1	Rubber	20ms	0.6N	0.6N	0.6mm							
2	Rubber	20ms	0.6N	0.6N	0.9mm							
3	Rubber	20ms	0.6N	1.0N	0.6mm							
4	Rubber	20ms	0.6N	1.0N	0.9mm							
5	Rubber	20ms	1.0N	0.6N	0.6mm							
6	Rubber	20ms	1.0N	0.6N	0.9mm							
7	Rubber	20ms	1.0N	1.0N	0.6mm							
8	Rubber	20ms	1.0N	1.0N	0.9mm							
9	Rubber	80ms	0.6N	0.6N	0.6mm							
10	Rubber	80ms	0.6N	0.6N	0.9mm							
11	Rubber	80ms	0.6N	1.0N	0.6mm							
12	Rubber	80ms	0.6N	1.0N	0.9mm							
13	Rubber	80ms	1.0N	0.6N	0.6mm							
14	Rubber	80ms	1.0N	0.6N	0.9mm							
15	Rubber	80ms	1.0N	1.0N	0.6mm							
16	Rubber	80ms	1.0N	1.0N	0.9mm							
17	Delrin	20ms	0.6N	0.6N	0.6mm							
18	Delrin	20ms	0.6N	0.6N	0.9mm							
19	Delrin	20ms	0.6N	1.0N	0.6mm							
20	Delrin	20ms	0.6N	1.0N	0.9mm							
21	Delrin	20ms	1.0N	0.6N	0.6mm							
22	Delrin	20ms	1.0N	0.6N	0.9mm							
23	Delrin	20ms	1.0N	1.0N	0.6mm							
24	Delrin	20ms	1.0N	1.0N	0.9mm							
25	Delrin	80ms	0.6N	0.6N	0.6mm							
26	Delrin	80ms	0.6N	0.6N	0.9mm							
27	Delrin	80ms	0.6N	1.0N	0.6mm							
28	Delrin	80ms	0.6N	1.0N	0.9mm							
29	Delrin	80ms	1.0N	0.6N	0.6mm							
30	Delrin	80ms	1.0N	0.6N	0.9mm							
31	Delrin	80ms	1.0N	1.0N	0.6mm							
32	Delrin	80ms	1.0N	1.0N	0.9mm							

Table 3.6: Full factorial DOE plan interaction factor

Factors					Interaction Factor																												
A	B	C	D	E	A	AB	ABC	ABCD	ABCDE	ABCE	ABD	ABDE	ABE	AC	ACD	ACDE	ACE	AD	ADE	AE	B	BC	BCD	BCDE	BCE	BD	BDE	BE	C	CD	CDE	CE	D	E	ED
-1	-1	-1	-1	-1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	-1	1
-1	-1	-1	-1	1	-1	1	-1	1	1	-1	-1	-1	1	1	-1	-1	1	1	1	-1	-1	1	-1	-1	1	1	1	-1	-1	1	-1	-1	1	-1	-1
-1	-1	-1	1	-1	-1	1	-1	-1	1	1	1	-1	-1	1	1	-1	-1	-1	1	1	-1	1	1	-1	-1	-1	1	1	-1	-1	1	1	1	-1	-1
-1	-1	-1	1	1	-1	1	-1	-1	-1	-1	1	1	1	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	1	1	1
-1	-1	1	-1	-1	-1	1	1	-1	1	-1	-1	1	-1	-1	1	-1	1	1	-1	1	-1	-1	1	-1	1	1	-1	1	1	-1	1	-1	-1	-1	1
-1	-1	1	-1	1	-1	1	1	-1	-1	1	-1	-1	1	-1	1	1	-1	1	1	-1	-1	-1	1	1	-1	1	1	-1	1	-1	-1	1	-1	1	-1
-1	-1	1	1	-1	-1	1	1	1	-1	-1	1	-1	-1	-1	-1	1	1	-1	1	1	-1	-1	-1	1	1	-1	1	1	1	1	-1	-1	1	-1	-1
-1	-1	1	1	1	-1	1	1	1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	1	1	1	1	1	1	1
-1	1	-1	-1	-1	-1	-1	1	-1	1	-1	1	-1	1	1	-1	1	-1	1	-1	1	1	-1	1	-1	1	-1	1	-1	-1	1	-1	1	-1	-1	1
-1	1	-1	-1	1	-1	-1	1	-1	-1	1	1	1	-1	1	-1	-1	1	1	1	-1	1	-1	1	1	-1	-1	-1	1	-1	1	1	-1	-1	1	-1
-1	1	-1	1	-1	-1	-1	1	1	-1	-1	-1	1	1	1	1	-1	-1	-1	1	1	1	-1	-1	1	1	1	-1	-1	-1	-1	1	1	1	-1	-1
-1	1	-1	1	1	-1	-1	1	1	1	1	-1	-1	-1	1	1	1	1	-1	-1	-1	1	-1	-1	-1	1	1	1	-1	-1	-1	-1	1	1	1	1
-1	1	1	-1	-1	-1	-1	-1	1	-1	1	1	-1	1	-1	1	-1	1	1	-1	1	1	1	-1	1	-1	-1	1	-1	1	-1	-1	-1	-1	-1	1
-1	1	1	-1	1	-1	-1	-1	1	1	-1	1	1	-1	-1	1	1	-1	1	1	-1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	1	-1	1	-1
-1	1	1	1	-1	-1	-1	-1	-1	1	1	-1	1	1	-1	-1	1	1	-1	1	1	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	1	-1	-1
-1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	-1	-1	-1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	-1	1
1	-1	-1	-1	1	1	-1	1	-1	-1	1	1	1	-1	-1	1	1	-1	-1	-1	1	-1	1	-1	-1	1	1	1	-1	-1	1	1	-1	-1	1	-1
1	-1	-1	1	-1	1	-1	1	1	-1	-1	-1	1	1	-1	-1	1	1	1	-1	-1	-1	1	1	-1	-1	-1	1	1	-1	-1	1	1	1	-1	-1
1	-1	-1	1	1	1	-1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	1	1	1	-1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	1	1	1
1	-1	1	-1	-1	1	-1	-1	1	-1	1	1	-1	1	1	-1	1	-1	-1	1	-1	-1	-1	1	-1	1	1	-1	1	1	-1	1	-1	-1	-1	1
1	-1	1	-1	1	1	-1	-1	1	-1	1	1	-1	1	1	-1	1	-1	-1	1	-1	-1	-1	1	-1	1	1	-1	1	1	-1	1	-1	-1	1	-1
1	-1	1	1	-1	1	-1	-1	-1	1	1	1	-1	1	1	-1	1	-1	-1	-1	1	-1	1	-1	-1	1	1	1	-1	-1	1	1	-1	-1	1	-1
1	-1	1	1	1	1	-1	-1	-1	-1	1	1	-1	1	1	-1	1	-1	-1	1	-1	-1	-1	1	-1	1	1	-1	1	1	-1	1	-1	-1	1	-1
1	1	-1	-1	-1	1	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	-1	1
1	1	-1	-1	1	1	1	-1	1	1	-1	-1	-1	1	1	-1	-1	1	1	1	-1	-1	1	-1	-1	1	1	1	-1	-1	1	1	-1	-1	1	-1
1	1	-1	1	-1	1	1	-1	-1	1	1	1	-1	-1	-1	-1	1	1	1	-1	-1	-1	1	1	1	-1	-1	-1	1	1	1	-1	-1	-1	1	-1
1	1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	-1	-1	-1	-1	1	1	1
1	1	1	-1	-1	1	1	1	-1	1	-1	-1	1	-1	1	-1	1	-1	-1	1	-1	1	1	-1	1	-1	-1	1	-1	1	-1	1	-1	-1	-1	1
1	1	1	-1	1	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	1	-1	-1	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	1	-1	1	-1
1	1	1	1	-1	1	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	1	-1	-1	1	1	1	-1	-1	1	-1	-1	1	1	-1	-1	1	-1	-1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

3.5 Failure analysis method using destructive test

All samples of DOE experiment are decapsulated, and performed inspection of severity of crack, and table the results shown in Table 3.5.

CHAPTER 4

RESULTS AND DISCUSSIONS

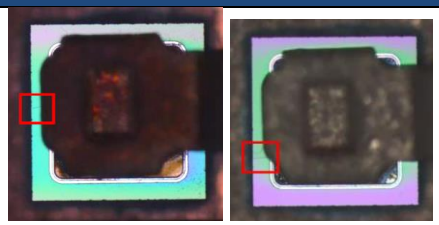
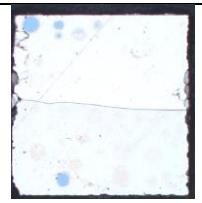
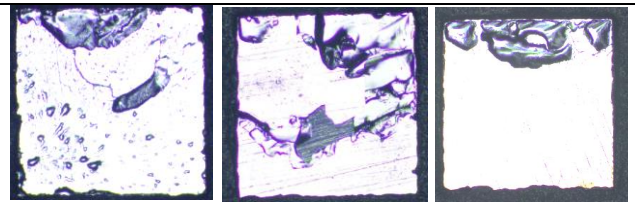
4.1 Introduction

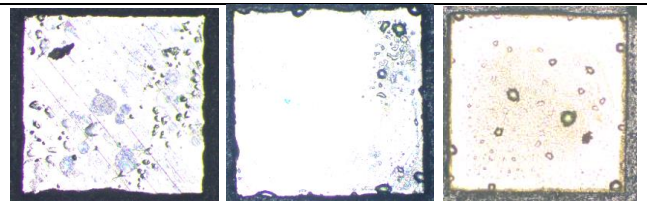
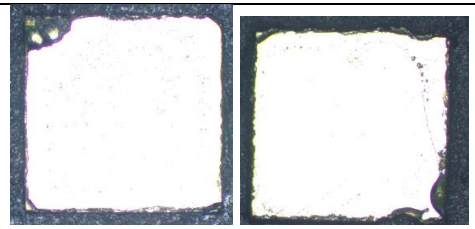
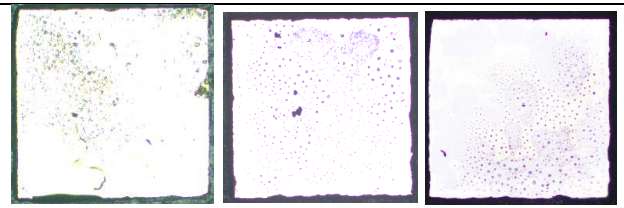
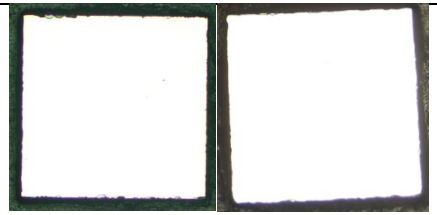
Prior to the DOE, all the root cause investigation were conducted through the usage of DMAIC tools. This chapter will discuss about the outcome of the DOE conducted per methodology section which are the DOE decapsulation results, the severity rating tabulated results, analysis of variance and associate Effect analysis and discussion, and the optimized setting.

4.2 DOE decapsulation result

Results of decapsulation for the analysing the crack with sample results shown in Table 4.1.

Table 4.1: Sampling of decapsulation unit result

Percentage	Justification	Image
100	Vertical crack line same as customer return pattern	
85	Vertical crack line from bottom	
70	Lateral Crack	
60	Shell chip at die bottom	

30	Random chipping at die bottom (big size)	
20	Corner Chip	
5	Random chipping at die bottom (small size)	
0	No crack and chip	

The tabulated results of the DOE is shown in Table 4.2.

Table 4.2: Tabulated result of DOE

Run	Factor					Duplicate						Sum of Experiment
	A	B	C	D	E	1	2	3	4	5	6	
1	Rubber	20ms	0.6N	0.6N	0.6mm	0	0	0	0	30	0	30
2	Rubber	20ms	0.6N	0.6N	0.9mm	0	30	0	0	0	0	30
3	Rubber	20ms	0.6N	1.0N	0.6mm	0	0	30	0	0	0	30
4	Rubber	20ms	0.6N	1.0N	0.9mm	0	0	5	5	0	0	10
5	Rubber	20ms	1.0N	0.6N	0.6mm	5	0	0	5	0	0	10
6	Rubber	20ms	1.0N	0.6N	0.9mm	5	0	0	0	0	0	5
7	Rubber	20ms	1.0N	1.0N	0.6mm	0	70	20	0	5	0	95
8	Rubber	20ms	1.0N	1.0N	0.9mm	0	0	60	60	0	0	120
9	Rubber	80ms	0.6N	0.6N	0.6mm	0	0	0	0	0	0	0
10	Rubber	80ms	0.6N	0.6N	0.9mm	0	0	0	0	5	0	5
11	Rubber	80ms	0.6N	1.0N	0.6mm	0	0	0	0	20	0	20
12	Rubber	80ms	0.6N	1.0N	0.9mm	30	0	5	20	0	5	60
13	Rubber	80ms	1.0N	0.6N	0.6mm	0	0	0	0	0	5	5
14	Rubber	80ms	1.0N	0.6N	0.9mm	5	0	0	5	0	0	10

15	Rubber	80ms	1.0N	1.0N	0.6mm	30	5	0	5	30	0	70
16	Rubber	80ms	1.0N	1.0N	0.9mm	0	0	70	30	0	0	100
17	Delrin	20ms	0.6N	0.6N	0.6mm	0	30	0	0	5	0	35
18	Delrin	20ms	0.6N	0.6N	0.9mm	60	0	0	0	5	0	65
19	Delrin	20ms	0.6N	1.0N	0.6mm	0	30	0	5	0	5	40
20	Delrin	20ms	0.6N	1.0N	0.9mm	70	0	0	0	0	60	130
21	Delrin	20ms	1.0N	0.6N	0.6mm	0	5	0	30	0	0	35
22	Delrin	20ms	1.0N	0.6N	0.9mm	5	70	70	30	5	5	185
23	Delrin	20ms	1.0N	1.0N	0.6mm	30	70	20	0	0	0	120
24	Delrin	20ms	1.0N	1.0N	0.9mm	0	85	100	60	5	100	350
25	Delrin	80ms	0.6N	0.6N	0.6mm	0	0	0	30	30	5	65
26	Delrin	80ms	0.6N	0.6N	0.9mm	5	5	0	0	85	20	115
27	Delrin	80ms	0.6N	1.0N	0.6mm	20	0	0	30	0	30	80
28	Delrin	80ms	0.6N	1.0N	0.9mm	0	60	0	5	5	0	70
29	Delrin	80ms	1.0N	0.6N	0.6mm	30	0	0	20	5	30	85
30	Delrin	80ms	1.0N	0.6N	0.9mm	60	5	5	5	20	5	100
31	Delrin	80ms	1.0N	1.0N	0.6mm	30	0	30	5	30	5	100
32	Delrin	80ms	1.0N	1.0N	0.9mm	20	5	20	60	85	70	260

4.3 Analysis of Variance and Associate Effect Analysis and Discussion

Total sum of square calculation;

$$SS_T = \sum_{i=1}^{2^5} \sum_{k=1}^{6} y^2_{ik} - \frac{(\sum_{i=1}^{2^5} \sum_{k=1}^{6} yik)^2}{(2^5)(6)}$$

$$= 99934.24$$

The sum of squares, degrees of freedom, mean square value and calculated F-value was calculated per formula given in chapter 2 sub-section 2.4 and the result was tabulated in Table 4.3. The analysis of variance ANOVA for all factors and the F-test results for α=0.05 or 95% confidence level are analysed and compared with F-value from F-table (Appendix C).

Table 4.3: ANOVA table for five-factor two level design

Factor	Sum of square of	Degrees of Freedom of	Mean square	Calculated F-value	F-Value from F-Table @ α=0.05	Remarks
A	7943.8802	1	7943.8802	18.29	$F_{0.05}[1,161]=3.89$	Significant
AB	3.2552	1	3.2552	0.01	$F_{0.05}[1,161]=3.89$	Not significant
ABC	159.5052	1	159.5052	0.37	$F_{0.05}[1,161]=3.89$	Not significant
ABCD	141.7969	1	141.7969	0.33	$F_{0.05}[1,161]=3.89$	Not significant
ABCDE	312.6302	1	312.6302	0.72	$F_{0.05}[1,161]=3.89$	Not significant
ABCE	29.2969	1	29.2969	0.07	$F_{0.05}[1,161]=3.89$	Not significant
ABD	263.6719	1	263.6719	0.61	$F_{0.05}[1,161]=3.89$	Not significant
ABDE	57.4219	1	57.4219	0.13	$F_{0.05}[1,161]=3.89$	Not significant
ABE	693.8802	1	693.8802	1.60	$F_{0.05}[1,161]=3.89$	Not significant
AC	854.2969	1	854.2969	1.97	$F_{0.05}[1,161]=3.89$	Not significant
ACD	37.6302	1	37.6302	0.09	$F_{0.05}[1,161]=3.89$	Not significant
ACDE	178.2552	1	178.2552	0.41	$F_{0.05}[1,161]=3.89$	Not significant
ACE	693.8802	1	693.8802	1.60	$F_{0.05}[1,161]=3.89$	Not significant
AD	15.7552	1	15.7552	0.04	$F_{0.05}[1,161]=3.89$	Not significant
ADE	125.1302	1	125.1302	0.29	$F_{0.05}[1,161]=3.89$	Not significant
AE	2100.1302	1	2100.1302	4.83	$F_{0.05}[1,161]=3.89$	Significant
B	109.5052	1	109.5052	0.25	$F_{0.05}[1,161]=3.89$	Not significant
BC	287.6302	1	287.6302	0.66	$F_{0.05}[1,161]=3.89$	Not significant
BCD	68.8802	1	68.8802	0.16	$F_{0.05}[1,161]=3.89$	Not significant
BCDE	81.3802	1	81.3802	0.19	$F_{0.05}[1,161]=3.89$	Not significant
BCE	159.5052	1	159.5052	0.37	$F_{0.05}[1,161]=3.89$	Not significant
BD	81.3802	1	81.3802	0.19	$F_{0.05}[1,161]=3.89$	Not significant
BDE	0.1302	1	0.1302	0.00	$F_{0.05}[1,161]=3.89$	Not significant
BE	218.8802	1	218.8802	0.50	$F_{0.05}[1,161]=3.89$	Not significant
C	3897.0052	1	3897.0052	8.97	$F_{0.05}[1,161]=3.89$	Significant
CD	2443.8802	1	2443.8802	5.63	$F_{0.05}[1,161]=3.89$	Significant
CDE	365.7552	1	365.7552	0.84	$F_{0.05}[1,161]=3.89$	Not significant
CE	940.7552	1	940.7552	2.17	$F_{0.05}[1,161]=3.89$	Not significant
D	3987.6302	1	3987.6302	9.18	$F_{0.05}[1,161]=3.89$	Significant
E	3291.7969	1	3291.7969	7.58	$F_{0.05}[1,161]=3.89$	Significant
ED	453.2552	1	453.2552	1.04	$F_{0.05}[1,161]=3.89$	Not significant
Error	69936.4583	161	434.3879	-	-	
Total	99934.24479	192	-	-	-	

Table 4.4: Significant factor in ANOVA table

Significant factor	Interaction
A	Collet type
B	Separation Time
E	Ejector needle height
A*B	Collet type and separation time
A*B*C*D	Collet type, separation time, pick force, bond force
A*B*C*D*E	All interaction
A*B*E	Collet type, separation time and needle height
A*C*D	Collet type, pick force, bond force
A*C*D*E	Collet type, needle height, pick force, bond force
A*E	Collet type and needle height

B*C*D	Separation time, pick force, bond force
B*C*D*E	Separation time, pick force, bond force, needle height
B*E	Separation time and needle height
C*D	Pick force and bond force
C*D*E	Pick force, bond force, needle height

All of the calculated F-value is compared to F-value from F [1, 161] at α=0.05 or 95% confidence level, which is 3.89. Table 4.3 summarizes the main factor and interaction factors that significantly contribute to crack die. The DOE shows that main factor A, C, D and E and interaction factor AE and CD can significantly cause crack die. All the other factors calculated F-Value is lesser than given F-value from α=0.05 table thus can be classified as not significant. Table 4.6 lists all the contrast values and the associated effects of factors.

Table 4.5: Contrast values and associated factors

Factors	Sum of "-1"	Sum of "+1"	Contrast	Associated factor
A	600	1835	-1235	-12.8646
B	1290	1145	145	1.5104
C	785	1650	-865	-9.0104
D	780	1655	-875	-9.1146
E	820	1615	-795	-8.2813
AB	1230	1205	25	0.2604
ABC	1305	1130	175	1.8229
ABCD	1135	1300	-165	-1.7188
ABCDE	1095	1340	-245	-2.5521
ABCE	1255	1180	75	0.7813
ABD	1330	1105	225	2.3438
ABDE	1270	1165	105	1.0938
ABE	1400	1035	365	3.8021
AC	1015	1420	-405	-4.2188
ACD	1175	1260	-85	-0.8854
ACDE	1125	1310	-185	-1.9271
ACE	1035	1400	-365	-3.8021
AD	1190	1245	-55	-0.5729

ADE	1140	1295	-155	-1.6146
AE	900	1535	-635	-6.6146
BC	1335	1100	235	2.4479
BCD	1275	1160	115	1.1979
BCDE	1155	1280	-125	-1.3021
BCE	1305	1130	175	1.8229
BD	1280	1155	125	1.3021
BDE	1220	1215	5	0.0521
BE	1320	1115	205	2.1354
CD	875	1560	-685	-7.1354
CDE	1085	1350	-265	-2.7604
CE	1005	1430	-425	-4.4271
ED	1070	1365	-295	-3.0729

From the table 4.4 result, the effect due to factor A is the highest contrast value which is -12.86 compared to factor D which is -9.1146 and followed by factor C and factor E.

The results has shown by using rubber collet, is the best significant factor to reduce the crack die occurrence. The association factor shows the higher the negative value, the better the improvement on the crack die. It indicates that lower bond force, pick force and ejector needle can contribute to improvement on the crack die.

Table 4.6: Proposed die attach setting

Factor	Current setting	Proposed setting
Collet type A	Delrin	Rubber
Pick Force C	0.9N	0.6N
Bond Force D	0.9N	0.6N
Ejector needle height E	0.9mm	0.6mm

By using the proposed die attach settings, no crack die was observed after sampling of one hundred units from the production lots.

CHAPTER 5

CONCLUSIONS AND RECOMMENDATIONS

5.1 Conclusions

A lot of studies have been done regarding crack die improvement in semiconductor field. There are many factors that may contribute to crack die such as die bond parameter not optimized, silicon defect during wafer fabrication process, solder void issue during reflow, CTE mismatch, mechanical stress, insufficient solder thickness and package stress. Thus, studies from similar defect mode are greatly contributing to this crack die improvement project to understand the crack mechanism and narrow down the possible root cause.

The DOE performed able to replicate the customer return crack pattern. Based on the DOE results, four out of five main factors which are collet type, pick force, bond force and ejector needle settings was identified to significantly contribute to die crack issue. The associated effect was studied to obtain the optimized setting. The results shown that rubber type collet is the most contributing factor to reduce crack die follows by lower pick force, bond force and ejector needle. The optimized parameter was implemented and no crack die was observed after sampling of one hundred units from production lots.

5.2 Recommendations for future work

The DOE results in this project have shown the significant factor contributing to crack die. However, future work for this project is to replicate this experiment through Taguchi method to find the best optimized parameter for die attach area.

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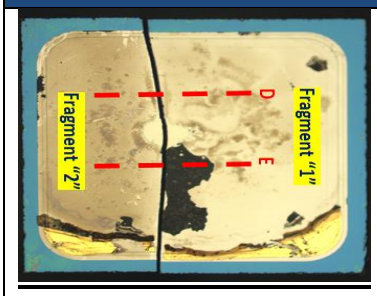
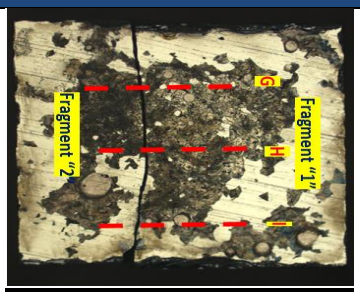
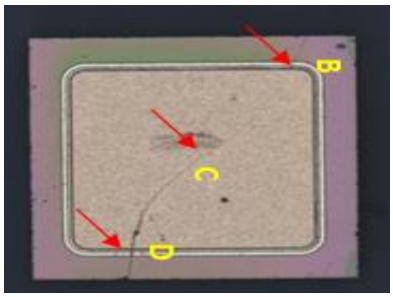
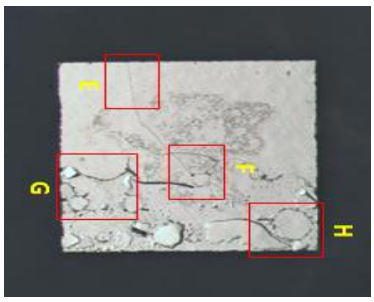
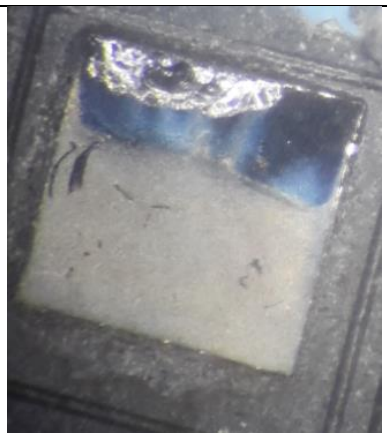
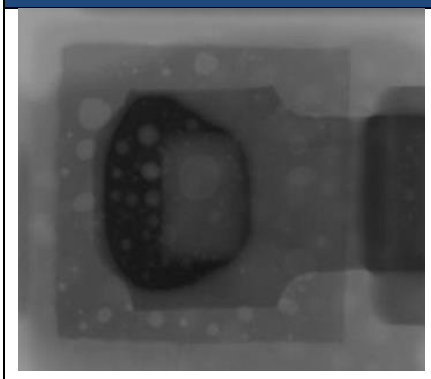
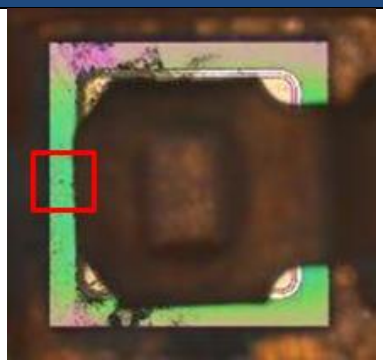
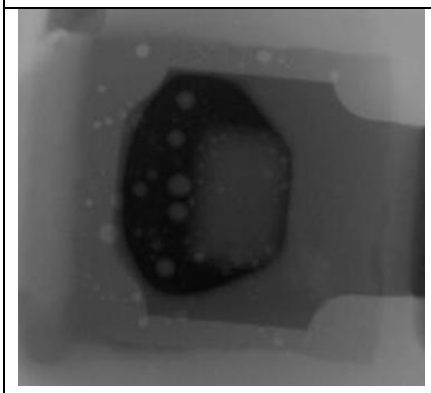
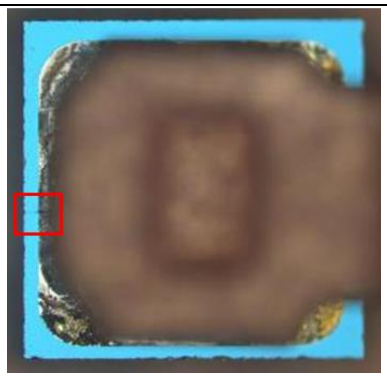
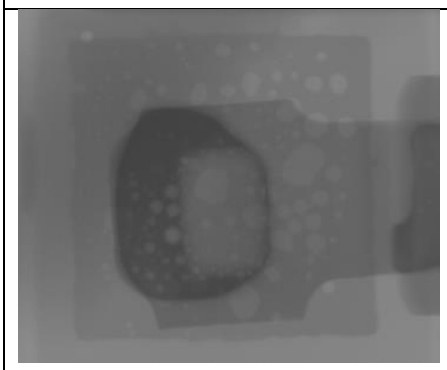
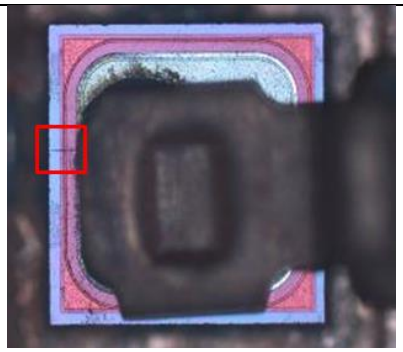
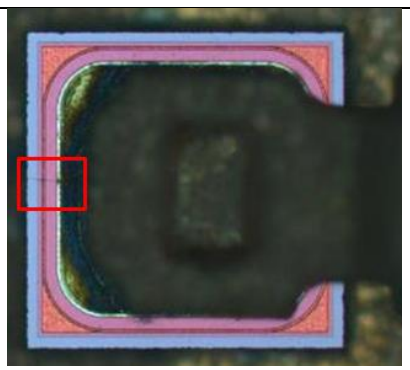
APPENDICES

Appendix A: Crack die pattern

Top Side	Back side	Remarks
		Vertical crack
		Diagonal crack
N/A		Lateral crack

Appendix B: Crack die image mapping vs solder void location

Solder Void	Crack Line	Remarks
		No correlation to crack location
		No correlation to crack location
		No correlation to crack location
		No correlation to crack location

Appendix C: F-Tables at α=0.05

TABLE E

F critical values (continued)

Degrees of freedom in the denominator			Degrees of freedom in the numerator								
		p	1	2	3	4	5	6	7	8	9
	28	.100	2.89	2.50	2.29	2.16	2.06	2.00	1.94	1.90	1.87
		.050	4.20	3.34	2.95	2.71	2.56	2.45	2.36	2.29	2.24
		.025	5.61	4.22	3.63	3.29	3.06	2.90	2.78	2.69	2.61
		.010	7.64	5.45	4.57	4.07	3.75	3.53	3.36	3.23	3.12
		.001	13.50	8.93	7.19	6.25	5.66	5.24	4.93	4.69	4.50
	29	.100	2.89	2.50	2.28	2.15	2.06	1.99	1.93	1.89	1.86
		.050	4.18	3.33	2.93	2.70	2.55	2.43	2.35	2.28	2.22
		.025	5.59	4.20	3.61	3.27	3.04	2.88	2.76	2.67	2.59
		.010	7.60	5.42	4.54	4.04	3.73	3.50	3.33	3.20	3.09
		.001	13.39	8.85	7.12	6.19	5.59	5.18	4.87	4.64	4.45
	30	.100	2.88	2.49	2.28	2.14	2.05	1.98	1.93	1.88	1.85
		.050	4.17	3.32	2.92	2.69	2.53	2.42	2.33	2.27	2.21
		.025	5.57	4.18	3.59	3.25	3.03	2.87	2.75	2.65	2.57
		.010	7.56	5.39	4.51	4.02	3.70	3.47	3.30	3.17	3.07
		.001	13.29	8.77	7.05	6.12	5.53	5.12	4.82	4.58	4.39
	40	.100	2.84	2.44	2.23	2.09	2.00	1.93	1.87	1.83	1.79
		.050	4.08	3.23	2.84	2.61	2.45	2.34	2.25	2.18	2.12
		.025	5.42	4.05	3.46	3.13	2.90	2.74	2.62	2.53	2.45
		.010	7.31	5.18	4.31	3.83	3.51	3.29	3.12	2.99	2.89
		.001	12.61	8.25	6.59	5.70	5.13	4.73	4.44	4.21	4.02
	50	.100	2.81	2.41	2.20	2.06	1.97	1.90	1.84	1.80	1.76
		.050	4.03	3.18	2.79	2.56	2.40	2.29	2.20	2.13	2.07
		.025	5.34	3.97	3.39	3.05	2.83	2.67	2.55	2.46	2.38
		.010	7.17	5.06	4.20	3.72	3.41	3.19	3.02	2.89	2.78
		.001	12.22	7.96	6.34	5.46	4.90	4.51	4.22	4.00	3.82
	60	.100	2.79	2.39	2.18	2.04	1.95	1.87	1.82	1.77	1.74
		.050	4.00	3.15	2.76	2.53	2.37	2.25	2.17	2.10	2.04
		.025	5.29	3.93	3.34	3.01	2.79	2.63	2.51	2.41	2.33
		.010	7.08	4.98	4.13	3.65	3.34	3.12	2.95	2.82	2.72
		.001	11.97	7.77	6.17	5.31	4.76	4.37	4.09	3.86	3.69
	100	.100	2.76	2.36	2.14	2.00	1.91	1.83	1.78	1.73	1.69
		.050	3.94	3.09	2.70	2.46	2.31	2.19	2.10	2.03	1.97
		.025	5.18	3.83	3.25	2.92	2.70	2.54	2.42	2.32	2.24
		.010	6.90	4.82	3.98	3.51	3.21	2.99	2.82	2.69	2.59
		.001	11.50	7.41	5.86	5.02	4.48	4.11	3.83	3.61	3.44
	200	.100	2.73	2.33	2.11	1.97	1.88	1.80	1.75	1.70	1.66
		.050	3.89	3.04	2.65	2.42	2.26	2.14	2.06	1.98	1.93
		.025	5.10	3.76	3.18	2.85	2.63	2.47	2.35	2.26	2.18
		.010	6.76	4.71	3.88	3.41	3.11	2.89	2.73	2.60	2.50
		.001	11.15	7.15	5.63	4.81	4.29	3.92	3.65	3.43	3.26
	1000	.100	2.71	2.31	2.09	1.95	1.85	1.78	1.72	1.68	1.64
		.050	3.85	3.00	2.61	2.38	2.22	2.11	2.02	1.95	1.89
		.025	5.04	3.70	3.13	2.80	2.58	2.42	2.30	2.20	2.13
		.010	6.66	4.63	3.80	3.34	3.04	2.82	2.66	2.53	2.43
		.001	10.89	6.96	5.46	4.65	4.14	3.78	3.51	3.30	3.13