CHARACTERIZATION OF HIGH VOLTAGE POWER SCHOTTKY DIODE UNDER UNCLAMPED INDUCTANCE SWITCHING (UIS) AVALANCHE STRESS

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A project report submitted in partial fulfilment of the requirements for the award of Master of Engineering (Electronics System)

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> > April 2019

DECLARATION

I hereby declare that this project report is based on my original work except for citations and quotations which have been duly acknowledged. I also declare that it has not been previously and concurrently submitted for any other degree or award at UTAR or other institutions.

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ACKNOWLEDGEMENTS

I would like to thank everyone who had contributed to the successful completion of this project. I would like to express my gratitude to my research supervisor, Dr. Yeoh Keat Hoe for his invaluable advice, guidance and his enormous patience throughout the development of the research.

In addition, I would like to thank the employees from Amkor Technology Malaysia to success my data collection throughout the research.

Lastly, I would also like to express my deepest gratitude to my loving parents, family and friends who had helped and given me encouragement.

ABSTRACT

Nowadays, power electronic plays an important role due to the continuing growth of electrification and control of functions in applications such as consumer, commercial, industrial, transportation and medical application. Power Schottky diodes are commonly used in high switching applications and thus, it is necessary to ensure stability, robustness and reliability. The assessment can be evaluated through the device's ability to withstand avalanche breakdown regime, which is usually assessed under the rigorous test condition such as unclamped inductive switching (UIS) conditions. Therefore, avalanche ruggedness is essential for standard reliability test and is an important asset for the overall system. In this project, 60 V rated voltage and 100 V rated voltage of Power Schottky diodes in PSMC packages are measured with non-repetitive pulse and repetitive pulse of avalanche test. The actual breakdown voltage obtained from the experiments are higher than the rated reverse voltage of the devices. Using a 0.3 mH inductance, the 60 V rated voltage devices are measured up to drain current (I_D) of 20.9 A, resulting to the maximum amount of avalanche energy that the device can withstand of 0.124 J. For 100 V rated voltage device, the maximum avalanche energy is measured up to 0.271 J at 16.4 A. Repetitive pulse avalanche test yielded good stability of the samples by using the median value defined from the drain current before destruction point. Full characteristics test such as forward voltage and reverse voltage are measured prior to UIS test and additionally after UIS test. The results shown no obvious degradation, with which P-values exceeded 0.005 for either 60 V rated voltage device, or 100 V rated voltage device. Lastly, the optimum drain current (I_D) values and related UIS test time are determined.

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LIST OF SYMBOLS / ABBREVIATIONS

UIS	unclamped inductive switching
DUT	device under test
L	inductance, H
V _{GS}	gate source voltage, V
B _{VDSS}	drain source breakdown voltage, V
I _D	drain current, A
I _R	reverse current, A
V_{F}	forward voltage, V
V _R	reverse voltage, V
V _{DS}	drain source voltage, V
V _{DD}	supply drain voltage, V
MOSFET	metal-oxide semiconductor field-effect transistor
BJT	bipolar junction transistor
IGBT	insulated-gate bipolar transistor
Si	silicon
Ec	critical electric field, V/cm
SEM	scanning electron microscope
RTF	ramp to fail
E	energy, J

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CHAPTER 1

INTRODUCTION

1.1 General Introduction

Over hundred years ago, the expectations for automobiles were only related to safe operation and durability of the devices. However, more innovative features and functions have been added due to the continual development of the design. Advances in automation and electrical engineering granted these features and driverless cars are available nowadays. The quantity of electronic units such as diodes used in electric vehicles are increasing and it can be as high as 100 electronic units or more. The evolution of electronics technology bring a better efficiency system and high power density application. (She et al. 2017).

Power discrete devices become more important in this evolution and are widely use in electrical and power electronic systems. Specifically, Power Schottky diode has gained a lot of popularity due to its special characteristics such as low forward voltage drops, low reverse current density, high breakdown voltage and low power dissipation (Liou 2013). The conceptual images of diode characteristics and its application are presented in Figure 1.1.



Figure 1.1: Conceptual images of diode characteristics and application

This chapter provides an introduction to the research entitled "Characterization Of High Voltage Power Schottky Diode Under Unclamped Inductance Switching (UIS) Avalanche Stress". This chapter is organized to seven sections which include background study, importance of this project, problem statement, objectives, research's scope and limitation, contribution and report outline.

1.1.1 Power Schottky Diode

The demand of power Schottky diode in power conversion systems is increasing as it has smaller size in design and low power loss. It is a unipolar junction. A metal-semiconductor junction (M-S Junction) diode as shown in Figure 1.2(a), where a metal such as aluminium, platinum, titanium etc. joins with N-type semiconductor (silicon) to create a Schottky barrier. The metal acts as the anode and N-type semiconductor acts as the cathode, symbol as shown in Figure 1.2(b) (Baliga 2008).



Figure 1.2: (a) Metal-semiconductor junction and (b) electronic symbol of a Schottky diode

Over the years, the performance of Power Schottky diode has been significantly improved because it is a vital component in power electronics applications. This is attributed to its special characteristics such as low forward voltage drops, low reverse current density, fast reverse recovery time and high breakdown voltage. Low voltage drops provide high switching speed and thus improve the system efficiency. System efficiency is very important in power electronic application especially at high power level as a marginal shift in efficiency can highly impact the system performance. A fast reverse recovery time diode only require a little stored charge for high speed switching application.

Power Schottky diodes are widely used in the design of power electronics' switch mode where the devices operate with maximum sustainable power during avalanche operation. Hence, the device reliability and ruggedness are the main concerns for the electronic system designers. This concern is aggravated by the insufficient understanding of breakdown in high Power Schottky diodes.

1.1.2 Unclamped Inductive Switching (UIS)

Ruggedness of a device is an important factor in the device design. Unclamped inductive switching (UIS) test is used as the circuit switching operation to evaluate the device's ruggedness, which specifies the maximum amount of avalanche energy that can be absorbed by the device prior to its catastrophic failure. Hence, avalanche test is developed to validate the device's avalanche rating. A typical unclamped inductive switching (UIS) schematic test circuit is shown in Figure 1.3.



Figure 1.3: Schematic inductive switching test circuit for a MOSFET

Device under test (DUT) is turned on when there is gate bias. After the DUT turned on, the inductor (L) began to store energy at a linear rate while the drain current (I_D) is continuously increased and being monitored. When the I_D reached the programmed setting, the gate signal is cut off and thereby immediately turns off the DUT, causing the inductor to dissipate the stored energy. But, the current cannot decay immediately as there is inductive load exists in the circuit. Thus, it resulted in high voltage forces and the device undergoes avalanche phase. The DUT remains in avalanche phase until all energy is dissipated. The voltage waveform of avalanche test is shown in Figure 1.4.



Figure 1.4: Voltage waveform of avalanche test

Avalanche operation is encountered when there is dissipation of the stored energy from the inductor within the device during off state (Kelley et al. 2017). High reverse voltages within the device generate electric fields across the junction and thus increase the velocity of electrons movement. These electrons are accelerated by the applied voltage until hitting other atoms and dislodge the electrons out of the valance band. The electron-hole pairs created thereby go through multiplication effect and lead to the increased of reverse current.

The avalanche currents are unwanted because they can damage the devices through the narrow current channels that occur either in the conducting state or blocking state in the device during avalanche test. In the UIS test, the failure mechanism of power discrete devices can categorize into two modes, active mode and passive mode. Active mode is related to the current, which is caused by the latching of the parasitic bipolar junction transistor (BJT) in the Metal Oxide Field Effect Transistor (MOSFET) (Ren et al. 2019), where the current flows through its resistance and multiplied by the gain. On the other hand, passive mode is related to the power dissipation, which is caused by external factors such as high temperature of the chip. When the temperature of the junction rises to a critical value, it will provoke the formation of hot spots, which then triggers extremely rapid device destruction.

1.2 Importance of the Study

Power Schottky diodes are widely used in electronic applications due to their special characteristics such as low switching loss, high voltage capability, and little stored charge. As the weak pellet can be sorted out easily through avalanche test, unclamped inductive switching (UIS) is an essential test to ensure the reliability of high voltage Power Schottky diode. Hence, the capability of Power Schottky diode under avalanche condition is critically important as it can provide protection for the application.

A better understanding on the characteristics of Power Schottky diode products under avalanche mode would help in determining the parameter setting for unclamped inductive switching (UIS) test. The finding of this project also would contribute to the identification of the safe operation region of the Power Schottky diode under extreme conditions.

1.3 Problem Statement

Power Schottky diode in high power conversion application causes reliability issues due to the avalanche effect. This is because Schottky diodes have the limitation of avalanche breakdown stability which caused by the avalanche current filamentation that usually occur at the interface or edge termination of the diodes.

Avalanche breakdown is a common failure mechanism of Schottky diodes during transient operation in the switching application. Therefore, the avalanche test is vital for high power devices to filter out the weak diodes. However, the degradation behaviour of Power Schottky diode under unclamped inductance switching (UIS) test are not fully understood yet and the optimum parameter setting for UIS test of a Power Schottky diode in PSMC package is not widely available.

1.4 Aims and Objectives

The objectives of this project are:

- (i) To analyse the avalanche energy performance of two different voltage class of Power Schottky Diodes at non-repetitive avalanche condition.
- (ii) To evaluate the impact of unclamped inductive switching (UIS) test operation towards forward and reverse characteristics of two different voltage class of Power Schottky diodes.
- (iii) To obtain the optimum parameter setting for unclamped inductive switching (UIS) test of two different voltage class of Power Schottky diodes.

1.5 Scope and Limitation of the Study

The scope of this project is to evaluate the avalanche ruggedness of 60 V and 100 V rated voltage of commercial Power Schottky diodes in PSMC package and to obtain their optimum parameter setting under unclamped inductive switching (UIS) test operation.

In this project, only two different voltage class of Power Schottky diodes are used and tested with a standard tester at room temperature. Thirty devices from each voltage class diode are used to perform the mortality test, where the samples are tested with different current at a pre-determined inductance until the destruction of the devices. Besides that, one sample from each device is used for stability check through repetitive test and other thirty devices are used to confirm there is no shift in term of diode performance after characteristics test. This project only involved test item analysis. Hardware setup and failure analysis are not discussed in details in this project.

1.6 Contribution of the Study

A clearer understanding on the avalanche robustness of power discrete products is crucial in order to design a better unclamped inductance switching experimental test for different voltage class of diodes. Evaluation and analysis of the characteristics and avalanche performance of the diode would help to obtain the optimum unclamped inductance switching parameter setting and hence create a more robust diode. The results of this finding would contribute to the safe operation of the power Schottky diodes under harsh conditions.

1.7 Outline of the Report

In this project, the optimum parameter setting of unclamped inductance switching test of Power Schottky diode is obtained. This thesis is structured to five chapters. Chapter 1 explains the background study, importance of this project, problem statement, objectives, scope and limitation of the research, contribution and outline of this report.

Chapter 2 gives an overview of the literature review related to the basic structure of Power Schottky diode and the operating principle of avalanche test for diodes. The failure mechanisms of power semiconductor that limit the device performance are discussed in this chapter too.

Chapter 3 is devoted to the methodology of setting up the experiment to investigate the characteristics of Power Schottky diode under unclamped inductance switching condition. Flow chart for the procedure to obtain the parameter setting is described in details.

Chapter 4 gives the detail comparison of the experimental results obtained. Analysis of the avalanche energy performance between the two different voltage class of the Schottky diodes under unclamped inductance switching test are systematically analysed.

Lastly, chapter 5 gives the achievement of this project and highlight the possible future work to be carried out.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

This chapter is organised in three sections. At the beginning of this chapter, the basic structures and characteristics of Power Schottky diodes are discussed, followed by the operating principle of the avalanche stress test experiment for power discrete products. Next, the failure mechanism of the power semiconductors that limit the reliability of the devices is discussed in details.

2.2 Basic Structure and Characteristics of Schottky Diode

Silicon (Si) Schottky diodes consist of a metal-semiconductor junction, which also known as a "Schottky barrier." There are two types of Schottky barrier, which are rectifying and non-rectifying barriers. The rectifying barrier is formed when a metal joins with the low doping level of semiconductor, while the non-rectifying barrier which also known as ohmic contact; it is formed when a metal is in close contact with high doping level N-type semiconductor (Baliga 2008). The metal-semiconductor junction makes the Schottky diode perfectly to replace the PN-junction diode. It is a majority carrier device, where the current flows due to movement of electrons. These materials distort the conduction bands by allowing the electrons to pass freely only in one direction, where the Schottky diode also acts as a unipolar device. In contrast, PN-junction diode has a structure based on a junction of P-type silicon and N-type silicon, where the current flows due to both electrons and holes. Hence, PN-junction diode acts as a bipolar device. Figure 2.1 shows the structure for Si Schottky diode and PN-junction diode.



Figure 2.1: (a) Si Schottky diode and (b) PN-junction diode

During unbiased condition, few free electrons in N-type semiconductor (cathode) move to the metal side (anode) in the Schottky diode. Movement of these electrons resulted positive ions formed at the cathode and negative ions formed at the anode. Combinations of the position and negative ions created depletion region in the diode. The diode is in forward bias when a positive terminal and negative terminal of a battery connected to anode and cathode respectively. Negative ions are formed at the anode when there is forward bias voltage supply, as shown in Figure 2.2. Contrary, the diode is in reverse bias when the battery terminal connection to diode is reversed. The width of depletion region increases when a reverse bias voltage is applied (Baliga 2008).



Figure 2.2: Forward bias diode

Si Schottky diode has low forward voltage drop and fast switching function as it has a much higher current density than PN-junction diodes. The voltage drop is affected by the resistance of the semiconductor and the Schottky barrier height. Besides that, the majority carrier conduction mechanism in Schottky diode also makes the diode to switch rapidly and results in no reverse recovery current can be formed (She et al. 2017). The fast reverse recovery characteristics of Schottky diode is its most important advantage over the PN-junction diode. This makes the Schottky diode ideal to use in the power rectification application. On the other hand, the minority carrier holes in the N-layer of PN-junction diode makes it to have higher voltage and lower resistance. The comparison between Schottky diode and PNjunction diode is summarized in Table 2.1.

Schottky Diode	PN-Junction Diode
Unipolar	Bipolar
Smaller reverse breakdown voltage	Larger reverse breakdown voltage
Depletion layer is absent	Depletion layer is present
Fast switching	Slower switching
Low voltage drop $(0.2V \sim 0.3V)$	High voltage Drop (0.6V ~ 0.7V)

Table 2.1: Comparison between Schottky diode and PN-junction diode

Figure 2.3 shows the overall I-V characteristics of Si Schottky diode and PNjunction diode. The characteristics of Schottky diode differ from PN-junction diode due to the physical properties and structures. In the forward state, Schottky diode has much lower turn on voltage compared to PN-junction diode. Majority carrier electron movement in Schottky diode results in the current flow, which flow from anode to the cathode.



Figure 2.3: I-V characteristics of a Schottky diode

The metal type used in Schottky diode is the important factor as it affects the thickness of drift layer, its barrier height, and its doping. Consequently, it also influences the electric field at the interface of Schottky diode. Figure 2.4 shows the structures of a pure Schottky diode and a Schottky diode with merged PN junction. There is a slight different in the structure of merged PN Schottky diode, which it has more P+ implantation. The electric field of merged PN Schottky diode is affected by the shielding effect that exists in P+ regions in the active area, where it changes based on the distance between the P+ areas. Shorter distance between the P+ areas are able to decrease the electrical field that exists at the rectifying interface (Treu et al. 2010).



Figure 2.4: (a) Structure of a pure Schottky diode and (b) Schottky diode with additional merged PN junction.

Metal types used in the devices design highly affect the characteristics of Schottky diode. Different metal types resulted in different features of Schottky diode. For instances, devices with titanium type feature an extremely low forward voltage, but high reverse leakage current compared to other devices. Hence, these devices are not suitable to operate at high temperature condition due to more heat is generated. These devices are suitable to use in battery-powered circuits as low conduction loss and low voltage drop. On the contrary, Schottky diodes with platinum type have extremely low I_R values and thus generate little heat. Therefore, these devices are suitable to use at high temperature condition. Table 2.2 summarizes the features and suitable application for different barrier metals of Schottky diode.

Metal Types	Forward voltage, V _F	Forward Reverse oltage, V _F current, I _R		Suitable Application
Titanium, Ti	Ultra low	High	Not suitable	Battery control
Molybdenum, Mo	Normal	Normal	Suitable	DC-DC converter
Platinum, Pt	Normal	Ultra low	Very Suitable	Automotive

Table 2.2: Features for different barrier metals of Schottky diode.

Crystal defects in the semiconductor will reduce the Schottky barrier and increase the device's temperature. The rise of internal temperature further degrades the interface of Schottky diode and thereby contribute to the device failure (Treu et al. 2010). Hence, the electric field which induces the reverse current become an important factor during device's design stage as it affects the heat dissipation within the device. A double metal structure with a tuneable barrier height can be used to adjust the forward voltage and reverse voltage to improve the power efficiency of a Schottky barrier diode. Studies by (Liou 2013) found that the reverse leakage current was reduced and the breakdown voltage was increased when the titanium-aluminium area ratio decreased.

The switching speed and leakage currents of a diode are affected by depletion width, where the depletion width is influenced by the level of doping in the diffusion layers. High concentrations of doping create a non-rectifying property, and vice versa. Additionally, the high field gradients that exist at the edge of Schottky contact generate lower breakdown voltage and thus cause premature avalanche breakdown.

Guard rings are often use in the design to obtain better performance of the diodes for high voltage application because the rings will elongate the electric field and able to improve the voltage that can absorbed by the devices. For example, in the paper of (Driche, K., Rugen, S., Kaminiski, N., Umezawa, H., Okumura, H., Gheeraert 2018), found that the electric field can be improved by the reduction of the guard ring distances. Effective isolation of main junction region with low doped guard ring region was implemented to enhance the thermal reliability by reducing the density of heat affected region (Shin et al. 2017). Besides that, oxide field-plate at the edge termination or junction termination extension (Konstantinov et al. 2018) also used to reduce the field concentration. Figure 2.5 shows a schematic view of the Schottky diode with guard ring design.



Figure 2.5: Schottky diode structure with guard ring

2.3 Avalanche Mode Operation of Diodes

2.3.1 Avalanche Mechanism

Avalanche mechanism (Infineon 2017) originates from operation above the rated reverse voltage of the device, which then induces electric fields in excess of the critical electric field (E_C). The acceleration applied to the free carriers by these strong electric fields provides the carriers with enough energy to release electron-hole pairs via impact ionization. This phenomenon cannot be controlled, potentially leading to large currents being generated and/or high temperature rise within the silicon. Ultimately, such uncontrolled events can lead to the destruction of the device or also known as avalanche breakdown. Figure 2.6 show that avalanche manifests itself through a clamping of the drain-source voltage spike.



Figure 2.6: V_{DS} waveform of (a) no facing avalanche condition and (b) under avalanche condition

2.3.2 Operation Principle of Avalanche Test

During the avalanche test, the current is applied through an inductor and the device is pulsed on for a certain period. When the energy in the inductor reaches the desired level, the switch is triggered to open, and the device is switched off. However, the current cannot cut off directly due to the inductive load. It continues to flow through the circuit, it is either flows through the blocking switch or rerouted through a lower resistances of blocking device. This depends on the type of semiconductor is under test. Figure 2.7 shows an example of an avalanche test circuit (Lillehaug 2014) of a diode. The blue circle indicated the current path when the device was switched on while the red circle was the current loop during off state and the current was forced through the device under test (DUT).



Figure 2.7: Example of avalanche current test setup

The blocking voltage increased to the device's rated reverse voltage when the device is in blocking mode. Once it exceeded the rated reverse voltage, the device undergoes avalanche mode. The avalanche voltage is then kept constant along the avalanche phase, while the current decreased linearly. The avalanche voltage drop towards its static level and the drain voltage returned to supply voltage (V_{DD}) when the device passed the avalanche test. Typical avalanche waveforms are shown in Figure 2.8.



Figure 2.8: Typical waveform of avalanche test

The avalanche current (I_{peak}) depends on both inductance value and the power time (gate switch on time). Therefore, a small inductance value or a longer power time is required to get a high avalanche current. I_{peak} calculation as below:

$$I_{peak} = \frac{V_{DD}}{L} \times Power Time$$
(2.1)

where,

 I_{peak} is the peak current in the inductor V_{DD} is the supply voltage L is the inductance value

Energy dissipation is occurred at the junction of the device during avalanche phase. The junction heated up rapidly and increased the temperature; consequently it led to the device failure. The energy dissipation of avalanche test is calculated using equation 2.2 (Lillehaug 2014).

$$E = \frac{1}{2} \times V_{BR} \times I_{peak} \times t_{avg}$$
(2.2)

where,

E = energy $V_{breakdown} = voltage \ level \ of \ DUT$ $I_{peak} = the \ initial \ peak \ current \ in \ the \ inductor$ $t_{avg} = the \ time \ that \ current \ totally \ cut \ off$

The avalanche time and energy is varied according to the inductance and peak current (Basler, T.B., Rupp, R., Gerlach, R., Zippelius, B., and Draghici 2016). When the inductance increases, the energy will increase, whereas the current will drop linearly. Examples of pellet failure patterns at different inductances (L) are shown in Figure 2.9.





Figure 2.9: Failure spot on pellet at inductance of 9 uH and 30 mH (Basler, T.B., Rupp, R., Gerlach, R., Zippelius, B., and Draghici 2016)

2.3.3 Non-Repetitive and Repetitive of Avalanche Test

There are two ratings related to avalanche event, one for non-repetitive pulse (Konstantinov et al. 2015), or also known as single event avalanche test and another one is repetitive avalanches test (Huang et al. 2012). Non-repetitive pulse avalanche is an isolated event that can potentially generate significant avalanche current. In the case of repetitive avalanche, its occurrence is characterized by a fast repetition rate and the energy per event would be much lower than for non-repetitive pulse avalanche. Both of these avalanche tests are equally important and should be tested. The inductive energy that tested in non-repetitive avalanche test must be higher than the repetitive test to determine the ruggedness of the device. The failures from both tests are expected to be similar. Besides that, removal of the heat generated between the test in the repetitive test is important because lack of heat removal could lead to overheating and result in inaccurate measurement.

The currents that carry high power densities during avalanche test usually will lead to the devices failure. The power dissipated internally in the devices corresponds to the current filaments that occur in the silicon crystal. It causes overheating and destruction of device. Details of failure mechanism are discussed in next section.

2.4 Failure Mechanism of Power Semiconductors

Power semiconductors usually experience operation under harsh conditions such as repeated stress and small irregularities which lead to fatalities. It is hard to identify the key failure mechanism when analysing the device's failure due to the failure is strongly interdependent. During avalanche test, the heat dissipated across the surface of device until the failure occurs randomly in the active area of the device. Due to this, avalanche rugged devices usually are designed to contain no single weak spot as the device destructs at higher current if the avalanche currents are shared among the cells. The common failure mechanisms under avalanche conditions are the active and passive failure modes (Kuan.W.A. & Ye.T.H. 2018).

Active mode failure arises from the device's parasitic transistor intrinsic. During avalanche operation, the impact ionization process and avalanche multiplication occur as the electric field in the diode increases rapidly and causes the diode no longer blocks the voltage. Thereby, the reverse currents flow through the p-well and associated rise in the local temperature. As a result, the voltage drops across the p-well increase and once this voltage drops exceed the parasitic BJT's turn-on voltage (0.7V); latch-up occurs and forms a hot spot. It leads to the destruction of device when overcurrent flows into the device. Figure 2.10 shows the cross-section of a MOSFET with parasitic BJT.



Figure 2.10: Cross-section of a MOSFET with parasitic BJT (Infineon 2017)

On the other hands, the passive mode failure is caused by thermal effect. The dissipation of energy in the inductor during avalanche test raises the device temperature and thus changes its breakdown voltage. As a result, larger reverse current flow through the device and increases the power dissipation. The failure caused by the avalanche effect can be observed from the burnt marks on the top pellet. The existence of these hot spots indicated there is current crowding into the device and fatally damaged the device. Figure 2.11 shows the relationship between avalanche current and test temperature for different inductor values.



Figure 2.11: Avalanche current at failure vs test temperature (Siliconix Vishay 2011)

2.4.1 Types of Short Circuit Failure

The short circuit failure leads to potential destruction of a diode as it induces uncontrolled high current in the circuit (Wu et al. 2013). The failure mechanisms are high breakdown voltage, high leakage current, snappy recovery, high power dissipation and dynamic avalanche during reverse recovery. Table 2.3 shows the types of short circuit failures.

Table 2.3: Types of short circuit failures



The leakage current of the diodes is highly dependent on the voltage or temperature. Although the leakage current of diodes is usually low, it increases dramatically when the operating voltage and temperature are above the rating parameters and results in device short circuit. The value is doubled for every tendegree Celcius rise of temperature, which may thermally destroy the device at high temperature. Besides that, the forward voltage also increases when forward current increases. This leads to the rise of the operating temperature and the high-power dissipation is then fatally destroys the device when the forward current exceeds a specified value (Wu et al. 2013).

(Dchar et al. 2016) reported that energy dissipation in the silicon carbide (SiC) Schottky diode increased quickly and it was not distributed uniformly across the surface of the device. Figure 2.12 shows the short-circuit failure that occurred on the die edge with low energy level. The initial failure spot is enlarged if many currents remained in the device after its failure and it will destroy the device permanently.



Figure 2.12: Example of the failure on the die edge of a diode (Dchar et al. 2016)

2.4.2 Thermal Runaway Failure

Thermal runaway is a phenomenon in which heat generation causes the junction temperature exceeded the maximum rating of a diode and culminating in device failure. Current filaments are the narrow current channels exist either in conducting state or the blocking state of a diode during avalanche operation, which cause the rise of temperature and create hot spot in the silicon material. The temperature due to occurrence of hot spot can lead to thermal runaways and burnout (Hurkx, G.A.M., Koper 1999).

The electric field provides sufficient energy to the thermal electrons and holes in the semiconductor junction to initiate the avalanche multiplication. The high reverse current generated in the device will speed up the dissipation of the power, which then thermally destroyed the device. (George et al. 2013) found that most failures occurred either at the inner or outer edge of the guard band and also in the active area. Heavier ions usually produce failures at the outer edge while lighter ions create failures at the inner edge. Those failures are due to the premature avalanche breakdown. Figure 2.13 shows the image of burnout over guard ring's inner edge using the scanning electron microscope (SEM). A study by (Bodeker et al. 2015) proved that modern SiC Schottky diodes are very robust against thermal runaway compared to Si PiN diode. This is due to higher temperature is required to double the amount of the leakage current in Sic Shottky diodes.



Figure 2.13: Scanning electron microscope (SEM) image of burnout over guard ring's inner edge (George et al. 2013)

CHAPTER 3

METHODOLOGY AND WORK PLAN

3.1 Introduction

Figure 3.1 shows the UIS test circuit used to validate the avalanche ruggedness of a diode in this project. Gate voltage (V_G) is supplied through the UIS module to switch on the device and the current charged linearly in the inductor. When the current reached the programmed I_D value, the switch is turned off. At this stage, the DUT avalanches until the current completely discharged. (Huang et al. 2012).



Figure 3.1: Unclamped inductance switching test circuit

The test configuration is setup as shown in the Figure 3.2. An UIS inductance box is connected to the UIS module, and the other side of the UIS module is connected to the device's test socket.



Figure 3.2: UIS test configuration setup

3.2 Software Requirement

The test program to test the device is prepared with PEditor as shown in Figure 3.3. This is the interface where the test condition can be designed. Fixed variables applied in this project are gate pulse supply (V_G), voltage source (V_{DD}) and the inductance (L). Pulse supply (V_G) used in both experiments are 12 V. For low voltage device, voltage source (V_{DD}) and the inductance (L) are set as 50 V and 300 μ H respectively. On the other hand, for high voltage device, the voltage source and inductance are set as 80 V and 1 mH respectively. All measurements are carried out in the production line temperature (25 °C). In this project, a statistical tool known as Minitab software is used to analyse the data collected. It provides a simple, effective way to statistically analyse the data.

File Name : UIS Test Program.ptf						Test Item			
Polari	ty : NPN	Discription			TestMode: Branch Date: 03/10/2019 2:14:45 P				
M#	ltem Name	Min	Max	Bias/(Compare)			Time	Fail	Pass
1	EAS								
2	EASIDT								
3	EASIHT								
4	EASILT								
5	ADD								
6	EASIDMAX								
7	VFSE								
8	DELAY								
9	EAS								
10	EASIDT								
11	EASIHT								
12	EASILT								
13	ADD								
14	EASIDMAX								

Figure 3.3: Example of the PEditor interface

3.3 Sample Requirement

Seventy pieces of samples from voltage class of 60 V and 100 V of Power Schottky diodes are used in this project. Thirty devices from each voltage class diode are tested with different current at a pre-determined inductance (mortality experiment). Besides that, one sample from each device is used for stability check through the looping test and other thirty pieces devices are used to confirm there is no shift in term of diode performance after characteristics test. The remaining nine samples are for back up purpose in case there is samples drop or damage during the experiment. Both voltage class diodes have the same pellet size and clip size.

3.4 Description of Methodology

First, a non-repetitive avalanche test by baseline ramp to fail (RTF) experiment with a pre-determined inductance value has been carried out using the UIS test circuit. The drain current (I_D) is gradually increased with a step of 1 A until the destruction of the device. The purpose of this mortality test is to determine the maximum energy that a device can withstand. The avalanche voltages on thirty samples of each device at every current step have been measured and analysed. The maximum drain current before the destruction point are also recorded. Then, the median of single drain current (I_D) below the destruction point is determined and used for the repetitive test. Avalanche energy (E) is calculated with equation below:

$$E = \frac{1}{2} \times L \times I_D^2 \times \frac{V_{DS}}{V_{DS} - V_{DD}}$$
(3.1)

where

L = inductance, mH I_D = drain current, A V_{DS} = drain-source voltage, V V_{DD} = supply voltage, V

With the new defined drain current (I_D) setting, a repetitive avalanche test is carried out by a sample from each voltage class. The sample is tested for 100 times with an interval time of 500 ms between the tests. The purpose of this looping test is to confirm the stability of the device and ensure no degradation of the good units.

After that, a full characteristics test included the unclamped inductance switching test is carried out with the new set of samples. Forward voltage and reverse voltage are compared before and after unclamped inductance switching test. With the same devices, final ramp to fail (RTF) activity is carried out with the same inductance setting to confirm if there is a shift in the diode performance. Hypothesis of this experiment is to have the similar breakdown voltage and avalanche current with the baseline ramp to fail activity's result.

The general methodology of this project is shown in flow chart:



Figure 3.4: Flow chart of the methodology

Lastly, the UIS related test parameter such as avalanche measuring time is calculated with the new defined I_D value. The parameters such as I_{DT} , I_{HT} , I_{LT} and I_{Dmax} are illustrated in Figure 3.5. I_{Dmax} is the maximum drain current supply to device under test (DUT). Due to tester capability, the drain current supply to the device under test (DUT) might slightly higher than test program setting due to overshoot of current or delay. Hence this test parameter is required as a judgment of actual drain current supply and ensures there is no tester malfunction. Equation used as shown below:

$$I_{Dmax} = I_{Dset} \times 1.1 \tag{3.2}$$

$$I_{Dmin} = I_{Dset} \times 0.9 \tag{3.3}$$

where

 I_{Dmax} = maximum drain current, A

I_{Dmin} = minimum drain current, A

 $I_{Dset} = programmed drain current, A$



Figure 3.5: Measuring time for avalanche test

 I_{DT} is the power time when there is gate voltage (V_G) supply, which began to measure after achieved 10 % of the pre-determined drain current until I_{Dmax} . I_{HT} and I_{LT} are the time measured during energy discharged. These test parameters are essential to judge whether the device under test (DUT) are in good condition during avalanche test. The formulas considering the tester tolerance rate and rising time are used to determine the avalanche time parameter. Equations (Tech n.d.) as below:

$$I_{DTmax} = I_D \times \frac{L}{V_{DD}} \times 1.1 \times 1.1 \times 2$$
(3.4)

$$I_{DTmin} = I_D \times \frac{L}{V_{DD}} \times 0.9 \times 0.9 \times 1$$
(3.5)

$$I_{HTmax} = I_D \times \frac{L}{B_{VDSS}} \times 1.1 \times 1.1 \times 0.1 \times 2 + 5us \quad (3.6)$$

$$I_{HTmin} = I_D \times \frac{L}{B_{VDSS}} \times 0.9 \times 0.9 \times 0.1 \times 0.6$$
(3.7)

$$I_{LTmax} = I_D \times \frac{L}{B_{VDSS}} \times 1.1 \times 0.8 \times 2 + 5us$$
(3.8)

$$I_{LTmin} = I_D \times \frac{L}{B_{VDSS}} \times 0.9 \times 0.7 \times 0.5 \times 0.6$$
(3.9)

where I_D , L, V_{DD} and B_{VDSS} are the drain current, inductance, drain voltage supply and breakdown voltage respectively.

CHAPTER 4

RESULTS AND DISCUSSIONS

4.1 Introduction

This chapter presents the data gathered from the experiments, the results of the statistical analysis and the interpretation of the finding. These are presented either in Histograms, scatterplots, waveforms, boxplots or tables.

4.2 Non-Repetitive Avalanche Test Result

In non-repetitive avalanche test or so called ramp to fail (RTF) activity, 30 pieces samples from both voltage class devices were tested with different current supply until destruction point to explore the impact of the current rating towards the avalanche ruggedness in the 60 V and 100 V power Schottky diodes. The current was gradually increased with a step of 1 A and the avalanche voltage was collected at each current step until the sample is destroyed. The breakdown voltages before destruction point across the sample population are plotted with Histogram as shown in Figure 4.1.



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Figure 4.1: Histogram of breakdown voltage before destruction point for (a) 60 V rated voltage device and (b) 100 V rated voltage device

From the graph in Figure 4.1(a) and (b), it shows that actual breakdown voltage is higher than the rated voltage of the devices. The mean breakdown voltage obtained for the 60 V rated voltage devices is 106.3 V whereas for 100 V rated devices, the mean breakdown voltage is 158.9 V. There is a small deviation of the breakdown voltage across the samples for each voltage class device, where the standard deviation is only around 1.1 V for both 60 V and 100 V devices. Most of the samples have a breakdown voltages around 105.5 V for the 60 V devices and 158.5 V for the 100 V devices. High reverse voltages increased the electric field across the Schottky barrier and increased the velocity of electrons movement. The thermally generated electrons and holes gain sufficient energy from the electric field and initiated avalanche multiplication.

The avalanche voltage is measured at the very beginning of the avalanche phase to avoid device self-heating. When the current supply increases, the DUT temperature rises as there is increase of power dissipation. Thus, it resulted in an increase of the avalanche voltage measured across the devices, and also amount of energy. The energy is calculated from equation below:

$$Energy = \frac{1}{2} \times L \times I_D^2 \times \frac{V_{DS}}{V_{DS} - V_{DD}}$$
(4.1)

Where L, I_D , V_{DS} and V_{DD} are the inductance value, drain current, drain-source voltage and voltage supply respectively.

Figure 4.2 shows the average avalanche voltage and energy obtained from baseline ramp to fail (RTF) activities with different current supply for the 60 V and 100 V rated devices.







Figure 4.2: Average avalanche voltage and energy vs current for (a) 60 V rated device and (b) 100 V rated device

As can be seen from Figure 4.2(a), the 60 V rated voltage samples are corrupted at an average current of 20.9 A with the maximum breakdown voltage of 108.5 V. For 100 V devices as shown in Figure 4.2(b), the samples are corrupted at an average current of 16.4 A with the maximum breakdown voltage of 159.4 V. The experimental results showed that the energy required to destroy the chip are 0.136 J and 0.290 J for the 60 V and 100 V rated devices respectively. The collapse of voltage across the sample indicated that the sample is damaged and not able to sustain its reverse voltage. The median of the drain current (I_D) are around 10 A and 8 A for both 60 V and 80 V devices respectively. These drain current values are used to perform the next activites such as looping test and full characteristics test to evaluate its effectiveness towards the device's performance.

The statistical value of avalanche voltage and current obtained from baseline ramp to fail (RTF) actitvity is summarized in Table 4.1.

Itama	60 V rated	100 V rated
nems	device	device
Mean avalanche voltage, V	106.3	158.9
Maximum avalanche voltage, V	108.5	159.4
Most frequent avalanche voltage, V	105.5	158.5
Standard deviation	1.1	1.1
Average current before destruction point, A	20.9	16.4
Median of current before destruction point, A	10.0	8.0

Table 4.1: Statistical data analysis from RTF

In order to understand the impact of different inductance used, another nonrepetitive avalanche experiment with inductance of 1 mH is carried out on the 60 V devices. With the same method, the current is gradually increased with a step of 1 A and the avalanche voltage was collected at each current step until the device destroyed. The data obtained is plotted in Figure 4.3. Results show that similar avalanche voltage are obtained for both inductance values, but with higher energy created. With the inductance of 300 uH, the maximum avalanche energy of the device was measured to be 0.124 J at 21 A before destruction occurred. However, when the inductance is changed to 1 mH, the maximum avalanche energy increases to 0.189 J at 14 A. The devices corrupted at lower current with higher inductance used due to the high energy generated causing the devices heated up rapidly.



Figure 4.3: Avalanche voltage and energy result vs current supplied for different inductance values

Oscillscope was used to collect the avalanche waveform during avalanche test to confirm the accuracy of the test data. The waveform is shown in Figure 4.4. The switch was first turned on when there is gate voltage supply and then the current was stored in the inductor. When the current reached the programmed drain current (ID), the switch was turned off by cutting off the gate voltage supply and the device undergo avalanche phase until the stored current was fully discharged.



Figure 4.4: (a) Waveform with 300 μ H inductance and (b) Waveform with 1 mH inductance. Green, yellow and blue lines denote the gate voltage, drain voltage and drain current respectively.

With the same current setting ($I_D = 10$ A), the device is switched on for a longer time with higher inductance because the inductor required longer time to store energy. Similar to avalanche phase period, higher inductance have a longer avalanche phase as it required longer time to dissipate the energy stored. However, the different inductance values don't affect the avalanche voltage of a device. As it can be seen from the results, the avalanche voltage obtained for both inductance setting is 100 V.

4.3 Repetitive Avalanche Test Result

Repetitive test is to confirm the stability of the device, where it can be represented by the total measurement variation of the same device measured over time. In this project, repetitive avalanche test of 100 times is carried out with the median current obtained from RTF activitiy. The samples were tested 100 times is to provide a more accurate result based on statistical data. An interval time of 500 ms between each test is applied to cool down the device after each test in order to avoid inaccurate measurement. The parameters setting used are summarized in Table 4.2.

Itama	60 V rated	100 V rated
Items	device	device
Gate Voltage (V _{GS}), V	12.0	12.0
Drain Voltage (V _{DD}), V	50.0	80.0
Drain Current (I _D), A	10.0	8.0
Inductance (L), mH	0.3	1.0

Table 4.2: UIS test parameter setting for repetitive pulse test

Figure 4.5 shows the avalanche waveform obtained from the oscilloscope for both of the 60 V and 100 V rated devices.







Figure 4.5: Avalanche measurement waveform of (a) 60 V rated voltage device and (b) 100 V rated voltage device. Green, yellow and blue lines denote the gate voltage, drain voltage and drain current respectively.

Measurement data obtained are plotted in Figure 4.6. The data show that both devices achieved good stability and there is no failure between the repetitive test. From the results, the device can be considered to have a rugged behavior with the UIS parameter setting.







(b)

Figure 4.6: Process capability graph of (a) 60 V and (b) 100 V rated devices

4.4 Full Characteristics Test Result

Full characteristics tests were carried out to investigate the impact of avalanche test towards static characteristics of the devices. A significant variation in device performance, such as drift of forward voltage (V_F) or reverse voltage (V_R) indicates the devices were damaged as a result of high energy dissipation induced from avalanche test.

A new set of diode samples for both voltage class i.e. 60 V and 100 V devices were used to measure the forward voltage (V_F) and reverse voltage (V_R), followed by the avalanche test. Both forward voltage and reverse voltage were measured again after avalanche test. The measurement data obtained were compared as shown in Figure 4.7 and Figure 4.8. Both types of devices exhibited negligible deviation in device performance in terms of forward voltage or reverse voltage when compared to the initial measurements.

Mean value and P-value were analysed and summarized in Table 4.3. There is no significant different (P > 0.005) in the device performance between before and after avalanche test for both of the devices. This result indicates that there is no degradation of the device, thus the Schottky diodes are robust to avalanche test.

Device type	Test item	Mean value (before UIS)	Mean value (after UIS)	P-Value
Low voltage (60 V)	V _F (mV)	455.23	455.64	0.587
	V _R (V)	74.16	74.15	0.976
High voltage (100 V)	V _F (mV)	673.39	673.78	0.360
	$V_{R}(V)$	125.23	124.95	0.078

Table 4.3: Mean and P-Value for forward voltage (V_F) and reverse voltage (V_R)



(a)



Figure 4.7: A comparison between the 60 V rated device before and after UIS for (a) forward voltage (V_F) and (b) reverse voltage (V_R)



(a)



(b)

Figure 4.8: A comparison between the 100 V rated device before and after UIS for (a) forward voltage (V_F) and (b) reverse voltage (V_R)

Using the same dataset, the energy as a function of breakdown voltage are plotted as shown in Figure 4.9. As expected, lower breakdown voltage is having higher avalanche energy.







Figure 4.9: Scatterplot of energy vs breakdown voltage for (a) 60 V and (b) 100 V rated devices.

4.5 Final Ramp to Fail Activity Test Result

The same sets of devices from full characteristics test were used to perform ramp to fail test activity again to confirm if there is no degradation of the devices after unclamped inductive switching (UIS) test. During the test, the current was gradually increased with a step of 1 A on the device under test (DUT). Only the avalanche energy and avalanche voltage before destruction point are collected. Table 4.4 shows the test result. There is no significant variation between this RTF result and baseline RTF result. This indicates, the devices are still in good condition after the UIS test.

Measurement parameter	60 V rated device		100 V rated device	
	Baseline RTF	Final RTF	Baseline RTF	Final RTF
Avalanche current, A	20.9	21.0	16.4	16.3
Mean avalanche voltage, V	106.3	106.1	158.9	158.8

Table 4.4: Avalanche current and avalanche voltage before destruction point

4.6 Unclamped Inductive Switching (UIS) Test Parameter

The optimum values for drain current (I_D) in unclamped inductive switching (UIS) test are finalized from previous experiments for both 60 V rated voltage and 100 V rated voltage devices, there are 10 A and 8 A respectively. Besides that, avalanche measuring time such as I_D , I_{DT} , I_{HT} and I_{LT} are also determined from the equations discussed in Chapter 3. The overall UIS test parameter settings are summarized in Appendix A.

CHAPTER 5

CONCLUSIONS AND RECOMMENDATIONS

5.1 Conclusions

Non-repetitive and repetitive pulse avalanche ruggedness were evaluated for 60 V and 100 V rated voltage power Schottky devices in PSMC package. An unclamped inductive switching (UIS) module was utilized in the test circuit. In non-repetitive pulse test, each device was tested with increasing avalanche current at a fixed inductance value in order to creep up to the device's failure point. Using 0.3 mH inductance in the test setup, the drain current (I_D) of a 60 V rated device was measured to be 20.9 A. This corresponds to the maximum avalanche energy of 0.124 J. On the other hand, for a 100 V rated device, the measured I_D and maximum avalanche energy are 16.4 A and 0.271 J respectively. Additionally, with inductance of 1 mH in test setup, the 60 V rated device was measured to be 0.189 J at 14 A. In the repetitive pulse avalanche test, the devices were achieved good stability with the new defined drain current setting (median of the maximum avalanche current at failure) as there is no significant variation from the measurement data.

Full characteristics test such as forward voltage and reverse voltage were measured before and after the UIS test. Comparison of these results yielded no observable degradation, where P-values exceeded 0.005 for either 60 V or 100 V rated devices. Result from the final ramp to fail avalanche tests shows that there is no shift in the device performance after unclamped inductive switching (UIS) test. Based on the characterization results, the optimum drain current and related UIS measuring test time setting for avalanche test were obtained.

5.2 **Recommendations for future work**

The main objective of this project is to obtain the optimum unclamped inductive switching (UIS) test parameters for 60 V and 100 V rated power Schottky diodes in PSMC package. Following are the recommendations of the future works:

- 1. Study on the breakdown mechanism of power Schottky diode under the avalanche test.
- 2. Optimization of the UIS tester hardware configuration to improve test performance.

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APPENDICES

APPENDIX A: UIS Parameter Setting

Items	60 V rated device	100 V rated device
Gate voltage (V _{GS}), V	12	12
Drain voltage (V _{DD}), V	50	80
Drain current (I _D), A	10	8
Inductance (L), mH	0.3	1
I _{Dmin} , A	9	7.2
I _{Dmax} , A	11	8.8
I _{DTmin} , μs	48.6	81
<i>I_{DTmax}</i> , μs	145.2	242
I _{HTmin} , μs	0.81	2.16
I _{HTmax} , μs	13.1	26
I _{LTmin} , μs	5.67	15.11
<i>I_{LTmax}</i> , μs	63.67	161.44

TableA-1: UIS Parameter Setting