DEVICE AND TRANSISTOR LEVEL CIRCUIT PERFORMANCE ANALYSIS OF NANOSCALE MOSFET

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By

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ABSTRACT

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Ooi Chek Yee

When nano-MOSFET structural dimension is downscaled to nanometer regime, quantum effects become obvious. This small channel length nano-MOSFET reduces electron transit time from source to drain. Owing to small dimension, its smaller capacitance would result lower power dissipation. When applying this nano-MOSFETs in designing resistive loaded logic gates, lower power dissipation high speed logic gates are produced. The first objective of this thesis is to prove the optimized parameters of *n*-channel nano-MOSFET formulated by Purdue University using nanoMOS software also developed by Purdue University. The nano-MOSFET parameters involved include channel length, temperature, gate contact work function, gate underlap, intrinsic channel and gate length. They are optimized by characterizing the electrical quantities such as subband energy levels, electron density profile, transmission coefficient, leakage current and threshold voltage aiming to produce low potential barrier height, unity transmission coefficient, low leakage current and small threshold voltage. The second objective is to characterize the dc and ac parameters for the logic gates designed with this optimized parameters *n*-channel nano-MOSFET by simulation using WinSpice and HSPICE simulators. The logic gates timing characteristics such as rise

time, fall time and propagation delay are evaluated by using simulators. The power dissipation reduction is observed from simulation results.

This research project has successfully achieved the objectives. The final optimized parameters of the nano-MOSFET are channel thickness of 1.5 nm, temperature of 300 K, gate contact work function of 4.188 eV, no gate underlap, gate length of 10 nm and intrinsic channel. The criteria used to justify the above device optimization are low threshold voltage of 0.20 V, ballistic efficiency of 0.96 and low leakage current of 5.312×10^{-2} μA/μm. The ac parameters mainly rise time, fall time and propagation delay of the logic circuits have been analyzed and the dc parameters analysed are V_{OH}, V_{OL}, V_{IH}, V_{IL}, V_M, V_{LS}, V_{TW},V_{NMH}, V_{NML}, V_{NSH}, V_{NSL} , V_{NIH} and V_{NIL}. The value of lower power dissipation and shorter propagation delay of logic gates achieved are in the range of microwatts (μW) and femtosecond (fs), respectively.

In future work, the similar study on the characteristics *p*-channel nano-MOSFET can be done so that it can combine with *n*-channel nano-MOSFET to design and characterize the nano-complimentary MOSFET (nano-CMOS) logic gates.

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DECLARATION

I hereby declare that the dissertation is based on my original work except for quotations and citations which have been duly acknowledged. I also declare that it has not been previously or concurrently submitted for any other degree at UTAR or other institutions.

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SUBMISSION OF THESIS

It is hereby certified that Ooi Chek Yee (ID No: ***09UED09071***) has completed this thesis entitled "Device and Transistor Level Circuit Performance Analysis of Nanoscale MOSFET" under the supervision of Dr. Lim Soo King (Supervisor) from the Department of Electrical and Electronic Engineering, Lee Kong Chian Faculty of Engineering and Science, and Dr. Chen Kah Pin (Co-Supervisor) from the Department of Mechanical and Material Engineering, Lee Kong Chian Faculty of Engineering and Science.

I understand that University will upload softcopy of my thesis in pdf format into UTAR Institutional Repository, which may be made accessible to UTAR community and public.

Yours truly,

_____
(Ooi Chek Yee)

APPROVAL SHEET

This dissertation/thesis entitled "**DEVICE AND TRANSISTOR LEVEL CIRCUIT PERFORMANCE ANALYSIS OF NANOSCALE MOSFET**" was prepared by OOI CHEK YEE and submitted as partial fulfillment of the requirements for the degree of Doctor of Philosophy in Engineering at Universiti Tunku Abdul Rahman.

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λ_e	de Broglie wavelength
h	Planck's constant
$\hbar$	reduced Planck's constant
m_e	electron mass
E	energy
n_x , n_z	quantum numbers
F_s^+ , F_d^-	electron flux
m_t	transverse electron mass
m_l	longitudinal electron mass
B	ballistic efficiency
λ	backscattering mean free path
r	backscattering coefficient
l	critical length
v_T	thermal velocity
R_{load}	load resistance
R_{on}	on-state resistance
$\frac{I_D}{W}$	drain current per micro width
k_B	Boltzmann's constant
$\mathcal{F}$	Fermi-Dirac integral
C_{ox}	oxide capacitance
V_{OH}	output high voltage
V_{OL}	output low voltage

V_{IH}	input high voltage
V_{IL}	input low voltage
V_M	midpoint voltage
V_{TW}	transition width
V_{LS}	logic swing
V_{NMH}	high noise margin
V_{NML}	low noise margin
V_{NSH}	high noise sensitivity
V_{NSL}	low noise sensitivity
V_{NIH}	high noise immunity
V_{NIL}	low noise immunity
P	power dissipation
W	width
L	length
T_{Si}	silicon channel thickness
C_G	gate capacitance
C_D	drain capacitance
C_S	source capacitance
τ_r	rise time constant
τ_f	fall time constant
t_r	rise time
t_f	fall time
s	scaling factor

CHAPTER ONE

INTRODUCTION

1.1 Overview of the Problem and Objectives

Nowadays, digital logic circuits can be designed using device technologies such as heterojunction bipolar junction transistor, modulated doped field effect transistor, nano-MOSFET etc. The digital technology grows rapidly over the last decades because of the great increases of digital logic circuits speed due to implementation of new fast speed devices and miniaturization of the device or down scaling sizes of device, advances in lithography etc. When transistors are downscaled to nanometer regime, the classical drift-diffusion transport cannot fully describe the electron transport in transistors. However, electron transport in these nano-transistors can be properly described by using quantum mechanical approach. The nano-transistor which is studied in this project is the nano-MOSFET proposed by Purdue University. The benefits of using this downscaled nano-MOSFET in designing logic circuits are reduction in power dissipation and enhancement in speed of logic circuits. Power dissipation reduction is due to reduced capacitances in nano-MOSFET whereas speed enhancement is due to shortening of time for electrons to travel from source to drain in nano-MOSFET (A. A. Ziabari, 2013; Adelmo, 2006; Aissa, 2008).

To characterize quantum parameters of the optimized design parameters of nano-MOSFET proposed by Purdue University in implementing logic circuits, nanoMOS 3.5 device simulator is used. The simulation examines the quantum effects like subband energy levels, electron density profile, transmission coefficient and electrical and physical parameters including channel length, channel thickness, gate contact work function, gate overlap, intrinsic channel, leakage current, threshold voltage and temperature of nano-MOSFET so that various nanoMOS simulation plots produce low potential barrier height, unity transmission coefficient, low leakage current and small threshold voltage parameters for obtaining an optimized nano-MOSFET. This proposed optimized parameters nano-MOSFET design is then used as the transistor to implement logic circuits. The dc and ac performance of these logic circuits is then evaluated by simulation using WinSpice and HSPICE simulation software (W. S. Cho, et al., 2014; S. Panigrahy and P. K. Sahu, 2013; R. Venugopal, 2008; R. Ramesh, et al., 2008).

The first objective of this thesis is to prove the optimized *n*-channel nano-MOSFET formulated by Purdue University using nanoMOS software also developed by Purdue University. The nano-MOSFET parameters involved included channel length, temperature, gate contact work function, gate underlap, intrinsic channel and gate length are optimized by characterizing the electrical quantities such as subband energy levels as shown in Figure 1.1, electron density profile, transmission coefficient, leakage current and threshold voltage. The aim of this optimization is to produce low potential barrier height, unity transmission coefficient, low leakage current and small

threshold voltage.

Figure 1.1 shows the subband energy profile along the channel length. The potential peak near the source region is the potential barrier height. If the fraction of backscattered electrons to source region is given by *r*, then the fraction of electrons which are transmitted to drain region is given by 1-*r*. *l* is the critical length where the potential energy of electron has been dropped by an amount equal to k_BT/q.

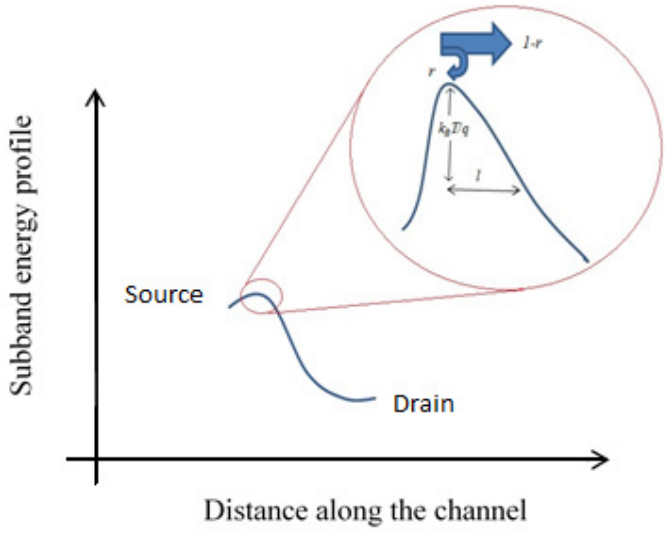

Figure 1.1: Subband energy profile of double gate (DG) nano-MOSFET

The second objective is to characterize the dc such as power dissipation and voltage transfer characteristics and ac parameters such as rise time, fall time and propagation delay for the logic gates designed with this optimized parameters *n*-channel nano-MOSFET by simulation using WinSpice and

HSPICE simulators.

1.2 Methodology

Based on structural nano-MOSFET model proposed by Purdue University, quantum effects parameters in nano-MOSFET are investigated using nanoMOS 3.5 online device simulator developed by Purdue University, USA (X. F Wang, 2010). Four quantum effects of nano-MOSFET, which are quantization of energy levels, wave nature of electron at extremely low cryogenic temperature 77 K, ballistic transport of electron flow, and electron tunnelling property are investigated. The simulation results are retrieved from simulation output and appropriate graphs are plotted to analyse these four quantum effects. Then, simulation of nano-MOSFET logic circuits is done using WinSpice and 90 nm HSPICE simulators modified to nanometer device. The transport model in WinSpice MOSFET library is modified to quantum corrected drift diffusion transport model by modifying *n*-type MOSFET dimension to width 125 nm and channel length 10 nm which has quantum effects. Logic gates studied are NOT, 2-input NOR, 2-input NAND and 3-input combinational logic with Boolean expression $\overline{x(y+z)}$. Type of logic families studies are *n*-type nano-MOSFET loaded circuit and resistive loaded circuit. In WinSpice simulation, the 733.8 Ω calculated based on simulation results resistive loaded logic circuit using *n*-type nano-MOSFET with channel length 10 nm and channel width 125 nm is used. Whereas in HSPICE with 90 nm library, the 50 kΩ resistive loaded logic gates simulated in HSPICE used *n*-channel MOSFET with channel length 100 nm and width 500 nm.

1.3 Overview of the Thesis

Chapter 2 is devoted to literature review. The research background of this thesis is described followed by electron transport models, which are drift diffusion and quantum ballistic transport using Green's function approach. The theory of nano-MOSFET device simulation is presented followed by theory of nano-MOSFET logic circuits simulation.

Chapter 3 is devoted to presentation of quantum effects simulation of nano-MOSFET. This quantum effects simulation is done using nano-MOSFET 3.5 on-line device simulator. Device parameters optimized are channel thickness, temperature, gate contact work function, gate underlap, intrinsic channel and gate length based on criteria electrical quantities such as subband energy levels, electron density profile, transmission coefficient, leakage current and threshold voltage in order to produce low potential barrier height, unity transmission coefficient, low leakage current and small threshold voltage. Then proper structural design parameters of nano-MOSFET are listed out. These optimized parameters nano-MOSFET are used in Chapter 4 to implement logic circuits.

In Chapter 4, logic circuits simulation results performed using WinSpice and HSPICE are presented separately. The logic circuits simulation results are categorized into ac parameters and dc parameters. The ac parameters studied are timing characteristics such as rise time, fall time and

propagation delay. Meanwhile, the dc parameters studied are voltage transfer characteristic and power dissipation.

Chapter 5 is the conclusions, which specified the attainment of the objectives and future work of this research.

CHAPTER TWO

LITERATURE REVIEW

2.1 Carrier Transport

Carrier transport in semiconductors has two main mechanisms, namely (i) the drift diffusion and (ii) ballistic transport. In drift diffusion transport, the mean free path λ between scattering events, or collisions is much shorter than the MOSFET device channel length (L) (A. A. Ahmadain et al., 2006; A. Domaingo and F. Schurrer, 2004; A. Rahman, et al., 2002; W. Wang, et al., 2006). On the other hand, ballistic transport occurs when the mean free path between scattering events, or collisions in much larger than the MOSFET device channel length (J. J. Liou, 1992a; J. J. Liou, 1992b; J. P. Datling, et al., 1988; K. Souissi, et al., 1993; K. Banoo and M. Lundstrom, 2000). Under this condition, scattering can be ignored completely. However, in modern practical nano-MOSFET, the carrier transport is midway between drift diffusion and ballistic regime. In this case, quasi-ballistic transport concept is used in modern practical nano-MOSFET because the channel length is smaller than mean free path between scattering events (K. Etessam-Yazdani, et al., 2006). Nowadays, modern device physicists and device engineers need to familiar with both drift diffusion and ballistic transport (E. Gnani, et al., 2008; E.

Sangiorgi, et al., 2008; F. Djeffal, et al., 2009; F. Gamiz, et al., 1998).

During downscaling of gate length of nano-MOSFET, the capacitance and resistance can hinder the performance of the nano-MOSFET. The threshold voltage of the nano-MOSFET can also be affected during gate length downscaling which can increase the off-state current. This increase in leakage current is not desirable because it will cause higher power consumption and low current drive ability. The capacitance and resistance components can be counterbalanced by increasing carrier velocity, or more precisely, enhance the virtual source velocity. There are three ways to increase the virtual source velocity, namely (i) increase ballistic velocity, (ii) increase backscattering mean free path, and (iii) decrease critical length of scattering.

2.2 Review on nanoMOS, WinSpice and HSPICE Simulator

nanoMOS 3.5 is a device on-line simulator developed by Purdue University in 2009. Structural dimension settings in nanoMOS 3.5 are in nanometer regime. Hence, quasi-ballistic transport model is modeled in nanoMOS 3.5. Device engineer can do simulation everywhere in the world when internet is available. nanoHUB webpage is the on-line simulator which includes many nanoelectronics simulation tools, ranging from materials to devices, for education and research purposes (B. Pejcinovic, 1989; G. Klimeck, et al., 2008; X. F. Wang; Z. B. Ren, 2003; X. F. Wang, 2010).

WinSpice is a free circuit simulator in Windows platform. In this

thesis, *n*-type MOSFET with LEVEL 6 MOS6 engine model is used to design the logic circuits. The width and length of the nano-MOSFET in this engine are 125 nm and 10 nm, respectively. Hence, quantum corrected drift diffusion transport model is fulfilled with WinSpice. Limitations of WinSpice are: no schematic capture, only spice coding and only works in Windows.

HSPICE is industry standard circuit simulator. In this thesis, *n*-type MOSFET with LEVEL 54 BSIM 4.0 engine model is used to design the logic circuits. The width and length of the nano-MOSFET in this engine are 500 nm and 100 nm, respectively. HSPICE can works in Windows/ Linux/UNIX environment. HSPICE needs Wave Viewer which is the waveform viewer to display timing diagrams. Limitations of HSPICE are: no schematic capture, only has spice codes.

2.3 Theory of nano-MOSFET Device

2.3.1 Electron Transport Models in nanoMOS Simulator

Electron has wave-particle dual properties (K. Talele and D. S. Patil, 2008). In quantum mechanics, electron behaves like wave whereas in classical mechanic electron acts as a particle (M. K. Ashraf, et al., 2009).

In quantum ballistic transport model, Schrödinger equation is used to solve for the quantum effects in the vertical confinement direction to obtain subband profiles. The electron transport at transmission direction in each subband is solved by Schrödinger equation using the non-equilibrium green's

function method, which includes quantum tunnelling. (A. Martinez, et al., 2007; A. Martinez, et al., 2007; A. Martinez, et al., 2009; A. T. Ramu, et al., 2007; C. J. Ni and J. Murthy, 2008a; C. J. Ni and J. Murthy, 2008b; G. Gildenblat, et al., 2009; H. Sakamoto, et al., 2008; P. Atten, et al., 2005; S. H. Jin, et al., 2008a).

In quantum corrected drift diffusion transport model, the vertical confinement is quantum mechanics treated by using Schrödinger equation to obtain subband profiles. The electron transport at transmission direction in each subband can be solved by drift diffusion model (A. Martinez, et al., 2009).

2.3.2 Quantum Effects in nano-MOSFET

Quantum effects occurred in nano-MOSFET when thickness of silicon channel is reduced to a few atomic layer sizes, which would cause splitting of energy level, ballistic transport and electron tunnelling. Since nano-MOSFET is in nanometer dimension, the de Broglie wavelength given by equation (2.1) should be in nanometer regime so that nano-MOSFET exhibits quantum effect characteristics.

$$\lambda_e = \frac{h}{\sqrt{2m_e E}} \tag{2.1}$$

where h is Planck's constant, m_e is taken as 0.98 time mass of electron, which is the unprimed subband longitudinal electron mass and E is the kinetic energy of electron.

Energy levels quantization in nano-MOSFET silicon channel is given by the equation (2.2).

$$E_{n_x,n_z} = \frac{\hbar^2\pi^2}{2m^*}\left(\left(\frac{n_x}{L_x}\right)^2 + \left(\frac{n_z}{L_z}\right)^2\right) \quad (2.2)$$

where n_x, n_z are quantum number. x and z are coordinate axis of nano-MOSFET 2D structure in Figure 2.1. When the number of energy levels increase, there will be situation where few energy levels which have the same energy value. Degenerate is the situation where states with different quantum numbers but have the same energy (G. W. Hansoon, 2008; A. Abramo, et al., 1993; A. T. Pham, et al., 2009).

When a nano-MOSFET is biased with proper drain, source and gate voltages, the simulation output of nanoMOSFET will show its subband energy profile. Electrons that are injected from source reservoir into channel region which have energy higher than the potential barrier height are totally transmitted to the drain side without reflection back to the source. This electron transport is called ballistic transport. Those electrons with energy less than the potential barrier height can tunnel through the potential barrier to other side of the subband energy. By this way, electron exhibits quantum tunnelling property.

2.3.3 Natori-Lundstrom Models of Quasi-Ballistic Transport

The energy subbands of nano-MOSFET consist of a set of unprimed and primed subbands. Natori-Lundstrom model describes electron transport in term of flux. The general expression for the electron flux F_s^+ emitted from the

source and injected into the channel is given by equation (2.3).

$$F_s^+ = \frac{(2kT)^{3/2}}{\pi^2\hbar^2}\left[\sum_i \sqrt{m_{cL}} F_{1/2}\left(\frac{E_{Fs}-E_i^L}{kT}\right) + \sum_i \sqrt{m_{cT}} F_{1/2}\left(\frac{E_{Fs}-E_i^T}{kT}\right)\right] \quad (2.3)$$

where m_{cL}=m_t= unprimed subband conductivity electron effective mass

$m_{cT} = \left(m_l^{1/2} + m_t^{1/2}\right)^2$ is primed subband conductivity electron effective mass, where m_t = transverse electron effective mass

m_l = longitudinal electron effective mass

E_i^L = unprimed subband energies

E_i^T = primed subband energies

$F_{1/2}$ = Fermi integral of order ½

E_{Fs} = energy level of the Fermi level of the source

The general expression for the electron flux F_d^- emitted from the drain and injected into the channel is basically similar to F_s^+ except that $E_{Fd} = E_{Fs} - qV_{ds}$. F_d^- is thus given by equation (2.4).

$$F_d^- = \frac{(2kT)^{3/2}}{\pi^2\hbar^2}\left[\sum_i \sqrt{m_{cL}} F_{1/2}\left(\frac{E_{Fs}-qV_{ds}-E_i^L}{kT}\right) + \sum_i \sqrt{m_{cT}} F_{1/2}\left(\frac{E_{Fs}-qV_{ds}-E_i^T}{kT}\right)\right] \quad (2.4)$$

where E_{Fd} = energy level of the Fermi level of the drain.

2.3.4 Electrical Parameters Theoretical Calculation and Capacitance Model of Nano-MOSFET

Figure 2.1 shows the nano-MOSFET structure used in nanoMOS

simulation tool (S. Hasan, et al., 2004; X. Shao and Z. P. Yu, 2005).

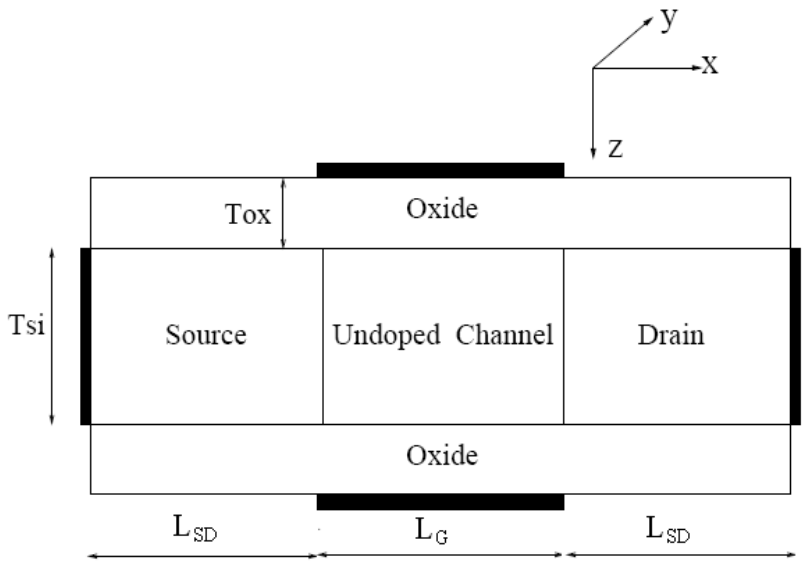

Figure 2.1: Nano-MOSFET structure used in nanoMOS simulation

The output of the simulation, which are current-voltage and subband energy profile as well as the simulation parameters of nanoMOS are used to obtain parameters such as ballistic efficiency, B, backscattering mean free path, λ, backscattering coefficient, r, critical length, l, thermal velocity, v_t, capacitances, resistance (R_{load} and $R_{channel\ at\ on\text{-}state}$) and drain current per micro width, $\frac{I_D}{W}$ (C. W. Jeong, et al., 2009; I. Pappas, et al., 2009; M. Lundstrom, 2005; M. Weidemann, et al., 2008).

The steady on-state current of nano-MOSFET is controlled by the virtual source region near the source terminal. This length of this region is called critical length, l which is equal to the distance over which the potential is lowered from the top of potential profile by an amount equal to $\beta kT/q$. β is a numerical factor ≥ 1. It is approximately equals to 1 for non-degenerate

carriers and slightly greater than 1 for degenerate carriers (V. K. Khanna, 2004). So, in this calculation β is taken as 1.1. This value is used in calculation of critical length *l* using equation (2.5).

$$l = L\left\{\frac{\beta\left(\frac{k_B T}{q}\right)}{V_{DS}}\right\}^{\alpha} \tag{2.5}$$

Since α = 0.66 is lower bound for used at diffusive transport and α = 0.75 is upper bound used at ballistic transport, α = 0.705 is used for quasi-ballistic transport (V. K. Khanna, 2004). *L* is the channel length of nano-MOSFET. V_{DS} is drain-to-source biasing voltage. kT/q is the thermal voltage.

In reality, not all scatterings can cause electrons to backscatter back into source reservoir. Only the scattering events which are determined by backscattering mean free path will cause backscattrering of electrons to source reservoir. According to (V. K. Khanna, 2004), the backscattering mean free path, λ is given by equation (2.6).

$$\lambda = \frac{2\mu}{v_T}\frac{k_B T}{q}\frac{\mathcal{F}_0(\eta_F)\mathcal{F}_0(\eta_F)}{\mathcal{F}_{-1}(\eta_F)\mathcal{F}_{1/2}(\eta_F)} \tag{2.6}$$

where electron mobility at ballistic transport in intrinsic silicon is $\mu = 1200\ cm^2/Vs$ and thermal velocity, v_T is given by equation (2.7).

$$v_T = \sqrt{\frac{2k_B T}{\pi m_t^*}} \tag{2.7}$$

where m_t^* is the transverse effective mass=0.19 time the electron mass.

By using *l* and λ, the ballistic efficiency, *B* and backscattering coefficient, *r* are defined as below according to (V. K. Khanna, 2004):

$$B = \frac{\lambda}{\lambda + 2l} \tag{2.8}$$

$$r = \frac{l}{l+\lambda} \tag{2.9}$$

In studying the theoretical part of this device, the Fermi-Dirac integrals of order zero, -1 and 1/2 are used (R. S. Kim, 2011) respectively as defined in equation (2.10) to (2.12).

$$\mathcal{F}_0(\eta_F) = \ln(1 + e^{\eta_F}) \tag{2.10}$$

$$\mathcal{F}_{-1}(\eta_F) = \frac{1}{1+e^{-\eta_F}} \tag{2.11}$$

$$\mathcal{F}_{1/2}(\eta_F) = e^{\eta_F} \tag{2.12}$$

and

$$\eta_F = \frac{\epsilon - E_i}{k_B T} \tag{2.13}$$

E_i is the energy level taken at the center of the device at channel position 0 nm and ϵ is the average energy level between source and drain.

The drain current per micron width mentioned by Lundstrom (M. Lundstrom, 2005) is defined by equation (2.14).

$$\frac{I_D}{W} = C_{ox}\widetilde{v_T}(V_{GS} - V_T)\left[\frac{1-\frac{\mathcal{F}_{1/2}\left(\eta_{F1}-\frac{qV_D}{k_BT}\right)}{\mathcal{F}_{1/2}(\eta_{F1})}}{1+\frac{\mathcal{F}_0\left(\eta_{F1}-\frac{qV_D}{k_BT}\right)}{\mathcal{F}_0(\eta_{F1})}}\right] \tag{2.14}$$

$C_{ox} = \frac{3.9\times\varepsilon_o\times 2}{T_{ox}}$ is the gate oxide capacitance per unit area for double gate device.

After considering the ballistic efficiency, B, equation (2.14) becomes

$$\frac{I_D}{W} = BC_{ox}\widetilde{v_T}(V_{GS} - V_T)\left[\frac{1-\frac{\mathcal{F}_{1/2}\left(\eta_{F1}-\frac{qV_D}{k_BT}\right)}{\mathcal{F}_{1/2}(\eta_{F1})}}{1+\frac{\mathcal{F}_0\left(\eta_{F1}-\frac{qV_D}{k_BT}\right)}{\mathcal{F}_0(\eta_{F1})}}\right] \tag{2.15}$$

and

$$\eta_{F1} = \frac{\epsilon - E_i}{k_B T} \tag{2.16}$$

E_i is the energy level taken at region around top of the barrier at channel position -5 nm and ϵ is the average energy level between source and drain.

Figure 2.2 shows the capacitance model from this citation (M. Lundstrom, 2005; M. P. Anantram, et al., 2007; B. V. Zeghbroeck, 2007).

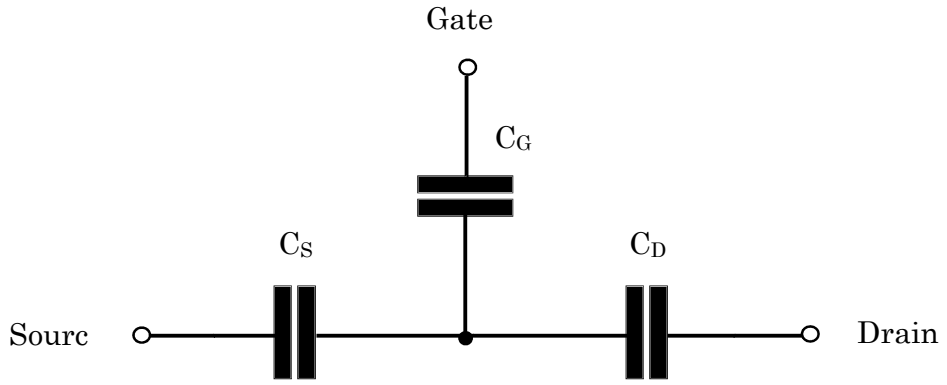

Figure 2.2: Capacitance model in nano-MOSFET device that exhibit quantum effects

Since the nano-MOSFETis a double gates device and operates at quasi-ballistic condition, its gate capacitance is defined as

Gate Capacitance $C_G = \frac{(3.9 \times \varepsilon_0 \times L \times W) \times 2}{t_{ox}}$

Capacitance per unit area = 8.6×10^{-4} F/m^2 for abrupt junctions

Area of capacitance = 8.6×10^{-4} x W x T_{Si}

Capacitance per unit length = 2.4×10^{-10} F/m for linearly graded junction.

Sidewall Capacitance = $2.4 \times 10^{-10} \times (2W \times 2T_{Si})$

The total $C_\Sigma = C_G + C_S + C_D$ = Gate Capacitance + Source Capacitance + Drain Capacitance

$$\frac{C_G}{C_\Sigma} = \frac{2.3k_BT/q}{S} \tag{2.17}$$

$$\frac{C_D}{C_\Sigma} = \frac{2.3k_BT}{q}\frac{DIBL}{S} \tag{2.18}$$

From (Z. B. Ren, 2001), subthreshold swing S=75 mV/V and drain induced barrier lowering DIBL = 80 mV/dec. So, C_G, C_S and C_D can be calculated.

2.4 Theory of nano-MOSFET Logic Gates

The logic family studied in this thesis is nano-MOSFET loaded nano-MOSFET transistor level circuit and resistive loaded nano-MOSFET transistor level circuit. The logic functions which are studied in this thesis are NOT, 2-input NOR, 2-input NAND and 3 input combinational logic with Boolean expression $\overline{x(y+z)}$. The circuit simulators used are freeware WinSpice and industrial simulator HSPICE.

2.4.1 NOT Logic Gate

Figure 2.3 shows the transistor circuit of nano-MOSFET loaded nano-MOSFET circuit for NOT logic gate. The nano-MOSFET at the top portion acts as a *n*-channel nano-MOSFET pass transistor.

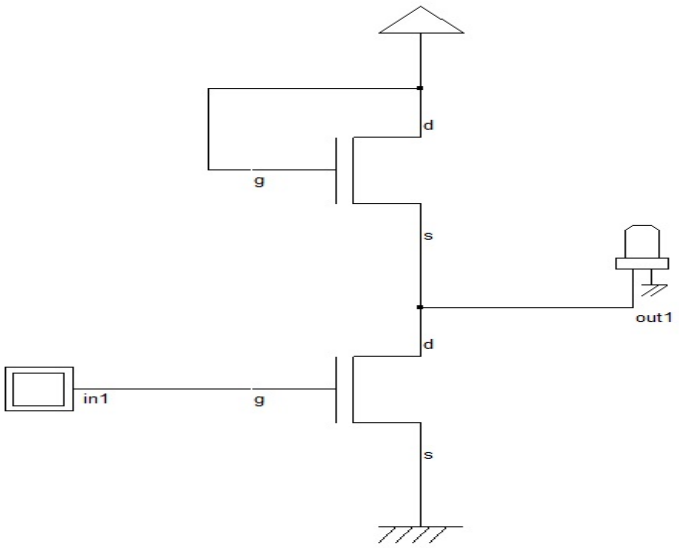

Figure 2.3: The transistor circuit of nano-MOSFET loaded nano-MOSFET circuit for NOT logic gate

2.4.1.1 ac Parameter

The theoretical timing characteristics of NOT logic gate in Figure 2.3 will be derived in this subsection. The total capacitance at the output node is calculated based on the capacitances obtained from capacitance model of nano-MOSFET in previous subsection.

The load resistance R_{Load}, on-state channel resistance, $R_{channel\ at\ on\text{-}state}$ is given as

$$R_{Load} = \left(\frac{V_{DS}}{I_{DS}}\right) = \frac{V_{th}}{I_{on-state\ at\ linear\ region} \times W} \tag{2.19}$$

since digital logic gates operate at linear portion of current-voltage (I-V) curve, $R_{channel\ at\ on\text{-}state}$ is

$$R_{channel\ at\ on-state} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{DD} - V_{th})} \tag{2.20}$$

μ_n is electron mobility at ballistic mode , which is equal to 1200 cm^2/Vs and C_{OX} = Oxide capacitance per unit area. *W*= channel width, *L*= channel length and V_{th} is the threshold voltage.

Rise time (t_f) is the time taken to charge the output from 10% of its maximum output voltage to 90% of its maximum output voltage, while fall time (t_r) is the time to discharge from 90% of its maximum output voltage to 10% of its maximum output. Note that the maximum output voltage should be equal to (V_{DD}-V_{tn}), where V_{tn} is the threshold voltage of *n*-channel nanoMSFET. The illustration of rise time and fall time are shown in Figure 2.4. The rise time and fall time are dependent on the rise time constant (τ_r) and fall time constant channel (τ_f) in which they are product of channel resistance $R_{channel\ at\ on\text{-}state}$ and the external total capacitance (C_{total}) connected to its output. Based on the definition of rise and fall times, they are equal to $2.2\tau_f$ and $2.2\tau_r$ respectively. The channel resistance $R_{channel\ at\ on\text{-}state}$ is measured from the linear region of the output characteristic of the *n*-channel nano-MOSFET. The charging involves passing a logic 1 to *n*-channel pass nano-MOSFET transistor, there is threshold loss and according to the analysis the rise time is 6.1 of the rise time for passing a logic 1 without threshold loss.

The total external capacitance comprise of the drain capacitance and resistance load source capacitance, whereby the capacitances of both drain and source are dependent on the gate contact area with drain or source (it should be twice since there are two gates) and the side wall perimeter of the drain and source structure.

Propagation delay time t_p is often used to estimate the "reaction" delay time from input to output and it is defined as $t_p = \frac{t_{nf} + t_{nr}}{2}$, where t_{nf} is the time taken for the output to fall from its maximum output voltage to 50% of its maximum output voltage. Thus, it is equal to $\tau_f \ln(2)$. t_{nr} is the time taken for the output to rise from zero volt to 50% of its maximum output voltage. It is equal to $\tau_r \ln(2)$. Based on the analysis, the propagation delay time (t_p) is equal to $t_p = 0.35(\tau_r + \tau_f)$.

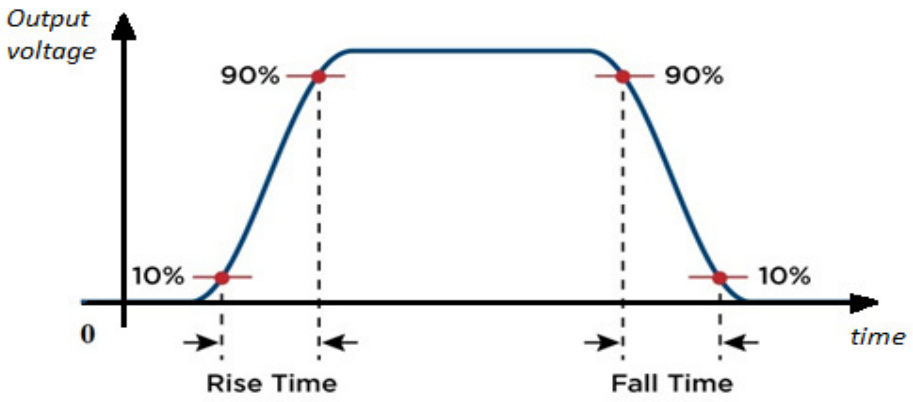

Figure 2.4: The rise time and fall time measurement

2.4.1.2 dc Parameters

In NOT logic gate study, the dc parameters involve include voltage transfer characteristic (VTC) and power dissipation (P). The ideal VTC curve for NOT logic gate is shown in Figure 2.5. In Figure 2.5, the vertical axis is the output voltage and the horizontal axis is the input voltage. V_{OH} and V_{OL} correspond to the output high state voltage level and output low state voltage level, respectively. Meanwhile, the V_{IH} and V_{IL} correspond to the input high

state voltage level and input low state voltage level, respectively.

The maximum input voltage that will produce a high output state is defined as V_{IL}. Meanwhile, the minimum input voltage that will produce a low output state in defined as V_{IH}. The critical voltages of VTC referred to V_{OH}, V_{OL}, V_{IL} and V_{IH} because these points determine the transition between logic high and low. Normally, it is useful to indicate output voltages V_{OH} and V_{OL} on the horizontal input axis because the output of NOT gate is the input to next logic gate. In order to distinguish between high voltage level and low voltage level, the following relationships must be met:$V_{OH} > V_{IH}$and $V_{OL} < V_{IL}$.

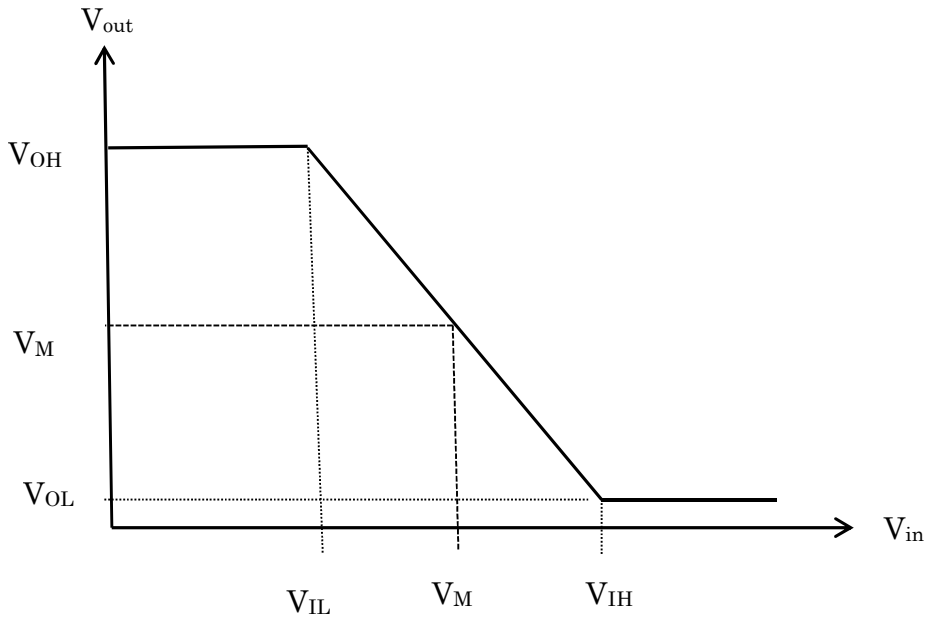

Figure 2.5: Voltage transfer characteristic (VTC) of NOT logic gate

The mid-point voltage, V_m is defined as the point on VTC where output voltage equals to input voltage. Other relevant parameters that can be obtained from VTC are: Output high voltage is V_{OH}. Output low voltage is V_{OL}; Input

high voltage is V_{IH}. Input low voltage V_{IL}; The midpoint voltage in the VTC where $V_O = V_I$ is V_M; Logic swing $V_{LS} = V_{OH} - V_{OL}$; Transition width $V_{TW} = V_{IH} - V_{IL}$; High noise margin $V_{NMH} = V_{OH} - V_{IH}$; Low noise margin $V_{NML} = V_{IL} - V_{OL}$; High noise sensitivity $V_{NSH} = V_{OH} - V_M$; Low noise sensitivity $V_{NSL} = V_M - V_{OL}$; High noise immunity $V_{NIH} = \frac{V_{NSH}}{V_{LS}}$ and Low noise immunity $V_{NIL} = \frac{V_{NSL}}{V_{LS}}$.

The power dissipation is given by:

$$P = aCfV_{DD}^2 \tag{2.21}$$

where *a* is the activity coefficient, *C* is the total capacitance at the output node, *f* is the switching frequency of the signal and V_{DD} is the supply voltage. For NOT logic gate, there are 2 possible input states (0 and 1) and there is 1 logic high output state as well as 1 logic low output state. Thus, activity coefficient is 0.25.

2.4.2 NOR Logic Gate

Figure 2.6 shows the transistor circuit of nano-MOSFET loaded nano-MOSFET circuit for 2-input NOR logic gate. The nano-MOSFET at the top portion acts as a *n*-channel nano-MOSFET pass transistor.

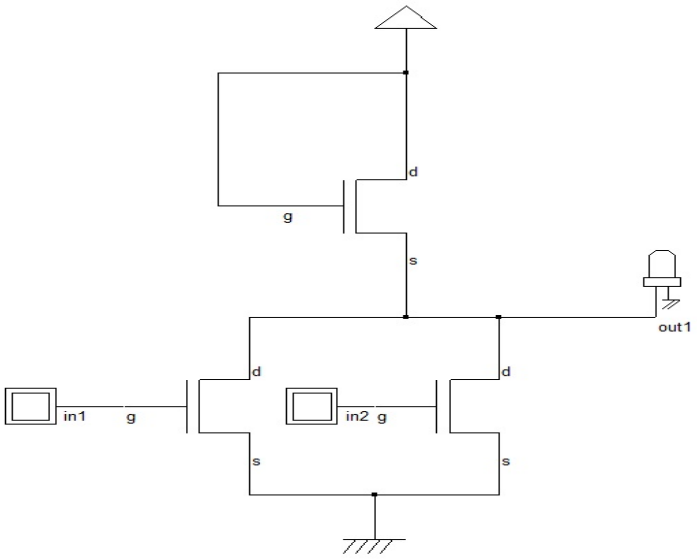

Figure 2.6: The transistor circuit of nano-MOSFET loaded nano-MOSFET circuit for 2-input NOR logic gate.

The theoretical timing characteristics of 2-input NOR logic gate in Figure 2.6 will be derived in this subsection. The total capacitance at the output node is calculated based on the capacitances obtained from capacitance model of nano-MOSFET in previous subsection.

Rise time constant (τ_r) is the product of load resistance (R_{load}) and total capacitance (C_{total}). Rise time (t_r) is equal to 2.2 x τ_r x 6.1. The factor 6.1 is caused by time duration to pass logic 1 through a *n*-MOS pass transistor. The factor 2.2 is due to 10% to 90% rising time interval. Maximum output voltage with threshold voltage loss is equal to V_{DD}-V_{tn} where V_{DD} is the power supply voltage and V_{tn} is the threshold voltage.

The total external capacitance comprise of the two parallel drain capacitances and one resistance load source capacitance, whereby the

capacitances of both drain and source are dependent on the gate contact area with drain or source (it should be twice since there are two gates) and the side wall perimeter of the drain and source structure.

The best case timing characteristic occurs when the two parallel *n*-nanoMOSFET turn on and so total on-state resistance ($R_{on\text{-}state}$) is equal to half of on-state channel resistance ($R_{channel\ at\ on\text{-}state}$). The best case fall time is 2.2 x τ_f where the factor 2.2 is due to 90% to 10% falling time interval and τ_f is the fall time constant. The worst case timing characteristic occurs when the two parallel *n*-MOS are in opposite state (one *n*-MOS turn on and the other turn off) and so total on-state resistance ($R_{on\text{-}state}$) is equal to on-state channel resistance ($R_{channel\ at\ on\text{-}state}$). The worst case fall time is 2.2 x τ_f where the factor 2.2 is due to 10% to 90% falling time interval and τ_f is the fall time constant.

Propagation delay time t_p is often used to estimate the "reaction" delay time from input to output and it is defined as $t_p = \frac{t_{nf} + t_{nr}}{2}$, where t_{nf} is the time taken for the output to fall from its maximum output voltage to 50% of its maximum output voltage. Thus, it is equal to $\tau_f \ln(2)$. t_{nr} is the time taken for the output to rise from zero volt to 50% of its maximum output voltage. It is equal to $\tau_r \ln(2)$. Based on the analysis, the propagation delay time (t_p) is equal to $t_p = 0.35(\tau_r + \tau_f)$.

The power dissipation theoretical expression is given by:

$$P = aCfV_{DD}^2 \tag{2.22}$$

where a is the activity coefficient, C is the total capacitance at the output node, f is the switching frequency of the signal and V_{DD} is the supply voltage. For 2-input NOR logic, there are 4 possible input states (00, 01, 10 and 11) and there is 1 logic high output state as well as 3 logic low output states. Thus, activity coefficient is 0.1875. During downscaling of nano-MOSFET, the power dissipation reduction is expected to be observed for 2-input NOR logic gate implemented using nano-MOSFETs as will be shown in chapter 4.

2.4.3 NAND Logic Gate

Figure 2.7 shows the transistor circuit of nano-MOSFET loaded nano-MOSFET circuit for 2-input NAND logic gate. The nano-MOSFET at the top portion acts as a *n*-channel nano-MOSFET pass transistor. The theoretical timing characteristics of 2-input NAND logic gate in Figure 2.6 will be derived in this subsection. The total capacitance at the output node is calculated based on the capacitances obtained from capacitance model of nano-MOSFET in previous subsection.

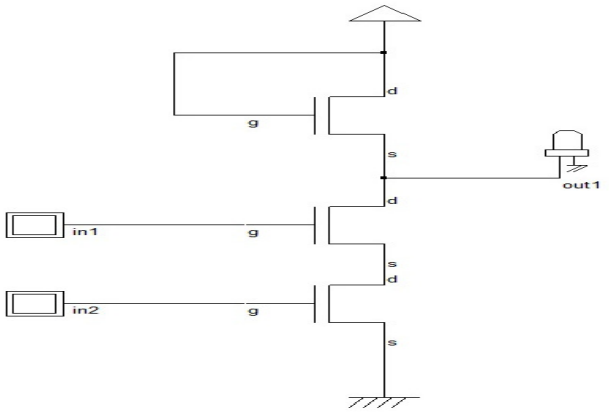

Figure 2.7: The transistor circuit of nano-MOSFET loaded nano-MOSFET circuit for 2-input NAND logic gate.

Rise time constant (τ_r) is the product of load resistance (R_{load}) and total capacitance (C_{total}). Rise time (t_r) is equal to 2.2 x τ_r x 6.1. The factor 6.1 is caused by time duration to pass logic 1 through a *n*-MOS pass transistor. The factor 2.2 is due to 10% to 90% rising time interval. Maximum output voltage with threshold voltage loss is equal to V_{DD}-V_{tn} where V_{DD} is the power supply voltage and V_{tn} is the threshold voltage.

The total external capacitance comprise of drain capacitances and resistance load source capacitance, whereby the capacitances of both drain and source are dependent on the gate contact area with drain or source, which should be twice since there are two gates and the side wall perimeter of the drain and source structure.

Since the two *n*-nanoMOSFET are connected in series, the total capacitance between these two *n*-MOS connection (C_{sd}) is equal to the sum of source capacitance and drain capacitance. Then, applying Elmore formula for two series connected *n*-MOS, the fall time constant τ_f is given by (C_{total} x $2R_{Channel\ on\text{-}state}$) + ($C_{sd}$ x $R_{Channel\ on\text{-}state}$). The fall time is 2.2 x τ_f where the factor 2.2 is due to 10% to 90% falling time interval.

Propagation delay time t_p is often used to estimate the "reaction" delay time from input to output and it is defined as $t_p = \frac{t_{nf} + t_{nr}}{2}$, where t_{nf} is the time taken for the output to fall from its maximum output voltage to 50% of its maximum output voltage. Thus, it is equal to $\tau_f \ln(2)$. t_{nr} is the time taken for the output to rise from zero volt to 50% of its maximum output voltage. It is

equal to $\tau_r \ln(2)$. Based on the analysis, the propagation delay time (t_p) is equal to $t_p = 0.35(\tau_r + \tau_f)$.

Next, the power dissipation theoretical expression is given by:

$$P = aCfV_{DD}^2 \tag{2.23}$$

where *a* is the activity coefficient, *C* is the total capacitance at the output node, *f* is the switching frequency of the signal and V_{DD} is the supply voltage. For 2-input NAND logic gate, there are 4 possible input states (00, 01, 10 and 11) and there is 3 logic high output states as well as 1 logic low output state. Thus, activity coefficient is 0.1875. During downscaling of nano-MOSFET, the power dissipation reduction is expected to be observed for 2-input NAND logic gate implemented using nano-MOSFETs as will be shown in chapter 4.

2.4.4 Combinational Logic Gate

Figure 2.7 shows the transistor circuit of nano-MOSFET loaded nano-MOSFET gate for 3-input combinational logic with Boolean expression $\overline{x(y+z)}$. The nano-MOSFET at the top portion acts as a *n*-channel nano-MOSFET pass transistor. The theoretical timing characteristics of 3-input combinational logic gate with Boolean expression $\overline{x(y+z)}$ in Figure 2.8 will be derived in this subsection. The total capacitance at the output node is calculated based on the capacitances obtained from capacitance model of nano-MOSFET in previous subsection.

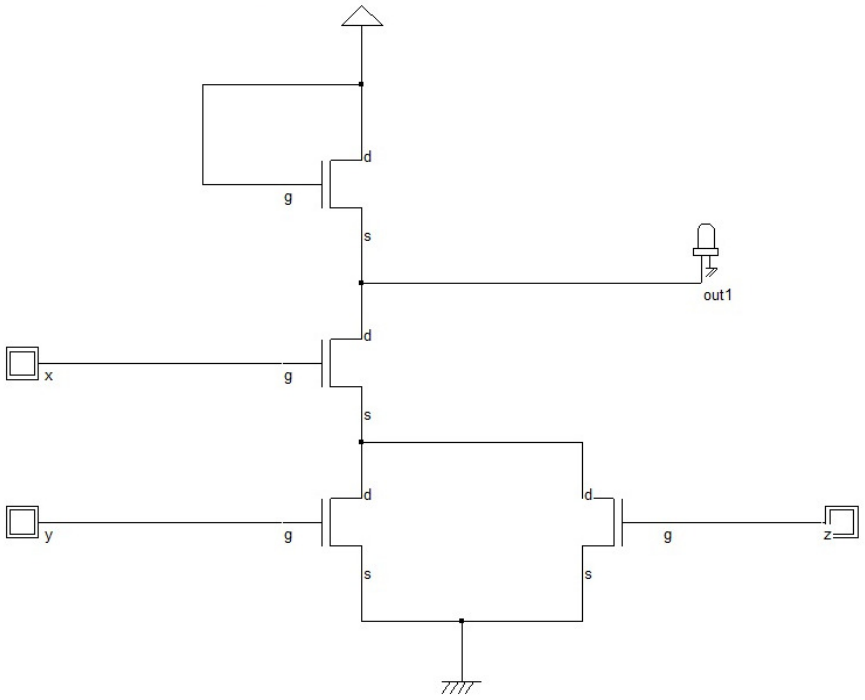

Figure 2.8: The transistor circuit of nano-MOSFET loaded nano-MOSFET circuit for 3-input combinational logic gate with Boolean expression $\overline{x(y+z)}$.

Rise time constant (τ_r) is the product of load resistance (R_{load}) and total capacitance (C_{total}). Rise time (t_r) is equal to 2.2 x τr x 6.1. The factor 6.1 is caused by time duration to pass logic 1 through a *n*-MOS pass transistor. The factor 2.2 is due to 10% to 90% rising time interval. Maximum output voltage with threshold voltage loss is equal to V_{DD}-V_{tn} where V_{DD} is the power supply voltage and V_{tn} is the threshold voltage.

The total external capacitance comprise of drain capacitances and resistance load source capacitance, whereby the capacitances of both drain and source are dependent on the gate contact area with drain or source, which should be twice since there are two gates and the side wall perimeter of the drain and source structure.

The worst case fall time t_f occurs when x *n*-nano MOSFET turn on and y *n*-nanoMOSFET or z *n*-nanoMOSFET turn on. The fall time constant τ_f is given by $4xR_{on}$ x (Drain Capacitance) + $3xR_{on}$ x (Source Capacitance). The fall time is 2.2 x τ_f where the factor 2.2 is due to 10% to 90% falling time interval.

Propagation delay time t_p is often used to estimate the "reaction" delay time from input to output and it is defined as $t_p = \frac{t_{nf} + t_{nr}}{2}$, where t_{nf} is the time taken for the output to fall from its maximum output voltage to 50% of its maximum output voltage. Thus, it is equal to $\tau_f \ln(2)$. t_{nr} is the time taken for the output to rise from zero volt to 50% of its maximum output voltage. It is equal to $\tau_r \ln(2)$. Based on the analysis, the propagation delay time (t_p) is equal to $t_p = 0.35(\tau_r + \tau_f)$.

Table 2.1 shows the truth table for this combinational logic gate.

Table 2.1: Truth table for combinational logic gate with Boolean expression $\overline{x(y+z)}$.

Inputs			Output
x	y	z	$\overline{x(y+z)}$
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

The power dissipation theoretical expression is given by:

$$P = aCfV_{DD}^2 \tag{2.24}$$

where *a* is the activity coefficient, *C* is the total capacitance at the output node, *f* is the switching frequency of the signal and V_{DD} is the supply voltage. For 3-input combinational logic gate with Boolean expression $\overline{x(y+z)}$, there are 8 possible input states (000, 001, 010, 011, 100, 101, 110 and 111) and there is 5 logic high output states as well as 3 logic low output states. Thus, activity coefficient is 0.234375. During downscaling of nano-MOSFET, the power dissipation reduction is expected to be observed for 3-input combinational logic gate with Boolean expression $\overline{x(y+z)}$ implemented using nano-MOSFETs as will be shown in next chapter.

2.4.5 Logic Gates Simulation Using HSPICE

HSPICE is industry standard logic circuit simulator. In this thesis, the logic family which is simulated using HSPICE is 50 kΩ resistive loaded MOSFET logic circuits. The type of logic gates studied includes NOT, 2-input NOR, 2-input NAND and combinational logic with Boolean expression $\overline{x(y+z)}$. Figure 2.9 to Figure 2.12 show these 4 logic gates accordingly.

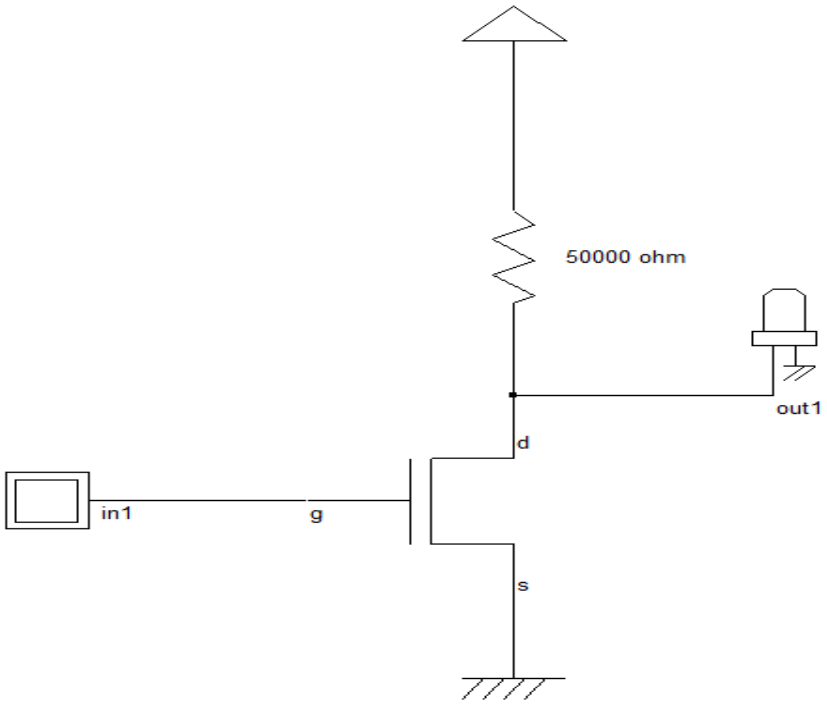

Figure 2.9: 50 kΩ resistive loaded MOSFET NOT logic gate used in HSPICE.

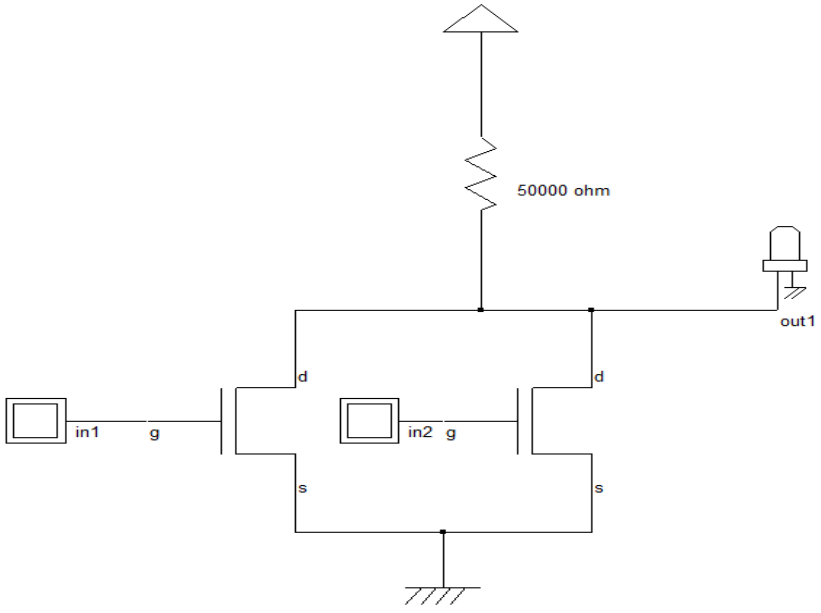

Figure 2.10: 50 kΩ resistive loaded MOSFET 2-inputs NOR logic gate used in HSPICE.

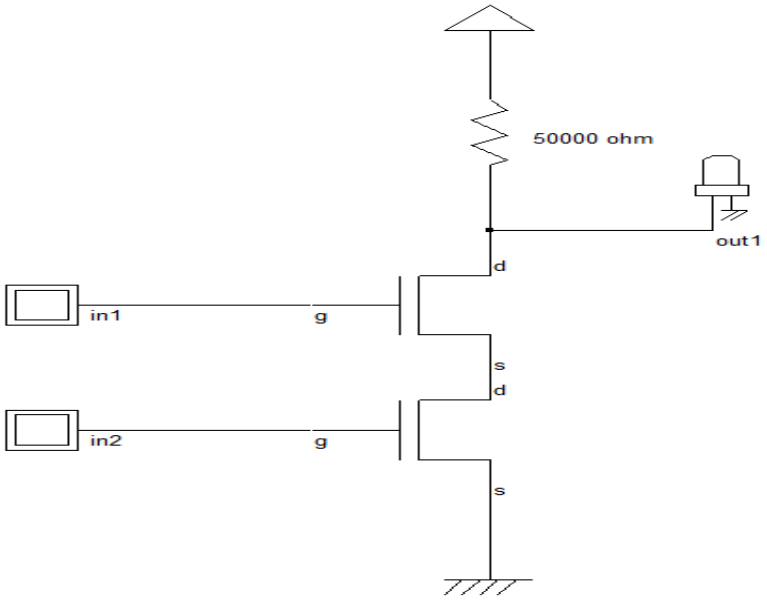

Figure 2.11: 50 kΩ resistive loaded MOSFET 2-input NAND logic gate used in HSPICE.

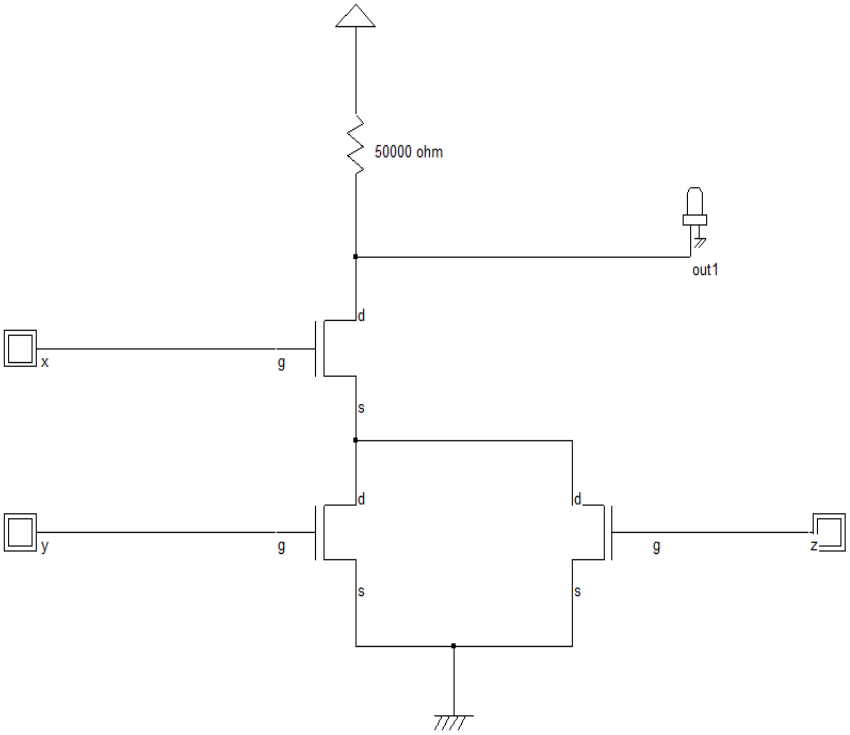

Figure 2.12: 50 kΩ resistive loaded MOSFET 3-input combinational logic gate with Boolean expression $\overline{x(y+z)}$ used in HSPICE.

The simulation output timing diagrams from HSPICE for all these four logic gates are used to obtain their timing characteristics. Rise time and fall time are measured from 10% to 90% interval and 90% to 10% interval, respectively. All the other timing characteristics are obtained from these timing diagrams according to following relationships:

- Rise time constant (τ_r) is equal to Rise time (t_r)/2.2
- Fall time constant (τ_f) is equal to Fall time (t_f)/2.2
- Propagation delay (t_p) is equal to $0.35(\tau_r + \tau_f)$
- Maximum signal frequency (f_{max}) is equal to $1/(t_r + t_f)$

CHAPTER THREE

NANO-MOSFET DEVICE SIMULATION RESULTS AND DISCUSSION

3.1 Overview of the Chapter

In this chapter, the simulation results of quantum effects like energy level quantization, wave nature of electron, electron ballistic transport, and electron quantum tunnelling of nano-MOSFET are presented. Quantum effect due to physical parameters which are thickness of silicon channel, channel length or gate contact length and gate contact work function are reported in this chapter. Quasi-ballistic transport of electron in nano-MOSFET is used to model electron flow when implementing basic logic circuit using nano-MOSFET. From the device simulation results, a set of optimized nano-MOSFET parameters are derived based on channel length, leakage current, threshold voltage, gate contact work function and no overlapping structure. Then, the optimized nano-MOSFET is used to design logic circuits; NOT gate, 2-input NOR gate, 2-input NAND gate and $\overline{x(y+z)}$ combinational circuit. Subsequently, their dc and ac parameters are extracted from simulation using free software WinSpice and commercial industrial circuit simulator HSPICE as will be described in Chapter 4.

3.2 Nano-MOSFET Device Simulation Output Result

In this section, nano-MOSFET device optimization results which are done by using nanoMOS device simulator is presented and also discussed based on theory from Chapter 2. Parameters which have been optimized by this simulation procedure included channel thickness, temperature, gate contact work function, gate underlap, intrinsic channel and gate length. The criteria used to derive the above listed optimized parameters are electrical quantities such as subband energy levels, electron density profile, transmission coefficient, leakage current and threshold voltage are analysed. Low potential energy barrier height, unity transmission coefficient, low leakage current (so that lower power dissipation can be realized) and small threshold voltage (so that nano-MOSFET switching activities are smooth) are needed in the optimized nano-MOSFET. After completing simulation and analysis, an optimum nano-MOSFET device design is proposed which will be used to design logic gates in Chapter 4.

3.2.1 Quantum Effects Simulation Result by nanoMOS

The nano-MOSFET structure shown in Figure 2.1 is used in the nanoMOS 3.5 on-line device simulator tool developed by Purdue University in 2009. A nano-MOSFET with silicon dioxide (SiO_2) dielectric is simulated in this project. In this simulation project, abrupt junctions for source/drain–substrate are considered in order to give a clear investigation on the effects of optimization. Table 3.1 shows the physical dimensions and electrical

properties of nano-MOSFET used in the simulator and designing logic circuits.

Table 3.1: The physical dimensions and electrical properties of nano-MOSFET used in quantum effects simulation and designing of logic circuits.

Double Gate nano-MOSFET Device Simulation Parameters	
V_{GS}	0.60 V
V_{DS}	0.60 V
V_{TO}	0.20 V
Source/Drain Doping Concentration (N_D)	$1x10^{20}$ cm^{-3}
Channel Body Acceptor Impurity Concentration (N_A)	$1x10^{16}$ cm^{-3}
Channel Width (W)	125 nm
Channel Length (L)	10 nm
Source Length/Drain Length (L_{SD})	7.5 nm
Silicon Channel Thickness (T_{Si})	1.5 nm
Top/Bottom Oxide Insulator Thickness (T_{OX})	1.5 nm
Top/Bottom Insulator Relative Dielectric Constant	3.9
Channel Body Relative Dielectric Constant	11.7
Top/Bottom Gate Contact Work Function	4.188 eV

Figure 3.1 shows the plot of 1st unprimed subband energy profile along the channel at equilibrium condition (zero biasing voltages) for silicon channel thickness of 1.0 nm, 1.5 nm and 2.0 nm at temperature 300 K with other parameters fixed at value as stated in Table 3.1 using electron ballistic transport using Green's function approach (H. Y. Jiang, et al., 2008; J. Fonseca and S. Kaya, 2004; W. E. Manhawy, et al., 2008). The value of channel thicknesses T_{Si} simulated are 1.0 nm, 1.5 nm and 2.0 nm. The region between -5 nm to 5 nm is the silicon intrinsic channel region that is the channel length.

The left region with negative value (from -5 nm to -12.5 nm) is the heavily doped n^+ source terminal whereas the right region with positive value (from 5 nm to 12.5 nm) is the heavily doped n^+ drain terminal. The peak of the 1st unprimed subband is located at the center of the intrinsic channel, which is at 0 nm, for all three channel thicknesses.

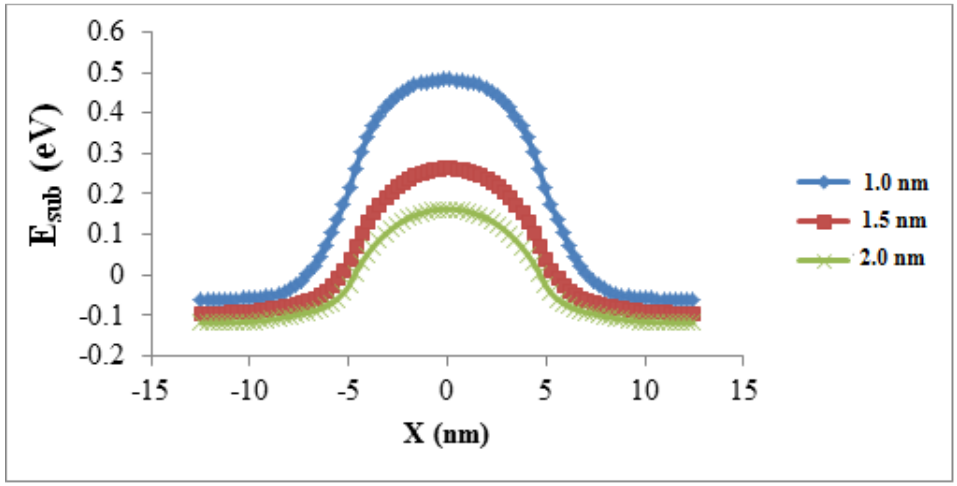

Figure 3.1: 1st unprimed subband energy along the channel at equilibrium condition for silicon channel thickness of 1.0 nm, 1.5 nm and 2.0 nm at 300 K with ballistic transport using Green's function approach.

Table 3.2 tabulated the value of 1st unprimed subband energy at the middle of the channel for three different channel thicknesses extracted from Figure 3.1. The de Broglie wavelength value, calculated using equation (2.1), indicates the quantum behaviors of the nano-MOSFET with these three values of silicon channel thicknesses. In the nanometer regime, when the structural dimension of nano-MOSFET becomes comparable to silicon lattice (0.5431 nm), the wave nature property of electron becomes obvious that the electron tunnelling property must be considered.

Table 3.2: This table shows silicon channel thickness values and their corresponding 1st unprimed subband energy as well as de Broglie wavelength.

Thickness (nm)	1st unprimed subband energy at middle of the channel (eV)	de Broglie Wavelength (nm)
1.0	0.50	1.752
1.5	0.27	2.384
2.0	0.16	3.097

With reference to equation (2.3) in Chapter 2, the equation for electron flux F_s^+ emitted from the source and injected into the channel for 2 unprimed subband and 1 primed subband is expressed as

$$F_s^+ = \frac{(2kT)^{3/2}}{\pi^2\hbar^2}\left[\left\{\sqrt{m_{cL}}\mathcal{F}_{1/2}\left(\frac{E_{Fs}-E_1^L}{kT}\right)+\sqrt{m_{cL}}\mathcal{F}_{1/2}\left(\frac{E_{Fs}-E_2^L}{kT}\right)\right\}+\sqrt{m_{cT}}\mathcal{F}_{1/2}\left(\frac{E_{Fs}-E_1^T}{kT}\right)\right] \quad (3.1)$$

where $m_{cL} = m_t$=unprimed subband conductivity electron effective mass $m_{cT} = \left(m_l^{1/2} + m_t^{1/2}\right)^2$= primed subband conductivity electron effective mass, m_t= transverse electron effective mass, m_l=longitudinal electron effective mass, $E_{1,2}^L$=1st and 2nd unprimed subband energies, E_1^T=1 primed subband energy, and $\mathcal{F}_{1/2}$=Fermi integral of order ½.

With reference to equation (2.4) in Chapter 2, the equation for electron flux F_d^- emitted from the drain and injected into the channel for 2 unprimed subband and 1 primed subband is expressed as

$$F_d^- = \frac{(2kT)^{3/2}}{\pi^2\hbar^2}\left[\left\{\sqrt{m_{cL}}\mathcal{F}_{1/2}\left(\frac{E_{Fd}-E_1^L}{kT}\right) + \sqrt{m_{cL}}\mathcal{F}_{1/2}\left(\frac{E_{Fd}-E_2^L}{kT}\right)\right\} + \sqrt{m_{cT}}\mathcal{F}_{1/2}\left(\frac{E_{Fd}-E_1^T}{kT}\right)\right] \quad (3.2)$$

Electron flux F_d^- emitted from the drain to the source has a similar expression with F_s^+ except $E_{Fd} = E_{Fs} - qV_{ds}$. Since V_{ds}=0V and V_{gs}=0V, $E_{Fd} = E_{Fs}$=energy level of the Fermi level of source and drain.

The calculated electron flux from source to drain and from drain to source are respectively equal to F_s^+= 1.648x10^{16} and F_d^-=1.648x10^{16}. They are equal because the nano-MOSFET is symmetric when no biasing voltages are applied. Electron flux from source to drain is calculated using equation (3.1), which is

$$F_s^+ = \frac{(2kT)^{3/2}}{\pi^2\hbar^2}\left[\left\{\sqrt{m_{cL}}\mathcal{F}_{1/2}\left(\frac{E_{Fs}-E_1^L}{kT}\right) + \sqrt{m_{cL}}\mathcal{F}_{1/2}\left(\frac{E_{Fs}-E_2^L}{kT}\right)\right\} + \sqrt{m_{cT}}\mathcal{F}_{1/2}\left(\frac{E_{Fs}-E_1^T}{kT}\right)\right]$$

where $\frac{(2kT)^{3/2}}{\pi^2\hbar^2} = \frac{(2\times1.38\times10^{-23}\times300)^{3/2}}{\pi^2\times(1.05\times10^{-34})^2} = 6.869\times10^{36}$;

$\mathcal{F}_{1/2}\left(\frac{E_{Fs}-E_1^L}{kT}\right) = \mathcal{F}_{1/2}\left(\frac{-0.09-0.25}{1.38\times10^{-23}\times300}\times q\right) = \mathcal{F}_{1/2}(-13.151) = e^{-13.151} = 1.942\times10^{-6}$;

$\mathcal{F}_{1/2}\left(\frac{E_{Fs}-E_2^L}{kT}\right) = \mathcal{F}_{1/2}\left(\frac{E_{Fs}-E_1^T}{kT}\right) = \mathcal{F}_{1/2}\left(\frac{0.59-0.95}{1.38\times10^{-23}\times300}\times q\right) = \mathcal{F}_{1/2}(-13.925) = e^{-13.925} = 8.959\times10^{-7}$;

$\sqrt{m_{cL}} = \sqrt{m_t} = \sqrt{0.19\times m_e} = 4.16\times10^{-16}$;

and

$\sqrt{m_{cT}} = \sqrt{\left(m_l^{1/2} + m_t^{1/2}\right)^2} = m_l^{1/2} + m_t^{1/2} = (0.98\times m_e)^{1/2} + (0.19\times m_e)^{1/2} = 1.36\times10^{-15}$.

By the same way electron flux from drain to source is calculated using equation (3.2), which is also equal to $F_d^- = 1.648 \times 10^{16}$, since the nano-MOSFET is symmetric and the nano-MOSFET is at equilibrium condition.

Figure 3.2 shows the plot of energy subbands profile along the channel for channel thickness 1.0 nm at equilibrium (no voltage biasing) condition and other parameters fixed at value as stated in Table 3.1. The subbands consist of 2 unprimed subbands (1st unprimed and 2nd unprimed) and 1 primed subband. From this plot, it is obvious that 2nd unprimed subband has the same energy value with 1st primed subband. This situation is termed degenerate where states have different quantum numbers but have the same energy value. Figure 3.3 and Figure 3.4 are the same plots but with channel thicknesses 1.5 nm and 2.0 nm respectively.

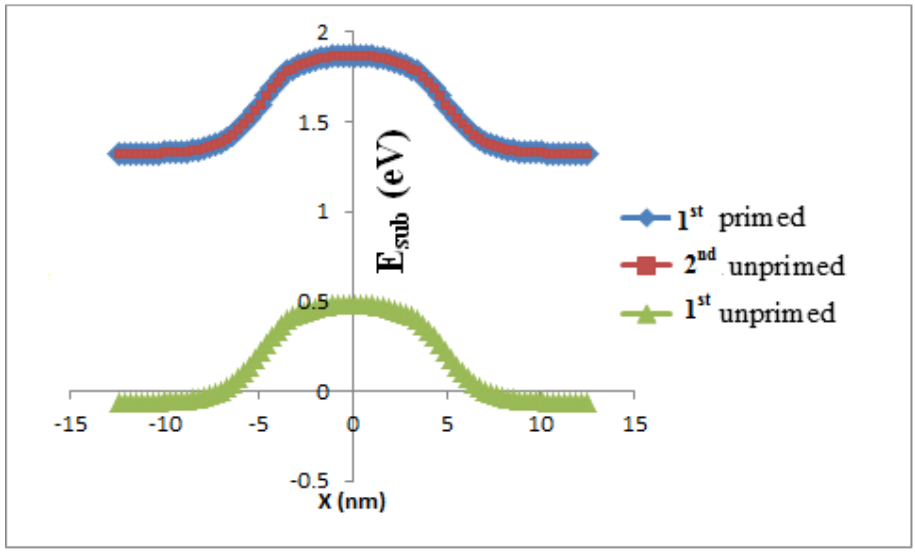

Figure 3.2: Energy subband profile along the channel for channel thickness 1.0 nm.

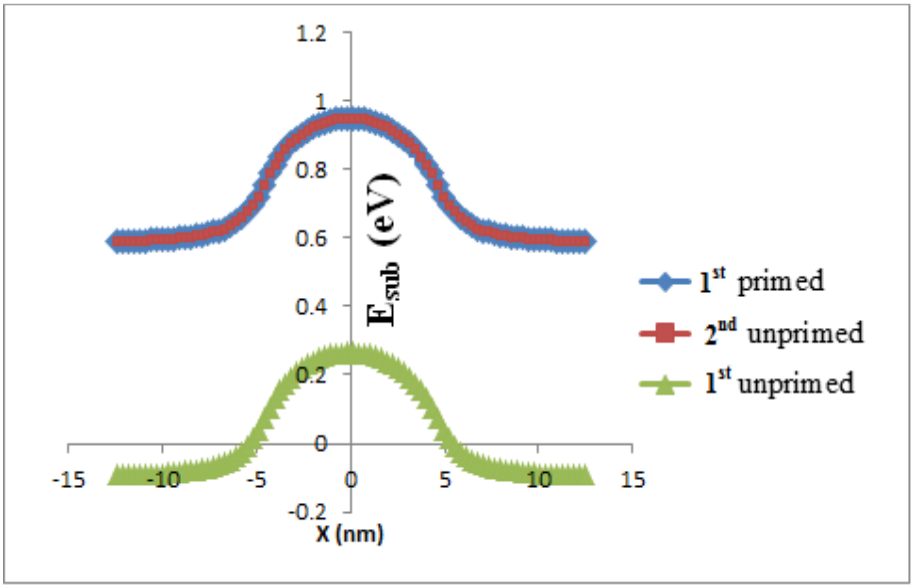

Figure 3.3: Energy subband profile along the channel for channel thickness 1.5 nm.

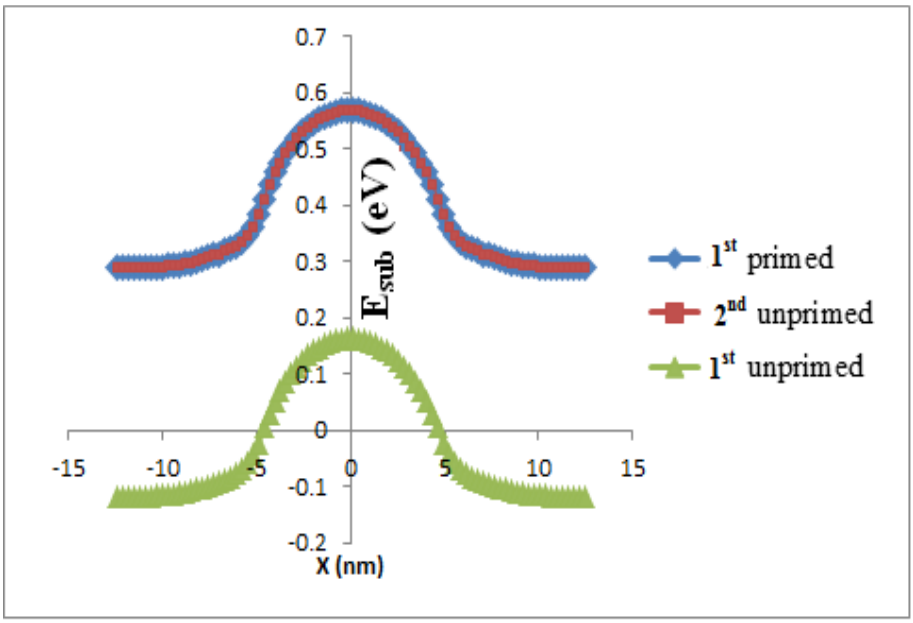

Figure 3.4: Energy subband profile along the channel for channel thickness 2.0 nm.

Based on the results shown in Figure 3.2, Figure 3.3, and Figure 3.4, the subband energy levels splitting values for the simulated thicknesses are tabulated in Table 3.3. Table 3.3 indicates that the thinner the channel thickness, the larger the energy levels splitting due to energy levels

quantization at nano-MOSFET channel. When channel thickness is thin (typically less than 2.0 nm), energy level splitting value is much larger than thermal voltage. This situation causes electrons to occupy bottom subband without jumping to higher energy levels.

Table 3.3: The table shows the silicon channel thickness values and their corresponding quantum energy levels splitting values

Thickness (nm)	**Separation between energy levels (eV)**
1.0	1.30
1.5	0.60
2.0	0.40

Table 3.4 tabulated the simulated value and theoretical calculated value of the energy subbands at channel thickness 1.5 nm and other parameters fixed at value as stated in Table 3.1. Simulated value of the energy subbands are extracted from Figure 3.2, Figure 3.3 and Figure 3.4. Meanwhile, equation (2.2) is used to calculate the theoretical value of the energy subbands. From the result shown in Table 3.4, the simulated energy values are nearly matched the theoretical calculated energy values. Figure 3.2 to 3.4 and Table 3.3 above indicate that the conceptual model of multiple subbands (equation (3.1) and (3.2)) are applicable to silicon semiconductor material with 2 dimensional cross-sectional geometry and ballistic transport (refer to Figure 2.1).

Table 3.4: This table shows the simulated and calculated energy values for three subbands energy levels at silicon channel thickness 1.5 nm.

Energy levels	simulated energy (eV)	calculated energy (eV)
1st unprimed subband	0.25	0.261
2nd unprimed subband	0.95	0.959
1st primed subband	0.95	0.899

Next, the simulation result showing the wave property of electron at nano-MOSFET is presented. The wave nature of electron in nano-MOSFET was investigated by performing 2D electron density distribution simulation at cryogenic temperature 77 K and comparing the simulated quantum model result with semiclassical results.

Figure 3.5 shows the plot of 2D electron density profile along the channel for silicon channel thicknesses of 1.0 nm, 1.5 nm and 2.0 nm at equilibrium (no biasing voltage) condition temperature 77 K with other parameters fixed at value as stated in Table 3.1 using quantum model stated in section 2.3.1, whereas Figure 3.6 shows the same plot but at temperature 300 K. Figure 3.7 shows the same plot also but at 77 K using semiclassical model. From the result of 77 K with quantum model stated in section 2.3.1, electron distribution exhibits oscillation patterns at region 5 nm to 12.5 nm at drain reservoir and -5 nm to -12.5 nm at source reservoir. These oscillation patterns indicate that electron behaves like wave at extremely low cryogenic temperature 77 K when quantum model, as stated in section 2.3.1, is used in describing electron transport (R. Clerc and G. Ghibaudo, 2013). As shown in Fig. 3.7, when semiclassical model is used to account for the electron transport

at cryogenic temperature at 77 K, no oscillation pattern is observed because electron behaves as particle in semiclassical model. At high temperature, 300 K in this simulation result, wave nature of electron disappears as there is no oscillation pattern at 300 K using quantum model. From this simulation result, electron is shown to acquire wave-particle duality property.

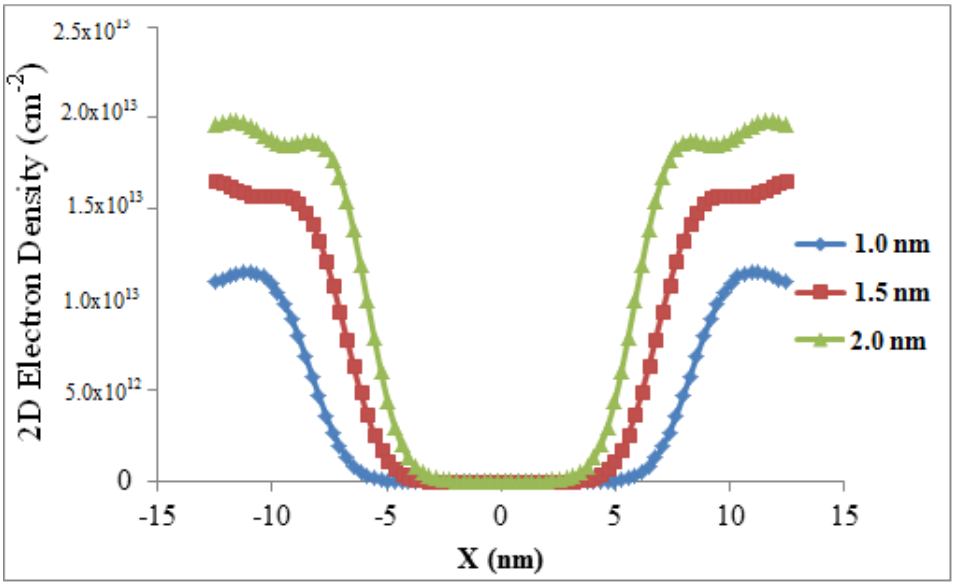

Figure 3.5: Normal plot of 2D electron density along the channel for three silicon channel thicknesses at 77 K using quantum model

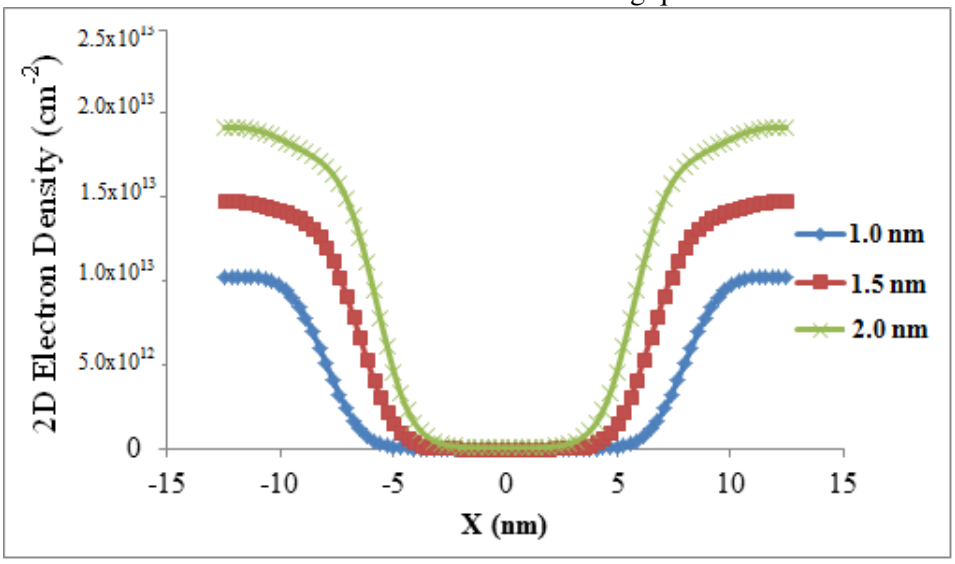

Figure 3.6: Normal plot of 2D electron density along the channel for three silicon channel thicknesses at temperature 300 K using quantum model.

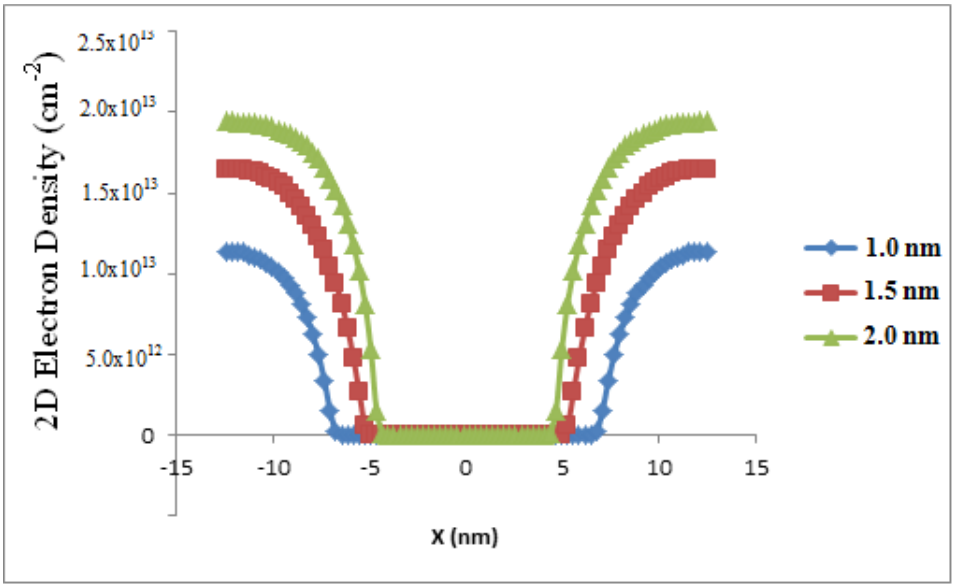

Figure 3.7: Normal plot of 2D electron density along the channel for three silicon channel thicknesses at temperature 77 K using semiclassical model.

Next, quantum tunnelling property of electron is examined. Figure 3.8 shows the plots of subband energy profile for silicon thickness 1.5 nm simulated at temperature 300K with other parameters fixed at value as stated in Table 3.1 using Green's function approach. From nano-MOSFET simulation result in Figure 3.8, there is a potential barrier in the channel of nano-MOSFET. According to quantum mechanics concept, electron is able to penetrate through this potential barrier width and this tunnelling property is prohibited classically. The simulation result shown in Figure 3.8 is carried out with zero underlap and zero overlap of gate and the source/drain junction is abrupt. Electron at the source terminal with energy lower than the peak of potential barrier height at 0 nm can tunnel through the potential barrier width to the right hand side (drain terminal). The disadvantage of this electron tunnelling is it can cause leakage current in nano-MOSFET. It is important to

suppress this leakage current in order to reduce power dissipation in logic circuits. In nano-MOSFET channel, the shape of potential barrier is controlled by gate voltage, channel thickness, channel length and gate contact work function (K. Tse and J. Robertson, 2006). Device engineers and device physicists can use underlap gate, channel length and gate contact work function to control this leakage current. The wider this potential barrier width, the lower the electron tunnelling probability will be and thereby causing less leakage current.

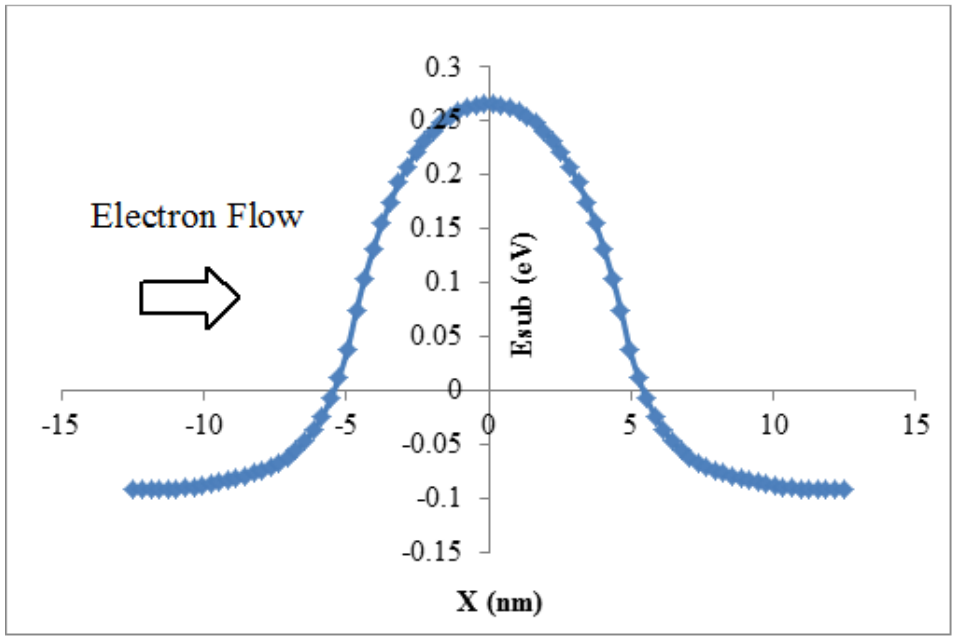

Figure 3.8: Subband energy profile along the channel at 300 K for T_{Si}=1.5 nm

Figure 3.9 shows the plot of first subband energy profile against underlapped of -7 nm, -4 nm, 0 nm and 4 nm simulated at temperature 300 K using ballistic Green's function approach. The gate voltage is 0.40 V, no source voltage biasing, drain voltage 0.001 V and other parameters fixed at value as stated in Table 3.1. In this figure, the shape of the potential barrier is

controlled by underlapped symmetric gate. Therefore, subthreshold leakage current caused by electron tunnelling can be reduced by introducing symmetric gate underlap. In Figure 3.9, underlap case is indicated by negative sign while overlap case is indicated by positive sign. Zero value means no overlap and no underlap. In Figure 3.9, there are 2 underlap results, which are -7 nm and -4 nm. There is 1 overlap case with 4 nm and 1 perfect gate alignment with 0 nm overlap. Underlap gate causes an increment in the effective channel length without affecting gate length. In large negative underlap case, wider potential barrier is observed. This leads to reducing electron quantum tunnelling. The larger the underlap, the wider the potential barrier and so the smaller the leakage current caused by quantum tunnelling. Tunnelling can be decreased and device characteristics can be enhanced by altering the shape of channel potential barrier, either by applying gate underlap or reducing channel thickness.

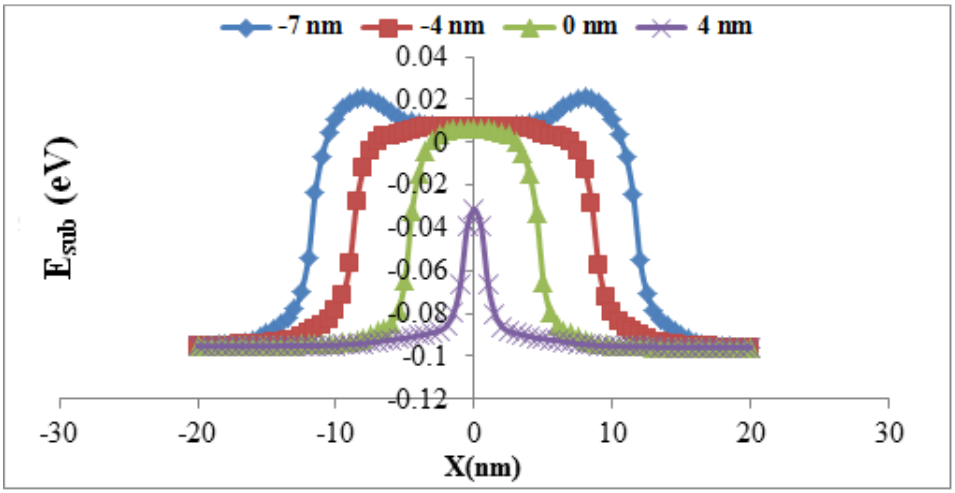

Figure 3.9: Plot of first subband energy profile against underlapped gate at temperature 300 K with ballistic Green's function.

The ballistic transport characteristic of electron in nano-MOSFET has

been investigated (K. Etessam-Yazdani, et al., 2006). Figure 3.10 shows the plot of energy versus transmission coefficient in the channel of nano-MOSFET for channel thicknesses 1.0 nm, 1.5 nm and 2.0 nm at temperature 300 K with other parameters fixed at value as stated in Table 3.1. They are 3 subbands, which are 2 unprimed and 1 primed, used in the simulation as shown in Figure 3.10. When electron acquires energy greater than the potential barrier height and is transmitted totally from source to drain without backscattering, the transmission coefficient of electron becomes 1. Transmission coefficient is a quantity determining the probability of electron transmission over a single subband. Since each subband contributes transmission coefficient from 0 to 1, the total transmission coefficient is 3 for each channel thickness 1.0 nm, 1.5 nm and 2.0 nm (M. C. Vecchi and M. Rudan, 1998). Transmission coefficient between 1 and 3 is due to same value of 2^{nd} unprimed subband and 1^{st} primed subband (P. Michetti, et al., 2009; R. Clerc, et al., 2006; S. Eminente, et al., 2005). The thickness 1.0 nm has the higher energy value because of the higher and wider potential barrier profile when compared to other two thicknesses. When ballistic transport occurs, the maximum transmission coefficient is 3 (M. K. Ashraf, et al., 2009).

From the results shown in Figure 3.10, it shows that for channel thickness 1.0 nm, electron with energy below 0.5 eV will has negligible transmission. When electron has energy above this cut-off energy, electron has good chance to transmit to drain from source. This cut-off energy is roughly corresponds to the height of potential barrier. As electron acquires more energy, electron can jump to second and third subband and thereby

transmission coefficient increases. Once the electron energy reaches the top of third subband, the transmission coefficient stop since there is no more subband for conduction.

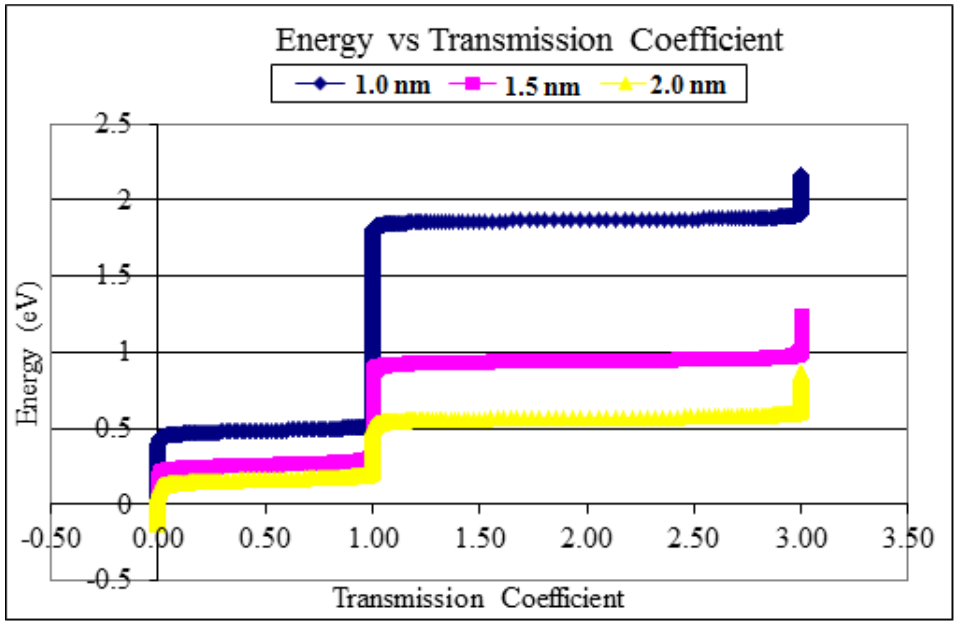

Figure 3.10: Plot of energy versus transmission coefficient in thickness T_{Si} 1.0 nm, 1.5 nm and 2.0 nm. Green's function approach is used at 300 K.

3.2.2 Simulation Results of Device Electrical Characteristic of Nano-MOSFET

In this section, electrical characteristics of nano-MOSFET is investigated, particularly the effect of channel gate length and gate contact work function.

Y. Zheng, et al., 2004 reported that the effect of dopant fluctuation in the channel of nano-MOSFET can be eliminated by using undoped nano-

MOSFETs. The dopant fluctuation effect can cause threshold voltage to vary and thereby affects the on-state current. In intrinsic channel, the threshold voltage is not sensitive to dopant fluctuation. Furthermore, undoped channel leads to carrier mobility enhancement because no depletion charges which cause electric field degrading carrier mobility (T. Khan, et al., 2005; Y. H. Dai, et al., 2006). Instead of using dopant concentration to adjust the threshold voltage, undoped nano-MOSFET must use gate contact work function to control threshold voltage. The effects of gate contact work function on device performance, which includes on-state current, leakage current, subband energy profile and electron density are examined. A high threshold voltage nano-MOSFET needs a higher voltage to switch on and thereby power consumption becomes a problem.

Figure 3.11 shows the plot of subband energy profile along the channel for gate length values 5 nm, 10 nm, 15 nm, 20 nm and 30 nm at 300 K with other parameters fixed at value as stated in Table 3.1 using Green's function approach. The biasing voltages are drain-to-source voltage V_{DS} = 0.60V and gate-to source voltage V_{GS} = 0.60V. The larger the gate length leads to wider potential barrier width and electrons are less likely to tunnel through the barrier. Moreover, electrons could not be found within the region of the potential barrier. As a result, 2D electron density plot shows a wider low electron density in channel region as indicated by Figure 3.12 with the same simulation settings as in Figure 3.11. When there is no underlap or overlap of gate, the larger the channel length, the wider the potential barrier width, the lesser the electron tunnelling resulting in smaller the leakage current as shown

in Figure 3.11 and Figure 3.13 (X. S. Jin, et al., 2008).

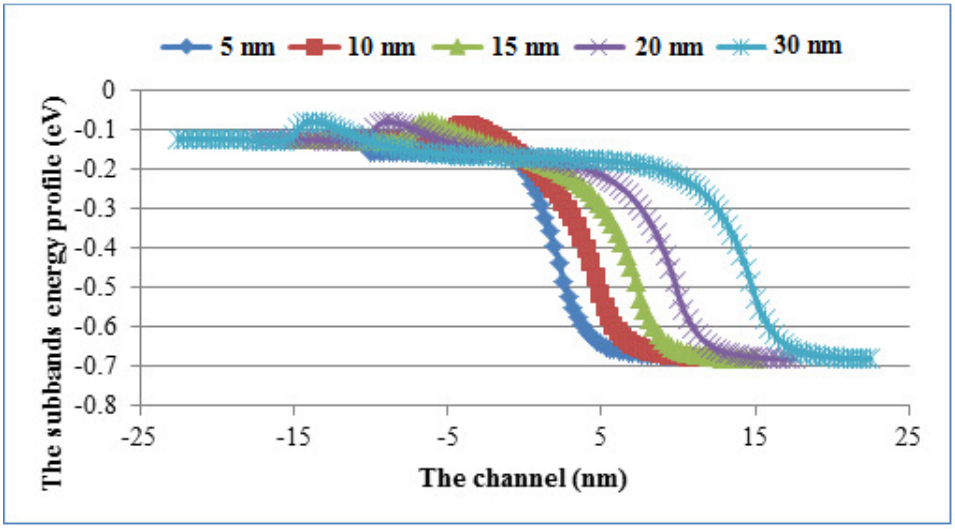

Figure 3.11: Plot of subband energy profile along the channel for gate length of 5 nm, 10 nm, 15 nm, 20 nm and 30 nm at temperature 300 K. Ballistic transport using Green's function approach is used in this simulation.

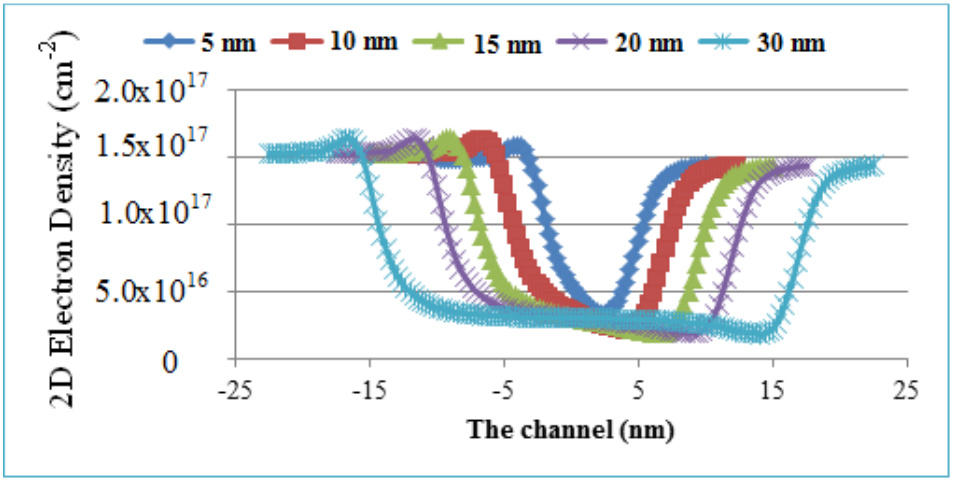

Figure 3.12: Plot of 2D electron density of the subband along the channel for gate length of 5 nm, 10 nm, 15 nm, 20 nm and 30 nm at temperature 300 K. Ballistic transport using Green's function approach is used in this simulation.

In sub-10 nm, gate length of 5 nm of nano-MOSFET device, device characteristics are affected by source-to-drain tunnelling which causes leakage

current to increase. As channel length reduces, the source and drain of the nano-MOSFET becomes closer and so the potential barrier becomes narrower. This leads to quantum tunnelling which causes subthreshold leakage current to increase. This situation is shown by Figure 3.13 and Figure 3.14 with the same simulation settings as shown in Figure 3.11 and 3.12. The leakage current is the drain current taken at V_{GS} = 0.00 V which is intercepts of vertical axis in Figure 3.13.

To evaluate the nano-MOSFET device characteristics, the on-state current, leakage current and threshold voltage are analysed by performing simulation with various channel lengths 5 nm, 10 nm, 15 nm, 20 nm and 30 nm.

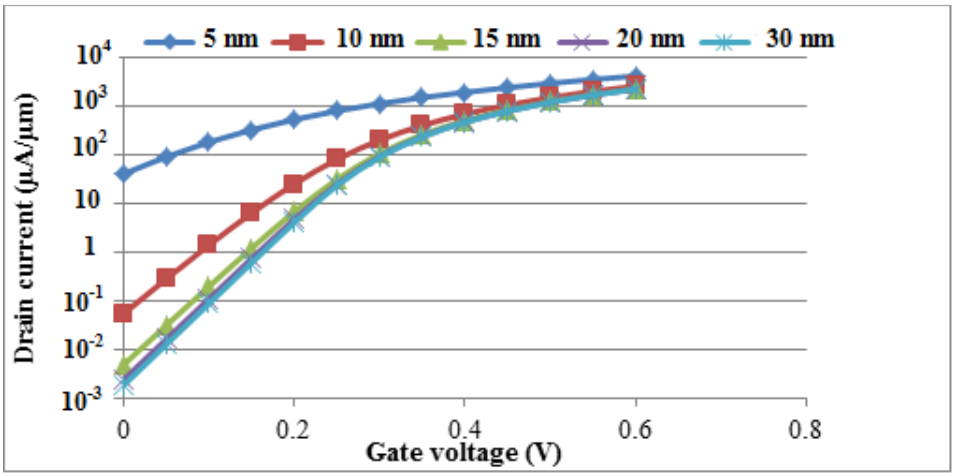

Figure 3.13: Semilog plot of drain current versus gate voltage for various combination of gate length at temperature 300 K. Ballistic transport using Green's function approach is used in this simulation.

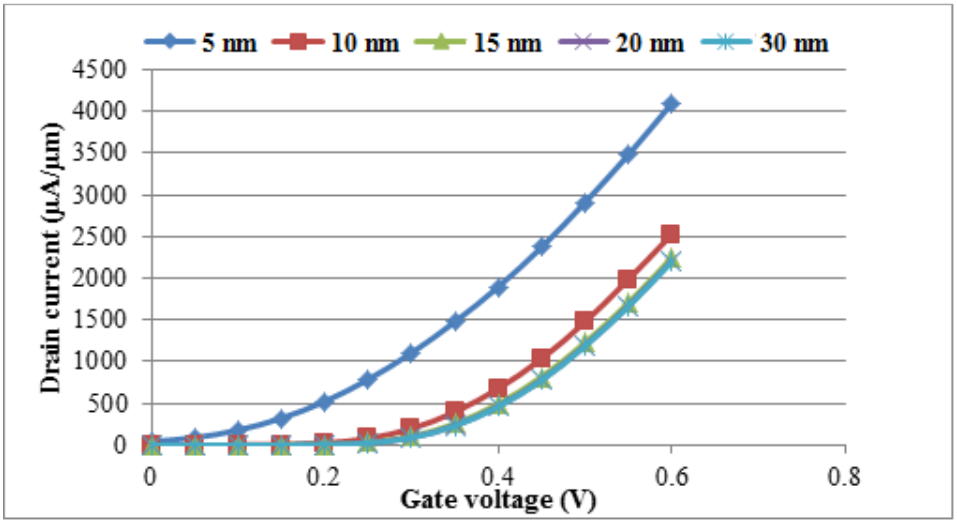

Figure 3.14: Normal plot of drain current versus gate voltage for gate length of 5 nm, 10 nm, 15 nm, 20 nm and 30 nm at temperature 300 K Ballistic transport using Green's function approach is used in this simulation.

When the channel length is reduced, this action results in shifting of current-voltage (I-V) characteristic to the left (S. L. Jang, et al, 1998). From the results shown in Figure 3.13, as the channel length becomes smaller than 15 nm, the leakage current increases dramatically. The leakage is extracted by taking drain current at $V_{GS} = 0.00$ V. The leakage currents for channel length 5 nm, 10 nm, 15 nm, 20 nm and 30 nm are 39.674 µA/µm, 5.312×10^{-2} µA/µm, 4.756×10^{-3} µA/µm, 2.331×10^{-3} µA/µm and 1.789×10^{-3} µA/µm, respectively. Since the on-state current depends on channel length, the threshold voltage of nano-MOSFET is also depends on channel length. Obviously, on-state current does not vary greatly with channel length, however leakage current varies dramatically. This leakage current is caused by quantum tunnelling for channel length less than 15 nm and is greatly channel length dependent. As channel length decreases, the threshold voltage decreases and hence the on-state current increases as indicated in Figure 3.14.

Even though threshold voltage is optimized and on-state current is satisfactory, as channel length is downscaled, nano-MOSFET device suffers a high leakage current. To suppress this high leakage current, gate contact work function is increased. Decrease in on-state current is due to increase in threshold voltage. Leakage current should be keep very low in order to lower power dissipation at off-state. Reducing the leakage current is good for producing lower power dissipation nano-MOSFET logic circuits but at the same this action increases threshold voltage which hinders fast switching of nano-MOSFET devices.

Figure 3.15 indicates the subband energy profile along the channel for different gate work functions. The values of gate work functions studied are 4.45 eV, 4.50 eV, 4.55 eV, 4.65 eV and 4.75 eV at 300 K with other parameters value fixed as stated in Table 3.1 using Green's function approach. There is a potential barrier height near the source terminal of the silicon channel. The potential barrier controls the amount of electron flowing into the channel. Its height is modulated by gate work function. When there is an increment in gate work function, the potential height is increased and so the number of electrons flowing into the channel is reduced. Therefore, the electron density decreases in the channel as shown in Figure 3.16 for gate work function 4.75 eV and other parameters value fixed at value stated in Table 3.1.

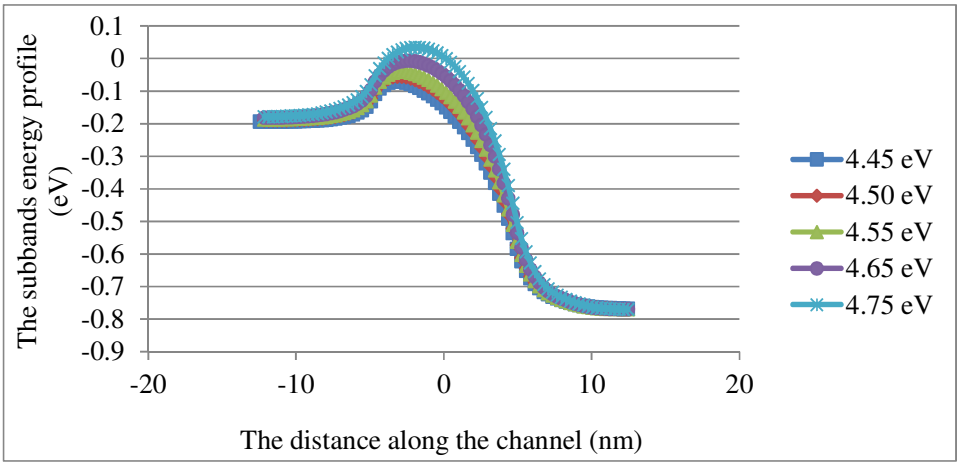

Figure 3.15: Plot of subband energy profile versus distance along the channel for different combination of top and bottom gate contact work function.

With an increment in gate contact work function, the potential barrier height is increased and so on-state current is reduced as shown in Figure 3.15 and Figure 3.17. Figure 3.17 simulation settings are the same as simulation settings in Figure 3.15. For an intrinsic (undoped) channel, the gate contact work function is used to control the height of potential barrier. By this method, gate contact work function can be used to control threshold voltage.

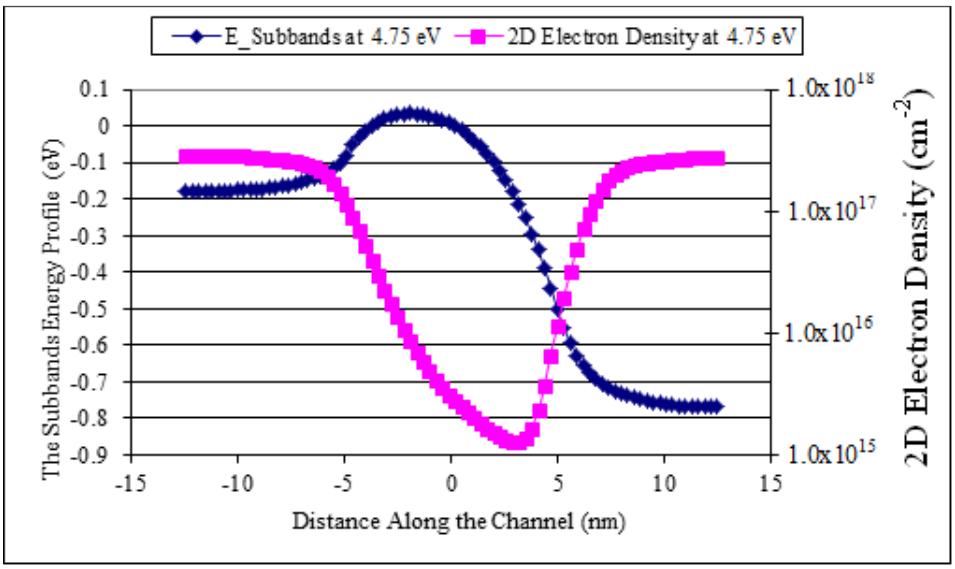

Figure 3.16: Plot of subband energy profile and 2D electron density against distance along the channel at work function 4.75 eV.

When the channel length and the gate contact work function become larger, so does the threshold voltage as shown in Figure 3.14 and Figure 3.17 (T. Khan, et al., 2005). This increment in threshold voltage hinders the performance of nano-MOSFET device in term of switching speed because larger voltage is needed to switch on the nano-MOSFETs in logic circuits. This problem violates the aim of achieving high speed nano-MOSFET logic circuits. The usage of channel length and gate contact work function to control the threshold voltage is better than using doped channel to control threshold voltage because dopants cause fluctuations in threshold voltage and also reduce carrier mobility. Therefore, intrinsic (undoped) silicon channel is used in conjunction with channel length and gate contact work function in order to optimize the threshold voltage (Y. T. Lee, et al., 2000).

From the results shown in Figure 3.18, the leakage current for gate contact work function values of 4.45 eV, 4.50 eV, 4.55 eV, 4.65 eV and 4.75 eV are 1.351×10^{-1} μA/μm, 3.432×10^{-2} μA/μm, 8.490×10^{-3} μA/μm, 4.910×10^{-4} μA/μm and 2.680×10^{-5} μA/μm, respectively. Note that the simulation settings in Figure 3.18 are the same as the settings in Figure 3.15 and Figure 3.17. Figure 3.18 shows the subthreshold characteristic with current at logarithmic scale. Steeper slope at subthreshold region is obvious for high gate contact work function and decreasing slope at subthreshold region is obvious for small gate contact work function. As the gate contact work function increases, the leakage current becomes smaller. Consequently, the leakage current rises drastically with smaller gate contact work function due to high electron quantum tunnelling at the potential barrier height. When gate contact work

function is small, from Figure 3.15 it shows that the potential barrier height is low and the potential barrier's width is smaller. This situation causes electron to tunnel through the potential barrier more easily.

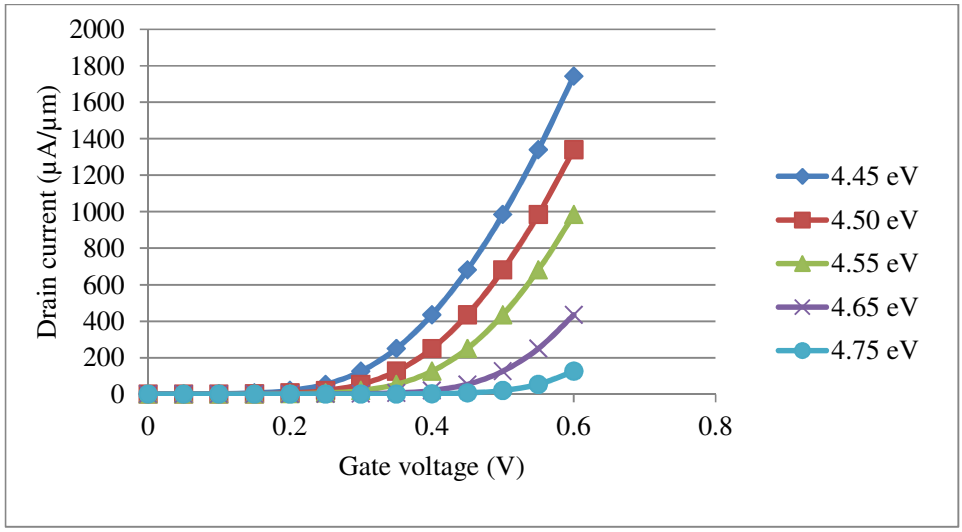

Figure 3.17: Normal plot of I-V for different work function using Green's function approach

The larger the value of gate contact work function, the higher and the wider the potential barrier and so less chance for electron to tunnel through the barrier resulting in smaller leakage current as shown in Figure 3.15 and Figure 3.18. The smaller leakage current means less power dissipation which meets the aim of low power nano-MOSFET logic circuits. The leakage current is the drain current taken at $V_{gs} = 0.00$ V which is intercepts of vertical axis in Figure 3.18.

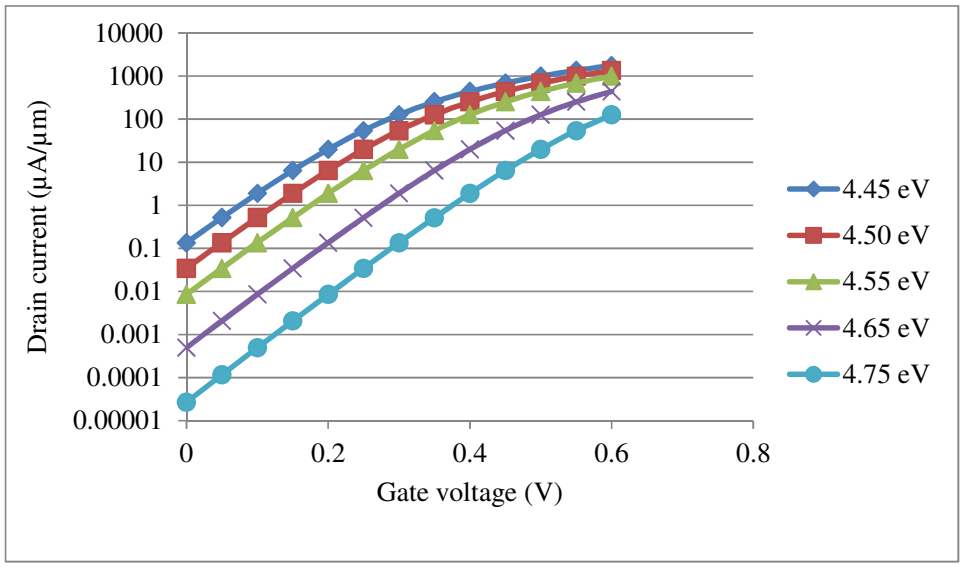

Figure 3.18: Semilog plot of I-V for different work function using Green's function approach.

In order to obtain the optimized parameters for nano-MOSFET, analysis discussed in this paragraph is carried out. Small channel length, L is desired in nano-MOSFET to reduce threshold voltage which is needed for fast switching. From Figure 3.14, the designer chooses L=5 nm and L=10 nm. However, small channel length causes larger leakage current. So, from Figure 3.13, designer choose only L=10 nm instead of L=5 nm. This implies a threshold voltage of 0.20 V which is almost equal to 0.23 V in worst case as justified by the research work of Z. B. Ren, 2001. With the chosen L=10 nm, as gate contact work function increases, both the on-state current and leakage current are reduced as observed in Figure 3.18. From Figure 3.17, gate contact work function 4.75 eV has a threshold voltage of 0.32 V and on-state current of 125 µA/µm. This on-state current is too low when compared with on-state current target of 2500 µA/µm as proposed by Z. B. Ren, 2001. This threshold voltage also deteriorates switching speed. If gate contact work function of 4.45 eV is chosen, the threshold voltage of 0.20 V and on-state current of 1744

μA/μm are obtained. The threshold voltage criteria is met but on-state current is not yet. Thus, a smaller gate contact work function 4.188 eV is proposed. To further control threshold voltage, an intrinsic channel is chosen to avoid threshold voltage fluctuation and also enhance electron mobility. Zero overlap structural design is chosen because this design is more easier to fabricate than underlap or overlap structure which need accurate gate alignment. From Table 3.3 which is simulation result at 300 K, the thinner the channel thickness, the larger the energy level splitting. This large energy level splitting value is much larger than thermal voltage. So, electron only occupy bottom subband and is unable to jump to higher energy levels. Therefore, a few silicon atomic layer channel thickness (in this case is 1.5 nm) with single subband profile (refer to Figure 3.19) is good enough to describe carrier transport in nano-MOSFET. At low temperature 77 K, electron density distribution showed oscillation as indicated in Figure 3.5 which means that electron has wave property in low temperature. Thus, quasi-ballistic transport of carrier is more suitable studied at room temperature than low temperature. The final targeted nano-MOSFET structural parameters which are passed to WinSpice circuit simulator are tabulated in Table 3.1.

Obviously, from above optimization simulation process, nano-MOSFET can be an excellent candidate for logic circuit operation with the following design optimization:

- channel length 10 nm
- gate contact work function 4.188 eV
- thin silicon channel 1.5 nm

- zero overlap
- intrinsic channel
- room temperature 300 K

3.2.3 Determination of Electrical Quantities and Capacitance of nano-MOSFET

Based on the literature presented in Section 2.3.4, from equation (2.5) to (2.13) and optimized parameters listed in Table 3.1, electrical quantities of nano-MOSFET are calculated and are tabulated in Table 3.5.

Table 3.5: Electrical Quantities of nano-MOSFET

Electrical Quantity	Value
Critical Length, l	1.16 nm
Thermal Velocity, v_T	123.43×10^3 m/s
Backscattering Mean Free Path, λ	50.267 nm
Ballistic Efficiency, B	0.96
Backscattering Coefficient, r	0.02

Figure 3.19 shows the plot of subband energy profile along the channel for simulation setting in Table 3.1. The subband energy in Figure 3.19 shows negative value because the source and drain reservoirs are heavily n-type doped. This is the conduction band energy value. On the other hand, for heavily p-type doped nano-MOSFET, the energy value is positive. This is the valence band energy value. In order to calculate the backscattering mean free path, λ as stated in equation (2.6), relevant energy level values in equation

(2.13) are extracted from Figure 3.19 as follow:

$$\eta_F = \frac{\epsilon - E_i}{k_B T} = \frac{(-0.4)-(-0.2)}{k_B(300)} \times q = -7.736$$

Energy levels are taken at the center of the device (-0.2 eV) at channel position 0 nm and also between source and drain (-0.4 eV) which is the average energy between source (-0.1 eV) and drain (-0.7 eV). From equation (2.10) to (2.12), the following Fermi-Dirac integral are obtained:

$$\mathcal{F}_0(\eta_F) = \ln(1 + e^{\eta_F}) = \ln(1 + e^{-7.736}) = 4.365 \times 10^{-4}$$

$$\mathcal{F}_{-1}(\eta_F) = \frac{1}{1+e^{-\eta_F}} = \frac{1}{1+e^{7.736}} = 4.364 \times 10^{-4}$$

$$\mathcal{F}_{1/2}(\eta_F) = e^{\eta_F} = e^{-7.736} = 4.366 \times 10^{-4}$$

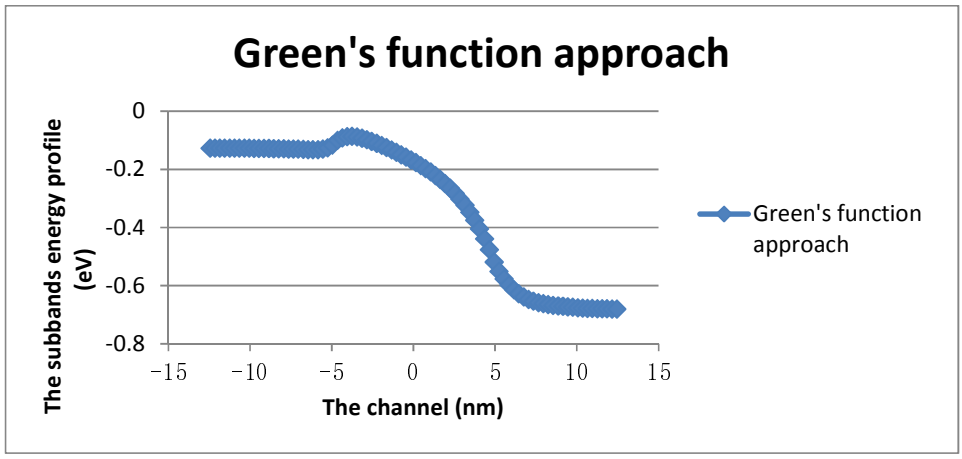

Figure 3.19: The subband energy profile along the channel for nano-MOSFET.

Figure 3.20 shows the simulated drain current versus drain voltage for the same setting in Table 3.1. In order to compare the simulated drain current-drain voltage (I-V) with theoretical calculated I-V, equation (2.15) is used. In order to apply equation (2.15), equation (2.10), (2.12) and equation (2.16) are used. So, with V_D=0.60 V, the following results are obtained:

$$\frac{qV_D}{k_BT} = \frac{q\times 0.60}{k_B\times 300} = 23.21$$

$$\eta_{F1} = \frac{\epsilon - E_i}{k_BT} = \frac{(-0.4)-(-0.12)}{k_B(300)} \times q = -10.83$$

Energy levels are taken at region around top of the barrier (-0.12 eV) at channel position -5 nm and between source and drain (-0.4 eV) which is the average energy between source (-0.1 eV) and drain (-0.7 eV).

$$\mathcal{F}_{1/2}(\eta_{F1}) = e^{\eta_F} = \mathcal{F}_{1/2}(-10.83) = e^{-10.83} = 1.979 \times 10^{-5}$$

$$\mathcal{F}_{1/2}\left(\eta_{F1} - \frac{qV_D}{k_BT}\right) = \mathcal{F}_{1/2}(-34.04) = e^{-34.04} = 1.648 \times 10^{-15}$$

$$\mathcal{F}_0(\eta_F) = \ln(1 + e^{\eta_{F1}}) = \ln(1 + e^{-10.83}) = 1.979 \times 10^{-5}$$

$$\mathcal{F}_0\left(\eta_{F1} - \frac{qV_D}{k_BT}\right) = \mathcal{F}_0(-34.04) = \ln(1 + e^{-34.04}) = 0$$

$$\frac{I_D}{W} = BC_{ox}\widetilde{v_T}(V_{GS} - V_T)\left[\frac{1-\frac{\mathcal{F}_{1/2}\left(\eta_{F1}-\frac{qV_D}{k_BT}\right)}{\mathcal{F}_{1/2}(\eta_{F1})}}{1+\frac{\mathcal{F}_0\left(\eta_{F1}-\frac{qV_D}{k_BT}\right)}{\mathcal{F}_0(\eta_{F1})}}\right] = 2182.23\ \mu A/\mu m$$

Simulated result with Nano-MOSFET shown in Figure 3.20 has $\frac{I_D}{W} = 2500\,\frac{\mu A}{\mu m}$ versus theoretically, $\frac{I_D}{W} = 2182.23\,\frac{\mu A}{\mu m}$ as shown above. These two results are 87.3 % closely matched.

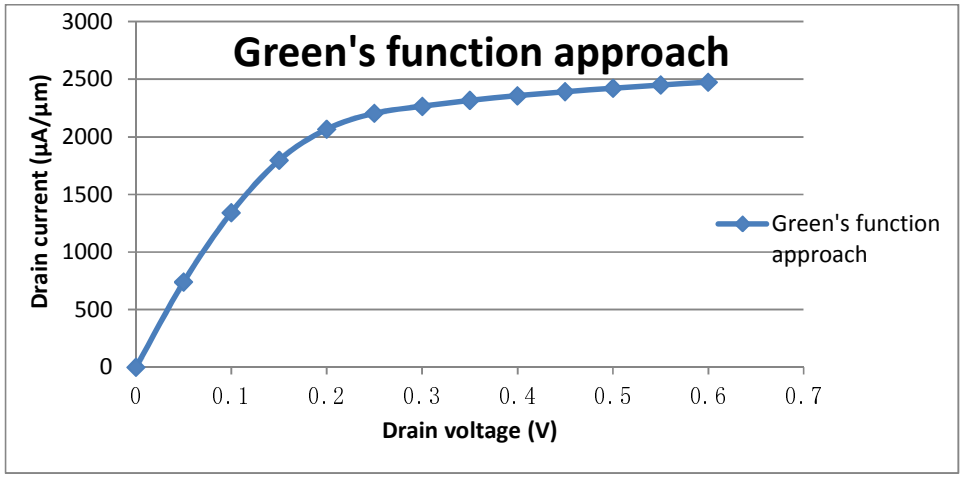

Figure 3.20: Drain current versus drain voltage for nano-MOSFET.

The capacitance model in nano-MOSFET as shown in Figure 2.2 is examined. By using equation (2.17) and (2.18), the calculated quantum effects gate capacitance, drain capacitance and source capacitance for 10 nm nano-MOSFET are calculated and tabulated in Table 3.6. From M. L. P. Tan, et al., 2012, the 45 nm MOSFET capacitances are tabulated in Table 3.6 as well. Since the 10 nm nano-MOSFET and 45 nm MOSFET both have the same width of 125 nm, therefore, the scaling factor between 45 nm technology and 10 nm technology is 0.222 as indicated in Table 3.6. Table 3.6 shows that as MOSFET is scaled down, the capacitance value also scaled down (R. Murali and J. D. Meindl, 2007). These capacitances affect the rise time, fall time and propagation delay of logic circuits. The theoretical calculated capacitance value for 10 nm technology nano-MOSFET are closely matched the downscaled capacitance value obtained through 45 nm technology MOSFET downscaled by scaling factor 0.222. The capacitance mentioned above are important in determining the timing characteristics of logic circuits designed with nano-MOSFET (G. Ghione and A. Benvenuti, 1997; M. Vaidyanathan and D. L. Pulfrey, 1997).

Table 3.6: Capacitance of 10 nm nano-MOSFET using 45 nm nano-MOSFET scaled down

	45 nm MOSFET	After downscaled by scaling factor s = 0.222	10 nm DG nano-MOSFET
Gate Capacitance (F)	6.58×10^{-17}	1.46×10^{-17}	5.76×10^{-17}
Drain Capacitance (F)	1.90×10^{-17}	4.22×10^{-18}	4.60×10^{-18}
Source Capacitance (F)	7.87×10^{-17}	1.75×10^{-17}	1.05×10^{-17}

3.3 Summary

In this chapter nanoMOS simulation software is used to simulate nano-MOSFET in order to characterize the quantum effects and electrical quantities of an optimized parameters nano-MOSFET formulated by Purdue University. The final optimized parameters are channel thickness of 1.5 nm, temperature of 300 K, gate contact work function of 4.188 eV, no gate underlap, gate length of 10 nm and intrinsic channel. The characterized criteria used to justify the above device optimization are low threshold voltage of 0.20 V, ballistic efficiency of 0.96 and low leakage current of 5.312×10^{-2} μA/μm. The above optimized parameters nano-MOSFET will be used to design logic gates in the next chapter where circuit simulations are carried out to evaluate the dc and ac parameters for these logic gates.

CHAPTER FOUR

LOGIC GATES SIMULATION RESULT AND DISCUSSION

4.1 Overview of the Chapter

In this chapter, the logic gates designed with optimized parameter nano-MOSFETs from chapter 3 are ac and dc characterized by performing circuit simulation using WinSpice and HSPICE. The types logic families examined are nano-MOSFET loaded nano-MOSFET logic gates and resistive loaded nano-MOSFET logic gates. Logic gates examined are NOT, 2-input NOR, 2-input NAND and combinational logic with Boolean expression $\overline{x(y+z)}$. These logic gates logical operations are examined by performing circuit simulation with above mentioned software (K. Jabeur, et al., 2014). Timing characteristics such as rise time, fall time and propagation delay of these logic circuits are theoretically calculated and also software simulated (H. Tsuchiya, et al., 2007).

4.2 Nano-MOSFET Logic Gates Simulation using WinSpice

This section is devoted to present the theoretical and WinSpice simulation result of nano-MOSFET loaded nano-MOSFET logic gate and 733.8 Ω resistive loaded nano-MOSFET logic gate. The logic circuits to be simulated are NOT, 2-input NOR, 2-input NAND and combinational logic

with Boolean expression $\overline{x(y+z)}$.

The nano-MOSFET loaded resistance is equivalent to a 733.8 Ω resistor as calculated based on equation (2.19) based on linear portion of the results shown in Figure 3.20 because digital logic circuits operate at linear portion of current-voltage (I-V) curve. When the nano-MOSFET is switched on, the on-state resistance is calculated based on equation (2.20) and is equal to 36.2 Ω. The detail steps to calculate these resistance values are listed below. Since digital logic operates at linear region of I-V curve which is V_D equal to 0.20 V as taken from Figure 3.20. Then,

$$\frac{qV_D}{k_BT} = \frac{q\times 0.20}{k_B\times 300} = 7.736$$

$$\eta_{F1} = \frac{\epsilon - E_i}{k_BT} = \frac{(-0.4)-(-0.12)}{k_B(300)} \times q = -10.83$$

$$\mathcal{F}_{1/2}(\eta_{F1}) = e^{\eta_{F1}} = e^{-10.83} = 1.979 \times 10^{-5}$$

$$\mathcal{F}_{1/2}\left(\eta_{F1} - \frac{qV_D}{k_BT}\right) = \mathcal{F}_{1/2}(-18.566) = e^{-18.566} = 8.647 \times 10^{-9}$$

$$\mathcal{F}_0(\eta_{F1}) = \ln(1 + e^{\eta_{F1}}) = \ln(1 + e^{-10.83}) = 1.979 \times 10^{-5}$$

$$\mathcal{F}_0\left(\eta_{F1} - \frac{qV_D}{k_BT}\right) = \mathcal{F}_0(-18.566) = \ln(1 + e^{-18.566}) = 8.649 \times 10^{-9}$$

$$\widetilde{v_T} = \sqrt{\frac{2k_BT}{\pi m_t^*}} \frac{\mathcal{F}_{1/2}(\eta_{F1})}{\mathcal{F}_0(\eta_{F1})} = 123.434 \times 10^3\ m/s$$

$$C_{ox} = \frac{3.9\times\varepsilon_o\times 2}{T_{ox}} = 46.04 \times 10^{-3}\ F/m^2 \qquad T_{ox} = 1.5 \text{ nm}$$

Take V_{GS} = 0.60 V, V_T = threshold voltage = 0.20 V, B = 0.96, V_D = 0.2 V, L=10 nm and W=125 nm. From equation (2.15) and then applying equation (2.19) and (2.20):

$$\frac{I_D}{W} = BC_{ox}\widetilde{v_T}(V_{GS} - V_T)\left[\frac{1-\frac{\mathcal{F}_{1/2}\left(\eta_{F1}-\frac{qV_D}{k_BT}\right)}{\mathcal{F}_{1/2}(\eta_{F1})}}{1+\frac{\mathcal{F}_0\left(\eta_{F1}-\frac{qV_D}{k_BT}\right)}{\mathcal{F}_0(\eta_{F1})}}\right] = 2180.32\ \mu A/\mu m$$

$$R_{Load} = \left(\frac{V_{DS}}{I_{DS}}\right) = \frac{V_{th}}{I_{on-state\ at\ linear\ region} \times W} = \frac{0.20\ V}{2180.32\frac{\mu A}{\mu m} \times 125\ nm} =$$

$$733.8\ \Omega$$

$$R_{channel\ at\ on-state} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{DD} - V_{th})} =$$

$$\frac{1}{0.12\ m^2/Vs \times 46.04 \times 10^{-3}\ F/m^2 \times \left(\frac{125\ nm}{10\ nm}\right)(0.60\ V - 0.20\ V)} = 36.2\ \Omega$$

These resistances values are used to determine the rise time and fall time of the logic gates.

4.2.1 NOT Logic Gate

This section is devoted to present the simulation result for NOT logic circuit. Two types of NOT logic circuits are studied, namely (i) nano-MOSFET loaded MOSFET circuit (refer to Figure 2.3) and (ii) resistive loaded MOSFET circuit (refer to Figure 4.1). The theory of nano-MOSFET loaded MOSFET NOT circuit is covered in section 2.4.1 in chapter 2. The timing characteristics investigated include rise time, fall time and propagation delay. Theoretical values of these timing characteristics are compared with simulated value using WinSpice. Voltage transfer characteristics VTC including power dissipation results are presented.

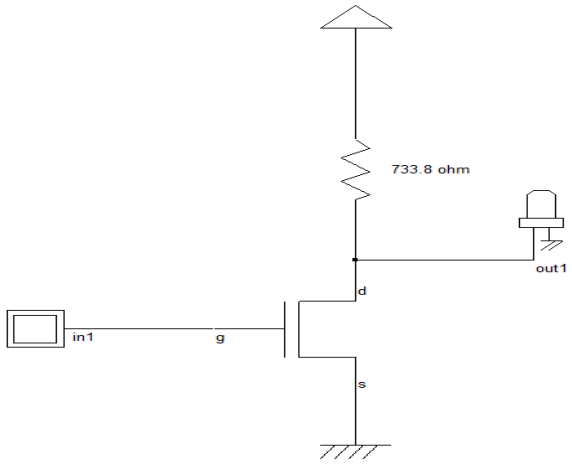

Figure 4.1: Resistive loaded NOT transistor level circuit

4.2.1.1 ac Parameter

Figure 4.2(a) and Figure 4.2(b) are the input and output signal to logic circuit at Figure 2.3. The input signal has a period of 10 ns with duty cycle 50% and amplitude of 0.6 V. The output signal has amplitude of 0.4 V due to threshold voltage loss of 0.2 V at the load nano-MOSFET which acts as *n*-type pass transistor. The input and output signal show correct logical NOT operation relationship. Figure 4.3(a) and Figure 4.3(b) are the input and output signal to logic circuit at Figure 4.1. The input signal has a period of 10 ns with duty cycle 50% and amplitude of 0.6 V. The output signal has amplitude of 0.6 V. The input and output signal also show correct logical NOT operation relationship. Figure 4.4(a) and Figure 4.4(b) are the input and output signal which are used for transient analysis for logic circuit shown in Figure 2.3. The input signal has a period of 8 ps with duty cycle 50% and amplitude of 0.6 V. The output signal has amplitude of 0.4 V due to threshold voltage loss of 0.2 V at the load nano-MOSFET which acts as *n*-type pass transistor. The output signal shows obvious rise time and fall time. The fall time is 0.24 ps and rise

time is 1.69 ps with period 8 ps which is equivalent to pulse width 4 ps (50% duty cycle). The theoretical calculated propagation delay based on section 2.4.1 is 0.036 ps as tabulated in Table 4.1. The simulated propagation delay is 0.0827 ps as measured from WinSpice output result. Therefore, the theoretical switching speed is 2.32 times that of simulated value. By using theory in section 2.4.1.1, the ac parameters of NOT gate Table 4.1 is obtained. From Table 4.1, the theoretical maximum frequency of operation is around 754 GHz whereas the simulated maximum frequency of operation is 516 GHz. The percentage of error between these two values is 32%. The reason for the difference is due to; in theoretical calculation, quasi-ballistic transport model is used whereas in Winspice simulation quantum corrected drift-diffusion model is used. Scattering events are more obvious in quantum corrected drift-diffusion model than quasi-ballistic transport model. So, theoretical quasi-ballistic model has shorter delay and hence faster frequency. Both of these values are higher than operation frequency of 65 nm MOSFET circuits which is around 300 GHz as reported by J. Sharma and H. Krishnaswamy, 2013. Thus, high speed logical NOT circuit designed with 10 nm nano-MOSFET has been achieved.

Table 4.1 tabulated the timing characteristic of nano-MOSFET loaded NOT logic circuit.

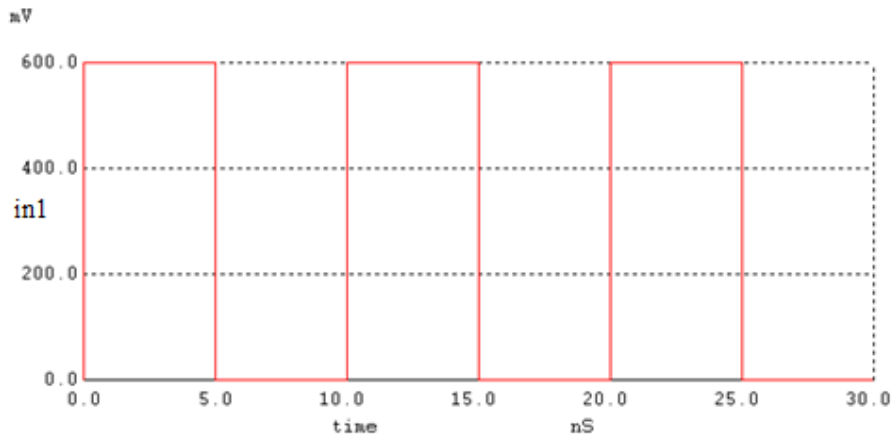

Figure 4.2(a): Input signal in1 of nano-MOSFET loaded NOT logic gate

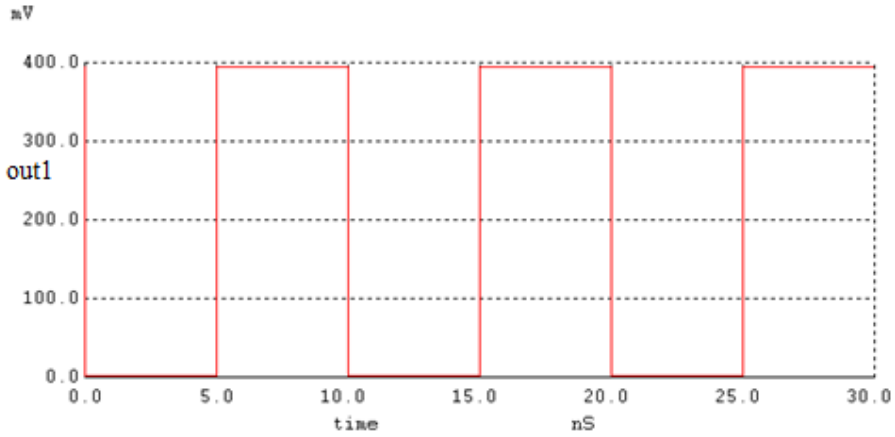

Figure 4.2(b): Output signal out1 of nano-MOSFET loaded NOT logic gate

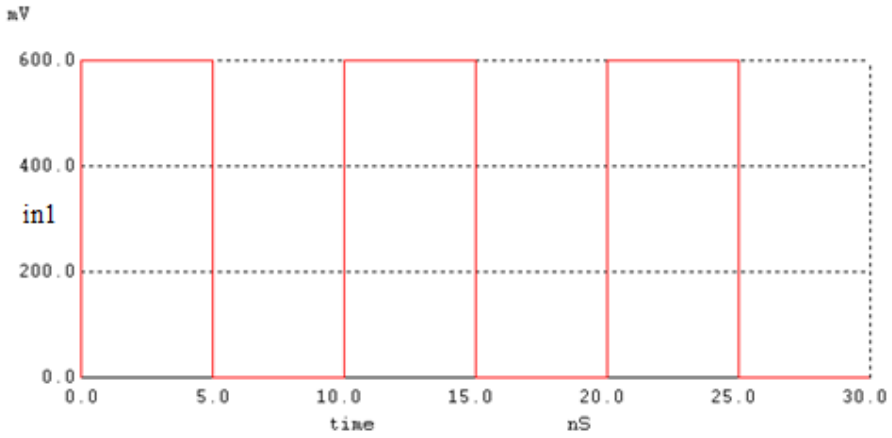

Figure 4.3(a): Input signal in1 of resistive loaded NOT logic gate

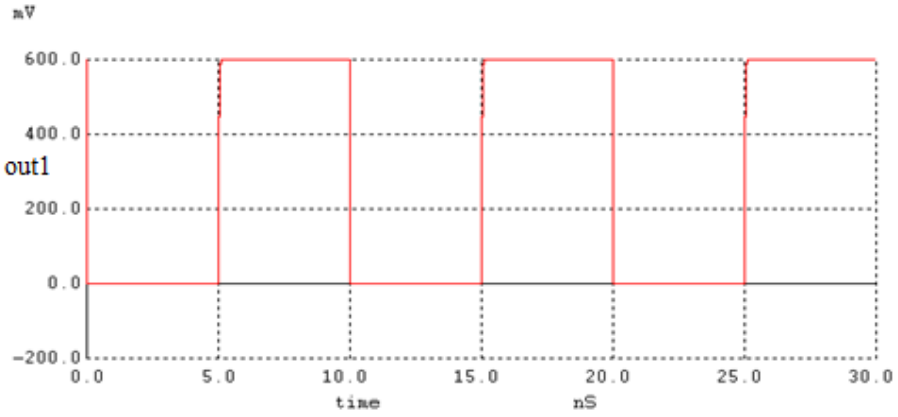

Figure 4.3(b): Output signal out1 of resistive loaded NOT logic gate

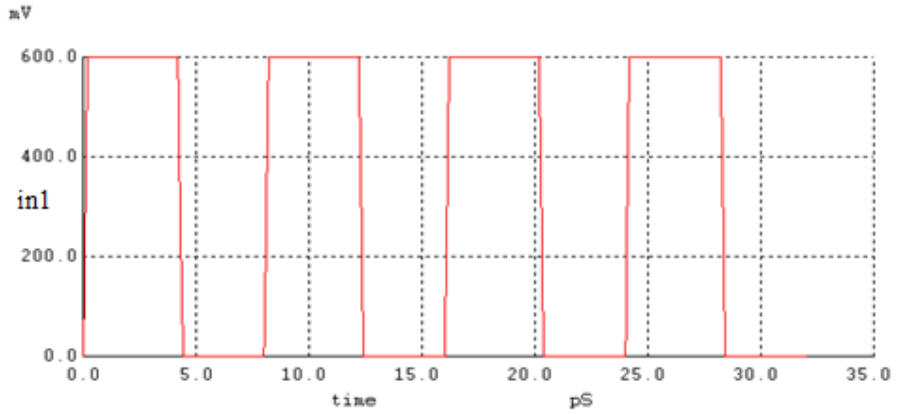

Figure 4.4(a): Transient Response of WinSpice Input Signal in1 with period 8 ps to NOT logic gate

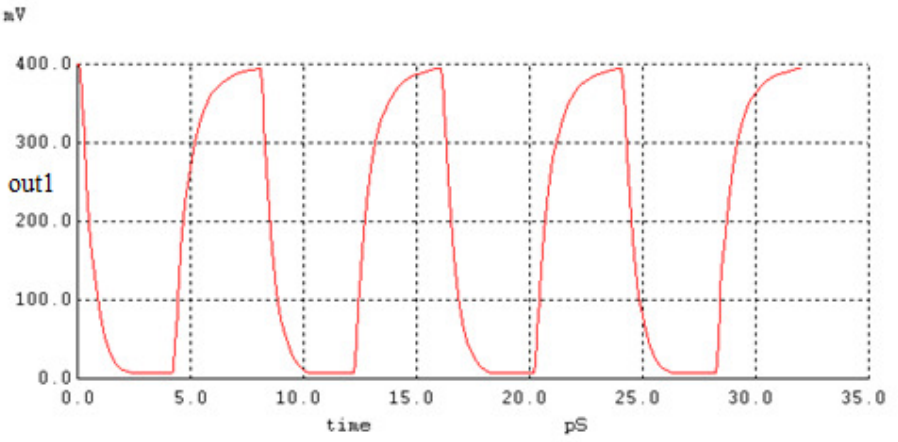

Figure 4.4(b): Transient Response of WinSpice Output Signal out1 of NOT logic gate

Table 4.1: Theoretical and Simulated value of nano-MOSFET loaded NOT logic gate.

Parameters	-	
Gate Capacitance (F)	5.755×10^{-17}	
Area Capacitance (F)	1.612×10^{-19}	
Sidewall Capacitance (F)	6.072×10^{-17}	
Total Drain Capacitance (F)	4.604×10^{-18}	
Total Source Capacitance (F)	1.046×10^{-17}	
NOT Gate Total Capacitance (F)	1.340×10^{-16}	
Load Resistance (ohm)	733.8	
On-state Channel Resistance (ohm)	36.2	
	Theoretical Value	WinSpice Simulated Value
Rise Time Constant	9.996×10^{-14}	1.264×10^{-13}
Rise Time (s)	1.314×10^{-12}	1.696×10^{-12}
Fall Time Constant	4.832×10^{-15}	1.100×10^{-13}
Fall Time (s)	1.063×10^{-14}	2.420×10^{-13}
Propagation Delay (s)	3.562×10^{-14}	8.275×10^{-14}
Maximum Frequency (Hz)	7.545×10^{11}	5.160×10^{11}

4.2.1.2 dc Parameters

The section is devoted to present the dc parameters of NOT logic circuit which its theory is covered in section 2.4.1.2 in chapter 2. Both two resistive loaded NOT logic circuit and nano-MOSFET loaded NOT logic circuit are investigated (H. C. Chin, et al., 2014; R. Hosseini and N. Teimuorzadeh, 2013).

Figure 4.5 and Figure 4.6 show the plot of simulated WinSpice voltage transfer characteristic (VTC) of logic NOT gates shown in Figure 2.3 and Figure 4.1, respectively. The advantage of one logic gate over the other is

assessed by comparing VTC in term of noise margin and transition width of both logic circuits. The VTC parameters which are listed in section 2.4.1.2 are extracted from these two plots and tabulated in Table 4.2 and Table 4.3.

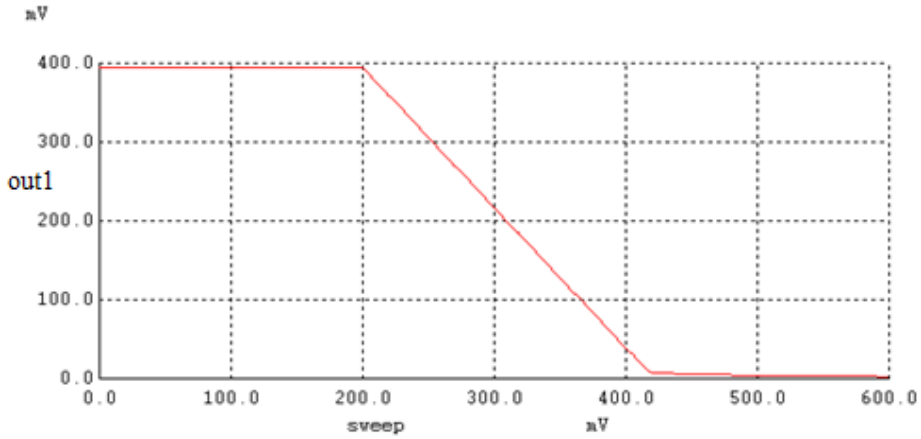

Figure 4.5: Simulated VTC curve of nano-MOSFET loaded NOT logic gate.

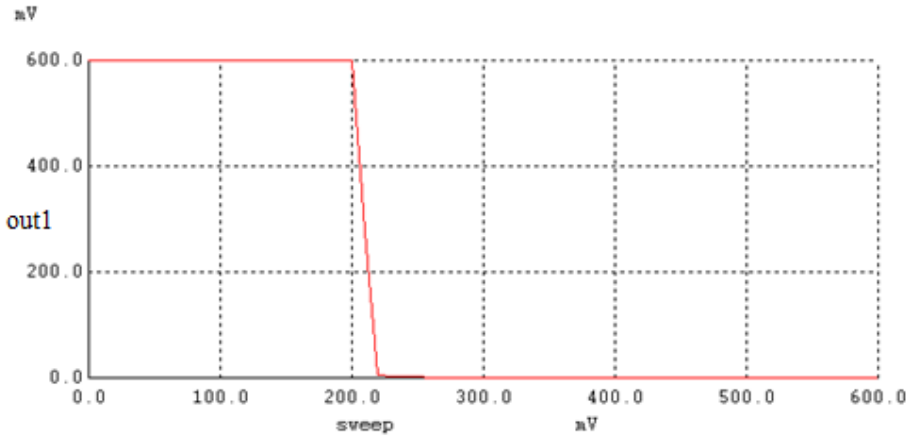

Figure 4.6: Simulated VTC curve of resistive loaded NOT logic gate.

Table 4.2: VTC parameters for nano-MOSFET loaded NOT logic gate

Nano-MOSFET loaded NOT logic gate	
V_{OH}	0.40 V
V_{OL}	0.00 V
V_{IH}	0.42 V
V_{IL}	0.20 V
V_{M}	0.27 V
V_{LS}	0.40 V
V_{TW}	0.22 V
V_{NMH}	-0.02 V
V_{NML}	0.20 V
V_{NSH}	0.13 V
V_{NSL}	0.27 V
V_{NIH}	0.33
V_{NIL}	0.68

Table 4.3: VTC parameters for resistive loaded NOT logic gate

Resistive loaded 733.8 Ω NOT logic gate	
V_{OH}	0.60 V
V_{OL}	0.00 V
V_{IH}	0.22 V
V_{IL}	0.20 V
V_{M}	0.21 V
V_{LS}	0.60 V
V_{TW}	0.02 V
V_{NMH}	0.38 V
V_{NML}	0.20 V
V_{NSH}	0.39 V
V_{NSL}	0.21 V
V_{NIH}	0.65
V_{NIL}	0.35

The transition width of NOT logic gate listed in Table 4.2 is 0.22 V whereas the transition width of NOT logic gate listed in Table 4.3 is 0.02 V. The NOT logic gate listed in Table 4.2 has noise margin low 0.20 V and noise margin high -0.02 V. This negative noise margin high value is due to threshold voltage loss. Meanwhile, the NOT logic gate listed in Table 4.3 has noise margin low

0.20 V and noise margin high 0.38 V. Therefore, resistive loaded nano-MOSFET NOT logic gate has high noise margin and low transition width. This feature enable resistive loaded nano-MOSFET NOT logic gate has better switching characteristic. This is because the presence of larger capacitance at the output node of nano-MOSFET loaded NOT logic gate.

Table 4.4 tabulates the power dissipation for two different NOT logic gates calculated using equation (2.21) in section 2.4.1.2. When compared with logic gate designed using MOSFET with width, W=1 µm, length, L=120 nm and thickness, T_{Si} = 60 nm, which has a downscaled power dissipation of 140.9 µW range as reported by K. Naskar, et al., 2012, the two power dissipation in Table 4.4 showed reduction during down scaling nano-MOSFET to nanometer regime. This is equivalent to power reduction of 23.44 when compared to nano-MOSFET loaded NOT circuit.

Table 4.4: Power dissipation of two different NOT logic gates.

	nano-MOSFET loaded NOT	Resistive loaded NOT
Power dissipation, (Watts)	6.01×10^{-6}	2.07×10^{-7}
Volatge Supply, V_{DD} (V)	0.6	0.6
Frequency of switching, *f*(Hz)	5.00×10^{11}	5.00×10^{11}

Comparison is carried out between these two NOT logic gates in term of power dissipation and VTC. By using WinSpice circuit simulator, simulated

power dissipation and propagation delay for nano-MOSFET loaded NOT logic gate are reported to be 6.01 μW and 82.76 fs, respectively. The analysis done here has confirmed that nano-MOSFET can be used as switching circuit that can fulfill the requirement of lower power dissipation and higher speed NOT logic gate (K. Navi, et al., 2010).

4.2.2 NOR Logic Gate

This section is devoted to present the simulation result for 2 inputs NOR logic gate. Two types of NOR logic gates are studied, namely (i) nano-MOSFET loaded MOSFET logic gate (refer to Figure 2.6) and (ii) resistive loaded MOSFET logic gate (refer to Figure 4.7). The theory of nano-MOSFET loaded MOSFET NOR logic gate is covered in section 2.4.2 in chapter 2. The timing characteristics investigated include rise time, fall time and propagation delay. Theoretical values of these timing characteristics are compared with simulated value using WinSpice.

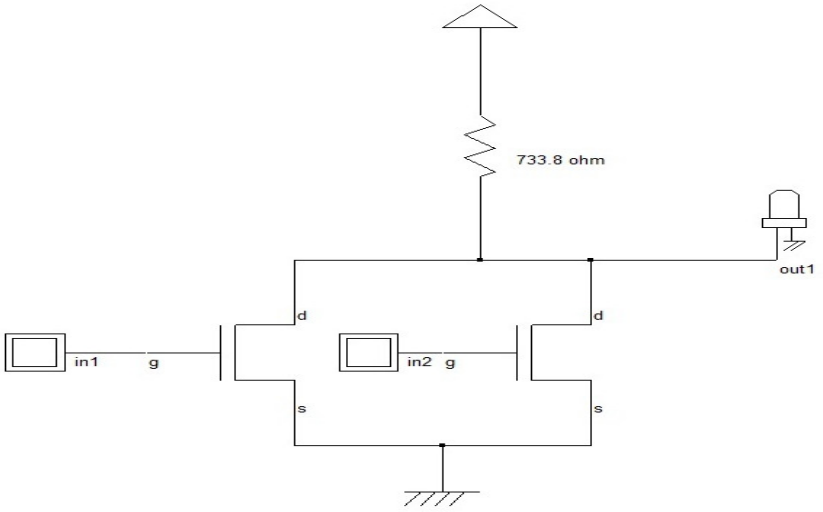

Figure 4.7: Two inputs resistive loaded nano-MOSFET NOR logic gate

Figure 4.8(a), Figure 4.8(b) and Figure 4.8(c) are the input and output signals to logic gate at Figure 2.6. The first input signal has a period of 20 ns with duty cycle 50% and amplitude of 0.6 V. The second input signal has a period of 10 ns with duty cycle 50% and amplitude of 0.6 V. The output signal has amplitude of 0.4 V due to threshold voltage loss of 0.2 V at the load nano-MOSFET which acts as *n*-type pass transistor. The input and output signals show correct logical NOR operation relationship. Figure 4.9(a), Figure 4.9(b) and Figure 4.9(c) are the input and output signals to logic gate at Figure 4.7. The first input signal has a period of 20 ns with duty cycle 50% and amplitude of 0.6 V. The second input signal has a period of 10 ns with duty cycle 50% and amplitude of 0.6 V. The output signal has amplitude of 0.6 V. The input and output signals also show correct logical NOR operation relationship. Figure 4.10(a), Figure 4.10(b) and Figure 4.10(c) are the input and output signals which are used for transient analysis for logic gate shown in Figure 2.6. The first input signal has a period of 20 ps with duty cycle 50% and amplitude of 0.6 V. The second input signal has a period of 10 ps with duty cycle 50% and amplitude of 0.6 V. The output signal has amplitude of 0.4 V due to threshold voltage loss of 0.2 V at the load nano-MOSFET which acts as *n*-type pass transistor. The output signal shows obvious rise time and fall time. The simulated fall time is 0.308 ps and rise time is 2.231 ps with period 20 ps which is equivalent to pulse width 6 ps (30% duty cycle). The theoretical calculated best case propagation delay is 35.9 fs as tabulated in Table 4.5. The theoretical calculated worst case propagation delay is 36.9 fs as tabulated in Table 4.5. The simulated propagation delay is 107.1 fs as measured from

WinSpice output result. Therefore, the theoretical best case switching speed is 2.97 times that of simulated value. On the other hand, the theoretical worst case switching speed is 2.91 times that of simulated value. From Table 4.5 and Table 4.7, the best case maximum frequency of operation is around 732 GHz whereas the worst case maximum frequency of operation is around 729 GHz. The simulated maximum frequency of operation is 394 GHz. The percentage of error between simulated maximum frequency of operation and the best case maximum frequency of operation values is 46.2%. The percentage of error between simulated maximum frequency of operation and the worst case maximum frequency of operation values is 46%. All of these frequencies are higher than operation frequency of 65 nm MOSFET circuits which is around 300 GHz as reported by J. Sharma and H. Krishnaswamy, 2013. The reason for the difference between simulated and theoretical frequency of operation is due to; in theoretical calculation, quasi-ballistic transport model is used whereas in Winspice simulation quantum corrected drift-diffusion model is used. Scattering events are more obvious in quantum corrected drift-diffusion model than quasi-ballistic transport model. So, theoretical quasi-ballistic model has shorter delay and hence faster frequency. Thus, high speed NOR logic gate designed with 10 nm nano-MOSFET has been achieved. Table 4.5 tabulated the timing characteristic of nano-MOSFET loaded NOR logic gate. Table 4.6 and Table 4.7 tabulated the theoretical derived timing characteristics and WinSpice simulated timing characteristics, respectively.

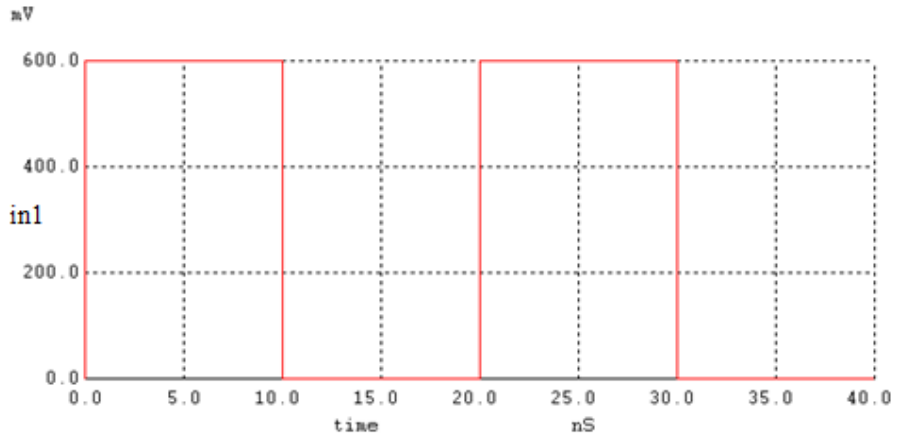

Figure 4.8(a): First input in1 to nano-MOSFET loaded nano-MOSFET NOR logic gate

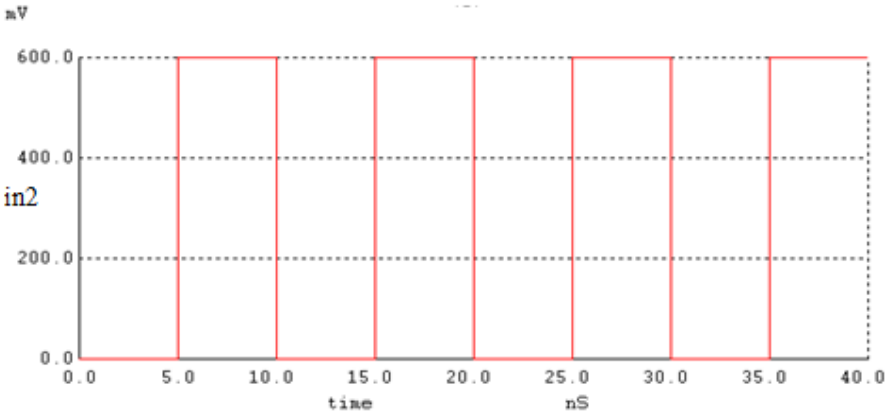

Figure 4.8(b): Second input in2 to nano-MOSFET loaded nano-MOSFET NOR logic gate

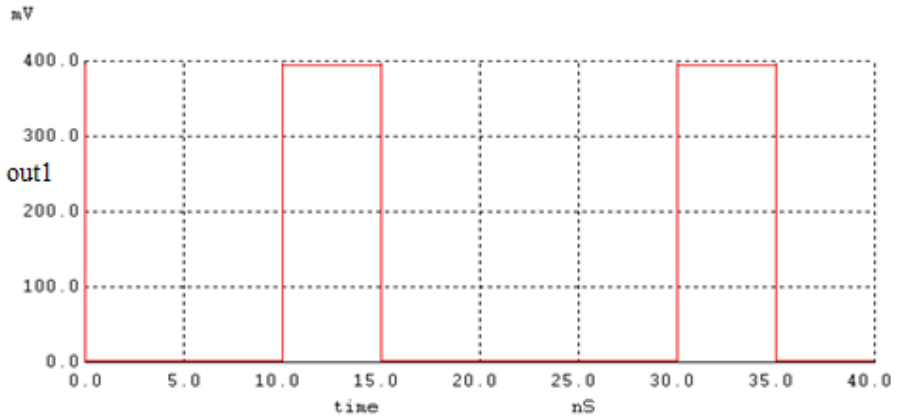

Figure 4.8(c): Output out1 of nano-MOSFET loaded nano-MOSFET NOR logic gate

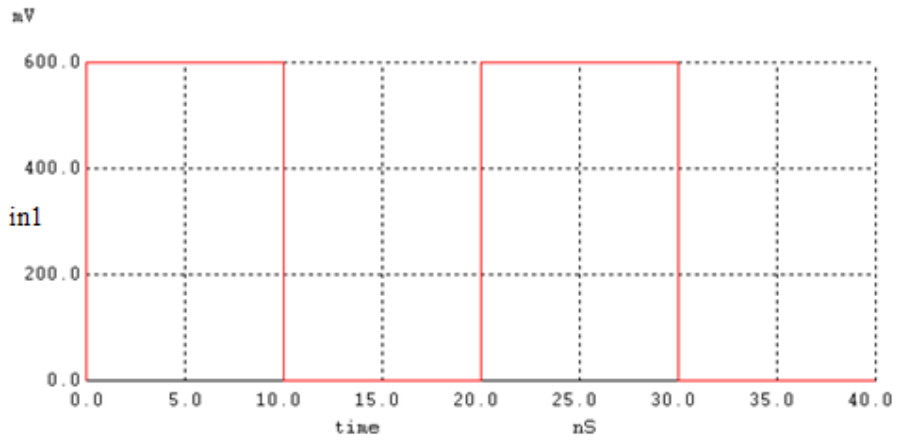

Figure 4.9(a): First input in1 to resistive loaded nano-MOSFET NOR logic gate

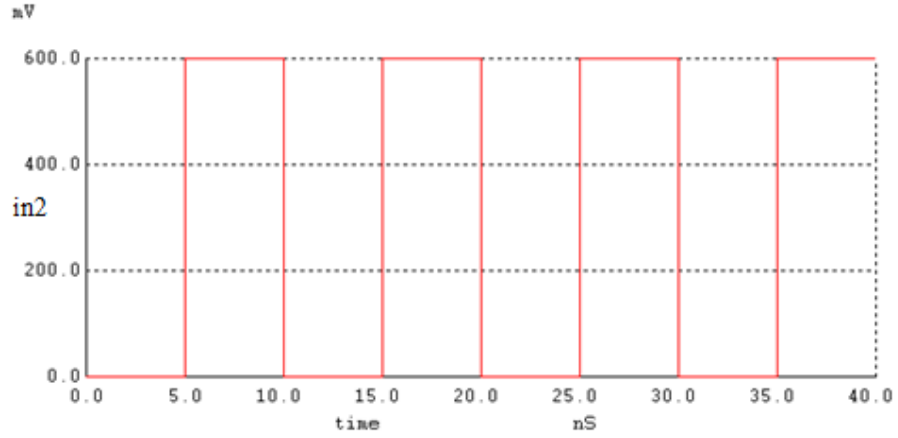

Figure 4.9(b): Second input in2 to resistive loaded nano-MOSFET NOR logic gate

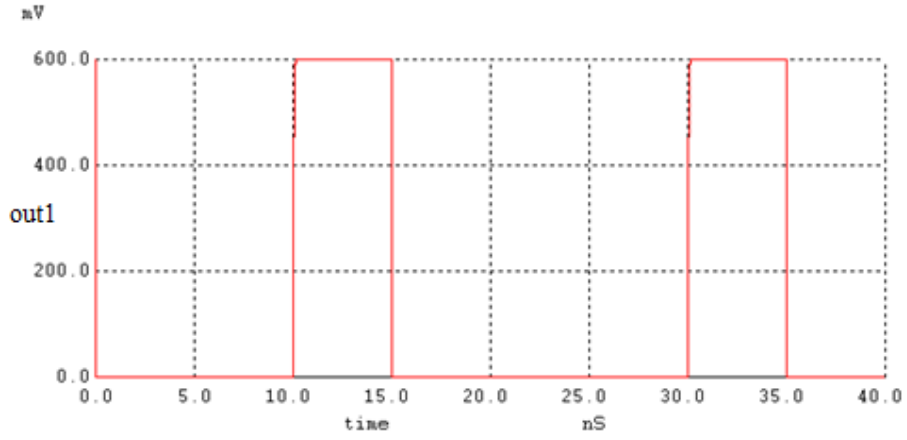

Figure 4.9(c): Output out1 of resistive loaded nano-MOSFET NOR logic gate

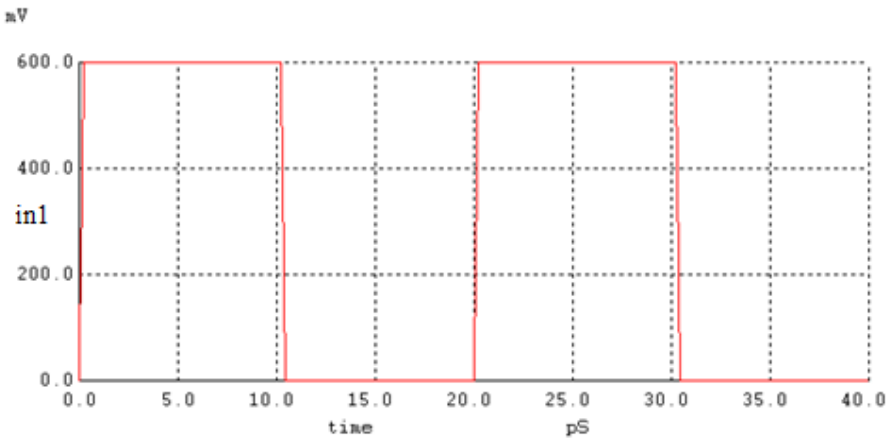

Figure 4.10(a): First input in1 to nano-MOSFET loaded nano-MOSFET NOR logic gate for transient analysis

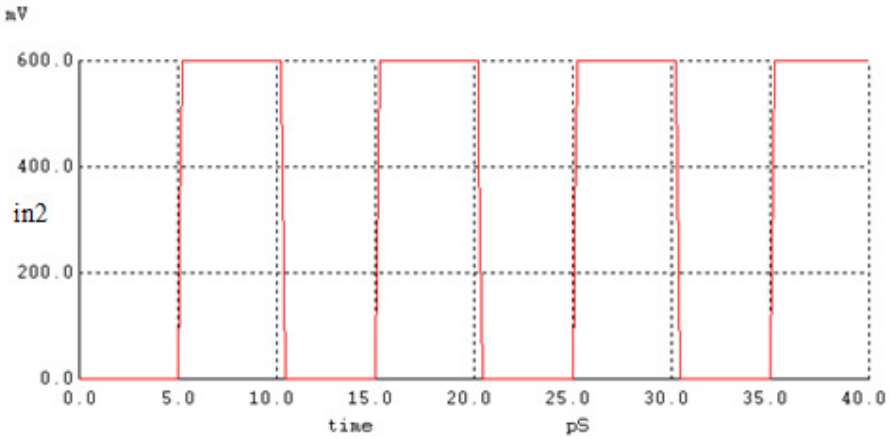

Figure 4.10(b): Second input in2 to nano-MOSFET loaded nano-MOSFET NOR logic gate for transient analysis

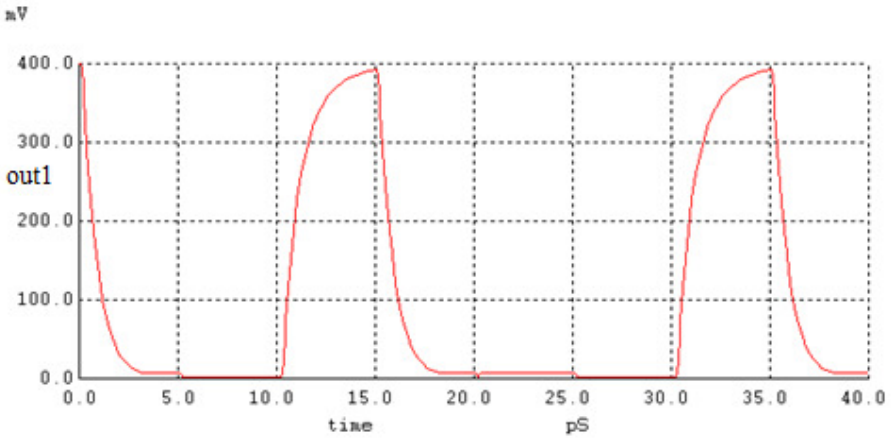

Figure 4.10(c): Output out1 of nano-MOSFET loaded nano-MOSFET NOR logic gate for transient analysis

Table 4.5: Theoretical value of nano-MOSFET loaded 2-input NOR logic gate.

Double Gate n nano-MOSFET Loaded NOR Gate	
Gate Capacitance (C_G)	5.755×10^{-17} F
Area Capacitance (C_A)	1.612×10^{-19} F
Sidewall Capacitance (C_{SW})	6.072×10^{-17} F
Drain Capacitance (C_D)	4.604×10^{-18} F
Source Capacitance (C_S)	1.046×10^{-17} F
nano-MOSFET Loaded Resistance (R_{Load})	733.8 Ω
nano-MOSFET on-state Resistance (R_{on})	36.2 Ω
Loaded NOR2 Gate Total Capacitance (C_{total})	1.381×10^{-16} F
Rise Time Constant (τ_r)	1.013×10^{-13} s
Rise Time (t_r)	1.360×10^{-12} s
(i) Best Case when 2 nMOS Turn On	
Fall Time Constant (τ_f)	2.499×10^{-15} s
Fall Time (t_f)	5.499×10^{-15} s
Propagation Delay (t_p)	3.598×10^{-14} s
Maximum Signal Frequency ($f$max)	7.323×10^{11} Hz
(ii) Worst Case when 1 nMOS On and 1 nMOS Off	
Fall Time Constant (τ_f)	4.999×10^{-15} s
Fall Time (t_f)	1.099×10^{-14} s
Propagation Delay (t_p)	3.685×10^{-14} s
Maximum Signal Frequency (f_{max})	7.293×10^{11} Hz

Table 4.6: Theoretical derived timing characteristic of 2 input NOR logic gate

Theoretical Modeling Calculations from NanoMOS Device Simulation Data (10% and 90% Points)				
Logic Gates	Rise Time (t_r)	Fall Time (t_f)	Propagation Delay (t_p)	Maximum Operating Frequency (f_{max})
NOR	1.36×10^{-12} s	1.10×10^{-14} s	3.69×10^{-14} s	7.29×10^{11} Hz

Table 4.7: Simulated value of timing characteristic of 2 input NOR logic gate

WinSpice Simulation Results Using Model Level MOS6 (10% and 90% Points)				
Logic Gates	Rise Time (t_r)	Fall Time (t_f)	Propagation Delay (t_p)	Maximum Operating Frequency (f_{max})
NOR	2.23×10^{-12} s	30.76×10^{-14} s	1.07×10^{-13} s	3.94×10^{11} Hz

Table 4.8 shows the power dissipation for two different NOR logic gates calculated using equation of power dissipation in equation (2.22) in section 2.4.2. When compared with logic gate designed using MOSFET with width, W=1 μm, length, L=120 nm and thickness, T_{Si} = 60 nm, which has a downscaled power dissipation of 140.9 μW range as reported by K. Naskar, et al., 2012, the two power dissipation in Table 4.8 showed reduction during down scaling nano-MOSFET to nanometer regime. This is equivalent to power reduction of 30.23 when compared to nano-MOSFET loaded NOR circuit.

Table 4.8: Power dissipation of two different 2 input NOR logic circuits.

	nano-MOSFET loaded NOR	Resistive loaded NOR
Power Dissipation (Watts)	4.66×10^{-6}	3.11×10^{-7}
Voltage Supply (Volts)	0.6	0.6
Frequency of switching (Hertz)	5.00×10^{11}	5.00×10^{11}

Comparison is carried out between the two logic NOR logic gates in term of power dissipation. By using WinSpice circuit simulator, simulated power dissipation and worst case propagation delay for nano-MOSFET loaded NOR logic gate are reported to be 4.66 μW and 107.1 fs, respectively. The analysis done here has confirmed that nano-MOSFET can be used as switching circuit that can fulfill the requirement of lower power dissipation and higher speed NOR logic gate (K. Navi, et al., 2010).

4.2.3 NAND Logic Gate

This section is devoted to present the simulation result for 2 inputs NAND logic circuit. Two types of NAND logic gates are studied, namely (i) nano-MOSFET loaded MOSFET logic gate (refer to Figure 2.7) and (ii) resistive loaded MOSFET logic gate (refer to Figure 4.11). The theory of nano-MOSFET loaded MOSFET NAND logic gate is covered in section 2.4.3 in chapter 2. The timing characteristics investigated include rise time, fall time and propagation delay. Theoretical values of these timing characteristics are compared with simulated value using WinSpice.

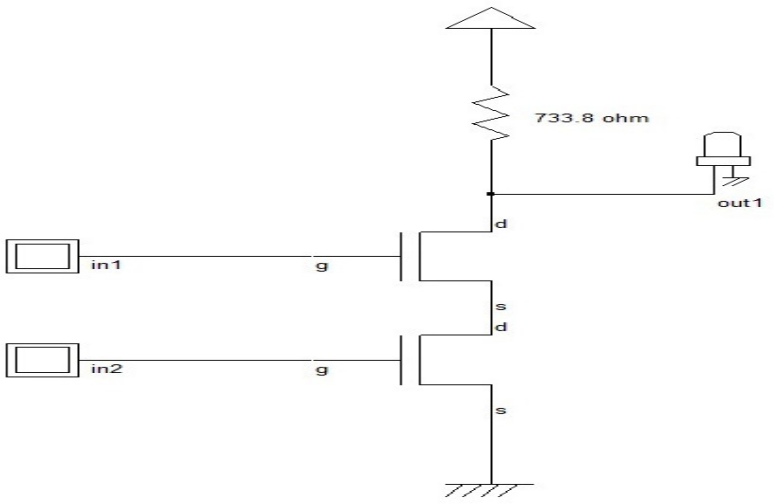

Figure 4.11: Two inputs resistive loaded nano-MOSFET NAND logic gate

Figure 4.12(a), Figure 4.12(b) and Figure 4.12(c) are the input and output signals to logic gate at Figure 2.7. The first input signal has a period of 20 ns with duty cycle 50% and amplitude of 0.6 V. The second input signal has a period of 30 ns with duty cycle 50% and amplitude of 0.6 V. The output signal has amplitude of 0.4 V due to threshold voltage loss of 0.2 V at the load nano-MOSFET which acts as *n*-type pass transistor. The input and output signals show correct logical NAND operation relationship. Figure 4.13(a), Figure 4.13(b) and Figure 4.13(c) are the input and output signals to logic gate at Figure 4.11. The first input signal has a period of 20 ns with duty cycle 50% and amplitude of 0.6 V. The second input signal has a period of 30 ns with duty cycle 50% and amplitude of 0.6 V. The output signal has amplitude of 0.6 V. The input and output signals also show correct logical NAND operation. Figure 4.14(a), Figure 4.14(b) and Figure 4.14(c) are the input and output signals which are used for transient analysis for logic gate at Figure 2.7. The first input signal has a period of 20 ps with duty cycle 50% and amplitude of

0.6 V. The second input signal has a period of 30 ps with duty cycle 50% and amplitude of 0.6 V. The output signal has amplitude of 0.4 V due to threshold voltage loss of 0.2 V at the load nano-MOSFET which acts as *n*-type pass transistor. The output signal shows obvious rise time and fall time. The simulated fall time is 0.68 ps and rise time is 2.73 ps with period 60 ps which is equivalent to pulse width 45 ps (75% duty cycle). The theoretical calculated propagation delay is 0.037 ps as tabulated in Table 4.9. The simulated propagation delay is 0.18 ps as measured from WinSpice output result. Therefore, the theoretical switching speed is 4.79 times that of simulated value. From Table 4.9 and Table 4.11, the theoretical maximum frequency of operation is around 747 GHz whereas the simulated maximum frequency of operation is 293 GHz. The percentage of error between these two values is 61%. All of these frequencies are higher than operation frequency of 65 nm MOSFET circuits which is around 300 GHz as reported by J. Sharma and H. Krishnaswamy, 2013. The reason for this difference is due to; in theoretical calculation, quasi-ballistic transport model is used whereas in Winspice simulation quantum corrected drift-diffusion model is used. Scattering events are more obvious in quantum corrected drift-diffusion model than quasi-ballistic transport model. So, theoretical quasi-ballistic model has shorter delay and hence faster frequency. Thus, high speed NAND logic gate designed with nano-MOSFET has been achieved. Table 4.9 tabulated the timing characteristic of nano-MOSFET loaded NAND logic gate based on theory in section 2.4.3. Table 4.10 and Table 4.11 tabulated the theoretical derived timing characteristics and WinSpice simulated timing characteristics, respectively.

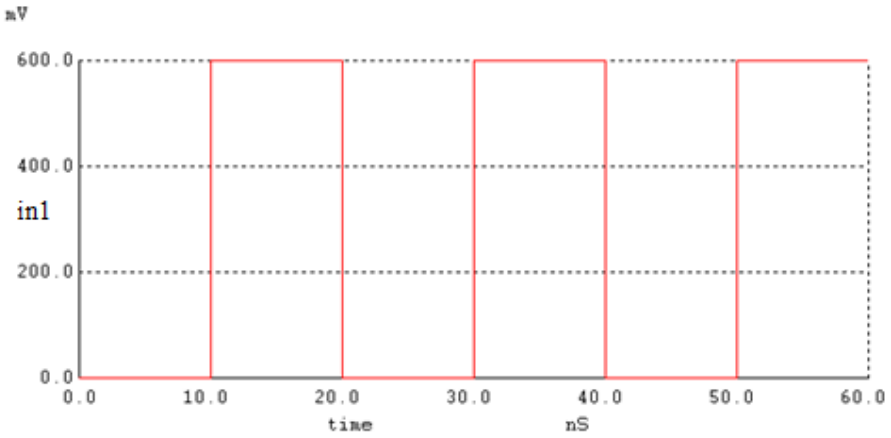

Figure 4.12(a): First input in1 to nano-MOSFET loaded nano-MOSFET NAND logic gate

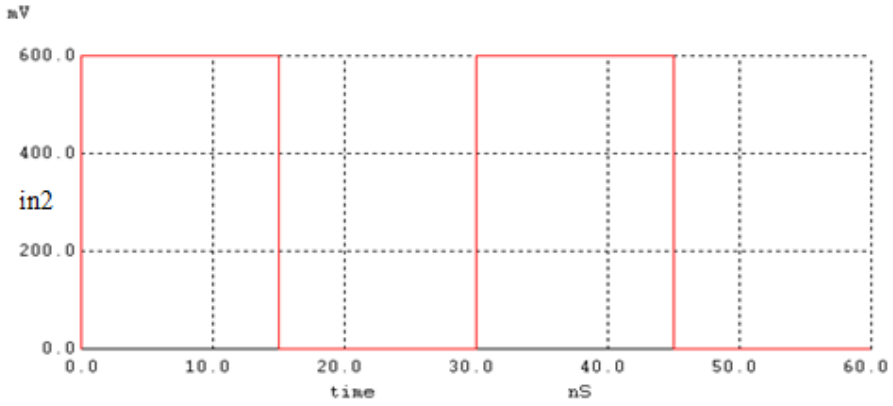

Figure 4.12(b): Second input in2 to nano-MOSFET loaded nano-MOSFET NAND logic gate

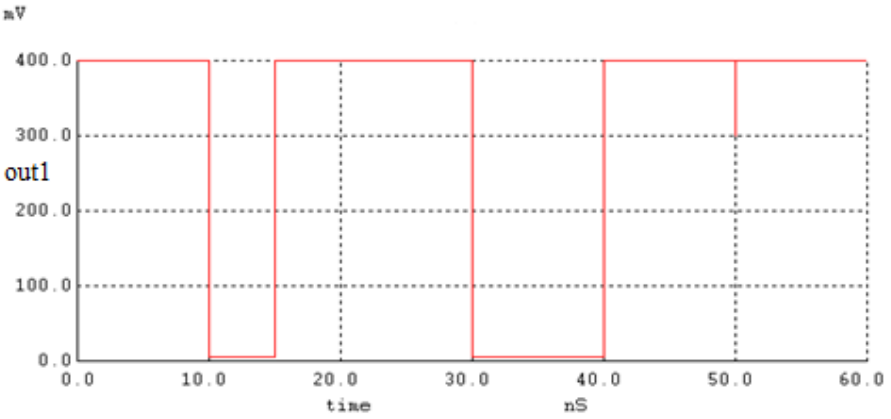

Figure 4.12(c): Output out1 of nano-MOSFET loaded nano-MOSFET NAND logic gate

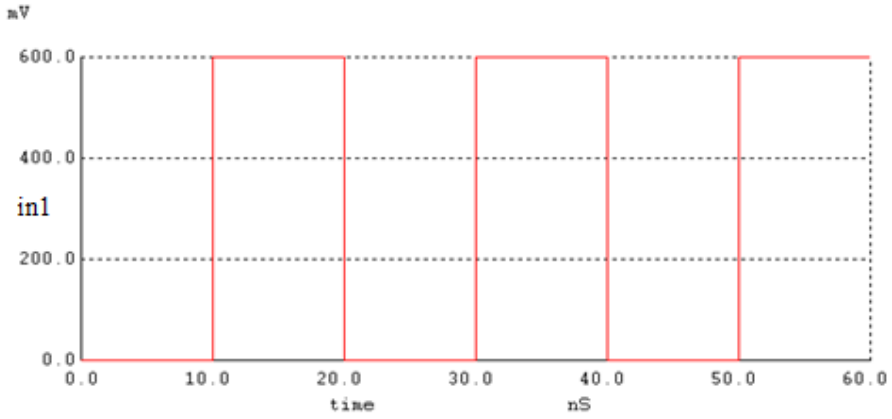

Figure 4.13(a): First input in1 to resistive loaded nano-MOSFET NAND logic gate

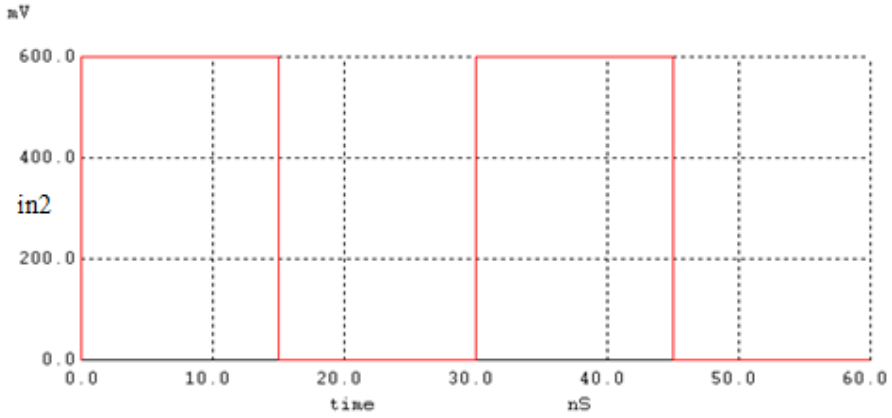

Figure 4.13(b): Second input in2 to resistive loaded nano-MOSFET NAND logic gate

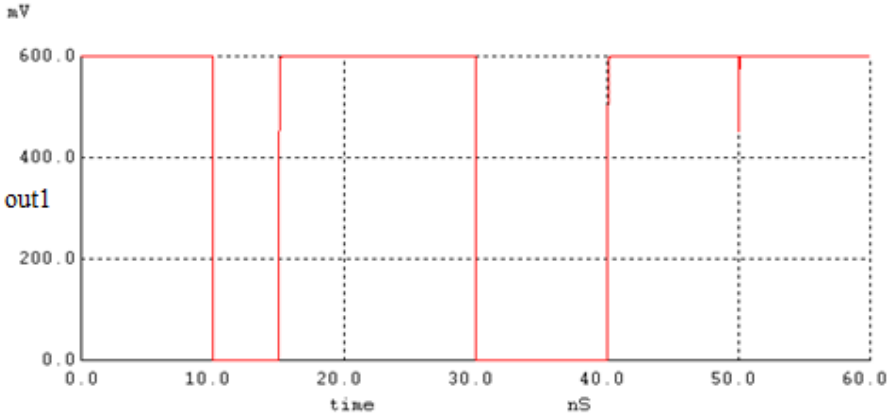

Figure 4.13(c): Output out1 of resistive loaded nano-MOSFET NAND logic gate

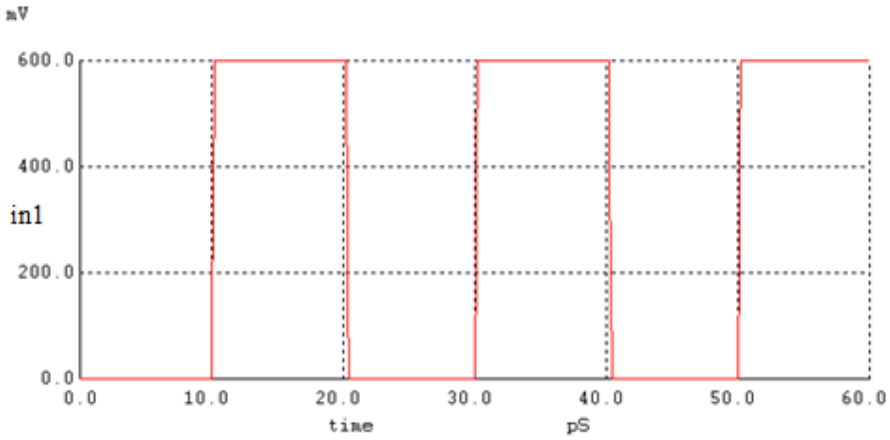

Figure 4.14(a): First input in1 to nano-MOSFET loaded nano-MOSFET NAND logic gate for transient analysis

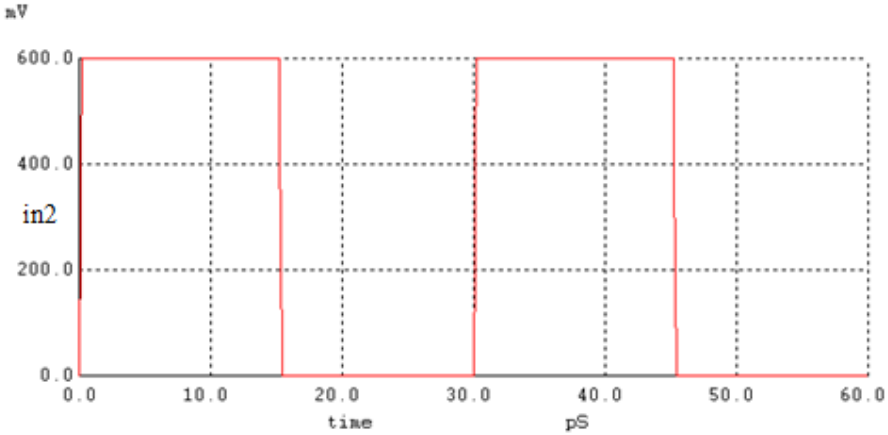

Figure 4.14(b): Second input in2 to nano-MOSFET loaded nano-MOSFET NAND logic gate for transient analysis

There is racing problem in output signal at time 50 ps of Figure 4.14(c). The glitch at 50 ps is due time constants. The simulated rise time constant is R_{load} x C_{total}=2.034x10^{-13} s whereas the simulated fall time constant is R_{on} x C_{total}=3.100x10^{-13} s. The theoretical rise time constant is 9.796x10^{-14} s and the theoretical fall time constant is 1.021x10^{-14} s. The ratio between simulated rise time constant to theoretical rise time constant is 2.08. The ratio between simulated fall time constant to theoretical fall time constant is 30.36. At 50 ps,

input in1 is at low to high transition and so the *n*-MOS start to turn on whereas input in2 is at low state and so the *n*-MOS turn off. Thereby, racing problem occurred at 50 ps.

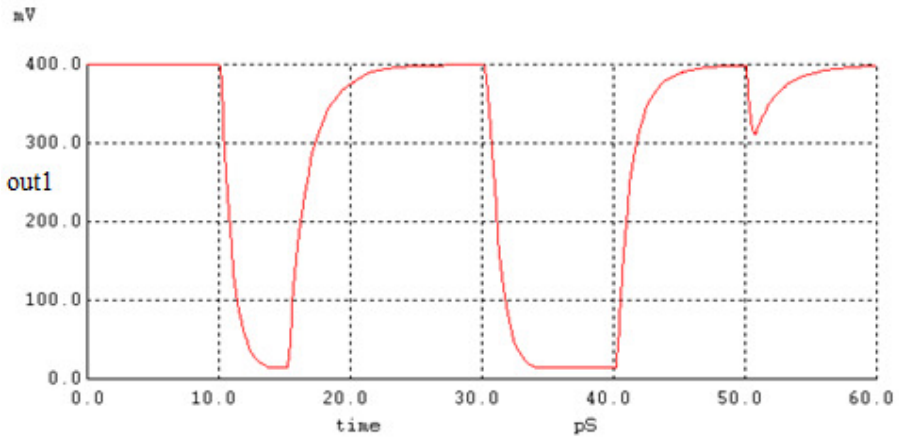

Figure 4.14(c): Output out1 signal of nano-MOSFET loaded nano-MOSFET NAND logic gate for transient analysis

Table 4.9: Theoretical value of nano-MOSFET loaded 2-input NAND logic gate.

Double Gate n nano-MOSFET Loaded NAND Gate	
Gate Capacitance (C_G)	5.755×10^{-17} F
Area Capacitance (C_A)	1.612×10^{-19} F
Sidewall Capacitance (C_{SW})	6.072×10^{-17} F
Total Drain Capacitance (C_D)	4.604×10^{-18} F
Total Source Capacitance (C_S)	1.046×10^{-17} F
nano-MOSFET Loaded Resistance (R_{load})	733.8 Ω
nano-MOSFET on-state Resistance (R_{on})	36.2 Ω
Loaded NAND2 Gate Total Capacitance at Output Node (C_{total})	1.335×10^{-16} F
Total Capacitance between Two nano-MOSFETs Connection (C_{SD})	1.507×10^{-17} F
Rise Time Constant (τ_r)	9.796×10^{-14} s
Rise Time (t_r)	1.314×10^{-12} s
Fall Time Constant (τ_f)	1.021×10^{-14} s
Fall Time (t_f)	2.246×10^{-14} s
Propagation Delay (t_p)	3.749×10^{-14} s
Maximum Signal Frequency (f_{max})	7.478×10^{11} Hz

Table 4.10: Theoretical derived timing characteristic of 2 input NAND logic gate

Theoretical Modeling Calculations from NanoMOS Device Simulation Data (10% and 90% Points)				
Logic Gates	Rise Time (t_r)	Fall Time (t_f)	Propagation Delay (t_p)	Maximum Operating Frequency (f_{max})
NAND	1.31×10^{-12} s	2.25×10^{-14} s	3.75×10^{-14} s	7.48×10^{11} Hz

Table 4.11: Simulated value of timing characteristic of 2 input NAND logic gate

WinSpice Simulation Results Using Model Level MOS6 (10% and 90% Points)				
Logic Gates	Rise Time (t_r)	Fall Time (t_f)	Propagation Delay (t_p)	Maximum Operating Frequency (f_{max})
NAND	2.73×10^{-12} s	68.18×10^{-14} s	1.80×10^{-13} s	2.93×10^{11} Hz

Table 4.12 tabulates the power dissipation for two different NAND logic gates calculated using equation of (2.23). When compared with logic gate designed using MOSFET with width, W=1 µm, length, L=120 nm and thickness, T_{Si} = 60 nm, which has a downscaled power dissipation of 140.9 µW range as reported by K. Naskar, et al., 2012, the two power dissipation in Table 4.12 showed reduction during down scaling nano-MOSFET to nanometer regime. This is equivalent to power reduction of 31.24 when compared to nano-MOSFET loaded NAND circuit (P. A. Gowri Sankar and K. Udhayakumar, 2014; Ulrich Wulf, et al., 2011).

Table 4.12: Power dissipation of two different 2 input NAND logic gate

	nano-MOSFET loaded NAND	Resistive loaded NAND
Power Dissipation (Watts)	4.51×10^{-6}	1.55×10^{-7}
Voltage Supply (Volts)	0.6	0.6
Frequency of switching (Hertz)	5.00×10^{11}	5.00×10^{11}

Comparison is carried out between the two NAND logic gates in term of power dissipation. By using WinSpice circuit simulator, simulated power dissipation and propagation delay for nano-MOSFET loaded NAND logic gate are reported to be 4.51 μW and 180 fs respectively. The analysis done here has confirmed that nano-MOSFET can be used as switching circuit that can fulfill the requirement of lower power dissipation and higher speed NAND logic gate (K. Navi, et al., 2010).

4.2.4 Combinational Logic Gate

This section is devoted to present the simulation result for 3 inputs combinational logic gate with Boolean expression $\overline{x(y+z)}$. Two types of combinational logic gates are studied, namely (i) nano-MOSFET loaded MOSFET logic gate (refer to Figure 2.8) and (ii) resistive loaded MOSFET logic gate (refer to Figure 4.15). The theory of nano-MOSFET loaded MOSFET combinational logic gate is covered in section 2.4.4 in chapter 2. The timing characteristics investigated include rise time, fall time and

propagation delay. Theoretical values of these timing characteristics are compared with simulated value using WinSpice.

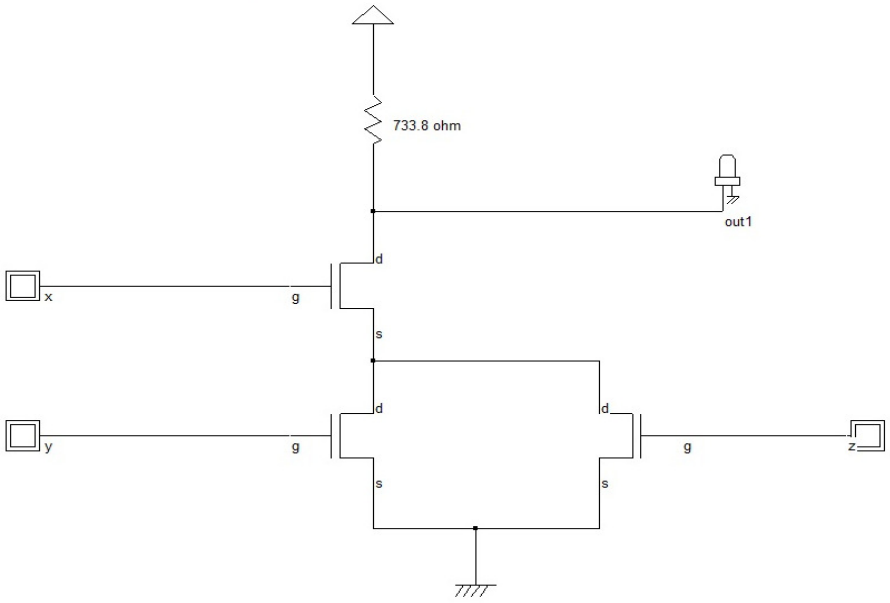

Figure 4.15: Three inputs resistive loaded nano-MOSFET combinational logic gate with Boolean expression $\overline{x(y+z)}$

Figure 4.16(a), Figure 4.16(b), Figure 4.16(c) and Figure 4.16(d) are the input and output signals to logic gate at Figure 2.8. The first input signal has a period of 40 ns with duty cycle 50% and amplitude of 0.6 V. The second input signal has a period of 20 ns with duty cycle 50% and amplitude of 0.6 V. The third input signal has a period of 60 ns with duty cycle 50% and amplitude of 0.6 V. The output signal has amplitude of 0.4 V due to threshold voltage loss of 0.2 V at the load nano-MOSFET which acts as *n*-type pass transistor. The input and output signals show correct combinational logic gate operation with Boolean expression $\overline{x(y+z)}$ relationship as in Table 2.1 in section 2.4.4. Figure 4.17(a), Figure 4.17(b), Figure 4.17(c) and Figure 4.17(d) are the input and output signals to logic gate at Figure 4.15. The first input

signal has a period of 40 ns with duty cycle 50% and amplitude of 0.6 V. The second input signal has a period of 20 ns with duty cycle 50% and amplitude of 0.6 V. The third input signal has a period of 60 ns with duty cycle 50% and amplitude of 0.6 V. The output signal has amplitude of 0.6 V. The input and output signals also show correct combinational logic gate operation with Boolean expression $\overline{x(y+z)}$ relationship as in Table 2.1. Figure 4.18(a), Figure 4.18(b), Figure 4.18(c) and Figure 4.18(d) are the input and output signals which are used for transient analysis for logic gate at Figure 2.8. The first input signal has a period of 40 ps with duty cycle 50% and amplitude of 0.6 V. The second input signal has a period of 20 ps with duty cycle 50% and amplitude of 0.6 V. The third input signal has a period of 60 ps with duty cycle 50% and amplitude of 0.6 V. The output signal has amplitude of 0.4 V due to threshold voltage loss of 0.2 V at the load nano-MOSFET which acts as *n*-type pass transistor. The simulated fall time is 0.692 ps and rise time is 2.692 ps with period 120 ps which is equivalent to pulse width 70 ps (58.33% duty cycle). The theoretical calculated propagation delay is 0.034 ps as tabulated in Table 4.13. The simulated propagation delay is 0.180 ps as measured from WinSpice output result. Therefore, the theoretical switching speed is 5.22 times that of simulated value. From Table 4.13 and Table 4.15, the theoretical maximum frequency of operation is around 758 GHz whereas the simulated maximum frequency of operation is 295 GHz. The percentage of error between these two values is 61%. All of these frequencies are higher than operation frequency of 65 nm MOSFET circuits which is around 300 GHz as reported by J. Sharma and H. Krishnaswamy, 2013. This difference in percentage of error is due to; in theoretical calculation, quasi-ballistic transport

model is used whereas in Winspice simulation quantum corrected drift-diffusion model is used. Scattering events are more obvious in quantum corrected drift-diffusion model than quasi-ballistic transport model. So, theoretical quasi-ballistic model has shorter delay and hence faster frequency. Thus, high speed combinational logic gate designed with nano-MOSFET has been achieved. Table 4.13 tabulated the timing characteristic of nano-MOSFET loaded combinational logic gate with Boolean expression $\overline{x(y+z)}$. Table 4.14 and Table 4.15 tabulated the theoretical derived timing characteristics and WinSpice simulated timing characteristics, respectively.

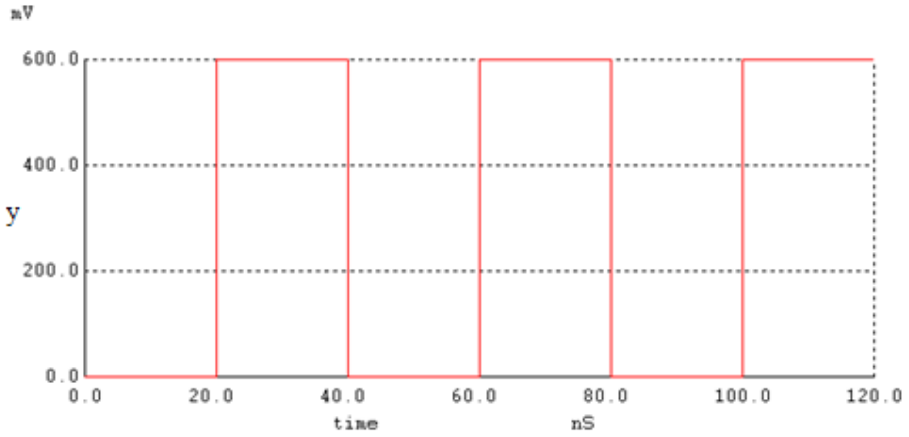

Figure 4.16(a): First input y to nano-MOSFET loaded nano-MOSFET combinational logic gate with Boolean expression $\overline{x(y+z)}$

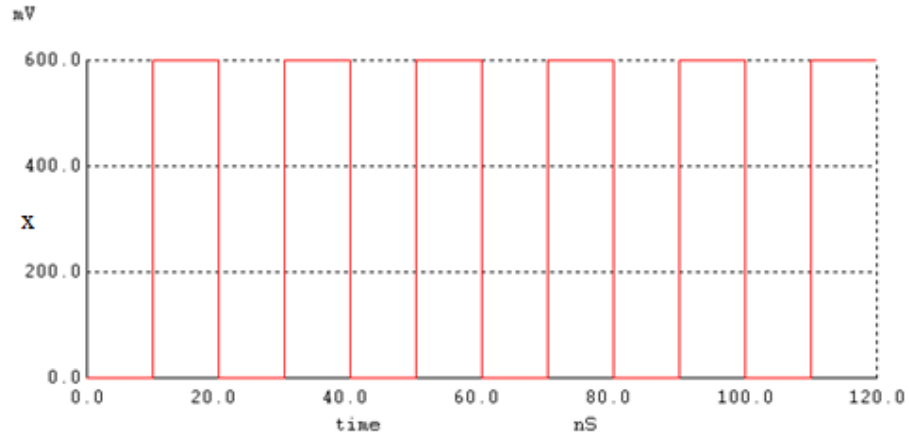

Figure 4.16(b): Second input x to nano-MOSFET loaded nano-MOSFET combinational logic gate with Boolean expression $\overline{x(y+z)}$

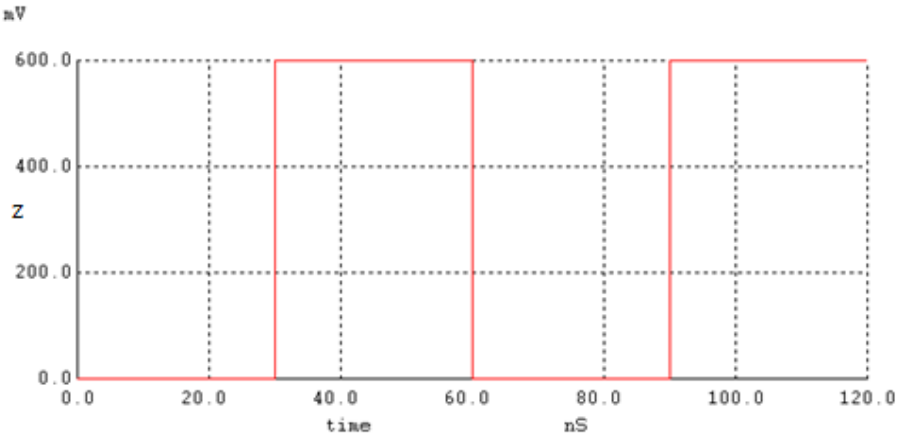

Figure 4.16(c): Third input z to nano-MOSFET loaded nano-MOSFET combinational logic gate with Boolean expression $\overline{x(y+z)}$

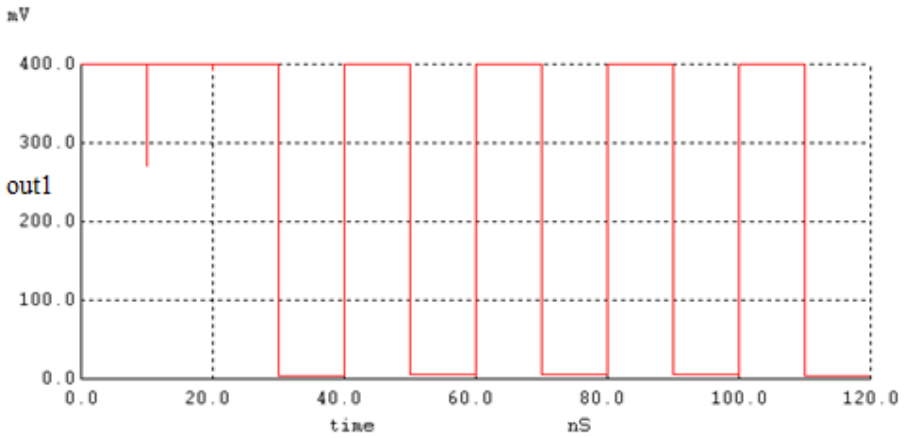

Figure 4.16(d): Output signal out1 of nano-MOSFET loaded nano-MOSFET combinational logic gate with Boolean expression $\overline{x(y+z)}$

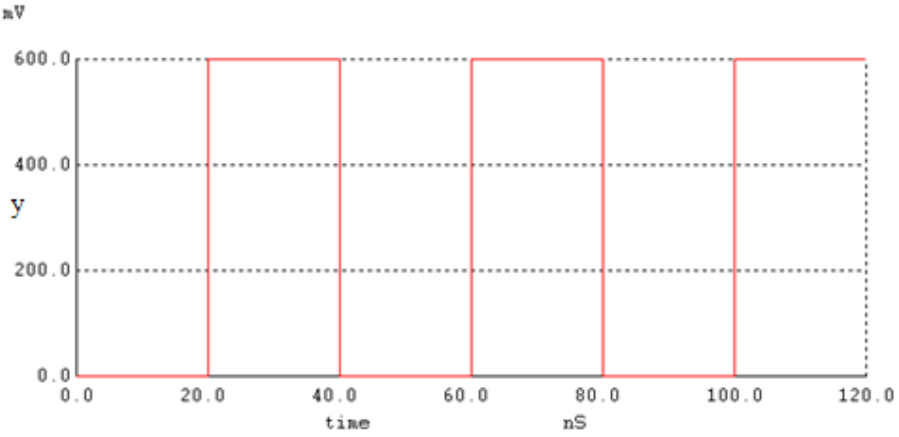

Figure 4.17(a): First input y to resistive loaded nano-MOSFET combinational logic gate with Boolean expression $\overline{x(y+z)}$

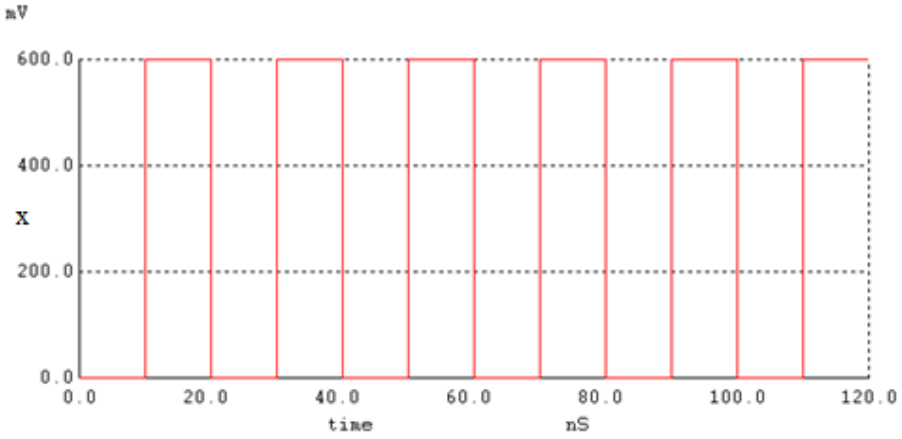

Figure 4.17(b): Second input x to resistive loaded nano-MOSFET combinational logic gate with Boolean expression $\overline{x(y+z)}$

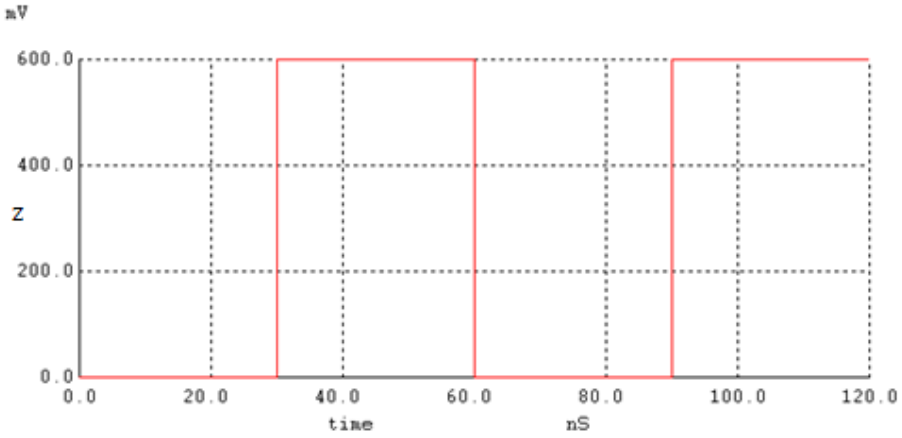

Figure 4.17(c): Third input z to resistive loaded nano-MOSFET combinational logic gate with Boolean expression $\overline{x(y+z)}$

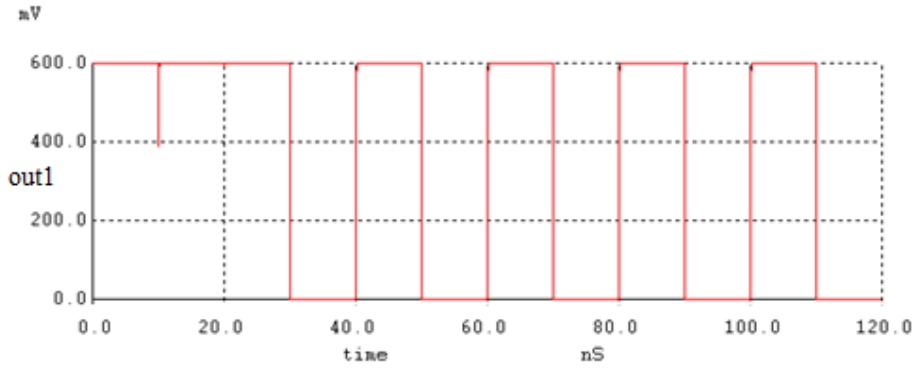

Figure 4.17(d): Output signal out1 of resistive loaded nano-MOSFET combinational logic gate with Boolean expression $\overline{x(y+z)}$

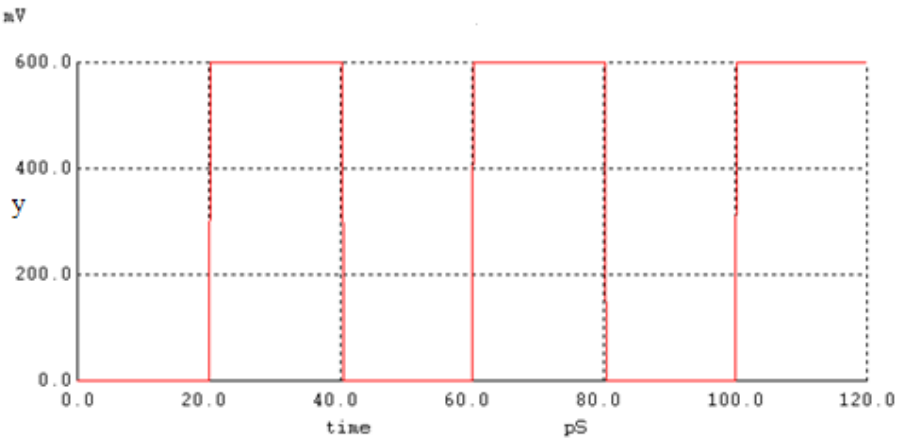

Figure 4.18(a): First input y to nano-MOSFET loaded nano-MOSFET combinational logic gate with Boolean expression $\overline{x(y+z)}$ for transient analysis

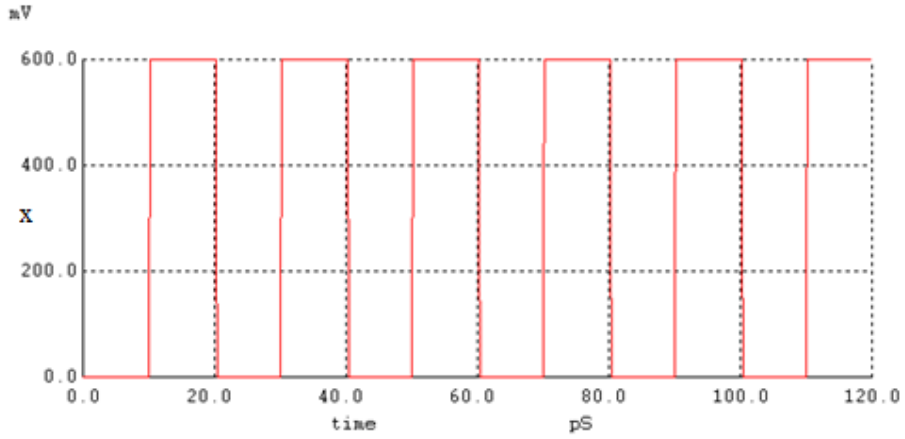

Figure 4.18(b): Second input x to nano-MOSFET loaded nano-MOSFET combinational logic gate with Boolean expression $\overline{x(y+z)}$ for transient analysis

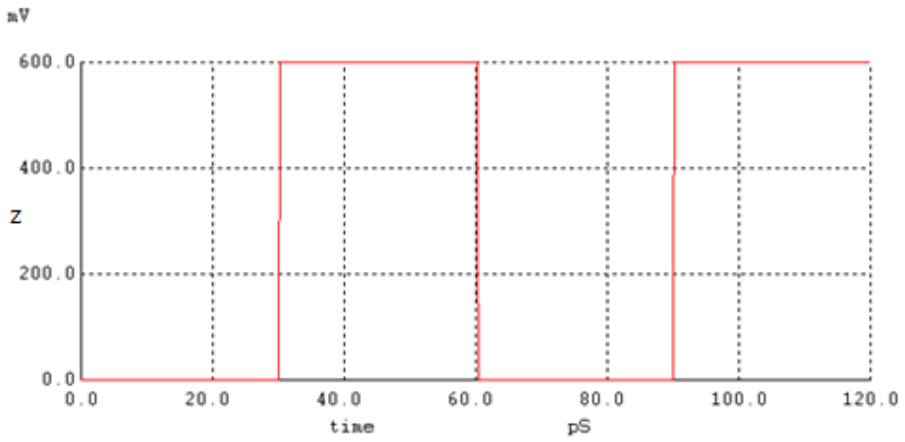

Figure 4.18(c): Third input z to nano-MOSFET loaded nano-MOSFET combinational logic gate with Boolean expression $\overline{x(y+z)}$ for transient analysis

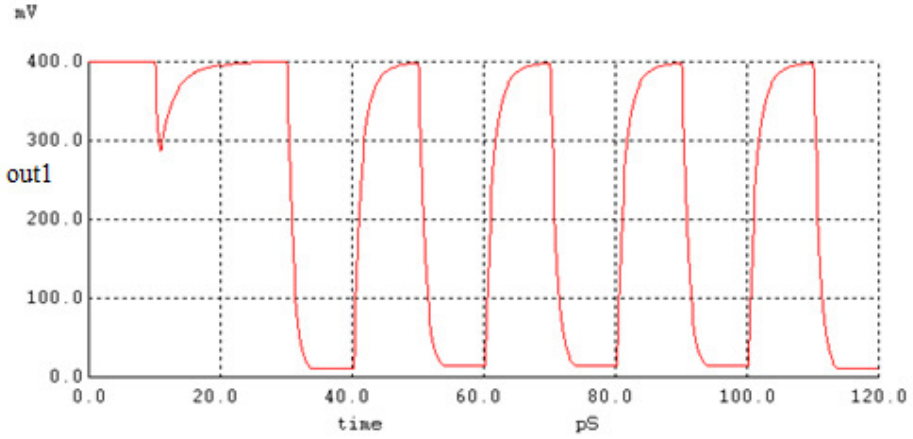

Figure 4.18(d): Output signal out1 of nano-MOSFET loaded nano-MOSFET combinational logic gate with Boolean expression $\overline{x(y+z)}$ for transient analysis.

There is racing problem in output signal at time 10 ps in Figure 4.18(d). It is caused by racing. The simulated rise time constant is R_{load} x C_{total} =2.00x10^{-13} s whereas the simulated fall time constant is R_{on} x C_{total}=3.15x10^{-13} s. The theoretical rise time constant is 9.796x10^{-14} s and the theoretical fall time constant is 1.803x10^{-15}. The ratio between simulated rise time constant to theoretical rise time constant is 2.04. The ratio between simulated fall time

constant to theoretical fall time constant is 174.65. At 10 ps, input y is at low state and so *n*-MOSFET turn off, while input x is at low to high transition and so *n*-MOSFET start to turn on, and input z is at low state, the *n*-MOSFET turn off. Thereby 10 ps portion has racing problem. The same situations occur in Figure 4.16(d) and Figure 4.17(d) at 10 ns.

Table 4.13: Theoretical value of nano-MOSFET loaded 3-input combinational logic gate with Boolean expression $\overline{x(y+z)}$.

Double Gate n nano-MOSFET Loaded Combinational Gate	
Gate Capacitance (C_G)	5.755×10^{-17} F
Area Capacitance (C_A)	1.612×10^{-19} F
Sidewall Capacitance (C_{SW})	6.072×10^{-17} F
Total Drain Capacitance (C_D)	4.604×10^{-18} F
Total Source Capacitance (C_S)	1.046×10^{-17} F
nano-MOSFET Loaded Resistance (R_{load})	733.8 Ω
nano-MOSFET on-state Resistance (R_{on})	36.2 Ω
Loaded Combinational Gate Total Capacitance at Output Node (C_{total})	1.335×10^{-16} F
Total Capacitance between Two nano-MOSFETs Connection (C_{SD})	1.967×10^{-17} F
Rise Time Constant (τ_r)	9.796×10^{-14} s
Rise Time (t_r)	1.314×10^{-12} s
Fall Time Constant (τ_f)	1.803×10^{-15} s
Fall Time (t_f)	3.967×10^{-15} s
Propagation Delay (t_p)	3.457×10^{-14} s
Maximum Signal Frequency (f_{max})	7.583×10^{11} Hz

Table 4.14: Theoretical derived timing characteristic of 3 input combinational logic gate with Boolean expression $\overline{x(y+z)}$

Theoretical Modeling Calculations from NanoMOS Device Simulation Data (10% and 90% Points)				
Logic Gates	Rise Time (t_r)	Fall Time (t_f)	Propagation Delay (t_p)	Maximum Operating Frequency (f_{max})
Combinational	1.31×10^{-12} s	3.97×10^{-15} s	3.46×10^{-14} s	7.58×10^{11} Hz

Table 4.15: Simulated value of timing characteristic of 3 input combinational logic gate with Boolean expression $\overline{x(y+z)}$

WinSpice Simulation Results Using Model Level MOS6 (10% and 90% Points)				
Logic Gates	Rise Time (t_r)	Fall Time (t_f)	Propagation Delay (t_p)	Maximum Operating Frequency (f_{max})
Combinational	2.69×10^{-12} s	69.23×10^{-14} s	1.80×10^{-13} s	2.95×10^{11} Hz

Table 4.16 tabulates the power dissipation for two different combinational logic gates with Boolean expression $\overline{x(y+z)}$ calculated using equation (2.24). When compared with logic gate designed using MOSFET with width, W=1 μm, length, L=120 nm and thickness, T_{Si} = 60 nm, which has a downscaled power dissipation of 140.9 μW range as reported by K. Naskar, et al., 2012, the two power dissipation in Table 4.16 showed reduction during down scaling nano-MOSFET to nanometer regime. This is equivalent to power reduction of 25.03 when compared to nano-MOSFET loaded combinational circuit (P. A. Gowri Sankar and K. Udhayakumar, 2014; Ulrich Wulf, et al., 2011).

Table 4.16: Power dissipation of two different 3 input combinational logic gates with Boolean expression $\overline{x(y+z)}$

	nano-MOSFET loaded Combinational logic	Resistive loaded Combinational logic
Power Dissipation (Watts)	5.63 x10^{-6}	1.94 x10^{-7}
Voltage Supply (Volts)	0.6	0.6
Frequency of switching (Hertz)	5.00 x10^{11}	5.00 x10^{11}

Comparison is carried out between the two combinational logic gates with Boolean expression $\overline{x(y+z)}$ in term of power dissipation. By using WinSpice circuit simulator, simulated power dissipation and propagation delay for nano-MOSFET loaded combinational logic gates with Boolean expression $\overline{x(y+z)}$ are reported to be 5.63 μW and 180.4 fs, respectively. The analysis done here has confirmed that nano-MOSFET can be used as switching circuit that can fulfill the requirement of lower power dissipation and higher speed combinational logic gates with Boolean expression $\overline{x(y+z)}$ (K. Navi, et al., 2010).

4.3 nano-MOSFET Logic Gates Simulation using HSPICE

This section is devoted to present the HSPICE simulation result. Only one type of logic family is simulated namely, resistive loaded nano-MOSFET logic gate. The logic gates simulated are NOT (refer to Figure 2.9), 2-input

NOR (refer to Figure 2.10), 2-input NAND (refer to Figure 2.11) and combinational logic with Boolean expression $\overline{x(y+z)}$ (refer to Figure 2.12). The theory of these logic gates simulation is covered in section 2.4.5 in chapter 2.

4.3.1 NOT Logic Gate

Figure 4.19 shows the input and output timing diagrams of 50 kΩ resistive loaded NOT MOSFET logic gate simulated using commercial HSPICE, an industrial standard circuit simulator. The *n*-type MOSFET used has width (W) equal to 500 nm and length (L) equal to 100 nm. The HSPICE library used is the 90 nm technology. The fall time is 42.20 ps and rise time is 67.60 ps with period 10 ns and pulse width 5 ns (50% duty cycle). The power supply used is 1.2 V. The propagation delay, which can be derived from simulated fall time and rise time, is 17.47 ps. The fall time is measured from 90% to 10% transition and the rise time is measured from 10% to 90% transition by using Wave Viewer software tool. The propagation delay is calculated from the simulated result using formulae stated in section 2.4.5.

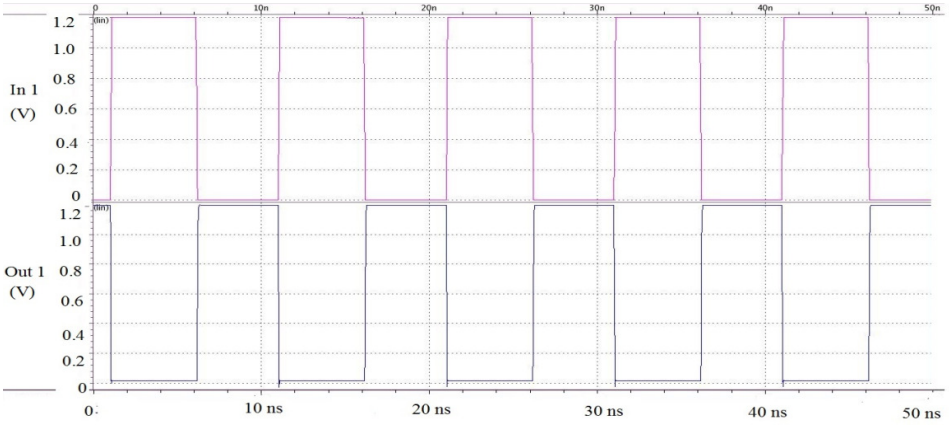

Figure 4.19: Input and output signal timing diagram of 50 kΩ resistive loaded NOT logic gate simulated using HSPICE.

4.3.2 NOR Logic Gate

Figure 4.20 shows the two input and one output timing diagrams of 50 kΩ resistive loaded NOR MOSFET logic gate simulated using commercial HSPICE, an industrial standard circuit simulator. Both the *n*-type MOSFETs used have width (W) equal to 500 nm and length (L) equal to 100 nm. The HSPICE library used is the 90 nm technology. The first input signal has period 10 ns with pulse width 5 ns (duty cycle 50%) and the second input signal has period 20 ns with pulse width 10 ns (duty cycle 50%). The power supply is 1.2 V. The fall time is 42.20 ps and rise time is 109 ps. The propagation delay, which can be derived from simulated fall time and rise time, is 24.05 ps. The fall time is measured from 90% to 10% transition and the rise time is measured from 10% to 90% transition by using Wave Viewer software tool. The propagation delay is calculated from the simulated result using formulae stated in section 2.4.5.

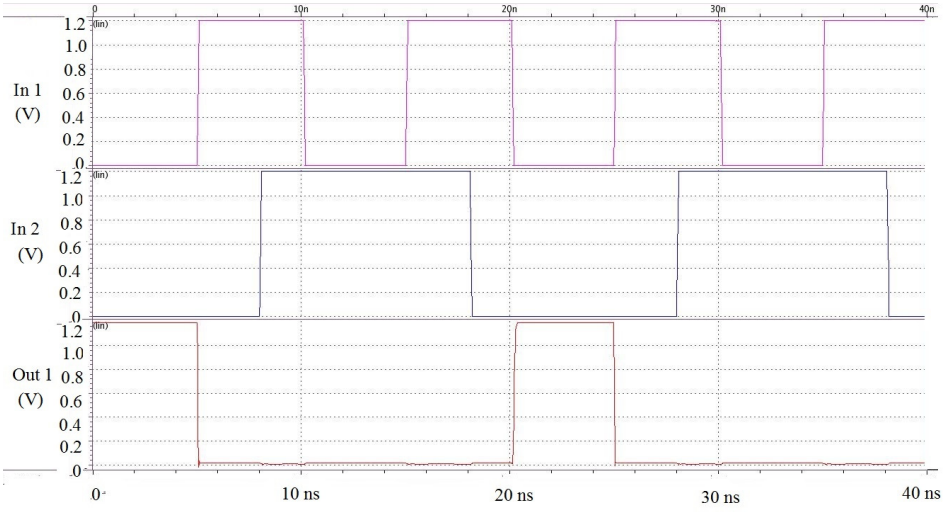

Figure 4.20: Input and output signal timing diagram of 50 kΩ resistive loaded NOR logic gate simulated using HSPICE.

4.3.3 NAND Logic Gate

Figure 4.21 shows the two input and one output timing diagrams of 50 kΩ resistive loaded NAND MOSFET logic gate simulated using commercial HSPICE, an industrial standard circuit simulator. Both the *n*-type MOSFETs used have width (W) equal to 1.0 µm and length (L) equal to 0.1 µm. The HSPICE library used is the 90 nm technology. The first input signal has period 10 ns with pulse width 5 ns (duty cycle 50%) and the second input signal has period 20 ns with pulse width 10 ns (duty cycle 50%). The power supply is 1.2 V. The fall time is 42.30 ps and rise time is 109 ps. The propagation delay, which can be derived from simulated fall time and rise time, is 24.07 ps. The fall time is measured from 90% to 10% transition and the rise time is measured from 10% to 90% transition by using Wave Viewer software tool. The propagation delay is calculated from the simulated result using formulae stated in section 2.4.5. At 7ns, In 1 is at low to high transition and In 2 is at

low state and thereby glitch occur. At 20 ns, In 1 is at high to low transition and In 2 is at low state and thereby a glitch happened. At 27 ns, In 1 is at low to high transition, In 2 is at low state and thereby a glitch occurred.

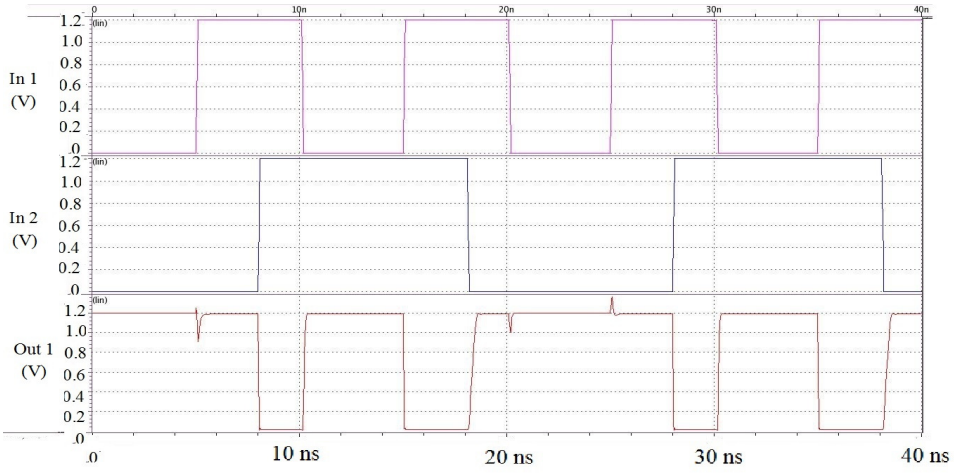

Figure 4.21: Input and output signals timing diagram of 50 kΩ resistive loaded NAND logic gate simulated using HSPICE.

4.3.4 Combinational Logic Gate

Figure 4.22 shows the three input and one output timing diagrams of 50 kΩ resistive loaded combinational MOSFET logic gate simulated using commercial HSPICE, an industrial standard circuit simulator. All the *n*-type MOSFETs used have width (W) equal to 1.0 µm and length (L) equal to 0.1 µm. The HSPICE library used is the 90 nm technology. The first input signal has period 10 ns with pulse width 5 ns (duty cycle 50%). The second input signal has period 20 ns with pulse width 10 ns (duty cycle 50%). The third input signal has period 30 ns with pulse width 15 ns (duty cycle 50%). The power supply is 1.2 V. The fall time is 43.70 ps and rise time is 109 ps. The propagation delay, which can be derived from simulated fall time and rise time, is 24.29 ps. The fall time is measured from 90% to 10% transition and

the rise time is measured from 10% to 90% transition by using Wave Viewer software tool. The propagation delay is calculated from the simulated result using formulae stated in section 2.4.5.

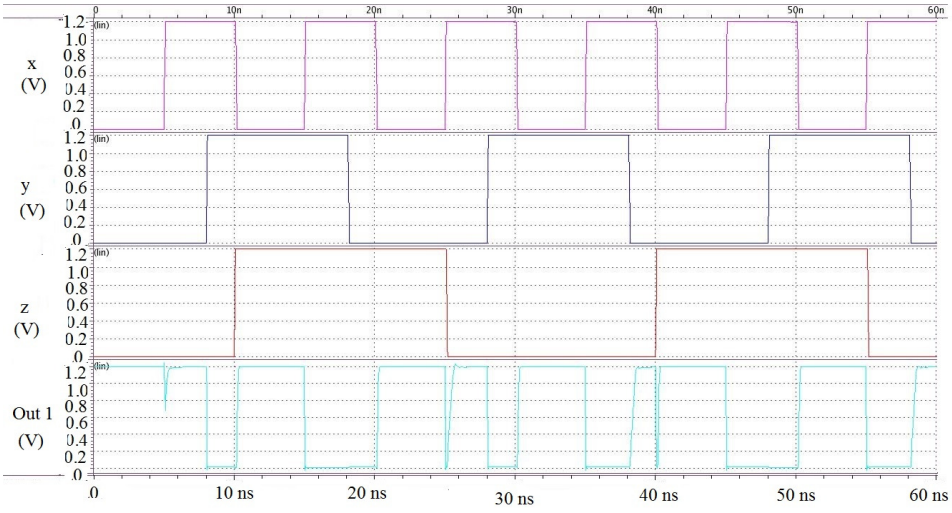

Figure 4.22: Input and output signals timing diagram of 50 kΩ resistive loaded combinational logic gate with Boolean expression $\overline{x(y+z)}$ simulated using HSPICE.

4.3.5 High Speed Improvement of Nano-MOSFET Logic Gates

The propagation delay of various logic gates with MOSFET channel 45 nm and 10 nm are benchmarked. The data for channel length 45 nm is obtained from the work of M. L. P. Tan, et al., 2012. Meanwhile, the data for channel length 10 nm is collected by performing WinSpice simulation.

The theory which is used to extract these data for Table 4.17 is when nano-MOSFET is down scaling by a scaling factor *s*, the propagation delay is downscaled by the same scaling factor *s*.

Table 4.17 tabulates the propagation delay of logic gates when downscaling from channel length 45 nm to 10 nm and voltage from 1.0 V to 0.6 V with scaling factor 0.133 by using voltage scaling. Both nano-MOSFETs have the same width equal to 125 nm. This table shows that propagation delay of all logic gates become smaller when channel length is downscaled. The ratio between propagation delay at 45 nm to propagation delay at 10 nm are 8.06, 10.95 and 6.47 for NOT, NOR and NAND, respectively. Thus, higher speed logic gates are achieved during downscaling of nano-MOSFET. The power dissipation of 45 nm logic gates can be calculated using equation (2.21), (2.22) and (2.23) with the following HSPICE setting: (i) C=164 aF, *f*=500 GHz and V_{DD}=1.0 V for NOT logic gate, (ii) C=183 aF, *f*=500 GHz and V_{DD}=1.0 V for NOR logic gate, and (iii) C=164 aF, *f*=500 GHz and V_{DD}=1.0 V for NAND logic gate. From these HSPICE simulation result, the calculated power dissipation values are 20.4 µW, 17.1 µW and 15.3 µW for NOT, NOR and NAND, respectively.

Table 4.17: Benchmarking between L= 45 nm logic gates against L=10 nm logic gates

MOSFET with 45 nm nano-MOSFET with 10 nm				
Logic Gate	Propagation Delay,t_p (s)	Logic Gate	WinSpice Simulated Propagation Delay, t_p (s)	Delay (s) Downscaled from 45 nm Result Based on Voltage Scaling Theory
NOT	5.005×10^{-12}	NOT	8.276×10^{-14}	6.673×10^{-13}
NOR	8.797×10^{-12}	NOR	1.071×10^{-13}	1.173×10^{-12}
NAND	8.719×10^{-12}	NAND	1.796×10^{-13}	1.163×10^{-12}
Combinational	N/A	Combinational	1.804×10^{-13}	N/A

4.4 Summary

In this chapter, the optimized parameter nano-MOSFET obtained from chapter 3 is used to design logic circuits and then these logic circuits are simulated using circuit simulators to obtain their ac and dc characteristics. All simulation results of each logic circuit showed correct logical operations. Theoretical derived timing characteristics have a good agreement with simulated derived timing characteristics. The ac parameters which have been analyzed and discussed in this chapter are rise time, fall time and propagation delay. The dc parameters which have been analyzed and discussed in this chapter are V_{OH}, V_{OL}, V_{IH}, V_{IL}, V_M, V_{LS}, V_{TW},V_{NMH}, V_{NML}, V_{NSH}, V_{NSL} , V_{NIH} and V_{NIL}. After analyzing simulation results, the logic circuits designed using nano-MOSFETs showed lower power dissipation and also enhanced speed both due to shrinking size of nano-MOSFETs.

The propagation delay of 10 nm nano-MOSFET loaded NOT, NOR, NAND and combinational logic gates when simulated with WinSpice are 0.082 ps, 0.107 ps, 0.180 ps and 0.181 ps respectively. The downscaled propagation delay of 45 nm to 10 nm and 1.0 V to 0.6 V, that is with scaling factor 0.133, nano-MOSFET NOT, NOR and NAND logic gates when simulated with HSPICE are 0.667 ps, 1.173 ps and 1.163 ps, respectively. The ratio between HSPICE simulated to WinSpice simulated propagation delay ratio for 10 nm nano-MOSFET NOT, NOR and NAND logic gates are 8.06, 10.95 and 6.47, respectively. The HSPICE simulation used drift diffusion transport whereas the WinSpice simulation used quantum-corrected drift

diffusion which has lesser scatterings and so WinSpice simulated propagation delays are smaller. This indicates high speed logic gates due to shrinking size of nano-MOSFET. The power dissipation of 10 nm nano-MOSFET loaded NOT, NOR, NAND and combinational logic gates when simulated with WinSpice are 6.01 μW, 4.66 μW, 4.51 μW and 5.63 μW, respectively. The power dissipation of 45 nm nano-MOSFET loaded NOT, NOR and NAND logic gates when simulated with HSPICE are 20.4 μW, 17.1 μW and 15.3 μW, respectively. This indicates lower power dissipation logic gates due to shrinking size of nano-MOSFET. After these two simulation measurements, a category of lower power dissipation and higher speed logic gates are produced by using 10 nm nano-MOSFETs.

CHAPTER FIVE

CONCLUSION

The goals of this thesis are to characterize the quantum effect and electrical quantities of an optimized nano-MOSFET parameters formulated by Purdue University and then to evaluate the logical operations and ac and dc characteristics of logic gates designed using the optimized parameters nano-MOSFET. The device optimization is carried out using device simulator. The nano-MOSFET parameters involved include channel thickness, temperature, gate contact work function, gate underlap, intrinsic channel and gate length. In performing device simulation, only one parameter is varied at a time while the others are fixed. In logic gates simulations, timing characteristics such as rise time, fall time and propagation delay and dc parameters are derived. After performing both types of simulation, a category of lower power dissipation and high speed logic gates designed from nano-MOSFET is realized. The speed enhancement is justified by benchmarking HSPICE simulation results of 45 nm with WinSpice simulation results of 10 nm.

This research has achieved the objectives of designing logic gates with the optimized nano-MOSFET and characterizing for their ac and dc parameters. The ac parameters which have been analysed and discussed in this thesis are rise time, fall time and propagation delay. The dc parameters which have been analysed and discussed are V_{OH}, V_{OL}, V_{IH}, V_{IL}, V_M, V_{LS}, V_{TW},V_{NMH},

V_{NML}, V_{NSH}, V_{NSL} , V_{NIH} and V_{NIL}.The final optimized parameters of the nanoMOSFET are channel thickness of 1.5 nm, temperature of 300 K, gate contact work function of 4.188 eV, no gate underlap, gate length of 10 nm and intrinsic channel. The criteria used to justify the above device optimization are low threshold voltage of 0.20 V, ballistic efficiency of 0.96 and low leakage current of 5.312×10^{-2} μA/μm. The value of lower power dissipation and shorter propagation delay of logic gates achieved are in the range of microwatts (μW) and femtosecond (fs), respectively.

In future work, the study on the characteristics *p*-channel nano-MOSFET can be done so that it can combine with *n*-channel nano-MOSFET to design and characterize nano-complimentary MOSFET (nano-CMOS) logic gates. The carriers in *n*-channel nano-MOSFET are electrons whereas the carriers in *p*-channel nano-MOSFET are holes. Nano-CMOS logic gates are used because they have the advantages of low power dissipation, high speed and no threshold voltage loss as compared with *n*-channel nano-MOSFET loaded logic gates. Moreover, fabrication of nano-CMOS logic gates can benefit from the current stable existing fabrication process technology.

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