CMOS LOW POWER ANALOGUE ADDER

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A project report submitted in partial fulfilment of the requirements for the award of Bachelor of Engineering (Honours) Electrical and Electronic Engineering

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DECLARATION

I hereby declare that this project report is based on my original work except for citations and quotations which have been duly acknowledged. I also declare that it has not been previously and concurrently submitted for any other degree or award at UTAR or other institutions.

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APPROVAL FOR SUBMISSION

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Date : 17/5/2020

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ABSTRACT

As the world moves forward into the realm of artificial intelligence (AI), obstacles and challenges keep on popping up along the road. For digital circuit, the main improvement comes in the form of MOSFET downsizing, which will eventually reach a limit. Thus, it is believed that analogue is the way forward to tackle these big challenges. Design of a CMOS low power analogue adder that computes the sum of two analogue inputs voltages is described. In this project, different adder designs are studied and compared. An analogue adder design with low power techniques are proposed which satisfies the parameters of power dissipation less than $1mW$, time delay less than $10ps$ and output accuracy greater than 90%. The main focus of the proposed design is on power dissipation and performance. The proposed design utilises the current mode technique as its operational principle, where the inputs voltages are converted to current forms and sum together before converting back to voltage forms. Complementary input pairs and input offset voltage are needed to the proposed design to perform correctly and for the best performance, the inputs voltages must even. In order to reduce the power dissipation, addition MOSFETs are added to the design to limit the current, which reduced the power dissipation by almost 10 times form its original values. The proposed design is constructed and simulated using SAED $90nm$ process technology in Synopsys custom compiler. The proposed design is able to handle input voltage up to $\pm 1.5V$ and the output of the design has an accuracy greater than 90%. The accuracy is not able to achieve 100% accuracy due to the current flow accuracy. The layout design of the proposed design is optimized and has a layout area of $22.628\mu m^2$. The power dissipation of the proposed design is dependent on the input voltages, and the maximum recorded power dissipation is $574\mu W$ with $\pm 1.5V$ input voltages. For future work, offset compensation can be implemented to improve the design accuracy and smaller technologies process can improve the overall performance of the design.

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LIST OF SYMBOLS / ABBREVIATIONS

I_D	drain current
P_d	power dissipation
t_d	time delay
SiO	silicon oxide
V_{DD}	drain voltage
V_{DS}	drain to source voltage
V_g	gate voltage
V_{GS}	gate to source voltage
V_{SS}	source voltage
V_s	switching voltage

ADC	analogue to digital converter
AI	artificial intelligence
ALU	arithmetic logic unit
ASIC	application specific integrated circuit
CMOS	complementary metal-oxide-semiconductor
C_{IN}	carry in
C_{OUT}	carry out
DRC	Device Rule Check
DSP	digital signal processing
EDA	electrical design automation
EEPROM	Electrically Erasable Programmable Read-only Memory
EPROM	Erasable Programmable Read-only Memory
FA	full adder
IC	integrated circuit
KCL	Kirchhoff’s Current Law
LPE	Layout Parasitic Extraction
LVS	Layout vs Schematic test
NMOS	n-channel field-effect transistors
PMOS	p-channel field-effect transistors

PTL	pass transistor logic
RCA	ripple carry adder
RTL	register transfer level
SAE	simulation and analysis environment
VLSI	very-large-scale integration

CHAPTER 1

INTRODUCTION

1.1 CMOS Technology

In the mid-1980s, the integrated circuit (IC) technologies available at that period were n-channel field-effect transistors (NMOS), bipolar and complementary metal-oxide-semiconductor (CMOS) designs. CMOS technology quickly gained popularity over others, as the power dissipation of other technologies scaled with their complexity, whereas CMOS only dissipated power when the output was transitioning, instead of all the time. (Horowitz, 2008). Fast forward to the present day, CMOS technology is one of the most widely used IC fabrication technology around the world, IC is used in many electronic applications and embedded systems. Devices surrounding our life: computers, smartphones, tablets, home appliances, assistant devices, and entertainment devices, require an IC chip to operate. (Jiang *et al.*, 2010).

As the name suggested, CMOS technology uses both p-channel and n-channel field-effect transistors (PMOS and NMOS transistors) as the main components to fabricate IC, NMOS utilizes its majority carriers, electrons and PMOS utilizes its majority carriers, holes. Figure 1-1 shows a basic CMOS device structure commonly used, the gate, drain, source and bulk connection are not shown to simplify the device structure. The transistor channel length, *L* and the channel width, *W* shown on the NMOS are important design parameters when selecting a suitable CMOS process. (Bruun, 2018).

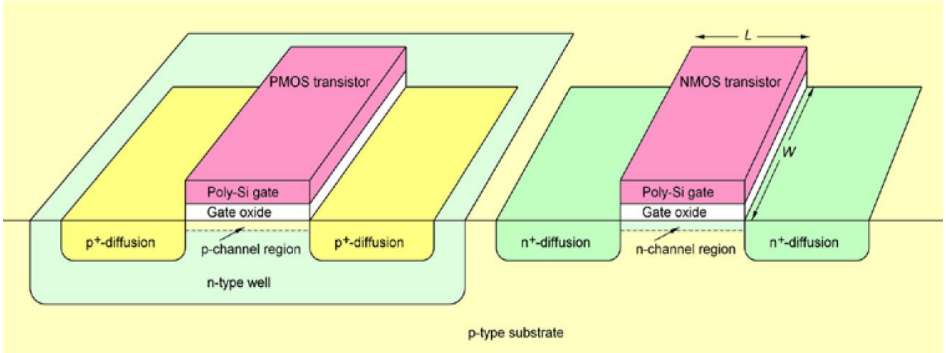

Figure 1-1: CMOS device structure. (Bruun, 2018).

A CMOS integrated circuit performance depends on many factors, a major factor is the mobility of the electrons and holes. The mobility for both the electrons and holes should be high to intensify the performance of both the PMOS and NMOS, thus enhancing the CMOS integrated circuit performance. (Armstrong *et al.*, 2007). The advantages of CMOS technology are the usage of both PMOS and NMOS transistors reduces the digital circuit design complexity and the size of the transistors used, scale down as the fabrication technology improves. The size reduction of the transistors allows more transistors to be packed in an IC without increasing its size and improving the speed and power characteristics of the IC. (Bruun, 2018).

1.2 Analogue Adder

Digital devices or electronic applications operate by taking in inputs and processing it through an Arithmetic Logic Unit (ALU) to produce the outputs. In the ALU, the inputs undergo arithmetic operations to create the desired outputs. Adder is a digital circuit used to perform addition of number, since addition is one of the most fundamental operations used in a digital system, adders are used in ALU, general microprocessor and digital signal processor. (Nagaraj *et al.*, 2017).

An adder performs the addition operation of multiple inputs and the output is the sum. A digital adder or better known as Full Adder are bitwise, each adder can only operate for one-bit, thus they only have two inputs. Figure 1-2 shows the block diagram and schematic of a typical Full Adder. Multiple Full Adders are cascaded in series to create a logic circuit for multiple bits addition, each Full adder inputs a C_{IN} from previous adder C_{OUT} as shown in Figure 1-3. (Rashmi *et al.*, 2016).

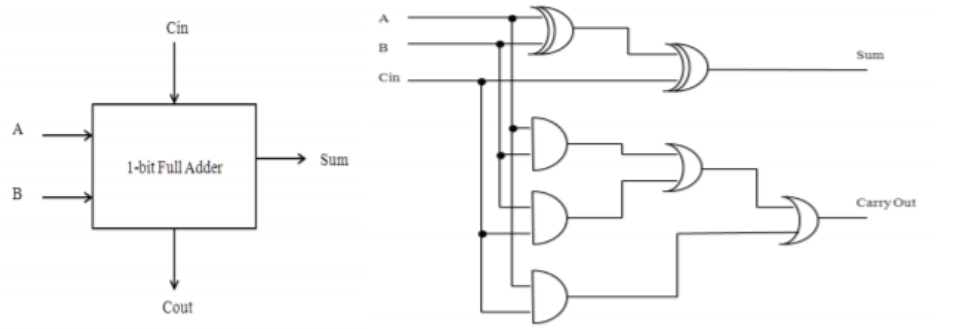

Figure 1-2: Block diagram and schematic of a Full Adder. (Rashmi *et al*., 2016).

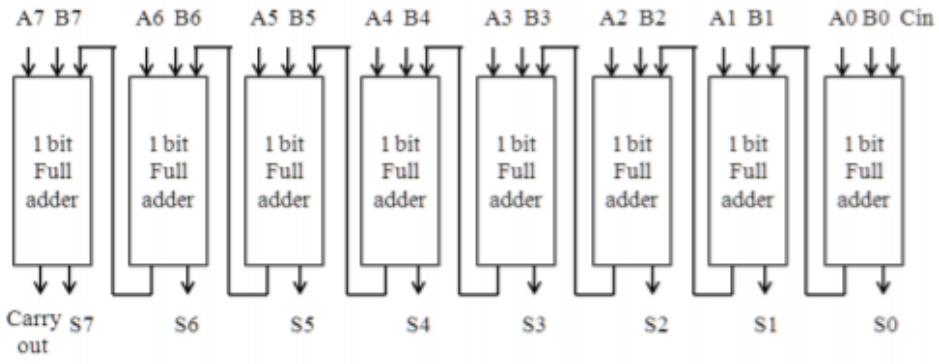

Figure 1-3: Block diagram of an 8-bit Adder. (Rashmi *et al*., 2016).

An analogue adder indicates that the inputs taken in by the adder are not digital but in analogue forms and unlike digital adder then can have multiple inputs. Therefore, the transistors could have an infinite number of states, which allow for an infinite range of mathematical value. Analogue adders are important and widely used in analogue computing, which models a certain problem by adapting to their structure and internal relations, unlike the algorithmic approach used in digital computing.

Since most natural signals are in analogue forms, many applications need an analogue to digital converter (ADC) to convert these signals to digital forms before sending them to any operation. This is an additional step that can be avoided with analogue system, which can directly operate with the natural signal. Normally, an analogue adder operates using an operational amplifier or resistive adder circuit.

1.3 Problem Statement

In the early 1980s, many experts predicted and speculated that analogue circuits will become absolute and eventually demise. During that period, digital signal processing algorithms were becoming more powerful and were easily implemented in integrated circuit (IC). (Razavi, 2005). Fast forward to the present day, the majority of computing and processing are done in digital forms but analogue circuits are gaining momentum.

In the word where almost, everything is in digital forms and analogue has no place to stand, digital is almost reaching its limit. As the world moves towards artificial intelligence (AI), challenges continue to arise where it gets harder and harder for digital signal processing to solve. According to Gene Frantz, a well-known person in the field of digital signal processing (DSP), he thinks that analogue is the way forward in solving the problems faced in AI. (Dahad,2019). Since analogue circuits provide advantages over digital circuits and natural signals are in analogue forms, analogue circuits should be the superior choice for future circuits. Furthermore, advancement in analogue technology has shortened the gap between analogue and digital, with active filter analogue signals are less prone to noise distortion and accuracy and linearity of the analogue signal have greatly been improved. Table 1-1 summarizes the differences between digital circuits and analogue circuits.

Table 1-1: Comparison between digital and analogue circuits.

Features	Digital Circuits	Analogue Circuits
Power Dissipation	Low	Lower
Operation Speed	Fast	Faster
Design Complexity	Simple	Complex
Input Levels	2	Variety
Noise Distortion	Immune	Highly
Accuracy and Linearity	High	Low
Reliability	High	Low

MOSFET downsizing is one of the most well known and commonly used technique to reduce the power dissipation, the power dissipated and improve performance of CMOS circuit, but there is a limit to how much a MOSFET can be shrunk. Previously, there were many downsizing limits predicted but most

were proven wrong. In recent years, MOSFET size had shrunk dramatically and it is expected that problems will arise when implementing small-geometry MOSFETs into large scale IC, problems such as reliability, yield, and current drive might surface. (Iwai, 2006).

To prove that analogue could hold its ground against digital or even surpassing it, a circuit of both types must be compared. Adder is one of the most basic components in a digital system, thus there will be an abundance of different adder designs to compare to an analogue adder.

1.4 Aim and Objectives

For the purpose of proving analogue circuit design is the way forward, a circuit designed in analogue must provide similar or better results than an identical circuit designed in digital. The main aim of the project is to design a low power CMOS analogue adder. Different methods and techniques of IC design are implemented to improve the analogue adder design performance and power dissipation.

The objectives of the project are shown below:

1) Compare different adder design schematic performance.
2) Propose an analogue adder design which satisfies the following parameters:
    - Power dissipation < $1mW$
    - Time delay < $10ps$
    - Output accuracy > 90%
3) Optimize layout design to reduce the layout area to less than $30\mu m^2$.
4) Apply low power techniques on the design to lower the power dissipation and increase performance.

1.5 Scope and Limitation of the Study

The project can be divided into three major parts, which are the main focuses and intentions. The three major parts are to design an analogue adder, comparing the schematic result of the analogue adder with other design and optimize the layout design of the analogue adder.

Different adder designs are compared against each other to distinguish the pros and cons of each design. The pros of each design are studied and tested for suitability to be implemented in the analogue adder design. Schematic for the analogue adder is constructed and tested, the results obtained are compared to other designs. After the desired schematic results are obtained, the layout of the design is constructed. Different layout placement will be tested to reduce the layout area and improve performance.

This project has a potential limitation, all testing and results are obtained from simulation using Synopsys Custom Compiler software instead of using actual hardware. Therefore, the results obtained might be subjected to biases, since the simulation conditions are ideal cases instead of real-world conditions.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Since the introduction of CMOS technology, many types of research have been done on the technology. Advancements have been made to the technology to achieve low power and high-performance design. Advancements of CMOS very-large-scale integration (VLSI) fabrication technologies are mainly focused on the reduction of the size of the MOSFETs; the channel length, junction depth and the thickness of the gate oxide are scaled down to improve the MOSFETs properties. (Leblebici, 1996). Thanks to the advancement, CMOS technology has become highly scalable, provide performance gain and reduction of cost to the semiconductor chips. (Dhar *et al.*, 2011). With never-ending greed, the desire to achieve greater performance and lower power design never stops, therefore despite the advancements, the design for low power and high-performance devices and circuits remains as a challenge. To the present day, CMOS scaling remains as the main factor in silicon technology advancement to achieve greater performance, but there is a limit to how much a MOSFET can be shrink. In this chapter different adder design will be compared and discussed to determine the aspects or features of the design which allow it to achieve low power and high performance. The technology process used by those design will not be the main focus, as smaller the technology used, provide more performance gain and lower power dissipation.

2.2 CMOS Digital Adder Design

The performance of a Full Adder (FA) circuit mainly depends on the propagation delay and the power dissipation. Since the FA does not generate the output instantaneously, the time taken for the FA to generate the output is the propagation delay. The propagation delay depends on the switching speed of the transistor and the time taken for the signal to reach the transistor.

CMOS power dissipation can be separated into two types. The first type is static power dissipation, which is the power dissipated when the inputs logic remains the same at a level and there is no change of states, the leakage current

is the cause of the power dissipation. The static power dissipation of a CMOS is very low, which one of the advantages CMOS over other IC technologies. Dynamic power dissipation can be separate to short circuit dissipation and switching power dissipation. Switching power dissipation is caused by charging and discharging of internal capacitances. Whereas short circuit power dissipation is caused by the direct connection between V_{DD} and V_{SS}, this occurs when the NMOS and PMOS are conducting at the same time. (Kabbani, 2008).

2.2.1 Low Number of Transistor Design

The power dissipation of a circuit is mainly contributed by the power dissipation of each component in it. Therefore, the power dissipation of each individual component should be minimized, but reducing the number of components used in a circuit could also yield the same result. For a CMOS circuit, reducing the number of transistors used in the design or a logic function reduces the device and interconnect parasitic. With a smaller number of transistors implemented, the layout area of the circuit can be reduced, lowering time delay and power dissipation. (Vasefi *et al.*, 2005).

According to the paper "Low Power N-Bit Adders and Multiplier Using Lowest Number of Transistor 1-Bit Adders" published by Vasefi and Abid in 2005, the performance of an adder can be improved by reducing the number of transistors used. In the paper, two 1-bit adders were designed with 10 transistors and the performance of the adder was compared to a standard CMOS-28T Adder. The adder designed was then cascaded to create a 4-bit ripple carry adder (RCA). The schematic diagrams of the 10 transistor 1-bit adder (10T 1-bit adder) and CMOS-28T adder are shown in the figures below:

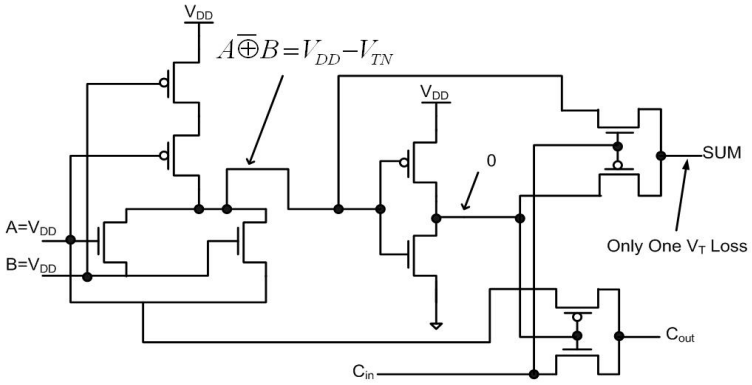

Figure 2-1: N-10T 1-bit Adder schematic diagram. (Vasefi *et al.*, 2005).

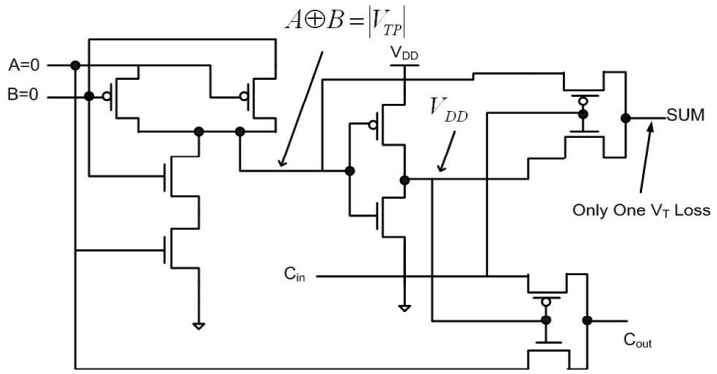

Figure 2-2: P-10T 1-Bit Adder schematic diagram. (Vasefi *et al.*, 2005).

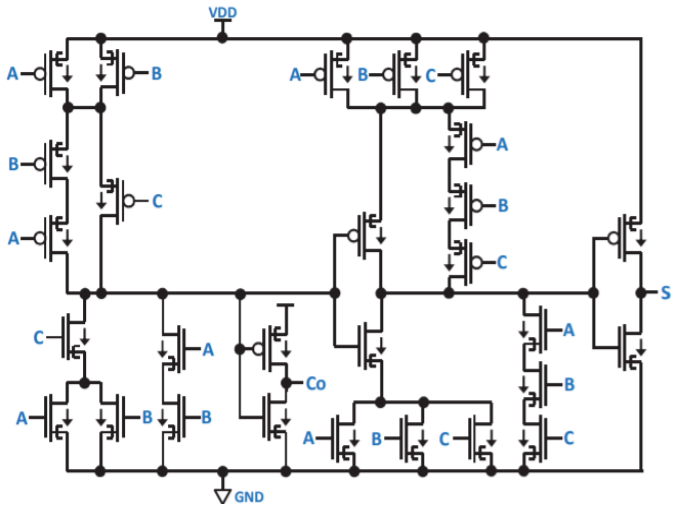

Figure 2-3: CMOS-28T Adder schematic diagram. (Strangio *et al.*, 2016).

To reduce the power dissipation, narrow series-connected transistor was added to the inverter to reduce leakage current. Furthermore, the inverter in the design is a skewed inverter, where the transistors are sized to create switching voltage, V_s higher than 0.5 V_{DD} for the P-10T Adder and lower than 0.5 V_{DD} for

the N-10T Adder. The adders were simulated and the results were compared to those of the CMOS-28T Adder, the results are recorded in Table 2-1. The adders were simulated with 100 *MHz* input signals and the result showed that the time delays for both of the new design were higher but the N-10T adder was able to achieve a 43.68% reduction in power dissipation.

Table 2-1: Results of P-10T, N-10T, and CMOS 28T adder designs.

Adder Design	**Power Dissipation (μW)**	**Time Delay (SUM) (*ps*)**	**Time Delay (C_{OUT}) (*ps*)**
P-10T	20.9	792	629
N-10T	9.94	566	598
CMOS-28T	17.65	307	222

Since the N-10T adder has a better result, it is used to construct the 4-bit adder and the results are 34.28 μW power dissipation and 3.103 *ns* delay. The problem faced in the design is voltage level degradation (V_T loss) at the output.

Similar to the previous paper, paper "A Novel Multiplexer-Based Low-Power Full Adder" published by Jiang *et al* in 2004, showed a new 1-bit adder design with 12 transistors and the adder was able to lower the power dissipation and improve the speed performance compared to some other 10 transistors adders and the CMOS-28T adder. The adder was named MBA-12T and the schematic diagram of the design is shown in the figure below:

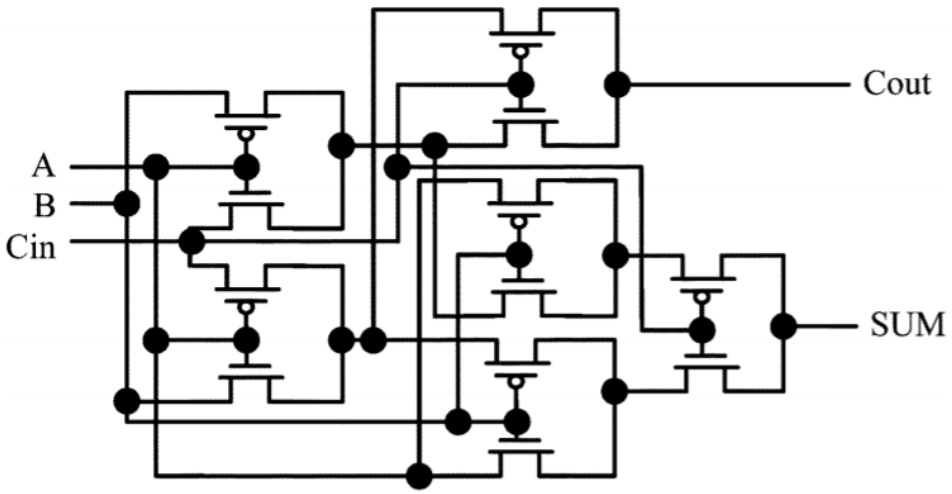

Figure 2-4: MBA-12T Adder schematic diagram. (Jiang *et al.*, 2004).

The design is built with six identical multiplexer gates; each multiplexer is built using two transistors as shown in Figure 2-5. The design does not have a direct path connected to V_{DD} or V_{SS}, thus the short circuit current is reduced to almost none and therefore the power dissipation due to short circuit current is greatly reduced. Besides all the transistor are excited by the input signals, this greatly reduces the time delay and fasten the transition of the output signal.

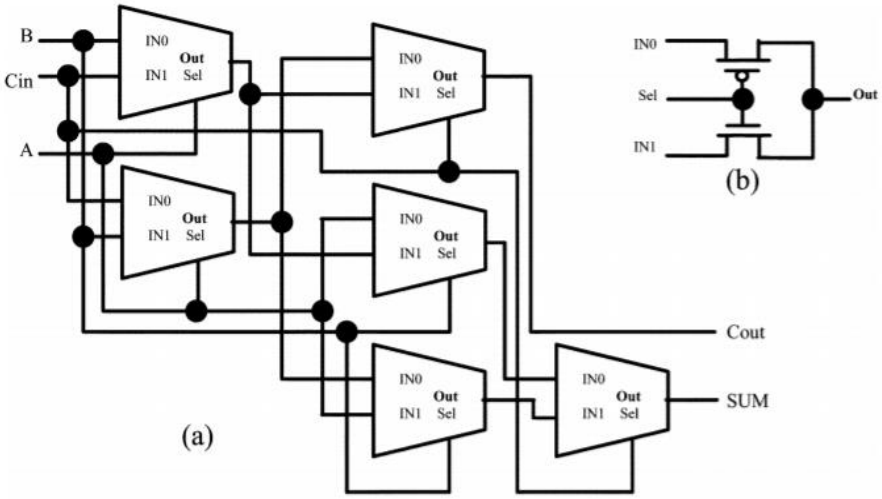

Figure 2-5: (a) Architecture of MBA-12T Adder. (b) 2-T MUX. (Jiang *et al*., 2004).

The MBA-12T Adder was simulated with 6 different frequencies, ranging from 10 to 200 *MHz*, and the results obtained were averaged and the reduction comparing to different 10T adders and CMOS-28T adder were calculated. The MBA-12T Adder was able to achieve at least 26% in power saving and over 78% speed improvement, the table below shows the reduction obtained:

Table 2-2: MBA-12T power dissipation and time delay reduction.

Adder Design	**Power Dissipation (*%*)**	**Time Delay (*%*)**
CMOS-28T	26	-
SERF	37.5	78.9
10T09A	36.5	78.2
10T09B	30.9	78.4
10T13A	36.3	78.5

2.2.2 Hybrid Design

Hybrid design uses a mixture of different logic, elements, technologies or processes to improve the conventional design or generate a new design. The hybrid design assimilates the advantages of other designs and incorporates them into their designs.

According to the paper "A Low-Power High-Speed Hybrid CMOS Full Adder for Embedded System" published by Tung *et al* in 2007, a new hybrid full adder was designed with pass transistor logic (PTL) and conventional static CMOS logic. The use of PTL greatly reduces the number of transistors needed and smaller input loads, due to PTL requiring lower number of transistors to perform an operation than CMOS. (Lee, *n.d.*). The performance of the hybrid adder greatly improves over conventional adders. In the paper, the advantages and disadvantages of other adder designs were discussed, the table below summarizes all the aspects of the adders discussed in the paper.

Table 2-3: Summarize of the aspects of different adder designs.

Adder Design	Aspect
Conventional CMOS full adder	• Symmetrical schematic topology, simple layout design • 28 transistors • Low power dissipation • Slower speed
Transmission Function full adder (TFA)	• Provides driving capability and buffered outputs • 26 transistors • High power dissipation • Slow speed
Pass Transistor Logic full adder (PTLA)	• Operates at full swing signal voltage • Require lesser transistor • Consumes m • Too much delay
Hybrid Pass Logic with Static CMOS output drive full adder (HPSC)	• Uses feedback loop to overcome a weak signal • Eliminates the propagation speed

The new hybrid adder is designed with 24 transistors and is separated into two circuits: the first circuit is dedicated for the SUM and the second circuit is for the C_{OUT}, both circuits require 12 transistors each. The SUM operation

circuit is a 3-input XOR function designed by cascading 2 2-input XOR gates. Buffers are added to the design since PTL are non-regenerative. The design of the SUM operation circuit is shown in Figure 2-6 and the design of the C_{OUT} operation circuit is shown in Figure 2-7.

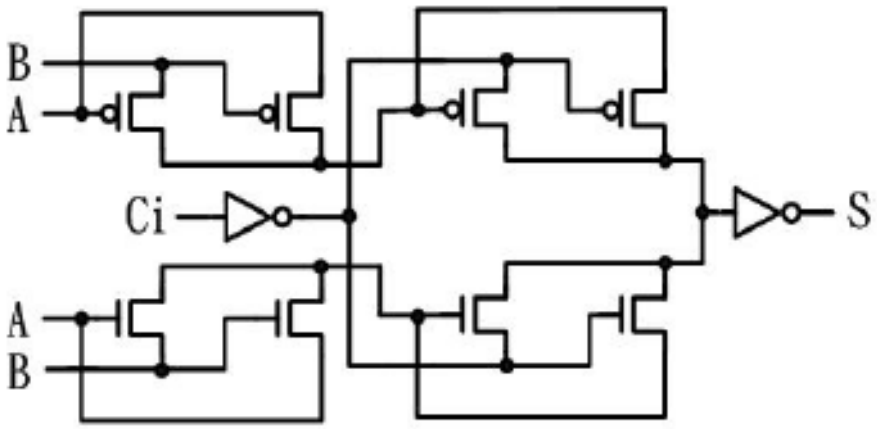

Figure 2-6: SUM operation circuit of the new hybrid adder schematic diagram. (Tung *et al*., 2007).

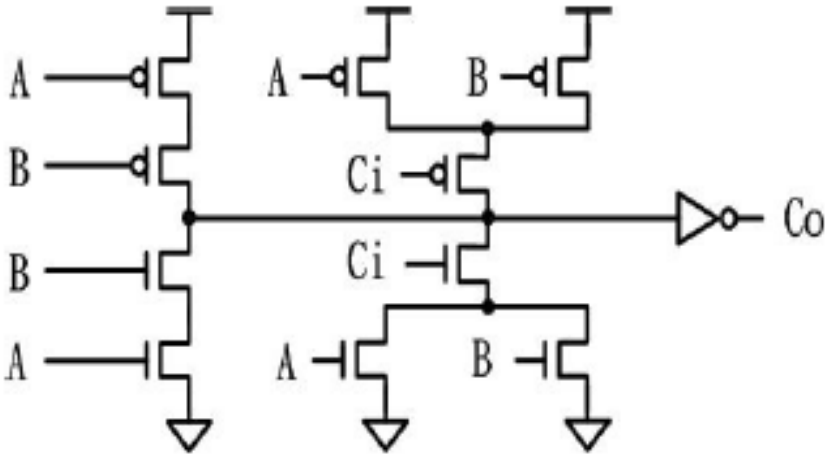

Figure 2-7: COUT operation circuit of the new hybrid adder schematic diagram. (Tung *et al*., 2007).

The new hybrid adder was simulated with a 200 *MHz* clock signal and the results obtained were compared to the other adder designs. The new hybrid adder was able to achieve up to 35.6% in power saving and up to 41.2% speed improvement, the simulation results are tabulated in Table 2-4.

Table 2-4: Hybrid design power dissipation and time delay.

Adder Design	Power Dissipation (μW)	Time Delay (SUM) (*ns*)	Time Delay (Co) (*ns*)
New Hybrid Design	65.21	0.26	0.17
CMOS-28T	66.39	0.29	0.19
TFA	87.08	0.20	0.23
PTLA	88.45	0.27	0.24
HPSC	78.50	0.24	0.23

Similar to the previous paper, paper "A New High Speed, Low Power Adder; Using Hybrid Analogue-Digital Circuits" published by Taherinejad *et al* in 2009, proposed a hybrid design full adder, the hybrid full adder combine the concepts of analogue and digital circuits. The analogue-digital hybrid (AD Hybrid) provides benefits of both analogue and digital circuits. The time delay of an adder is determined by the C_{OUT} propagation path, which usually takes the longest time, therefore the SUM and C_{OUT} are separated into different circuits to reduce the propagation delay.

The COUT circuit of the adder is designed with 10 transistors as shown in Figure 2-8. The trigger level of the inputs and clock transistors are required to be adjusted to generate the correct output, Table 2-5 show the desired inputs and output relationship. The adjustments are made by changing the transistor *W* to *L* ratio. The SUM circuit of the adder made up of 2-input XNOR gate, designed with 6 transistors as shown in Figure 2-9. The adder was simulated and the design was able to achieve 78 *ps* delay and 7.26 μW power dissipation.

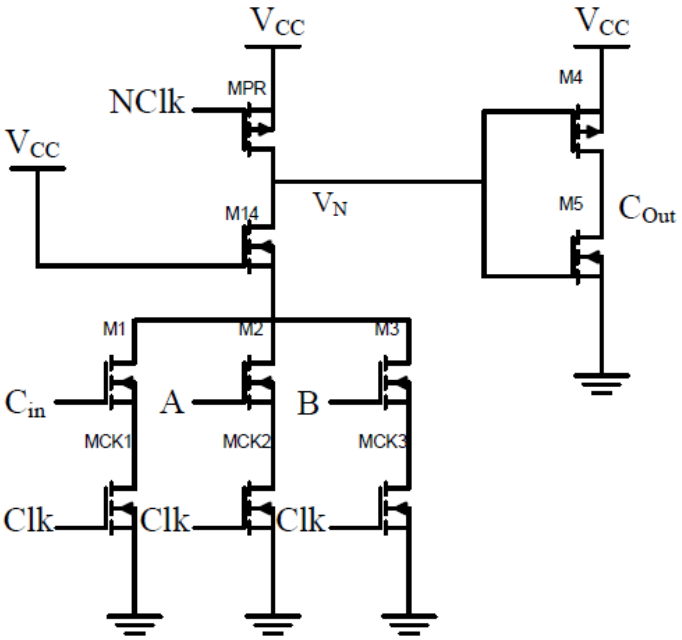

Figure 2-8: COUT circuit of the AD Hybrid adder schematic diagram.

(Taherinejad *et al*., 2009).

Table 2-5: Desired inputs, voltage level, and Cout relationship.

Numbers of High Inputs	**Voltage Level**	**Cout**
0	Highest	Low
1	High	Low
2	Low	High
3	Lowest	High

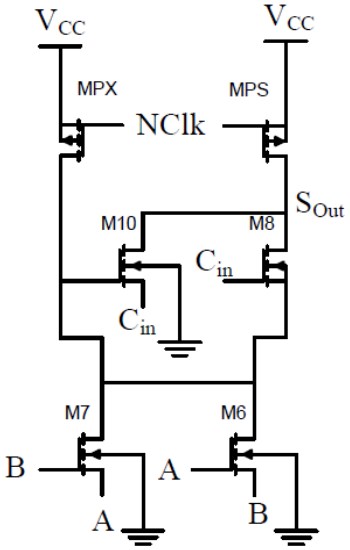

Figure 2-9: SUM circuit of the AD Hybrid adder schematic diagram.

(Taherinejad *et al*., 2009).

2.3 CMOS Analogue Adder Design

There are many ways to design an analogue adder with or without an operational amplifier. The difficulties faced when designing an analogue adder are linearity and accuracy. Most analogue adder designs have their MOSFETs operate in the saturation region (active region), where the drain current, I_D is independent of the drain to source voltage, V_{DS}, unlike digital design where their MOSFETs operate in triode region (linear region) and cut-off region. The equations below characterize the I_D in the triode region and saturation region:

$$Triode\ region: V_{DS} \leq V_{GS} - V_{TH}$$

$$I_D = \mu_n c_{ox} \frac{W}{L}\left((V_{GS} - V_{TH})V_{DS} - \frac{{V_{DS}}^2}{2}\right)$$

$$Saturation\ region: V_{DS} \geq V_{GS} - V_{TH}$$

$$I_D = \frac{\mu_n c_{ox}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

Figure 2-10 illustrates the relationship between I_D and V_{DS} of an NMOS, and the conditions to operate in those specific regions.

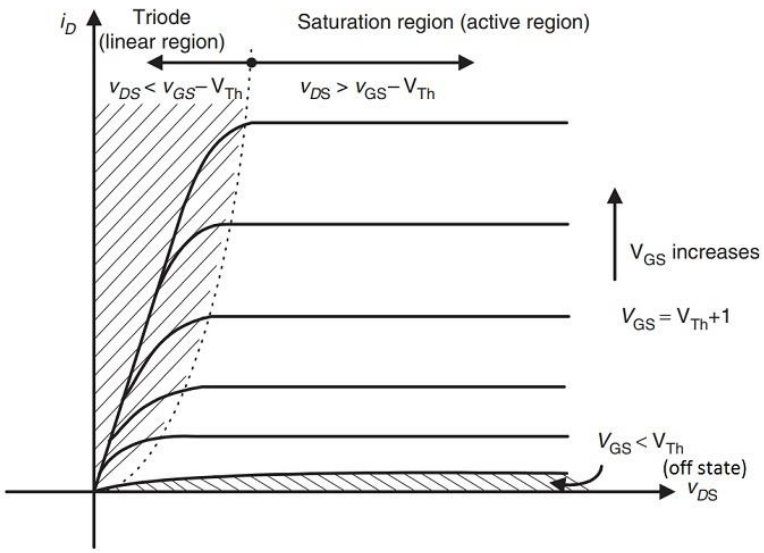

Figure 2-10: Relationship between drain current and drain to source voltage of an NMOS.

In the paper "Functionally Complete Element for Fuzzy Control Hardware Implementation" published by Varshavsky *et al* in 2004, a simple CMOS summing amplifier design was described and the schematic diagram is shown in Figure 2-11. With the gain factor set to 1, the summing amplifier is equivalent to an adder.

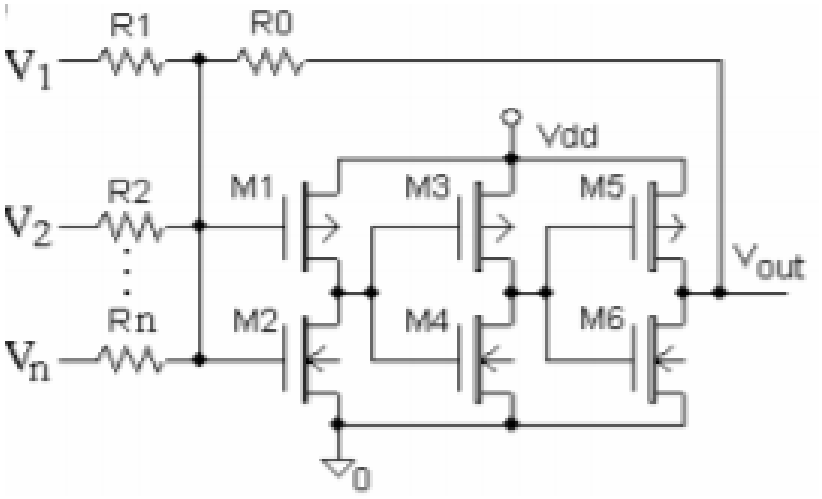

Figure 2-11: CMOS summing amplifier schematic diagram. (Varshavsky *et al*., 2004).

The output of the summing amplifier range between V_{DD} to 0 *V* and can be calculated using the equations below:

$$When \sum_{j=1}^{n} \frac{R_0}{R_j}\left(V_j - \frac{V_{DD}}{2}\right) \leq -\frac{V_{DD}}{2} \quad : V_{out} = V_d$$

$$When \frac{V_{DD}}{2} > \sum_{j=1}^{n} \frac{R_0}{R_j}\left(V_j - \frac{V_{DD}}{2}\right) > -\frac{V_{DD}}{2} : V_{out} = \frac{V_{DD}}{2} - \sum_{j=1}^{n} \frac{R_0}{R_j}\left(V_j - \frac{V_{DD}}{2}\right)$$

$$When \frac{V_{DD}}{2} \leq \sum_{j=1}^{n} \frac{R_0}{R_j}\left(V_j - \frac{V_{DD}}{2}\right) \quad : V_{out} = 0$$

$Where\ R_0 = feedback\ resistance$

$V_j = voltage\ on\ j^{th}\ input$

$R_j = j^{th}\ input\ resistance$

In the paper “CMOS analogue adder” published by Chaoi in 1995, an analogue adder was designed without the use of operational amplifiers. The working principle behind the design is mode current technique with the use of linear voltage to current and current to voltage converters, as shown in Figure 2-12 and the schematic of the design is shown in Figure 2-13.

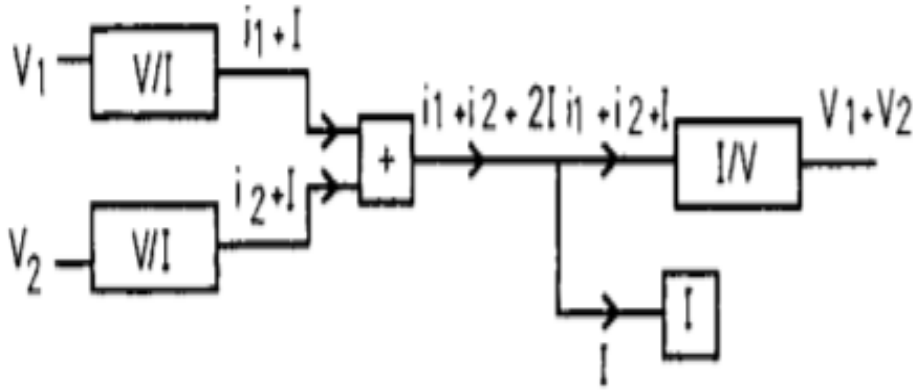

Figure 2-12: Chaoi analogue adder design principle. (Chaoi, 1995).

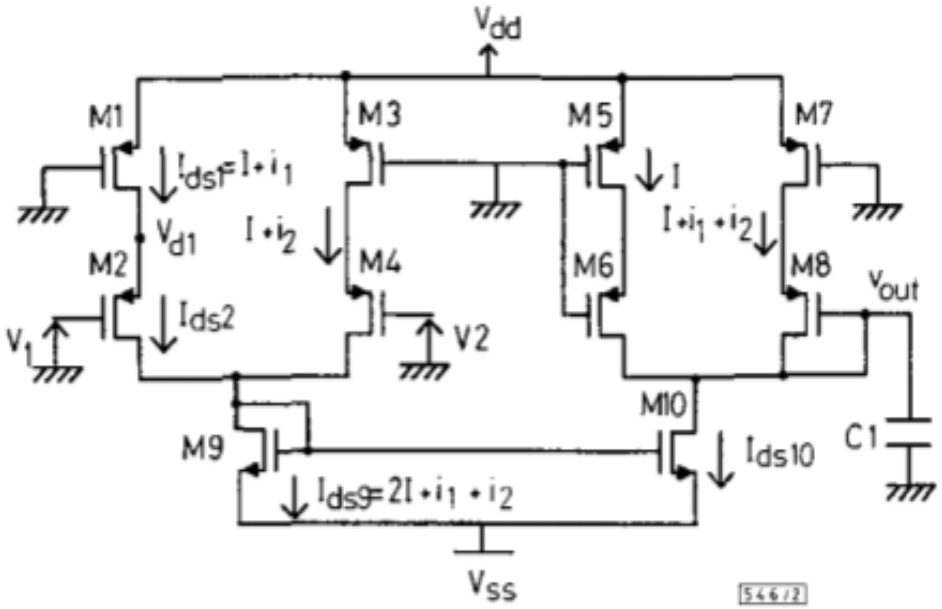

Figure 2-13: Chaoi analogue adder schematic diagram. (Chaoi, 1995).

The design was simulated and the results obtained are 30 *mW* power dissipation and 90 *MHz* bandwidth. The design provides a simple design which carries a small layout area and the power dissipation is reduced due to the design self-biased characteristic and no operational amplifier is required.

Similar to Chaoi design, Dianz-Sanchez and Ramirez-Angulo proposed a design with similar operation principle in the paper "A Compact High Frequency VLSI Differential Analogue Adder" published in 1996. The schematic of the design is shown in the figure below:

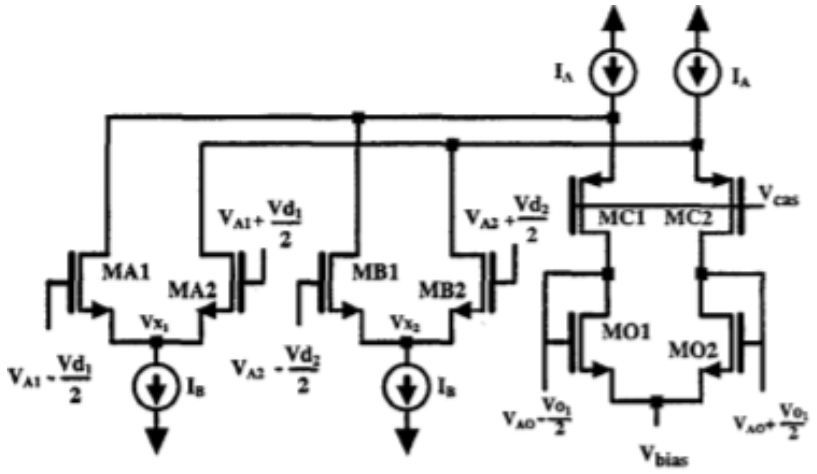

Figure 2-14: Dianz-Sanchez and Ramirez-Angulo analogue adder schematic diagram. (Dianz-Sanchez and Ramirez-Angulo, 1996).

The design is based on Kirchhoff's Current Law (KCL), where:

$$I_A - I_{D_{MO1}} = I_{D_{MA1}} + I_{D_{MB1}} \qquad \cdots (2.a)$$
$$I_A - I_{D_{MO2}} = I_{D_{MA2}} + I_{D_{MB2}} \qquad \cdots (2.b)$$

Since the MA1, MA2, MB1 and MB2 are biased by the same current I_B, thus v_{x1} and v_{x2} are the same. By equating equations 2.a and 2.b together then simplifying them, it can show that output is equal to the input summation:

$$Let\ V_{A1} = V_{A2}, V_{A1} - v_{x1} - V_{TH} = V_{A2} - v_{x2} - V_{TH} = A1\ and$$
$$V_{AO} - v_{bias} - V_{TH} = AO$$

$$I_{D_{MA1}} + I_{D_{MB1}} + I_{D_{MO1}} = I_{D_{MA2}} + I_{D_{MB2}} + I_{D_{MO2}}$$
$$\left(A1 - \frac{V_{d1}}{2}\right)^2 + \left(A1 - \frac{V_{d2}}{2}\right)^2 + \left(AO - \frac{V_{o1}}{2}\right)^2 = \left(A1 + \frac{V_{d1}}{2}\right)^2 + \left(A1 + \frac{V_{d2}}{2}\right)^2 + \left(AO + \frac{V_{o1}}{2}\right)^2$$
$$-A1V_{d1} - A1V_{d2} - AOV_{o1} = A1V_{d1} + A1V_{d2} + AOV_{o1}$$
$$-2AOV_{o1} = 2A1(V_{d1} + V_{d2})$$

Then making the AO equal to -$A1$, the final equation will be $V_{o1} = V_{d1} + V_{d2}$. The design is able to achieve linear operation if it fulfils two conditions:

1) The dimension ratio of the output transistors must be N^2 larger than the input transistors, where N is the gain of the system.
2) Same bias current for both the input and output transistors.

2.4 Low Power Analogue Design Techniques

Since the number of battery-powered handhelds (portable) electronic devices has greatly increased over the past few years, the amount of time the devices are functional or useable greatly depend on their battery life, therefore the demand for greater battery life in these devices is given a high priority. The power consumption of these devices mainly depends on the power consumption of the processors or the IC, which affect the battery life of the devices. Hence, low power design is important to the future development of these devices.

As mentioned in the previous part, dynamic power dissipation and static power dissipation can be found in CMOS integrated circuits. Dynamic power dissipation is the major power consumption, and by reducing it the total power consumption of the device may be reduced, and the battery life of the device can be extended. (Zhang *et al*., 2019).

There are many lower power design techniques available such as clock gating, power gating, multiple clocks and power domains, dynamic voltage and frequency scaling and sleep states. These techniques are great, highly effective and widely implemented in digital design, but the same story cannot be told for analogue design, these techniques are less effective in analogue design.

2.4.1 Low Voltage Current Mirror Technique

Current mirror principle stated that if the voltage between the gate terminal and source terminal of two uniforms MOSFET is the same, both MOSFET channel current will be the same. Current mirror techniques are implemented by integrating a reference current source into the circuit and that current will be mirrored through the circuit. (Singh *et al*., 2018).

According to "Implementation of CMOS Current Mirror for Low Voltage and Low Power" published by Yadav *et al* in 2012, low voltage current mirror provides better performance on temperature dependence and power

supply variations, CMOS mirror current also provides better performance thanks to their simple design and less complexity. The proposed CMOS low voltage current mirror design is shown in Figure 2-15 below:

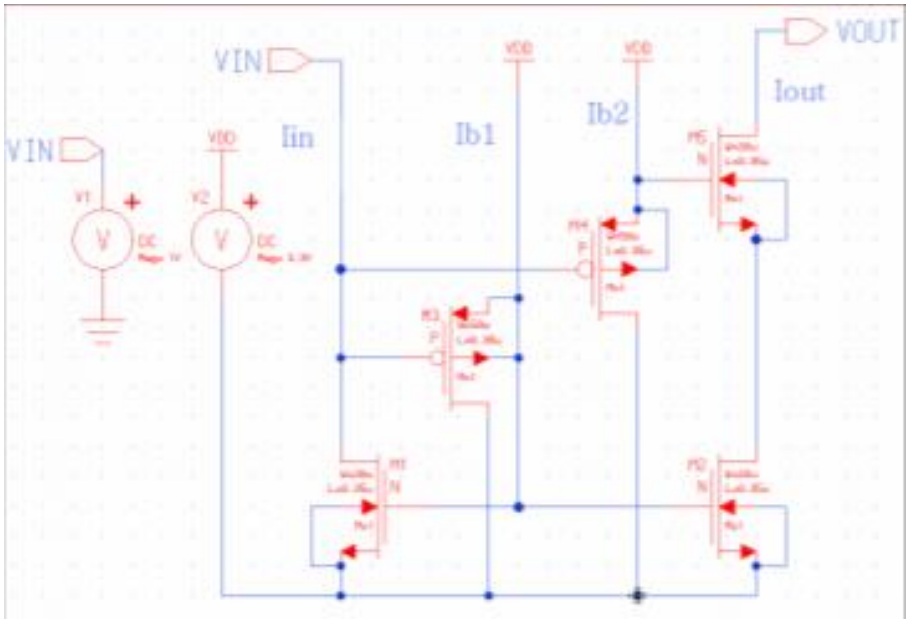

Figure 2-15: Proposed CMOS LCVM design. (Yadav *et al*., 2018).

2.4.2 Bulk-Driven Technique

PMOS and NMOS are 4 terminals MOSFET but they are typically used as 3 terminals devices by connecting or shorting the bulk terminal to either the source terminal, V_{SS} (for NMOS) or V_{DD} (for PMOS). This cause the threshold voltage to be fixed and the gate voltage must be higher than the threshold for the MOSFET to operates, this is a waste of power since it can be greatly reduced.

According to the Bulk-driven method, the threshold voltage can be either reduced or eliminated from the signal path, by setting the voltage between the gate terminal and source terminal to a minimum value, that is sufficient to form the inversion layer, and the input signal is connected to the bulk terminal. When the MOSFET is Bulk-driven, it operates similar to a junction gate field-effect transistor (JFET), capable of operating with negative, zero or slightly positive biasing condition. (Khateb *et al.*, 2010).

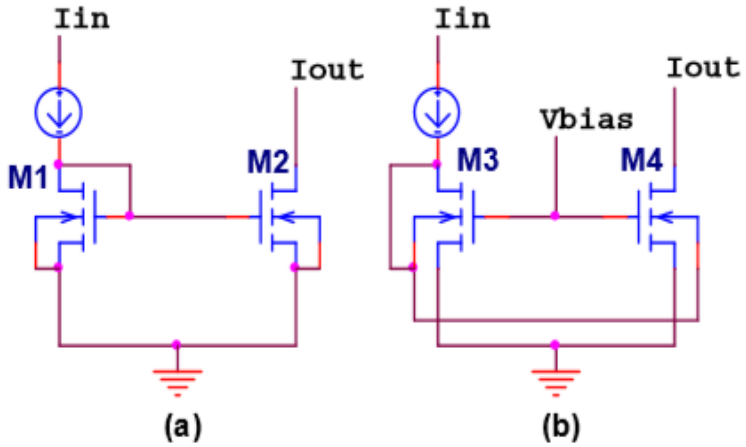

Figure 2-16: Conventional simple current mirror (a) vs Bulk-driven current mirror (b). (Khateb *et al*., 2010).

Table 2-6: Characteristic of Bulk-driven MOSFET

Characteristics of Bulk-driven MOSFET	
Desirable	**Undesirable**
• Low power and low voltage circuits consumption • None complicated design structure • Depletion characteristic avoid voltage threshold requirement in the signal path	• Transconductance of Bulk-driven is smaller than Gate-driven • Polarity bounded by MOSFET technology • Bulk-channel PN junction is prone to turn on

2.4.3 Floating Gate Technique

Floating-gate technique is commonly used in digital erasable programmable read-only memory (EPROM) or electrically erasable programmable read-only memory (EEPROM), but it can also be used in analogue design. A floating gate is a polysilicon gate surrounded by silicon oxide (*SiO*) as illustrated in Figure 2-17. Due to high quality insulator surrounding the floating gate, the charge on the floating gate is permanently stored acting as memory storage. (Hasler and Dugger, 2001).

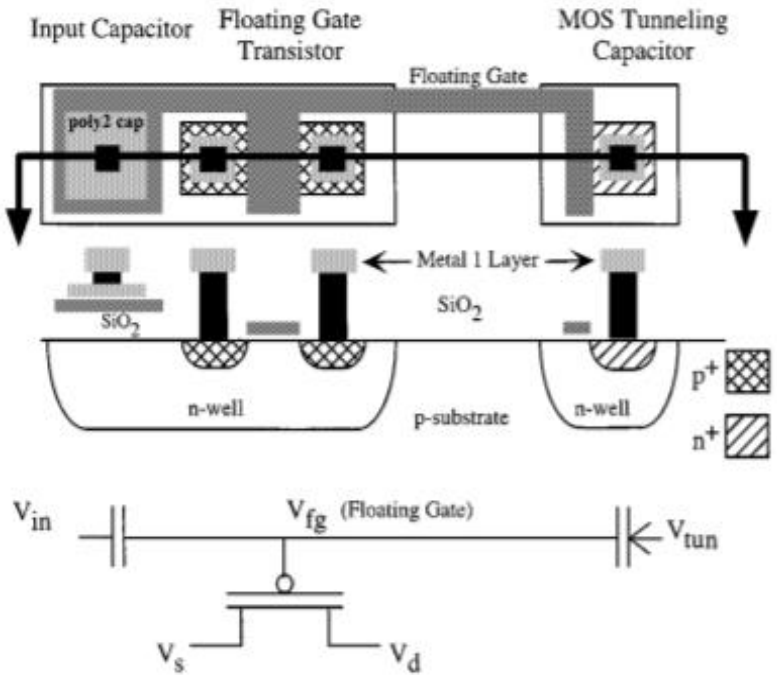

Figure 2-17: Layout, cross section and circuit diagram of floating gate design. (Hasler and Dugger, 2001).

In the paper "Programmable Floating-Gate Techniques for CMOS Inverters" published by Degnan *et al* in 2005, a floating-gate inverter which is a combination of two separate part: a common CMOS inverter and an analogue programming circuitry was proposed, the schematic of the design is shown in Figure 2-18 below.

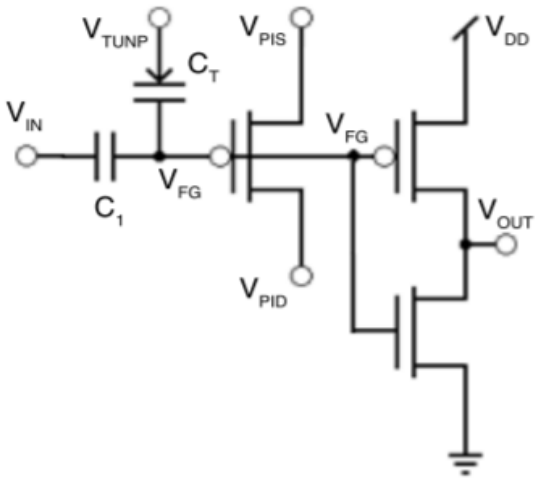

Figure 2-18: Proposed single floating-gate inverter design. (Degnan *et al*., 2005).

Hot electron injection and electron tunnelling are used to modify the threshold voltage of the floating gate inverter. The design result showed a wide range of threshold programmability which allow for a lower threshold to be used for the inverter operation.

2.5 Summary

Many different types of adder designs had been gone through and discussed in this chapter, to summarize all the adder designs, the simulation results of each adder design are tabulated in Table 2-7 and their description in Table 2-8.

Table 2-7: Simulation results of each adder design.

Adder Design	Number of Transistor	Process Technology (µ*m*)	Simulation Frequency (*MHz*)	Power Dissipation (*µW*)	Critical Time Delay (*ps*)
CMOS-28T	28	-	100	17.65	307
		0.35	200	66.39	290
P-10T	10	-	100	20.9	792
N-10T	10	-	100	17.65	598
MBA-12T	12	0.35	10 -200	-	-
TFA	26	0.35	200	87.08	230
PTLA	20	0.35	200	88.45	270
HPSC	22	0.35	200	78.50	240
Tung Hybrid Design	24	0.35	200	65.21	260
AD Hybrid Design	16	0.18	-	7.26	78
Varshavsky Design	6	-	-	-	-
Chaoi Design	10	-	90	30000	-
D&R Design	8	2	-	-	-

Table 2-8: Adder design description.

Adder Design	Description
CMOS-28T	• Required the most number of transistors • Symmetrical schematic design • Slow design
P-10T	• Require the least number of transistors • Simple design • Voltage level degradation problem
N-10T	• Require the least number of transistors • Simple design • Voltage level degradation problem
MBA-12T	• Reduces power dissipation due to short circuit current to a minimum • Design built from 6 multiplexer gates
TFA	• Slow design • High power dissipation
PTLA	• Less transistor needed than CMOS • Require buffer • Slow design • High power dissipation
HPSC	• Incorporates a feedback loop in the design • Design more complicated
Tung Hybrid Design	• Separate the summation and carry operation into 2 circuits • Low power dissipation
AD Hybrid Design	• Lowest power dissipation and time delay among the compared adder design • Simple carry circuit design • Separate the summation and carry operation into 2 circuits • Require adjusting the trigger level to obtain the desired output
Varshavsky Design	• Simple design • Limited operation range
Chaoi Design	• Simple design • Current mode technique
D&R Design	• Current mode technique • Linear operation achievable when conditions are met

The digital adder designs could not be directly compared based on the simulation results since the adders were simulated with different frequency and the process technology used was different. Therefore, selected few digital adder designs are required to be constructed with the same process technology and

simulated at the same frequency. This simulated result will then only be compared to the analogue adder.

Form the analogue adder designs discussed, design using current mode technique seems to provide more beneficial over the summing amplifier design. Since the techniques work based on KCL, more inputs can be easily added to the design without major changes. Therefore, the purposed analogue adder design will be designed using current mode technique.

Among the low power techniques discussed above, lower voltage current mirror technique seems suitable to be implemented in the proposed design. The low input and output voltage requirements of the technique are very well suited for the proposed design since the proposed design only operates for a low voltage range. The technique is not complicated to implement and provide good power dissipation reduction. Bulk-driven technique and floating gate technique are not implemented in the proposed design due to unsuitability, despite their ability to lower or eliminate the threshold voltage.

CHAPTER 3

METHODOLOGY AND WORK PLAN

3.1 Work Plan

The project is separated into two parts and is carried out at two different semesters. The first part of the project or better known as FYP 1 is carried out in the May semester, starting from May 27, 2019, to August 30, 2019, with a duration of 13 weeks. For the second part of the project, FYP 2 is carried out in January semester, starting from January 13, 2020, the due date was originally April 17, 2020, but is extended to April 30, 2020, due to coronavirus incident and movement control order (MCO), extending the duration from 14 weeks to 16 weeks.

In FYP 1, the main focus is to propose a low power analogue adder design. Majority of the time is spent on research and information gathering for the literature review. Different type of adder designs: analogue, digital and hybrid are analysed and studied, then compared against each other to distinguish the pros and cons of each design. The pros of each design are studied and tested for suitability to be implemented in the proposed analogue adder design. Among the designs studied, some are chosen for comparison against the proposed design. Before moving forward to the schematic design, some time is used to familiarize and adapt to the Synopsys Custom Compiler software. Figure 3-1 shows the Gantt Chart for the first part of the project.

In FYP 2, the basic proposed analogue adder design is constructed and simulated, and on the design low power techniques are implemented. After obtaining satisfying results, it can then move forward into the layout design. In the layout design, the layout of the proposed design is constructed and simulated, the results obtained are then compared to the schematic results. Figure 3-2 shows the Gantt Chart for the second part of the project.

Task Name	Duration	Start	Finish
FYP 1			
Discussion and Progress Update with Supervisor	12 wks	Thu 6/6/19	Wed 28/8/19
Research and Information Gathering	8 wks	Mon 10/6/19	Fri 2/8/19
Literature Review	8 wks	Mon 1/7/19	Fri 23/8/19
Report Writing and Presentation	7 wks	Mon 15/7/19	Fri 30/8/19
Familiarize with Synopsys Custom Compiler Software	2 wks	Mon 22/7/19	Fri 2/8/19
Simulation of Others Adder Design for Comparison	3 wks	Mon 29/7/19	Fri 16/8/19
Proposing Analogue Adder Design	1 wk	Mon 19/8/19	Fri 23/8/19

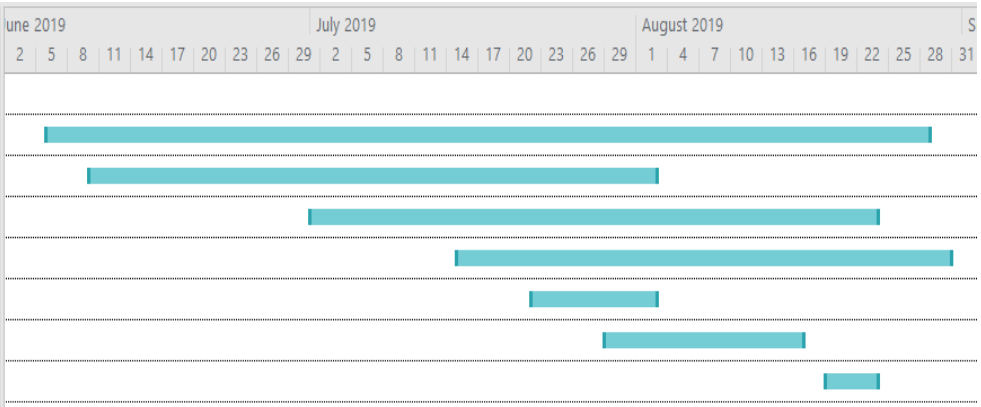

Figure 3-1: FYP 1 Gantt Chart.

Task Name	Duration	Start	Finish
FYP 2			
Discussion and Progress Update with Supervisor	15 wks	Mon 13/1/20	Fri 24/4/20
Constructing 2-inputs Analogue Adder Schematic	2 wks	Mon 20/1/20	Fri 31/1/20
Implementing Low Power Techniques	4 wks	Mon 3/2/20	Fri 28/2/20
Constructing 4-inputs Analogue Adder Schematic	3 wks	Mon 2/3/20	Fri 20/3/20
Analogue Adder Layout Deisgn	4 wks	Mon 23/3/20	Fri 17/4/20
Report Writing and Presentation	12 wks	Mon 3/2/20	Fri 24/4/20

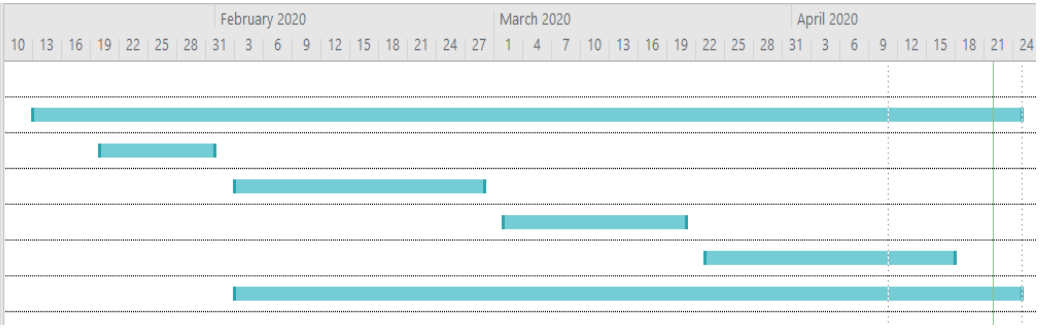

Figure 3-2: FYP 2 Gantt Chart.

3.2 Project Flow

The project can be broken down into three major parts: Adder Design, Schematic Design and Layout Design. The project begins at Adder Design part, where analogue, digital and hybrid adder design are analysed and studied. Different analogue adder designs are analysed and studied in term of their operation principle and approach in low power design. Whereas digital and hybrid adder designs are analysed and studied for comparison purpose to show the difference between their performance, the chosen adder designs are listed in Table 3-1.

Table 3-1: Chosen adder design for comparison.

Adder Design	Reason
CMOS-28T	• Conventional CMOS adder design • Use as the baseline for comparison
N-10T	• Design with the least number of transistors
MBA-12T	• Unique design with no direct path between the V_{DD} and ground
Tung Hybrid	• Separate the SUM and COUT into two circuits • Designed with pass transistor logic (PTL)

Low power techniques for analogue design are also studied since they differ from those implemented in digital design. Based on the research and studies, current mode technique is used in the proposed analogue adder design due to its simplicity and modifiability, low voltage current mirror technique and other low power techniques are also implemented in the design to improve the performance.

The next part of the project is Schematic Design, before directly diving into the schematic design of the adders, some time is used to familiarize and adapt to the Synopsys Custom Compiler Software. For an apple to apple comparison, the results obtained from the papers are unusable since different process technologies are used and simulated at a different frequency. Therefore, all the designs used for comparison are reconstructed using 90*nm* process technology and simulated at the same frequency of 250 *MHz*. The basic proposed analogue adder design is then constructed and simulate to ensure it operates as intended. Using the obtained simulation results as a baseline, low

voltage current mirror technique is implemented and the MOSFETs are tweaked to further improve the performance.

If the pre-layout results fulfil the design requirement, the design will move on to the last part of the project flow. In the Layout Design, different layout placements of the proposed design are tested to show the effect of layout area on the performance of the design. In the end, the simulation results of the layout design are compared to those from the schematic design.

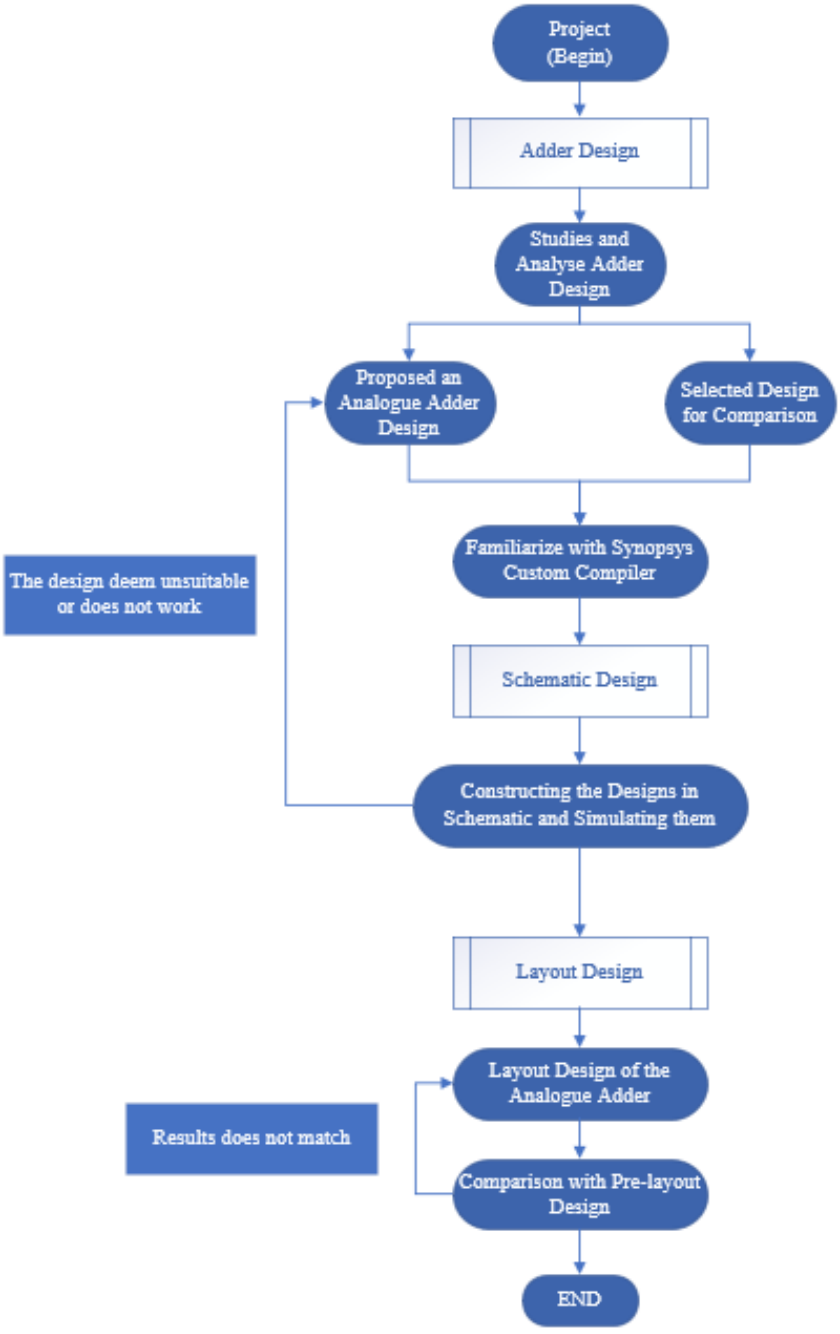

Figure 3-3: Project flow diagram.

3.3 Proposed Analogue Adder Design

The proposed analogue adder design is based on current mode technique, where the inputs in the voltage form are converted to current form. In current form, the summation is easily achieved by applying KCL, the currents entering a node are equal to the currents exiting it. The sum of the currents is then converted back voltage form to obtain the final output.

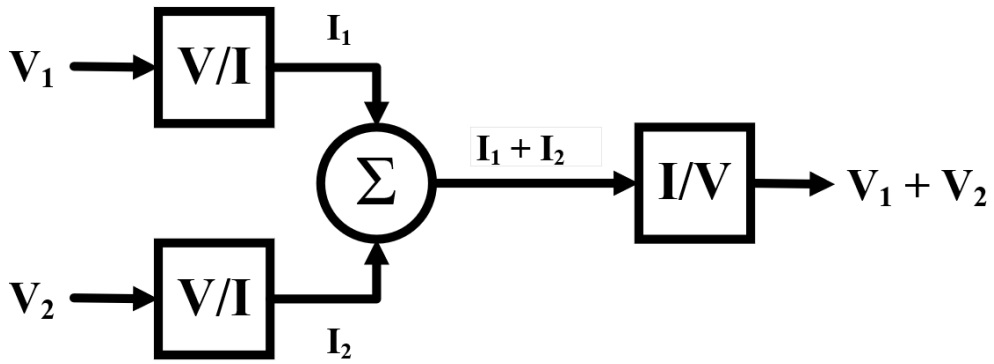

Figure 3-4: Analogue adder principle of operation.

The input voltage can easily be converted to current form since I_D is dependent on the gate voltage, V_g but there is no convenient way for current to voltage conversion. Therefore, complementary input pairs are used to even out the equation and solve this problem. The proposed analogue adder design is shown in the figure below:

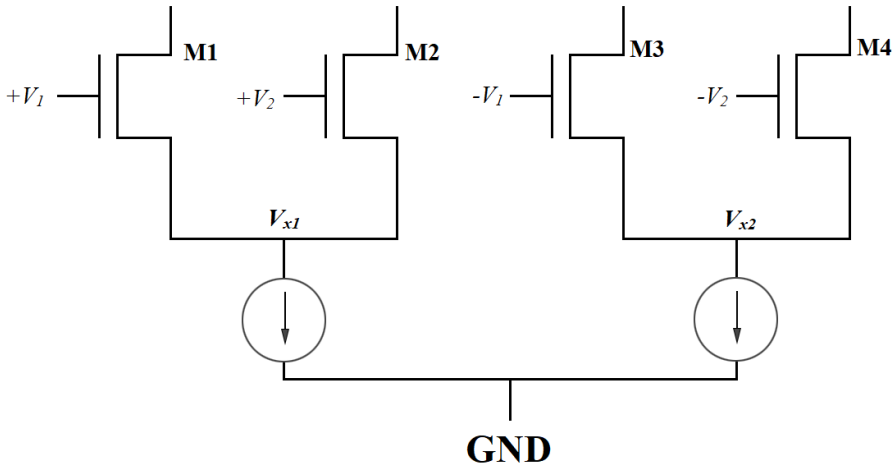

Figure 3-5: Proposed analogue adder design.

For I_D to be independent of V_{DS}, the MOSFETs used for current conversion will operate in the saturation region. An offset voltage, V_{offset} will be added to each input to ensure the gate voltage is greater than the threshold voltage, since the input voltage may be less than the threshold voltage of the MOSFET. The inputs voltage is converted to currents form:

$$I_{D_{M1}} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_T)^2$$

$$= \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left(V_1 + V_{offset} - V_{x1} - V_T\right)^2 \quad \ldots(4.a)$$

$$I_{D_{M2}} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left(V_2 + V_{offset} - V_{x1} - V_T\right)^2 \quad \ldots(4.b)$$

$$I_{D_{M3}} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left(-V_1 + V_{offset} - V_{x2} - V_T\right)^2 \ldots(4.c)$$

$$I_{D_{M4}} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left(-V_2 + V_{offset} - V_{x2} - V_T\right)^2 \ldots(4.d)$$

The currents entering their respective node are summed together and the current exiting the nodes are identical based on the design:

$$I = I_{D_{M1}} + I_{D_{M2}} \quad \ldots(4.e)$$

$$I = I_{D_{M3}} + I_{D_{M4}} \quad \ldots(4.f)$$

By equating the equation 4.e and 4.f together and sizing the MOSFET identically, it shows that the inputs voltage summation is equivalent to $V_{x1} - V_{x2}$.

$$Let\ V_{offset} - V_{x1} - V_T = VA\ and\ V_{offset} - V_{x2} - V_T = VB$$

$$I_{D_{M1}} + I_{D_{M2}} = I_{D_{M3}} + I_{D_{M4}}$$

$$(V_1 + VA)^2 + (V_2 + VA)^2 = (-V_1 + VB)^2 + (-V_1 + VB)^2$$

$$2V_1VA + 2V_2VA + 2VA^2 = -2V_1VB - 2V_2VB + 2VB^2$$

$$V_1VA + V_2VA + V_1VB + V_2VB = VB^2 - VA^2$$

$$(V_1 + V_2)(VA + VB) = (VB - VA)(VB + VA)$$

$$V_1 + V_2 = VB - VA$$

$$= V_{x1} - V_{x2}$$

For the design to work, the current exiting the nodes must be equivalent, thus a current mirror must be added to the design. Cascode current mirror is used instead of a basic current mirror to reduce the mirrored current difference and improve the accuracy of the design. PMOSs are added before the current converting NMOSs to reduce the current entering the NMOSs, which reduces the power dissipation of the design. The finalized design is shown in the figure below:

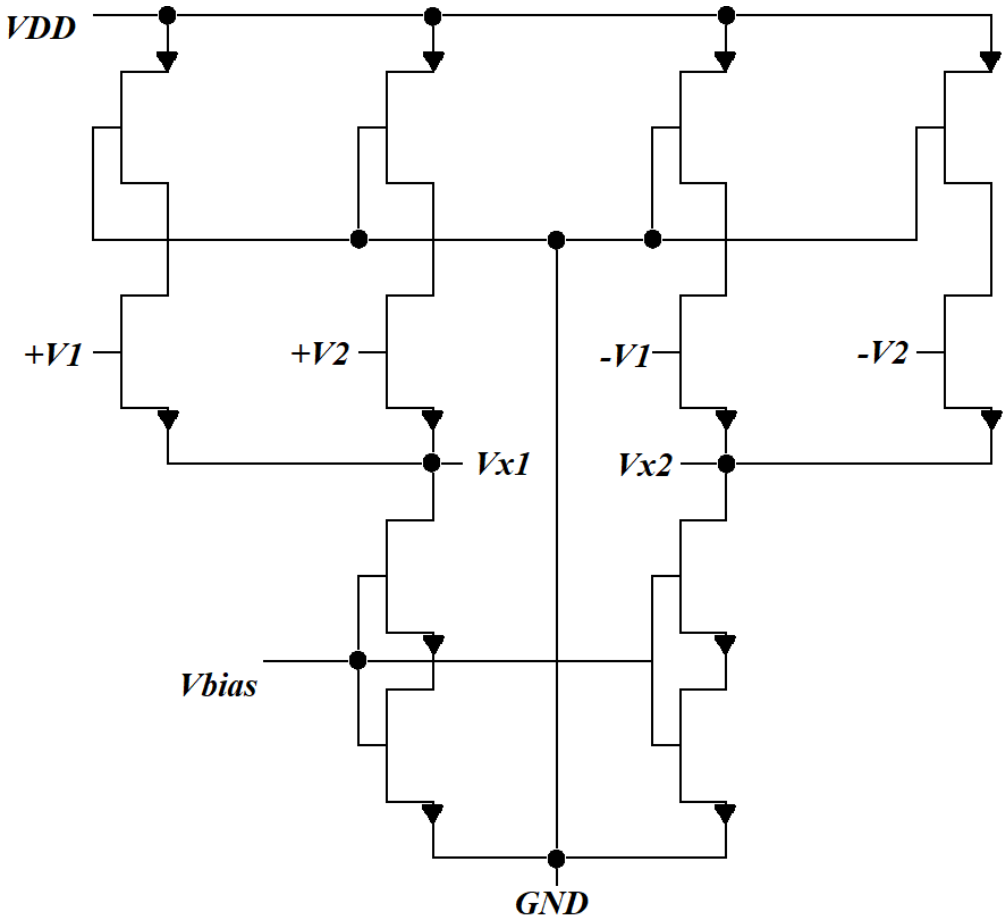

Figure 3-6: Finalized proposed analogue adder design.

3.4 Analogue Adder Design Methodology

In this project, custom design is used instead of Application Specific Integrated Circuit (ASIC) design. ASIC design uses electrical design automation (EDA) tool to synthesis the register transfer level (RTL) design and automate the placement and routing for the layout design. For custom design, the designer will design all or some of the logic cells and the layout, no predefined gates will be used in the design. (Kommuru and Mahmoodi, 2009). Custom designs are able to achieve 3 times to 8 times faster performance than ASIC design with the same technology process, due to the high optimization capability of custom design. (Chinnery and Keutzer, 2005). The table below summarizes the advantages and disadvantages of custom IC design.

Table 3-2: Advantages and disadvantages of Custom IC Design

Custom Integrated Circuit Design	
Advantage	**Disadvantage**
• High flexibility in design • High degree of optimization in performance and layout area • Ability to integrate analogue and pre-designed components	• Long design time • Large amount of design effort • Complexity

Custom design is suitable for this project since a major aim for the proposed analogue adder design is to have low power dissipation and custom design provide a high degree of optimization in performance and layout area. Synopsys Custom Compiler is the software used to create the custom design, it provides a user-friendly environment and useful features such as design debug, simulation analysis and reporting. These features help to detect errors in the design and report them, simplifying the debugging process. Figure 3-7 shows the overall process flow of the custom design.

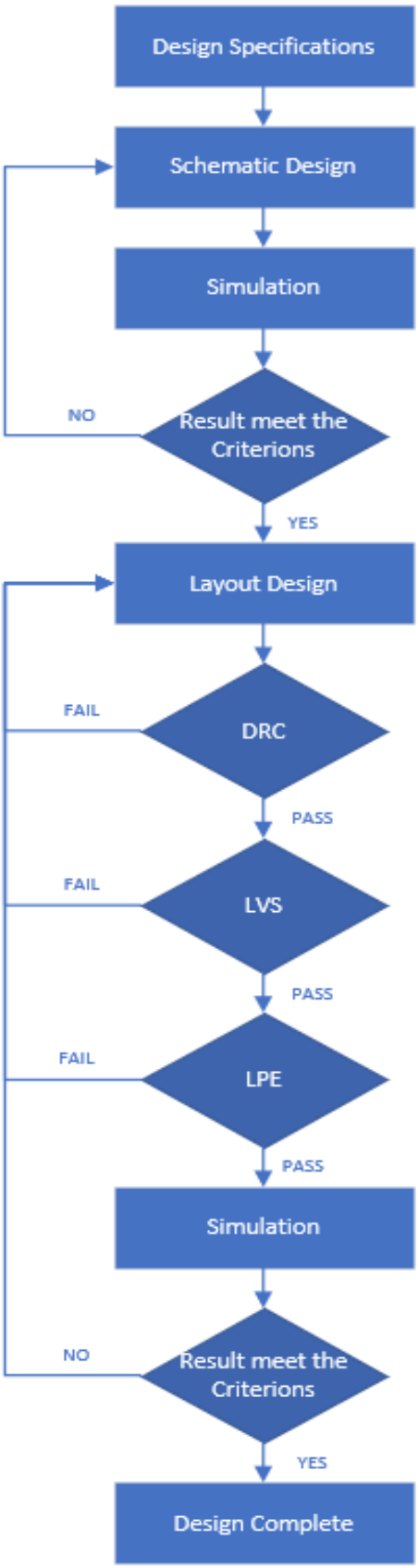

Figure 3-7: Custom design flow.

The first stage of the design flow is the listing of the design specifications or the design criteria to be made. The table below list all the specifications for the proposed analogue adder design, the design is designed revolving around these specifications.

Table 3-3: Analogue adder specifications and criteria

NO	Parameter Description	Value
1	Process	SAED 90nm
2	Input Voltage	-1.5V ~ 1.5V
3	Power Dissipation	< 1mW
4	Time Delay	< 10ps
5	Layout Area	< 30μm^2
6	Output Accuracy	> 90%

Using the formulas of the MOSFET, an equation to obtain the output is created and based on that equation, the MOSFETs parameters, placement, connection and operational region are all determined. After completing the design, the design will be constructed and simulated using Synopsys Custom Compiler.

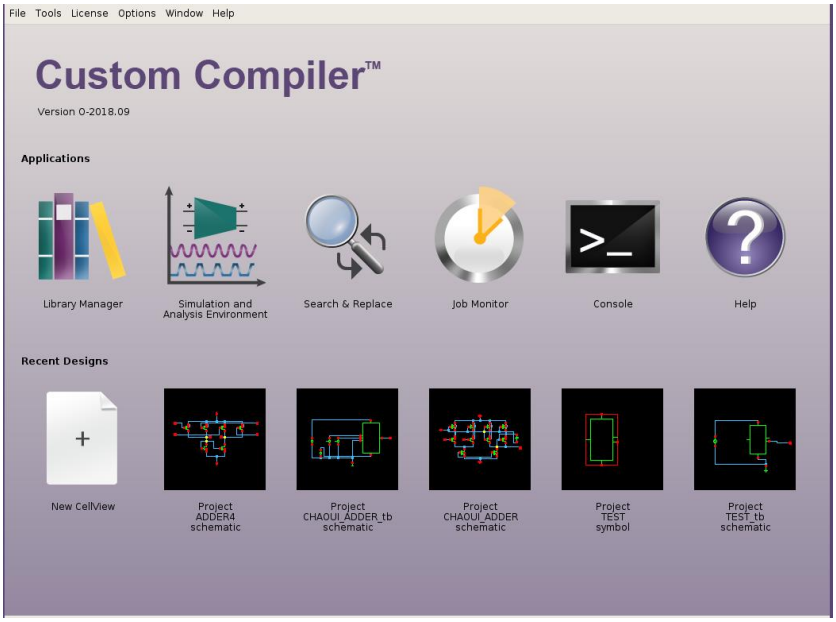

Figure 3-8: Synopsys Custom Compiler.

The next stage of the design flow is the schematic design. For the schematic design, components are selected from the library and are then placed

and route according to the design. The parameters of the MOSFETs are set and the input/output pins are added as shown in Figure 3-9.

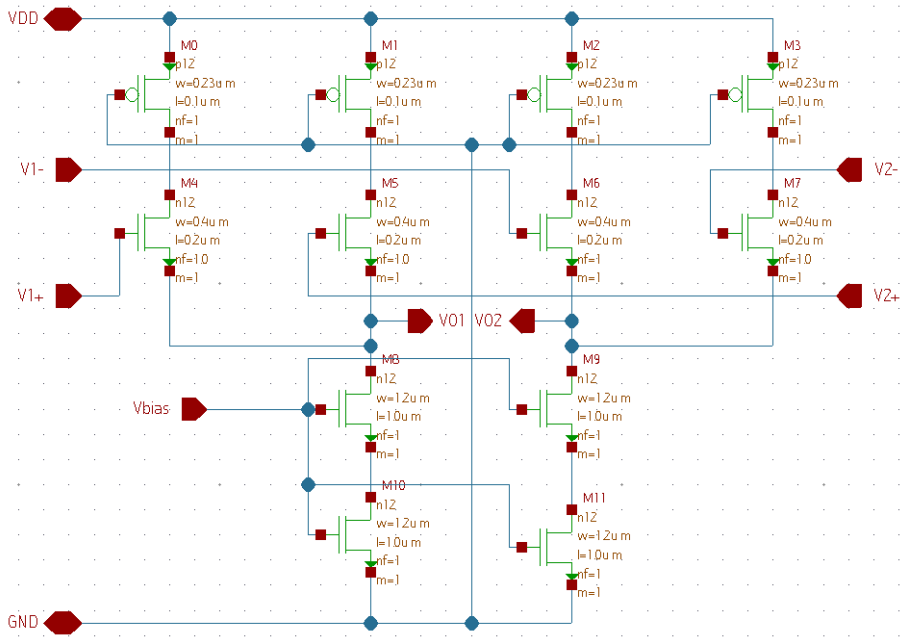

Figure 3-9: Constructing the schematic circuit.

After the schematic circuit is fully constructed, the circuit is then checked for schematic errors: connection mismatch, unconnected terminals and others. The custom compiler will help to check for those errors and report them.

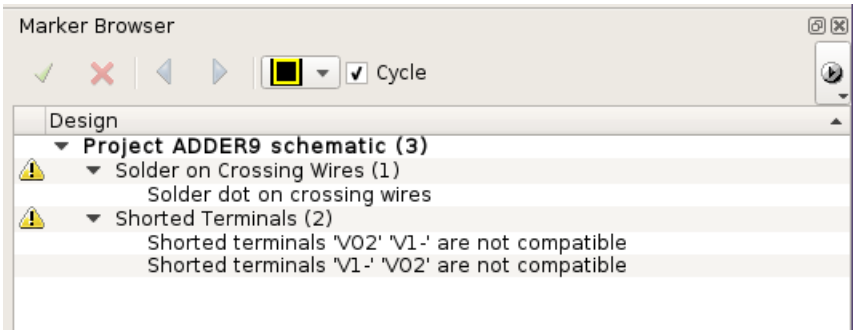

Figure 3-10: Schematic error checking.

After passing the schematic error checking, a symbol is generated to represent the circuit, which only shows the input/output ports and not the MOSFETs placement and connection, as shown in Figure 3-11. A test bench is created

using the symbol to verify the design output correctness by injecting various inputs into the design and the outputs generated are checked.

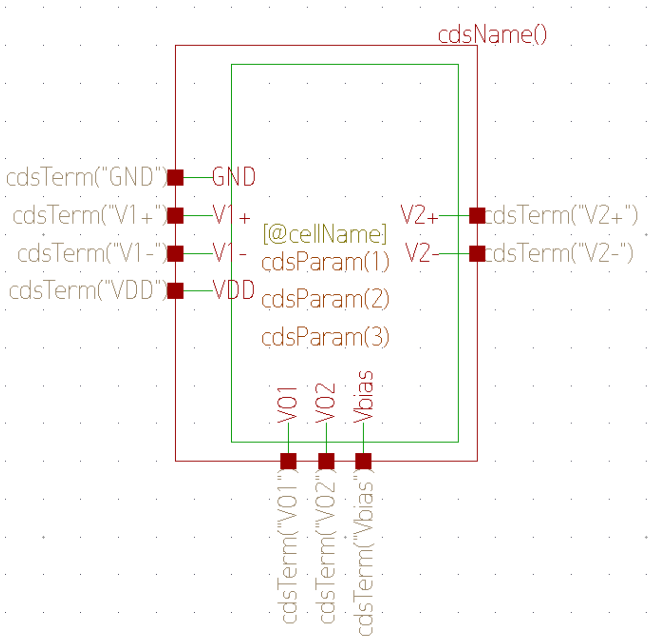

Figure 3-11: Generating a symbol to represent the schematic circuit.

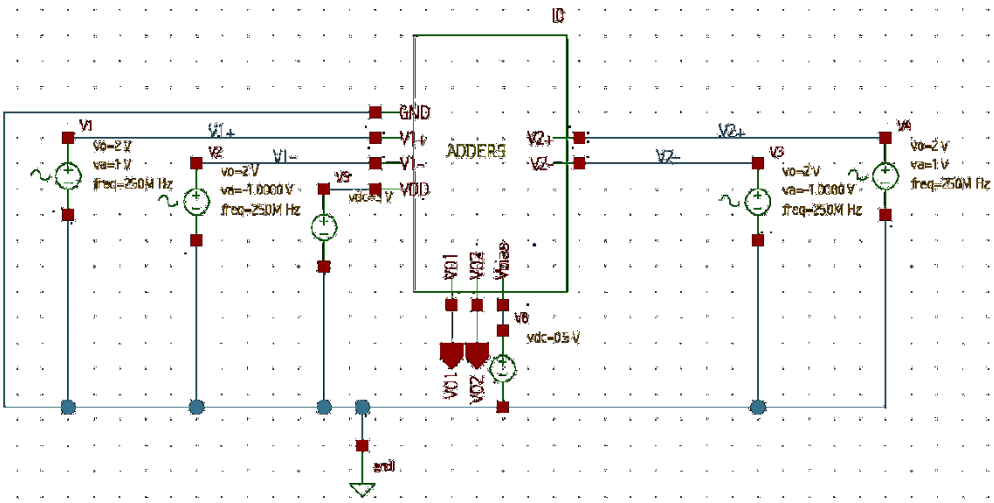

Figure 3-12: Test bench.

Within the Simulation and Analysis Environment (SAE), the simulation parameters are set and the components to display in wave view are selected. Any error in the schematic design will terminate the simulation and the errors found will be reported. Within the wave view, the simulation results or better known as pre-layout results are analysed and verified for its correctness, tools

and settings are provided in the wave view to ease the analysing process. The maximum power dissipation is obtained from the maximum setting and the time delay is obtained by measuring the difference between input peak and output peak. If the pre-layout results are verified and meet the criteria of the design, then it proceeds to the layout stage, else it will return to the schematic design stage to re-evaluate the design.

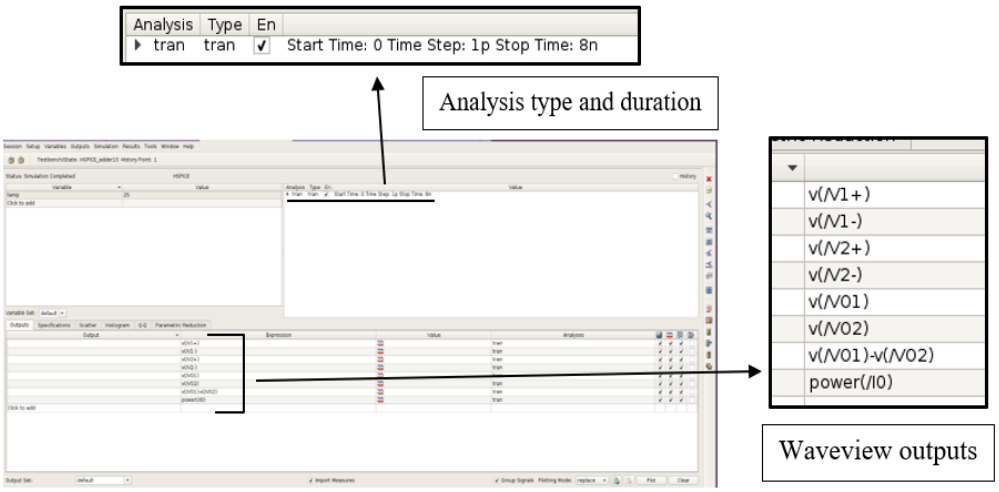

Figure 3-13: Simulation and Analysis Environment (SAE).

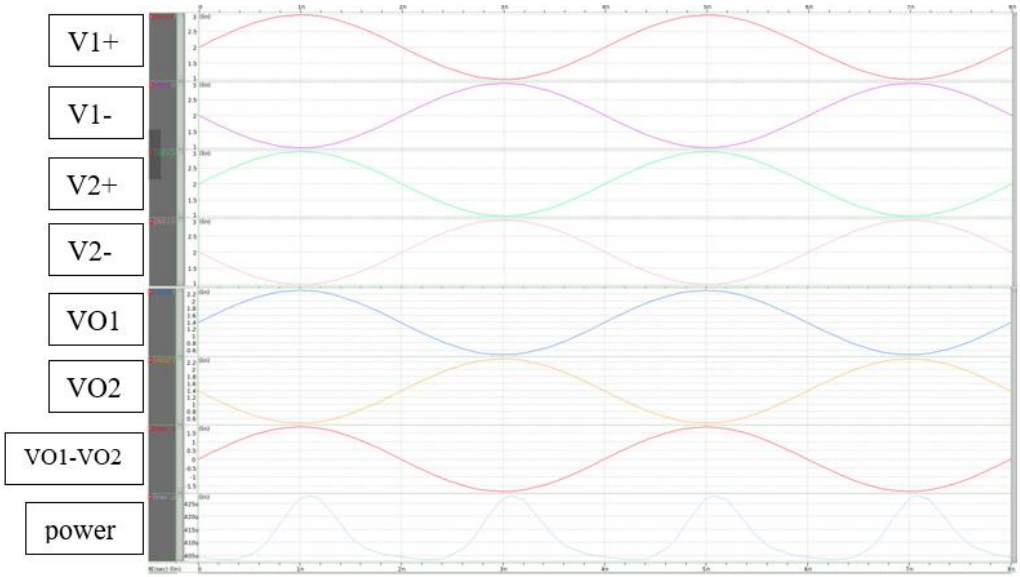

Figure 3-14: Pre-layout simulation results in wave view.

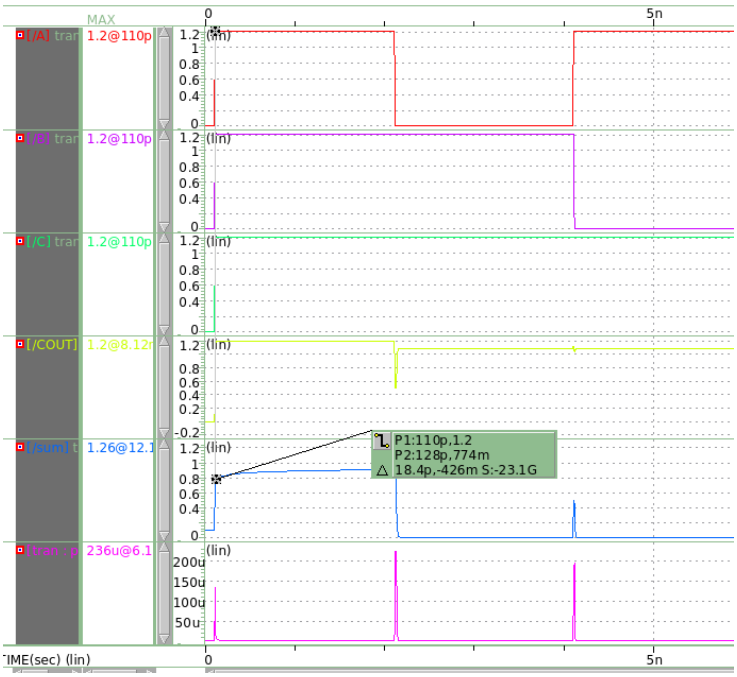

Figure 3-15: Obtaining maximum power dissipation and measuring time delay.

In the layout design stage, the design is constructed with MOSFETs in their layout view and the wires used for connection are now in the form of metal layers, the connections between the MOSFETs remain the same as in the schematic design. As different metal layers are not connected or interlinked, specific via contacts are needed to connect them, this characteristic allows the connections to be overlapped on top of one another using different metal layers as shown in Figure 3-16, this greatly reduces the layout are of the design.

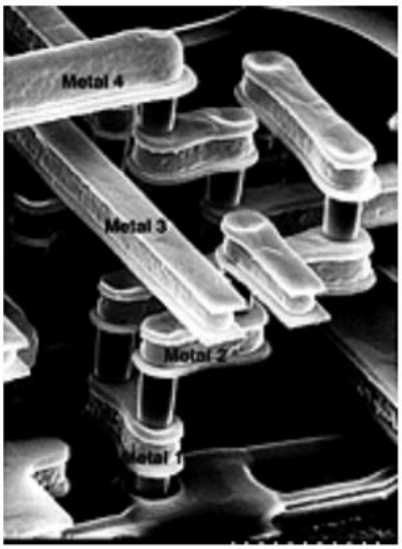

Figure 3-16: Connections stacking using different metal layers

The layout design is required to pass several tests to ensure there are no physical and design errors in the design. The first test is Device Rule Check (DRC), where the design tested if there are any design rule violations such as minimum spacing between metal or contact requirement. If the violations are found, they will be reported and the type of violations are explained as shown in Figure 3-17. This ease the correction process of the design as all the violations are located and explained.

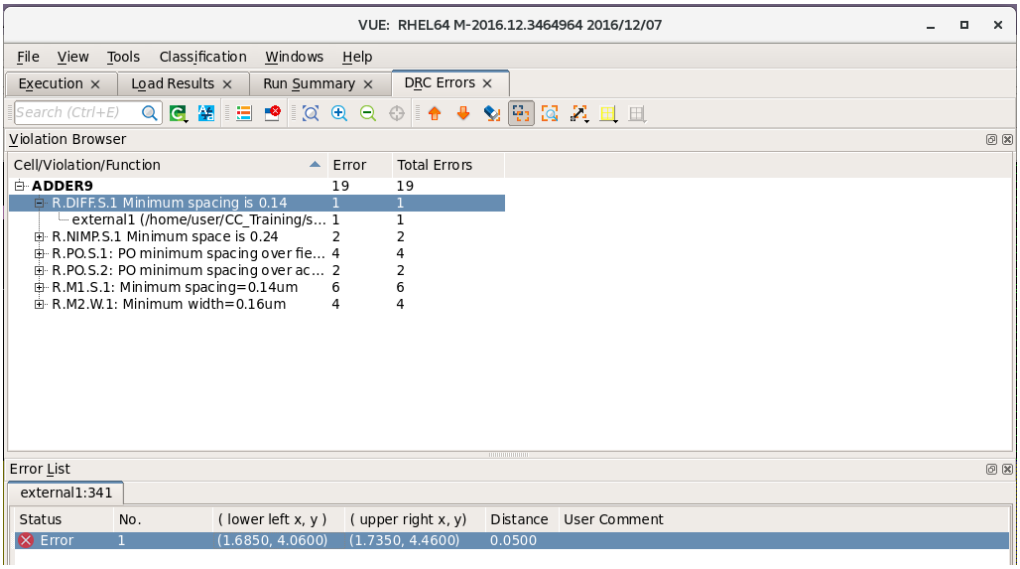

Figure 3-17: DRC violations reporting.

The next test is Layout vs Schematic (LVS), the layout design is compared to the schematic design in this test. The connections, input/output ports and components used are all compared in test and to pass this test, all of them must be matched, the layout design must be identical to schematic design. Similar to DRC, the mismatches between the layout and schematic are all reported and explained as shown in Figure 3-18.

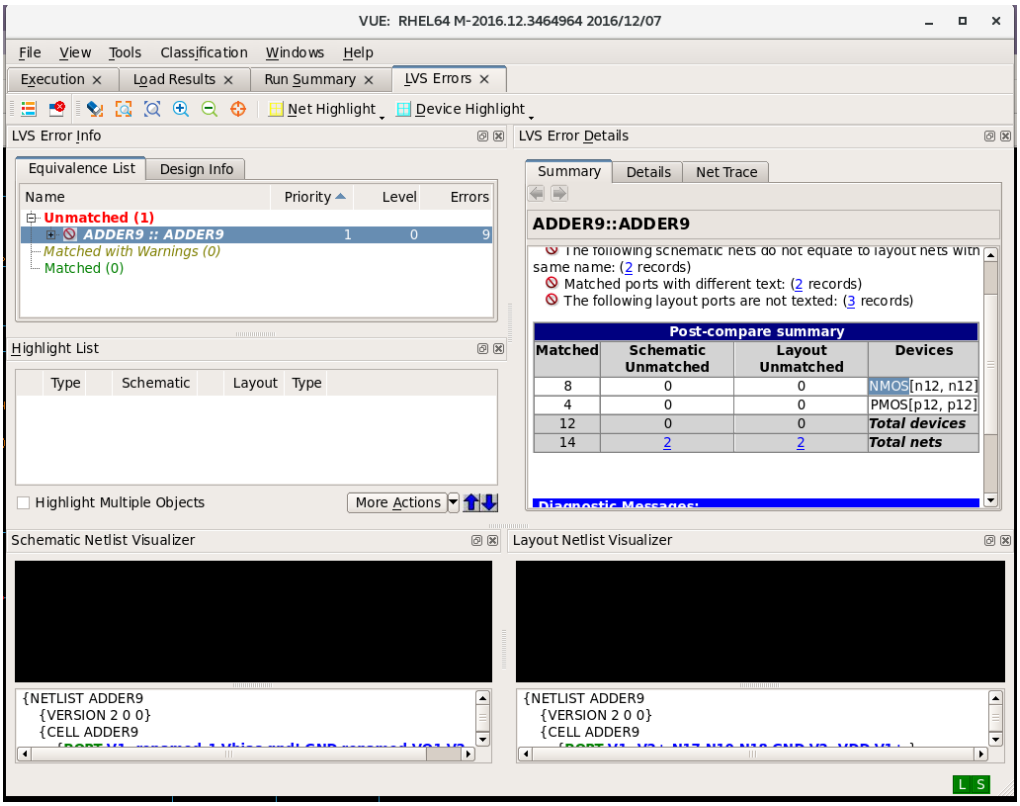

Figure 3-18: LVS error: layout and schematics mismatch.

The last test is the Layout Parasitic Extraction (LPE), where the layout parasitic is extracted. StarRC is the layout parasitic tool used since it handles with LVS violations, timing converge can be ensured before the physical verification phase. Completing this test will generate a new layout (starrc layout) as shown in Figure 3-19, where the patristic has been extracted and will be used for post-layout simulations.

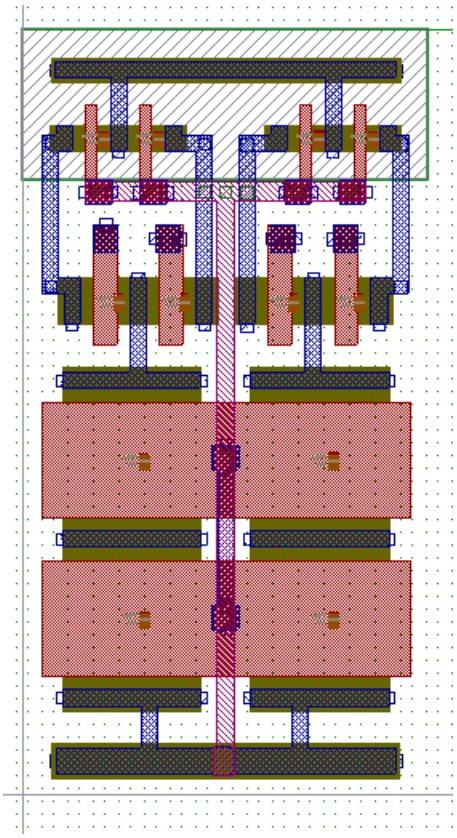

Figure 3-19: Starrc layout (after patristic extraction).

Failure of any test will cause the design to move back to the layout design phase to revise the layout design. If all the tests are passed, the layout design moves towards the simulation phase, where the layout design is simulated and the results obtained are compared to the pre-layout results and the design criteria. The custom design is completed when the results obtained are similar to pre-layout results and all criteria are met, else it is move back to the layout designs stage.

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Introduction

In this chapter, the performance of the 4 chosen adder designs and the proposed analogue adder are analysed and discussed. The 4 chosen adder designs will represent the performance of digital and hybrid adders and will be used for comparison against the proposed analogue adder. The 4 chosen adder designs are constructed using the same technology process and simulated under the same conditions for a fair comparison. For the digital and hybrid adder design, the main focus will be on the time delay of the output and the design power dissipation, whereas the main focus for the analogue adder design will be on the accuracy of the output and the power dissipation. The principle of operation and decision made in analogue adder design are also explained in this chapter. Both the schematic and layout design are constructed for the analogue adder design, and post-layout results are compared against pre-layout results.

4.2 Digital and Hybrid Adders Simulation Results

To ensures an apple to apple comparison between the adder designs, the simulations are done under the same condition, as listed in the table below:

Table 4-1: Digital and Hybrid Adders Simulation Parameters.

No	Parameter Description	Values
1	Process Technology	90*nm*
2	Temperature	25℃
3	PMOS to NMOS ratio	2:1
4	Input Frequency	250*MHz* and 125*MHz*
5	Input Voltage	1.2*V*
6	VDD	1.2*V*

The adder designs are designed with 90 *nm* process technology and the threshold voltage of each MOSFET are fixed by fixing their bulk voltage. The PMOS is sized twice the size of the NMOS to equalize their resistance since electrons have 2.7 times higher mobility than holes. All the adder designs are 1-bit adder

which has 8 types of input combinations, all the combinations are simulated and the results obtained are compared to the truth table.

Table 4-2: 1-bit Full Adder truth table.

Inputs			Outputs	
A	**B**	**C**	**SUM**	**COUT**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

4.2.1 CMOS-28T

Since CMOS-28T adder is a conventional CMOS adder design, it is selected for comparison. As the name suggested, the design is made up of 28 MOSFET which is the most among the simulated design. The width of PMOS and NMOS used are calculated and adjusted to fulfil the 2:1 ratio. Figure 4-1 shows the schematic design constructed and Figure 4-2 shows the simulation outputs timing diagram.

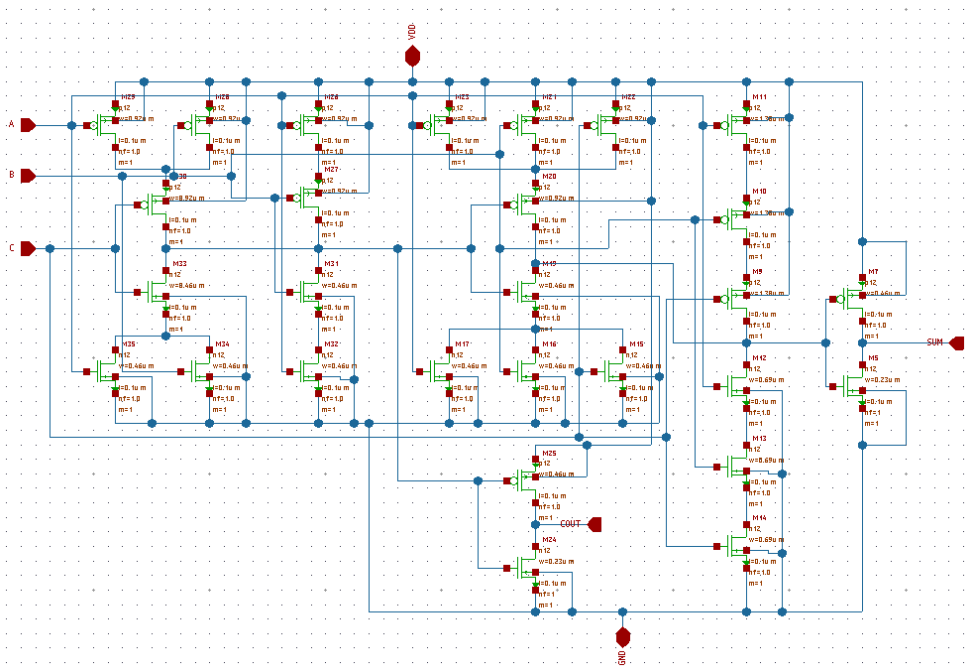

Figure 4-1: CMOS-28T schematic diagram in custom compiler.

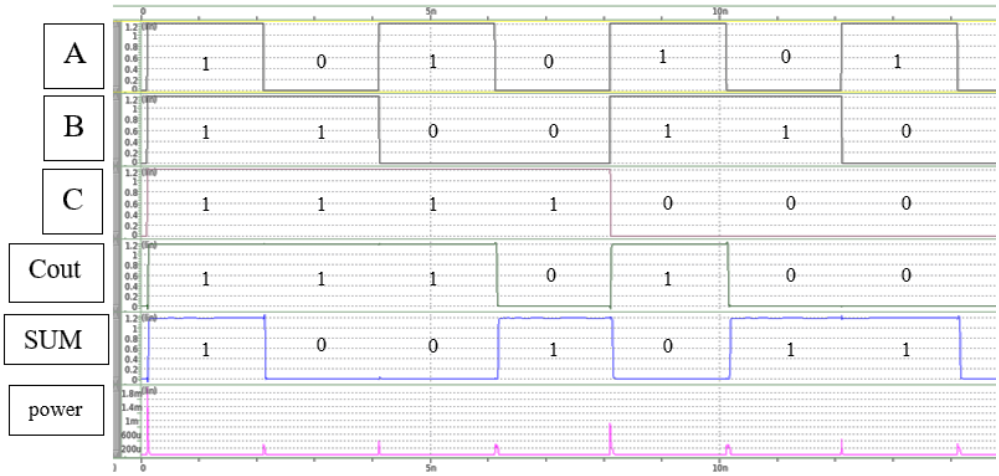

Figure 4-2: Timing diagram of CMOS-28T.

The outputs of the simulation are compared to the truth table for verification. The maximum power dissipation and maximum time delay are measured and tabulated in Table 4-3, the critical path is determined to be the SUM path.

Table 4-3: Maximum power dissipation and time delay of CMOS-28T.

Maximum Power Dissipation (*mW*)			**1.93**
Time Delay (*ps*)	**SUM**	**1**	20.3
		2	32.2
		3	66
		4	48.6
		5	70
		6	49
	COUT	**1**	15.3
		2	44.7
		3	16.7
		4	37.1
	Maximum		**70**

4.2.2 N-10T

N-10T adder utilizes the least number of transistors, therefore it is selected for comparison. The width of PMOS and NMOS used are calculated and adjusted to fulfil the 2:1 ratio. Figure 4-3 shows the schematic design constructed and Figure 4-4 shows the simulation outputs timing diagram.

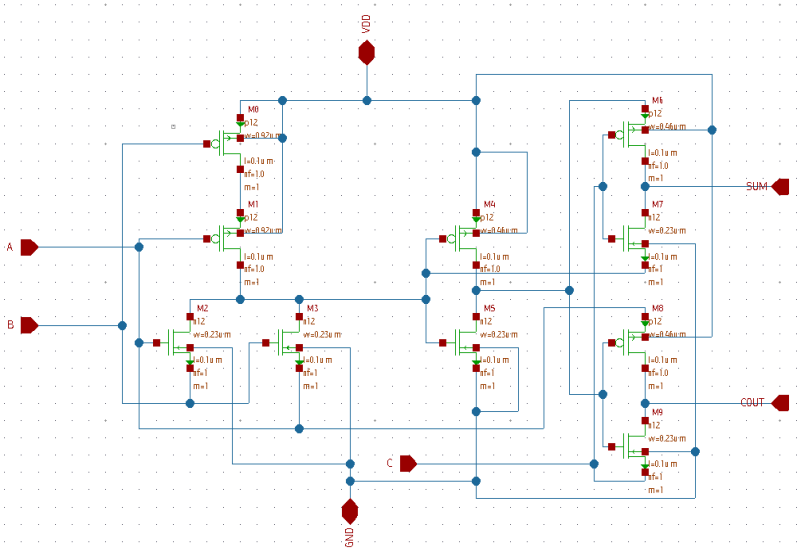

Figure 4-3: N-10T schematic diagram in custom compiler.

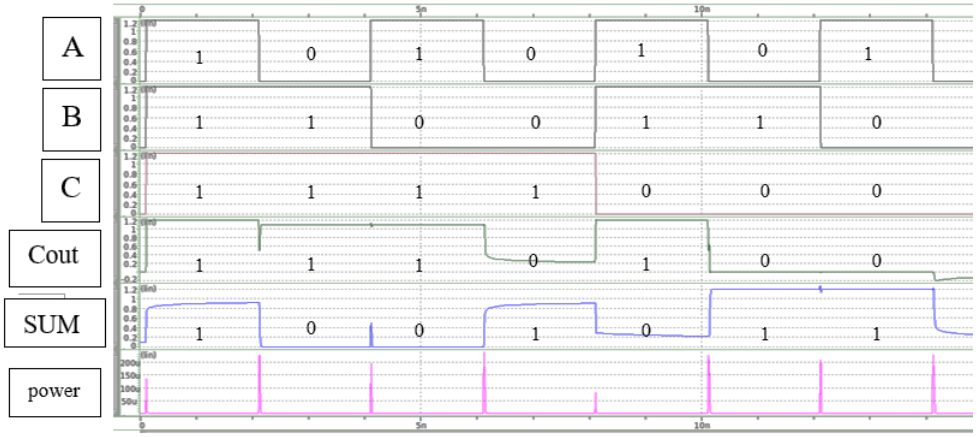

Figure 4-4: Timing diagram of N-10T.

The outputs of the simulation are compared to the truth table for verification. The maximum power dissipation and maximum time delay are measured and tabulated in Table 4-4, the critical path is determined to be the COUT path. The simulation output showed that the outputs of the design are not strong ‘1’ and strong ‘0’, this is mainly due to the voltage level degradation.

Table 4-4: Maximum power dissipation and time delay of N-10T.

Maximum Power Dissipation (μW)			**236**
Time Delay (*ps*)	**SUM**	**1**	3.37
		2	13.1
		3	16.1
		4	10.1
		5	28.3
		6	37.4
	COUT	**1**	4.87
		2	28.9
		3	2.11
		4	21.4
	Maximum		**37.4**

4.2.3 MBA-12T

MBA-12T adder utilize a unique design, where there is no direct path between the V_{DD} and ground, therefore it is selected for comparison. The width of PMOS and NMOS used are calculated and adjusted to fulfil the 2:1 ratio. Figure 4-5 shows the schematic design constructed and Figure 4-6 shows the simulation outputs timing diagram.

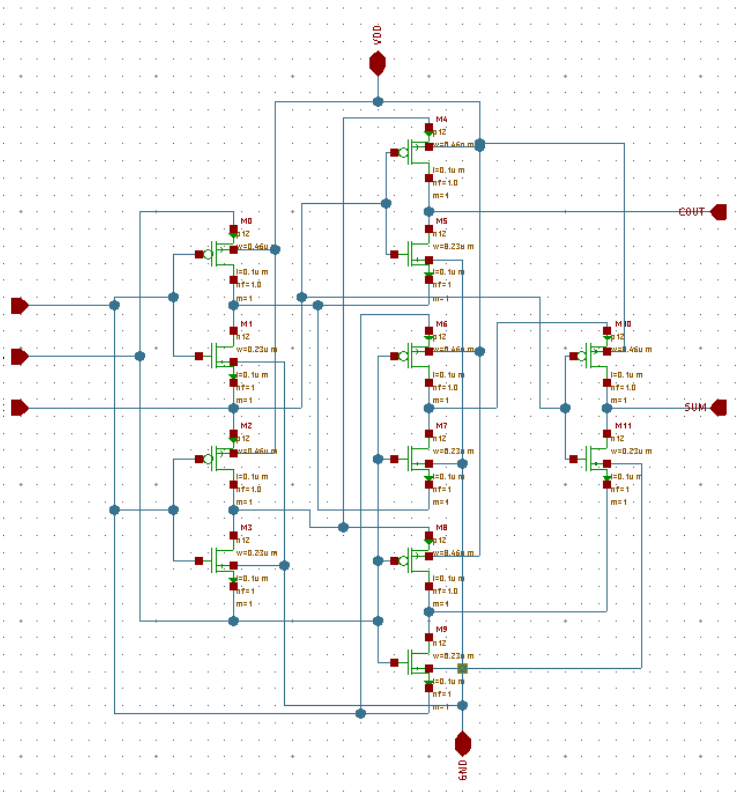

Figure 4-5: MBA-12T schematic diagram in custom compiler.

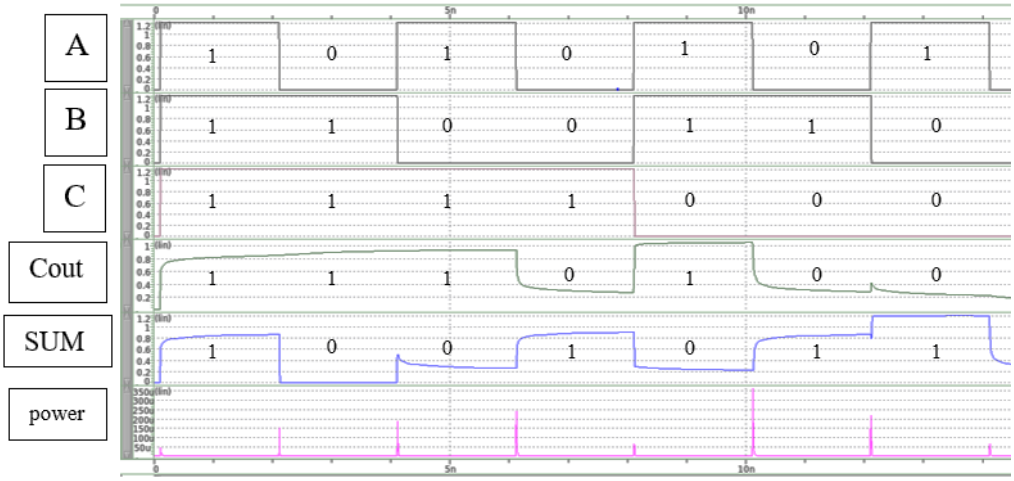

Figure 4-6: Timing diagram of MBA-12T.

The outputs of the simulation are compared to the truth table for verification. The maximum power dissipation and maximum time delay are measured and tabulated in Table 4-5, the critical path is determined to be the SUM path. The simulation results show that both the COUT and the SUM does not always reach its maximum and minimum value. As there are no direct V_{DD} or V_{SS} connections, all the voltage supplied to the MOSFETs are by the inputs, therefore the voltage will slowly degrade as it moves to COUT and SUM.

Table 4-5: Maximum power dissipation and time delay of MBA-12T.

Maximum Power Dissipation (μW)			**361**
Time Delay (*ps*)	**SUM**	**1**	2.18
		2	5.66
		3	20.3
		4	10
		5	35.5
		6	19.5
	COUT	**1**	2.18
		2	19.2
		3	9.35
		4	25.6
	Maximum		**35.5**

4.2.4 Hybrid

The hybrid adder separates the SUM and COUT into two separate circuits. The SUM circuit is designed with pass transistor logic (PTL) as shown in Figure 4-7 and the simulation results of the circuit are shown in Figure 4-8. The COUT circuit is designed with conventional CMOS as shown in Figure 4-9 and the simulation results of the circuit are shown in Figure 4-10.

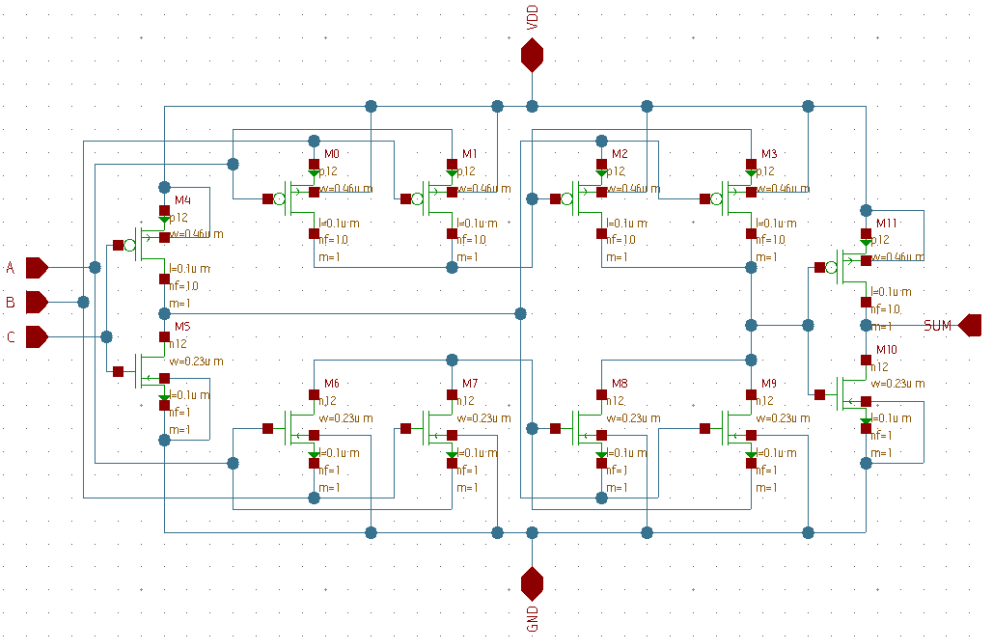

Figure 4-7: Hybrid SUM circuit schematic diagram.

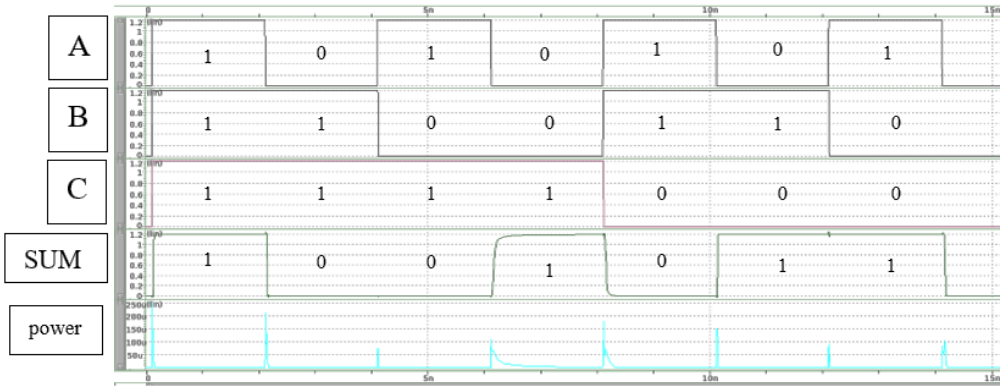

Figure 4-8: Timing diagram of hybrid SUM circuit.

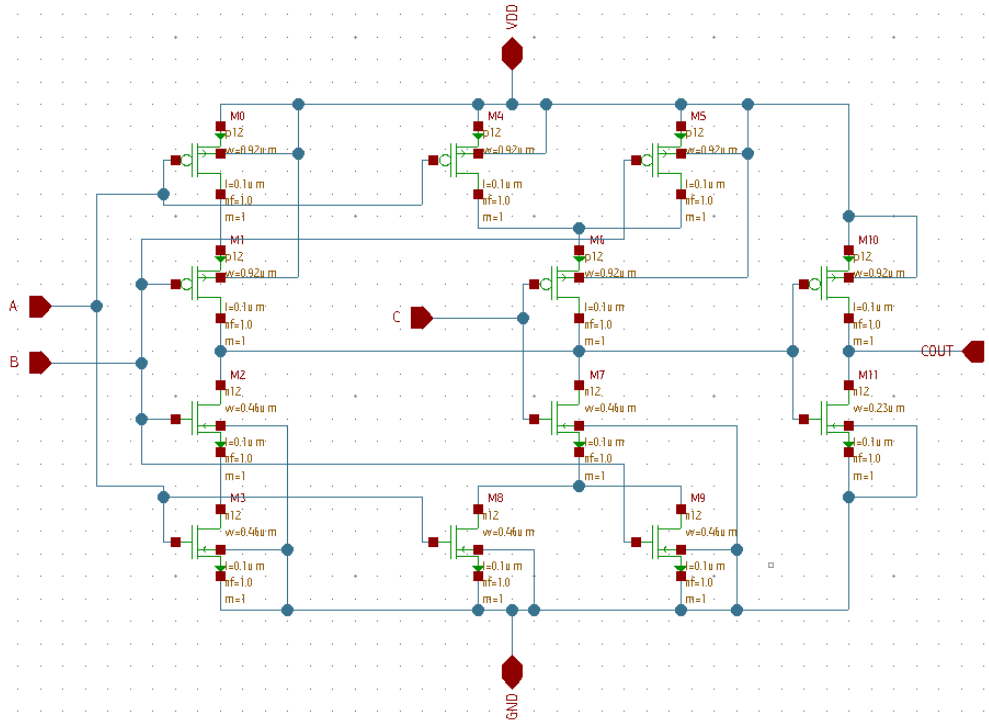

Figure 4-9: Hybrid COUT circuit schematic diagram.

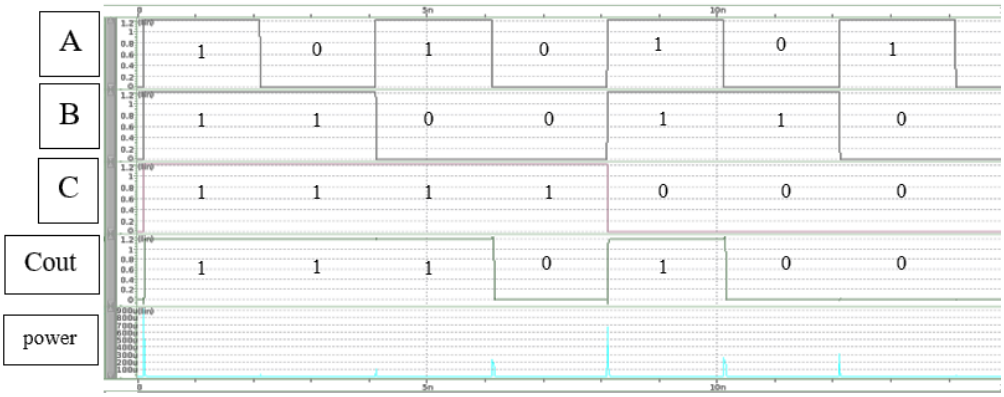

Figure 4-10: Timing diagram of hybrid COUT circuit.

The outputs of the simulation are compared to the truth table for verification. The maximum power dissipation and maximum time delay of both circuits are measured and tabulated in Table 4-6, the power dissipation of the design is measured as the sum of the power dissipation of both the SUM and COUT circuits since they operate at the same time and the critical path is determined to be the SUM path.

Table 4-6: Maximum power dissipation and time delay of hybrid design.

Power Dissipation (*mW*)	**SUM**		0.913
	COUT		0.254
	Total		**1.167**
Time Delay (*ps*)	**SUM**	**1**	27.2
		2	34.1
		3	59
		4	55.9
		5	20.5
		6	59
	COUT	**1**	13.9
		2	43.9
		3	11.6
		4	39.5
	Maximum		**59**

4.2.5 Simulation Summary

After completing the 4 adder designs simulation, it shows that the results obtained from the literature review cannot be compared directly, as they vary greatly with the simulation results. The table below summarizes the simulation results and power-delay products are calculated.

Table 4-7: Performance of the digital and hybrid adder design.

Adder Design	Power Dissipation (*mW*)	Time Delay (*ps*)	Power-Delay Product (*mW* × *ps*)
CMOS-28T	1.930	70	135.1
N-10T	0.236	37.4	8.8264
MBA-12T	0.361	35.5	12.8155
Hybrid	1.167	59	68.853

Among the 4 adders simulated, N-10T adder design has the lower power dissipation of 236μW and MBA-12T adder design has the shortest time delay. Even though N-10T design does provide the shortest time delay, as an overall design it has the best performance as shown by the power-delay product.

4.3 Proposed Analogue Adder Design Simulation

The finalized design is constructed in Synopsys Custom Compiler for simulation as shown in Figure 4-11 and the sizing of the transistors are listed in Table 4-8.

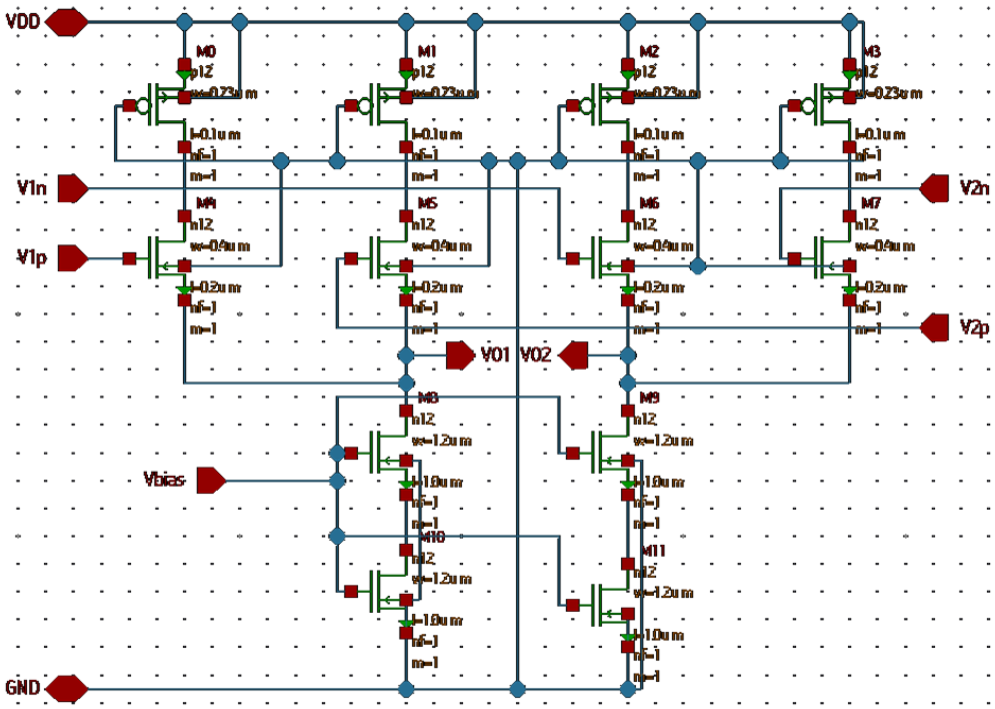

Figure 4-11: Finalized analogue adder design constructed in the custom compiler.

Table 4-8: MOSFET sizing used in the design.

Transistor	Type	Size (W/L) (*μm*)
M0	PMOS	0.23/0.1
M1	PMOS	0.23/0.1
M2	PMOS	0.23/0.1
M3	PMOS	0.23/0.1
M4	NMOS	0.4/0.2
M5	NMOS	0.4/0.2
M6	NMOS	0.4/0.2
M7	NMOS	0.4/0.2
M8	NMOS	1.2/1.0
M9	NMOS	1.2/1.0
M10	NMOS	1.2/1.0
M11	NMOS	1.2/1.0

The design can be easily modified to have more than two inputs since the additional input only requires extra voltage to current conversion part for the design to work. A four inputs analogue adder can be easily constructed from this design by attaching 4 more voltage to current conversion part to it as shown in Figure 4-12.

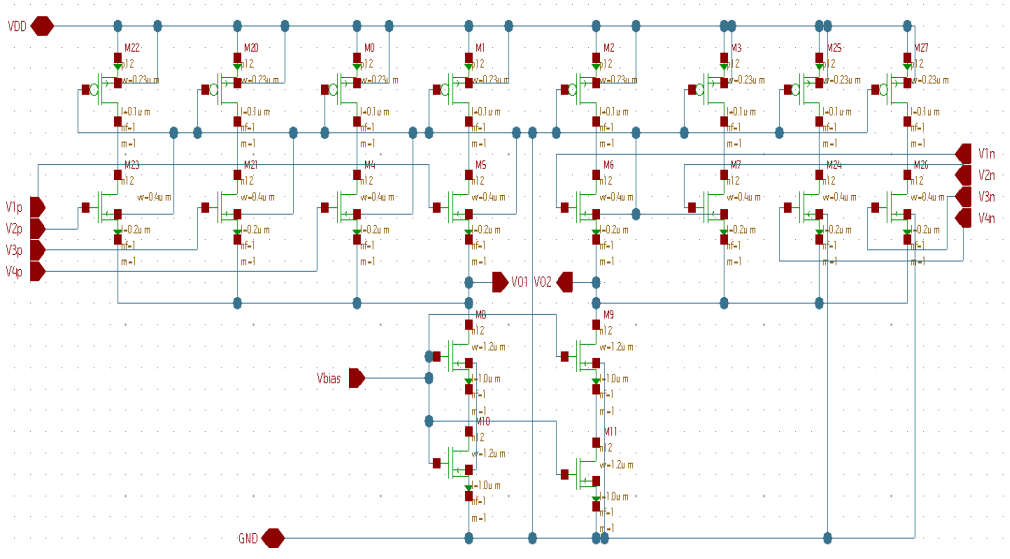

Figure 4-12: 4-Inputs analogue adder design.

4.3.1 Schematic Design Simulation Results

The simulation parameters are set according to Table 4-9 and the output wave view is shown in Figure 4-13.

Table 4-9: Simulation parameters.

Parameter	Values
V_{DD}	$3V$
V_{offset}	$2V$
V_{bias}	$0.5V$
Input Voltage	$-1.5V - 1.5V$
Temp	$25℃$

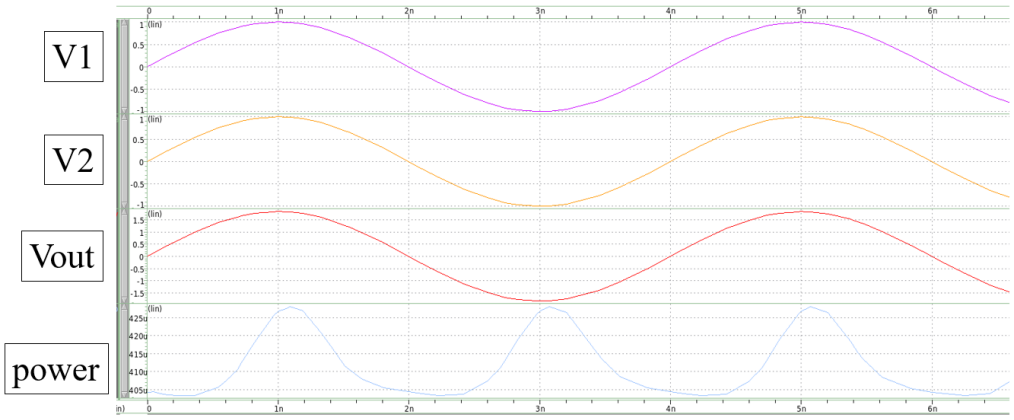

Figure 4-13: Pre-layout simulation output wave view.

For the NMOS to be in the saturation region, $V_{DS} > V_{gs} - V_{th}$ and $V_g > V_{th}$. With the input minimum value to be -1.5V and maximum to be 1.5V, it is calculated that V_{offset} has to be 2V to ensure the NMOSs (M4-M7) operates in the saturation region. For the current mirror to operate correctly the NMOSs (M8-M11) must operate in the saturation region, thus the V_{bias} is set to 0.5V.

The design can operate properly without including the transistor M0 to M3 (PMOSs), but including them greatly reduces the power dissipation of the design without affecting the output accuracy as shown in Table 4-10. For the design to operates at its best performance, both the inputs must be equivalent as the difference between them increase, the output accuracy will decrease and power dissipation will increase as shown in Table 4-11, these are mainly due to how the adder design operates. Therefore, all the simulation results are done with identical input voltages, and the overall simulation results for the analogue adder are shown in Table 4-12. Output time delay is not measured for the analogue design as the output is generated as soon as the inputs are injected to the design.

Table 4-10: Power dissipation reduction with the addition of the PMOS.

Input V_1 (V)	**Input V_2 (V)**	**Without PMOS**		**With PMOS**	
		V_{out} (V)	**Power Dissipation**	**V_{out} (V)**	**Power Dissipation**
0.5	0.5	0.933	$5.5mW$	0.933	$405\mu W$
1	1	1.85	$5.55mW$	1.85	$428\mu W$
1.5	1.5	2.74	$5.89mW$	2.74	$599\mu W$

Table 4-11: The effect of inputs difference.

Input V_1 (V)	**Input V_2 (V)**	**V_{out} (V)**	**Power Dissipation (μW)**
1	1	1.85	428
1.5	0.5	1.81	448
1.8	0.2	1.76	518

Table 4-12: Analogue adder pre-layout simulation results.

V_1 (V)	**V_2 (V)**	**V_{out} (V)**	**Power Dissipation (μW)**	**Accuracy (%)**
-1.5	-1.5	-2.74	599	91.33
-1.2	-1.2	-2.21	466	92.08
-0.9	-0.9	-1.68	418	93.33
-0.6	-0.6	-1.12	406	93.33
-0.3	-0.3	-0.561	404	93.50
0	0	0	404	100
`0.3	0.3	0.561	404	93.50
0.6	0.6	1.12	406	93.33
0.9	0.9	1.67	418	92.78
1.2	1.2	2.21	466	92.08
1.5	1.5	2.73	599	91

From the simulation results, it is shown that as the inputs voltage amplitude increase (analogue form input), the output accuracy will decrease. With the inputs level of 1.5V, the output produced is only 91% accurate (9% error), which is the lowest accuracy among the results. Inputs exceeding 1.5V/-1.5V are not simulated, since at those voltages level the NMOS will no longer operate ($V_{gs} < V_{th}$) or does not operate in the saturation region, thus the result generated will no longer be accurate. The power dissipation also increases with inputs voltage amplitude as more voltages are flowing into the MOSFET generating more power.

4.3.2 Layout Design and Simulation Results

The layout design constructed is shown in Figure 4-14, 2 layers of metal are used in the design and the spacing between the metal connections are keep at minimum to optimize the layout area. The total area of the layout is 22.628μm^2, 3.5μm (width) by 6.465μm (length). The layout design has passed all the test: DRC. LVS and LPE; and simulation output is shown in Figure 4-15.

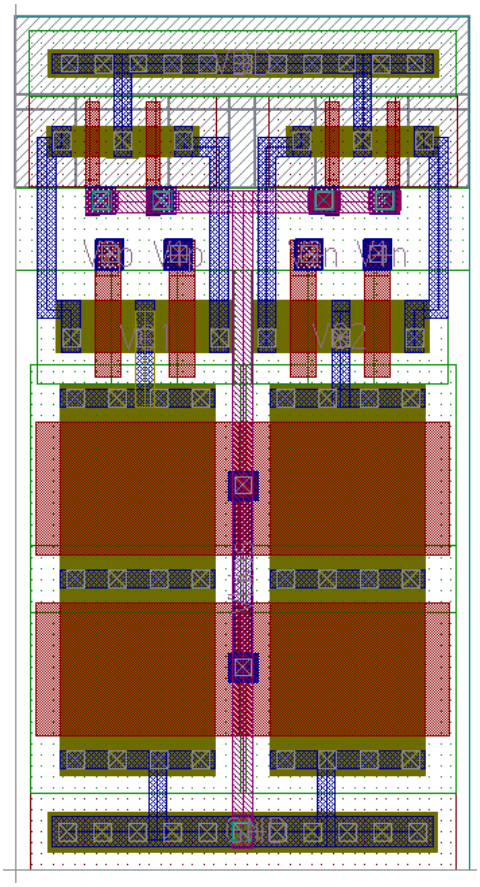

Figure 4-14: Analogue adder layout design.

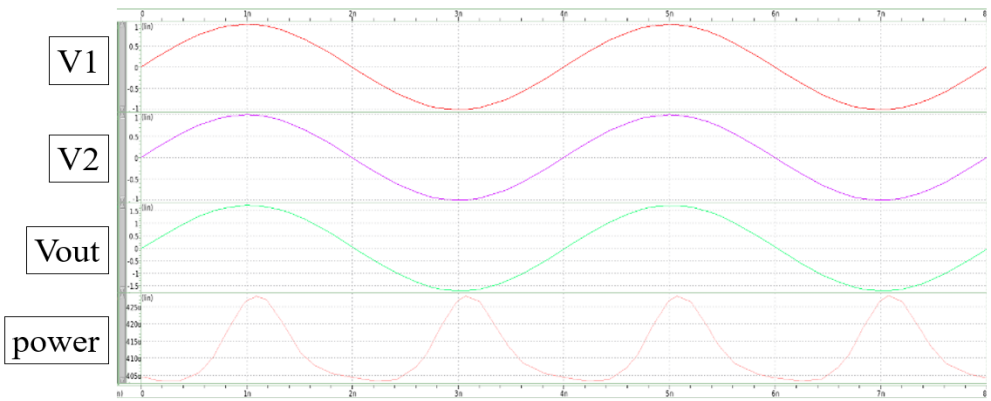

Figure 4-15: Post-layout simulation output wave view.

Since the design is not complicated and the connections are not extremely nested, the layout area for the design is not large. 22.628μm^2 layout area is only achieved after optimization and 2 layers of metal are used for the connection, else the design will have an area of 26.673 μm^2, 3.86μm (width) by 6.91μm (length). The difference may not be large but there is still a difference of power dissipation between them as shown in Table 4-13. Therefore, all the simulation results are done using the smaller layout area (22.628μm^2), and the overall simulation results for the analogue adder are shown in Table 4-14.

Table 4-13: Effect of layout area.

V_1 (V)	V_2 (V)	Width (μm)	Length (μm)	Area (μm^2)	V_{out} (V)	Power Dissipation (μW)
1	1	3.5	6.465	22.628	1.84	418
1	1	3.86	6.91	26.673	1.84	423

Table 4-14: Analogue adder post-layout simulation results.

V_1 (V)	V_2 (V)	V_{out} (V)	Power Dissipation (μW)	Accuracy (%)
-1.5	-1.5	-2.74	574	91.33
-1.2	-1.2	-2.21	445	92.08
-0.9	-0.9	-1.67	408	92.78
-0.6	-0.6	-1.11	402	92.50
-0.3	-0.3	-0.560	400	93.33
0	0	0	400	100
0.3	0.3	0.559	400	93.17
0.6	0.6	1.11	402	92.50
0.9	0.9	1.68	408	93.33
1.2	1.2	2.20	445	91.67
1.5	1.5	2.74	574	91.33

From the post-layout simulation results, it is shown that the results obtained are similar to those of the pre-layout, the difference in the output voltages are less than 1% and the power dissipation decrease by some distance. The reduction of the power dissipation is mainly due to the optimization of the layout since there is no longer any redundancy in the design.

For digital adder cascading is normal practice to take in more inputs, for example cascading 4 1-bit full adders together to make a 4-bit full adder, but the layout area of that 4-bit full bit full adder is also equivalent to 4 times the layout area of the 1-bit full adder. For this design, modifying it to take in more inputs does not increase the overall layout area by a lot as shown in Table 4-14.

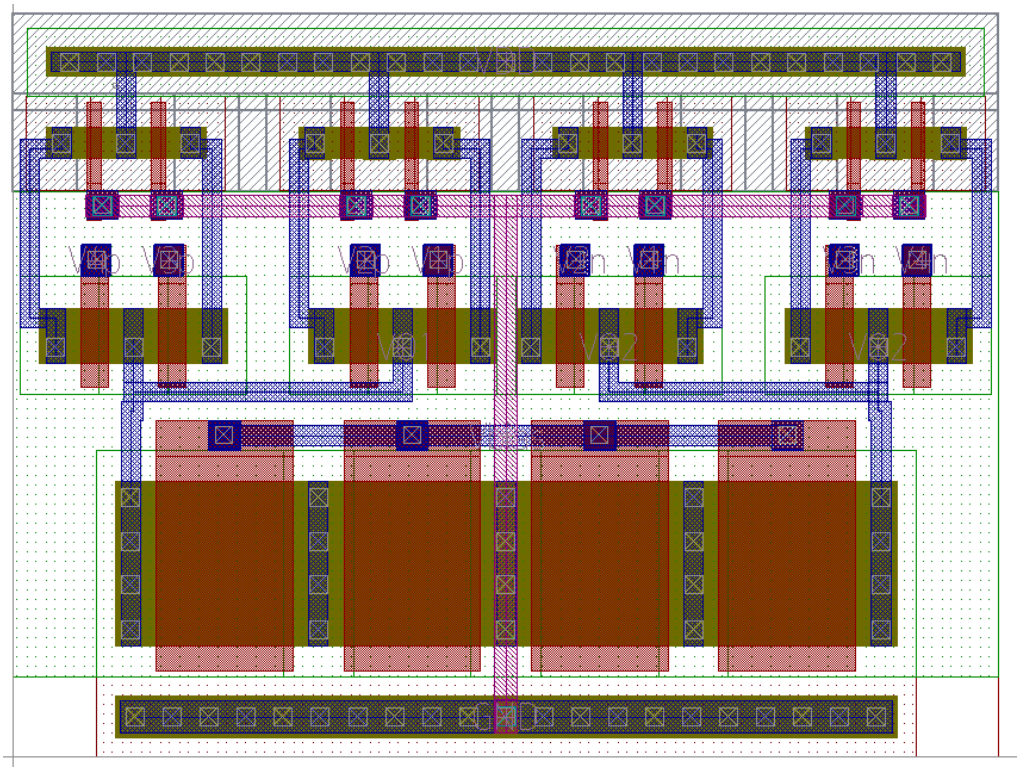

Figure 4-16: 4-Inputs analogue adder layout design.

The layout area of the 4-inputs analogue adder is only 39.024μm^2, 7.2μm (width) by 5.42μm (length), which is only 1.72 times the layout area of the 2-inputs analogue adder.

4.4 Summary

In this chapter, the 4 chosen adder designs are constructed and simulated, the results obtained are then compared against each other, among the four adder designs, N-10T design provided the best performance. On the other hand, the proposed analogue adder design is explained and both the schematic and layout for the design are completed. The proposed analogue adder design was not able to achieve 100% accuracy due to the current flow accuracy. In theory, the input voltage can be directly be converted to current forms, but in reality, the current-voltage conversion is not 100% accurate, the converted current is not accurately representing the input voltage. Therefore, this inaccuracy in conversion leads to the design unable to achieve 100% accuracy. The analogue adder design has met all the criteria and specifications previously specified.

For an analogue to digital comparison, the proposed analogue adder design is going up against N-10T. Since the analogue adder design performance

is dependent on the inputs, the analogue design cannot be directly compared to the N-10T design, thus only 1*V*-inputs performance is used in the comparison. The difference in their design and performance are tabulated in Table 4-15.

Table 4-15: Analogue adder design vs N-10T design.

Aspects	Analogue Adder	N-10T
Design Complexity	simple	simple
Operational Principle	~ V/I conversion ~ KCL ~ current mirror	~ logic Sum = $C_{in} \oplus A \oplus B$ $C_{out} = AC_{in} + BC_{in} + AB$
Power Dissipation (*μW*)	428	236
Time Delay (*ps*)	-	37.4
Accuracy	> 90%	-
Modifiability/ Flexibility	High	Low

The analogue adder designed to operate for input voltage ranging from -1.5*V* to 1.5*V* and not for specific inputs voltage level and the MOSFETs in the design are always at 'on state', thus the power dissipation is higher compared to N-10T. N-10T has a perfect accuracy, since digital adder only outputs 2 levels, unlike analogue adder which the output has ranges. In overall, analogue adder design provided more advantages over the N-10T design.

CHAPTER 5

CONCLUSIONS AND RECOMMENDATIONS

5.1 Conclusions

A CMOS low power analogue adder design is proposed and its performance is validated through schematic and layout design simulations. The details of the analogue adder design are listed in the table below:

Table 5-1: CMOS low power analogue adder description.

Aspects	Description / Value
Operational Principle	~ current mode technique (V/I conversion) ~ KCL ~ current mirror
Number of Transistor	12
Inputs Voltage Range	$-1.5V - 1.5V$
Operation Speed	Fast
Maximum Power Dissipation	$574\mu W$ (with $\pm 1.5V$ inputs)
Accuracy	> 90%
Layout Area	$22.628\mu m^2$
Features	~ small modification to increase the number of inputs ~ small increases in layout area corresponding to the number of inputs increase

Synopsys Custom Compiler is used to construct the analogue adder custom design. The tools provided in the custom compiler are extremely helpful in design checking, error correction and analysing the results. The analogue adder design does not require the first row of PMOS for its operation, but the addition of them reduces the power dissipation from a few milliwatts to a few hundred microwatts. The power dissipation is reduced by almost 10 times from its original values, thus greatly improving the performance of the design. For the design to perform at its best, the inputs must be even, else both the accuracy and power dissipation are affected. As the design is simple and there is no longer propagation path, the design output is generated as fast the inputs are injected, there is no time delay detected which can be measured in the custom compiler.

In the layout design, the layout area of the design is optimized to improve design performance. The layout design is completed without any rule violations and the layout design matches with the schematic design, avoiding any operational mismatch between them. The post-layout results showed that power dissipation has been further decreased by a few microwatts, mainly due to the layout optimization and parasitic extraction. Overall, the analogue adder designs showed low power dissipation and great performance.

5.2 Recommendations for future work

Based on the formulas, summing two analogue voltage together may be very easy, but in term of actual world implementation it is very hard. Even though the analogue adder is able to achieve greater than 90% accuracy, it can still be further improved. Implementing an offset compensation or auto-zero techniques into the design can greatly improve output accuracy. The compensation techniques require a calibration phase where the offset voltage of the building blocks is sampled and dynamically stored in a memory. Another factor that leads to the output incorrectness is the current mirror. Despite a cascode current mirror is being used instead of a basic current mirror, the current is still not perfectly mirrored, there is a difference between the currents exiting the nodes. For the analogue adder design to work perfectly, the currents exiting the two nodes being the same is crucial. Eliminating these differences and ensuring the currents exiting the nodes are identical are crucial to the accuracy of the output.

Despite the power dissipation of the analogue adder design has been greatly reduced, it can still be further lowered. Based on the analogue adder design, all the MOSFETs are operational (‘on’) all the time, even if there are no inputs, this is a problem faced in the design. In digital circuits, power is dissipated from a certain part of the design which is triggered, whereas other parts remain idle and there is almost zero power dissipation. This is a good characteristic of a design, if this was successfully implemented into the analogue adder design, it will greatly reduce the power dissipation.

In this project, 90nm process technology and educational based library are used to design the analogue adder. The results from this do not represent actual word performance, as the process technology has been greatly improved.

Comparing to the process technology used in industrial nowadays: 14*nm* and 7*nm*, 90*nm* process technology can be considered as very old technology. With smaller process technology, the layout area of the design can be reduced and further optimized, producing greater performance with lower power dissipation.

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