DESIGN OF 6-STAGE PIPELINE PROCESSOR

By

TENG WEN JUN

A REPORT

SUBMITTED TO

Universiti Tunku Abdul Rahman

in partial fulfillment of the requirements

for the degree of

BACHELOR OF INFORMATION TECHNOLOGY (HONOURS)

COMPUTER ENGINEERING

Faculty of Information and Communication Technology

(Kampar Campus)

JAN 2021

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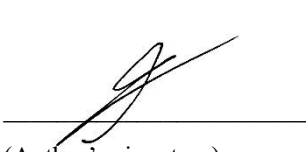

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I would like to express my sincere thanks and appreciation to my supervisors, Mr. Mok Kai Ming who has given me this bright opportunity to engage in a digital system design project. It is my first step to establish a career in digital system design field. A million thanks to you.

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ABSTRACTS

This project is about the design and implementation of RISC 6-stage pipeline processor for academic purpose. The main objective of this project is to improve the performance of the current RISC32 5-stage pipeline processor that developed in Universiti Tunku Abdul Rahman which is under Faculty of Information Technology by increasing the stages from 5 stages to 6 stages. After reviewing the timing delay of each stage, the longest delay of the 5-stage pipeline processor is accessing the memory stage which will reduce the performance due to the imbalance among the pipeline stages. This longest delay will slow down the clock rate of the processor. Thus, this project is initiated to divide the memory unit (cache) into 3 stages. Cache unit access will require 3 clock cycles if cache hit detection occur. Some modifications on cache unit were done to increase the performance of the performance. The instruction cache is pipelined at the appropriate location while distributing the components among 3 stages to achieve a balance stage delay. This project is modelled using Verilog code and a test program will be developed to test the functionality and compatibility of the newly design pipelined cache unit and RISC32. Lastly, Xilinx Vivado is used to synthesis and implement it to get the timing delay of each stage.

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LIST OF ABBREVIATIONS

ALU	Arithmetic Logic Unit
CISC	Complex Instruction Set Computer
CP 0	core processor 0
CPU	Central Processing Unit
EXE	Execute
FP	Floating Point
FPGA	Field Programmable Gate Array
HDL	hardware description Language
I/O	input / output
ID	Instruction Decode
IF	Instruction Fetch
J	Jump
jal	Jump and Link
MEM	Memory Access
MIPS	Microprocessor without Interlocked Pipeline Stages
PC	Program Counter
RISC	Reduced Instruction Set Computer
RTL	Register Transfer Level
TC	Tag Check
WB	Write Back

Chapter 1: Introduction

1.1 Background Information

1.1.1 MIPS

MIPS stand for Microprocessor without Interlocked Pipeline Stages. In 1984, the MIPS processor is designed by researchers at Stanford University. According to Jones (2016), RISC, or Reduced Instruction Set Computer processors typically support small and simple instruction compared to CISC. MIPS design for pipelining efficiency, emphasizes a simple load-store instruction set and competence as a compiler target (Patterson and Hennessy, 2001, A-33). MIPS is used instead of Intel 80x86 because it has simple design and high performance as embedded processor as well as large market for embedded apps. Nowadays, MIPS architecture supports 64-bit addressing and operation and high-performance floating point. This is the reason why it is popular in the embedded systems implementation such as video game consoles. The MIPS architecture products include the MIPS32 and MIPS64.

1.1.2 MIPS Instruction Format

Instruction format is the layout of the instruction bits in field. There are 3 basic types of instruction formats. These instruction formats include:

- I-format: for arithmetic or logic, data transfer and branch.
- J-format: for j and jal.
- R-format: for all other instructions.

Figure 1.1.2.1 shows the instruction layout.

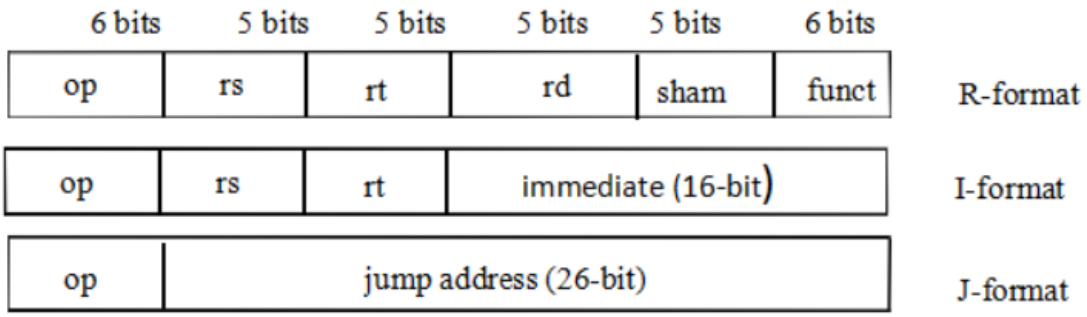

Figure 1. 1. 2. 1: Instruction layout for MIPS

1.1.3 MIPS Execution Cycle

The execution of an instruction can be done in 5 basic stages and the execution of an instruction is partially completed with each stage. These 5 basic stages include:

- IF: Instruction fetch and update PC
- ID: Instruction decode and registers fetch
- EX: Execute
- MEM: For lw and sw instruction. Data will be written and read from data memory
- WB: Write back the result data into the register file

"Stages" implies datapath resources at each stage. Figure 1.1.1 shows the instruction execution cycles for lw instruction. Besides, the structural view for datapath is shown in Figure 1.1.3.1.

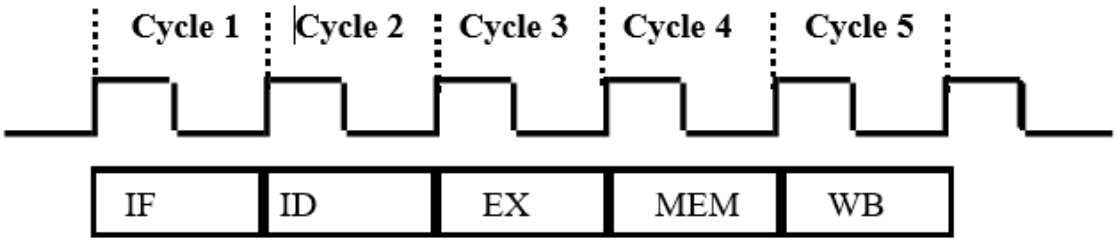

Figure 1. 1. 3. 1: Instruction execution cycles for lw instruction

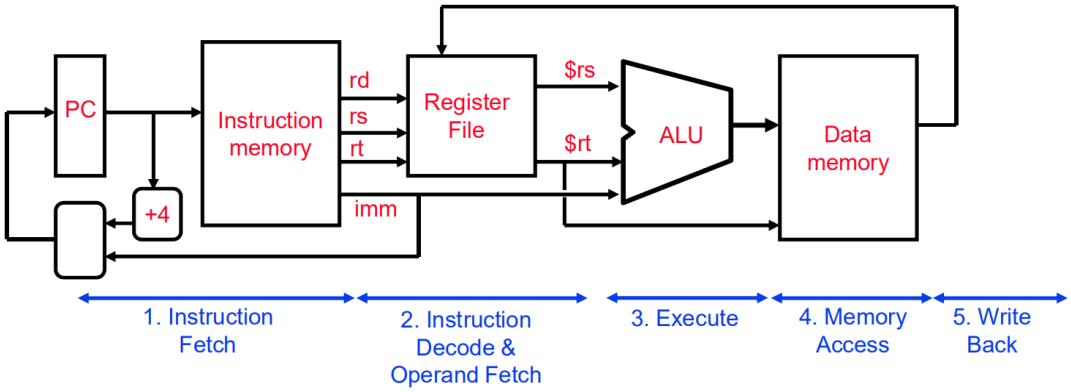

Figure 1. 1. 3. 2: Structural view for datapath

1.1.4 RISC

RISC, also known as Reduced Instruction Set Computer. It is a type of microprocessor architecture that utilizes a small, highly-optimized set of instructions. According to Gatner (n.d), RISC has 5 design principles:

- Single-cycle execution
- Hard-wired control, little or no microcode
- Simple instructions, few addressing modes
- Load and store, register to register design
- Efficient, deep pipelining

UC-Berkeley, Stanford, and IBM started the first RISC projects in the late 70s and early 80s. Nowadays, there are a lot of computer systems that take advantage of a RISC processor. For examples, A13 Bionic, which integrated in all iPhone 11 models and the A12X Bionic, which integrated in iPad Pro.

1.1.5 Pipelining

Pipelining is a usage strategy whereby more than 1 instruction are overlapped during execution and it exploits parallelism that exists among the actions expected to execute an instruction (Patterson and Hennessy, 2001, C-2). Performance is improved by increasing throughput which is average instructions completed per clock cycle. The basic pipeline processor for RISC32 has only 5 stages. Figure 1.1.5.1 illustrates the hardware components allocate in each pipeline stages of the 5-stage pipeline processor RISC32.

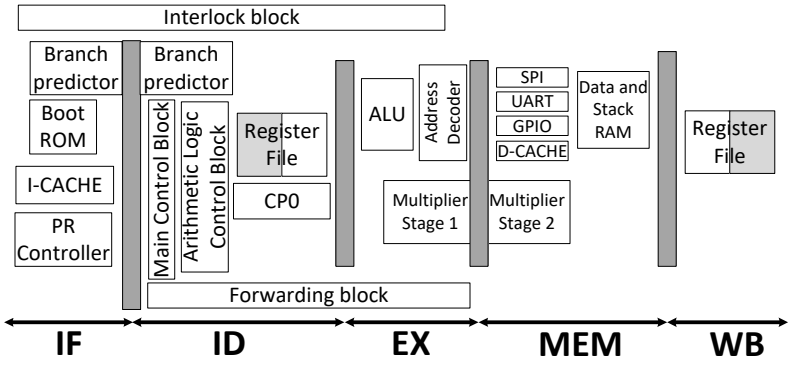

Figure 1. 1. 5. 1: Abstract view of 5-stage pipeline processor

1.2 Problem Statement

Basic 5-stage pipeline processor increases the CPU instruction throughput. However, clock rate of the processor is reduced due to the imbalance timing delay among the pipe stages since the clock rate must fulfill the delay of the longest stage to execute the instruction without error (Patterson and Hennessy, 2001, C-10). This problem is very important because it will slow down the clock rates of the processor. Table 1.2.1 shows the timing delay for the pipeline stages. MEM stage has the longest timing delay in the pipeline stage which is 17.75 ns. Thus, the length of the clock period must be 17.75 ns even though the other stages have a shorter timing delay. The clock rate of the processor is determined by the longest time delay in the pipeline stages.

Pipeline Stage	IF	ID	EX	MEM	WB
Timing delay	13.762 ns	12.366 ns	14.873 ns	17.75 ns	3.983 ns

Table 1.2.1: Timing delay for 5 pipeline stage.

*These values are derived from the post-synthesis static timing of the RISC32 using Xilinx Vivado 2019.2 IDE. The details of the timing can be found in Appendix A.

Clock rate of 5-stage pipeline processor = $\frac{1}{17.75\ \text{ns}}$

= 56.338 MHz

1.3 Motivation

Motivation of this project is to improve the performance of the MIPS 5-stage pipeline processor by decomposing the instruction memory unit into 3 stages to achieve higher clock rate. As a result, the speed of execution of instructions can be run faster.

1.4 Project Scope

The project scope will mainly focus on designing and implementing the 6-stage pipeline processor. The specifications of the 6-stage pipeline processor will be functionally verified by using testbench. Besides that, the 6-stage pipeline processor will be synthesized on the Field Programmable Gate Array (FPGA) technology.

At the end of this project, a comprehensive documentation, a piece of software and simulation result are expected to be delivered.

1.5 Project Objectives

The major objective of this proposed project is to design and implement the 6-stage pipeline processor by decomposing the instruction memory access of basic 5-stage pipeline processor to achieve a higher clock rate. However, it can also be divided into several sub-objectives and they are listed accordingly in below.

- Design level
    i. To design and develop a 6-stage pipeline processor that can meet all the specifications correctly by using Verilog HDL.
- Verification level
    i. To develop a complete testbench to verify all the functional correctness of the 6-stage pipeline processor.
- Logic synthesis level
    i. To synthesis and integrate the 6-stage pipeline processor which is the FPGA technology

1.6 Impact, Significance, and Contribution

After this project is done, it can provide a complete 6-stage pipeline RISC32 processor with the following documentation:

- A completely functional well-developed 6-stage pipeline processor which is written in Verilog in the form of synthesis-ready RTL.
- A fully developed verification specification of the 6-stage pipeline processor. The verification specification contains adequate verification techniques, verification methodology, test plan of each instructions and testbench architecture.
- Timing report of the project that show the delay of each stages due to the wire and logic delay.

This project can contribute to develop an environment that stated above by providing support to the hardware modeling research work. Besides, a researcher will be able to further improve the performance of the processor by decomposing the stage which is time critical. Thus, the developer can speed up their research work and can be done easier.

Chapter 2: Literature Review

2.1 MIPS R4000 Background

To solve the performance issue due to the imbalance among pipe stages, MIPS R4000 processor family is introduced. A Computer Business Review (1991) state that in 1991, "first true 64-bit RISC microprocessor", which is R4000 processor family is introduced and it was developed by MIPS Computer Systems. R4000 implements MIPS64 but uses a deeper pipeline than that of our 5-stage design both for FP programs and integer (Patterson and Hennessy, 2001, C-61). The advantage of this deeper pipeline is to increase the clock rates. To increase the clock rates, the 5-stage pipeline processor is decomposed into 8 stages. The extra stages come from decomposing the memory unit because the cache access has the longest delay in the processor. Sometimes, this type of deeper pipelining is called superpipelining. Figure 2.1.1 shows the R4000 processor internal block diagram.

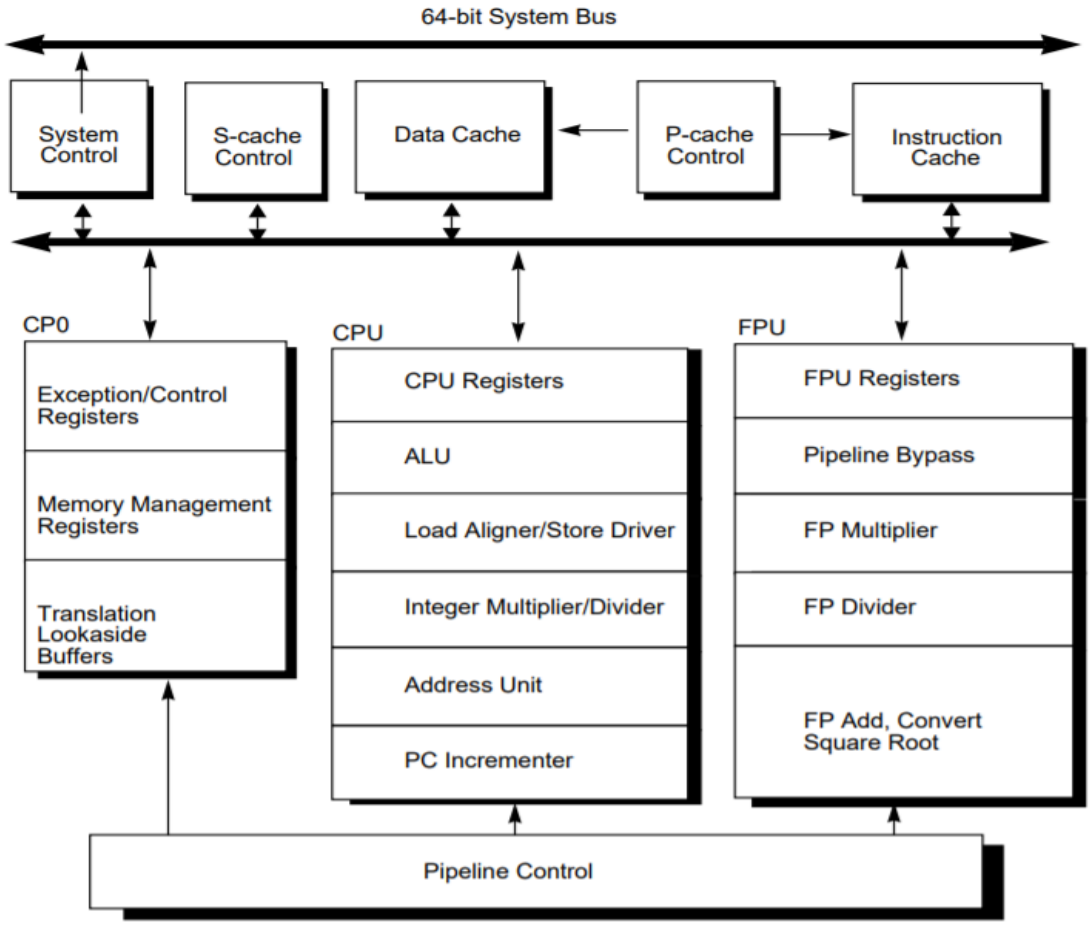

Figure 2. 1. 1: R4000 processor internal block diagram (Heinrich, 1994, Fig 1-1, p.10)

2.2 MIPS R4000 CPU Pipeline

The 8-stage pipeline processor can execute more instructions at once compared to the basic 5-stage processor. The execution of an instruction in R4000 can be done by 8 stages. These 8 stages include:

■ IF—First half of instruction fetch, program counter selection happens here, PC<=PC+4, and then initiation of instruction cache access.
■ IS—Second half of instruction fetch, instruction cache access completely.
■ RF—Instruction cache hit detection →instruction decode → register fetch, hazard checking.
■ EX—Execution, which includes ALU operation, condition evaluation, branch-target computation and calculate effective address.
■ DF—Data fetch, first half access to the data cache.
■ DS—Second half access to the data fetch, data cache access complete.
■ TC—Tag check, data cache hit detection.
■ WB—Write-back the result into the register file.

Figure 2.2.1 shows the 8-stage pipeline structure using an abstracted version of data path. At IF and IS stages, the processor accesses the instruction cache with a new cache access starting every cycle. An instruction word is available at RF stage because the cache hit detection is done at RF stage, while fetching the registers. This is the reason why the instruction memory is operating through RF stage as shown in the Figure 2.2.1. Since the data cannot be written into the register file before cache hit detection, to access data memory, TC stage is required.

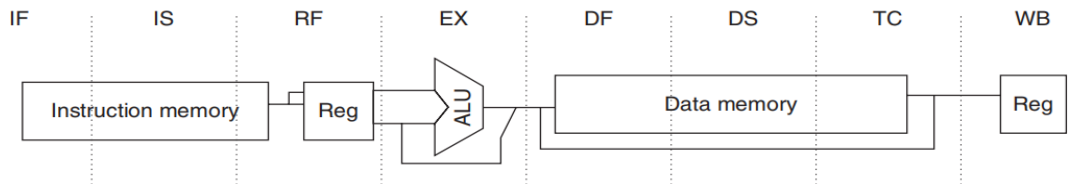

Figure 2. 2. 1: R4000 CPU pipeline structure

Superpipelining splits the data and instruction memory references across 2 stages. Therefore, the logic is distributed more evenly across pipeline stages. Figure 2.2.2 shows the pipeline activities.

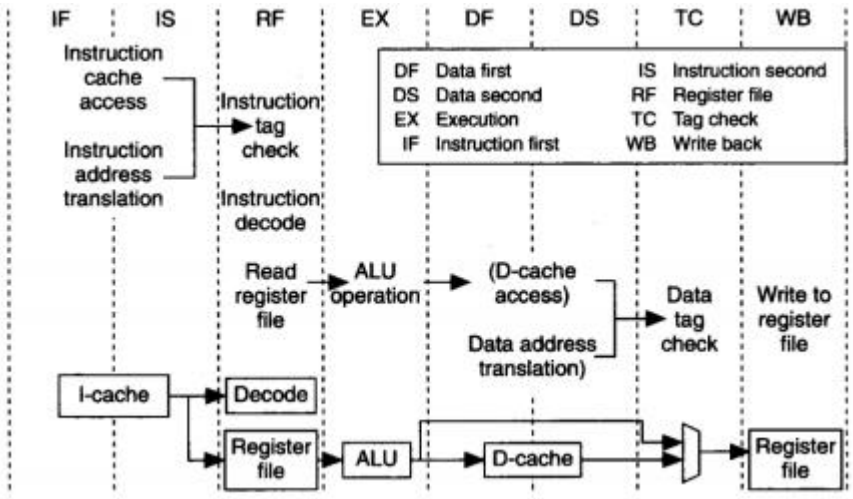

Figure 2. 2. 2: Pipeline activities

2.2.1 Load Delay

The CPU pipeline leads to a 2-cycle load delay. This is because the 32 bits data is only available at the end of the cache access in DS stage. Figure 2.3.1 shows the 2 clock cycles for load delay because the data is only available at the end of DS stage which is clock cycle 6.

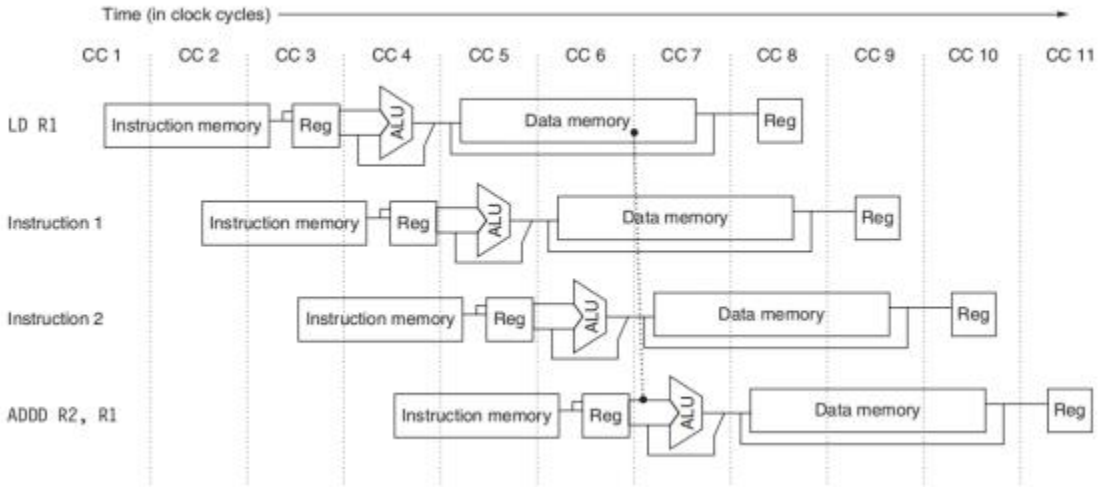

Figure 2. 2. 1. 1 : CPU pipeline load delay

The hardware will interlock and slip the instructions if there are 2 instructions use the load's result right after a load instruction in their EX stage. Figure 2.2.1.2 shows during the slip, the DF, DS, TC and WB stages of the pipeline shift forward while the IF, IS, RF, and EX stages do not.

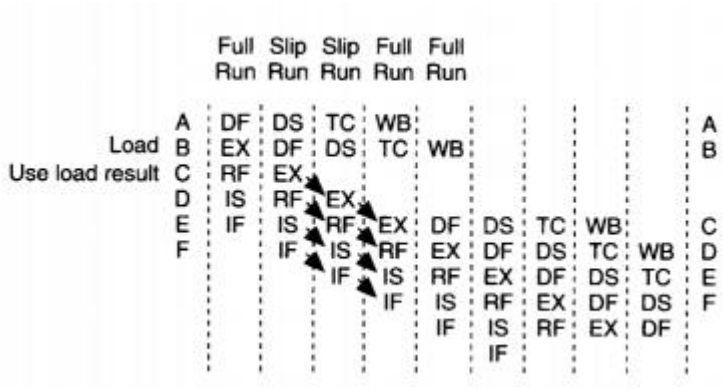

Figure 2. 2. 1. 2: Load interlock/slip cycle

2.2.2 Branch Delay

For branch instruction, there are 3-cycle delay because the branch condition is executed at EX stage. Figure 2.2.2.1 shows the basic branch delay is 3 cycles.

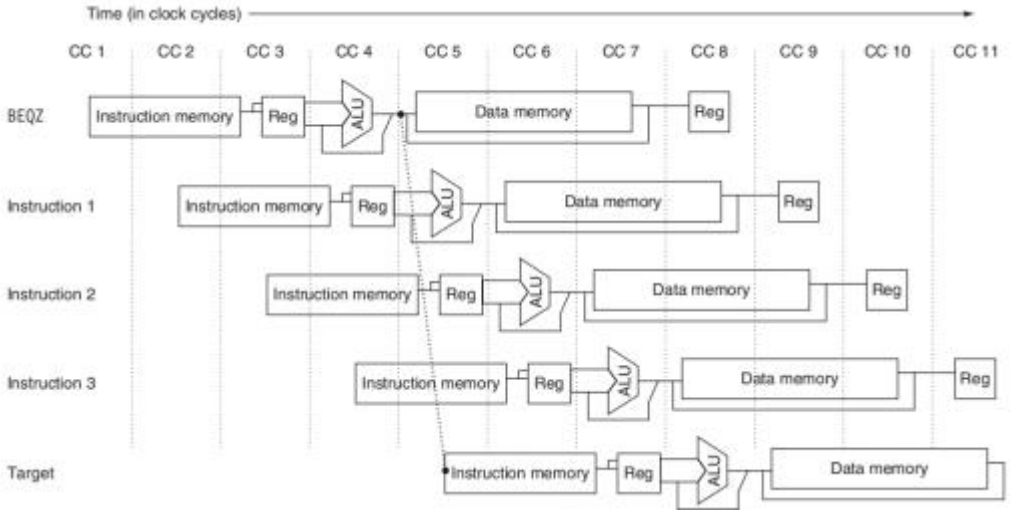

Figure 2. 2. 2. 1: CPU pipeline branch delay

Based on the Figure 2.2.2.1, there are 3 instructions have entered the pipeline. If the branch is not taken, all the instructions that already entered the pipeline can be executed by processor with no penalty. However, if the branch is taken, the MIPS architecture allows one instruction after the branch target instruction. The other 2 instructions that have already entered the pipeline will be discarded. A predicted-not-taken strategy for the remaining branch delay's 2 cycles is used by R4000 processor.

2.3 Memory Organization

In the logical memory hierarchy, the position of caches placed between the CPU and main memory (RAM). The main function of caches is to increase the speed of memory access. Figure 2.3.1 shows the R4000 system memory hierarchy. In figure 2.3.1, each functional block has larger capacity to hold data than the block above it. For example, main memory has a larger capacity than the secondary cache. Besides, the time to access each functional block is longer than any block above it. For example, the main memory takes longer time to access data compared to the CPU on-chip registers.

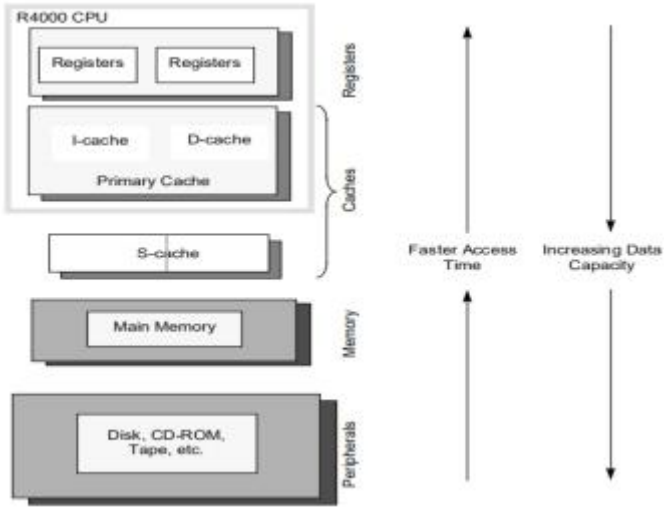

Figure 2. 3. 1: R4000 system memory hierarchy

Based on the figure 2.3.1, we can observe that the R4000 processor has 2 on-chip primary caches and one off-chip secondary cache. One is instruction cache which stores instructions while the another one is data cache which stores data.

2.3.1 Organization of Instruction Cache

Instruction cache in the processor is read only memory. It stores all the instructions that will be executed. The R4000 processor instruction cache used direct-mapped cache mapping technique, index with a virtual address, check with a physical tag and has 8 words cache block.

2.3.2 Organization of Data Cache

Data cache in the processor is used stores all the variable that will be needed to execute. For example, lw and sw instructions will use the data cache in the processor. The R4000 processor used direct-mapped cache mapping technique, write back policy, index with a virtual address, check with a physical tag and has 8 words cache block.

2.3.3 Cache Write Policy

There are 2 cache write policy in accessing the cache unit:

Write-through scheme: Data is written into both cache and memory. Data in the cache and memory is the same. Thus, a dirty bit is not required for the cache access. One of the advantages of this policy is easier to implement and it is suitable for use in multilevel caches. However, the speed of writing the data is too slow because it is written at the speed of the memory

Write-back scheme: Main memory is not updated with this policy because the data is written into cache only. It allows the data in the cache and memory to be not the same. Thus, a dirty bit is required for each block to indicate a block is modified. Dirty block which is kept in write buffer will be evicted when block replacement occurs. One of the advantages of this policy is it can reduce the frequency in writing into main memory. However, it needs to update the block in memory if evicting a dirty block when read miss and it is harder to implement compared to write-through scheme because it has a complex hardware.

For the R4000 processor, write-back scheme is implemented to manage its caches.

2.4 Cache Operation

Cache is a fast temporary data storage which its speed is 10 to 100 times faster than normal memory. To decompose the cache unit, the operation or procedure of cache unit need to be studied before starting the project. A cache unit with write-back scheme has been modelled by Goh Dih Jian. A write buffer is needed for the policy to store dirty block when there is a block replacement occur and write back to secondary memory later. This modelled cache can be used as read only memory (instruction cache) and data cache. Figure 2.4.1 shows the block diagram of cache unit modelled by Goh Dih Jian.

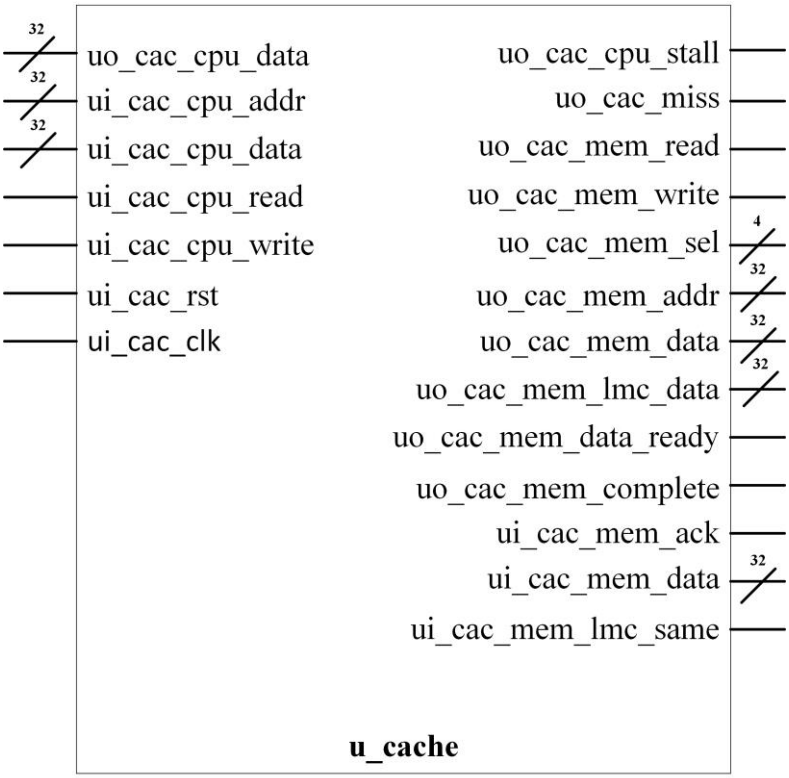

Figure 2. 4. 1: Block diagram of cache unit

2.4.1 Scenario for Cache

Cache hit

- CPU sends 32 bits address and read signal to cache unit.
- 15 bits tag bit and a valid bit are read for cache hit detection
- If there is a cache hit, no pipeline stalling is needed, and the 32 bits data will be read in 1 clock cycle.

Write hit

- CPU sends 32 bits address and write signal to cache unit.
- 15 bits tag bit and a valid bit are read for cache hit detection
- If there is a cache hit, no pipeline stalling is needed.
- Prepare dirty = 1 because it is a write back scheme and data from CPU write into cache.
- Data is written into cache.

Read miss

- CPU sends 32 bits address and read signal to cache unit.
- 15 bits tag bit and a valid bit are read for cache hit detection
- If cache hit signal is de-asserted, it means read miss and cache control will be activated.
- The address (15 bits tag and 12 bits index) is used to compare with (15 bits tag and 12 bits index) which is stored inside AFIFO for AFIFO hit detection.
- The entire pipelines in the processor will be stalled to wait for completion of block transfer from SDRAM OR AFIFO.

- If there is cache miss and AFIFO hit
    - It means that latest copy of data is in AFIFO.
    - Read the data in the AFIFO and copy it to a temporary buffer
    - The block from temporary buffer will be transfers to cache and CPU
- If there is cache miss and AFIFO also miss
    - It means that the latest copy of data is in SDRAM.
    - Use the physical address to copy the required block of data from SDRAM into cache unit
- When data transferring is completed, then the hit signal will be asserted.
- Resume the pipeline stages and continue for execution of instruction.

Write miss

- CPU sends 32 bits address and write signal to cache unit.
- 15 bits tag bit and a valid bit are read for cache hit detection
- If cache hit signal is de-asserted, it means write miss and cache control will be activated.
- Evicted cache block will be moved to write buffer if it is dirty.
- Start to transfer a block of data from SDRAM into cache
- Stall the entire pipelines of the processor to wait for completion of block transfer from SDRAM control.
- Dirty bit = 1, valid bit = 1, 15 bits tag and 32 bits data from CPU will be written into cache unit.
- After the process is done, the entire pipeline stages will be continued.

Chapter 3: Proposed Method/Approach

3.1 Design Methodology

There are 3 types of design methodologies available in the design process for digital system:

- Top-down design methodology
- Bottom-up design methodology
- Mixed design methodology

In this project, the top-down design methodology will be used for designing and developing the 6-stage pipeline processor. In top-down design methodology, the top-level representation of a chip is first defined, followed by the lower-level representations like ALU, cache unit and datapath unit based on some important criteria such as functionality and speed.

3.2 RTL Design Flow

Figure 3.2.1 shows The RTL design flow that will be used throughout the project. In this project, the micro-architectural level design will be focused more on the RTL design flow.

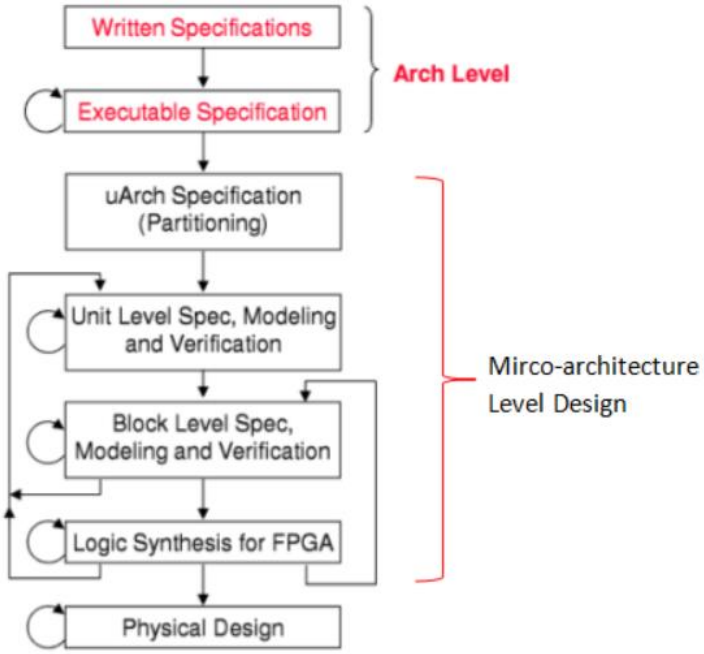

Figure 3. 2. 1: RTL design flow

3.2.1 Micro-architecture Specification

Micro-architecture specifications describe the internal design of the pipelined I-cache unit, cache controller block, and branch predictor unit. The internal design of the pipelined I-cache and branch predictor will be described. The following information will be included in the unit level of the pipelined I-cache and branch predictor:

- Functionality description
- Input and output pin description
- Micro-architecture of the unit
- Test plan

While the block level of cache controller will have the following information:

- Functionality description
- Input and output pin description
- Internal operation: FSM
- Block diagram
- Test plan

3.2.2 RTL Modelling and Verification

After the RISC32 are verified for functional correctness and requirements, then the logic synthesis and implementation will be carried out on the FPGA technology in this project. If the design of RISC32 does not meet all the specified functional requirement, then the design flow will be repeated.

3.2.3 Logic Synthesis for FPGA

The RISC32 is ready for logic synthesis and implementation when it has been functionally verified. RTL codes will be converted into an optimized gate level representation. If all the necessary specifications are met, the gate level netlist is ready for physical design. Else, corrections need to be made based on the RTL model and gate level netlist

3.3 Design Tools

3.3.1 Modelsim PE Student Edition 10.4a

For this project, which is HDL (Hardware Description Language) based design, Modelsim from Mentor Graphic will be used for simulation and debugging. There are many versions of Modelsim, but student edition will be used for Verilog design simulation because it is free of charge and it can be downloaded from its official website. It supports both Verilog and VHDL languages. Besides, this simulator can also check the syntax of the code and provide waveform simulation which play the most important part in developing the project. To verify the functionality of the model after writing a testbench, the timing diagram and the waveform are very useful.

3.3.2 Xilinx Vivado 2019.2

This software will be used to synthesis and implement the project and get the static timing analysis of each stages. This software is designed for HDL designs analysis and synthesis. Artix-7 board will be used to run implementation of this project.

3.4 Timeline

3.4.1 Gantt Chart for Project I

Task Name	Duration	Start Date	End Date	week											
	(weeks)			1	2	3	4	5	6	7	8	9	10	11	12
Study the existing work that being developed	2	8/6/2020	22/6/2020												
Develop test for the existing RISC 32 pipeline processor	2	22/6/2020	6/7/2020												
Learn how to get timing analysis using Xilinx Vivado	2	6/7/2020	20/7/2020												
Analyze the cache unit developed by senior	2	20/7/2020	3/8/2020												
Decomposing the instruction cache unit	2	3/8/2020	17/8/2020												
Report writing	2	17/8/2020	2/9/2020												

Figure 3. 4. 1. 1: Gantt chart for Project I

3.4.2 Gantt Chart for Project II

Task Name	Duration	Start Date	End Date	week											
	(weeks)			1	2	3	4	5	6	7	8	9	10	11	12
Study RISC32 architecture	2	18/1/2021	1/2/2021												
Integration of pipelined cache	2	1/2/2021	15/2/2021												
RISC32 functionality test	2	15/2/2021	1/3/2021												
Synthesis and implement newly design RISC32	2	1/3/2021	15/3/2021												
Static timing analysis	2	15/3/2021	29/3/2021												
Report writing	2	29/3/2021	12/4/2021												

Figure 3. 4. 2. 1: Gantt chart for Project II

Chapter 4: System Specification

4.1 System Design / Overview

The 6-stage pipeline processor is made up Central Processing Unit (CPU), memory system (cache unit) and Input/output system which are the main parts of the processor. It evolved from 5-stage pipeline processor which is compatible to MIPS Instruction Set Architecture (ISA). Numerous instructions can be supported. For example, arithmetic, logical, program control and data memory access. For the memory system of the processor, it made up of instruction cache, data cache, stack RAM, boot ROM and flash memory. For the I/O system, it made up of UART controller, SPI controller, GPIO controller and priority interrupt controller. The usage of UART, SPI and GPIO controllers is for data transfer with sensors, personal computer, and wireless components. For the priority interrupt, it mainly uses is to deal with multiple interrupt that occur at the same time based on its priority level. It works together with coprocessor0 (cp0) to handle various type of exception. For example, undefined instruction exception, overflow exception, I/O interrupt and syscall exception. Figure 4.1.1 shows the overview of RISC32 pipeline processor architecture.

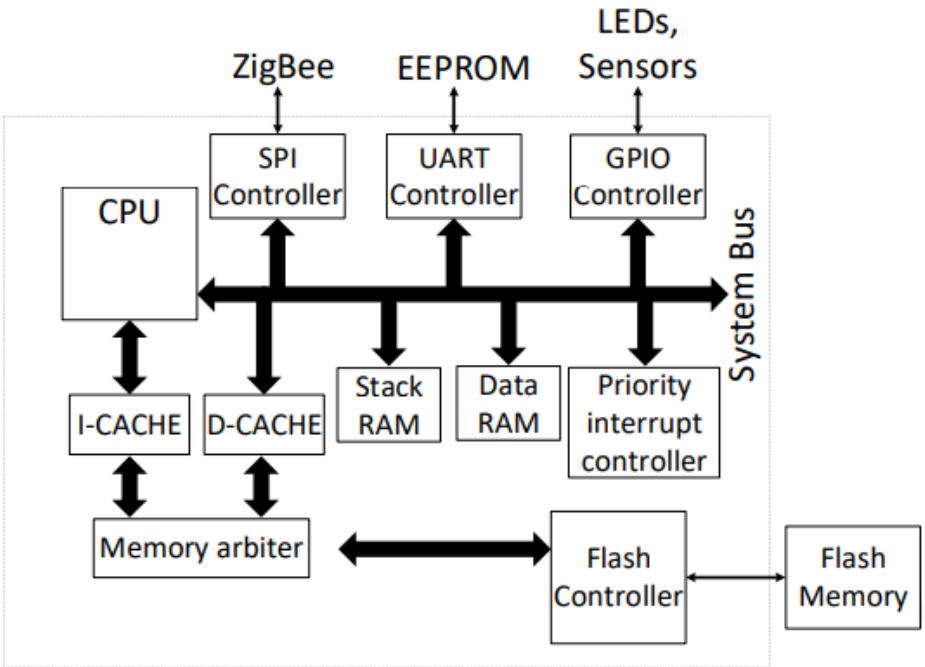

Figure 4. 1. 1: Overview of RISC32 pipeline processor architecture.

4.1.1 RISC32 6-Stage Pipeline Processor Hierarchy

Table 4.1.1.1 shows the RISC32 6-stage pipeline processor hierarchy. There are 4 main levels which is chip level, unit level, block level and sub-block.

Chip Level	Unit Level	Block Level	Sub-block
Processor (crisc)	Data-path unit (u_datapath)	Branch predictor (bbp_4way)	
		Register file (b_rf)	
		Forward control (b_fw)	
		Interlock control (b_itl)	
		Coprocessor0 (b_cp0)	
		ALB (b_alb)	
		Multiplier (b_mult)	adder_lvl1
			adder_lvl2
			adder_lvl3
			adder_lvl4
			adder_lvl5
			adder_lvl1_firstrow
			add_lvl1_lastrow
			adder_lvl2_lastrow
			sub_lvl1_lastrow
		Address decoder (baddr_decoder)	
	Control-path unit (uctrl_path)	ALB Control (balb_ctrl)	
		Main Control (bmain_ctrl)	
	Instruction Cache unit (upipelined_cache)	Cache Controller (bcache_ctrl_v3)	
		Cache RAM (bcache_ram)	
		FIFO Controller (bfifo_ctrl)	
		FIFO (bfifo)	
	Data cache unit (ucache)	Cache Controller (bcache_ctrl_v3)	
		Cache RAM (bcache_ram)	
		FIFO Controller	

	(bfifo_ctrl)	
	FIFO (bfifo)	
Flash Controller (ufc)	FIFO (bfc_FIFO)	
	Flash Controller Finite State Machine (FSM) (bfc_fsm)	
	Flash Controller Transmitter (bfcTX)	
	Flash Controller Clock Generator (bfc_clk_gen)	
	Flash Controller Receiver (bfcRX)	
Data RAM (uram)		
UART Controller (uuart_v2)	UART Transmitter (btx)	
	UART Baud Clock Generator (bclkctr)	
	UART Receiver (brx)	
SPI Controller unit	Receiver (bspiRX)	
	SPI Clock Generator (bspiclk_gen)	
	FIFO (bFIFO)	
	Transmitter block (bspiTX)	
	SPI I/O control (bspiIO_ctrl)	
ROM (uboot_rom)		
Programmable interrupt controller (upi_ctrl_v2)	Priority resolver (bpic_resolver)	
GPIO Controller (ugpio_v2)		
Memory Arbiter (umem_arbiter)		

Figure 4.1. 1. 1 : RISC32 processor design hierarchy

4.1.2 Micro-architecture of RISC32 5-Stage Pipeline Processor

Figure 4.1.2.1 shows the micro-architecture of RISC32 5-Stage pipeline processor.

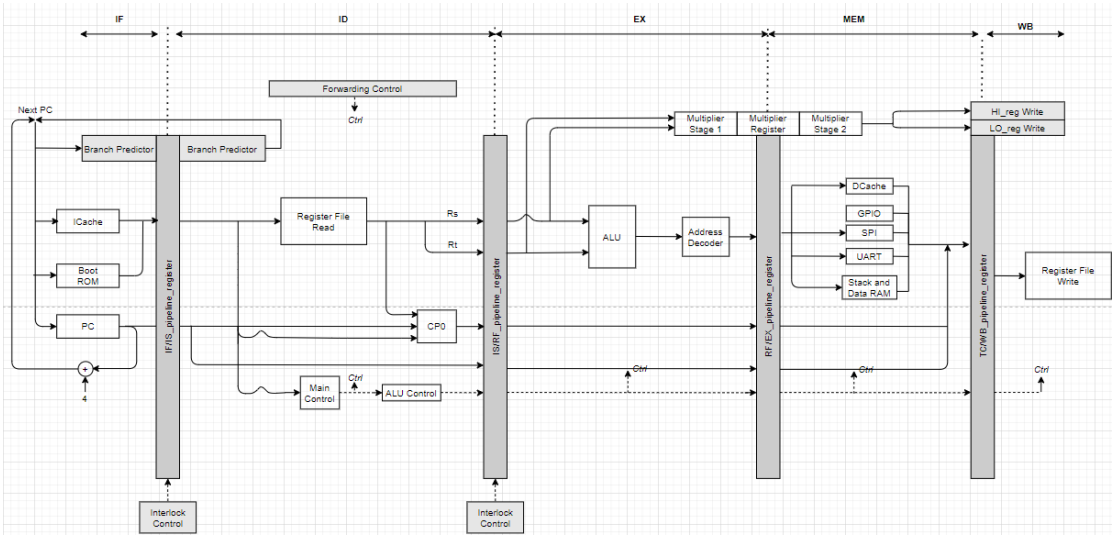

Figure 4. 1. 2. 1: Micro-architecture of RISC32 5-stage pipeline processor

4.1.3 Micro-architecture of RISC32 6-Stage Pipeline Processor

Figure 4.1.3.1 shows the micro-architecture of RISC32 6-Stage pipeline processor

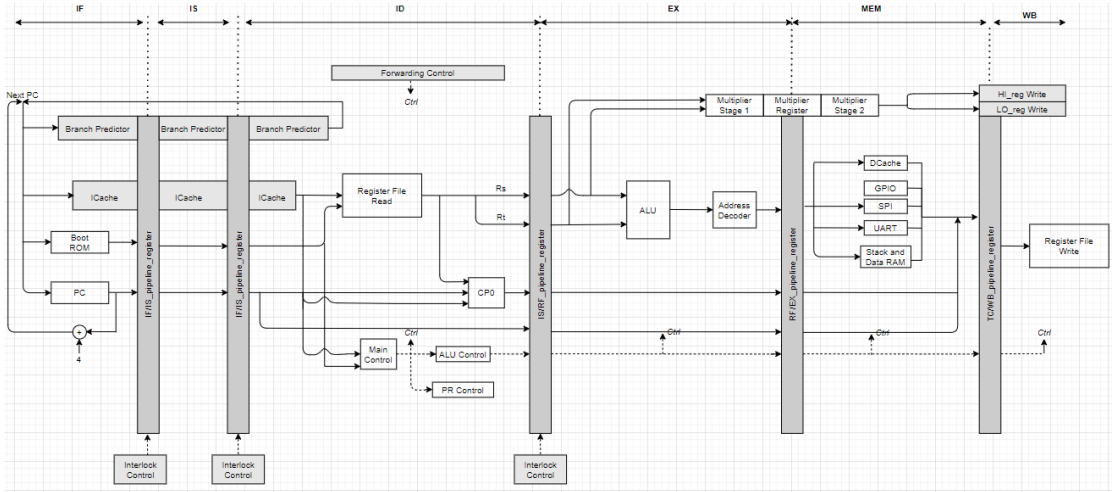

Figure 4. 1. 3. 1: Micro-architecture of RISC32 6-stage pipeline processor

4.1.4 Memory Map

MIPS memory space of RISC32 pipeline processor is implemented in two ways, which is physical and virtual addresses. The purpose of physical address is used to allocate physical memory such as data RAM, flash memory and boot ROM. The purpose of virtual address is used to access instruction program and data. Figure 4.1.4.1 shows the memory map of the RISC32 pipeline processor.

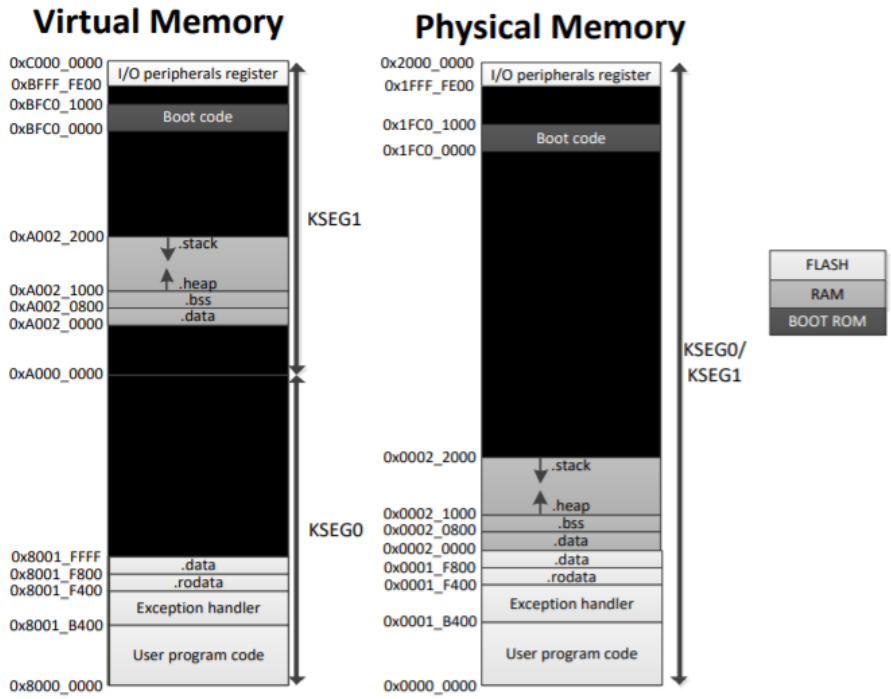

Figure 4. 1. 4. 1: Memory map of the RISC32 pipeline processor

*This figure is from THE DESIGN OF AN FPGA-BASED PROCESSOR WITH RECONFIGURABLE PROCESSOR EXECUTION STRUCTURE FOR INTERNET OF THINGS (IoT) APPLICATIONS, 2018 by Kiat Wei Pau

Table 4.1.3.1 shows the use of different memory allocation.

Memory Usage	Description	Memory Size
I/O peripheral register	Used as the memory-mapped registers for I/O peripheral controllers.	512 bytes
Boot code	Used to store bootloader program code for initial system configuration when powered on.	4k bytes
Stack	Used by procedure during execution to store register values.	8k bytes
Heap	Used to hold variables declared dynamically.	
Exception handler	Used to store the exception handler codes.	16k bytes
User program code	Used to store user program codes	128k bytes

Table 4. 1. 3. 1: RISC32 pipeline processor memory map description

4.2 Chip Interface of RISC32 Pipeline Processor

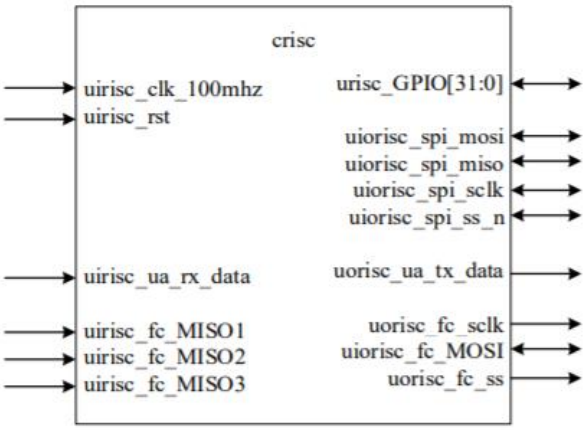

Figure 4. 2. 1: Chip Interface of RISC32 pipeline processor

4.2.1 Input Pin Description

Pin Name: uirisc_clk_100mhz **Pin Class**: Global **Pin Function**: Synchronize signals **Source->Destination**: External -> Crisc
Pin Name: uirisc_rst **Pin Class**: Global **Pin Function**: Reset pipeline processor **Source->Destination**: External -> Crisc
Pin Name: uirisc_ua_rx_data **Pin Class**: Data **Pin Function**: Receive serial data **Source->Destination**: External UART device -> Crisc
Pin Name: uirisc_fc_MISO1 **Pin Class**: Data **Pin Function**: SPI protocol serial pin **Source->Destination**: Flash memory -> Crisc
Pin Name: uirisc_fc_MISO2 **Pin Class**: Data **Pin Function**: SPI protocol serial pin **Source->Destination**: Flash memory -> Crisc
Pin Name: uirisc_fc_MISO3 **Pin Class**: Data **Pin Function**: SPI protocol serial pin **Source->Destination**: Flash memory -> Crisc

Table 4. 2. 1. 1: RISC32 input pin description

4.2.2 Output Pin Description

Pin Name: uorisc_ua_tx_data **Pin Class**: Data **Pin Function**: Transmit serial data **Source->Destination**: Crisc -> External UART unit
Pin Name: uorisc_fc_sclk **Pin Class**: Data **Pin Function**: SPI protocol serial clock signal **Source->Destination**: Crisc -> Flash memory
Pin Name: uorisc_fc_ss **Pin Class**: Control **Pin Function**: SPI protocol slave selects **Source->Destination**: Crisc -> Flash memory

Table 4. 2. 2. 1: RISC32 output pin description

4.2.3 Input Output Pin Description

Pin Name: urisc_GPIO **Pin Class**: Data **Pin Function**: GPIO pins **Source->Destination**: -> Crisc <-> External devices
Pin Name: uiorisc_spi_mosi **Pin Class**: Data **Pin Function**: This pin will become an input if crisc is configured as a master, else otherwise. **Source->Destination**: -> Crisc <-> External SPI unit
Pin Name: uiorisc_spi_miso **Pin Class**: Data **Pin Function**: This pin will become an input if crisc is configured as a master, else otherwise. **Source->Destination**: -> Crisc <-> External SPI unit
Pin Name: uiorisc_spi_sclk **Pin Class**: Control **Pin Function**: This pin will become an output if crisc is configured as a master, else otherwise. **Source->Destination**: -> Crisc <-> External SPI unit
Pin Name: uiorisc_spi_ss_n **Pin Class**: Control **Pin Function**: This pin will become an output if crisc is configured as a master, else otherwise. **Source->Destination**: -> Crisc <-> External SPI unit
Pin Name: uiorisc_fc_MOSI **Pin Class**: Data **Pin Function**: SPI protocol serial input output pin **Source->Destination**: -> Crisc <-> Flash Memory

Table 4. 2. 3. 1: RISC32 input output pin description

Chapter 5: Micro-Architecture Specification

5.1 Pipelined I-Cache

5.1.1 Functionality of I-Cache

Figure 5.1.1.1 shows the block diagram of i-cache. The functionalities of i-cache are:

- Store instructions of main memory.
- Output instructions to CPU.
- Stall the CPU when read miss.
- Communicate with flash memory controller to fetch new block of instructions when read miss.

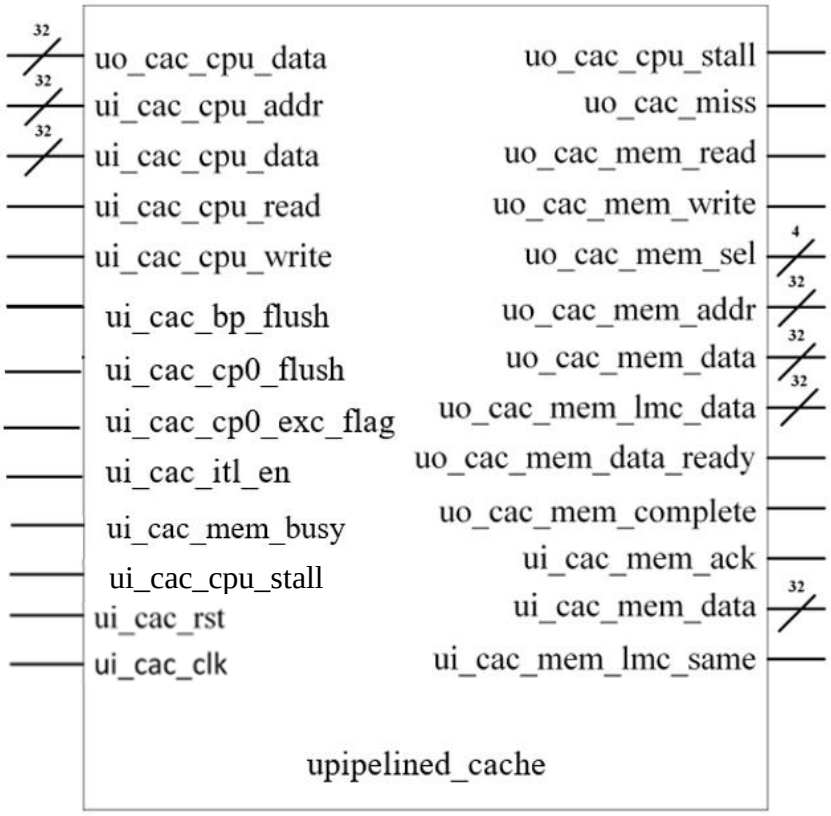

Figure 5. 1. 1. 1: Block diagram of I-cache

5.1.2 Input Pin Description

Pin Name: ui_cac_clk **Pin Class**: Global **Pin Function**: Synchronize signals **Source->Destination**: External -> Cache
Pin Name: ui_cac_rst **Pin Class**: Global **Pin Function**: Reset cache **Source->Destination**: External -> Cache
Pin Name: ui_cac_cpu_data **Pin Class**: Data **Pin Function**: Data from CPU that required to write into cache **Source->Destination**: CPU -> Cache
Pin Name: ui_cac_cpu_addr **Pin Class**: Address **Pin Function**: Address to be accessed in cache **Source->Destination**: CPU -> Cache
Pin Name: ui_cac_cpu_read **Pin Class**: Control **Pin Function**: Enable read from cache **Source->Destination**: CPU -> Cache
Pin Name: ui_cac_cpu_write **Pin Class**: Control **Pin Function**: Enable write of data into cache **Source->Destination**: CPU -> Cache
Pin Name: ui_cac_mem_ack **Pin Class**: Control **Pin Function**: HIGH: Read data is ready from flash memory LOW: Flash memory is prepared to receive data **Source->Destination**: Memory arbiter -> Cache
Pin Name: ui_cac_mem_data **Pin Class**: Data **Pin Function**: Data read from flash memory **Source->Destination**: Memory arbiter -> Cache
Pin Name: ui_cac_mem_lmc_same **Pin Class**: Status **Pin Function**: HIGH: Configuration of flash memory is same **Source->Destination**: Memory arbiter -> Cache
Pin Name: ui_cac_bp_flush **Pin Class**: Control **Pin Function**: Flush the pipeline inside cache when wrong prediction **Source->Destination**: Datapath unit -> Cache

Pin Name: ui_cac_cp0_flush **Pin Class**: Control **Pin Function**: Flush the pipeline inside cache when exception occur **Source->Destination**: Datapath unit -> Cache
Pin Name: ui_cac_cp0_exc_flag **Pin Class**: Control **Pin Function**: Stall the pipeline inside cache when exception occur **Source->Destination**: Datapath unit -> Cache
Pin Name: ui_cac_itl_en **Pin Class**: Control **Pin Function**: Stall the pipeline inside cache when data hazard occurs **Source->Destination**: Datapath unit -> Cache
Pin Name: ui_cac_mem_busy **Pin Class**: Control **Pin Function**: HIGH: Indicate flash memory is busy LOW: Indicate flash memory is ready to use **Source->Destination**: Flash controller unit -> Cache
Pin Name: ui_cac_cpu_stall **Pin Class**: Control **Pin Function**: HIGH: Stall the pipeline inside the cache **Source->Destination**: Datapath unit -> Cache

Table 5. 1. 2. 1: Cache input pin description

5.1.3 Output Pin Description

Pin Name: uo_cac_cpu_data **Pin Class**: Data **Pin Function**: Instruction output to CPU **Source->Destination**: Cache -> CPU
Pin Name: uo_cac_cpu_stall **Pin Class**: Control **Pin Function**: Stall all the pipelines inside the processor **Source->Destination**: Cache -> CPU
Pin Name: uo_cac_miss **Pin Class**: Status **Pin Function**: Indicate cache miss **Source->Destination**: Cache -> Memory arbiter

Pin Name: uo_cac_mem_write **Pin Class**: Control **Pin Function**: Indicate the need of write data into flash memory **Source->Destination**: Cache -> Memory arbiter
Pin Name: uo_cac_mem_read **Pin Class**: Control **Pin Function**: Indicate the need of read data from flash memory **Source->Destination**: Cache -> Memory arbiter
Pin Name: uo_cac_mem_sel **Pin Class**: Control **Pin Function**: Mask 32 bits data **Source->Destination**: Cache -> Memory arbiter
Pin Name: uo_cac_mem_addr **Pin Class**: Address **Pin Function**: Indicate the location in the flash memory to be accessed **Source->Destination**: Cache -> Memory arbiter
Pin Name: uo_cac_mem_data **Pin Class**: Data **Pin Function**: Data to be written into flash memory **Source->Destination**: Cache -> Memory arbiter
Pin Name: uo_cac_mem_lmc_data **Pin Class**: Data **Pin Function**: Configure flash memory **Source->Destination**: Cache -> Memory arbiter
Pin Name: uo_cac_mem_data_ready **Pin Class**: Status **Pin Function**: HIGH: Data is ready to write back from FIFO to flash memory **Source->Destination**: Cache -> Memory arbiter
Pin Name: uo_cac_mem_complete **Pin Class**: Status **Pin Function**: HIGH: Indicate one block of data is written into flash memory **Source->Destination**: Cache -> Memory arbiter

Table 5. 1. 3. 1: Cache output pin description

5.1.4 Micro-architecture of I-cache

Figure 5.1.4.1 shows the original I-cache in RISC32 5-stage pipeline processor. The 2 red lines indicate new pipeline stages will be placed in new design of I-cache. Cache control, FIFO, and FIFO control will be only activated when cache miss.

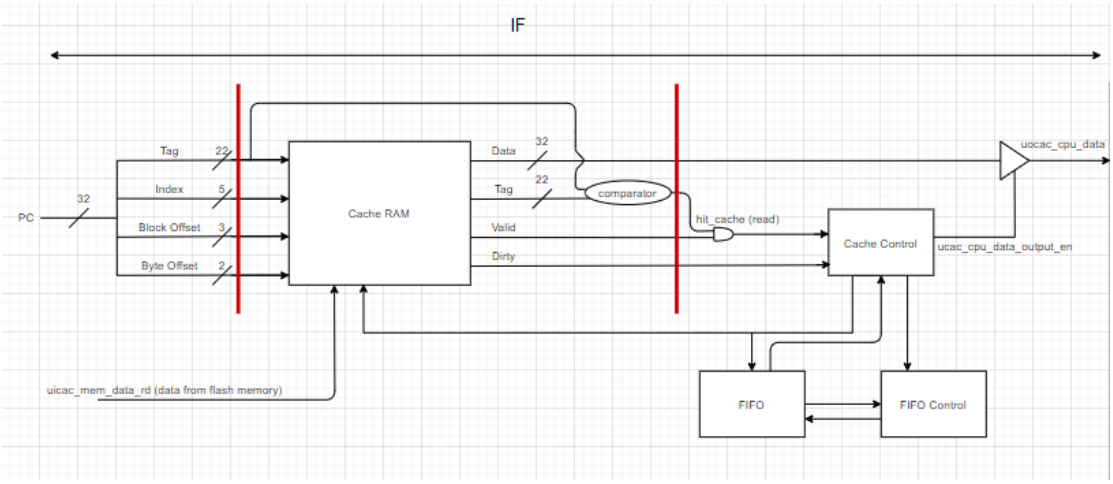

Figure 5. 1. 4. 1: Micro-architecture of I-cache.

5.1.5 Micro-architecture of Pipelined I-cache

Figure 5.1.5.1 shows the micro-architecture of pipelined I-cache. Cache control, FIFO, and FIFO control will be only activated when cache miss and asynchronous to the program execution flow. I-cache access is divided into 3 stages which are:

- IF: Initiation of cache access
- IS: Cache RAM access
- ID: Instruction cache hit detection

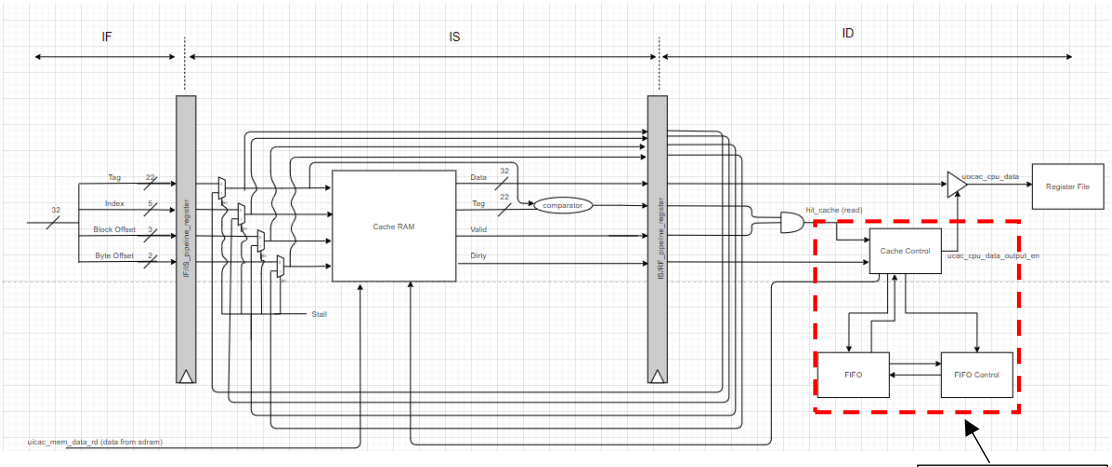

Figure 5. 1. 5. 1: Micro-architecture of pipelined I-cache

Asynchronous to the program execution flow

5.1.6 Read Protocol

Figure 5.1.6.1 shows the read protocol for I-cache.

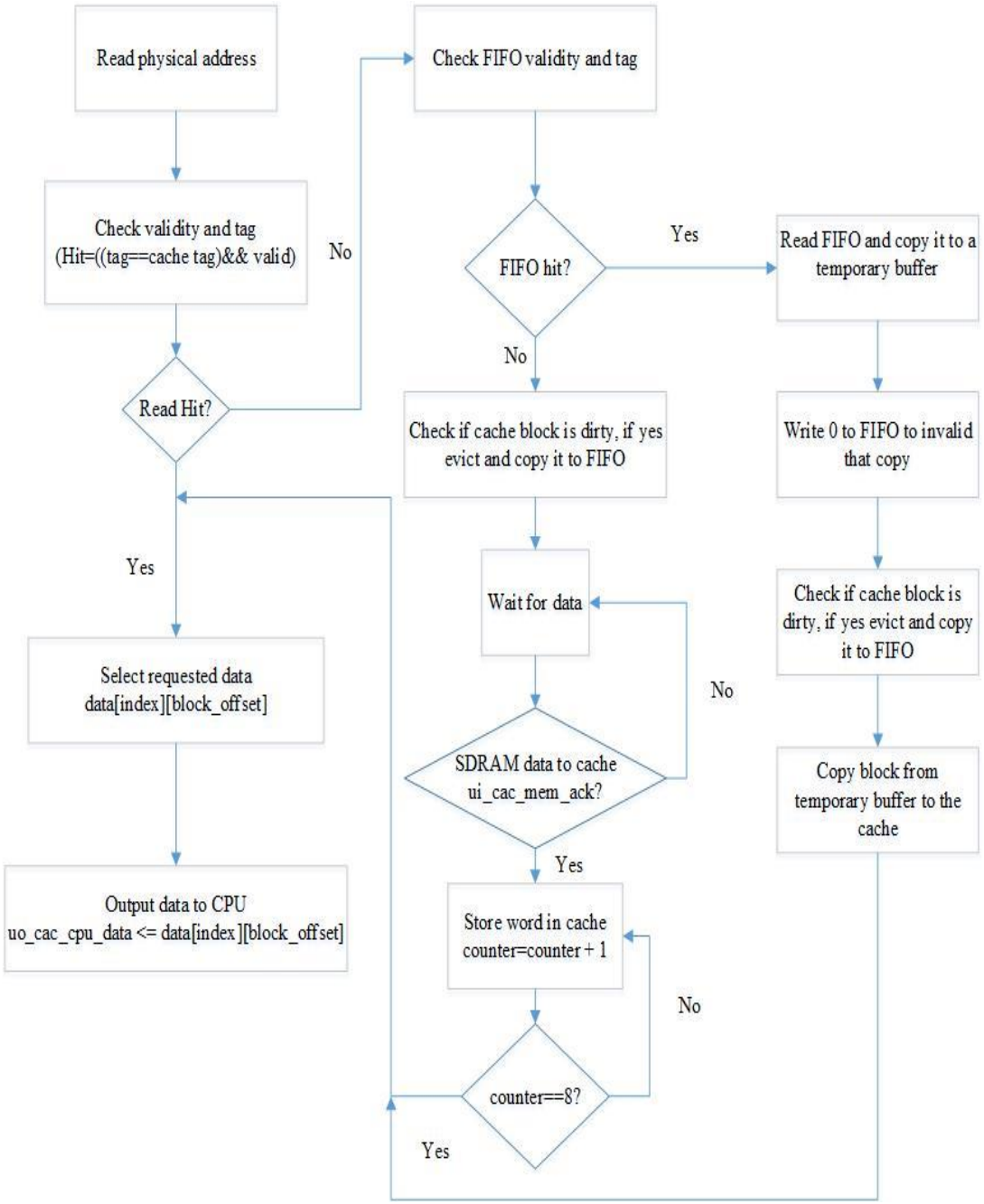

Figure 5. 1. 6. 1: I-cache read protocol

5.2 Branch Predictor

5.2.1 Functionality of Branch Predictor

Figure 5.2.1.1 shows the block diagram of branch predictor. The functionalities of branch predictor are:

- Predict next PC for the CPU based on the information in branch target buffer.
- Check predicted PC and update the branch target buffer.
- Flush the IS and ID stage of CPU if the prediction is incorrect and provide correction PC.

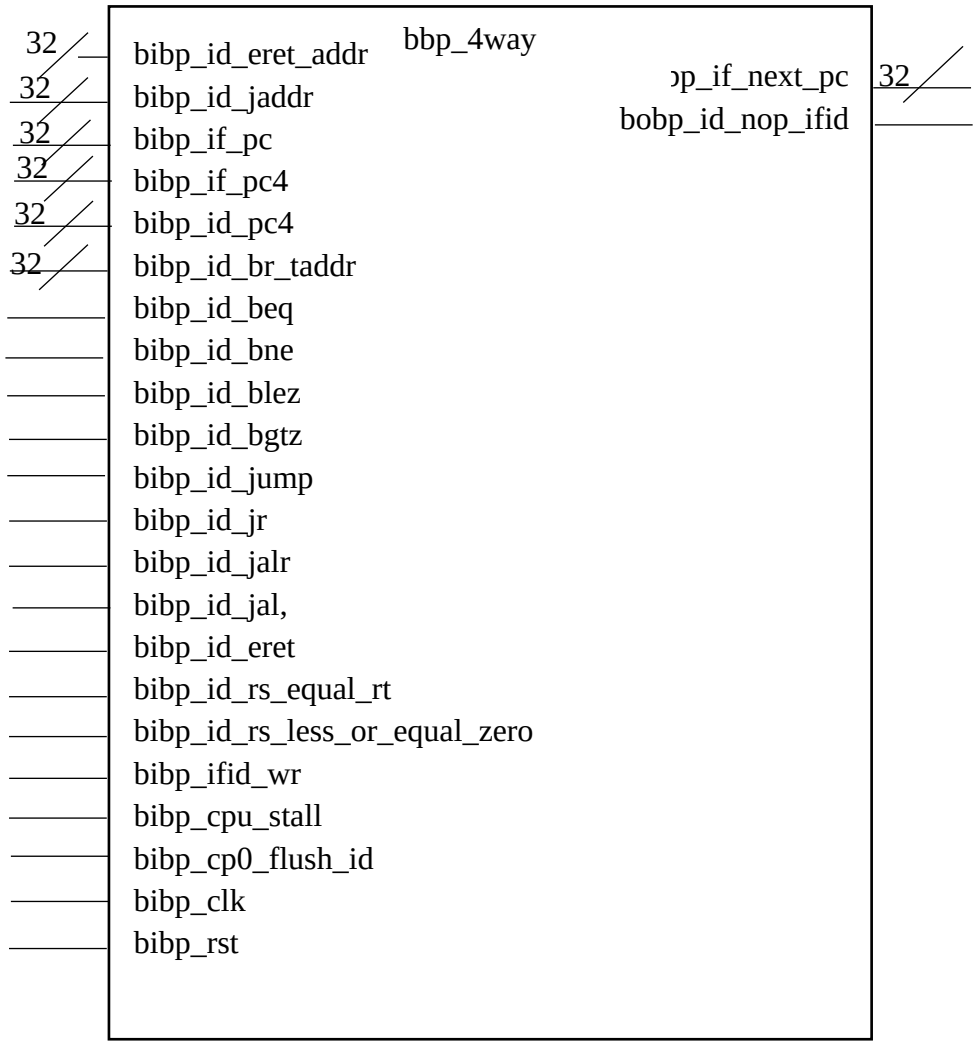

Figure 5. 2. 1. 1: Block diagram of branch predictor

5.2.2 Input Pin Description

Pin Name: bibp_id_eret_addr [31:0] **Pin Class**: Address **Pin Function**: Exception PC **Source->Destination**: Datapath unit -> Branch predictor
Pin Name: bibp_id_jaddr [31:0] **Pin Class**: Address **Pin Function**: Jump PC **Source->Destination**: Datapath unit -> Branch predictor
Pin Name: bibp_if_pc [31:0] **Pin Class**: Address **Pin Function**: Access branch target buffer to predict next PC **Source->Destination**: Datapath unit -> Branch predictor
Pin Name: bibp_if_pc4 [31:0] **Pin Class**: Address **Pin Function**: Prediction PC for predict untaken **Source->Destination**: Datapath unit -> Branch predictor
Pin Name: bibp_id_pc4 [31:0] **Pin Class**: Address **Pin Function**: Correction PC for miss predict taken **Source->Destination**: Datapath unit -> Branch predictor
Pin Name: bibp_id_br_taddr [31:0] **Pin Class**: Address **Pin Function**: Correction PC for miss predict untaken **Source->Destination**: Datapath unit -> Branch predictor
Pin Name: bibp_id_beq **Pin Class**: Status **Pin Function**: HIGH: Indicate instruction is beq in ID stage **Source->Destination**: Datapath unit -> Branch predictor
Pin Name: bibp_id_bne **Pin Class**: Status **Pin Function**: HIGH: Indicate instruction is bne in ID stage **Source->Destination**: Datapath unit -> Branch predictor
Pin Name: bibp_id_blez **Pin Class**: Status **Pin Function**: HIGH: Indicate instruction is blez in ID stage **Source->Destination**: Datapath unit -> Branch predictor
Pin Name: bibp_id_bgtz **Pin Class**: Status **Pin Function**: HIGH: Indicate instruction is bgtz in ID stage **Source->Destination**: Datapath unit -> Branch predictor

Pin Name: bibp_id_jump **Pin Class**: Status **Pin Function**: HIGH: Indicate instruction is jump in ID stage **Source->Destination**: Datapath unit -> Branch predictor
Pin Name: bibp_id_jr **Pin Class**: Status **Pin Function**: HIGH: Indicate instruction is jr in ID stage **Source->Destination**: Datapath unit -> Branch predictor
Pin Name: bibp_id_jalr **Pin Class**: Status **Pin Function**: HIGH: Indicate instruction is jalr in ID stage **Source->Destination**: Datapath unit -> Branch predictor
Pin Name: bibp_id_jal **Pin Class**: Status **Pin Function**: HIGH: Indicate instruction is jal in ID stage **Source->Destination**: Datapath unit -> Branch predictor
Pin Name: bibp_id_eret **Pin Class**: Status **Pin Function**: HIGH: Indicate exception occur in ID stage **Source->Destination**: Datapath unit -> Branch predictor
Pin Name: bibp_id_rs_equal_rt **Pin Class**: Status **Pin Function**: Indicate the correctness of previous prediction for bne and beq **Source->Destination**: Datapath unit -> Branch predictor
Pin Name: bibp_id_rs_less_or_equal_zero **Pin Class**: Status **Pin Function**: Indicate the correctness of previous prediction for bgtz and blez **Source->Destination**: Datapath unit -> Branch predictor
Pin Name: bibp_ifid_wr **Pin Class**: Control **Pin Function**: LOW: Stall IF/IS and IS/ID pipeline **Source->Destination**: Datapath unit -> Branch predictor
Pin Name: bibp_cpu_stall **Pin Class**: Control **Pin Function**: HIGH: Stall IF/IS and IS/ID which caused by cache miss **Source->Destination**: Datapath unit -> Branch predictor
Pin Name: bibp_cp0_flush_id **Pin Class**: Control **Pin Function**: Flush the pipelines register when exception occur **Source->Destination**: Datapath unit -> Branch predictor

Pin Name: bibp_clk **Pin Class**: Global **Pin Function**: Synchronize signals **Source->Destination**: Datapath unit -> Branch predictor
Pin Name: bibp_rst **Pin Class**: Global **Pin Function**: Reset branch predictor **Source->Destination**: Datapath unit -> Branch predictor

Table 5. 2. 2. 1: Branch predictor input pin description

5.2.3 Output Pin Description

Pin Name: bobp_if_next_pc **Pin Class**: Address **Pin Function**: Predicted next PC **Source->Destination**: Branch predictor ->
Pin Name: bobp_id_nop_ifid **Pin Class**: Control **Pin Function**: **Source->Destination**: Branch predictor ->

Table 5. 2. 3. 1: Branch predictor output pin description

5.2.4 Micro-architecture of Branch Predictor

Figure 5.2.4.1 shows the micro-architecture of branch predictor designed by Chang Boon Chiao. The red line indicates an additional pipeline register is newly added. Since MIPS architecture has a cycle single branch delay, therefore prediction can be made in clock cycle 2 and take this advantage to split the logic of the branch predictor more evenly. Instruction only available in clock cycle 3. Thus, checking correctness of the prediction should also in clock cycle 3.

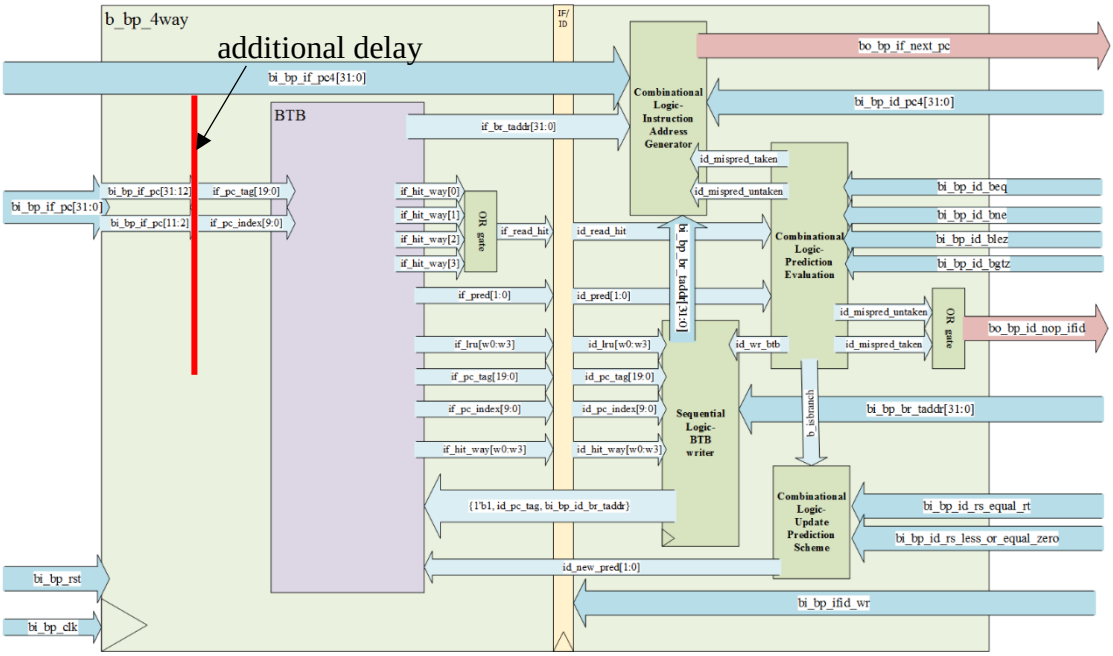

Figure 5. 2. 4. 1: Micro-architecture of branch predictor.

5.2.5 Internal Operation

Stage 1: IF

- PC selection and initiation of branch predictor access

Stage 2: IS

- Read branch target buffer (BTB) based on the PC to predict next PC by looking for entry with the same index and tag as the PC in the BTB.
- Branch target address will be assigned as next PC if the entry is found in the BTB
- Normal PC (PC+4) will be assigned as next PC if the entry is not found in the BTB

Stage 3: ID

- Check the correctness of the prediction.
- IS and ID stage will be flushed if the prediction is incorrect.
- When there is no matching entry is found in the previous IF stage, a new entry will be created to store the information of the instruction.
- When there is matching entry is found in the previous IF stage, information in the entry will be updated.

5.2.6 State Transition of BTB

Figure 5.2.6.1 shows the FSM of BTB.

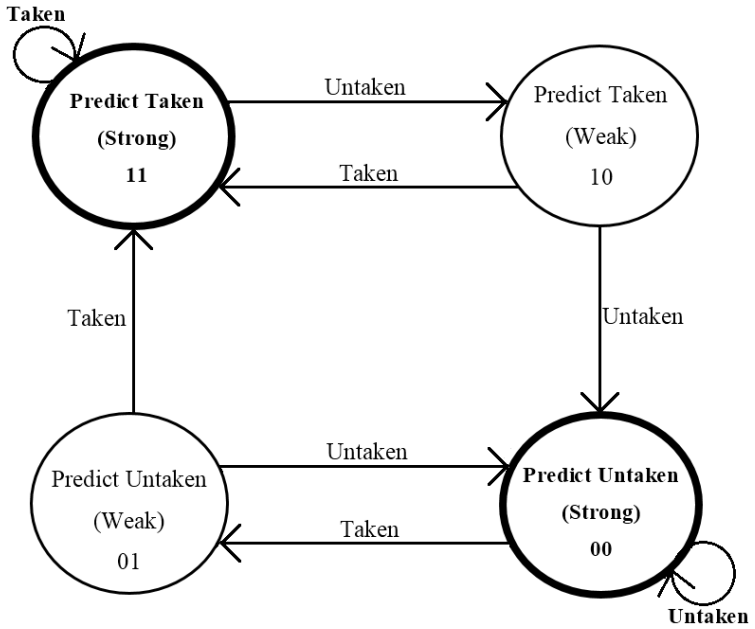

Figure 5. 2. 6. 1: FSM of BTB

5.3 Cache Controller

5.3.1 Functionality of Cache Controller

Figure 5.3.1.1 shows the block diagram of cache controller designed by Goh Dih Jian.

The functionalities of cache controller are:

- Control the activity of pipelined I-cache
- Determine the data to read from flash memory when cache miss
- Output status and control signal to write back data from FIFO to cache
- Output status and control signal to move dirty data from cache to FIFO
- Output status and control signal to flash memory

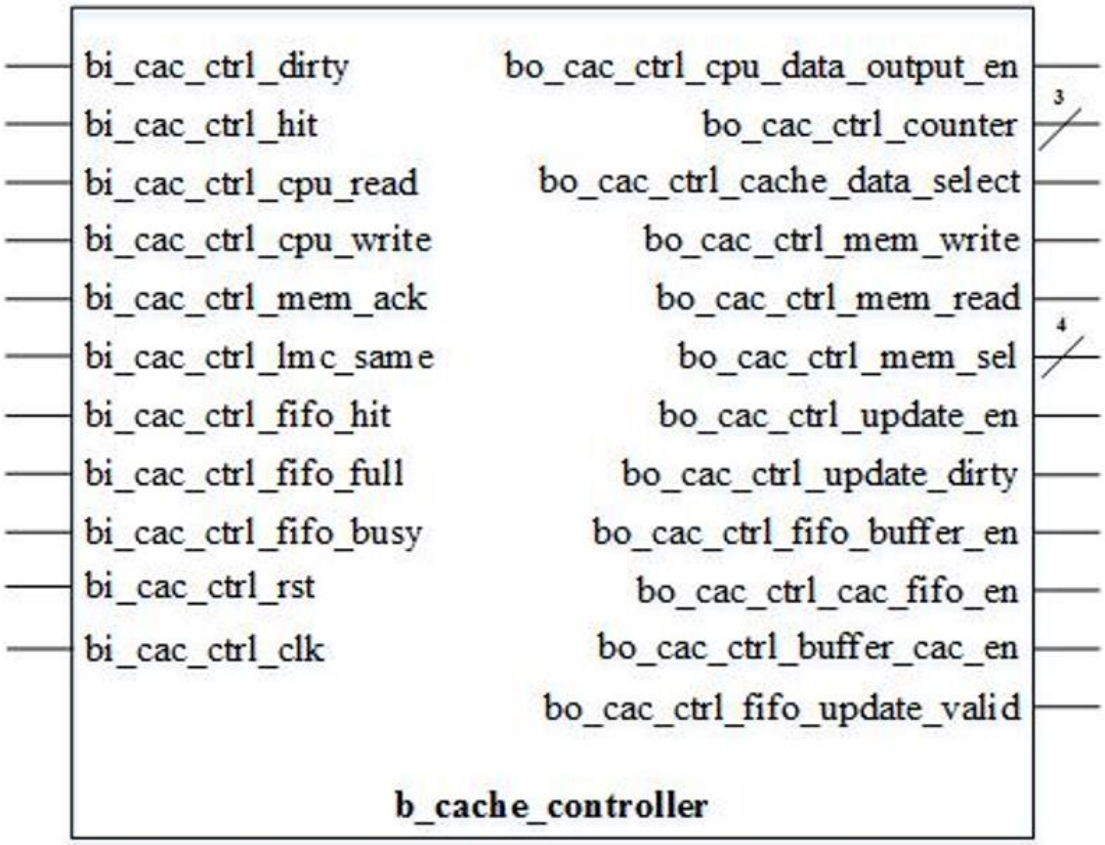

Figure 5. 3. 1. 1: Block diagram of cache controller

5.3.2 Input Pin Description

Pin Name: bi_cac_ctrl_clk **Pin Class**: Global **Pin Function**: Synchronize signals **Source->Destination**: External -> Cache unit -> Cache controller
Pin Name: bi_cac_ctrl_rst **Pin Class**: Global **Pin Function**: Reset cache controller **Source->Destination**: External -> Cache unit -> Cache controller
Pin Name: bi_cac_ctrl_lmc_same **Pin Class**: Status **Pin Function**: HIGH: Indicate the configuration of flash memory is same **Source->Destination**: Memory arbiter -> Cache unit -> Cache controller
Pin Name: bi_cac_ctrl_mem_ack **Pin Class**: Control **Pin Function**: HIGH: Indicate data is ready from flash memory LOW: Indicate flash memory is prepared to receive data **Source->Destination**: Flash memory controller -> Memory arbiter -> Cache unit ->Cache controller
Pin Name: bi_cac_ctrl_cpu_write **Pin Class**: Control **Pin Function**: HIGH: Enable data to be written into cache **Source->Destination**: CPU -> Cache unit -> Cache controller
Pin Name: bi_cac_ctrl_cpu_read **Pin Class**: Control **Pin Function**: HIGH: Enable data to be read from cache **Source->Destination**: CPU -> Cache unit -> Cache controller
Pin Name: bi_cac_ctrl_hit **Pin Class**: Status **Pin Function**: HIGH: Indicate cache hit **Source->Destination**: Cache unit -> Cache controller
Pin Name: bi_cac_ctrl_dirty **Pin Class**: Status **Pin Function**: HIGH: Indicate the data to be accessed is dirty **Source->Destination**: Cache unit -> Cache controller
Pin Name: bi_cac_ctrl_fifo_busy **Pin Class**: Status **Pin Function**: HIGH: Indicate FIFO is writing into flash memory **Source->Destination**: FIFO -> Cache controller
Pin Name: bi_cac_ctrl_fifo_full **Pin Class**: Status **Pin Function**: HIGH: Indicate FIFO is full **Source->Destination**: FIFO -> Cache controller

Pin Name: bi_cac_ctrl_fifo_hit **Pin Class**: Status **Pin Function**: HIGH: Indicate latest copy of data is in FIFO **Source->Destination**: FIFO -> Cache controller

Table 5. 3. 2. 1: Input pin description of cache controller

5.3.3 Output Pin Description

Pin Name: bo_cac_ctrl_cpu_data_output_en **Pin Class**: Control **Pin Function**: HIGH: Indicate data is enabled to be output to CPU **Source->Destination**: Cache controller -> Cache unit
Pin Name: bo_cac_ctrl_counter[2:0] **Pin Class**: Control **Pin Function**: Count the data when transferring a block of data (8 words). **Source->Destination**: Cache controller -> Cache
Pin Name: bo_cac_ctrl_cache_data_select **Pin Class**: Control **Pin Function**: HIGH: Choose data from flash memory LOW: Choose data from CPU **Source->Destination**: Cache -> Cache controller -> Cache
Pin Name: bo_cac_ctrl_mem_read **Pin Class**: Control **Pin Function**: HIGH: Indicate there is a need of read from flash memory **Source->Destination**: Cache controller -> Cache
Pin Name: bo_cac_ctrl_mem_write **Pin Class**: Control **Pin Function**: HIGH: Indicate there is a need of write into flash memory **Source->Destination**: Cache controller -> FIFO controller
Pin Name: bo_cac_ctrl_mem_sel [3:0] **Pin Class**: Control **Pin Function**: Mask the data enter or leave flash memory **Source->Destination**: Cache controller -> Cache
Pin Name: bo_cac_ctrl_update_en **Pin Class**: Control **Pin Function**: HIGH: Enable update of cache **Source->Destination**: Cache controller -> Cache
Pin Name: bo_cac_ctrl_update_dirty **Pin Class**: Control **Pin Function**: HIGH: Enable update of ‘Dirty’ in cache **Source->Destination**: Cache controller -> Cache

Pin Name: bo_cac_ctrl_fifo_buffer_en **Pin Class**: Control **Pin Function**: HIGH: Enable to move write back data from FIFO to temporary buffer **Source->Destination**: Cache controller -> Cache
Pin Name: bo_cac_ctrl_cac_fifo_en **Pin Class**: Control **Pin Function**: HIGH: Enable to move data to FIFO **Source->Destination**: Cache controller -> Cache
Pin Name: bo_cac_ctrl_buffer_cac_en **Pin Class**: Control **Pin Function**: HIGH: Enable to move write back data from temporary buffer to cache **Source->Destination**: Cache controller -> Cache
Pin Name: bo_cac_ctrl_fifo_update_valid **Pin Class**: Control **Pin Function**: HIGH: Indicate update of valid bit in FIFO **Source->Destination**: Cache controller -> FIFO

Table 5. 3. 3. 1: Output pin description of cache controller

5.3.4 Cache Controller State Diagram for Read Instruction

Figure 5.3.4.1 shows the cache controller state diagram for read instruction. New state "WAIT" is added since the cache hit detection is delay by 1 clock cycle.

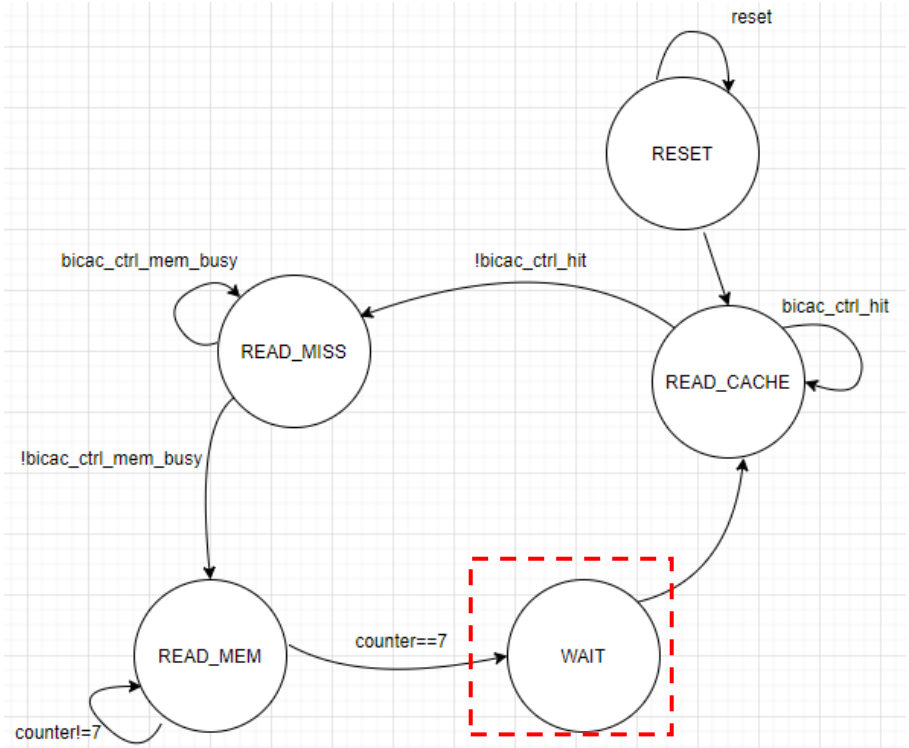

Figure 5. 3. 4. 1: Cache controller state diagram for read instruction

Chapter 6: Verification

6.1 Pipelined I-cache and Cache Controller

6.1.1 Test Plan

Test	Expected output	Status
Test case 1: Reset	uocac_cpu_data = 32'h0 ucac_hit = 1'b1 uocac_miss = 1'b0 uocac_cpu_stall = 1'b0 bcac_ctrl_status = "RESET"	Pass
Test case 2: Cache read miss **Input**: uicac_cpu_addr: 32'h8000_0000	uocac_cpu_data = 32'h0 ucac_hit = 1'b0 uocac_miss = 1'b1 uocac_cpu_stall = 1'b1 bcac_ctrl_status = "READ_CACHE"-> "READ_MISS"	Pass
Test case 3: Cache read hit after miss **Input**: uicac_cpu_addr: 32'h8000_0000	uocac_cpu_data = 32'h0c00_000a (jal) ucac_hit = 1'b1 uocac_miss = 1'b0 uocac_cpu_stall = 1'b0	Pass

6.1.2 Simulation Result

Figure 6.1.2.1 shows the simulation result for test case 1: Reset.

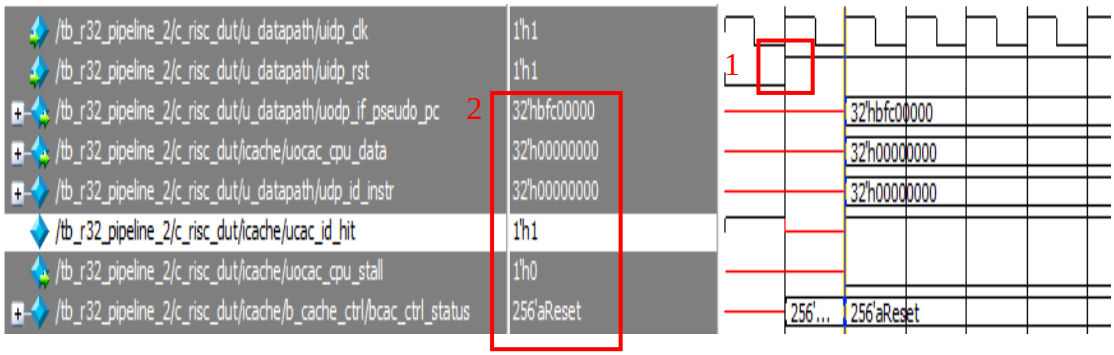

Figure 6. 1. 2. 1: Simulation result for test case 1

1. Reset signal is asserted.
2. All register and output signals are initialized to default value.

Figure 6.1.2.2 shows the simulation result for test case 2: Cache Read Miss

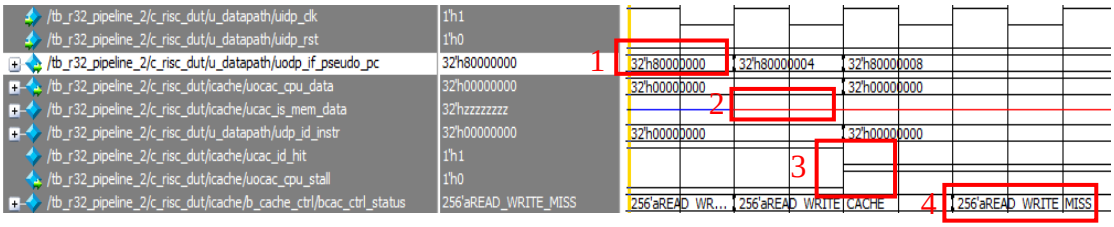

Figure 6. 1. 2. 2: Simulation result for test case 2

1. uicac_cpu_addr enter the first stage of the pipelined i-cache.
2. Clock cycle 2, cache RAM access.
3. Clock cycle 3, cache hit detection. Since there is cache miss, uocac_cpu_stall is asserted to stall the whole processor.
4. The status of cache controller will change to “READ_MISS”.

Figure 6.1.2.3 shows the simulation result for test case 3: Cache Read Hit After Hit

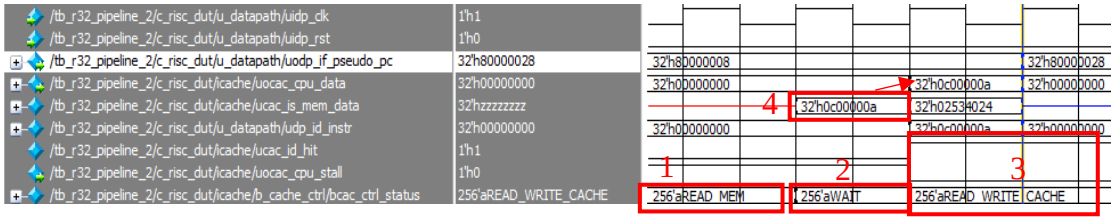

Figure 6. 1. 2. 3: Simulation result for test case 3

1. After cache miss, the cache controller will be activated and fetch a block of instruction from flash memory to the cache RAM.
2. After done fetching the instruction, the cache control will change to “WAIT” state to delay 1 clock cycle as cache hit detection is in next clock cycle.
3. Cache hit in next clock cycle. Processor is resumed.
4. Output the instruction to the CPU.

6.2 Branch Predictor

6.2.1 Test Plan

The following test program is a simple loop program to test the branch predictor.

Instruction address	Instruction code	Label	Mnemonic	Operand 1	Operand 2	Operand 3
0x80000000	34060005		ori	$a2,	$zero,	5
0x80000004	20c6ffff	DELAY	addi	$a2,	$a2,	-1
0x80000008	1cc0fffe		bgtz	$a2,	DELAY	
0x8000000c	00000000		nop			
0x80000010	3109000f		addi	$t1,	$t0,	15
0x80000014	00000000		Nop			
0x80000018	00000000		Nop			

6.2.2 Simulation Result

Figure 6.2.2.1 shows the simulation result for conditional branch instruction (bgtz).

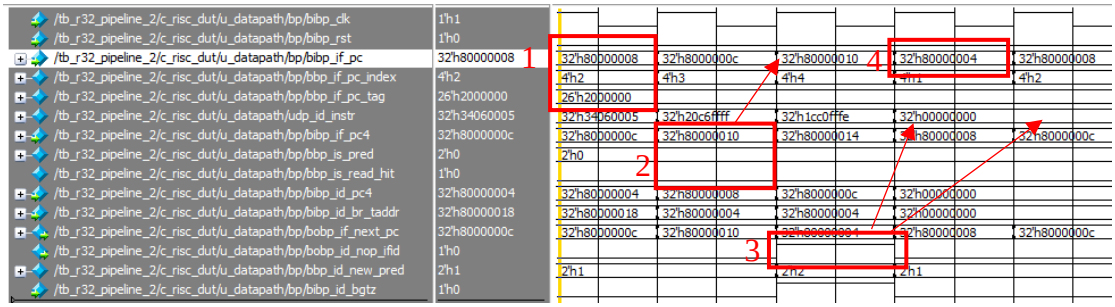

Figure 6. 2. 2. 1: Simulation result for conditional branch instruction (bgtz).

1. Initiation of branch predictor access.
2. BTB is read based on the PC. Since the state of the entry is 2'h0, which is predict untaken (strong), so prediction will be not taken. Normal PC (PC+4) is assigned to the next PC.
3. In clock cycle 3, branch predictor evaluates the correctness of the prediction. Since the prediction is incorrect, IS and ID stage will be flushed and update the information of the entry.
4. Correction of PC is assigned to next clock cycle.

Figure 6.2.2.2 shows the simulation result after next PC is corrected.

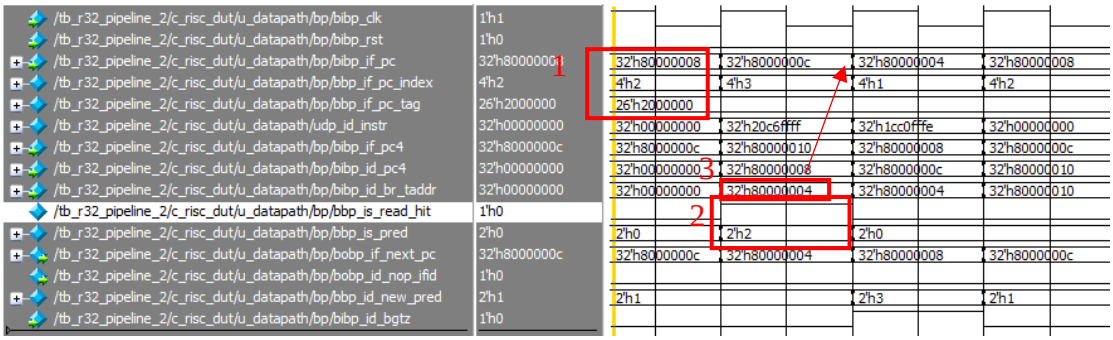

Figure 6. 2. 2. 2: Simulation result after next PC is corrected

1. After the correction of PC, same PC enter the branch predictor again and initiation of branch predictor access happen.
2. Since the entry information is updated last time and the state of entry is updated to 2'h2 which is predict taken (strong), so the prediction will be taken.
3. Next PC which is stored in BTB will be assigned as next PC.

Chapter 7: Synthesis and Implementation

When the behavioral simulation of the 6-stage pipeline processor is successful in the Modelsim, then it is ready for synthesis and implementation by using Xilinx Vivado. The FPGA board used for synthesis and implementation is Arty A7-100 and the default part is xc7a100tcsg324-1.

7.1 Project Settings

7.1.1 Synthesis Setting

Figure 7.1.1.1 shows the synthesis setting. -flatten_hierarchy is set to “none” so the output of synthesis will have the exact same hierarchy as the original RTL.

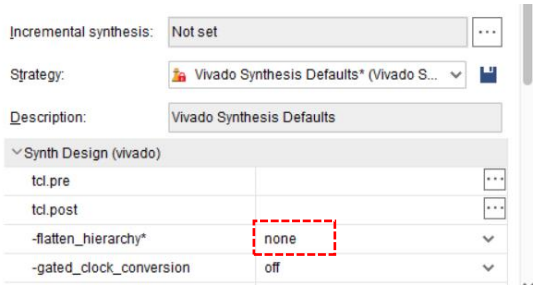

Figure 7. 1. 1. 1: Setting for synthesis

7.1.2 Implementation Setting

Figure 7.1.2.1 shows the implementation setting. Opt Design (opt_design) is disabled to not optimize the logical design.

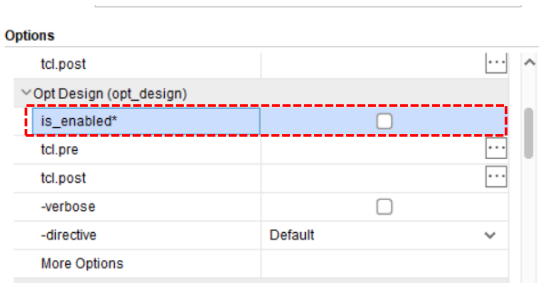

Figure 7. 1. 2. 1: Setting for implementation

7.2 Timing Analysis

After the process of synthesis and implementation is done, a tcl script file which developed by senior is run on the tcl console to get the timing delay of each stage. In the tcl console, type command "source <location of the script file>" to get the timing delay file. The source code can be found in Appendix C. Since there are 2 components (branch predictor and pipelined I-cache) have pipeline stages which does not in datapath unit, so timing delay of these components must be analyze separately. Table 7.1.1 shows the timing delay of the 6-stage pipeline processor. The details of each stage of timing delay can be found in Appendix B.

Pipeline Stage	IF	IS	ID	EX	MEM	WB
Timing delay	7.289 ns	13.245 ns	16.462 ns	13.712 ns	16.844 ns	3.688 ns

Table 7. 2. 1: Timing delay of 6-stage pipeline processor

7.2 Performance Analysis

By using the longest timing delay of the pipeline stage, the maximum clock rate of the CPU is:

$$\text{Clock rate of 6-stage pipeline processor} = \frac{1}{16.844\ \text{ns}}$$

$$= 59.368\ \text{MHz}$$

The clock rate of the 6-stage pipeline processor faster than 5-stage pipeline processor which is 56.338 MHz. The performance of the CPU is improved by 5.38%.

$$\text{Performance improved} = \frac{59.368 - 56.338}{56.338} \times 100\%$$

$$= 5.38\%$$

Chapter 8: Conclusion and Future Work

8.1 Conclusion

The objective of this project which is increased the clock rate of the processor has been achieved. IF stage has been split into 2 stages which is IF and IS. Moreover, the I-cache and branch predictor are decomposed into 3 stages which means it required 3 clock cycles to access both components. The timing delay of ID stage is increased slightly because of the cache hit detection logic is in ID stage.

Now, the RISC32 has 6 pipeline stages and all the instructions in the testbench has been verified with no errors. The micro-architecture specifications which are involved in the splitting of IF stage has been presented in Chapter 5. With the well-developed documentations, the speed of the research work can be done faster.

8.2 Future Work

To further improve the performance of the processor, data cache should be replaced by pipelined data cache as the longest delay is data cache in MEM stage based on the timing delay in Appendix B. Some modifications need to be done on pipelined I-cache so it can be also used as D-cache.

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Appendix A: Timing Delay of 5-stage Pipeline Processor

```
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~IFID~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~

  -------------------------------------------------------------------    -------------------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
    SLICE_X56Y92         FDRE (Prop_fdre_C_Q)         0.518     9.228 r  u_datapath/uodp_if_pseudo_pc_reg[2]/Q
                         net (fo=328, routed)         2.181    11.409    u_datapath/bp/bbp_tag_ram_2_reg_0_15_18_23/ADDRA0
    SLICE_X46Y94                                                      r  u_datapath/bp/bbp_tag_ram_2_reg_0_15_18_23/RAMA/RADR0
    SLICE_X46Y94         RAMD32 (Prop_ramd32_RADR0_O)
                                                      0.150    11.559 r  u_datapath/bp/bbp_tag_ram_2_reg_0_15_18_23/RAMA/O
                         net (fo=1, routed)           1.122    12.680    u_datapath/bp/bbp_if_hit_way[2]1[18]
    SLICE_X48Y93                                                      r  u_datapath/bp/bbp_id_hit_way[2]_i_12/I0
    SLICE_X48Y93         LUT6 (Prop_lut6_I0_O)        0.328    13.008 r  u_datapath/bp/bbp_id_hit_way[2]_i_12/O
                         net (fo=1, routed)           0.000    13.008    u_datapath/bp/bbp_id_hit_way[2]_i_12_n_2
    SLICE_X48Y93                                                      r  u_datapath/bp/bbp_id_hit_way_reg[2]_i_4/S[2]
    SLICE_X48Y93         CARRY4 (Prop_carry4_S[2]_CO[3])
                                                      0.398    13.406 r  u_datapath/bp/bbp_id_hit_way_reg[2]_i_4/CO[3]
                         net (fo=1, routed)           0.000    13.406    u_datapath/bp/bbp_id_hit_way_reg[2]_i_4_n_2
    SLICE_X48Y94                                                      r  u_datapath/bp/bbp_id_hit_way_reg[2]_i_2/CI
    SLICE_X48Y94         CARRY4 (Prop_carry4_CI_CO[0])
                                                      0.271    13.677 r  u_datapath/bp/bbp_id_hit_way_reg[2]_i_2/CO[0]
                         net (fo=4, routed)           1.359    15.036    u_datapath/bp/bbp_if_hit_way[2]0
    SLICE_X48Y106                                                     r  u_datapath/bp/bbp_id_hit_way[2]_i_1/I0
    SLICE_X48Y106        LUT2 (Prop_lut2_I0_O)        0.373    15.409 r  u_datapath/bp/bbp_id_hit_way[2]_i_1/O
                         net (fo=5, routed)           0.670    16.079    u_datapath/bp/bbp_if_hit_way[2]
    SLICE_X42Y110                                                     r  u_datapath/bp/bbp_id_pred[1]_i_2/I5
    SLICE_X42Y110        LUT6 (Prop_lut6_I5_O)        0.124    16.203 r  u_datapath/bp/bbp_id_pred[1]_i_2/O
                         net (fo=1, routed)           0.286    16.490    u_datapath/bp/bbp_id_pred[1]_i_2_n_2
    SLICE_X42Y110                                                     r  u_datapath/bp/bbp_id_pred[1]_i_1/I0
    SLICE_X42Y110        LUT3 (Prop_lut3_I0_O)        0.124    16.614 r  u_datapath/bp/bbp_id_pred[1]_i_1/O
                         net (fo=34, routed)          0.682    17.296    u_datapath/bp/p_0_in212_in
    SLICE_X48Y107                                                     r  u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4/I3
    SLICE_X48Y107        LUT5 (Prop_lut5_I3_O)        0.124    17.420 f  u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4/O
                         net (fo=32, routed)          1.563    18.983    u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4_n_2
    SLICE_X56Y97                                                      f  u_datapath/bp/bobp_if_next_pc[7]_INST_0/I3
    SLICE_X56Y97         LUT6 (Prop_lut6_I3_O)        0.124    19.107 r  u_datapath/bp/bobp_if_next_pc[7]_INST_0/O
                         net (fo=1, routed)           0.427    19.534    u_datapath/ubp_next_pc[7]
    SLICE_X56Y96                                                      r  u_datapath/uodp_if_pc[7]_INST_0_i_1/I1
    SLICE_X56Y96         LUT5 (Prop_lut5_I1_O)        0.124    19.658 r  u_datapath/uodp_if_pc[7]_INST_0_i_1/O
                         net (fo=1, routed)           0.811    20.469    u_datapath/uodp_if_pc[7]_INST_0_i_1_n_2
    SLICE_X56Y94                                                      r  u_datapath/uodp_if_pc[7]_INST_0/I0
    SLICE_X56Y94         LUT5 (Prop_lut5_I0_O)        0.124    20.593 r  u_datapath/uodp_if_pc[7]_INST_0/O
                         net (fo=4, routed)           0.743    21.336    icache/uicac_cpu_addr[7]
    SLICE_X56Y80                                                      r  icache/cache_cell_i_35/I5
    SLICE_X56Y80         LUT6 (Prop_lut6_I5_O)        0.124    21.460 r  icache/cache_cell_i_35/O
                         net (fo=2, routed)           1.012    22.472    icache/cache_cell/bicr_addr[5]
    RAMB18_X1Y30         RAMB18E1                                     r  icache/cache_cell/bcr_array_reg/ADDRARDADDR[10]
  -------------------------------------------------------------------    -------------------
  Below shown the delay from u_datapath/uodp_if_pseudo_pc_reg to icache/cache_cell/bcr_array_reg/ADDRARDADDR:
  Data Path Delay:        13.762ns  (logic 2.906ns (21.116%)  route 10.856ns (78.884%))


  -------------------------------------------------------------------    -------------------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
    SLICE_X56Y92         FDRE (Prop_fdre_C_Q)         0.518     9.228 r  u_datapath/uodp_if_pseudo_pc_reg[2]/Q
                         net (fo=328, routed)         2.181    11.409    u_datapath/bp/bbp_tag_ram_2_reg_0_15_18_23/ADDRA0
    SLICE_X46Y94                                                      r  u_datapath/bp/bbp_tag_ram_2_reg_0_15_18_23/RAMA/RADR0
    SLICE_X46Y94         RAMD32 (Prop_ramd32_RADR0_O)
                                                      0.150    11.559 r  u_datapath/bp/bbp_tag_ram_2_reg_0_15_18_23/RAMA/O
                         net (fo=1, routed)           1.122    12.680    u_datapath/bp/bbp_if_hit_way[2]1[18]
    SLICE_X48Y93                                                      r  u_datapath/bp/bbp_id_hit_way[2]_i_12/I0
    SLICE_X48Y93         LUT6 (Prop_lut6_I0_O)        0.328    13.008 r  u_datapath/bp/bbp_id_hit_way[2]_i_12/O
                         net (fo=1, routed)           0.000    13.008    u_datapath/bp/bbp_id_hit_way[2]_i_12_n_2
    SLICE_X48Y93                                                      r  u_datapath/bp/bbp_id_hit_way_reg[2]_i_4/S[2]
    SLICE_X48Y93         CARRY4 (Prop_carry4_S[2]_CO[3])
                                                      0.398    13.406 r  u_datapath/bp/bbp_id_hit_way_reg[2]_i_4/CO[3]
                         net (fo=1, routed)           0.000    13.406    u_datapath/bp/bbp_id_hit_way_reg[2]_i_4_n_2
    SLICE_X48Y94                                                      r  u_datapath/bp/bbp_id_hit_way_reg[2]_i_2/CI
    SLICE_X48Y94         CARRY4 (Prop_carry4_CI_CO[0])
                                                      0.271    13.677 r  u_datapath/bp/bbp_id_hit_way_reg[2]_i_2/CO[0]
                         net (fo=4, routed)           1.359    15.036    u_datapath/bp/bbp_if_hit_way[2]0
```

```
    SLICE_X48Y106                                                r  u_datapath/bp/bbp_id_hit_way[2]_i_1/I0
    SLICE_X48Y106        LUT2 (Prop_lut2_I0_O)        0.373    15.409 r  u_datapath/bp/bbp_id_hit_way[2]_i_1/O
                    net (fo=5, routed)           0.670    16.079    u_datapath/bp/bbp_if_hit_way[2]
    SLICE_X42Y110                                                r  u_datapath/bp/bbp_id_pred[1]_i_2/I5
    SLICE_X42Y110        LUT6 (Prop_lut6_I5_O)        0.124    16.203 r  u_datapath/bp/bbp_id_pred[1]_i_2/O
                    net (fo=1, routed)           0.286    16.490    u_datapath/bp/bbp_id_pred[1]_i_2_n_2
    SLICE_X42Y110                                                r  u_datapath/bp/bbp_id_pred[1]_i_1/I0
    SLICE_X42Y110        LUT3 (Prop_lut3_I0_O)        0.124    16.614 r  u_datapath/bp/bbp_id_pred[1]_i_1/O
                    net (fo=34, routed)          0.682    17.296    u_datapath/bp/p_0_in212_in
    SLICE_X48Y107                                                r  u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4/I3
    SLICE_X48Y107        LUT5 (Prop_lut5_I3_O)        0.124    17.420 f  u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4/O
                    net (fo=32, routed)          1.546    18.966    u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4_n_2
    SLICE_X56Y97                                                 f  u_datapath/bp/bobp_if_next_pc[6]_INST_0/I3
    SLICE_X56Y97         LUT6 (Prop_lut6_I3_O)        0.124    19.090 r  u_datapath/bp/bobp_if_next_pc[6]_INST_0/O
                    net (fo=1, routed)           0.338    19.428    u_datapath/ubp_next_pc[6]
    SLICE_X57Y97                                                 r  u_datapath/uodp_if_pc[6]_INST_0_i_1/I1
    SLICE_X57Y97         LUT5 (Prop_lut5_I1_O)        0.124    19.552 r  u_datapath/uodp_if_pc[6]_INST_0_i_1/O
                    net (fo=1, routed)           0.848    20.400    u_datapath/uodp_if_pc[6]_INST_0_i_1_n_2
    SLICE_X57Y91                                                 r  u_datapath/uodp_if_pc[6]_INST_0/I0
    SLICE_X57Y91         LUT5 (Prop_lut5_I0_O)        0.124    20.524 r  u_datapath/uodp_if_pc[6]_INST_0/O
                    net (fo=4, routed)           0.879    21.403    icache/uicac_cpu_addr[6]
    SLICE_X56Y80                                                 r  icache/cache_cell_i_36/I5
    SLICE_X56Y80         LUT6 (Prop_lut6_I5_O)        0.124    21.527 r  icache/cache_cell_i_36/O
                    net (fo=2, routed)           0.869    22.397    icache/cache_cell/bicr_addr[4]
    RAMB18_X1Y30         RAMB18E1                                r  icache/cache_cell/bcr_array_reg/ADDRBWRADDR[9]
  -------------------------------------------------------------------    -------------------
  Below shown the delay from u_datapath/uodp_if_pseudo_pc_reg to icache/cache_cell/bcr_array_reg/ADDRBWRADDR:
  Data Path Delay:        13.687ns  (logic 2.906ns (21.232%)  route 10.781ns (78.768%))
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~IFID~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~IDEX~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~


  -------------------------------------------------------------------    -------------------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
    SLICE_X52Y80         FDRE (Prop_fdre_C_Q)         0.456     9.154 f  u_datapath/udp_id_instr_reg[30]/Q
                    net (fo=40, routed)          2.215    11.369    u_ctrlpath/b_mc/bimc_opcode[4]
    SLICE_X30Y89                                                 f  u_ctrlpath/b_mc/bomc_hilo_acc_INST_0_i_1/I1
    SLICE_X30Y89         LUT4 (Prop_lut4_I1_O)        0.124    11.493 f  u_ctrlpath/b_mc/bomc_hilo_acc_INST_0_i_1/O
                    net (fo=4, routed)           0.619    12.112    u_ctrlpath/b_mc/bomc_hilo_acc_INST_0_i_1_n_2
    SLICE_X41Y90                                                 f  u_ctrlpath/b_mc/bomc_jalr_INST_0/I5
    SLICE_X41Y90         LUT6 (Prop_lut6_I5_O)        0.124    12.236 r  u_ctrlpath/b_mc/bomc_jalr_INST_0/O
                    net (fo=3, routed)           1.295    13.530    u_datapath/bp/bibp_id_jalr
    SLICE_X45Y97                                                 r  u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_8/I2
    SLICE_X45Y97         LUT4 (Prop_lut4_I2_O)        0.124    13.654 f  u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_8/O
                    net (fo=33, routed)          1.237    14.891    u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_8_n_2
    SLICE_X48Y105                                                f  u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_2/I3
    SLICE_X48Y105        LUT5 (Prop_lut5_I3_O)        0.124    15.015 r  u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_2/O
                    net (fo=66, routed)          1.420    16.435    u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_2_n_2
    SLICE_X55Y98                                                 r  u_datapath/bp/bobp_if_next_pc[2]_INST_0_i_3/I1
    SLICE_X55Y98         LUT4 (Prop_lut4_I1_O)        0.152    16.587 r  u_datapath/bp/bobp_if_next_pc[2]_INST_0_i_3/O
                    net (fo=1, routed)           1.034    17.622    u_datapath/bp/bobp_if_next_pc[2]_INST_0_i_3_n_2
    SLICE_X58Y98                                                 r  u_datapath/bp/bobp_if_next_pc[2]_INST_0/I5
    SLICE_X58Y98         LUT6 (Prop_lut6_I5_O)        0.326    17.948 r  u_datapath/bp/bobp_if_next_pc[2]_INST_0/O
                    net (fo=1, routed)           0.171    18.118    u_datapath/ubp_next_pc[2]
    SLICE_X58Y98                                                 r  u_datapath/uodp_if_pc[2]_INST_0_i_1/I1
    SLICE_X58Y98         LUT5 (Prop_lut5_I1_O)        0.124    18.242 r  u_datapath/uodp_if_pc[2]_INST_0_i_1/O
                    net (fo=1, routed)           0.868    19.110    u_datapath/uodp_if_pc[2]_INST_0_i_1_n_2
    SLICE_X58Y92                                                 r  u_datapath/uodp_if_pc[2]_INST_0/I0
    SLICE_X58Y92         LUT5 (Prop_lut5_I0_O)        0.124    19.234 r  u_datapath/uodp_if_pc[2]_INST_0/O
                    net (fo=4, routed)           0.762    19.996    icache/uicac_cpu_addr[2]
    SLICE_X56Y81                                                 r  icache/cache_cell_i_40/I2
    SLICE_X56Y81         LUT5 (Prop_lut5_I2_O)        0.124    20.120 r  icache/cache_cell_i_40/O
                    net (fo=2, routed)           0.944    21.064    icache/cache_cell/bicr_addr[0]
    RAMB18_X1Y30         RAMB18E1                                r  icache/cache_cell/bcr_array_reg/ADDRARDADDR[5]
  -------------------------------------------------------------------    -------------------
  Below shown the delay from u_datapath/udp_id_instr_reg to icache/cache_cell/bcr_array_reg/ADDRARDADDR:
  Data Path Delay:        12.366ns  (logic 1.802ns (14.572%)  route 10.564ns (85.428%))

  -------------------------------------------------------------------    -------------------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
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  SLICE_X52Y80         FDRE (Prop_fdre_C_Q)         0.456     9.154 f  u_datapath/udp_id_instr_reg[30]/Q
                   net (fo=40, routed)          2.215    11.369    u_ctrlpath/b_mc/bimc_opcode[4]
  SLICE_X30Y89                                                  f  u_ctrlpath/b_mc/bomc_hilo_acc_INST_0_i_1/I1
  SLICE_X30Y89         LUT4 (Prop_lut4_I1_O)        0.124    11.493 f  u_ctrlpath/b_mc/bomc_hilo_acc_INST_0_i_1/O
                   net (fo=4, routed)           0.619    12.112    u_ctrlpath/b_mc/bomc_hilo_acc_INST_0_i_1_n_2
  SLICE_X41Y90                                                  f  u_ctrlpath/b_mc/bomc_jalr_INST_0/I5
  SLICE_X41Y90         LUT6 (Prop_lut6_I5_O)        0.124    12.236 r  u_ctrlpath/b_mc/bomc_jalr_INST_0/O
                   net (fo=3, routed)           1.295    13.530    u_datapath/bp/bibp_id_jalr
  SLICE_X45Y97                                                  r  u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_8/I2
  SLICE_X45Y97         LUT4 (Prop_lut4_I2_O)        0.124    13.654 f  u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_8/O
                   net (fo=33, routed)          1.237    14.891    u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_8_n_2
  SLICE_X48Y105                                                 f  u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_2/I3
  SLICE_X48Y105        LUT5 (Prop_lut5_I3_O)        0.124    15.015 r  u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_2/O
                   net (fo=66, routed)          1.420    16.435    u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_2_n_2
  SLICE_X55Y98                                                  r  u_datapath/bp/bobp_if_next_pc[2]_INST_0_i_3/I1
  SLICE_X55Y98         LUT4 (Prop_lut4_I1_O)        0.152    16.587 r  u_datapath/bp/bobp_if_next_pc[2]_INST_0_i_3/O
                   net (fo=1, routed)           1.034    17.622    u_datapath/bp/bobp_if_next_pc[2]_INST_0_i_3_n_2
  SLICE_X58Y98                                                  r  u_datapath/bp/bobp_if_next_pc[2]_INST_0/I5
  SLICE_X58Y98         LUT6 (Prop_lut6_I5_O)        0.326    17.948 r  u_datapath/bp/bobp_if_next_pc[2]_INST_0/O
                   net (fo=1, routed)           0.171    18.118    u_datapath/ubp_next_pc[2]
  SLICE_X58Y98                                                  r  u_datapath/uodp_if_pc[2]_INST_0_i_1/I1
  SLICE_X58Y98         LUT5 (Prop_lut5_I1_O)        0.124    18.242 r  u_datapath/uodp_if_pc[2]_INST_0_i_1/O
                   net (fo=1, routed)           0.868    19.110    u_datapath/uodp_if_pc[2]_INST_0_i_1_n_2
  SLICE_X58Y92                                                  r  u_datapath/uodp_if_pc[2]_INST_0/I0
  SLICE_X58Y92         LUT5 (Prop_lut5_I0_O)        0.124    19.234 r  u_datapath/uodp_if_pc[2]_INST_0/O
                   net (fo=4, routed)           0.762    19.996    icache/uicac_cpu_addr[2]
  SLICE_X56Y81                                                  r  icache/cache_cell_i_40/I2
  SLICE_X56Y81         LUT5 (Prop_lut5_I2_O)        0.124    20.120 r  icache/cache_cell_i_40/O
                   net (fo=2, routed)           0.890    21.010    icache/cache_cell/bicr_addr[0]
  RAMB18_X1Y30         RAMB18E1                                 r  icache/cache_cell/bcr_array_reg/ADDRBWRADDR[5]
  -------------------------------------------------------------------    -------------------
  Below shown the delay from u_datapath/udp_id_instr_reg to icache/cache_cell/bcr_array_reg/ADDRBWRADDR:
  Data Path Delay:        12.312ns  (logic 1.802ns (14.636%)  route 10.510ns (85.364%))

  -------------------------------------------------------------------    -------------------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
  SLICE_X52Y80         FDRE (Prop_fdre_C_Q)         0.456     9.154 f  u_datapath/udp_id_instr_reg[30]/Q
                   net (fo=40, routed)          3.488    12.642    u_ctrlpath/b_mc/bimc_opcode[4]
  SLICE_X9Y87                                                   f  u_ctrlpath/b_mc/bomc_lw_INST_0/I0
  SLICE_X9Y87          LUT6 (Prop_lut6_I0_O)        0.124    12.766 r  u_ctrlpath/b_mc/bomc_lw_INST_0/O
                   net (fo=2, routed)           0.958    13.724    u_datapath/uidp_lw
  SLICE_X10Y88                                                  r  u_datapath/b_itl_i_1/I2
  SLICE_X10Y88         LUT5 (Prop_lut5_I2_O)        0.124    13.848 r  u_datapath/b_itl_i_1/O
                   net (fo=1, routed)           1.234    15.082    u_datapath/b_itl/biitl_id_load
  SLICE_X32Y89                                                  r  u_datapath/b_itl/boitl_ld_use_pc_en_INST_0_i_2/I1
  SLICE_X32Y89         LUT4 (Prop_lut4_I1_O)        0.124    15.206 r  u_datapath/b_itl/boitl_ld_use_pc_en_INST_0_i_2/O
                   net (fo=2, routed)           0.407    15.613    u_datapath/b_itl/boitl_ld_use_pc_en_INST_0_i_2_n_2
  SLICE_X33Y89                                                  r  u_datapath/b_itl/boitl_ld_use_pc_en_INST_0/I2
  SLICE_X33Y89         LUT5 (Prop_lut5_I2_O)        0.119    15.732 r  u_datapath/b_itl/boitl_ld_use_pc_en_INST_0/O
                   net (fo=69, routed)          2.650    18.382    u_datapath/udp_itl_pc_en
  SLICE_X48Y108                                                 r  u_datapath/udp_id_instr[31]_i_2/I0
  SLICE_X48Y108        LUT3 (Prop_lut3_I0_O)        0.326    18.708 r  u_datapath/udp_id_instr[31]_i_2/O
                   net (fo=96, routed)          2.192    20.900    u_datapath/udp_id_instr[31]_i_2_n_2
  SLICE_X44Y78         FDRE                                     r  u_datapath/udp_id_instr_reg[21]/CE
  -------------------------------------------------------------------    -------------------
  Below shown the delay from u_datapath/udp_id_instr_reg to u_datapath/udp_id_instr_reg:
  Data Path Delay:        12.202ns  (logic 1.273ns (10.433%)  route 10.929ns (89.567%))
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    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
  SLICE_X31Y106        FDRE (Prop_fdre_C_Q)         0.456     9.169 r  u_datapath/udp_ex_rt32_reg[0]/Q
                   net (fo=2, routed)           1.160    10.330    u_datapath/udp_ex_rt32[0]
  SLICE_X28Y95                                                  r  u_datapath/b_alb_i_32/I2
  SLICE_X28Y95         LUT3 (Prop_lut3_I2_O)        0.150    10.480 r  u_datapath/b_alb_i_32/O
                   net (fo=80, routed)          1.047    11.527    u_datapath/b_alb/bialb_op_b[0]
  SLICE_X13Y91                                                  r  u_datapath/b_alb/boalb_out[3]_INST_0_i_7/I1
  SLICE_X13Y91         LUT2 (Prop_lut2_I1_O)        0.326    11.853 r  u_datapath/b_alb/boalb_out[3]_INST_0_i_7/O
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                 net (fo=1, routed)          0.500    12.353    u_datapath/b_alb/boalb_out[3]_INST_0_i_7_n_2
   SLICE_X10Y91                                                  r  u_datapath/b_alb/boalb_out[3]_INST_0_i_4/CYINIT
   SLICE_X10Y91        CARRY4 (Prop_carry4_CYINIT_CO[3])
                                             0.595    12.948 r  u_datapath/b_alb/boalb_out[3]_INST_0_i_4/CO[3]
                 net (fo=1, routed)          0.000    12.948    u_datapath/b_alb/boalb_out[3]_INST_0_i_4_n_2
   SLICE_X10Y92                                                  r  u_datapath/b_alb/boalb_out[7]_INST_0_i_4/CI
   SLICE_X10Y92        CARRY4 (Prop_carry4_CI_CO[3])
                                             0.117    13.065 r  u_datapath/b_alb/boalb_out[7]_INST_0_i_4/CO[3]
                 net (fo=1, routed)          0.000    13.065    u_datapath/b_alb/boalb_out[7]_INST_0_i_4_n_2
   SLICE_X10Y93                                                  r  u_datapath/b_alb/boalb_out[11]_INST_0_i_4/CI
   SLICE_X10Y93        CARRY4 (Prop_carry4_CI_CO[3])
                                             0.117    13.182 r  u_datapath/b_alb/boalb_out[11]_INST_0_i_4/CO[3]
                 net (fo=1, routed)          0.000    13.182    u_datapath/b_alb/boalb_out[11]_INST_0_i_4_n_2
   SLICE_X10Y94                                                  r  u_datapath/b_alb/boalb_out[15]_INST_0_i_4/CI
   SLICE_X10Y94        CARRY4 (Prop_carry4_CI_CO[3])
                                             0.117    13.299 r  u_datapath/b_alb/boalb_out[15]_INST_0_i_4/CO[3]
                 net (fo=1, routed)          0.000    13.299    u_datapath/b_alb/boalb_out[15]_INST_0_i_4_n_2
   SLICE_X10Y95                                                  r  u_datapath/b_alb/boalb_out[19]_INST_0_i_4/CI
   SLICE_X10Y95        CARRY4 (Prop_carry4_CI_CO[3])
                                             0.117    13.416 r  u_datapath/b_alb/boalb_out[19]_INST_0_i_4/CO[3]
                 net (fo=1, routed)          0.000    13.416    u_datapath/b_alb/boalb_out[19]_INST_0_i_4_n_2
   SLICE_X10Y96                                                  r  u_datapath/b_alb/boalb_out[23]_INST_0_i_4/CI
   SLICE_X10Y96        CARRY4 (Prop_carry4_CI_CO[3])
                                             0.117    13.533 r  u_datapath/b_alb/boalb_out[23]_INST_0_i_4/CO[3]
                 net (fo=1, routed)          0.000    13.533    u_datapath/b_alb/boalb_out[23]_INST_0_i_4_n_2
   SLICE_X10Y97                                                  r  u_datapath/b_alb/boalb_out[27]_INST_0_i_4/CI
   SLICE_X10Y97        CARRY4 (Prop_carry4_CI_CO[3])
                                             0.117    13.650 r  u_datapath/b_alb/boalb_out[27]_INST_0_i_4/CO[3]
                 net (fo=1, routed)          0.000    13.650    u_datapath/b_alb/boalb_out[27]_INST_0_i_4_n_2
   SLICE_X10Y98                                                  r  u_datapath/b_alb/boalb_out[31]_INST_0_i_2/CI
   SLICE_X10Y98        CARRY4 (Prop_carry4_CI_O[3])
                                             0.315    13.965 r  u_datapath/b_alb/boalb_out[31]_INST_0_i_2/O[3]
                 net (fo=3, routed)          0.487    14.452    u_datapath/b_alb/p_0_in
   SLICE_X9Y95                                                   r  u_datapath/b_alb/boalb_ovfs_INST_0/I3
   SLICE_X9Y95         LUT5 (Prop_lut5_I3_O)       0.307    14.759 r  u_datapath/b_alb/boalb_ovfs_INST_0/O
                 net (fo=44, routed)         2.057    16.816    u_datapath/b_cp0/bicp0_sovf
   SLICE_X44Y101                                                 r  u_datapath/b_cp0/bocp0_exc_flag_INST_0/I4
   SLICE_X44Y101       LUT6 (Prop_lut6_I4_O)       0.124    16.940 r  u_datapath/b_cp0/bocp0_exc_flag_INST_0/O
                 net (fo=127, routed)        1.840    18.779    urisc_cp0_exc_flag
   SLICE_X15Y82                                                  r  u_datapath_i_65/I2
   SLICE_X15Y82        LUT3 (Prop_lut3_I2_O)       0.124    18.903 f  u_datapath_i_65/O
                 net (fo=48, routed)         2.339    21.242    u_datapath/uidp_pipe_stall
   SLICE_X48Y108                                                 f  u_datapath/udp_id_instr[31]_i_2/I2
   SLICE_X48Y108       LUT3 (Prop_lut3_I2_O)       0.152    21.394 r  u_datapath/udp_id_instr[31]_i_2/O
                 net (fo=96, routed)         2.192    23.586    u_datapath/udp_id_instr[31]_i_2_n_2
   SLICE_X44Y78        FDRE                                      r  u_datapath/udp_id_instr_reg[21]/CE
  -------------------------------------------------------------------    -------------------
  Below shown the delay from u_datapath/udp_ex_rt32_reg to u_datapath/udp_id_instr_reg:
  Data Path Delay:        14.873ns  (logic 3.251ns (21.859%)  route 11.622ns (78.141%))
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    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
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   SLICE_X12Y85        FDRE (Prop_fdre_C_Q)        0.518     9.244 r  u_datapath/udp_mem_alb_out_reg[5]/Q
                 net (fo=47, routed)         1.147    10.391    dcache/ucac_tag_ram_reg_0_3_1_1/A0
   SLICE_X8Y85                                                   r  dcache/ucac_tag_ram_reg_0_3_1_1/SP/ADR0
   SLICE_X8Y85         RAMS32 (Prop_rams32_ADR0_O)
                                             0.105    10.496 r  dcache/ucac_tag_ram_reg_0_3_1_1/SP/O
                 net (fo=5, routed)          1.205    11.701    dcache/bififo_data0[1]
   SLICE_X7Y83                                                   r  dcache/uocac_cpu_stall_INST_0_i_16/I2
   SLICE_X7Y83         LUT6 (Prop_lut6_I2_O)       0.124    11.825 r  dcache/uocac_cpu_stall_INST_0_i_16/O
                 net (fo=1, routed)          0.000    11.825    dcache/uocac_cpu_stall_INST_0_i_16_n_2
   SLICE_X7Y83                                                   r  dcache/uocac_cpu_stall_INST_0_i_8/S[0]
   SLICE_X7Y83         CARRY4 (Prop_carry4_S[0]_CO[3])
                                             0.532    12.357 r  dcache/uocac_cpu_stall_INST_0_i_8/CO[3]
                 net (fo=1, routed)          0.000    12.357    dcache/uocac_cpu_stall_INST_0_i_8_n_2
   SLICE_X7Y84                                                   r  dcache/uocac_cpu_stall_INST_0_i_6/CI
   SLICE_X7Y84         CARRY4 (Prop_carry4_CI_CO[3])
                                             0.114    12.471 r  dcache/uocac_cpu_stall_INST_0_i_6/CO[3]
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                 net (fo=1, routed)          0.000    12.471    dcache/uocac_cpu_stall_INST_0_i_6_n_2
   SLICE_X7Y85                                         r  dcache/uocac_cpu_stall_INST_0_i_1/CI
   SLICE_X7Y85         CARRY4 (Prop_carry4_CI_CO[0])
                                      0.271    12.742 r  dcache/uocac_cpu_stall_INST_0_i_1/CO[0]
                 net (fo=3, routed)          0.784    13.526    dcache/ucac_hit1
   SLICE_X6Y77                                         r  dcache/b_cache_ctrl_i_2/I0
   SLICE_X6Y77         LUT5 (Prop_lut5_I0_O)       0.373    13.899 r  dcache/b_cache_ctrl_i_2/O
                 net (fo=21, routed)         0.609    14.508    dcache/b_cache_ctrl/bicac_ctrl_hit
   SLICE_X3Y80                                         r  dcache/b_cache_ctrl/bocac_ctrl_cpu_data_output_en_INST_0/I1
   SLICE_X3Y80                                   LUT4    (Prop_lut4_I1_O)                   0.124         14.632    r
dcache/b_cache_ctrl/bocac_ctrl_cpu_data_output_en_INST_0/O
                 net (fo=2, routed)          0.323    14.955    dcache/cache_cell/bicr_cpu_data_output_en
   SLICE_X4Y80                                         r  dcache/cache_cell/enz_31_INST_0/I0
   SLICE_X4Y80         LUT4 (Prop_lut4_I0_O)       0.124    15.079 r  dcache/cache_cell/enz_31_INST_0/O
                 net (fo=64, routed)         1.150    16.229    dcache_n_154
   SLICE_X5Y98                                         r  u_datapath_i_224/I3
   SLICE_X5Y98         LUT6 (Prop_lut6_I3_O)       0.124    16.353 r  u_datapath_i_224/O
                 net (fo=1, routed)          0.741    17.094    u_datapath_i_224_n_2
   SLICE_X5Y105                                        r  u_datapath_i_159/I1
   SLICE_X5Y105        LUT2 (Prop_lut2_I1_O)       0.124    17.218 r  u_datapath_i_159/O
                 net (fo=1, routed)          0.430    17.648    u_datapath_i_159_n_2
   SLICE_X5Y105                                        r  u_datapath_i_47/I0
   SLICE_X5Y105        LUT2 (Prop_lut2_I0_O)       0.153    17.801 r  u_datapath_i_47/O
                 net (fo=5, routed)          0.854    18.656    u_datapath/uidp_mdata[17]
   SLICE_X5Y106                                        r  u_datapath/uodp_ex_dm_store[9]_INST_0_i_5/I0
   SLICE_X5Y106        LUT6 (Prop_lut6_I0_O)       0.327    18.983 r  u_datapath/uodp_ex_dm_store[9]_INST_0_i_5/O
                 net (fo=1, routed)          0.469    19.452    u_datapath/data1[9]
   SLICE_X5Y106                                        r  u_datapath/uodp_ex_dm_store[9]_INST_0_i_4/I2
   SLICE_X5Y106        LUT4 (Prop_lut4_I2_O)       0.118    19.570 r  u_datapath/uodp_ex_dm_store[9]_INST_0_i_4/O
                 net (fo=1, routed)          0.563    20.132    u_datapath/uodp_ex_dm_store[9]_INST_0_i_4_n_2
   SLICE_X6Y105                                        r  u_datapath/uodp_ex_dm_store[9]_INST_0_i_3/I0
   SLICE_X6Y105        LUT6 (Prop_lut6_I0_O)       0.326    20.458 r  u_datapath/uodp_ex_dm_store[9]_INST_0_i_3/O
                 net (fo=5, routed)          0.894    21.352    u_datapath/data4[9]
   SLICE_X14Y108                                       r  u_datapath/uodp_ex_dm_store[9]_INST_0_i_1/I3
   SLICE_X14Y108       LUT6 (Prop_lut6_I3_O)       0.124    21.476 r  u_datapath/uodp_ex_dm_store[9]_INST_0_i_1/O
                 net (fo=2, routed)          0.980    22.457    u_datapath/uodp_ex_dm_store[9]_INST_0_i_1_n_2
   SLICE_X28Y112                                       r  u_datapath/uodp_ex_dm_store[1]_INST_0/I4
   SLICE_X28Y112       LUT5 (Prop_lut5_I4_O)       0.124    22.581 r  u_datapath/uodp_ex_dm_store[1]_INST_0/O
                 net (fo=18, routed)         1.978    24.559    dcache/uicac_cpu_data[1]
   SLICE_X12Y72                                        r  dcache/cache_cell_i_31/I4
   SLICE_X12Y72        LUT5 (Prop_lut5_I4_O)       0.124    24.683 r  dcache/cache_cell_i_31/O
                 net (fo=4, routed)          0.984    25.666    dcache/cache_cell/bicr_din[1]
   SLICE_X10Y72                                        r  dcache/cache_cell/bcr_array_reg_i_24/I2
   SLICE_X10Y72        LUT3 (Prop_lut3_I2_O)       0.157    25.823 r  dcache/cache_cell/bcr_array_reg_i_24/O
                 net (fo=1, routed)          0.652    26.475    dcache/cache_cell/bcr_array_reg_i_24_n_2
   RAMB18_X0Y29        RAMB18E1                              r  dcache/cache_cell/bcr_array_reg/DIBDI[1]
  -------------------------------------------------------------------    -------------------
  Below shown the delay from u_datapath/udp_mem_alb_out_reg to dcache/cache_cell/bcr_array_reg/DIBDI:
  Data Path Delay:        17.750ns  (logic 3.986ns (22.457%)  route 13.764ns (77.543%))

  -------------------------------------------------------------------    -------------------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
   SLICE_X12Y85        FDRE (Prop_fdre_C_Q)        0.518     9.244 r  u_datapath/udp_mem_alb_out_reg[5]/Q
                 net (fo=47, routed)         1.147    10.391    dcache/ucac_tag_ram_reg_0_3_1_1/A0
   SLICE_X8Y85                                         r  dcache/ucac_tag_ram_reg_0_3_1_1/SP/ADR0
   SLICE_X8Y85         RAMS32 (Prop_rams32_ADR0_O)
                                      0.105    10.496 r  dcache/ucac_tag_ram_reg_0_3_1_1/SP/O
                 net (fo=5, routed)          1.205    11.701    dcache/bififo_data0[1]
   SLICE_X7Y83                                         r  dcache/uocac_cpu_stall_INST_0_i_16/I2
   SLICE_X7Y83         LUT6 (Prop_lut6_I2_O)       0.124    11.825 r  dcache/uocac_cpu_stall_INST_0_i_16/O
                 net (fo=1, routed)          0.000    11.825    dcache/uocac_cpu_stall_INST_0_i_16_n_2
   SLICE_X7Y83                                         r  dcache/uocac_cpu_stall_INST_0_i_8/S[0]
   SLICE_X7Y83         CARRY4 (Prop_carry4_S[0]_CO[3])
                                      0.532    12.357 r  dcache/uocac_cpu_stall_INST_0_i_8/CO[3]
                 net (fo=1, routed)          0.000    12.357    dcache/uocac_cpu_stall_INST_0_i_8_n_2
   SLICE_X7Y84                                         r  dcache/uocac_cpu_stall_INST_0_i_6/CI
   SLICE_X7Y84         CARRY4 (Prop_carry4_CI_CO[3])
                                      0.114    12.471 r  dcache/uocac_cpu_stall_INST_0_i_6/CO[3]
                 net (fo=1, routed)          0.000    12.471    dcache/uocac_cpu_stall_INST_0_i_6_n_2
   SLICE_X7Y85                                         r  dcache/uocac_cpu_stall_INST_0_i_1/CI
   SLICE_X7Y85         CARRY4 (Prop_carry4_CI_CO[0])
                                      0.271    12.742 r  dcache/uocac_cpu_stall_INST_0_i_1/CO[0]
                 net (fo=3, routed)          0.784    13.526    dcache/ucac_hit1
   SLICE_X6Y77                                         r  dcache/b_cache_ctrl_i_2/I0
```

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   SLICE_X6Y77         LUT5 (Prop_lut5_I0_O)       0.373    13.899 r  dcache/b_cache_ctrl_i_2/O
                  net (fo=21, routed)          0.609    14.508    dcache/b_cache_ctrl/bicac_ctrl_hit
   SLICE_X3Y80                                            r  dcache/b_cache_ctrl/bocac_ctrl_cpu_data_output_en_INST_0/I1
   SLICE_X3Y80                                   LUT4    (Prop_lut4_I1_O)                    0.124              14.632    r
dcache/b_cache_ctrl/bocac_ctrl_cpu_data_output_en_INST_0/O
                  net (fo=2, routed)           0.323    14.955    dcache/cache_cell/bicr_cpu_data_output_en
   SLICE_X4Y80                                            r  dcache/cache_cell/enz_31_INST_0/I0
   SLICE_X4Y80         LUT4 (Prop_lut4_I0_O)       0.124    15.079 r  dcache/cache_cell/enz_31_INST_0/O
                  net (fo=64, routed)          0.917    15.996    dcache_n_160
   SLICE_X2Y89                                            r  u_datapath_i_236/I3
   SLICE_X2Y89         LUT6 (Prop_lut6_I3_O)       0.124    16.120 r  u_datapath_i_236/O
                  net (fo=1, routed)           0.965    17.085    u_datapath_i_236_n_2
   SLICE_X3Y101                                           r  u_datapath_i_171/I1
   SLICE_X3Y101        LUT2 (Prop_lut2_I1_O)       0.124    17.209 r  u_datapath_i_171/O
                  net (fo=1, routed)           0.856    18.065    u_datapath_i_171_n_2
   SLICE_X3Y101                                           r  u_datapath_i_53/I0
   SLICE_X3Y101        LUT2 (Prop_lut2_I0_O)       0.154    18.219 r  u_datapath_i_53/O
                  net (fo=5, routed)           0.806    19.025    u_datapath/uidp_mdata[11]
   SLICE_X6Y105                                           r  u_datapath/uodp_ex_dm_store[27]_INST_0_i_4/I0
   SLICE_X6Y105        LUT6 (Prop_lut6_I0_O)       0.327    19.352 r  u_datapath/uodp_ex_dm_store[27]_INST_0_i_4/O
                  net (fo=2, routed)           0.685    20.037    u_datapath/data0[27]
   SLICE_X9Y107                                           r  u_datapath/uodp_ex_dm_store[3]_INST_0_i_3/I1
   SLICE_X9Y107        LUT6 (Prop_lut6_I1_O)       0.124    20.161 r  u_datapath/uodp_ex_dm_store[3]_INST_0_i_3/O
                  net (fo=4, routed)           1.184    21.345    u_datapath/data4[3]
   SLICE_X28Y110                                          r  u_datapath/uodp_ex_dm_store[3]_INST_0_i_1/I0
   SLICE_X28Y110       LUT3 (Prop_lut3_I0_O)       0.150    21.495 r  u_datapath/uodp_ex_dm_store[3]_INST_0_i_1/O
                  net (fo=3, routed)           0.471    21.966    u_datapath/udp_fw_data_ex_rt32[3]
   SLICE_X28Y110                                          r  u_datapath/uodp_ex_dm_store[3]_INST_0_i_2/I3
   SLICE_X28Y110       LUT6 (Prop_lut6_I3_O)       0.326    22.292 r  u_datapath/uodp_ex_dm_store[3]_INST_0_i_2/O
                  net (fo=1, routed)           0.433    22.725    u_datapath/uodp_ex_dm_store[3]_INST_0_i_2_n_2
   SLICE_X28Y110                                          r  u_datapath/uodp_ex_dm_store[3]_INST_0/I2
   SLICE_X28Y110       LUT5 (Prop_lut5_I2_O)       0.124    22.849 r  u_datapath/uodp_ex_dm_store[3]_INST_0/O
                  net (fo=18, routed)          1.932    24.780    dcache/uicac_cpu_data[3]
   SLICE_X13Y75                                           r  dcache/cache_cell_i_29/I4
   SLICE_X13Y75        LUT5 (Prop_lut5_I4_O)       0.124    24.904 r  dcache/cache_cell_i_29/O
                  net (fo=4, routed)           0.849    25.753    dcache/cache_cell/bicr_din[3]
   SLICE_X9Y72                                            r  dcache/cache_cell/bcr_array_reg_i_6/I2
   SLICE_X9Y72         LUT3 (Prop_lut3_I2_O)       0.150    25.903 r  dcache/cache_cell/bcr_array_reg_i_6/O
                  net (fo=1, routed)           0.317    26.220    dcache/cache_cell/bcr_array_reg_i_6_n_2
   RAMB18_X0Y29        RAMB18E1                                 r  dcache/cache_cell/bcr_array_reg/DIADI[11]
  -------------------------------------------------------------------    -------------------
  Below shown the delay from u_datapath/udp_mem_alb_out_reg to dcache/cache_cell/bcr_array_reg/DIADI:
  Data Path Delay:        17.494ns  (logic 4.012ns (22.933%)  route 13.482ns (77.067%))
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  -------------------------------------------------------------------    -------------------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
    SLICE_X34Y92         FDSE (Prop_fdse_C_Q)        0.518     9.242 r  u_datapath/udp_wb_rt5_rd5_reg[0]/Q
                  net (fo=98, routed)          3.465    12.707    u_datapath/b_rf/brf_reg_ram_reg_r1_0_31_12_17/ADDRD0
    SLICE_X34Y108        RAMD32                              r  u_datapath/b_rf/brf_reg_ram_reg_r1_0_31_12_17/RAMA/WADR0
  -------------------------------------------------------------------    -------------------
  Below         shown         the         delay         from         u_datapath/udp_wb_rt5_rd5_reg         to
u_datapath/b_rf/brf_reg_ram_reg_r1_0_31_12_17/RAMA/WADR0:
  Data Path Delay:        3.983ns  (logic 0.518ns (13.006%)  route 3.465ns (86.994%))


  -------------------------------------------------------------------    -------------------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
    SLICE_X34Y92         FDSE (Prop_fdse_C_Q)        0.518     9.242 r  u_datapath/udp_wb_rt5_rd5_reg[0]/Q
                  net (fo=98, routed)          3.465    12.707    u_datapath/b_rf/brf_reg_ram_reg_r1_0_31_12_17/ADDRD0
    SLICE_X34Y108                    RAMD32                                                                  r
u_datapath/b_rf/brf_reg_ram_reg_r1_0_31_12_17/RAMA_D1/WADR0
  -------------------------------------------------------------------    -------------------
  Below         shown         the         delay         from         u_datapath/udp_wb_rt5_rd5_reg         to
u_datapath/b_rf/brf_reg_ram_reg_r1_0_31_12_17/RAMA_D1/WADR0:
  Data Path Delay:        3.983ns  (logic 0.518ns (13.006%)  route 3.465ns (86.994%))


  -------------------------------------------------------------------    -------------------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
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  --------------------------------------------------------------------    -------------------
    SLICE_X34Y92         FDSE (Prop_fdse_C_Q)         0.518     9.242 r  u_datapath/udp_wb_rt5_rd5_reg[0]/Q
                         net (fo=98, routed)          3.465    12.707    u_datapath/b_rf/brf_reg_ram_reg_r1_0_31_12_17/ADDRD0
    SLICE_X34Y108        RAMD32                                        r  u_datapath/b_rf/brf_reg_ram_reg_r1_0_31_12_17/RAMB/WADR0
  --------------------------------------------------------------------    -------------------
  Below shown the delay from u_datapath/udp_wb_rt5_rd5_reg to u_datapath/b_rf/brf_reg_ram_reg_r1_0_31_12_17/RAMB/WADR0:
  Data Path Delay:        3.983ns  (logic 0.518ns (13.006%)  route 3.465ns (86.994%))


  --------------------------------------------------------------------    -------------------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  --------------------------------------------------------------------    -------------------
    SLICE_X34Y92         FDSE (Prop_fdse_C_Q)         0.518     9.242 r  u_datapath/udp_wb_rt5_rd5_reg[0]/Q
                         net (fo=98, routed)          3.465    12.707    u_datapath/b_rf/brf_reg_ram_reg_r1_0_31_12_17/ADDRD0
    SLICE_X34Y108        RAMD32                                        r  u_datapath/b_rf/brf_reg_ram_reg_r1_0_31_12_17/RAMB_D1/WADR0
  --------------------------------------------------------------------    -------------------
  Below shown the delay from u_datapath/udp_wb_rt5_rd5_reg to u_datapath/b_rf/brf_reg_ram_reg_r1_0_31_12_17/RAMB_D1/WADR0:
  Data Path Delay:        3.983ns  (logic 0.518ns (13.006%)  route 3.465ns (86.994%))


  --------------------------------------------------------------------    -------------------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  --------------------------------------------------------------------    -------------------
    SLICE_X34Y92         FDSE (Prop_fdse_C_Q)         0.518     9.242 r  u_datapath/udp_wb_rt5_rd5_reg[0]/Q
                         net (fo=98, routed)          3.465    12.707    u_datapath/b_rf/brf_reg_ram_reg_r1_0_31_12_17/ADDRD0
    SLICE_X34Y108        RAMD32                                        r  u_datapath/b_rf/brf_reg_ram_reg_r1_0_31_12_17/RAMC/WADR0
  --------------------------------------------------------------------    -------------------
  Below shown the delay from u_datapath/udp_wb_rt5_rd5_reg to u_datapath/b_rf/brf_reg_ram_reg_r1_0_31_12_17/RAMC/WADR0:
  Data Path Delay:        3.983ns  (logic 0.518ns (13.006%)  route 3.465ns (86.994%))
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~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~WB~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
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Appendix B: Timing Delay of 6-stage Pipeline Processor

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~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~IFIS~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
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  -------------------------------------------------------------------    -------------------
   Location            Delay type               Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
   SLICE_X59Y94        FDRE (Prop_fdre_C_Q)        0.456     9.170 r  u_datapath/uodp_if_pseudo_pc_reg[10]/Q
                 net (fo=6, routed)          1.416    10.586    u_datapath/uodp_if_pseudo_pc[10]
   SLICE_X57Y99                                              r  u_datapath/bp_i_46/S[1]
   SLICE_X57Y99        CARRY4 (Prop_carry4_S[1]_CO[3])
                                        0.674    11.260 r  u_datapath/bp_i_46/CO[3]
                 net (fo=1, routed)          0.001    11.261    u_datapath/bp_i_46_n_2
   SLICE_X57Y100                                              r  u_datapath/bp_i_45/CI
   SLICE_X57Y100       CARRY4 (Prop_carry4_CI_CO[3])
                                        0.114    11.375 r  u_datapath/bp_i_45/CO[3]
                 net (fo=1, routed)          0.000    11.375    u_datapath/bp_i_45_n_2
   SLICE_X57Y101                                              r  u_datapath/bp_i_44/CI
   SLICE_X57Y101       CARRY4 (Prop_carry4_CI_CO[3])
                                        0.114    11.489 r  u_datapath/bp_i_44/CO[3]
                 net (fo=1, routed)          0.000    11.489    u_datapath/bp_i_44_n_2
   SLICE_X57Y102                                              r  u_datapath/bp_i_43/CI
   SLICE_X57Y102       CARRY4 (Prop_carry4_CI_CO[3])
                                        0.114    11.603 r  u_datapath/bp_i_43/CO[3]
                 net (fo=1, routed)          0.000    11.603    u_datapath/bp_i_43_n_2
   SLICE_X57Y103                                              r  u_datapath/bp_i_42/CI
   SLICE_X57Y103       CARRY4 (Prop_carry4_CI_O[2])
                                        0.256    11.859 r  u_datapath/bp_i_42/O[2]
                 net (fo=2, routed)          0.935    12.794    u_datapath/bp/bibp_if_pc4[27]
   SLICE_X57Y106                                              r  u_datapath/bp/bobp_if_next_pc[27]_INST_0_i_2/I5
   SLICE_X57Y106       LUT6 (Prop_lut6_I5_O)       0.302    13.096 r  u_datapath/bp/bobp_if_next_pc[27]_INST_0_i_2/O
                 net (fo=1, routed)          0.877    13.972    u_datapath/bp/bobp_if_next_pc[27]_INST_0_i_2_n_2
   SLICE_X57Y106                                              r  u_datapath/bp/bobp_if_next_pc[27]_INST_0/I2
   SLICE_X57Y106       LUT6 (Prop_lut6_I2_O)       0.124    14.096 r  u_datapath/bp/bobp_if_next_pc[27]_INST_0/O
                 net (fo=1, routed)          0.515    14.611    u_datapath/ubp_next_pc[27]
   SLICE_X58Y106                                              r  u_datapath/uodp_if_pseudo_pc[27]_i_3/I3
   SLICE_X58Y106       LUT6 (Prop_lut6_I3_O)       0.124    14.735 f  u_datapath/uodp_if_pseudo_pc[27]_i_3/O
                 net (fo=1, routed)          0.436    15.171    u_datapath/uodp_if_pseudo_pc[27]_i_3_n_2
   SLICE_X58Y105                                              f  u_datapath/uodp_if_pseudo_pc[27]_i_2/I5
   SLICE_X58Y105       LUT6 (Prop_lut6_I5_O)       0.124    15.295 r  u_datapath/uodp_if_pseudo_pc[27]_i_2/O
                 net (fo=1, routed)          0.585    15.880    u_datapath/uodp_if_pseudo_pc[27]_i_2_n_2
   SLICE_X58Y105                                              r  u_datapath/uodp_if_pseudo_pc[27]_i_1/I3
   SLICE_X58Y105       LUT4 (Prop_lut4_I3_O)       0.124    16.004 r  u_datapath/uodp_if_pseudo_pc[27]_i_1/O
                 net (fo=1, routed)          0.000    16.004    u_datapath/p_1_in[27]
   SLICE_X58Y105       FDSE                                       r  u_datapath/uodp_if_pseudo_pc_reg[27]/D
  -------------------------------------------------------------------    -------------------
  Below shown the delay from u_datapath/uodp_if_pseudo_pc_reg to u_datapath/uodp_if_pseudo_pc_reg:
  Data Path Delay:        7.289ns  (logic 2.526ns (34.654%)  route 4.763ns (65.346%))
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~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~ISID(icache)~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
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  -------------------------------------------------------------------    -------------------
   Location            Delay type               Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
   SLICE_X13Y89        FDRE (Prop_fdre_C_Q)        0.456     9.184 r  icache/ucac_is_reg_cpu_addr_reg[5]/Q
                 net (fo=34, routed)          2.248    11.432    icache/ucac_is_reg_cpu_addr[5]
   SLICE_X13Y83                                              r  icache/cache_cell_i_37/I3
   SLICE_X13Y83        LUT4 (Prop_lut4_I3_O)       0.124    11.556 r  icache/cache_cell_i_37/O
                 net (fo=151, routed)         3.310    14.866    icache/cache_cell/bcr_array_reg_0_255_19_19/A3
   SLICE_X34Y80                                              r  icache/cache_cell/bcr_array_reg_0_255_19_19/RAMS64E_D/ADR3
   SLICE_X34Y80        RAMS64E (Prop_rams64e_ADR3_O)
                                        0.124    14.990 r  icache/cache_cell/bcr_array_reg_0_255_19_19/RAMS64E_D/O
                 net (fo=1, routed)          0.000    14.990    icache/cache_cell/bcr_array_reg_0_255_19_19/OD
   SLICE_X34Y80                                              r  icache/cache_cell/bcr_array_reg_0_255_19_19/F7.B/I0
   SLICE_X34Y80                       MUXF7     (Prop_muxf7_I0_O)               0.241             15.231    r
icache/cache_cell/bcr_array_reg_0_255_19_19/F7.B/O
                 net (fo=1, routed)          0.000    15.231    icache/cache_cell/bcr_array_reg_0_255_19_19/O0
   SLICE_X34Y80                                              r  icache/cache_cell/bcr_array_reg_0_255_19_19/F8/I0
   SLICE_X34Y80       MUXF8 (Prop_muxf8_I0_O)     0.098    15.329 r  icache/cache_cell/bcr_array_reg_0_255_19_19/F8/O
```

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                net (fo=2, routed)          1.020    16.349    icache/cache_cell/bcr_dout0[19]
   SLICE_X39Y83                                                r  icache/cache_cell/bocr_dout[3]_INST_0_i_2/I0
   SLICE_X39Y83         LUT6 (Prop_lut6_I0_O)       0.319    16.668 r  icache/cache_cell/bocr_dout[3]_INST_0_i_2/O
                net (fo=1, routed)          0.955    17.623    icache/cache_cell/bocr_dout[3]_INST_0_i_2_n_2
   SLICE_X40Y86                                                r  icache/cache_cell/bocr_dout[3]_INST_0_i_1/I4
   SLICE_X40Y86         LUT5 (Prop_lut5_I4_O)       0.124    17.747 r  icache/cache_cell/bocr_dout[3]_INST_0_i_1/O
                net (fo=1, routed)          0.433    18.181    icache/cache_cell/bocr_dout[3]_INST_0_i_1_n_2
   SLICE_X40Y86                                                r  icache/cache_cell/bocr_dout[3]_INST_0/I0
   SLICE_X40Y86         LUT1 (Prop_lut1_I0_O)       0.124    18.305 r  icache/cache_cell/bocr_dout[3]_INST_0/O
                net (fo=1, routed)          0.667    18.972    icache/cache_cell_n_31
   SLICE_X40Y86                                                r  icache/ucac_id_mem_data[3]_i_1/I0
   SLICE_X40Y86         LUT2 (Prop_lut2_I0_O)       0.124    19.096 r  icache/ucac_id_mem_data[3]_i_1/O
                net (fo=1, routed)          0.000    19.096    icache/ucac_is_mem_data[3]
   SLICE_X40Y86         FDRE                                   r  icache/ucac_id_mem_data_reg[3]/D
  -------------------------------------------------------------------    -------------------
  Below shown the delay from icache/ucac_is_reg_cpu_addr_reg to icache/ucac_id_mem_data_reg:
  Data Path Delay:        10.367ns  (logic 1.734ns (16.726%)  route 8.633ns (83.274%))
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~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~ISID(icache)~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
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~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~ISID(branch predictor)~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
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  -------------------------------------------------------------------    -------------------
   Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
   SLICE_X49Y94         FDRE (Prop_fdre_C_Q)        0.456     9.174 r  u_datapath/bp/bbp_is_pc_index_reg[1]/Q
                net (fo=321, routed)        4.209    13.384    u_datapath/bp/bbp_is_pc_index__0[1]
   SLICE_X39Y127                                               r  u_datapath/bp/bbp_id_hit_way[1]_i_9/I3
   SLICE_X39Y127        LUT6 (Prop_lut6_I3_O)       0.124    13.508 r  u_datapath/bp/bbp_id_hit_way[1]_i_9/O
                net (fo=1, routed)          0.482    13.989    u_datapath/bp/bbp_id_hit_way[1]_i_9_n_2
   SLICE_X39Y129                                               r  u_datapath/bp/bbp_id_hit_way[1]_i_3/I5
   SLICE_X39Y129        LUT6 (Prop_lut6_I5_O)       0.124    14.113 r  u_datapath/bp/bbp_id_hit_way[1]_i_3/O
                net (fo=1, routed)          1.161    15.274    u_datapath/bp/bbp_valid_ram_1
   SLICE_X44Y117                                               r  u_datapath/bp/bbp_id_hit_way[1]_i_1/I1
   SLICE_X44Y117        LUT2 (Prop_lut2_I1_O)       0.124    15.398 r  u_datapath/bp/bbp_id_hit_way[1]_i_1/O
                net (fo=38, routed)         0.818    16.216    u_datapath/bp/bbp_is_hit_way[1]
   SLICE_X42Y117                                               r  u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_7/I3
   SLICE_X42Y117        LUT6 (Prop_lut6_I3_O)       0.124    16.340 r  u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_7/O
                net (fo=34, routed)         1.497    17.837    u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_7_n_2
   SLICE_X51Y104                                               r  u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_1/I3
   SLICE_X51Y104        LUT5 (Prop_lut5_I3_O)       0.152    17.989 r  u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_1/O
                net (fo=32, routed)         1.689    19.678    u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_1_n_2
   SLICE_X54Y98                                                r  u_datapath/bp/bobp_if_next_pc[12]_INST_0/I0
   SLICE_X54Y98         LUT6 (Prop_lut6_I0_O)       0.326    20.004 r  u_datapath/bp/bobp_if_next_pc[12]_INST_0/O
                net (fo=1, routed)          0.601    20.604    u_datapath/ubp_next_pc[12]
   SLICE_X60Y98                                                r  u_datapath/uodp_if_pseudo_pc[12]_i_8/I3
   SLICE_X60Y98         LUT6 (Prop_lut6_I3_O)       0.124    20.728 f  u_datapath/uodp_if_pseudo_pc[12]_i_8/O
                net (fo=1, routed)          0.592    21.320    u_datapath/uodp_if_pseudo_pc[12]_i_8_n_2
   SLICE_X59Y95                                                f  u_datapath/uodp_if_pseudo_pc[12]_i_3/I0
   SLICE_X59Y95         LUT6 (Prop_lut6_I0_O)       0.124    21.444 f  u_datapath/uodp_if_pseudo_pc[12]_i_3/O
                net (fo=1, routed)          0.401    21.845    u_datapath/uodp_if_pseudo_pc[12]_i_3_n_2
   SLICE_X59Y94                                                f  u_datapath/uodp_if_pseudo_pc[12]_i_1/I3
   SLICE_X59Y94         LUT4 (Prop_lut4_I3_O)       0.118    21.963 r  u_datapath/uodp_if_pseudo_pc[12]_i_1/O
                net (fo=1, routed)          0.000    21.963    u_datapath/p_1_in[12]
   SLICE_X59Y94         FDRE                                   r  u_datapath/uodp_if_pseudo_pc_reg[12]/D
  -------------------------------------------------------------------    -------------------
  Below shown the delay from u_datapath/bp/bbp_is_pc_index_reg to u_datapath/uodp_if_pseudo_pc_reg:
  Data Path Delay:        13.245ns  (logic 1.796ns (13.560%)  route 11.449ns (86.440%))
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~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~ISID(branch predictor)~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
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~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~IDEX(icache)~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
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  -------------------------------------------------------------------    -------------------
   Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
   SLICE_X13Y88         FDRE (Prop_fdre_C_Q)        0.456     9.183 r  icache/ucac_id_reg_cpu_addr_reg[1]/Q
                net (fo=1, routed)          0.902    10.086    icache/ucac_id_reg_cpu_addr_reg_n_2_[1]
   SLICE_X13Y88                                                r  icache/uocac_cpu_data[31]_INST_0_i_7/I1
   SLICE_X13Y88         LUT4 (Prop_lut4_I1_O)       0.124    10.210 r  icache/uocac_cpu_data[31]_INST_0_i_7/O
                net (fo=2, routed)          0.603    10.812    icache/uocac_cpu_data[31]_INST_0_i_7_n_2
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  SLICE_X9Y87                                  r  icache/uocac_cpu_data[31]_INST_0_i_4/I4
  SLICE_X9Y87         LUT5 (Prop_lut5_I4_O)       0.118    10.930 f  icache/uocac_cpu_data[31]_INST_0_i_4/O
                      net (fo=2, routed)          0.966    11.896    icache/uocac_cpu_data[31]_INST_0_i_4_n_2
  SLICE_X12Y87                                  f  icache/uocac_cpu_data[31]_INST_0_i_2/I1
  SLICE_X12Y87        LUT4 (Prop_lut4_I1_O)       0.348    12.244 f  icache/uocac_cpu_data[31]_INST_0_i_2/O
                      net (fo=34, routed)         0.340    12.584    icache/uocac_cpu_data[31]_INST_0_i_2_n_2
  SLICE_X12Y86                                  f  icache/uocac_cpu_data[31]_INST_0_i_1/I0
  SLICE_X12Y86        LUT6 (Prop_lut6_I0_O)       0.328    12.912 f  icache/uocac_cpu_data[31]_INST_0_i_1/O
                      net (fo=36, routed)         1.259    14.171    icache/uocac_cpu_data[31]_INST_0_i_1_n_2
  SLICE_X44Y87                                  f  icache/uocac_cpu_data[4]_INST_0/I0
  SLICE_X44Y87        LUT3 (Prop_lut3_I0_O)       0.150    14.321 f  icache/uocac_cpu_data[4]_INST_0/O
                      net (fo=3, routed)          1.308    15.628    u_datapath/uidp_instr[4]
  SLICE_X35Y92                                  f  u_datapath/uodp_funct[4]_INST_0/I0
  SLICE_X35Y92        LUT3 (Prop_lut3_I0_O)       0.326    15.954 f  u_datapath/uodp_funct[4]_INST_0/O
                      net (fo=16, routed)         1.107    17.061    u_ctrlpath/b_mc/bimc_funct[4]
  SLICE_X14Y94                                  f  u_ctrlpath/b_mc/bomc_jalr_INST_0_i_1/I2
  SLICE_X14Y94        LUT4 (Prop_lut4_I2_O)       0.124    17.185 r  u_ctrlpath/b_mc/bomc_jalr_INST_0_i_1/O
                      net (fo=2, routed)          0.670    17.855    u_ctrlpath/b_mc/bomc_jalr_INST_0_i_1_n_2
  SLICE_X15Y94                                  r  u_ctrlpath/b_mc/bomc_syscall_INST_0/I5
  SLICE_X15Y94        LUT6 (Prop_lut6_I5_O)       0.124    17.979 r  u_ctrlpath/b_mc/bomc_syscall_INST_0/O
                      net (fo=8, routed)          0.950    18.929    u_datapath/b_cp0/bicp0_syscall
  SLICE_X28Y94                                  r  u_datapath/b_cp0/bocp0_exc_flag_INST_0/I2
  SLICE_X28Y94        LUT6 (Prop_lut6_I2_O)       0.124    19.053 r  u_datapath/b_cp0/bocp0_exc_flag_INST_0/O
                      net (fo=143, routed)        0.767    19.820    urisc_cp0_exc_flag
  SLICE_X9Y94                                   r  u_datapath_i_33/I2
  SLICE_X9Y94         LUT3 (Prop_lut3_I2_O)       0.124    19.944 f  u_datapath_i_33/O
                      net (fo=62, routed)         2.034    21.978    u_datapath/uidp_pipe_stall
  SLICE_X59Y94                                  f  u_datapath/bp_i_59/I0
  SLICE_X59Y94        LUT2 (Prop_lut2_I0_O)       0.124    22.102 f  u_datapath/bp_i_59/O
                      net (fo=2, routed)          0.936    23.039    u_datapath/bp/bibp_cpu_stall
  SLICE_X49Y94                                  f  u_datapath/bp/bbp_id_pc_index[3]_i_1/I2
  SLICE_X49Y94        LUT5 (Prop_lut5_I2_O)       0.150    23.189 r  u_datapath/bp/bbp_id_pc_index[3]_i_1/O
                      net (fo=75, routed)         2.001    25.189    u_datapath/bp/bbp_is_pc_tag0
  SLICE_X36Y130       FDRE                                     r  u_datapath/bp/bbp_id_lru_reg[1][0]/R
 -------------------------------------------------------------------    -------------------
 Below shown the delay from icache/ucac_id_reg_cpu_addr_reg to u_datapath/bp/bbp_id_lru_reg:
 Data Path Delay:        16.462ns  (logic 2.620ns (15.915%)  route 13.842ns (84.085%))
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~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~IDEX(icache)~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
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  Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
 -------------------------------------------------------------------    -------------------
  SLICE_X49Y94        FDRE (Prop_fdre_C_Q)        0.456     9.174 r  u_datapath/bp/bbp_id_pc_index_reg[0]/Q
                      net (fo=392, routed)        5.123    14.298    u_datapath/bp/bbp_id_pc_index[0]
  SLICE_X44Y123                                 r  u_datapath/bp/bbp_valid_ram_3[5]_i_2/I3
  SLICE_X44Y123       LUT4 (Prop_lut4_I3_O)       0.154    14.452 r  u_datapath/bp/bbp_valid_ram_3[5]_i_2/O
                      net (fo=8, routed)          2.146    16.597    u_datapath/bp/bbp_lru_ram_3_reg[5]
  SLICE_X44Y129                                 r  u_datapath/bp/bbp_lru_ram_2[5][1]_i_2/I4
  SLICE_X44Y129       LUT6 (Prop_lut6_I4_O)       0.327    16.924 r  u_datapath/bp/bbp_lru_ram_2[5][1]_i_2/O
                      net (fo=2, routed)          0.891    17.815    u_datapath/bp/bbp_lru_ram_2[5][1]_i_2_n_2
  SLICE_X46Y129                                 r  u_datapath/bp/bbp_lru_ram_2[5][0]_i_1/I1
  SLICE_X46Y129       LUT3 (Prop_lut3_I1_O)       0.150    17.965 r  u_datapath/bp/bbp_lru_ram_2[5][0]_i_1/O
                      net (fo=1, routed)          0.000    17.965    u_datapath/bp/bbp_lru_ram_2[5][0]_i_1_n_2
  SLICE_X46Y129       FDRE                                     r  u_datapath/bp/bbp_lru_ram_2_reg[5][0]/D
 -------------------------------------------------------------------    -------------------
 Below shown the delay from u_datapath/bp/bbp_id_pc_index_reg to u_datapath/bp/bbp_lru_ram_2_reg:
 Data Path Delay:        9.246ns  (logic 1.087ns (11.756%)  route 8.159ns (88.244%))

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  Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
 -------------------------------------------------------------------    -------------------
  SLICE_X51Y102       FDRE (Prop_fdre_C_Q)        0.456     9.161 f  u_datapath/bp/bbp_id_read_hit_reg/Q
                      net (fo=158, routed)        2.032    11.193    u_datapath/bp/bbp_id_read_hit
  SLICE_X56Y108                                 f  u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_13/I1
  SLICE_X56Y108       LUT2 (Prop_lut2_I1_O)       0.124    11.317 r  u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_13/O
                      net (fo=1, routed)          1.095    12.412    u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_13_n_2
  SLICE_X55Y108                                 r  u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_10/I4
  SLICE_X55Y108       LUT6 (Prop_lut6_I4_O)       0.124    12.536 r  u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_10/O
                      net (fo=34, routed)         0.702    13.238    u_datapath/bp/bbp_id_mispred_untaken
  SLICE_X54Y103                                 r  u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4/I3
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  SLICE_X54Y103       LUT4 (Prop_lut4_I3_O)       0.116    13.354 r  u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4/O
                      net (fo=34, routed)         1.159    14.513    u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4_n_2
  SLICE_X49Y94                                                   r  u_datapath/bp/bobp_id_nop_ifid_INST_0/I0
  SLICE_X49Y94        LUT2 (Prop_lut2_I0_O)       0.328    14.841 r  u_datapath/bp/bobp_id_nop_ifid_INST_0/O
                      net (fo=2, routed)          0.264    15.105    icache/uicac_bp_flush
  SLICE_X49Y94                                                   r  icache/ucac_id_reg_index[4]_i_1/I1
  SLICE_X49Y94        LUT4 (Prop_lut4_I1_O)       0.124    15.229 r  icache/ucac_id_reg_index[4]_i_1/O
                      net (fo=133, routed)        2.045    17.274    icache/ucac_id_reg_index[4]_i_1_n_2
  SLICE_X9Y88         FDRE                                       r  icache/ucac_id_reg_cpu_addr_reg[8]/R
 -------------------------------------------------------------------    -------------------
 Below shown the delay from u_datapath/bp/bbp_id_read_hit_reg/Q to icache/ucac_id_reg_cpu_addr_reg:
 Data Path Delay:        8.569ns  (logic 1.272ns (14.844%)  route 7.297ns (85.157%))

 -------------------------------------------------------------------    -------------------
  Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
 -------------------------------------------------------------------    -------------------
  SLICE_X51Y102       FDRE (Prop_fdre_C_Q)        0.456     9.161 f  u_datapath/bp/bbp_id_read_hit_reg/Q
                      net (fo=158, routed)        2.032    11.193    u_datapath/bp/bbp_id_read_hit
  SLICE_X56Y108                                                  f  u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_13/I1
  SLICE_X56Y108       LUT2 (Prop_lut2_I1_O)       0.124    11.317 r  u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_13/O
                      net (fo=1, routed)          1.095    12.412    u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_13_n_2
  SLICE_X55Y108                                                  r  u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_10/I4
  SLICE_X55Y108       LUT6 (Prop_lut6_I4_O)       0.124    12.536 r  u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_10/O
                      net (fo=34, routed)         0.702    13.238    u_datapath/bp/bbp_id_mispred_untaken
  SLICE_X54Y103                                                  r  u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4/I3
  SLICE_X54Y103       LUT4 (Prop_lut4_I3_O)       0.116    13.354 r  u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4/O
                      net (fo=34, routed)         1.159    14.513    u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4_n_2
  SLICE_X49Y94                                                   r  u_datapath/bp/bobp_id_nop_ifid_INST_0/I0
  SLICE_X49Y94        LUT2 (Prop_lut2_I0_O)       0.328    14.841 r  u_datapath/bp/bobp_id_nop_ifid_INST_0/O
                      net (fo=2, routed)          0.264    15.105    icache/uicac_bp_flush
  SLICE_X49Y94                                                   r  icache/ucac_id_reg_index[4]_i_1/I1
  SLICE_X49Y94        LUT4 (Prop_lut4_I1_O)       0.124    15.229 r  icache/ucac_id_reg_index[4]_i_1/O
                      net (fo=133, routed)        2.045    17.274    icache/ucac_id_reg_index[4]_i_1_n_2
  SLICE_X9Y88         FDRE                                       r  icache/ucac_is_reg_cpu_addr_reg[2]/R
 -------------------------------------------------------------------    -------------------
 Below shown the delay from u_datapath/bp/bbp_id_read_hit_reg/Q to icache/ucac_is_reg_cpu_addr_reg:
 Data Path Delay:        8.569ns  (logic 1.272ns (14.844%)  route 7.297ns (85.157%))

 -------------------------------------------------------------------    -------------------
  Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
 -------------------------------------------------------------------    -------------------
  SLICE_X49Y94        FDRE (Prop_fdre_C_Q)        0.456     9.174 r  u_datapath/bp/bbp_id_pc_index_reg[0]/Q
                      net (fo=392, routed)        5.123    14.298    u_datapath/bp/bbp_id_pc_index[0]
  SLICE_X44Y123                                                  r  u_datapath/bp/bbp_valid_ram_3[5]_i_2/I3
  SLICE_X44Y123       LUT4 (Prop_lut4_I3_O)       0.154    14.452 r  u_datapath/bp/bbp_valid_ram_3[5]_i_2/O
                      net (fo=8, routed)          2.376    16.828    u_datapath/bp/bbp_lru_ram_3_reg[5]
  SLICE_X46Y131                                                  r  u_datapath/bp/bbp_lru_ram_0[5][1]_i_2/I3
  SLICE_X46Y131       LUT6 (Prop_lut6_I3_O)       0.327    17.155 r  u_datapath/bp/bbp_lru_ram_0[5][1]_i_2/O
                      net (fo=2, routed)          0.463    17.618    u_datapath/bp/bbp_lru_ram_0[5][1]_i_2_n_2
  SLICE_X46Y131                                                  r  u_datapath/bp/bbp_lru_ram_0[5][0]_i_1/I3
  SLICE_X46Y131       LUT5 (Prop_lut5_I3_O)       0.124    17.742 r  u_datapath/bp/bbp_lru_ram_0[5][0]_i_1/O
                      net (fo=1, routed)          0.000    17.742    u_datapath/bp/bbp_lru_ram_0[5][0]_i_1_n_2
  SLICE_X46Y131       FDRE                                       r  u_datapath/bp/bbp_lru_ram_0_reg[5][0]/D
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 Below shown the delay from u_datapath/bp/bbp_id_pc_index_reg to u_datapath/bp/bbp_lru_ram_0_reg:
 Data Path Delay:        9.023ns  (logic 1.061ns (11.759%)  route 7.962ns (88.241%))
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  Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
 -------------------------------------------------------------------    -------------------
  SLICE_X12Y102       FDRE (Prop_fdre_C_Q)        0.518     9.237 r  u_datapath/udp_ex_alb_src_reg/Q
                      net (fo=32, routed)         1.517    10.754    u_datapath/udp_ex_alb_src
  SLICE_X28Y107                                                  r  u_datapath/b_alb_i_5/I1
  SLICE_X28Y107       LUT3 (Prop_lut3_I1_O)       0.152    10.906 r  u_datapath/b_alb_i_5/O
                      net (fo=42, routed)         1.769    12.675    u_datapath/b_alb/bialb_op_b[27]
  SLICE_X7Y100                                                   r  u_datapath/b_alb/boalb_out[23]_INST_0_i_12/I0
  SLICE_X7Y100        LUT6 (Prop_lut6_I0_O)       0.326    13.001 r  u_datapath/b_alb/boalb_out[23]_INST_0_i_12/O
                      net (fo=2, routed)          1.068    14.069    u_datapath/b_alb/boalb_out[23]_INST_0_i_12_n_2
  SLICE_X2Y98                                                    r  u_datapath/b_alb/boalb_out[21]_INST_0_i_5/I0
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    SLICE_X2Y98          LUT3 (Prop_lut3_I0_O)        0.150    14.219 r  u_datapath/b_alb/boalb_out[21]_INST_0_i_5/O
                         net (fo=2, routed)           0.847    15.066    u_datapath/b_alb/boalb_out[21]_INST_0_i_5_n_2
    SLICE_X7Y100                                                 r  u_datapath/b_alb/boalb_out[21]_INST_0_i_2/I1
    SLICE_X7Y100         LUT4 (Prop_lut4_I1_O)        0.328    15.394 r  u_datapath/b_alb/boalb_out[21]_INST_0_i_2/O
                         net (fo=1, routed)           0.642    16.036    u_datapath/b_alb/boalb_out[21]_INST_0_i_2_n_2
    SLICE_X9Y100                                                 r  u_datapath/b_alb/boalb_out[21]_INST_0/I1
    SLICE_X9Y100         LUT6 (Prop_lut6_I1_O)        0.124    16.160 r  u_datapath/b_alb/boalb_out[21]_INST_0/O
                         net (fo=3, routed)           1.114    17.274    u_datapath/addr_decoder/biad_ex_cpu_addr[21]
    SLICE_X12Y101                                                r  u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_6/I1
    SLICE_X12Y101        LUT4 (Prop_lut4_I1_O)        0.146    17.420 r  u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_6/O
                         net (fo=1, routed)           0.165    17.585    u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_6_n_2
    SLICE_X12Y101                                                r  u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_3/I4
    SLICE_X12Y101        LUT5 (Prop_lut5_I4_O)        0.328    17.913 r  u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_3/O
                         net (fo=4, routed)           0.996    18.909    u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_3_n_2
    SLICE_X10Y105                                                r  u_datapath/addr_decoder/boad_io_en[3]_INST_0/I5
    SLICE_X10Y105        LUT6 (Prop_lut6_I5_O)        0.124    19.033 r  u_datapath/addr_decoder/boad_io_en[3]_INST_0/O
                         net (fo=2, routed)           1.234    20.268    SPI_controller/uispi_wb_w_stb
    SLICE_X9Y118                                                 r  SPI_controller/TX_BUFFER16X8_i_2/I2
    SLICE_X9Y118         LUT3 (Prop_lut3_I2_O)        0.124    20.392 r  SPI_controller/TX_BUFFER16X8_i_2/O
                         net (fo=4, routed)           0.474    20.866    SPI_controller/uspi_wr_SPISR1
    SLICE_X9Y118                                                 r  SPI_controller/TX_BUFFER16X8_i_1/I4
    SLICE_X9Y118         LUT5 (Prop_lut5_I4_O)        0.124    20.990 r  SPI_controller/TX_BUFFER16X8_i_1/O
                         net (fo=11, routed)          0.809    21.799    SPI_controller/TX_BUFFER16X8/biFIFO_push
    SLICE_X9Y125                                                 r  SPI_controller/TX_BUFFER16X8/bFIFO_FIFOreg_reg_0_15_6_7_i_1/I0
    SLICE_X9Y125                                 LUT2    (Prop_lut2_I0_O)                 0.124                 21.923    r
SPI_controller/TX_BUFFER16X8/bFIFO_FIFOreg_reg_0_15_6_7_i_1/O
                         net      (fo=16,      routed)                                      0.508                 22.431
SPI_controller/TX_BUFFER16X8/bFIFO_FIFOreg_reg_0_15_0_5/WE
    SLICE_X10Y125                RAMD32                                                                                  r
SPI_controller/TX_BUFFER16X8/bFIFO_FIFOreg_reg_0_15_0_5/RAMA/WE
  ----------------------------------------------------------------------    -------------------
  Below          shown          the          delay          from          u_datapath/udp_ex_alb_src_reg/Q          to
SPI_controller/TX_BUFFER16X8/bFIFO_FIFOreg_reg_0_15_0_5/RAMA/WE:
  Data Path Delay:       13.712ns  (logic 2.568ns (18.728%)  route 11.144ns (81.272%))

  ----------------------------------------------------------------------    -------------------
  Location           Delay type              Incr(ns)  Path(ns)    Netlist Resource(s)
  ----------------------------------------------------------------------    -------------------
    SLICE_X12Y102        FDRE (Prop_fdre_C_Q)         0.518     9.237 r  u_datapath/udp_ex_alb_src_reg/Q
                         net (fo=32, routed)          1.517    10.754    u_datapath/udp_ex_alb_src
    SLICE_X28Y107                                                r  u_datapath/b_alb_i_5/I1
    SLICE_X28Y107        LUT3 (Prop_lut3_I1_O)        0.152    10.906 r  u_datapath/b_alb_i_5/O
                         net (fo=42, routed)          1.769    12.675    u_datapath/b_alb/bialb_op_b[27]
    SLICE_X7Y100                                                 r  u_datapath/b_alb/boalb_out[23]_INST_0_i_12/I0
    SLICE_X7Y100         LUT6 (Prop_lut6_I0_O)        0.326    13.001 r  u_datapath/b_alb/boalb_out[23]_INST_0_i_12/O
                         net (fo=2, routed)           1.068    14.069    u_datapath/b_alb/boalb_out[23]_INST_0_i_12_n_2
    SLICE_X2Y98                                                  r  u_datapath/b_alb/boalb_out[21]_INST_0_i_5/I0
    SLICE_X2Y98          LUT3 (Prop_lut3_I0_O)        0.150    14.219 r  u_datapath/b_alb/boalb_out[21]_INST_0_i_5/O
                         net (fo=2, routed)           0.847    15.066    u_datapath/b_alb/boalb_out[21]_INST_0_i_5_n_2
    SLICE_X7Y100                                                 r  u_datapath/b_alb/boalb_out[21]_INST_0_i_2/I1
    SLICE_X7Y100         LUT4 (Prop_lut4_I1_O)        0.328    15.394 r  u_datapath/b_alb/boalb_out[21]_INST_0_i_2/O
                         net (fo=1, routed)           0.642    16.036    u_datapath/b_alb/boalb_out[21]_INST_0_i_2_n_2
    SLICE_X9Y100                                                 r  u_datapath/b_alb/boalb_out[21]_INST_0/I1
    SLICE_X9Y100         LUT6 (Prop_lut6_I1_O)        0.124    16.160 r  u_datapath/b_alb/boalb_out[21]_INST_0/O
                         net (fo=3, routed)           1.114    17.274    u_datapath/addr_decoder/biad_ex_cpu_addr[21]
    SLICE_X12Y101                                                r  u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_6/I1
    SLICE_X12Y101        LUT4 (Prop_lut4_I1_O)        0.146    17.420 r  u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_6/O
                         net (fo=1, routed)           0.165    17.585    u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_6_n_2
    SLICE_X12Y101                                                r  u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_3/I4
    SLICE_X12Y101        LUT5 (Prop_lut5_I4_O)        0.328    17.913 r  u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_3/O
                         net (fo=4, routed)           0.996    18.909    u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_3_n_2
    SLICE_X10Y105                                                r  u_datapath/addr_decoder/boad_io_en[3]_INST_0/I5
    SLICE_X10Y105        LUT6 (Prop_lut6_I5_O)        0.124    19.033 r  u_datapath/addr_decoder/boad_io_en[3]_INST_0/O
                         net (fo=2, routed)           1.234    20.268    SPI_controller/uispi_wb_w_stb
    SLICE_X9Y118                                                 r  SPI_controller/TX_BUFFER16X8_i_2/I2
    SLICE_X9Y118         LUT3 (Prop_lut3_I2_O)        0.124    20.392 r  SPI_controller/TX_BUFFER16X8_i_2/O
                         net (fo=4, routed)           0.474    20.866    SPI_controller/uspi_wr_SPISR1
    SLICE_X9Y118                                                 r  SPI_controller/TX_BUFFER16X8_i_1/I4
    SLICE_X9Y118         LUT5 (Prop_lut5_I4_O)        0.124    20.990 r  SPI_controller/TX_BUFFER16X8_i_1/O
                         net (fo=11, routed)          0.809    21.799    SPI_controller/TX_BUFFER16X8/biFIFO_push
    SLICE_X9Y125                                                 r  SPI_controller/TX_BUFFER16X8/bFIFO_FIFOreg_reg_0_15_6_7_i_1/I0
    SLICE_X9Y125                                 LUT2    (Prop_lut2_I0_O)                 0.124                 21.923    r
SPI_controller/TX_BUFFER16X8/bFIFO_FIFOreg_reg_0_15_6_7_i_1/O
                         net      (fo=16,      routed)                                      0.508                 22.431
SPI_controller/TX_BUFFER16X8/bFIFO_FIFOreg_reg_0_15_0_5/WE
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  SLICE_X10Y125          RAMD32                                                                              r
SPI_controller/TX_BUFFER16X8/bFIFO_FIFOreg_reg_0_15_0_5/RAMA_D1/WE
 -------------------------------------------------------------------    -------------------
 Below        shown        the        delay        from        u_datapath/udp_ex_alb_src_reg/Q        to
SPI_controller/TX_BUFFER16X8/bFIFO_FIFOreg_reg_0_15_0_5/RAMA_D1/WE:
 Data Path Delay:     13.712ns  (logic 2.568ns (18.728%)  route 11.144ns (81.272%))


 -------------------------------------------------------------------    -------------------
  Location        Delay type          Incr(ns)  Path(ns)    Netlist Resource(s)
 -------------------------------------------------------------------    -------------------
  SLICE_X12Y102      FDRE (Prop_fdre_C_Q)       0.518     9.237 r  u_datapath/udp_ex_alb_src_reg/Q
                  net (fo=32, routed)        1.517    10.754    u_datapath/udp_ex_alb_src
  SLICE_X28Y107                                             r  u_datapath/b_alb_i_5/I1
  SLICE_X28Y107      LUT3 (Prop_lut3_I1_O)      0.152    10.906 r  u_datapath/b_alb_i_5/O
                  net (fo=42, routed)        1.769    12.675    u_datapath/b_alb/bialb_op_b[27]
  SLICE_X7Y100                                              r  u_datapath/b_alb/boalb_out[23]_INST_0_i_12/I0
  SLICE_X7Y100       LUT6 (Prop_lut6_I0_O)      0.326    13.001 r  u_datapath/b_alb/boalb_out[23]_INST_0_i_12/O
                  net (fo=2, routed)         1.068    14.069    u_datapath/b_alb/boalb_out[23]_INST_0_i_12_n_2
  SLICE_X2Y98                                               r  u_datapath/b_alb/boalb_out[21]_INST_0_i_5/I0
  SLICE_X2Y98        LUT3 (Prop_lut3_I0_O)      0.150    14.219 r  u_datapath/b_alb/boalb_out[21]_INST_0_i_5/O
                  net (fo=2, routed)         0.847    15.066    u_datapath/b_alb/boalb_out[21]_INST_0_i_5_n_2
  SLICE_X7Y100                                              r  u_datapath/b_alb/boalb_out[21]_INST_0_i_2/I1
  SLICE_X7Y100       LUT4 (Prop_lut4_I1_O)      0.328    15.394 r  u_datapath/b_alb/boalb_out[21]_INST_0_i_2/O
                  net (fo=1, routed)         0.642    16.036    u_datapath/b_alb/boalb_out[21]_INST_0_i_2_n_2
  SLICE_X9Y100                                              r  u_datapath/b_alb/boalb_out[21]_INST_0/I1
  SLICE_X9Y100       LUT6 (Prop_lut6_I1_O)      0.124    16.160 r  u_datapath/b_alb/boalb_out[21]_INST_0/O
                  net (fo=3, routed)         1.114    17.274    u_datapath/addr_decoder/biad_ex_cpu_addr[21]
  SLICE_X12Y101                                             r  u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_6/I1
  SLICE_X12Y101      LUT4 (Prop_lut4_I1_O)      0.146    17.420 r  u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_6/O
                  net (fo=1, routed)         0.165    17.585    u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_6_n_2
  SLICE_X12Y101                                             r  u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_3/I4
  SLICE_X12Y101      LUT5 (Prop_lut5_I4_O)      0.328    17.913 r  u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_3/O
                  net (fo=4, routed)         0.996    18.909    u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_3_n_2
  SLICE_X10Y105                                             r  u_datapath/addr_decoder/boad_io_en[3]_INST_0/I5
  SLICE_X10Y105      LUT6 (Prop_lut6_I5_O)      0.124    19.033 r  u_datapath/addr_decoder/boad_io_en[3]_INST_0/O
                  net (fo=2, routed)         1.234    20.268    SPI_controller/uispi_wb_w_stb
  SLICE_X9Y118                                              r  SPI_controller/TX_BUFFER16X8_i_2/I2
  SLICE_X9Y118       LUT3 (Prop_lut3_I2_O)      0.124    20.392 r  SPI_controller/TX_BUFFER16X8_i_2/O
                  net (fo=4, routed)         0.474    20.866    SPI_controller/uspi_wr_SPISR1
  SLICE_X9Y118                                              r  SPI_controller/TX_BUFFER16X8_i_1/I4
  SLICE_X9Y118       LUT5 (Prop_lut5_I4_O)      0.124    20.990 r  SPI_controller/TX_BUFFER16X8_i_1/O
                  net (fo=11, routed)        0.809    21.799    SPI_controller/TX_BUFFER16X8/biFIFO_push
  SLICE_X9Y125                                              r  SPI_controller/TX_BUFFER16X8/bFIFO_FIFOreg_reg_0_15_6_7_i_1/I0
  SLICE_X9Y125                              LUT2    (Prop_lut2_I0_O)                0.124          21.923    r
SPI_controller/TX_BUFFER16X8/bFIFO_FIFOreg_reg_0_15_6_7_i_1/O
                  net      (fo=16,      routed)                                     0.508                 22.431
SPI_controller/TX_BUFFER16X8/bFIFO_FIFOreg_reg_0_15_0_5/WE
  SLICE_X10Y125          RAMD32                                                                              r
SPI_controller/TX_BUFFER16X8/bFIFO_FIFOreg_reg_0_15_0_5/RAMB/WE
 -------------------------------------------------------------------    -------------------
 Below        shown        the        delay        from        u_datapath/udp_ex_alb_src_reg/Q        to
SPI_controller/TX_BUFFER16X8/bFIFO_FIFOreg_reg_0_15_0_5/RAMB/WE:
 Data Path Delay:     13.712ns  (logic 2.568ns (18.728%)  route 11.144ns (81.272%))


 -------------------------------------------------------------------    -------------------
  Location        Delay type          Incr(ns)  Path(ns)    Netlist Resource(s)
 -------------------------------------------------------------------    -------------------
  SLICE_X12Y102      FDRE (Prop_fdre_C_Q)       0.518     9.237 r  u_datapath/udp_ex_alb_src_reg/Q
                  net (fo=32, routed)        1.517    10.754    u_datapath/udp_ex_alb_src
  SLICE_X28Y107                                             r  u_datapath/b_alb_i_5/I1
  SLICE_X28Y107      LUT3 (Prop_lut3_I1_O)      0.152    10.906 r  u_datapath/b_alb_i_5/O
                  net (fo=42, routed)        1.769    12.675    u_datapath/b_alb/bialb_op_b[27]
  SLICE_X7Y100                                              r  u_datapath/b_alb/boalb_out[23]_INST_0_i_12/I0
  SLICE_X7Y100       LUT6 (Prop_lut6_I0_O)      0.326    13.001 r  u_datapath/b_alb/boalb_out[23]_INST_0_i_12/O
                  net (fo=2, routed)         1.068    14.069    u_datapath/b_alb/boalb_out[23]_INST_0_i_12_n_2
  SLICE_X2Y98                                               r  u_datapath/b_alb/boalb_out[21]_INST_0_i_5/I0
  SLICE_X2Y98        LUT3 (Prop_lut3_I0_O)      0.150    14.219 r  u_datapath/b_alb/boalb_out[21]_INST_0_i_5/O
                  net (fo=2, routed)         0.847    15.066    u_datapath/b_alb/boalb_out[21]_INST_0_i_5_n_2
  SLICE_X7Y100                                              r  u_datapath/b_alb/boalb_out[21]_INST_0_i_2/I1
  SLICE_X7Y100       LUT4 (Prop_lut4_I1_O)      0.328    15.394 r  u_datapath/b_alb/boalb_out[21]_INST_0_i_2/O
                  net (fo=1, routed)         0.642    16.036    u_datapath/b_alb/boalb_out[21]_INST_0_i_2_n_2
  SLICE_X9Y100                                              r  u_datapath/b_alb/boalb_out[21]_INST_0/I1
  SLICE_X9Y100       LUT6 (Prop_lut6_I1_O)      0.124    16.160 r  u_datapath/b_alb/boalb_out[21]_INST_0/O
                  net (fo=3, routed)         1.114    17.274    u_datapath/addr_decoder/biad_ex_cpu_addr[21]
  SLICE_X12Y101                                             r  u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_6/I1
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SLICE_X12Y101      LUT4 (Prop_lut4_I1_O)      0.146   17.420 r u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_6/O
                   net (fo=1, routed)          0.165   17.585    u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_6_n_2
SLICE_X12Y101                                                  r u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_3/I4
SLICE_X12Y101      LUT5 (Prop_lut5_I4_O)      0.328   17.913 r u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_3/O
                   net (fo=4, routed)          0.996   18.909    u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_3_n_2
SLICE_X10Y105                                                  r u_datapath/addr_decoder/boad_io_en[3]_INST_0/I5
SLICE_X10Y105      LUT6 (Prop_lut6_I5_O)      0.124   19.033 r u_datapath/addr_decoder/boad_io_en[3]_INST_0/O
                   net (fo=2, routed)          1.234   20.268    SPI_controller/uispi_wb_w_stb
SLICE_X9Y118                                                   r SPI_controller/TX_BUFFER16X8_i_2/I2
SLICE_X9Y118       LUT3 (Prop_lut3_I2_O)      0.124   20.392 r SPI_controller/TX_BUFFER16X8_i_2/O
                   net (fo=4, routed)          0.474   20.866    SPI_controller/uspi_wr_SPISR1
SLICE_X9Y118                                                   r SPI_controller/TX_BUFFER16X8_i_1/I4
SLICE_X9Y118       LUT5 (Prop_lut5_I4_O)      0.124   20.990 r SPI_controller/TX_BUFFER16X8_i_1/O
                   net (fo=11, routed)         0.809   21.799    SPI_controller/TX_BUFFER16X8/biFIFO_push
SLICE_X9Y125                                                   r SPI_controller/TX_BUFFER16X8/bFIFO_FIFOreg_reg_0_15_6_7_i_1/I0
SLICE_X9Y125       LUT2    (Prop_lut2_I0_O)   0.124   21.923 r SPI_controller/TX_BUFFER16X8/bFIFO_FIFOreg_reg_0_15_6_7_i_1/O
                   net    (fo=16,    routed)   0.508   22.431    SPI_controller/TX_BUFFER16X8/bFIFO_FIFOreg_reg_0_15_0_5/WE
SLICE_X10Y125      RAMD32                                      r SPI_controller/TX_BUFFER16X8/bFIFO_FIFOreg_reg_0_15_0_5/RAMB_D1/WE
-------------------------------------------------------------------    -------------------
Below shown the delay from u_datapath/udp_ex_alb_src_reg/Q to SPI_controller/TX_BUFFER16X8/bFIFO_FIFOreg_reg_0_15_0_5/RAMB_D1/WE:
Data Path Delay:        13.712ns  (logic 2.568ns (18.728%)  route 11.144ns (81.272%))


-------------------------------------------------------------------    -------------------
Location           Delay type            Incr(ns)  Path(ns)    Netlist Resource(s)
-------------------------------------------------------------------    -------------------
SLICE_X12Y102      FDRE (Prop_fdre_C_Q)       0.518    9.237 r u_datapath/udp_ex_alb_src_reg/Q
                   net (fo=32, routed)         1.517   10.754    u_datapath/udp_ex_alb_src
SLICE_X28Y107                                                  r u_datapath/b_alb_i_5/I1
SLICE_X28Y107      LUT3 (Prop_lut3_I1_O)      0.152   10.906 r u_datapath/b_alb_i_5/O
                   net (fo=42, routed)         1.769   12.675    u_datapath/b_alb/bialb_op_b[27]
SLICE_X7Y100                                                   r u_datapath/b_alb/boalb_out[23]_INST_0_i_12/I0
SLICE_X7Y100       LUT6 (Prop_lut6_I0_O)      0.326   13.001 r u_datapath/b_alb/boalb_out[23]_INST_0_i_12/O
                   net (fo=2, routed)          1.068   14.069    u_datapath/b_alb/boalb_out[23]_INST_0_i_12_n_2
SLICE_X2Y98                                                    r u_datapath/b_alb/boalb_out[21]_INST_0_i_5/I0
SLICE_X2Y98        LUT3 (Prop_lut3_I0_O)      0.150   14.219 r u_datapath/b_alb/boalb_out[21]_INST_0_i_5/O
                   net (fo=2, routed)          0.847   15.066    u_datapath/b_alb/boalb_out[21]_INST_0_i_5_n_2
SLICE_X7Y100                                                   r u_datapath/b_alb/boalb_out[21]_INST_0_i_2/I1
SLICE_X7Y100       LUT4 (Prop_lut4_I1_O)      0.328   15.394 r u_datapath/b_alb/boalb_out[21]_INST_0_i_2/O
                   net (fo=1, routed)          0.642   16.036    u_datapath/b_alb/boalb_out[21]_INST_0_i_2_n_2
SLICE_X9Y100                                                   r u_datapath/b_alb/boalb_out[21]_INST_0/I1
SLICE_X9Y100       LUT6 (Prop_lut6_I1_O)      0.124   16.160 r u_datapath/b_alb/boalb_out[21]_INST_0/O
                   net (fo=3, routed)          1.114   17.274    u_datapath/addr_decoder/biad_ex_cpu_addr[21]
SLICE_X12Y101                                                  r u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_6/I1
SLICE_X12Y101      LUT4 (Prop_lut4_I1_O)      0.146   17.420 r u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_6/O
                   net (fo=1, routed)          0.165   17.585    u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_6_n_2
SLICE_X12Y101                                                  r u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_3/I4
SLICE_X12Y101      LUT5 (Prop_lut5_I4_O)      0.328   17.913 r u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_3/O
                   net (fo=4, routed)          0.996   18.909    u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_3_n_2
SLICE_X10Y105                                                  r u_datapath/addr_decoder/boad_io_en[3]_INST_0/I5
SLICE_X10Y105      LUT6 (Prop_lut6_I5_O)      0.124   19.033 r u_datapath/addr_decoder/boad_io_en[3]_INST_0/O
                   net (fo=2, routed)          1.234   20.268    SPI_controller/uispi_wb_w_stb
SLICE_X9Y118                                                   r SPI_controller/TX_BUFFER16X8_i_2/I2
SLICE_X9Y118       LUT3 (Prop_lut3_I2_O)      0.124   20.392 r SPI_controller/TX_BUFFER16X8_i_2/O
                   net (fo=4, routed)          0.474   20.866    SPI_controller/uspi_wr_SPISR1
SLICE_X9Y118                                                   r SPI_controller/TX_BUFFER16X8_i_1/I4
SLICE_X9Y118       LUT5 (Prop_lut5_I4_O)      0.124   20.990 r SPI_controller/TX_BUFFER16X8_i_1/O
                   net (fo=11, routed)         0.809   21.799    SPI_controller/TX_BUFFER16X8/biFIFO_push
SLICE_X9Y125                                                   r SPI_controller/TX_BUFFER16X8/bFIFO_FIFOreg_reg_0_15_6_7_i_1/I0
SLICE_X9Y125       LUT2    (Prop_lut2_I0_O)   0.124   21.923 r SPI_controller/TX_BUFFER16X8/bFIFO_FIFOreg_reg_0_15_6_7_i_1/O
                   net    (fo=16,    routed)   0.508   22.431    SPI_controller/TX_BUFFER16X8/bFIFO_FIFOreg_reg_0_15_0_5/WE
SLICE_X10Y125      RAMD32                                      r SPI_controller/TX_BUFFER16X8/bFIFO_FIFOreg_reg_0_15_0_5/RAMC/WE
-------------------------------------------------------------------    -------------------
Below shown the delay from u_datapath/udp_ex_alb_src_reg/Q to SPI_controller/TX_BUFFER16X8/bFIFO_FIFOreg_reg_0_15_0_5/RAMC/WE:
Data Path Delay:        13.712ns  (logic 2.568ns (18.728%)  route 11.144ns (81.272%))
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  -------------------------------------------------------------------    -------------------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
    SLICE_X34Y93         FDRE (Prop_fdre_C_Q)         0.518     9.242 r  u_datapath/udp_mem_alb_out_reg[5]/Q
                         net (fo=47, routed)          1.101    10.344    dcache/ucac_tag_ram_reg_0_3_14_14/A0
    SLICE_X38Y94                                                      r  dcache/ucac_tag_ram_reg_0_3_14_14/SP/ADR0
    SLICE_X38Y94         RAMS32 (Prop_rams32_ADR0_O)
                                                      0.251    10.595 r  dcache/ucac_tag_ram_reg_0_3_14_14/SP/O
                         net (fo=5, routed)           1.269    11.864    dcache/bififo_data0[14]
    SLICE_X35Y90                                                      r  dcache/uocac_cpu_stall_INST_0_i_12/I0
    SLICE_X35Y90         LUT6 (Prop_lut6_I0_O)        0.124    11.988 r  dcache/uocac_cpu_stall_INST_0_i_12/O
                         net (fo=1, routed)           0.000    11.988    dcache/uocac_cpu_stall_INST_0_i_12_n_2
    SLICE_X35Y90                                                      r  dcache/uocac_cpu_stall_INST_0_i_6/S[0]
    SLICE_X35Y90         CARRY4 (Prop_carry4_S[0]_CO[3])
                                                      0.532    12.520 r  dcache/uocac_cpu_stall_INST_0_i_6/CO[3]
                         net (fo=1, routed)           0.000    12.520    dcache/uocac_cpu_stall_INST_0_i_6_n_2
    SLICE_X35Y91                                                      r  dcache/uocac_cpu_stall_INST_0_i_1/CI
    SLICE_X35Y91         CARRY4 (Prop_carry4_CI_CO[0])
                                                      0.271    12.791 r  dcache/uocac_cpu_stall_INST_0_i_1/CO[0]
                         net (fo=3, routed)           0.905    13.696    dcache/ucac_hit1
    SLICE_X11Y92                                                      r  dcache/b_cache_ctrl_i_2/I0
    SLICE_X11Y92         LUT5 (Prop_lut5_I0_O)        0.373    14.069 r  dcache/b_cache_ctrl_i_2/O
                         net (fo=19, routed)          0.590    14.658    dcache/b_cache_ctrl/bicac_ctrl_hit
    SLICE_X9Y90                                                       r  dcache/b_cache_ctrl/bocac_ctrl_cpu_data_output_en_INST_0/I1
    SLICE_X9Y90          LUT4 (Prop_lut4_I1_O)        0.119    14.777 r
dcache/b_cache_ctrl/bocac_ctrl_cpu_data_output_en_INST_0/O
                         net (fo=2, routed)           0.706    15.483    dcache/cache_cell/bicr_cpu_data_output_en
    SLICE_X9Y96                                                       r  dcache/cache_cell/enz_31_INST_0/I0
    SLICE_X9Y96          LUT4 (Prop_lut4_I0_O)        0.332    15.815 r  dcache/cache_cell/enz_31_INST_0/O
                         net (fo=64, routed)          0.923    16.738    dcache_n_151
    SLICE_X6Y107                                                      r  u_datapath_i_154/I1
    SLICE_X6Y107         LUT6 (Prop_lut6_I1_O)        0.124    16.862 r  u_datapath_i_154/O
                         net (fo=1, routed)           0.571    17.433    u_datapath_i_154_n_2
    SLICE_X6Y110                                                      r  u_datapath_i_89/I1
    SLICE_X6Y110         LUT2 (Prop_lut2_I1_O)        0.124    17.557 r  u_datapath_i_89/O
                         net (fo=1, routed)           1.176    18.732    u_datapath_i_89_n_2
    SLICE_X11Y112                                                     r  u_datapath_i_12/I0
    SLICE_X11Y112        LUT2 (Prop_lut2_I0_O)        0.124    18.856 r  u_datapath_i_12/O
                         net (fo=4, routed)           0.829    19.685    u_datapath/uidp_mdata[20]
    SLICE_X12Y113                                                     r  u_datapath/uodp_ex_dm_store[20]_INST_0_i_4/I1
    SLICE_X12Y113        LUT6 (Prop_lut6_I1_O)        0.124    19.809 f  u_datapath/uodp_ex_dm_store[20]_INST_0_i_4/O
                         net (fo=1, routed)           0.171    19.980    u_datapath/uodp_ex_dm_store[20]_INST_0_i_4_n_2
    SLICE_X12Y113                                                     f  u_datapath/uodp_ex_dm_store[20]_INST_0_i_3/I0
    SLICE_X12Y113        LUT3 (Prop_lut3_I0_O)        0.124    20.104 r  u_datapath/uodp_ex_dm_store[20]_INST_0_i_3/O
                         net (fo=1, routed)           0.641    20.746    u_datapath/uodp_ex_dm_store[20]_INST_0_i_3_n_2
    SLICE_X12Y113                                                     r  u_datapath/uodp_ex_dm_store[20]_INST_0_i_2/I3
    SLICE_X12Y113        LUT6 (Prop_lut6_I3_O)        0.124    20.870 r  u_datapath/uodp_ex_dm_store[20]_INST_0_i_2/O
                         net (fo=4, routed)           0.839    21.709    u_datapath/uodp_ex_dm_store[20]_INST_0_i_2_n_2
    SLICE_X14Y106                                                     r  u_datapath/uodp_ex_dm_store[20]_INST_0_i_1/I0
    SLICE_X14Y106        LUT3 (Prop_lut3_I0_O)        0.124    21.833 r  u_datapath/uodp_ex_dm_store[20]_INST_0_i_1/O
                         net (fo=4, routed)           0.697    22.530    u_datapath/udp_fw_data_ex_rt32[20]
    SLICE_X11Y108                                                     r  u_datapath/uodp_ex_dm_store[12]_INST_0/I2
    SLICE_X11Y108        LUT6 (Prop_lut6_I2_O)        0.124    22.654 r  u_datapath/uodp_ex_dm_store[12]_INST_0/O
                         net (fo=8, routed)           1.299    23.953    data_ram/uiram_wb_din[12]
    SLICE_X6Y103                                                      r  data_ram/uram_array_reg_0_i_23/I0
    SLICE_X6Y103         LUT3 (Prop_lut3_I0_O)        0.146    24.099 r  data_ram/uram_array_reg_0_i_23/O
                         net (fo=1, routed)           0.469    24.568    data_ram/uram_array_reg_0_i_23_n_2
    SLICE_X6Y103                                                      r  data_ram/uram_array_reg_0_i_13/I4
    SLICE_X6Y103         LUT5 (Prop_lut5_I4_O)        0.328    24.896 r  data_ram/uram_array_reg_0_i_13/O
                         net (fo=1, routed)           0.673    25.569    data_ram/p_1_in[4]
    RAMB36_X0Y20         RAMB36E1                                     r  data_ram/uram_array_reg_0/DIADI[4]
  -------------------------------------------------------------------    -------------------
  Below shown the delay from u_datapath/udp_mem_alb_out_reg to data_ram/uram_array_reg_0/DIADI:
  Data Path Delay:        16.844ns  (logic 3.986ns (23.663%)  route 12.858ns (76.337%))


  -------------------------------------------------------------------    -------------------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
    SLICE_X34Y93         FDRE (Prop_fdre_C_Q)         0.518     9.242 r  u_datapath/udp_mem_alb_out_reg[5]/Q
                         net (fo=47, routed)          1.101    10.344    dcache/ucac_tag_ram_reg_0_3_14_14/A0
    SLICE_X38Y94                                                      r  dcache/ucac_tag_ram_reg_0_3_14_14/SP/ADR0
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    SLICE_X38Y94         RAMS32 (Prop_rams32_ADR0_O)
                                 0.251    10.595 r  dcache/ucac_tag_ram_reg_0_3_14_14/SP/O
                 net (fo=5, routed)           1.269    11.864    dcache/bififo_data0[14]
    SLICE_X35Y90                                       r  dcache/uocac_cpu_stall_INST_0_i_12/I0
    SLICE_X35Y90         LUT6 (Prop_lut6_I0_O)        0.124    11.988 r  dcache/uocac_cpu_stall_INST_0_i_12/O
                 net (fo=1, routed)           0.000    11.988    dcache/uocac_cpu_stall_INST_0_i_12_n_2
    SLICE_X35Y90                                       r  dcache/uocac_cpu_stall_INST_0_i_6/S[0]
    SLICE_X35Y90         CARRY4 (Prop_carry4_S[0]_CO[3])
                                 0.532    12.520 r  dcache/uocac_cpu_stall_INST_0_i_6/CO[3]
                 net (fo=1, routed)           0.000    12.520    dcache/uocac_cpu_stall_INST_0_i_6_n_2
    SLICE_X35Y91                                       r  dcache/uocac_cpu_stall_INST_0_i_1/CI
    SLICE_X35Y91         CARRY4 (Prop_carry4_CI_CO[0])
                                 0.271    12.791 r  dcache/uocac_cpu_stall_INST_0_i_1/CO[0]
                 net (fo=3, routed)           0.905    13.696    dcache/ucac_hit1
    SLICE_X11Y92                                       r  dcache/b_cache_ctrl_i_2/I0
    SLICE_X11Y92         LUT5 (Prop_lut5_I0_O)        0.373    14.069 r  dcache/b_cache_ctrl_i_2/O
                 net (fo=19, routed)          0.590    14.658    dcache/b_cache_ctrl/bicac_ctrl_hit
    SLICE_X9Y90                                        r  dcache/b_cache_ctrl/bocac_ctrl_cpu_data_output_en_INST_0/I1
    SLICE_X9Y90                                  LUT4    (Prop_lut4_I1_O)                 0.119                 14.777     r
dcache/b_cache_ctrl/bocac_ctrl_cpu_data_output_en_INST_0/O
                 net (fo=2, routed)           0.706    15.483    dcache/cache_cell/bicr_cpu_data_output_en
    SLICE_X9Y96                                        r  dcache/cache_cell/enz_31_INST_0/I0
    SLICE_X9Y96          LUT4 (Prop_lut4_I0_O)        0.332    15.815 r  dcache/cache_cell/enz_31_INST_0/O
                 net (fo=64, routed)          1.271    17.085    dcache_n_143
    SLICE_X4Y109                                       r  u_datapath_i_138/I1
    SLICE_X4Y109         LUT6 (Prop_lut6_I1_O)        0.124    17.209 r  u_datapath_i_138/O
                 net (fo=1, routed)           0.563    17.773    u_datapath_i_138_n_2
    SLICE_X4Y112                                       r  u_datapath_i_73/I1
    SLICE_X4Y112         LUT2 (Prop_lut2_I1_O)        0.124    17.897 r  u_datapath_i_73/O
                 net (fo=1, routed)           0.838    18.735    u_datapath_i_73_n_2
    SLICE_X10Y112                                      r  u_datapath_i_4/I0
    SLICE_X10Y112        LUT2 (Prop_lut2_I0_O)        0.124    18.859 r  u_datapath_i_4/O
                 net (fo=5, routed)           0.626    19.484    u_datapath/uidp_mdata[28]
    SLICE_X12Y112                                      r  u_datapath/uodp_ex_dm_store[4]_INST_0_i_4/I5
    SLICE_X12Y112        LUT6 (Prop_lut6_I5_O)        0.124    19.608 f  u_datapath/uodp_ex_dm_store[4]_INST_0_i_4/O
                 net (fo=2, routed)           0.492    20.101    u_datapath/uodp_ex_dm_store[4]_INST_0_i_4_n_2
    SLICE_X13Y112                                      f  u_datapath/uodp_ex_dm_store[28]_INST_0_i_3/I0
    SLICE_X13Y112        LUT6 (Prop_lut6_I0_O)        0.124    20.225 r  u_datapath/uodp_ex_dm_store[28]_INST_0_i_3/O
                 net (fo=1, routed)           0.433    20.658    u_datapath/uodp_ex_dm_store[28]_INST_0_i_3_n_2
    SLICE_X13Y112                                      r  u_datapath/uodp_ex_dm_store[28]_INST_0_i_2/I3
    SLICE_X13Y112        LUT6 (Prop_lut6_I3_O)        0.124    20.782 r  u_datapath/uodp_ex_dm_store[28]_INST_0_i_2/O
                 net (fo=5, routed)           0.907    21.689    u_datapath/uodp_ex_dm_store[28]_INST_0_i_2_n_2
    SLICE_X14Y108                                      r  u_datapath/uodp_ex_dm_store[28]_INST_0_i_1/I0
    SLICE_X14Y108        LUT3 (Prop_lut3_I0_O)        0.150    21.839 r  u_datapath/uodp_ex_dm_store[28]_INST_0_i_1/O
                 net (fo=3, routed)           0.777    22.615    u_datapath/udp_fw_data_ex_rt32[28]
    SLICE_X8Y110                                       r  u_datapath/uodp_ex_dm_store[20]_INST_0/I5
    SLICE_X8Y110         LUT6 (Prop_lut6_I5_O)        0.328    22.943 r  u_datapath/uodp_ex_dm_store[20]_INST_0/O
                 net (fo=7, routed)           1.039    23.982    dcache/uicac_cpu_data[20]
    SLICE_X4Y96                                        r  dcache/cache_cell_i_12/I4
    SLICE_X4Y96          LUT5 (Prop_lut5_I4_O)        0.124    24.106 r  dcache/cache_cell_i_12/O
                 net (fo=1, routed)           0.766    24.872    dcache/cache_cell/bicr_din[20]
    SLICE_X7Y96                                        r  dcache/cache_cell/bcr_array_reg_i_5/I0
    SLICE_X7Y96          LUT3 (Prop_lut3_I0_O)        0.150    25.022 r  dcache/cache_cell/bcr_array_reg_i_5/O
                 net (fo=1, routed)           0.395    25.418    dcache/cache_cell/bcr_array_reg_i_5_n_2
    RAMB18_X0Y38         RAMB18E1                                r  dcache/cache_cell/bcr_array_reg/DIADI[12]
  ------------------------------------------------------------------    -------------------
  Below shown the delay from u_datapath/udp_mem_alb_out_reg to dcache/cache_cell/bcr_array_reg/DIADI:
  Data Path Delay:        16.693ns  (logic 4.016ns (24.057%)  route 12.677ns (75.943%))

  ------------------------------------------------------------------    -------------------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  ------------------------------------------------------------------    -------------------
    SLICE_X34Y93         FDRE (Prop_fdre_C_Q)         0.518     9.242 r  u_datapath/udp_mem_alb_out_reg[5]/Q
                 net (fo=47, routed)          1.101    10.344    dcache/ucac_tag_ram_reg_0_3_14_14/A0
    SLICE_X38Y94                                       r  dcache/ucac_tag_ram_reg_0_3_14_14/SP/ADR0
    SLICE_X38Y94         RAMS32 (Prop_rams32_ADR0_O)
                                 0.251    10.595 r  dcache/ucac_tag_ram_reg_0_3_14_14/SP/O
                 net (fo=5, routed)           1.269    11.864    dcache/bififo_data0[14]
    SLICE_X35Y90                                       r  dcache/uocac_cpu_stall_INST_0_i_12/I0
    SLICE_X35Y90         LUT6 (Prop_lut6_I0_O)        0.124    11.988 r  dcache/uocac_cpu_stall_INST_0_i_12/O
                 net (fo=1, routed)           0.000    11.988    dcache/uocac_cpu_stall_INST_0_i_12_n_2
    SLICE_X35Y90                                       r  dcache/uocac_cpu_stall_INST_0_i_6/S[0]
    SLICE_X35Y90         CARRY4 (Prop_carry4_S[0]_CO[3])
                                 0.532    12.520 r  dcache/uocac_cpu_stall_INST_0_i_6/CO[3]
                 net (fo=1, routed)           0.000    12.520    dcache/uocac_cpu_stall_INST_0_i_6_n_2
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   SLICE_X35Y91                                          r  dcache/uocac_cpu_stall_INST_0_i_1/CI
   SLICE_X35Y91         CARRY4 (Prop_carry4_CI_CO[0])
                                          0.271    12.791 r  dcache/uocac_cpu_stall_INST_0_i_1/CO[0]
                   net (fo=3, routed)          0.905    13.696    dcache/ucac_hit1
   SLICE_X11Y92                                          r  dcache/b_cache_ctrl_i_2/I0
   SLICE_X11Y92         LUT5 (Prop_lut5_I0_O)       0.373    14.069 r  dcache/b_cache_ctrl_i_2/O
                   net (fo=19, routed)         0.590    14.658    dcache/b_cache_ctrl/bicac_ctrl_hit
   SLICE_X9Y90                                          r  dcache/b_cache_ctrl/bocac_ctrl_cpu_data_output_en_INST_0/I1
   SLICE_X9Y90                                    LUT4     (Prop_lut4_I1_O)                              0.119                  14.777     r
dcache/b_cache_ctrl/bocac_ctrl_cpu_data_output_en_INST_0/O
                   net (fo=2, routed)          0.706    15.483    dcache/cache_cell/bicr_cpu_data_output_en
   SLICE_X9Y96                                          r  dcache/cache_cell/enz_31_INST_0/I0
   SLICE_X9Y96         LUT4 (Prop_lut4_I0_O)       0.332    15.815 r  dcache/cache_cell/enz_31_INST_0/O
                   net (fo=64, routed)         1.271    17.085    dcache_n_143
   SLICE_X4Y109                                          r  u_datapath_i_138/I1
   SLICE_X4Y109         LUT6 (Prop_lut6_I1_O)       0.124    17.209 r  u_datapath_i_138/O
                   net (fo=1, routed)          0.563    17.773    u_datapath_i_138_n_2
   SLICE_X4Y112                                          r  u_datapath_i_73/I1
   SLICE_X4Y112         LUT2 (Prop_lut2_I1_O)       0.124    17.897 r  u_datapath_i_73/O
                   net (fo=1, routed)          0.838    18.735    u_datapath_i_73_n_2
   SLICE_X10Y112                                          r  u_datapath_i_4/I0
   SLICE_X10Y112        LUT2 (Prop_lut2_I0_O)       0.124    18.859 r  u_datapath_i_4/O
                   net (fo=5, routed)          0.626    19.484    u_datapath/uidp_mdata[28]
   SLICE_X12Y112                                          r  u_datapath/uodp_ex_dm_store[4]_INST_0_i_4/I5
   SLICE_X12Y112        LUT6 (Prop_lut6_I5_O)       0.124    19.608 f  u_datapath/uodp_ex_dm_store[4]_INST_0_i_4/O
                   net (fo=2, routed)          0.492    20.101    u_datapath/uodp_ex_dm_store[4]_INST_0_i_4_n_2
   SLICE_X13Y112                                          f  u_datapath/uodp_ex_dm_store[28]_INST_0_i_3/I0
   SLICE_X13Y112        LUT6 (Prop_lut6_I0_O)       0.124    20.225 r  u_datapath/uodp_ex_dm_store[28]_INST_0_i_3/O
                   net (fo=1, routed)          0.433    20.658    u_datapath/uodp_ex_dm_store[28]_INST_0_i_3_n_2
   SLICE_X13Y112                                          r  u_datapath/uodp_ex_dm_store[28]_INST_0_i_2/I3
   SLICE_X13Y112        LUT6 (Prop_lut6_I3_O)       0.124    20.782 r  u_datapath/uodp_ex_dm_store[28]_INST_0_i_2/O
                   net (fo=5, routed)          0.790    21.571    u_datapath/uodp_ex_dm_store[28]_INST_0_i_2_n_2
   SLICE_X14Y108                                          r  u_datapath/uodp_ex_dm_store[12]_INST_0_i_1/I0
   SLICE_X14Y108        LUT6 (Prop_lut6_I0_O)       0.124    21.695 r  u_datapath/uodp_ex_dm_store[12]_INST_0_i_1/O
                   net (fo=2, routed)          0.584    22.280    u_datapath/uodp_ex_dm_store[12]_INST_0_i_1_n_2
   SLICE_X12Y106                                          r  u_datapath/uodp_ex_dm_store[4]_INST_0/I5
   SLICE_X12Y106        LUT6 (Prop_lut6_I5_O)       0.124    22.404 r  u_datapath/uodp_ex_dm_store[4]_INST_0/O
                   net (fo=18, routed)         0.971    23.374    dcache/uicac_cpu_data[4]
   SLICE_X7Y97                                          r  dcache/cache_cell_i_28/I4
   SLICE_X7Y97          LUT5 (Prop_lut5_I4_O)       0.124    23.498 r  dcache/cache_cell_i_28/O
                   net (fo=4, routed)          1.010    24.508    dcache/cache_cell/bicr_din[4]
   SLICE_X7Y96                                          r  dcache/cache_cell/bcr_array_reg_i_21/I2
   SLICE_X7Y96          LUT3 (Prop_lut3_I2_O)       0.152    24.660 r  dcache/cache_cell/bcr_array_reg_i_21/O
                   net (fo=1, routed)          0.540    25.200    dcache/cache_cell/bcr_array_reg_i_21_n_2
   RAMB18_X0Y38         RAMB18E1                                r  dcache/cache_cell/bcr_array_reg/DIBDI[4]
  -------------------------------------------------------------------    -------------------
  Below shown the delay from u_datapath/udp_mem_alb_out_reg to dcache/cache_cell/bcr_array_reg/DIBDI:
  Data Path Delay:        16.475ns  (logic 3.788ns (22.992%)  route 12.687ns (77.008%))
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  -------------------------------------------------------------------    -------------------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
    SLICE_X34Y94         FDRE (Prop_fdre_C_Q)        0.518     9.242 r  u_datapath/udp_wb_rf_wr_reg/Q
                   net (fo=98, routed)         3.170    12.412    u_datapath/b_rf/brf_reg_ram_reg_r2_0_31_18_23/WE
    SLICE_X34Y116        RAMD32                                 r  u_datapath/b_rf/brf_reg_ram_reg_r2_0_31_18_23/RAMA/WE
  -------------------------------------------------------------------    -------------------
  Below shown the delay from u_datapath/udp_wb_rf_wr_reg/Q to
u_datapath/b_rf/brf_reg_ram_reg_r2_0_31_18_23/RAMA/WE:
  Data Path Delay:        3.688ns  (logic 0.518ns (14.047%)  route 3.170ns (85.953%))


  -------------------------------------------------------------------    -------------------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
    SLICE_X34Y94         FDRE (Prop_fdre_C_Q)        0.518     9.242 r  u_datapath/udp_wb_rf_wr_reg/Q
                   net (fo=98, routed)         3.170    12.412    u_datapath/b_rf/brf_reg_ram_reg_r2_0_31_18_23/WE
    SLICE_X34Y116        RAMD32                              r  u_datapath/b_rf/brf_reg_ram_reg_r2_0_31_18_23/RAMA_D1/WE
  -------------------------------------------------------------------    -------------------
  Below shown the delay from u_datapath/udp_wb_rf_wr_reg/Q to
u_datapath/b_rf/brf_reg_ram_reg_r2_0_31_18_23/RAMA_D1/WE:
```

```
  Data Path Delay:       3.688ns  (logic 0.518ns (14.047%)  route 3.170ns (85.953%))

  ----------------------------------------------------------------------------    -------------------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  ----------------------------------------------------------------------------    -------------------
    SLICE_X34Y94         FDRE (Prop_fdre_C_Q)         0.518     9.242 r  u_datapath/udp_wb_rf_wr_reg/Q
                         net (fo=98, routed)          3.170    12.412    u_datapath/b_rf/brf_reg_ram_reg_r2_0_31_18_23/WE
    SLICE_X34Y116        RAMD32                                         r  u_datapath/b_rf/brf_reg_ram_reg_r2_0_31_18_23/RAMB/WE
  ----------------------------------------------------------------------------    -------------------
  Below shown the delay from u_datapath/udp_wb_rf_wr_reg/Q to
u_datapath/b_rf/brf_reg_ram_reg_r2_0_31_18_23/RAMB/WE:
  Data Path Delay:       3.688ns  (logic 0.518ns (14.047%)  route 3.170ns (85.953%))

  ----------------------------------------------------------------------------    -------------------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  ----------------------------------------------------------------------------    -------------------
    SLICE_X34Y94         FDRE (Prop_fdre_C_Q)         0.518     9.242 r  u_datapath/udp_wb_rf_wr_reg/Q
                         net (fo=98, routed)          3.170    12.412    u_datapath/b_rf/brf_reg_ram_reg_r2_0_31_18_23/WE
    SLICE_X34Y116        RAMD32                                         r  u_datapath/b_rf/brf_reg_ram_reg_r2_0_31_18_23/RAMB_D1/WE
  ----------------------------------------------------------------------------    -------------------
  Below shown the delay from u_datapath/udp_wb_rf_wr_reg/Q to
u_datapath/b_rf/brf_reg_ram_reg_r2_0_31_18_23/RAMB_D1/WE:
  Data Path Delay:       3.688ns  (logic 0.518ns (14.047%)  route 3.170ns (85.953%))

  ----------------------------------------------------------------------------    -------------------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  ----------------------------------------------------------------------------    -------------------
    SLICE_X34Y94         FDRE (Prop_fdre_C_Q)         0.518     9.242 r  u_datapath/udp_wb_rf_wr_reg/Q
                         net (fo=98, routed)          3.170    12.412    u_datapath/b_rf/brf_reg_ram_reg_r2_0_31_18_23/WE
    SLICE_X34Y116        RAMD32                                         r  u_datapath/b_rf/brf_reg_ram_reg_r2_0_31_18_23/RAMC/WE
  ----------------------------------------------------------------------------    -------------------
  Below shown the delay from u_datapath/udp_wb_rf_wr_reg/Q to
u_datapath/b_rf/brf_reg_ram_reg_r2_0_31_18_23/RAMC/WE:
  Data Path Delay:       3.688ns  (logic 0.518ns (14.047%)  route 3.170ns (85.953%))
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
```

Appendix C: Timing Delay TCL Script Code

```
set myinfile "C:/Users/Asus/Desktop/timing_delay/6stages.out"
set myoutfile "C:/Users/Asus/Desktop/timing_delay/6stages_less_detail.out"
set stagePathNum 5
set maxPathsGet 100000000

set_param general.maxThreads 8

set paths [get_timing_paths -delay_type max -from [get_cells u_datapath/*dp_if*] -
max_paths $maxPathsGet]
report_timing -of_object $paths -file $myinfile

set in_fh [open $myinfile]
set lines [split [read $in_fh] "\n"]
close $in_fh;

set out_fh [open $myoutfile w]

set cnt 0;
set start "";
set path "";
set done_start "";
set done_end "";
set data_paths "";
set heading "
  ---------------------------------------------------------------    ------------------
    Location            Delay type              Incr(ns)  Path(ns)    Netlist Resource(s)";
set diff_flag 1;
set count 0;
put                                                                          $out_fh
"~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~"
put                                                                          $out_fh
"~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~IFIS~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~"
put                                                                          $out_fh
"~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~"
foreach line $lines {
	set find_path_name [string first "    ------------------" $line];
	set x [string first "  Data Path Delay:" $line];
	#set prev $last
	if [expr {$find_path_name != -1}] then {
		set cnt [expr {$cnt + 1}]
	}
	if [expr {$x != -1}] then {
		set total_delay $line
	}
	if [expr {$cnt == 2}] then {
```

```
			#write the path create delay line by line
			#put $out_fh $line
			lappend data_paths $line
			set last [string range $line [expr {[string last " " $line] + 1}] [string length $line]]
			if [expr {[string first \[ $last] != -1}] then {set last [string range $last 0 [expr {[string first \[ $last] - 1}]]}

			if [expr {[llength $start] <= 1}] then {
				lappend start $last
			}
		}
		if [expr {$cnt == 3}] then {
			set diff_flag 1;

			for {set i 0} {$i < [llength $done_end]} {incr i} {
				if {[expr {[string compare [lindex $done_end $i] $last] == 0}] && [expr {[string compare [lindex $done_start $i] [lindex $start 1]] == 0}]} then {

					set diff_flag 0;
				}
			}

			if [expr {$diff_flag == 1}] then {
				lappend done_end $last
				lappend done_start [lindex $start 1];
				put $out_fh $heading
				foreach data_path $data_paths {
					#put $data_path
					put $out_fh $data_path
				}
				put $out_fh $line
				put $out_fh "  Below shown the delay from [lindex $start 1] to $last:"
				put $out_fh $total_delay
			}
			set start "";
			set data_paths "";
			incr count;
			set cnt 0
		}
		if [expr {$count == $stagePathNum}] then {
			break;
		}
}
put $out_fh "~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~"
```

```
put                                                                   $out_fh
"~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~IFIS~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~"
put                                                                   $out_fh
"~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~"
close $out_fh

set paths [get_timing_paths -delay_type max -from [get_cells icache/*cac_is*] -
max_paths $maxPathsGet]
report_timing -of_object $paths -file $myinfile

set in_fh [open $myinfile]
set lines [split [read $in_fh] "\n"]
close $in_fh;

set out_fh [open $myoutfile a]

set cnt 0;
set start "";
set path "";
set done_start "";
set done_end "";
set data_paths "";
set diff_flag 1;
set count 0;
put                                                                   $out_fh
"~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~"
put                                                                   $out_fh
"~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~ISID~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~"
put                                                                   $out_fh
"~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~"
foreach line $lines {
        set find_path_name [string first "    --------------------" $line];
        set x [string first "  Data Path Delay:" $line];
        #set prev $last
        if [expr {$find_path_name != -1}] then {
                set cnt [expr {$cnt + 1}]
        }
        if [expr {$x != -1}] then {
                set total_delay $line
        }
        if [expr {$cnt == 2}] then {
                #write the path create delay line by line
                #put $out_fh $line
                lappend data_paths $line
```

```
                    set last [string range $line [expr {[string last " " $line] + 1}] [string
length $line]]
                    if [expr {[string first \[ $last] != -1}] then {set last [string range $last
0 [expr {[string first \[ $last] - 1}]]}

                    if [expr {[llength $start] <= 1}] then {
                              lappend start $last
                    }
          }
          if [expr {$cnt == 3}] then {
                    set diff_flag 1;

                    for {set i 0} {$i < [llength $done_end]} {incr i} {
                              if {[expr {[string compare [lindex $done_end $i] $last] == 0}]
&& [expr {[string compare [lindex $done_start $i] [lindex $start 1]] == 0}]} then {

                                        set diff_flag 0;
                              }
                    }

                    if [expr {$diff_flag == 1}] then {
                              lappend done_end $last
                              lappend done_start [lindex $start 1];
                              put $out_fh $heading
                              foreach data_path $data_paths {
                                        #put $data_path
                                        put $out_fh $data_path
                              }
                              put $out_fh $line
                              put $out_fh "  Below shown the delay from [lindex $start 1] to
$last:"
                              put $out_fh $total_delay
                    }
                    set start "";
                    set data_paths "";
                    incr count;
                    set cnt 0
          }
          if [expr {$count == $stagePathNum}] then {
                    break;
          }
}

put                                                                                  $out_fh
"~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~"
put                                                                                  $out_fh
"~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~ISID~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~"
```

```
put $out_fh "~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~"
close $out_fh

set paths [get_timing_paths -delay_type max -from [get_cells icache/*cac_id*] -
max_paths $maxPathsGet]
report_timing -of_object $paths -file $myinfile

set in_fh [open $myinfile]
set lines [split [read $in_fh] "\n"]
close $in_fh;

set out_fh [open $myoutfile a]

set cnt 0;
set start "";
set path "";
set done_start "";
set done_end "";
set data_paths "";
set diff_flag 1;
set count 0;
put $out_fh "~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~"
put $out_fh "~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~IDEX~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~"
put $out_fh "~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~"
foreach line $lines {
	set find_path_name [string first "    -------------------" $line];
	set x [string first "  Data Path Delay:" $line];
	#set prev $last
	if [expr {$find_path_name != -1}] then {
		set cnt [expr {$cnt + 1}]
	}
	if [expr {$x != -1}] then {
		set total_delay $line
	}
	if [expr {$cnt == 2}] then {
		#write the path create delay line by line
		#put $out_fh $line
		lappend data_paths $line
		set last [string range $line [expr {[string last " " $line] + 1}] [string
length $line]]
		if [expr {[string first \[ $last] != -1}] then {set last [string range $last
0 [expr {[string first \[ $last] - 1}]]}
```

```
                if [expr {[llength $start] <= 1}] then {
                        lappend start $last
                }
        }
        if [expr {$cnt == 3}] then {
                set diff_flag 1;

                for {set i 0} {$i < [llength $done_end]} {incr i} {
                        if {[expr {[string compare [lindex $done_end $i] $last] == 0}]
&& [expr {[string compare [lindex $done_start $i] [lindex $start 1]] == 0}]} then {

                                set diff_flag 0;
                        }
                }

                if [expr {$diff_flag == 1}] then {
                        lappend done_end $last
                        lappend done_start [lindex $start 1];
                        put $out_fh $heading
                        foreach data_path $data_paths {
                                #put $data_path
                                put $out_fh $data_path
                        }
                        put $out_fh $line
                        put $out_fh "  Below shown the delay from [lindex $start 1] to
$last:"
                        put $out_fh $total_delay
                }
                set start "";
                set data_paths "";
                incr count;
                set cnt 0
        }
        if [expr {$count == $stagePathNum}] then {
                break;
        }
}

put                                                                     $out_fh
"~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~"
put                                                                     $out_fh
"~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~IDEX~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~"
put                                                                     $out_fh
"~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~"
close $out_fh
```

```
set paths [get_timing_paths -delay_type max -from [get_cells u_datapath/*dp_ex*]
-max_paths $maxPathsGet]
report_timing -of_object $paths -file $myinfile

set in_fh [open $myinfile]
set lines [split [read $in_fh] "\n"]
close $in_fh;

set out_fh [open $myoutfile a]

set cnt 0;
set start "";
set path "";
set done_start "";
set done_end "";
set data_paths "";
set diff_flag 1;
set count 0;
put                                                                    $out_fh
"~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~"
put                                                                    $out_fh
"~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~EXMEM~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~"
put                                                                    $out_fh
"~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~"
foreach line $lines {
        set find_path_name [string first "    -------------------" $line];
        set x [string first "  Data Path Delay:" $line];
        #set prev $last
        if [expr {$find_path_name != -1}] then {
                set cnt [expr {$cnt + 1}]
        }
        if [expr {$x != -1}] then {
                set total_delay $line
        }
        if [expr {$cnt == 2}] then {
                #write the path create delay line by line
                #put $out_fh $line
                lappend data_paths $line
                set last [string range $line [expr {[string last " " $line] + 1}] [string
length $line]]
                if [expr {[string first \[ $last] != -1}] then {set last [string range $last
0 [expr {[string first \[ $last] - 1}]]}

                if [expr {[llength $start] <= 1}] then {
                        lappend start $last
                }
        }
```

```
        if [expr {$cnt == 3}] then {
                set diff_flag 1;

                for {set i 0} {$i < [llength $done_end]} {incr i} {
                        if {[expr {[string compare [lindex $done_end $i] $last] == 0}]
&& [expr {[string compare [lindex $done_start $i] [lindex $start 1]] == 0}]} then {

                                set diff_flag 0;
                        }
                }

                if [expr {$diff_flag == 1}] then {
                        lappend done_end $last
                        lappend done_start [lindex $start 1];
                        put $out_fh $heading
                        foreach data_path $data_paths {
                                #put $data_path
                                put $out_fh $data_path
                        }
                        put $out_fh $line
                        put $out_fh "  Below shown the delay from [lindex $start 1] to
$last:"
                        put $out_fh $total_delay
                }
                set start "";
                set data_paths "";
                incr count;
                set cnt 0
        }
        if [expr {$count == $stagePathNum}] then {
                break;
        }
}

put                                                                    $out_fh
"~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~"
put                                                                    $out_fh
"~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~EXMEM~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~"
put                                                                    $out_fh
"~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~"
close $out_fh

set paths [get_timing_paths -delay_type max -from [get_cells
u_datapath/*dp_mem*] -max_paths $maxPathsGet]
report_timing -of_object $paths -file $myinfile

set in_fh [open $myinfile]
```

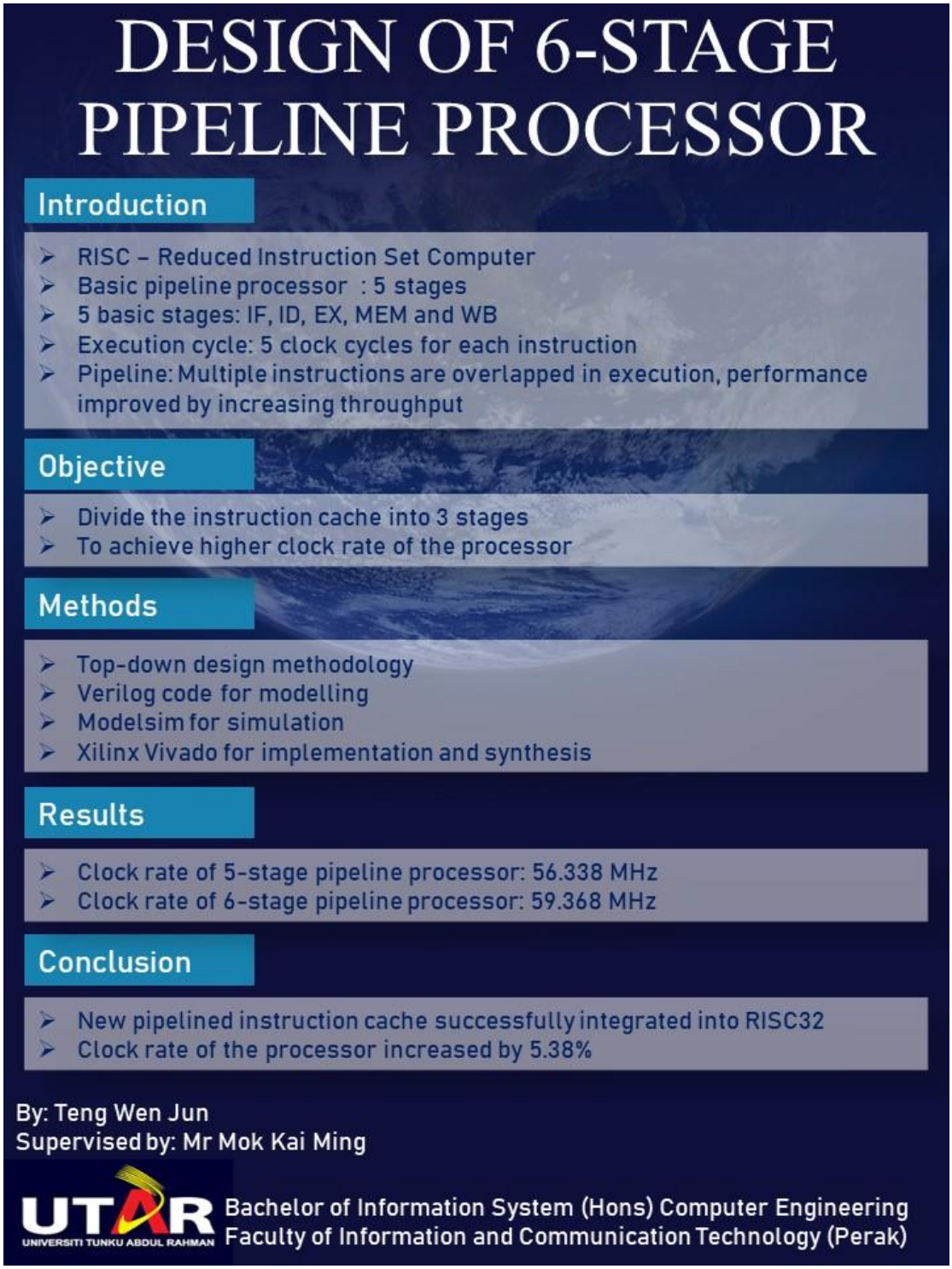
```
set lines [split [read $in_fh] "\n"]
close $in_fh;

set out_fh [open $myoutfile a]

set cnt 0;
set start "";
set path "";
set done_start "";
set done_end "";
set data_paths "";
set diff_flag 1;
set count 0;
put                                                                    $out_fh
"~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~"
put                                                                    $out_fh
"~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~MEMWB~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~"
put                                                                    $out_fh
"~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~"
foreach line $lines {
        set find_path_name [string first "    ----------" $line];
        set x [string first "  Data Path Delay:" $line];
        #set prev $last
        if [expr {$find_path_name != -1}] then {
                set cnt [expr {$cnt + 1}]
        }
        if [expr {$x != -1}] then {
                set total_delay $line
        }
        if [expr {$cnt == 2}] then {
                #write the path create delay line by line
                #put $out_fh $line
                lappend data_paths $line
                set last [string range $line [expr {[string last " " $line] + 1}] [string
length $line]]
                if [expr {[string first \[ $last] != -1}] then {set last [string range $last
0 [expr {[string first \[ $last] - 1}]]}

                if [expr {[llength $start] <= 1}] then {
                        lappend start $last
                }
        }
        if [expr {$cnt == 3}] then {
                set diff_flag 1;

                for {set i 0} {$i < [llength $done_end]} {incr i} {
```

```
                        if {[expr {[string compare [lindex $done_end $i] $last] == 0}]
&& [expr {[string compare [lindex $done_start $i] [lindex $start 1]] == 0}]} then {

                                set diff_flag 0;
                        }
                }

                if [expr {$diff_flag == 1}] then {
                        lappend done_end $last
                        lappend done_start [lindex $start 1];
                        put $out_fh $heading
                        foreach data_path $data_paths {
                                #put $data_path
                                put $out_fh $data_path
                        }
                        put $out_fh $line
                        put $out_fh "  Below shown the delay from [lindex $start 1] to
$last:"
                        put $out_fh $total_delay
                }
                set start "";
                set data_paths "";
                incr count;
                set cnt 0
        }
        if [expr {$count == $stagePathNum}] then {
                break;
        }
}

put                                                                                $out_fh
"~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~"
put                                                                                $out_fh
"~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~MEMWB~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~"
put                                                                                $out_fh
"~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~"
close $out_fh

set paths [get_timing_paths -delay_type max -from [get_cells u_datapath/*dp_wb*]
-max_paths $maxPathsGet]
report_timing -of_object $paths -file $myinfile

set in_fh [open $myinfile]
set lines [split [read $in_fh] "\n"]
close $in_fh;

set out_fh [open $myoutfile a]
```

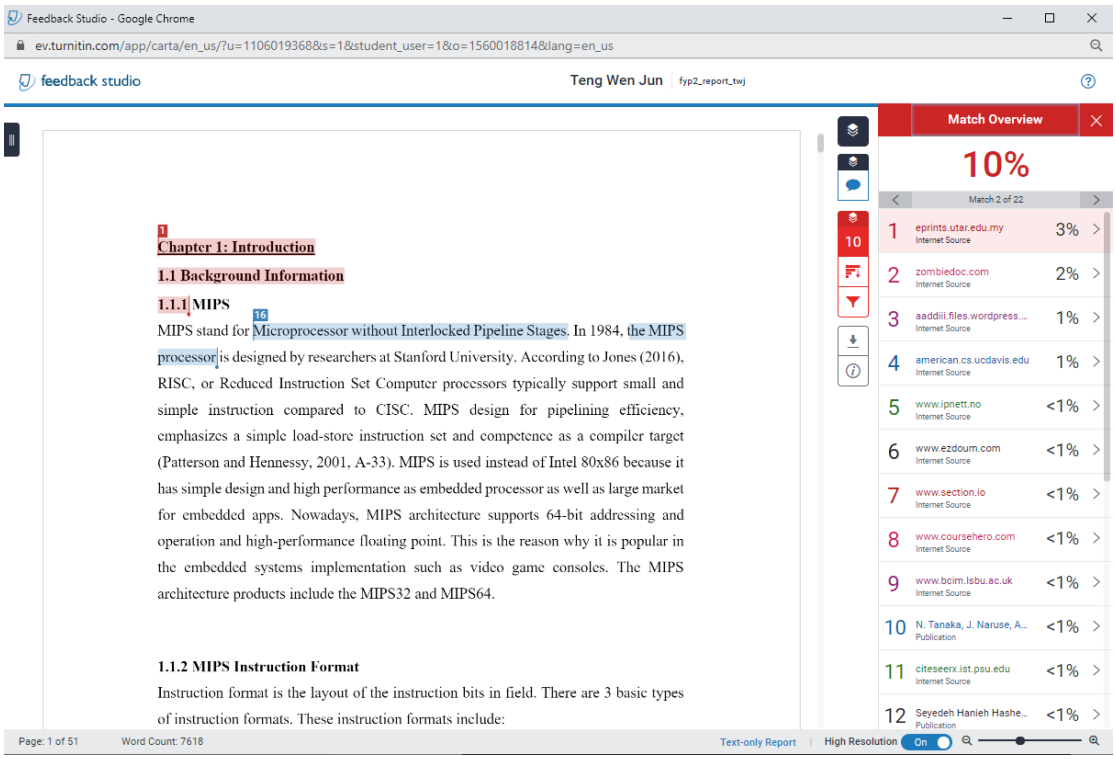
```
set cnt 0;
set start "";
set path "";
set done_start "";
set done_end "";
set data_paths "";
set diff_flag 1;
set count 0;
put                                                                    $out_fh
"~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~"
put                                                                    $out_fh
"~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~WB~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~"
put                                                                    $out_fh
"~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~"
foreach line $lines {
        set find_path_name [string first "    ----------" $line];
        set x [string first "  Data Path Delay:" $line];
        #set prev $last
        if [expr {$find_path_name != -1}] then {
                set cnt [expr {$cnt + 1}]
        }
        if [expr {$x != -1}] then {
                set total_delay $line
        }
        if [expr {$cnt == 2}] then {
                #write the path create delay line by line
                #put $out_fh $line
                lappend data_paths $line
                set last [string range $line [expr {[string last " " $line] + 1}] [string
length $line]]
                if [expr {[string first \[ $last] != -1}] then {set last [string range $last
0 [expr {[string first \[ $last] - 1}]]}

                if [expr {[llength $start] <= 1}] then {
                        lappend start $last
                }
        }
        if [expr {$cnt == 3}] then {
                set diff_flag 1;

                for {set i 0} {$i < [llength $done_end]} {incr i} {
                        if {[expr {[string compare [lindex $done_end $i] $last] == 0}]
&& [expr {[string compare [lindex $done_start $i] [lindex $start 1]] == 0}]} then {

                                set diff_flag 0;
                        }
```

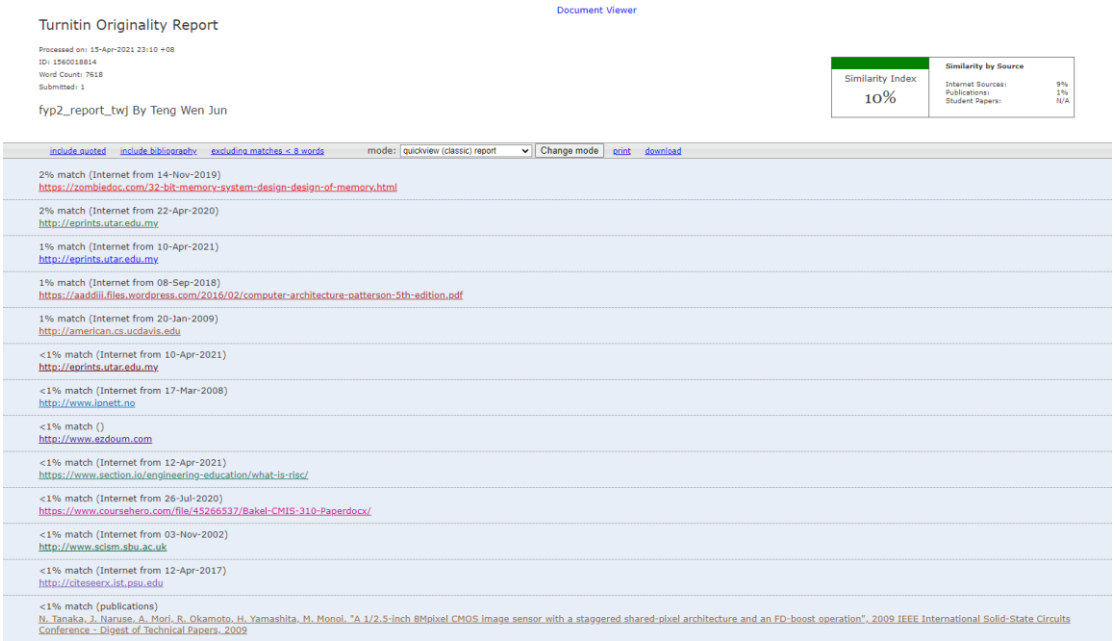
```
                }

                if [expr {$diff_flag == 1}] then {
                        lappend done_end $last
                        lappend done_start [lindex $start 1];
                        put $out_fh $heading
                        foreach data_path $data_paths {
                                #put $data_path
                                put $out_fh $data_path
                        }
                        put $out_fh $line
                        put $out_fh "  Below shown the delay from [lindex $start 1] to
$last:"
                        put $out_fh $total_delay
                }
                set start "";
                set data_paths "";
                incr count;
                set cnt 0
        }
        if [expr {$count == $stagePathNum}] then {
                break;
        }
}

put                                                                                $out_fh
"~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~"
put                                                                                $out_fh
"~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~WB~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~"
put                                                                                $out_fh
"~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~"
close $out_fh
```

Poster


DESIGN OF 6-STAGE PIPELINE PROCESSOR
Introduction
RISC – Reduced Instruction Set Computer
Basic pipeline processor : 5 stages
5 basic stages: IF, ID, EX, MEM and WB
Execution cycle: 5 clock cycles for each instruction
Pipeline: Multiple instructions are overlapped in execution, performance improved by increasing throughput
Objective
Divide the instruction cache into 3 stages
To achieve higher clock rate of the processor
Methods
Top-down design methodology
Verilog code for modelling
Modelsim for simulation
Xilinx Vivado for implementation and synthesis
Results
Clock rate of 5-stage pipeline processor: 56.338 MHz
Clock rate of 6-stage pipeline processor: 59.368 MHz
Conclusion
New pipelined instruction cache successfully integrated into RISC32
Clock rate of the processor increased by 5.38%
By: Teng Wen Jun
Supervised by: Mr Mok Kai Ming
UTAR
UNIVERSITI TUNKU ABDUL RAHMAN
Bachelor of Information System (Hons) Computer Engineering
Faculty of Information and Communication Technology (Perak)

Plagiarism Check Result





Universiti Tunku Abdul Rahman			
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Form Number: FM-IAD-005	Rev No.: 0	Effective Date: 01/10/2013	Page No.: 1of 1

FACULTY OF INFORMATION AND COMMUNICATION TECHNOLOGY

Full Name(s) of Candidate(s)	TENG WEN JUN
ID Number(s)	1701947
Programme / Course	CT
Title of Final Year Project	DESIGN OF 6-STAGE PIPELINE PROCESSOR

Similarity	**Supervisor's Comments (Compulsory if parameters of originality exceeds the limits approved by UTAR)**
Overall similarity index: 10 % **Similarity by source** Internet Sources: 9% Publications: 1 Student Papers: N/A %	
Number of individual sources listed of more than 3% similarity: 0	

Parameters of originality required and limits approved by UTAR are as Follows:

(i) Overall similarity index is 20% and below, and

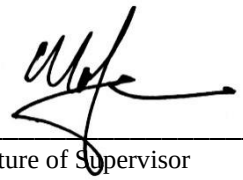
(ii) Matching of individual sources listed must be less than 3% each, and

(iii) Matching texts in continuous block must not exceed 8 words

Note: Parameters (i) – (ii) shall exclude quotes, bibliography and text matches which are less than 8 words.

Note Supervisor/Candidate(s) is/are required to provide softcopy of full set of the originality report to Faculty/Institute

Based on the above results, I hereby declare that I am satisfied with the originality of the Final Year Project Report submitted by my student(s) as named above.



Signature of Supervisor

Name: MOK KAI MING

Date: 16/4/2021

Signature of Co-Supervisor

Name: _____

Date: _____

UNIVERSITI TUNKU ABDUL RAHMAN

FACULTY OF INFORMATION & COMMUNICATION TECHNOLOGY (KAMPAR CAMPUS)

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√	List of Tables (if applicable)
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