DESIGN OF A 7-STAGE PIPELINE RISC PROCESSOR
(MEM STAGE)

BY

CHOO JIA ZHENG

A REPORT

SUBMITTED TO

Universiti Tunku Abdul Rahman

in partial fulfillment of the requirements

for the degree of

BACHELOR OF INFORMATION TECHNOLOGY (HONOURS)

COMPUTER ENGINEERING

Faculty of Information and Communication Technology

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FACULTY OF INFORMATION AND COMMUNICATION TECHNOLOGY
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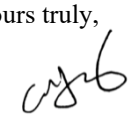
It is hereby certified that **CHOO JIA ZHENG** (ID No.: **18ACB03197**) has completed this final year project entitled "**DESIGN OF A 7-STAGE PIPELINE RISC PROCESSOR (MEM STAGE)**" under the supervision of **Mr. LEE HENG YEW** from the Department of Computer and Communication Technology, Faculty of Information and Communication Technology.

I understand that the University will upload softcopy of my final year project in pdf format into UTAR Institutional Repository, which may be made accessible to UTAR community and public.

Yours truly,



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I declare that this report entitled "**DESIGN OF A 7-STAGE PIPELINE RISC PROCESSOR (MEM STAGE)**" is my own work except as cited in the references. The report has not been accepted for any degree and is not being submitted concurrently in candidature for any degree or other award.

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Name : CHOO JIA ZHENG

Date : 4th April 2022

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I would like to express my sincere thanks and appreciation to my FYP ex-supervisor, Mr. Mok Kai Ming, my FYP supervisor, Mr Lee Heng Yew and my FYP moderator, Ts Ooi Joo On, where all of them have provided me this bright opportunity to engage in the processor and digital system design project. It is my first step to establish a career in the digital system design field. A special thanks too to Mr. Mok for guiding me and assisting me during the whole project development which makes me came to know and learn a lot of new things. Again, thanks for your precious time and patience along with the duration of my project.

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ABSTRACT

This project is about the design and implementation of a 32-bits RISC 7-Stage pipeline processor for academic purpose. The main objective of this project is to improve the performance of the existing 32-bits RISC 5-stage pipeline processor developed in Faculty of Information, Communication and Technology, University Tunku Abdul Rahman. The performance of the processor is improved and optimized by increasing the number of pipeline stages to obtain a shorter time delay for each stage. The MEM stages of the existing pipeline processor contribute to the longest timing delay, which reduce the performance of the processor due to the imbalance logics among the stages. In this project, the data cache unit is decomposed and pipelined into 2 stages. Cache unit access will now require two clock cycle if a CACHE HIT is detected. Another extra stage is reserved for the implementation of Translation Look Aside Buffer (TLB) in the future. Some modifications on the cache controller is done to improve its performance too. The newly developed data cache unit is modelled using Verilog coding follow with its functional verification. Lastly, synthesis and implementation using Xilinx Vivado is done to obtain the timing delay of the new developed 7-stage RISC pipeline processor.

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LIST OF ABBREVIATIONS

ALU	Arithmetic Logic Unit
CISC	Complex Instruction Set Computer
CPU	Central Processing Unit
D-Cache	Data Cache
DF	Data Fetch Stage, First Half
DS	Data Fetch Stage, Second Half
EDA	Electronic Design Automation
EX	Execution Stage
FP	Floating Point
FPGA	Field Programmable Gate Array
FYP	Final Year Project
HDL	Hardware Description Language
IC	Integrated Circuit
I-Cache	Instruction Cache
ID	Instruction Decode Stage
IF	Instruction Fetch Stage, (First Half)
IS	Instruction Fetch Stage, Second Half
ISA	Instruction Set Architecture
LRU	Least Recently Used
MEM	Data Memory Access Stage
MIPS	Microprocessor without Interlocked Pipelined Stages
PC	Program Counter
PR	Predict and Register Fetch Stage
RAM	Random Access Memory
RISC	Reduced Instruction Set Computer
RF	Register Fetch Stage
ROM	Read Only Memory
RTL	Register-transfer Level
SDRAM	Sequential Dynamic RAM
TC	Tag Check Stage
TLB	Translation Look-Aside Buffer

UC Berkeley EECS	University of California, Berkeley, Department of Electrical Engineering and Computer Science
UTAR	Universiti Tunku Abdul Rahman
WB	Write Back Stage

Chapter 1: Introduction

1.1 Background Information

The overview of the fields that matter for this project is provided to help in identifying and understanding some facts or pre-knowledge related to this project.

1.1.1 MIPS

Microprocessor without Interlocked Pipelined Stages, also known as MIPS, is a reduced instruction set computer (RISC) instruction set architecture (ISA) which is currently developed by the MIPS Technologies, based in the United States of America nowadays [9]. The MIPS processor was first designed and developed by a group of researchers at Stanford University including John L. Hennessy, Chris Rowen and David A. Patterson. The MIPS processor is well known for pioneering the RISC concept. According to [3], RISC processors typically support small and simple instruction compared to CISC. MIPS emphasizes a simple load-store instruction set, design for pipelining efficiency and efficiency as a compiler target [5, pp. A-33]. MIPS is mainly used as an embedded processor for the large market for embedded applications due to its simple design and high performance instead of the Intel 80x86 processor that is primarily “CISC” design with emphasis on backward compatibility which is lot more complex. Till nowadays, MIPS architecture supports up to 64-bit addressing and operation and is able to operate on single precision (32-bit) and double precision (64-bit) floating point numbers [1]. It is believed that this is the reason it is popular in the embedded systems implementation such as video game consoles. Some MIPS architecture designed include the MIPS32 and MIPS64.

1.1.2 Pipelining

In order to make a CPU processor run faster, pipelining is introduced. Pipelining is known as an implementation technique where multiple instructions are overlapped in execution [6, Ch. 6.1]. As what discussed earlier, MIPS basic processor consists of 5 stages. Figure 1-1 shows a single-cycle CPU executes the instruction while Figure 1-2 shows the pipeline CPU executes the instruction.

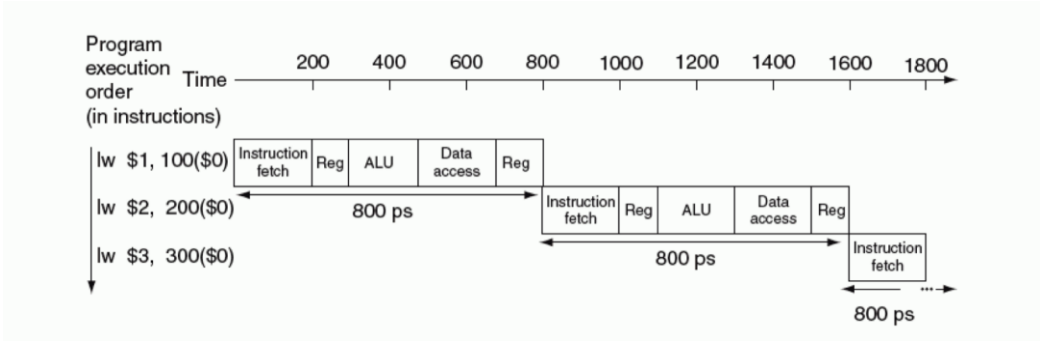

Figure 1-1: Single-cycle, Nonpipelined Execution [6, Ch.6.1].

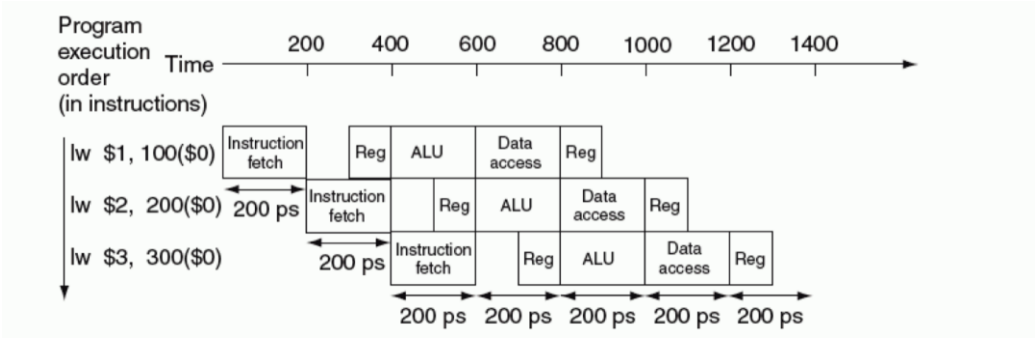

Figure 1-2: Pipelined Execution [6, Ch.6.1].

We clearly see that the next instruction will start to execute by being fetched into the IF stage only when the previous instruction has finished executing the WB stage in a single-cycle CPU. However, in the pipeline CPU, the next instruction starts to execute by fetching it into the IF stage once the IF stage finish executing the previous instruction.

The 5-stage pipelined processor is able to complete one instruction in one clock cycle. Throughput of the processor is increased which indicates the increment in performance for the processor. Nowadays, the pipelining is the key implementation techniques introduced to improve the CPU processor performance.

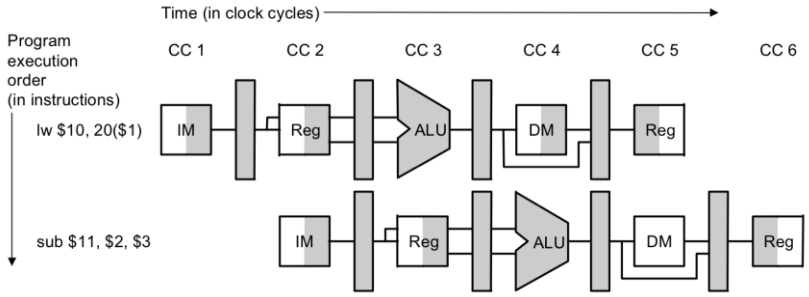

Figure 1-3: 5-stage Pipeline Execution Cycle in Structural View [5, pp. A-18]

Figure 1-4 shows a big picture on how the hardware components allocated in each pipeline stages for a basic 5-stage pipeline processor.

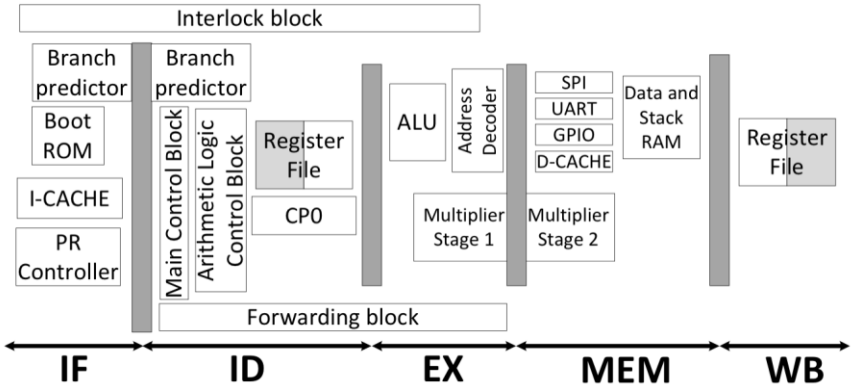

Figure 1-4: Abstract View of 5-stage Pipeline Execution Cycle [13]

1.2 Motivation

An existing 32-bit RISC 5-stage pipeline microprocessor has been developed in the FICT, UTAR by using Verilog Hardware Description Language. The project is based on the RISC architecture. The motivations to initiate the project are on account of the following reasons:

- Microchip design companies have designed microprocessors as Intellectual Property (IP) for commercial purposes. The microprocessor IP encompasses information on the complete design process for both the front-end (modeling and verification) and the back-end (physical design) of the integrated circuit (IC) design. These IPs are the trade secrets of a company and they are definitely not available in the market at an affordable price or without cost for research purposes.
- Several freely available microprocessor cores can be found in the Internet and most of them are available at OpenCores (**http://www.opencores.org/**). However, those processors do not implement the entire MIPS Instruction Set Architecture (ISA) and they lack comprehensive documentation. Because of these issues, it makes them not suitable for reuse and customization.
- The verification specifications for a freely available RISC microprocessor core that are available in the Internet are incomplete and not well developed. Therefore, without a comprehensive verification specification, the verification process of a RISC microprocessor core will be slow-going. Eventually, it might slow down the overall design process.
- The physical design phase will inevitably be affected due to the lack of well-developed verification specifications for these microprocessor cores. A design needs to be functionally verified before the physical design phase can be carried out smoothly. Otherwise, if the front-end design needs to be changed, the physical design process has to be redone.

The RISC32 project that has been initiated in UTAR aims to provide solutions to all the problems mentioned above by creating a 32-bit RISC core-based development environment in order to assist research works in the area of soft-core as well as the application specific hardware modeling. Up to date, the RISC32 project that was initiated in UTAR has completed the CPU designs that supports basic instructions similar to MIPS instructions. The system control coprocessor that is the Coprocessor 0 (CP0) is also available to interface with I/O devices and handle interrupts.

With the available microarchitecture design developed in the UTAR FICT, we can easily gain the software or firmware flexibility advantage without having to rely and wait for third party community to develop for us.

With the completion of this project, a data cache unit that is decomposed and pipelined into two stages will be available. It is then to be integrated into the existing 32-bit RISC 5-stage pipeline processor. With further development and modification, a 32-bit RISC 7-stage pipeline processor with improved timing delay will be developed for the academic purpose in the future.

1.3 Problem Domain

A basic 5-stage pipeline processor definitely improves the CPU throughput compared to the 5-stage single-cycle processor. However, there is still a lack on the performance of a basic 5-stage pipeline processor. This is due to the imbalance timing delay among the pipe stages since the clock can run no faster than the time needed for the slowest stage [5, pp. C-10].

This problem is emphasized as it directly affects the processor clock rate. Table 1-1 shows the timing delay from each of the pipeline stage of the existing 5-stage pipeline processor .

Pipeline Stage	IF	ID	EX	MEM	WB
Timing Delay (ns)	14.118	12.551	14.717	18.262	3.332

Table 1-1: Timing Delay for 5-stage Pipeline Processor Pipeline Stages

The problem is partially fixed by Teng Wen Jun, one of the seniors from FICT, UTAR. A 6-stage pipeline processor is developed by decomposing the instruction cache unit and branch predictor in the IF stage into three stages [12]. Table 1-2 shows the timing delay from each of the pipeline stage of the 6-stage pipeline processor developed.

Pipeline Stage	IF	IS	ID	EX	MEM	WB
Timing Delay (ns)	7.126	13.063	11.889	13.638	17.511	3.402

Table 1-2: Timing Delay for 6-stage Pipeline Processor Pipeline Stages

We clearly see that the timing delay of MEM stage is still the longest. As we know, every pipeline stage of a pipeline processor is operating at every clock cycle. Hence, we have to compromise by using the longest time delay which in this case is 17.511ns as our clock period even though other stages require a shorter timing delay. The worst case is when comparing the timing delay of MEM stage with the WB stage, a difference of 14.109ns is observed.

From the scenario above, the clock rate of the processor is determined using the longest time delay of the pipeline stages.

$$Clock\ rate\ of\ 6-stage\ pipeline\ processor = \frac{1}{17.511ns} = 57.107MHz$$

The problem mentioned is faced by all the users that use computational devices and at most, specifically the developers of computer software. No matter the one who use a personal computer or a large server, as we all know, we, the human, always requires the things around us better, faster and more advanced. Hence, human always make great invention and improve things around us to be better and better. No matter how good a software is, it still requires a faster enough processor for it to run on. And this project is going to improve the throughput of the processor.

1.4 Project Scope

The project scope is mainly focus on designing and implementing the MEM stages of the 7-stage pipeline processor. The MEM stages included the DF and TC stage. The specifications of the 7-stage pipeline processor will be functionally verified by using testbench. Besides, Field Programmable Gate Array (FPGA) technology will be used to synthesize the 7-stage pipeline processor designed.

Lastly, at the end of this project, a comprehensive documentation including the RTL modelling and testbench of this project will be well developed and a simulation results are expected to be delivered. Synthesis and implementation model of the developed works will also be submitted.

1.5 Project Objectives

The objectives of this project are as follow:

- To design and implement the 7-stage pipeline processor (MEM stages) by splitting the MEM stage of the basic 5-stage pipeline processor into two stages which are known as DF and TC stage in order to achieve a higher processor clock rate.
- To develop a complete test plan to test and verify the functional correctness of the 7-stage pipeline processor designed.
- To synthesis and implement the 7-stage pipeline processor using the FPGA technology.

1.6 Impact, Significance and Contribution

After this project is done, it can provide a complete 7-stage pipeline RISC microprocessor core-based development environment. The development environment refers to the availability of the following:

- A well-developed design documentation of chip specification, architecture specification and micro-architecture specification.
- A fully functional and well-developed 7-stage pipeline processor (MEM stages) in the form of synthesis-ready RTL written in Verilog HDL.
- A well-developed verification specification of the 7-stage pipeline processor (MEM stages) which contains suitable verification methodology, verification techniques, test plan, testbench architecture and etc.
- A complete design in FPGA with documented timing and resources usage information.

Furthermore, a higher clock rate RISC processor that is MIPS ISA compatible with 7 stages pipelining is developed. Imbalanced timing delay occurred in the MEM stage of the basic 5-stage pipeline processor is tackled to increase the overall performance of the pipeline processor.

In terms of contribution, this project can contribute to develop an environment mentioned above by providing support to the hardware modeling research work later. With the available well-developed basic RISC RTL model which has been fully functionally verified, the verification environment and the design documents, a researcher will be able to develop their own research specific RTL model as part of the MIPS environment and can quickly verify the model to obtain result. As a result, the research work could be done easier and speed up significantly.

1.7 Report Organization

This report consists of 9 chapters and the details of the project are shown as follow:

In **Chapter 1**, some background information that matters for this project is provided, followed by the motivation of this project, the problem statement, project scope and objective in order to help readers to understand some facts or knowledge related to this project.

In **Chapter 2**, a literature review on the 8-stage pipeline processors designed by MIPS and UC Berkeley, and cache unit designed by seniors has been highlighted and compared.

In **Chapter 3**, the methodologies and general work procedure for modeling, verifying, and synthesizing the 32-bits RISC 7-stage pipeline processors to be built has been discussed. It also discusses about the appropriate design tools used for the design work, the technologies involved, the implementation issues and challenges, as well as the timeline of this project.

In **Chapter 4**, the system overview of the newly developed 32-bits RISC 7-stage pipeline processor. The microarchitecture, memory map, chip interface, and pin description of the processor used are stated in detail in this chapter.

In **Chapter 5**, it shows the full information about the microarchitecture specification of the newly designed cache unit and cache controller. It gives an overview on how the datapath unit, cache unit, forwarding block, interlock block, address decoder block and cache controller block works in terms of their functionality, block interface, pin description, and so on.

In **Chapter 6**, it discusses about how the newly developed 7-stage pipeline processor and the pipelined cache (D-Cache) are functionally verified. All of the related verification specifications, test plans, and stimulation results can be found in this chapter too. The testbench of the pipeline cache could be further found in Appendices A.

In **Chapter 7**, it discusses the synthesis and implentation setting for the project. The timing delay of the newly developed 7-stage pipeline processor, and also the existing 32-bit RISC 5-stage and 6-stage pipeline processors can be found in this chapter.

In **Chapter 8**, it concludes the overall project development, highlighting what have been achieved or done in this project. The future work for this is projectalso discussed here.

Chapter 2: Literature Review

As what is mentioned in the previous section, although pipelining has greatly improved the throughput of the processor, the performance of the basic 5-stage pipeline processor is still not yet maximized. This is mainly due to the imbalance timing delay from each pipeline stages. Several researchers have put in effort in resolving the processor performance issue. One of the famous measures is through decomposing the basic 5 stages pipeline of the processor into more pipeline stages such as developing an 8-stage pipeline processor.

2.1 MIPS R4000 Pipeline Details [7]

MIPS R4000 is introduced to the world in 1991 to solve the performance issue due to the imbalance timing delay. 8-stage pipeline is firstly introduced. The MIPS R4000's 8 pipeline stages allow it to process more instruction per clock cycle than the basic 5-stage pipeline processor. From Figure 2-1, we can see that once the 8-stage pipeline is filled, eight instructions are executed simultaneously. Superpipelining has spilt the instruction and data memory references across two stages. Consequently, the logics are more evenly distributed across the pipeline stages.

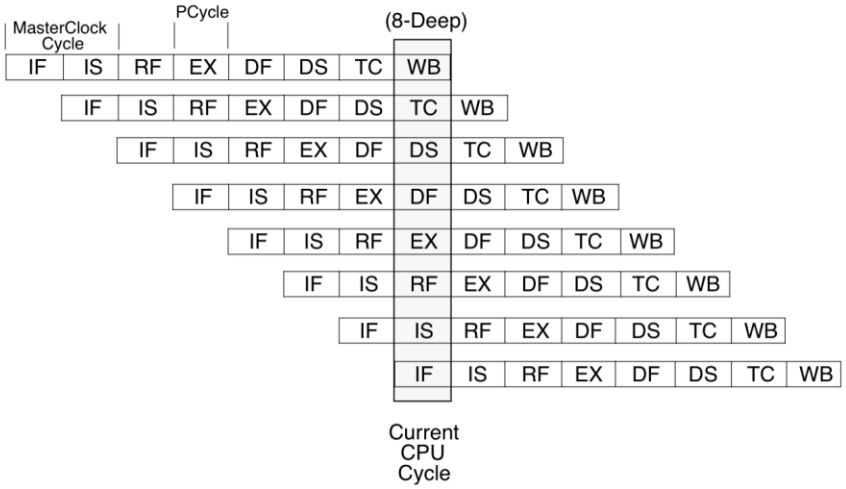

Figure 2-1: Instruction Pipeline Stages [7, pp. 74]

Basically, the execution of an instruction in R4000 can be done by 8 stages. Figure 2-2 below shows the 8-stage pipeline structure using an abstracted version of data path. The 8 stages are as below:

- IF : Instruction Fetch, First Half
- IS : Instruction Fetch, Second Half
- RF : Register Fetch
- EX : Execution
- DF : Data Fetch, First Half
- DS : Data Fetch, Second Half
- TC : Tag Check
- WB : Write Back

This section describes the 8 pipeline stages of R4000 processor.

IF - Instruction Fetch, First Half

During the IF stage, the following occurs:

- PC selection happens here.
- Branch logic selects an instruction address and the instruction cache fetch begins.
- The instruction translation lookaside buffer (ITLB) begins the virtual-to-physical address translation.

IS - Instruction Fetch, Second Half

During the IS stage, the instruction cache fetch and the virtual-to-physical address translation are completed.

RF - Register Fetch

During the RF stage, the following occurs:

- The instruction decoder (IDEC) decodes the instruction and checks for interlock conditions (hazard detection).
- The instruction cache tag is checked against the page frame number obtained from the ITLB (instruction cache hit detection).
- Any required operands are fetched from the register file.

EX - Execution

During the EX stage, one of the following occurs:

- The arithmetic logic unit (ALU) performs the arithmetic or logical operation for register-to-register instructions.
- The ALU calculates the data virtual address for load and store instructions.
- The ALU determines whether the branch condition is true and calculates the virtual branch target address for branch instructions.

DF - Data Fetch, First Half

During the DF stage, one of the following occurs:

- The data cache fetch and the data virtual-to-physical translation begins for load and store instructions.
- The branch instruction addresses translation and translation lookaside buffer (TLB)† update begins for branch instructions.
- No operations are performed during the DF, DS, and TC stages for register-to-register instructions.

DS - Data Fetch, Second Half

During the DS stage, one of the following occurs:

- The data cache fetch and data virtual-to-physical translation are completed for load and store instructions. The Shifter aligns data to its word or doubleword boundary.
- The branch instruction address translation and TLB update are completed for branch instructions.

TC - Tag Check

For load and store instructions, the cache performs the tag check during the TC stage. The physical address from the TLB is checked against the cache tag to determine if there is a hit or a miss.

WB - Write Back

For register-to-register instructions, the instruction result is written back to the register file during the WB stage. Branch instructions perform no operation during this stage.

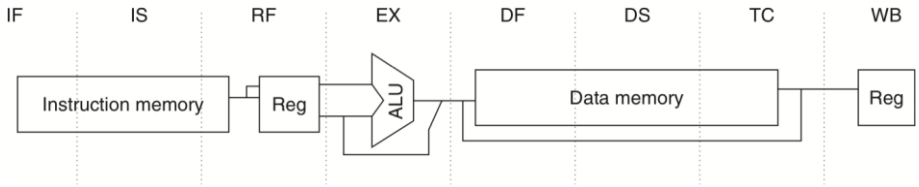

Figure 2-2: The 8-stage Pipeline Structure of R4000 [4, pp. A-64]

Figure 2-3 shows the pipeline activities that is more evenly distributed occurs in each pipeline stages of R4000.

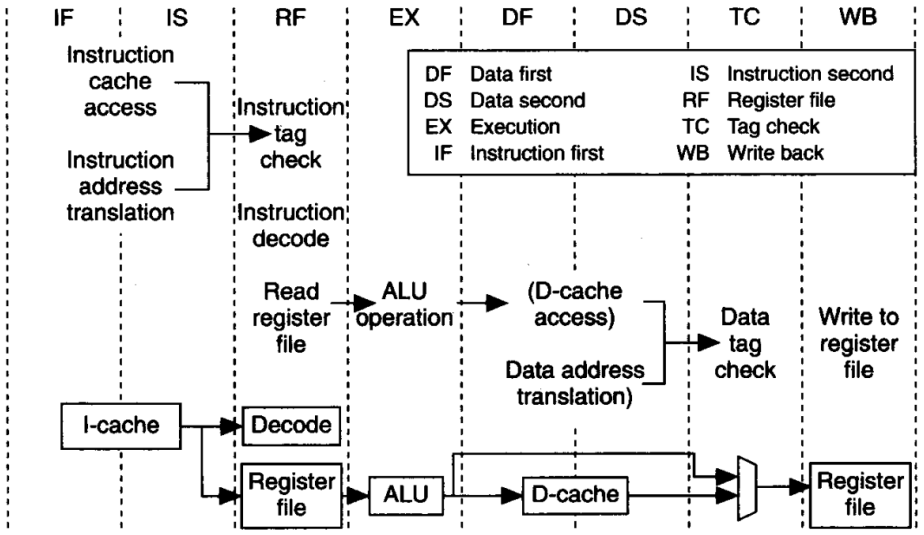

Figure 2-3: Pipelines Activities of R4000 [11]

2.2 Branch and Load Delay

2.2.1 Branch Delay

The R4000's pipeline has a branch delay of three cycles. The three-cycle branch delay is a result of the branch comparison logic operating during the EX stage of the branch instruction, producing a valid instruction address that is available in the IF stage, at the fourth instructions later.

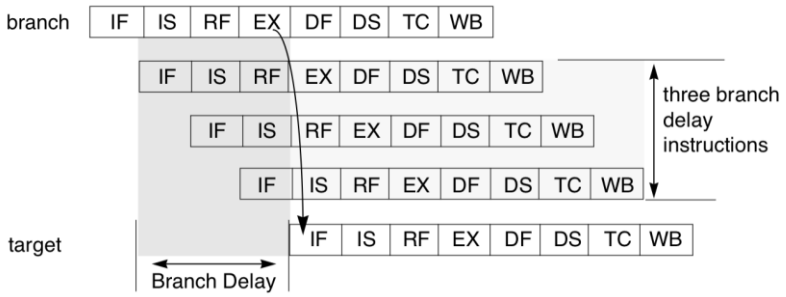

Figure 2-4: CPU Pipeline Branch Delay I [7, pp. 48]

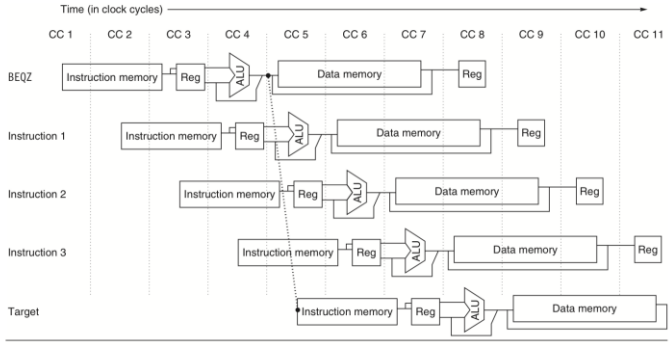

Figure 2-5: CPU Pipeline Branch Delay II [4, pp. A-66]

Figure 2-4 shows the basic branch delay of R4000 processor is 3 cycles using an abstracted structural view of data path due to the branch condition evaluation is performed during EX stage by using the ALU. MIPS architecture has a single cycle delayed branch. The R4000 processor uses a predicted-not-taken strategy for the remaining 2 cycles of the branch delay. This insists that untaken branches simply consist of 1-cycle delay slot and the processor will still continuing execute the instruction that enters the pipeline. However, for taken branches, there will be a 1-cycle delay slot followed by 2 idle cycles. This means that R4000 will still execute one more instruction after the branch instruction which known as the delayed slot instruction. By the same time, the remaining 2 instructions will be nullified by flushing the IF/IS and IS/RF pipeline register with '0' during the next clock cycle.

2.2.2 Load Delay

There is a 2-cycle delay for the load instruction to be executed on the R4000 processor. This is due to the data value can only be obtained at the end of the data cache access in DS stage. Figure 2-6 shows the R1 value can only be used as the input operand for the ALU in EX stage from the third instruction onwards after the load instruction which load values into R1 register is executed. If R1 value is used earlier than the third instruction, false value will be used which leads to incorrect operation.

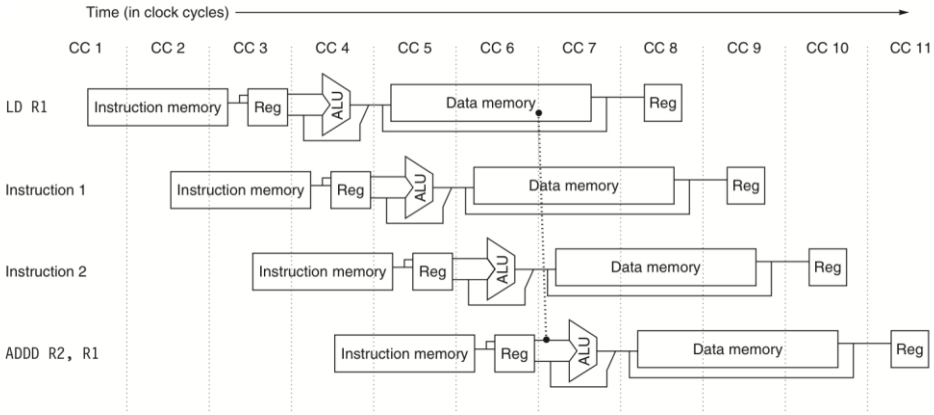

Figure 2-6: CPU Pipeline Load Delay I [4, pp. A-65]

Figure 2-7 shows the completion of a load at the end of the DS pipeline stage produces an operand that is available for the EX pipeline stage of the third subsequent instruction.

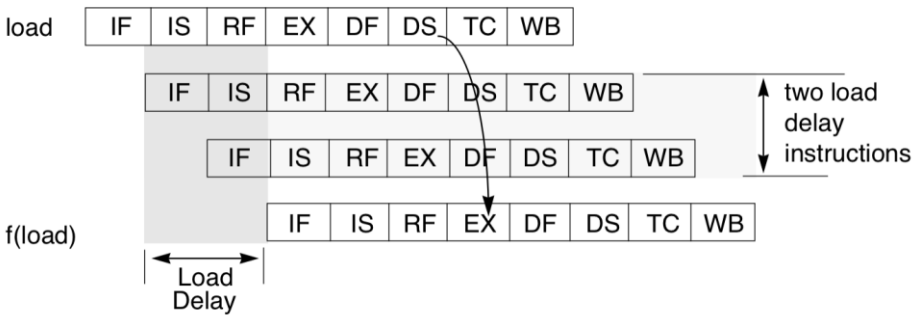

Figure 2-7: CPU Pipeline Load Delay II [7, pp. 48]

In order to maximize the processor performance, R4000 only interlock the pipeline stages if it is found that the two instructions after the load instruction access register same as the destination register (rd) of the load instruction. This ensure that the next two instruction will use the correct value which is the results obtained from load instruction.

When the hardware interlocks and slips, the PC and the IF/IS, IS/RF, RF/EX pipeline registers will be hold and retaining the old values in it. This insists that the DF, DS, TC and WB stages of the pipeline will advance while the IF, IS, RF and EX stage will not, and this is shown in Figure 2-8. In this case, the clock cycle that experiencing this type of operation is called a slip run instead of a full run as some stages are slip across the clock cycle. This permits the load instruction to execute and complete its data cache access in advance, while the next two instruction that depends on the load instruction will remain in the EX and RF stage.

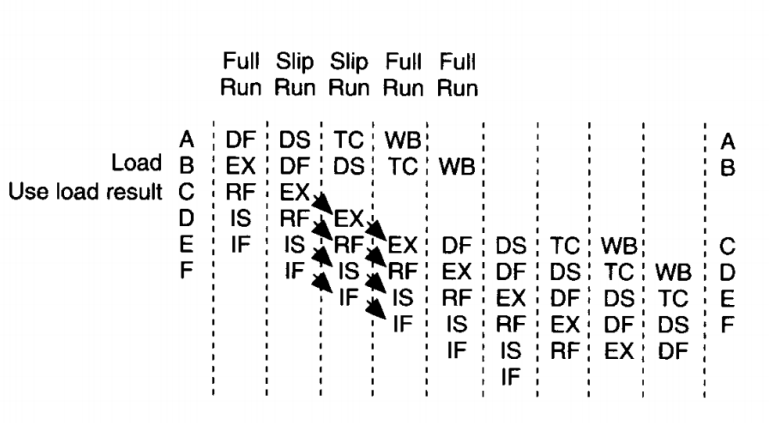

Figure 2-8: Load Interlock/ Slip Cycle [11]

2.3 Data Forwarding (Bypassing)

Data forwarding is a useful technique implements to resolve the data hazards of the processor. Besides, it improves the performance of the processor by reducing the number of stalling the processor. It takes the result from the earliest point that it exists and forward it to the functional units at the EX stage that needs it.

The deeper pipeline introduced to the R4000 also contributes to the increment in the number of levels of forwarding for ALU operations. Unlike the basic 5-stage where forwarding usually happened from the EX/MEM and MEM/WB pipeline register, there are actually four possible sources for ALU data forwarding which is from the EX/DF, DF/DS, DS/TC and TC/WB pipeline registers.

As what is shown in Figure 2-7, the instruction after the load instruction actually use data forwarding to obtain the valid operands from the DS/TC pipeline register for ALU operations after the stall [5, pp. C-21].

	Clock number								
Instruction number	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
LD R1,...	IF	IS	RF	EX	DF	DS	TC	WB	
DADD R2,R1,...		IF	IS	RF	Stall	Stall	EX	DF	DS
DSUB R3,R1,...			IF	IS	Stall	Stall	RF	EX	DF
OR R4,R1,...				IF	Stall	Stall	IS	RF	EX

Figure 2-9: A load instruction followed by an immediate use results in a 2-cycle stall [4, pp. A-65]

Another example would be from Figure 2-9. Normal forwarding path can be used after 2 cycles, so the DADD and DSUB get the value by forwarding after the stall. The OR instruction gets the value from the register file. Since the two instructions after the load could be independent and hence not stall, the bypass can be to instructions that are 3 or 4 cycles after the load.

2.4 Memory Hierarchy

Basically, there is a tradeoff among the access time, cost and capacity of the memories. Fast memories with short access time, like CPU registers and cache are low in capacity and high in cost. On the other hand, a cheap and large capacity memories, where its capacity is up to TBs (Terabytes), like the magnetic tape or optical disk, would has an extremely long access time.

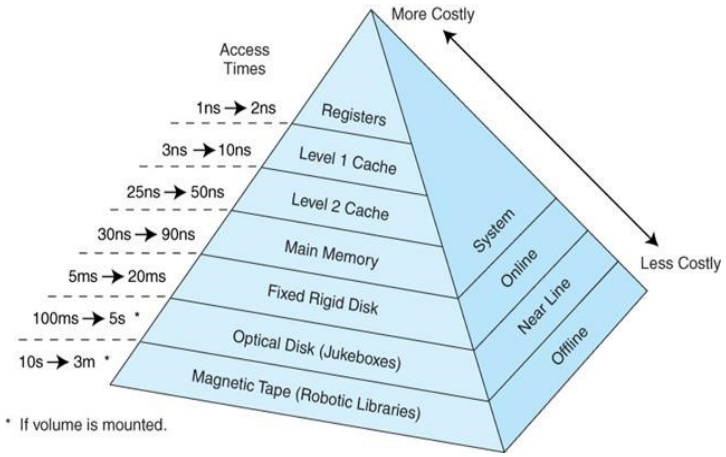

Figure 2-10: The Memory Hierarchy [8]

From Figure 2-10, we also get to know that the faster memory is closer to the processor, while the slower memory is relevantly further. The goal is to provide a memory system with cost per byte as low as the cheapest level of memory and speed almost as fast as the fastest level. Therefore, we have to take advantage by utilizing the memory hierarchy and implements the suitable memory system in order to speed up the processor performance.

2.4.1 MIPS R4000 Memory Organization

Cache memory is used in R4000 to speed up the memory access process, thus speed up the performance of the processor. Figure 2-11 shows the R4000 system memory hierarchy. The R4000 processor has two on-chip primary caches, the instruction cache (I-Cache) and the data cache (D-cache) which holds instructions and data respectively [7].

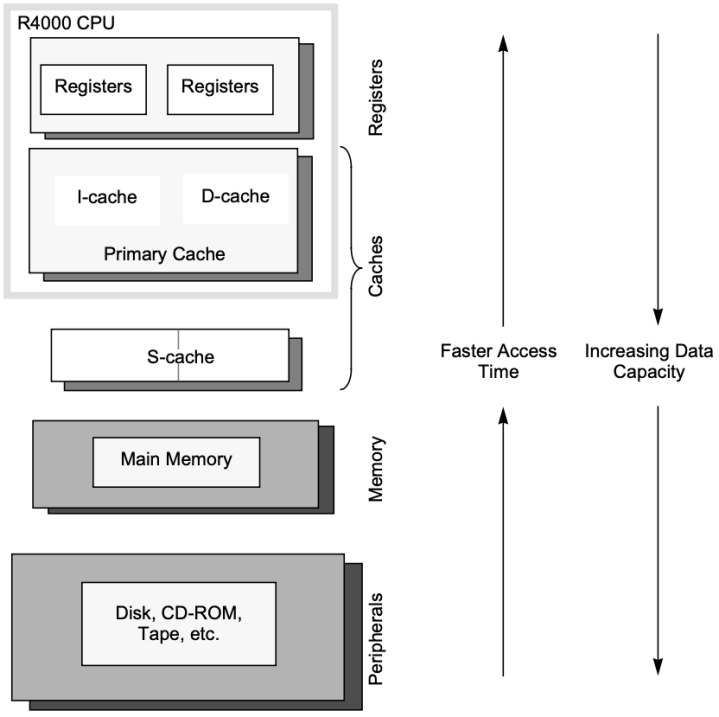

Figure 2-11: R4000 Logical Hierarchy of Memory [7, pp. 244]

In the logical memory hierarchy, caches lie between the processor and the main memory (RAM). They are designed to speed up the instruction and data memory accesses. From Figure 2-11, each functional block has a larger capacity to hold more data than the block above it. For illustration, the main memory has a larger capacity compared to the secondary cache.

However, at the same time, each functional block takes longer time to access than any block above it. For instance, it takes longer to access data in main memory than in the CPU on-chip registers. This is what the tradeoff among the access time, cost and capacity of the memories mentioned in the previous section.

2.5 Cache

2.5.1 Cache Operation [5], [7]

Caches provide fast temporary data storage, and they speed up the memory accesses transparent to the user. In general, the processor accesses cache-resident instructions or data through the following procedure:

1. The processor attempts to access the next instruction or data in the primary cache through the on-chip cache controller.

2. The cache controller checks to see if this instruction or data is present in the primary cache.
    - If the instruction/data is present, the processor retrieves it. This is called a primary cache hit.
    - If the instruction/data is not present in the primary cache, the cache controller must retrieve it from the secondary cache or memory. This is called a primary-cache miss.

3. If a primary-cache miss occurs, the cache controller checks to see if the instruction/data is in the secondary cache.
    - If the instruction/data is present in the secondary cache, it is retrieved and written into the primary cache.
    - If the instruction/data is not present in the secondary cache, it is retrieved as a cache line from the main memory and is written into both the secondary cache and the appropriate primary cache.

4. The processor retrieves the instruction/data from the primary cache and operation continues.

It is possible for the same data to be in three places simultaneously: main memory, secondary cache, and primary cache. This data is kept consistent through the use of write back methodology, that is, modified data is not written back to memory until the cache line is replaced and this obviously reduces the frequency of writing data into the main memory.

2.5.2 MIPS R4000 Cache Support and Brief Description

As shown in Figure 2-11, the R4000 contains separate primary instruction and data caches. It also shows that certain types of the R4000 supports a secondary cache (S-Cache) which can be split into two separate portions where one portion containing data and the other portion containing instructions. It is also possible to act as a joint cache, holding combined instructions and data [7].

Table 2-1 lists the cache and cache coherency support for the three types of R4000 models.

R4000 Model	Support Primary Cache?	Support Secondary Cache?	Support Cache Coherency?
R4000PC	Yes	No	No
R4000SC	Yes	Yes	No
R4000MC	Yes	Yes	Yes

Table 2-1: R4000 Cache and Coherency Support [7, pp. 246]

However, this project may only focus likely same as the R4000PC model which support only the primary cache. The block diagram of R4000PC is shown in Figure 2-12.

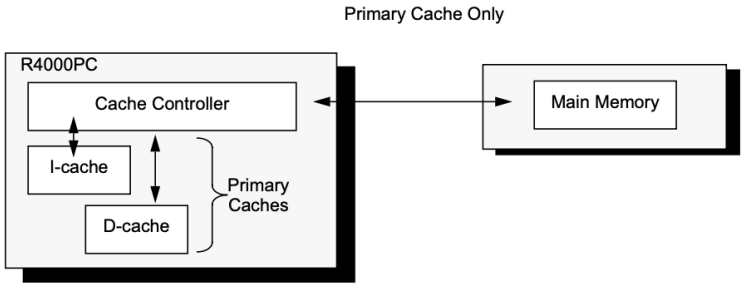

Figure 2-12: Cache Support in the R4000PC [7, pp. 247]

2.5.3 Organization of the Primary Data Cache (D-Cache) in R4000

Each line of primary D-cache data has an associated 29-bit tag that contains a 24-bit physical address, 2-bit cache line state, a write-back bit, a parity bit for the physical address and cache state fields, and a parity bit for the write-back bit. Byte parity is used on D-cache data. [7]

The R4000 processor primary D-cache has the following characteristics:

- write-back
- direct-mapped
- indexed with a virtual address
- checked with a physical tag
- organized with either a 4-word (16-byte) or 8-word (32-byte) cache line

Figure 2-13 shows the format of a 8-word (32-byte) primary D-cache line.

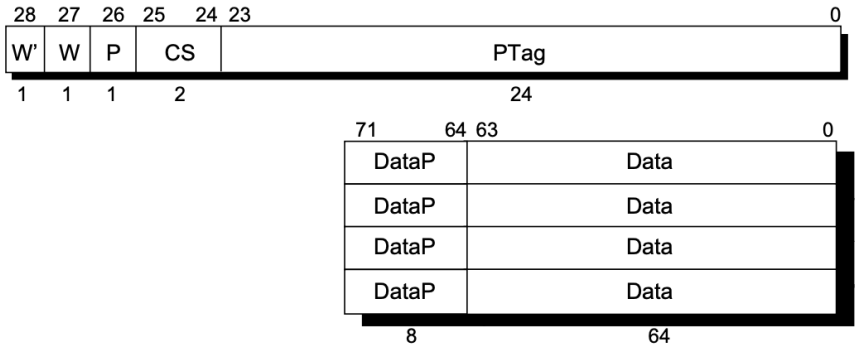

Figure 2-13: R4000 8-Word Primary D-Cache Line Format [7, pp. 249]

2.5.4 MIPS R4000 Cache Write Policy

The R4000 processor manages its primary and secondary caches by using the write-back policy. The written data is first stored into the caches, instead of writing it directly to memory. In the R4000 implementation, a modified cache line is not written back to memory until the cache line is replaced either in the course of satisfying a cache miss or during the execution of a Write-back cache instruction [7].

2.5.5 Cache Unit [2]

Cache is a small temporary data storage with faster speed compared to the SDRAM. It is placed between the processor and SDRAM to speed up the memory access process. A cache unit with write-back scheme has been modelled by Goh [2]. A write buffer is needed for the policy to store dirty block when there is a block replacement occur which is later written back to SDRAM later. This modelled cache can be used as the D-Cache in this project. Figure 2-14 shows the block diagram of cache unit modelled by Goh [2].

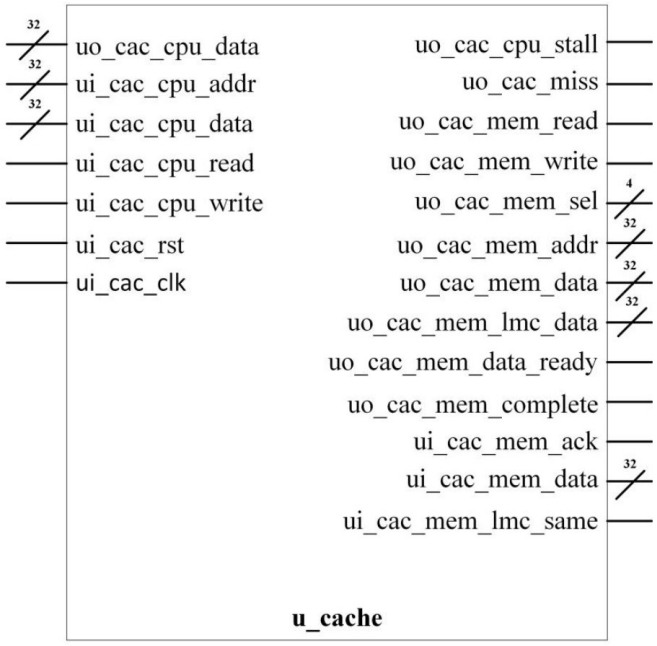

Figure 2-14: Block Diagram of Cache Unit [2]

2.5.6 Cache Scenario [2]

Basically, there are 4 scenarios might be happened on cache, we need to decide what to do when these scenarios happen.

1. Read Miss

- Receive physical address and instructions of read from the main controller of the CPU.
- Check validity and tag for the index of the physical address points to. A miss signal is produced due to either it is invalid, or the tag is different.
- Cache controller asserts strobe, cycle, and read signals to SDRAM controller to fetch new block of data.
- Meanwhile, the pipelines of the CPU are stalled.
- Check LRU to determine which slot is least recently used, store the newly fetched block of data in it.
- Set valid bit for the index pointed.
- Update LRU.
- Deassert the miss, strobe, cycle and read signal, the pipelines are un-stalled.

2. Read Hit

- Receive physical address and instruction of read from the main controller of CPU.
- Check validity and tag for index of the physical address points to.
- Miss signal is active low.
- Load the selected instruction or data by determining the byte offset to host.
- Update LRU.

3. Write Miss (For D-Cache only)

- Receive physical address, data, and instruction of write from the main controller of CPU.
- Check validity and tag for the index of the physical address points to.
- A miss signal is produced due to either it is invalid, or the tag is different.
- Stall the pipelines.
- Check LRU to determine which is least recently used.

- Cache controller asserts strobe, cycle, and read to SDRAM controller to access the data in SDRAM.
- If the block of data was dirty, send the block of 8 words back to SDRAM.
- Fetch new block of data from SDRAM.
- After the new block is updated from SDRAM, strobe, cycle, read and miss signals are deasserted.
- Perform the write.
- Update LRU.

4. Write Hit (For D-Cache only)

- Receive physical address, data, and instruction of write from main controller of CPU.
- Check validity of tag for index of the physical address points to. Miss
- signal is active low.
- Update the selected instruction or data.
- Update LRU.

2.6 UC Berkeley EECS Final Project - 8-Stage Deep-Pipelined MIPS Processor

In this project, Otto Chiu, Charles Choi, Teddy Lee, Man-Kit Leung, Bruce Wang designed an 8-stage Deep-Pipelined MIPS ISA Compatible Processor. Forwarding path and branch predictor is built to improve the processor performance. Other features include the unsigned multiply and division and the jump target predictor [10].

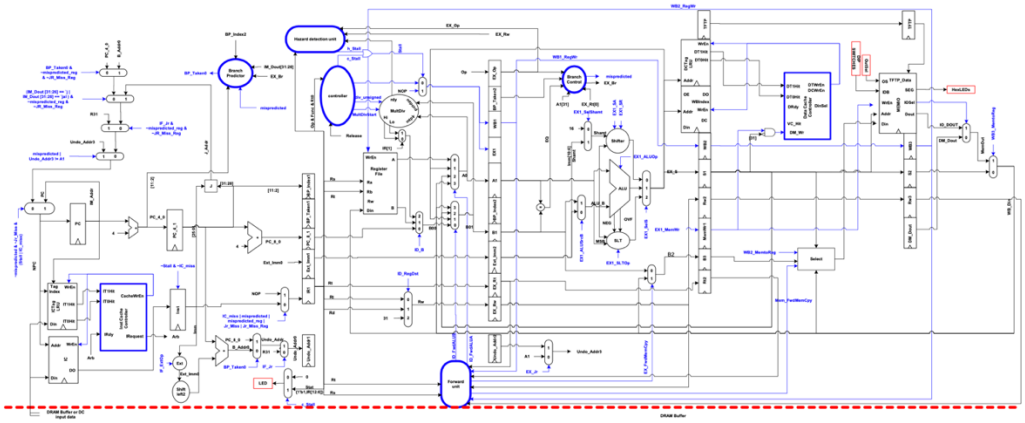

Figure 2-15: Berkeley EECS Final Project - Full Schematic of 8-stage Pipeline Processor [10]

The above is still not the main focus of the project. The highlight is the way they build and spilt the pipeline stages into 8 stages. In their project, as mentioned in the title, the processor is pipelined into 8 stages. The eight stages are as below:

- IF : Instruction Fetch
- PR : Predict and Register
- ID : Decode
- EX : Execute
- MR : Memory Read
- MW : Memory Write
- WB : Write Back
- FW : Forward (WB to ID)

The processor performance is improved due to the deeper pipeline introduced. However, from Figure 2-15, when we look through the pipeline by stages, we can actually notice that the logic may not be evenly distributed. This may lead to unmaximize performance

for the processor. The logic used at WB and FW stage is relevantly less compared to other stages.

As what is stated in the problem domain, the MEM stage of the basic 5-stage pipeline processor actually contributes to the longest timing delay, which we can say, it dragged the clock rate of the processor, thus, reduced the processor performance. The key solution is to balance the timing delay by evenly distribute the logics among the pipeline stages, for example, decompose and realign the pipeline stages that require longer delay into several clock cycles. Hence, the unmaximize performance of the processor is the weakness for this project.

2.7 Design of 6-stage Pipeline Processor [12]

Wen Jun's project is the upper part for this current project. Similar to this project, Wen Jun actually designs the 6-stage Pipeline Processor by improving the timing delay of the pipeline stages in the basic 5-stage pipeline processor [12]. In his project, the IF stage of the 5-stage pipeline is decomposed and realigned into 2 extra stages which is IF and IS stage. Primary Instruction Cache is implemented in his design to speed up the instruction memory access. However, due to time and manpower constraint, Wen Jun is unable to continue improving the MEM stage of the processor developing it into a 7-stage pipeline processor.

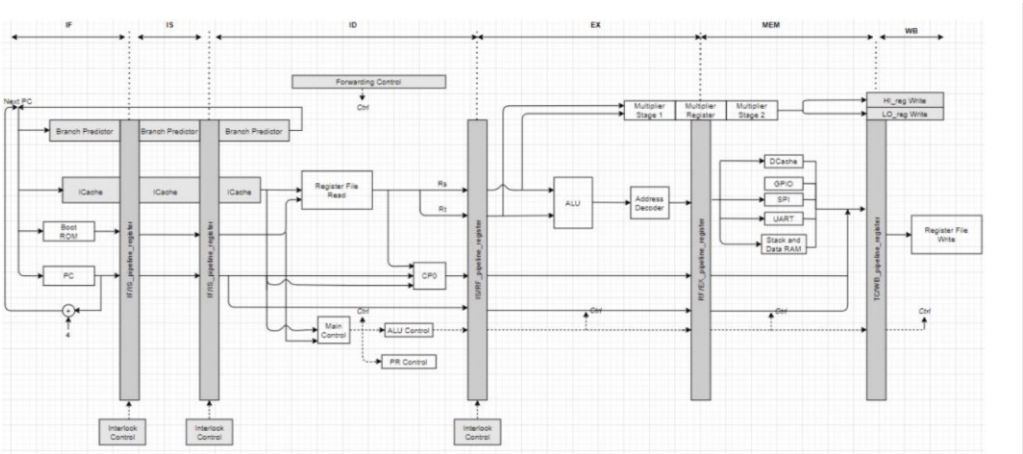

Figure 2-16: The Structural View of the 32-bits RISC 6-stage Pipeline Processor [12]

Chapter 3: Proposed Method / Approach

3.1 Proposed Solution

In order to shorten the timing delay of the memory access in the basic 5-stage pipeline processor, the 5-stage pipeline of the processor will be spilt into 7-stage pipeline. In this project, the MEM stage of the basic 5-stage pipeline processor is decomposed and realigned into 2 new stages in the 7-stage pipeline processor. Data cache (D-cache) is introduced and used for the data memory access to improve and increase the speed of data memory access significantly. Cache unit designed by seniors of UTAR Computer Engineering Course will be reviewed and utilized in this case. The D-Cache will be spilt into two separate stages with balanced logics to improve the overall timing delay of the processor. An extra stage is reserved for the TLB to be implemented in the future.

3.2 General Design Methodology and Work Procedures

Three types of design methodologies are available for the digital system design process. These three methodologies are as below:

I. Top-down design methodology
II. Bottom-up design methodology
III. Mixed design methodology

In this project, the top-down design methodology will be used to design and develop the 7-stage pipeline processor (MEM stages). By using the top-down design methodology, the top-level representation of the chip is first defined, followed by each lower-level representation based on several important criteria such as functionality and speed.

3.2.1 RTL Design Flow

The RTL design flow will be used throughout the whole project in designing and developing the 7-stage pipeline processor (MEM stages). Figure 3-1 shows the RTL design flow. In this project, the micro-architectural level design of the RTL design flow will be emphasized and focus more as the hardware to be designed for the MEM stages of the 7-stage pipeline processor is in unit level.

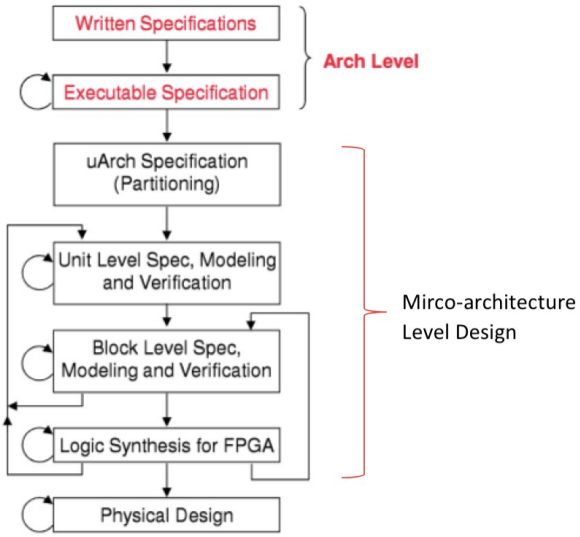

Figure 3-1: RTL Design Flow

3.2.2 Micro-architecture Specification

Micro-architecture specification will describe the internal design of the 7-stage pipeline processor (MEM stages). The internal design of the 7-stage pipeline processor (MEM stages) will be described with detailed design-specific technical information for the RTL coding. In this project, the unit level of the 7-stage pipeline processor (MEM stages) will include the following information:

- Functionality / Feature description
- Interfaces and I/O pin description
- Critical unit I/O timing and delay requirements
- Functional partitioning into blocks and inter-blocks signaling
- Test plan (focus on functional test)

3.2.3 RTL Modeling and Verification

After the microarchitecture specification is well developed, the RTL coding of the 7-stage pipeline processor (MEM stages) may begin. RTL models at each level are verified for functional correctness after the RTL coding is done. During the project development, the design flow should be done and repeated until the 7-stage pipeline processor (MEM stage) designed and built meet all the specific functional requirements. Once the RTL models are successfully built and meet all the specified requirements and specifications, logic synthesis should be carried out on the targeted technology which is the FPGA technology in this project.

3.2.4 Logic Synthesis for FPGA

After the 7-stage pipeline processor has been functionally verified, the model is said to be ready for logic synthesis. Logic synthesis is the process of converting the RTL coding into an optimized gate level representation (a netlist). Based on the logic synthesis result, the gate level netlist is verified again for functional correctness. If it can successfully meet all the necessary specifications, the gate level netlist is now ready for physical design. However, if it cannot meet the required specifications, depending on the severity, corrections need to be made accordingly to the gate level netlist, the RTL models or the microarchitecture.

3.3 Research Methodology of the Project

Phase 1: Study and research the basic 5-stage pipeline processor.

In this phase, the pipeline microarchitecture of the basic 5-stage processor will be studied. The weakness of the basic 5-stage pipeline processor is focused and should be improved after this project is done. MIPS R4000 ISA will be used as the study case in this project. Besides, some senior's work will also be reviewed in this project. For example, the 32-bit RISC 5-stage pipeline microprocessor microarchitecture will aid this project a lot [13]. Figure 3-2 show the 32-bit RISC 5-stage pipeline microprocessor microarchitecture drawn by Kiat [14].

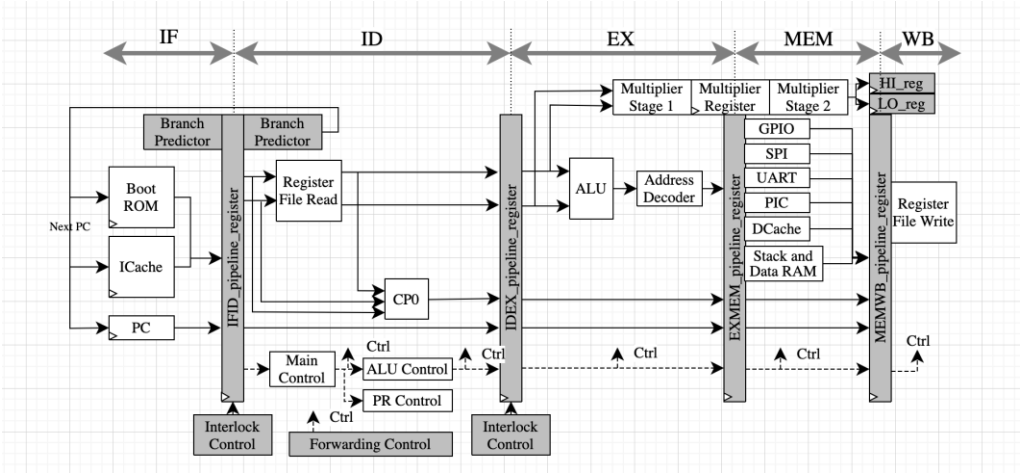

Figure 3-2: The RISC32 5-stage pipeline microprocessor microarchitecture [14]

Phase 2: Gather requirement data

Deep pipelining

In this phase, the pipeline microarchitecture of the 8-stage deep-pipelined processor will be studied. The Final Project 1 from EECS, UC Berkeley will be reviewed in detail and is used as the guidance for this project. The weakness of the project mentioned should also be identified and improved in this project. Other than that, the MIPS R4000 processor from the industry will also be reviewed.

Caching

D-Cache will be used to improve the speed of data memory access for the 7-stage pipeline processor designed in this project. The cache units designed and modelled in FICT, UTAR Computer Engineering program will be reviewed and modified to be utilized in this project [2].

Phase 3: Design and Implementation

The MEM stage of the basic 5-stage pipeline processor will be spilt into 2 phases which are DF and TC stage in the 7-stage pipeline processor. Instead of only one memory block, D-Cache and flash memory are implemented in the 7-stage pipeline processor. D-cache unit will be decomposed and pipelined into 2 separate stages.

D-cache

For data load, the data stored in the data memory with the memory address specified by the ALU will be loaded to the register file block. If the memory address specified is found in the cache and read immediately in only one clock cycle, it is called read hit, otherwise, it is called read miss. The processor pipeline will be stalled to allow the data of that particular memory address to be transferred into the cache first, then just read by the processor. After all, the processor pipeline will resume full run state.

For data store, the output of the register file will be stored to the data memory with the memory address specified by the ALU. If the memory address specified is found in the cache, it is called write hit and the data would be written to the cache and write back to the data memory based on the write policy set. In other hand, it is called write miss. The processor pipeline will be stalled to allow the data of that particular memory address to be transferred into the cache. The memory address is now found on the cache and is ready to be overwritten with new value. After all, the processor pipeline will resume full run state.

The process from checking the presence of the memory address in the cache till the reading or writing of data requires several clock cycles. This insists that decomposing of cache units modelled by seniors is required so that the cache unit would function optimally following the processor pipeline execution cycle.

Cache Controller

As the D-cache unit is decomposed into 2 separate stages, the cache controller needs to be modified. All the states in the cache controller are reviewed and analyzed in order to be modified so that the control signals could synchronized with the D-Cache pipeline stages. Besides, the new cache controller will be implemented using Registered Mealy Machine instead of Moore or Mealy Machine.

Pipelining

The datapath unit is also decomposed into 7-stage. In this project, the stage affected would be the existing MEM stages in the 5-stage or 6-stage pipeline processor. It is then decomposed into 2 stages which will be known as DF and TC stage that is similar to the pipelined D-Cache. Besides, due to the increment in pipeline stages introduced and in order to stall the processor pipeline during the cache miss, the forwarding block and interlock block of the processor requires modification. The control path unit requires modification too so that the control signals are connected to respective stages correctly.

After the microarchitecture specification is well developed, the RTL coding of the 7-stage pipeline processor will also be done in this stage.

Phase 4: Logic Synthesis of FPGA

The RTL coding from the previous phase is converted into an optimized gate level representation (a netlist). Based on the logic synthesis result, the gate level netlist is verified again for functional correctness. If it can successfully meet all the necessary specifications, the gate level netlist is now ready for physical design.

3.4 Design Tools

Each stage of the design jobs requires the use of appropriate design tools to help to automate the design work. Hence, there exist Electronic Design Automation (EDA) tools for digital system design work at each particular level of abstraction. Since Verilog Hardware Descriptive Language (HDL) will be used to design the RTL model of the 7-stage pipeline processor, hence, a Verilog simulator is definitely needed to emulate the Verilog HDL.

Some of the Verilog simulator is shown in Table 3-1 and comparison are made.

Simulator	Incisive Enterprise Simulator	ModelSim	VCS
Company	cadence	Mentor Graphics	SYNOPSYS® Predictable Success
Language Supported	• VHDL-2002 • V2001 • SV2005	• VHDL-2002 • V2001 • SV2005	• VHDL-2002 • V2001 • SV2005
Platform supported	• Sun-solaris • Linux	• Windows OS • Linux	• Linux
Availability for free?	✗	✓ (SE edition only)	✗

Table 3-1: Comparison among Verilog Simulator

Based on the comparison above, it is clear that the ModelSim from Mentor Graphic is the best choice among others to be chosen and used as the design tool for this project as it offers a free license for Student Edition version. Even though there is still certain degree of limitations on the ModelSim Student Edition version, it is adequate to be used for this project. In addition, it is considered lightweight compared to the rest simulator.

In terms of the synthesis tools, there are a lot of logic synthesis tools targeting FPGA in the market. Among all of them, Xilinx Vivado Design Suite is selected for this project

as it is able to support the FPGA that we have in UTAR and the most important is it is freely available in UTAR.

3.4.1 ModelSim PE Student Edition 10.5

ModelSim from Mentor Graphic is the industry-leading simulation and debugging environment for HDL-based design in which its license can be obtained freely by a student. The student version of the ModelSim is sufficient to be used for Verilog design stimulation in this project. Furthermore, ModelSim supports the Verilog and VHDL languages. This stimulator is also able to provide syntax error checking and waveform simulation which play an important part in developing the project. The timing diagrams and the waveforms are very useful in verifying the model functionalities after writing the testbench.

3.4.2 PCSpim

PCSpim is a Windows-based software stimulator that loads and executes assembly language program for the MIPS RISC microarchitecture. It provides a simple assembler, debugger and a set of operating services, thus, it is used for developing the MIPS test program for functional verification in this project.

3.4.3 Xilinx Vivado Design Suite

Xilinx Vivado Design Suite is a software designed for synthesis and analysis of HDL designs which enables the developers to synthesize their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer easily.

3.5 Technologies Involved

3.5.1 Field Programmable Gate Array (FPGA)

As what is mentioned, the logic synthesis of the 7-stage pipeline processor will be eventually carried out on the FPGA technology. The FPGA technology is actually an integrated circuit (IC) that is programmable in the field after manufacture. FPGAs have been used widely by engineers in the design of specialized integrated circuits that can be later produced hard-wired in large qualities for distribution to computer manufacturers and end users. It is commonly selected for prototype development due to its benefits of cost efficiency, high flexibility and good scalability when compared to the other technologies.

3.6 Implementation Issues and Challenges

This project tends to improve the timing delay for each pipeline stage of the existing 32-bits RISC pipeline processor. Additional pipeline stages are inserted at suitable position to obtain a lower timing delay for each stage, thus, increase the overall performance of the pipeline processor. However, inserting additional pipeline stages requires modification on some functional units and block like control path unit, interlock block, and forwarding block to ensure its functional robustness. It is necessary to study the whole existing pipeline processor before starting to work on it. Moreover, some RTL modelling of the existing pipeline processor are lack of complete documentations which requires hard work to identify their function based on solely the Verilog model.

3.7 Timeline

3.7.1 Gantt Chart for Project I

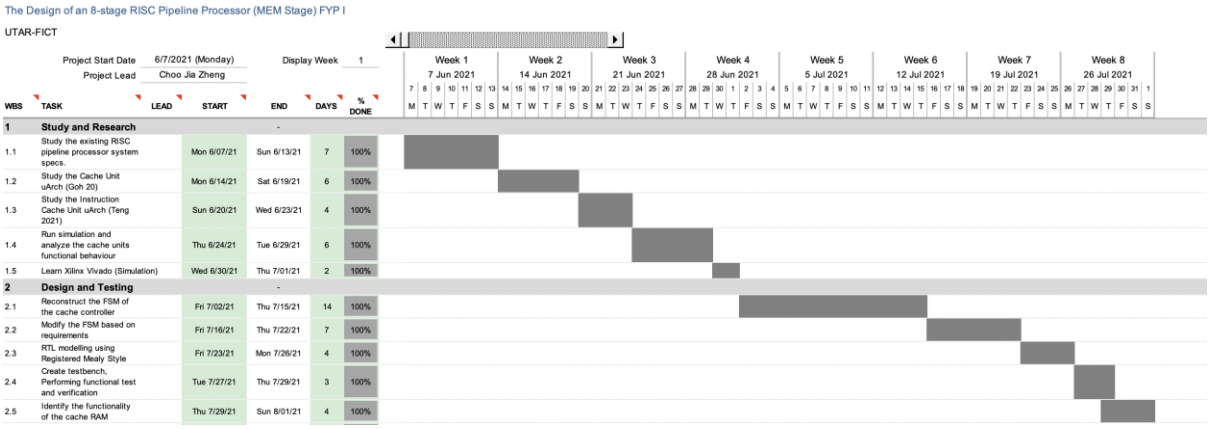

Figure 3-3: Gantt Chart I for Project I

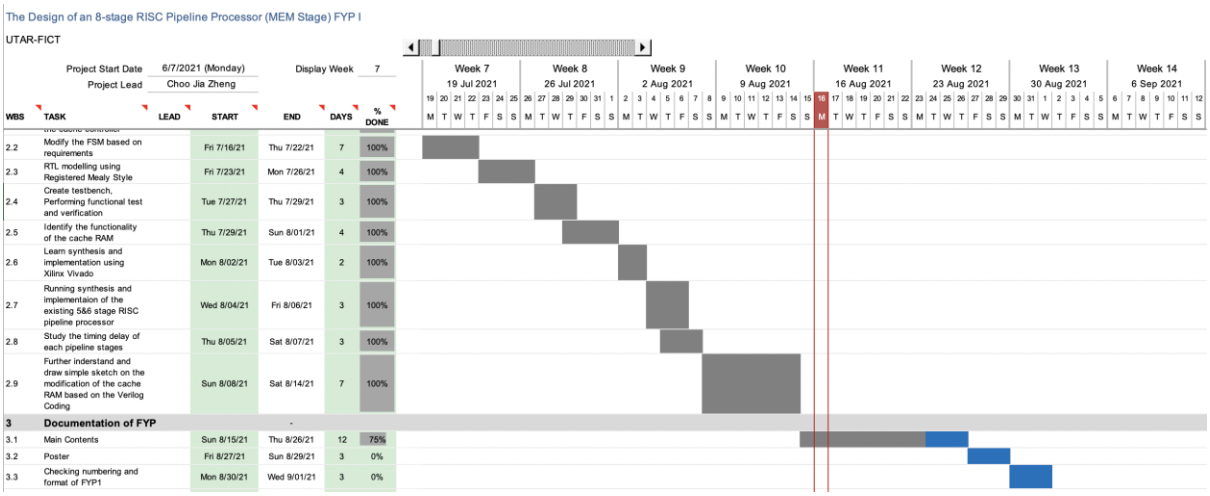

Figure 3-4: Gantt Chart II for Project I

3.7.2 Gantt Chart for Project II

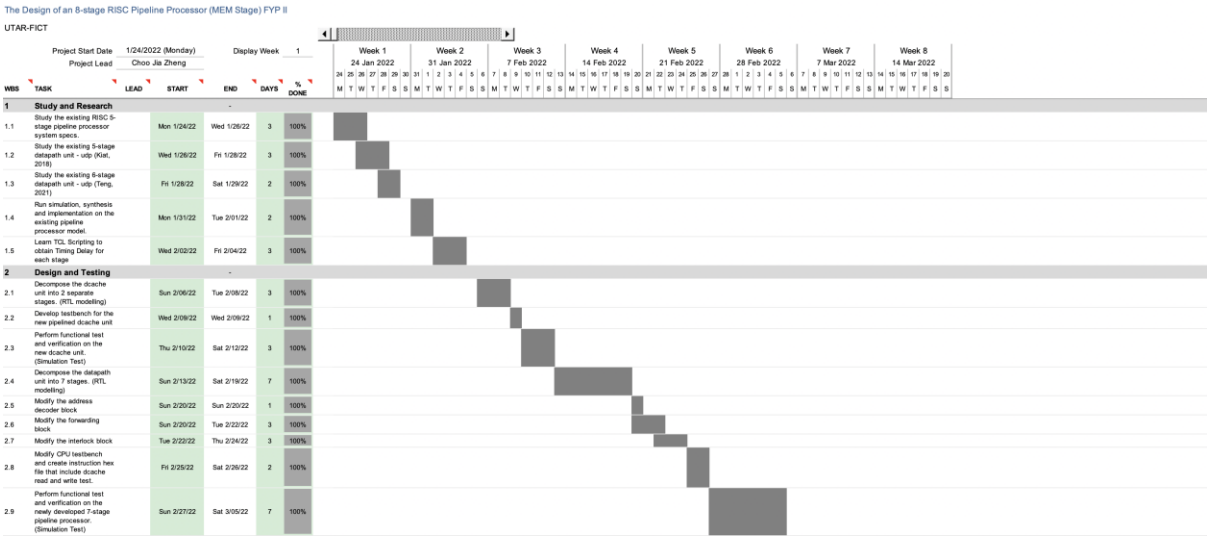

Figure 3-5: Gantt Chart I for Project II

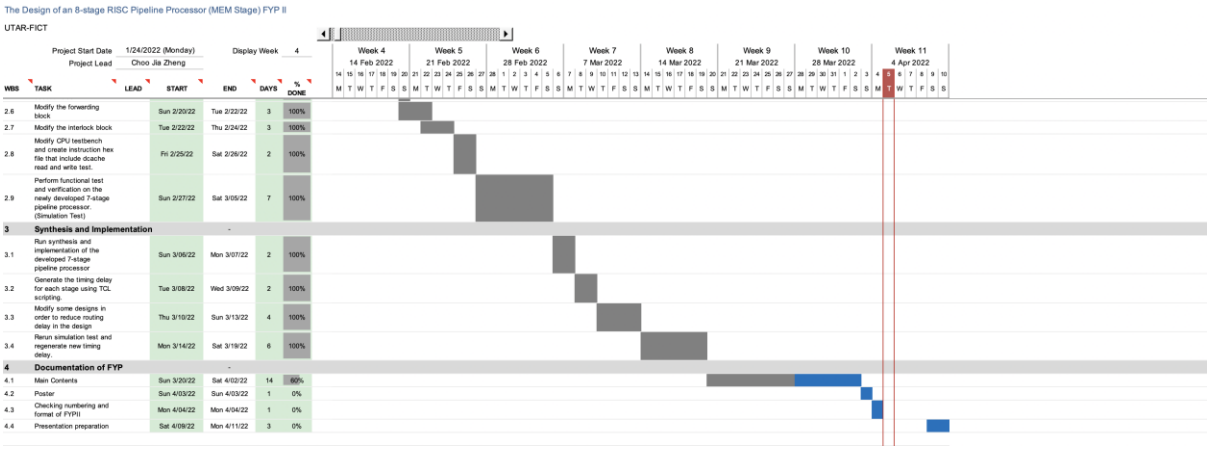

Figure 3-6: Gantt Chart II for Project II

Chapter 4: System Specification

4.1 System Overview

The 7-stage pipelined processor is built based on the existing 5-stage pipelined processor developed by seniors from FICT, UTAR. A 6-stage pipelined processor is built by Teng Wen Jun by decomposing and pipelining the I-Cache and branch predictor in IF stage into three separate stages [12]. In this project, the D-Cache will be decomposed and pipelined into two separate stages, which produces a 7-stage pipelined processor in the end.

4.2 System Design and Specification

The 7-stage pipelined processor made up of three main parts, which is the Central Processing Unit (CPU), memory system and input/output (I/O) system [13]. The developed processor is compatible to the 32-bits MIPS ISA. 49 instructions, covering arithmetic instructions, logical instructions, data transfer instruction, program control instruction and system instruction classes. Next, two-level memory hierarchy is developed for its memory system. The first level memory consists of caches, which are I-Cache and D-Cache, Boot ROM, and Data and Stack RAM. The second level memory consists of the flash memory. Besides, the I/O system of this processor consists of GPIO controller, SPI controller and UART controller which is used for data transfer with other communication devices. The priority interrupt controller works with the coprocessor 0 (cp0) and is mended to deal with multiple interrupt raised at the same time based on the priority level set for various exceptions. A branch predictor is also implemented to improve the performance of the processor. Figure 4-1 in the next page shows the architectural overview of the 32-bits RISC 7-stage pipeline processor.

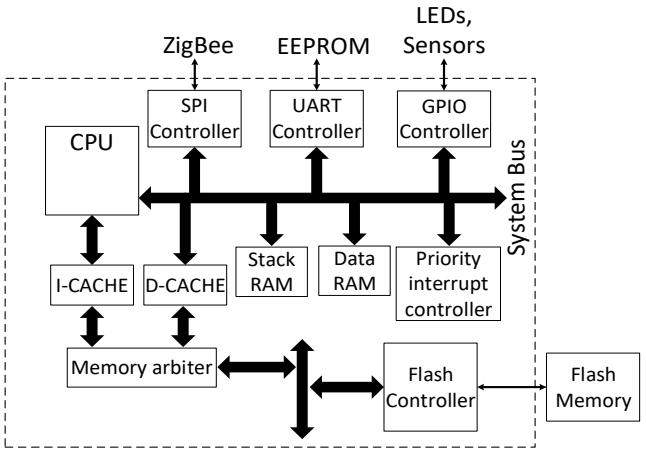

Figure 4-1: Architectural Overview of the RISC32 Processor [14]

Table 4-1 below shows the 7-stage pipeline processor specifications in detail.

		Pipeline
Frequency (MHz)		50
Instruction's cycle		7, overlapping
Branch predictor		64 entries 4 ways associative
Common features (Static Region)	Memory	4kBytes boot ROM, 128kBytes user access flash, 8kBytes RAM (Data & Stack), 1kBytes I-cache, 1kBytes D-cache, 512Bytes Memory Mapped I/O Register
	Communication interface	UART, SPI, 32 GPIO pins
Partial Bitstream start address		0x00A8_0000
Bitstream size		1,404,992 bits / 43906 words
FPGA board		Artix-7: Arty A7 (XC7A100T)
FPGA Resources (Overall)	LUT	8266
	LUTRAM	315
	FF	5643
	BRAM	3.50
	IO	46
	BUFG	1

Table 4-1**:** 32-bits RISC 7-stage Pipeline Processor Specifications

4.2.1 32-bits RISC 7-stage Pipeline Processor Design Hierarchy

Table 4-2 shows the 7-stage pipeline processor design hierarchy. The processor developed is classified into 4 main levels, which are chip level, unit level, block level, and sub-block level.

Chip Level	Unit Level	Block Level	Sub-block Level
Processor chip (crisc3)	Data Path unit (udata_path7)	Branch Predictor block (bbp_4way)	
		Register file block (b_rf)	
		Forward control block (bfw_ctrl3)	
		Interlock control block (bitl_ctrl_v2)	
		Co-processor 0 block (b_cp0)	
		Arithmetic Logic block (b_alb)	
		Multiplier block (b_mult)	adder_lvl1
			adder_lvl2
			adder_lvl3
			adder_lvl4
			adder_lvl5
			adder_lvl1_firstrow
			add_lvl1_lastrow
			adder_lvl2_lastrow
			sub_lvl1_lastrow
		Address decoder block	

		(baddr_decoder_v2)	
	Control path unit (uctrl_path)	ALB Control block (balb_ctrl)	
		Main Control block (bmain_ctrl)	
	Instruction Cache unit (upipelined_cache)	Cache Controller block (bcache_ctrl_v5)	
		Cache RAM block (bcache_ram)	
		FIFO Controller block (bfifo_ctrl)	
		FIFO block (bfifo)	
	Data Cache unit (upipelined_cache2)	Cache Controller block (bcache_ctrl_v6)	
		Cache RAM block (bcache_ram)	
		FIFO Controller block (bfifo_ctrl)	
		FIFO block (bfifo)	
	Flash Controller unit (ufc)	FIFO block (bfc_FIFO)	
		Flash Controller FSM block (bfc_fsm)	

		Flash Controller Clock Generator block (bfc_clk_gen)	
		Flash Controller Transmitter block (bfcTX)	
		Flash Controller Receiver block (bfcRX)	
	UART Controller unit (uuart_v2)	UART Transmitter block (btx)	
		UART Receiver block (brx)	
		UART Baud Clock Generator block (bclkctr)	
	SPI Controller unit	SPI Clock Generator block (bspiclk_gen)	
		Receiver block (bspiRX)	
		Transmitter block (bspiTX)	
		SPI I/O control block (bspiIO_ctrl)	
		FIFO block (bFIFO)	
	GPIO Controller (ugpio_v2)		
	Data RAM (uram)		

	Boot ROM (uboot_rom)		
	Programmable Interrupt Controller unit (upi_ctrl_v2)	Priority resolver block (bpic_resolver)	
	Memory Arbiter unit (umem_arbiter)		

Table 4-2: 7-stage Pipeline Processor Design Hierarchy

4.2.2 Microarchitecture of 32-bits RISC 7-stage Pipeline Processor

The 32-bits RISC pipeline processor developed consists of 7 hardware stages, which are Instruction Fetch-First stage (IF), Instruction Fetch-Second stage (IS), Register Fetch Stage (RF), Execution Stage (EX), Data Fetch Stage (DF), Tag Check Stage (TC) and Write Back Stage (WB). Hardware components are allocated in respective stage. A total of seven clock cycles is needed for a single instruction to complete its execution. Figure 4-2 below shows the functional view of the 7-stage pipeline processor.

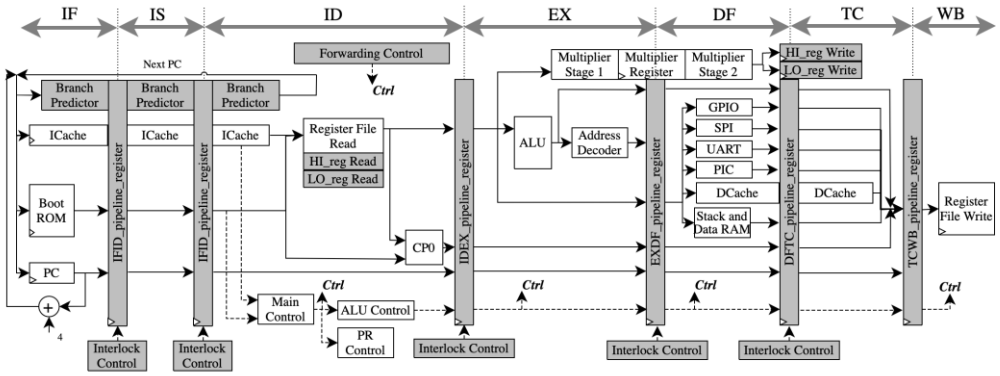

Figure 4-2: The Structural View of the 32-bits RISC 7-stage Pipeline Processor

4.2.3 Memory Map

The virtual and physical addresses are used in the implementation of memory space of the 7-stage pipelined processor. The virtual address is used for the purpose to access program instruction and data; The physical addresses is used for the purpose to allocate physical memory in flash memory, Data and Stack RAM and boot ROM. Figure 4-3 shows the memory map of the 32-bits RISC pipeline processor.

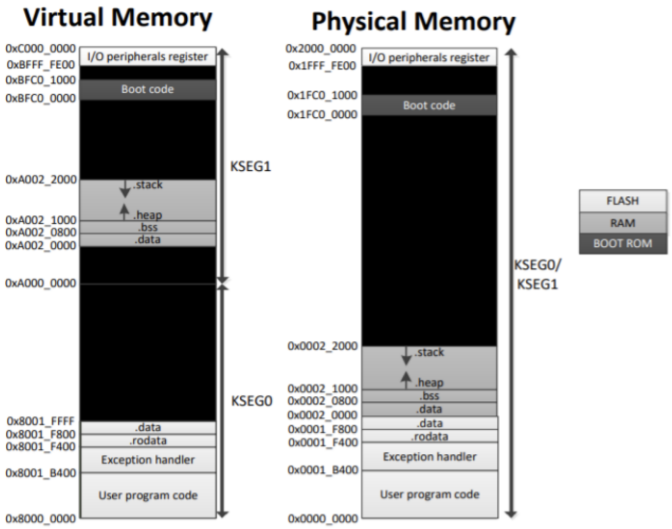

Figure 4-3: Memory Map of the 32-bits RISC pipeline processor [13]

Table 4-3 discussed the use of various memory allocation.

Memory Usage	Description	Memory Size
I/O peripheral register	Used as the memory-mapped registers for I/O peripheral controllers.	512 bytes
Boot code	Used to store bootloader program code for initial system configuration when powered on.	4k bytes
Stack	Used by procedure during execution to store register values.	8k bytes
Heap	Used to hold variables declared dynamically.	
Exception handler	Used to store the exception handler codes.	16k bytes
User program code	Used to store user program codes	128k bytes

Table 4-3: Memory Map Description [13]

4.3 32-bits RISC 7-stage Pipeline Processor Chip Interface

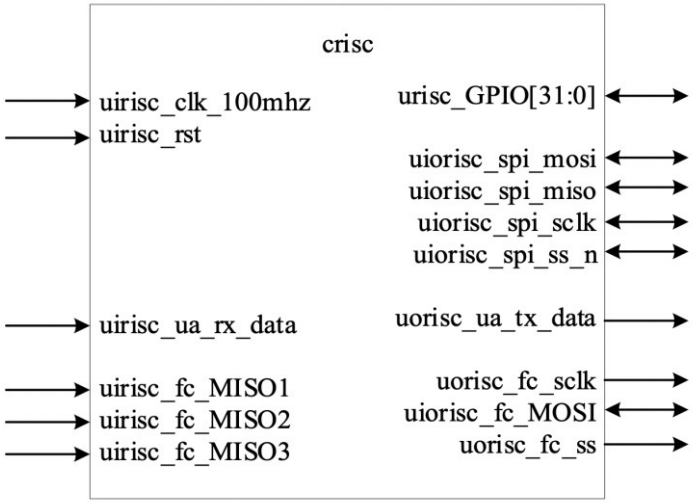

Figure 4-4: Chip Interface of the 32-bits RISC 7-stage Pipeline Processor

4.4 Pin Description of the 32-bits RISC 7-stage Pipeline Processor

4.4.1 Input Pin Description

Pin Name	**:**	uirisc_clk_100 mhz	**Pin Class**	**:**	Global	**Pin Size**	**:** 1 bit
Source to Destination	**:**	External ➔ crisc					
Pin Function	**:**	To synchronize the signals in the pipeline processor					
Pin Name	**:**	uirisc_rst	**Pin Class**	**:**	Global	**Pin Size**	**:** 1 bit
Source to Destination	**:**	External ➔ crisc					
Pin Function	**:**	To reset the pipeline processor					
Pin Name	**:**	uirisc_ua_rx_da ta	**Pin Class**	**:**	Data	**Pin Size**	**:** 1 bit
Source to Destination	**:**	External UART➔ crisc					
Pin Function	**:**	UART standard pin: To receive UART serial data					
Pin Name	**:**	uirisc_fc_MISO 1	**Pin Class**	**:**	Data	**Pin Size**	**:** 1 bit
Source to Destination	**:**	Flash memory ➔ crisc					
Pin Function	**:**	SPI protocol serial pin					
Pin Name	**:**	uirisc_fc_MISO 2	**Pin Class**	**:**	Data	**Pin Size**	**:** 1 bit
Source to Destination	**:**	Flash memory ➔ crisc					
Pin Function	**:**	SPI protocol serial pin					

Pin Name	**:**	uirisc_fc_MISO 3	**Pin Class**	**:**	Data	**Pin Size**	**:** 1 bit
Source to Destination	**:**	Flash memory ➔ crisc					
Pin Function	**:**	SPI protocol serial pin					

Table 4-4: 32-bits RISC 7-stage Pipeline Processor Input Pin Description

4.4.2 Output Pin Description

Pin Name	**:**	uorisc_ua_tx_da ta	**Pin Class**	**:**	Data	**Pin Size**	**:** 1 bit
Source to Destination	**:**	External ➔ crisc					
Pin Function	**:**	UART standard pin: To transmit UART serial data					
Pin Name	**:**	uorisc_fc_sclk	**Pin Class**	**:**	Data	**Pin Size**	**:** 1 bit
Source to Destination	**:**	External ➔ crisc					
Pin Function	**:**	SPI protocol serial clock signal					
Pin Name	**:**	uorisc_fc_ss	**Pin Class**	**:**	Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	External UART➔ crisc					
Pin Function	**:**	To select slaves for SPI protocol					

Table 4-5: 32-bits RISC 7-stage Pipeline Processor Output Pin Description

4.4.3 Bidirectional Pin Description

Pin Name	**:**	urisc_GPIO	**Pin Class**	**:**	Data	**Pin Size**	**:** 32 bits
Source and Destination	**:**	External devices ⇔ crisc					
Pin Function	**:**	GPIO pins					
Pin Name	**:**	uiorisc_spi_mosi	**Pin Class**	**:**	Data	**Pin Size**	**:** 1 bit
Source and Destination	**:**	External SPI ⇔ crisc					
Pin Function	**:**	SPI standard pin: Master Out Slave In (MOSI). The pin acts as an output pin when crisc is configured as master, else otherwise.					
Pin Name	**:**	uiorisc_spi_miso	**Pin Class**	**:**	Data	**Pin Size**	**:** 1 bit
Source and Destination	**:**	External SPI ⇔ crisc					
Pin Function	**:**	SPI standard pin: Master In Slave Out (MISO). The pin acts as an input pin when crisc is configured as master, else otherwise.					
Pin Name	**:**	uiorisc_spi_sclk	**Pin Class**	**:**	Control	**Pin Size**	**:** 1 bit
Source and Destination	**:**	External SPI ⇔ crisc					
Pin Function	**:**	SPI standard pin: Serial Clock Signal. Used for data synchronization. The pin acts as an output pin when crisc is configured as master, else otherwise.					

Pin Name	**:**	uiorisc_spi_ss_n	**Pin Class**	**:**	Control	**Pin Size**	**:** 1 bit
Source and Destination	**:**	External SPI ⇔ crisc					
Pin Function	**:**	SPI standard pin: Slave Select Control Signal. The pin acts as output pin when crisc is configured as master, else otherwise.					
Pin Name	**:**	uiorisc_fc_MOSI	**Pin Class**	**:**	Data	**Pin Size**	**:** 1 bit
Source and Destination	**:**	Flash memory ⇔ crisc					
Pin Function	**:**	SPI protocol bidirectional pin					

Table 4-6: 32-bits RISC 7-stage Pipeline Processor Bidirectional Pin Description

Chapter 5: Microarchitecture Specification

5.1 Pipelined Cache Unit (D-Cache)

5.1.1 D-Cache Functionality

- Increase and improve the speed of memory access by storing a small fraction of data from the main memory.
- Output desired data to the processor when it issues a READ instruction.
- Write data into desired location as instructed by the processor.
- Stall the pipeline of the processor when READ MISS or WRITE MISS occur.
- Check with FIFO block or communicate with the flash memory controller to fetch new block of data when READ MISS or WRITE MISS occur.

5.1.2 Pipelined Cache Unit Block Diagram

Figure 5-1 below shows the block diagram of the Pipelined Cache Unit.

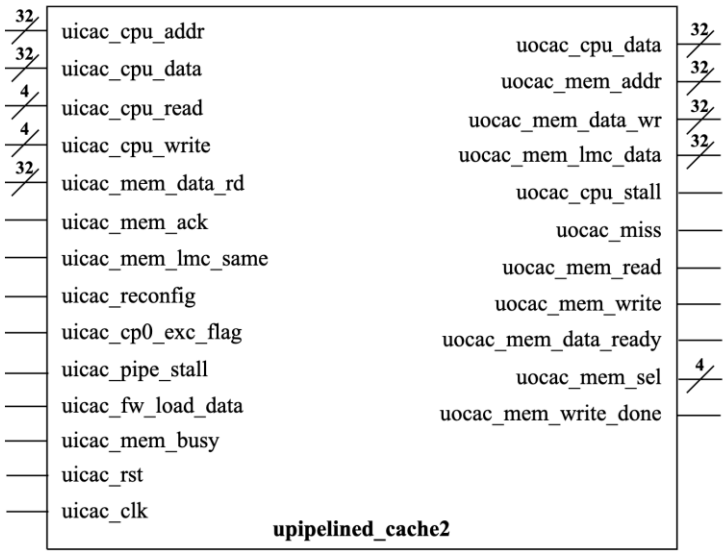

Figure 5-1: Block diagram of Pipelined Cache Unit

5.1.3 Pin Description of the Pipelined Cache

Input Pin Description

Pin Name	**:**	uicac_clk	**Pin Class**	**:**	Global	**Pin Size**	**:** 1 bit
Source to Destination	**:**	External ➔ upipelined_cache2					
Pin Function	**:**	To synchronize the signals in the pipeline cache					
Pin Name	**:**	uicac_rst	**Pin Class**	**:**	Global	**Pin Size**	**:** 1 bit
Source to Destination	**:**	External ➔ upipelined_cache2					
Pin Function	**:**	To reset the pipeline cache					
Pin Name	**:**	uicac_cpu_addr	**Pin Class**	**:**	Addr.	**Pin Size**	**:** 32 bits
Source to Destination	**:**	udp ➔ upipelined_cache2					
Pin Function	**:**	Address to be used to access the cache RAM					
Pin Name	**:**	uicac_cpu_data	**Pin Class**	**:**	Data	**Pin Size**	**:** 32 bits
Source to Destination	**:**	udp ➔ upipelined_cache2					
Pin Function	**:**	Data to be written into the cache RAM					
Pin Name	**:**	uicac_cpu_read	**Pin Class**	**:**	Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	uctrl_path ➔ upipelined_cache2					
Pin Function	**:**	Enable read from cache RAM					
Pin Name	**:**	uicac_cpu_write	**Pin Class**	**:**	Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	uctrl_path ➔ upipelined_cache2					
Pin Function	**:**	Enable write to cache RAM					
Pin Name	**:**	uicac_mem_ack	**Pin Class**	**:**	Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	umem_arbiter ➔ upipelined_cache2					
Pin Function	**:**	To acknowledge status of the flash memory. HIGH: Data from flash memory is ready. LOW: Flash memory is ready to receive data.					
Pin Name	**:**	uicac_mem_data_rd	**Pin Class**	**:**	Data	**Pin Size**	**:** 32 bits
Source to Destination	**:**	Flash memory ➔ umem_arbiter ➔ upipelined_cache2					
Pin Function	**:**	Carries data read from flash memory					
Pin Name	**:**	uicac_mem_lmc_same	**Pin Class**	**:**	Status	**Pin Size**	**:** 1 bit
Source to Destination	**:**	umem_arbiter ➔ upipelined_cache2					
Pin Function	**:**	Indicates the configuration of flash memory is same when HIGH.					
Pin Name	**:**	uicac_reconfig	**Pin Class**	**:**	Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	ufc ➔ upipelined_cache2					
Pin Function	**:**	Stop the cache operation for reconfiguration purpose when HIGH.					
Pin Name	**:**	uicac_cp0_exc_flag	**Pin Class**	**:**	Control	**Pin Size**	**:** 1 bit

Source to Destination	**:**	udp ➔ upipelined_cache2
Pin Function	**:**	Stall the cache pipelines when exception occurs.
Pin Name	**:**	uicac_pipe_stall **Pin Class :** Control **Pin Size :** 1 bit
Source to Destination	**:**	udp ➔ upipelined_cache2
Pin Function	**:**	Stall the cache pipelines.
Pin Name	**:**	uicac_fw_load_data **Pin Class :** Control **Pin Size :** 1 bit
Source to Destination	**:**	bfw_ctrl3 ➔ udp ➔ upipelined_cache2
Pin Function	**:**	Indicates the forwarding of cache ram loaded data from TC to DF stage.
Pin Name	**:**	ui_cac_mem_busy **Pin Class :** Control **Pin Size :** 1 bit
Source to Destination	**:**	ufc ➔ upipelined_cache2
Pin Function	**:**	Indicates flash memory is busy when HIGH.

Table 5-1: Pipelined Cache Input Pin Description

Output Pin Description

Pin Name	**:**	uocac_cpu_data **Pin Class :** Data **Pin Size :** 32 bits
Source to Destination	**:**	upipelined_cache2 ➔ udp
Pin Function	**:**	Data or instruction from cache RAM output to the processor.
Pin Name	**:**	uocac_cpu_stall **Pin Class :** Control **Pin Size :** 1 bit
Source to Destination	**:**	upipelined_cache ➔ udp
Pin Function	**:**	Stall the processor stage pipelines when CACHE MISS.
Pin Name	**:**	uocac_miss **Pin Class :** Status **Pin Size :** 1 bit
Source to Destination	**:**	upipelined_cache ➔ umem_arbiter
Pin Function	**:**	Indicates cache miss to the memory arbiter.
Pin Name	**:**	uocac_mem_write **Pin Class :** Control **Pin Size :** 1 bit
Source to Destination	**:**	upipelined_cache ➔ umem_arbiter
Pin Function	**:**	Send a write signal to write data into the flash memory.
Pin Name	**:**	uocac_mem_read **Pin Class :** Control **Pin Size :** 1 bit
Source to Destination	**:**	upipelined_cache ➔ umem_arbiter
Pin Function	**:**	Send a read signal to read data from the flash memory.
Pin Name	**:**	uocac_mem_sel **Pin Class :** Control **Pin Size :** 4 bits
Source to Destination	**:**	upipelined_cache ➔ umem_arbiter
Pin Function	**:**	To mask the 32 bits data.

Pin Name	**:**	uocac_mem_addr	**Pin Class**	**:**	Addr.	**Pin Size**	**:** 32 bits
Source to Destination	**:**	upipelined_cache ➔ umem_arbiter					
Pin Function	**:**	Address to be used to access the flash memory location.					
Pin Name	**:**	uocac_mem_data_wr	**Pin Class**	**:**	Data	**Pin Size**	**:** 32 bits
Source to Destination	**:**	upipelined_cache ➔ umem_arbiter					
Pin Function	**:**	Data to be written into the flash memory.					
Pin Name	**:**	uocac_mem_lmc_data	**Pin Class**	**:**	Global	**Pin Size**	**:** 32 bits
Source to Destination	**:**	upipelined_cache ➔ umem_arbiter					
Pin Function	**:**	To configure the flash memory					
Pin Name	**:**	uocac_mem_data_ready	**Pin Class**	**:**	Global	**Pin Size**	**:** 1 bit
Source to Destination	**:**	upipelined_cache ➔ umem_arbiter					
Pin Function	**:**	To indicates that data is ready to be written back from FIFO to the flash memory.					
Pin Name	**:**	uocac_mem_write_done	**Pin Class**	**:**	Global	**Pin Size**	**:** 1 bit
Source to Destination	**:**	upipelined_cache ➔ umem_arbiter					
Pin Function	**:**	To indicate that one block of data is written into the flash memory.					

Table 5-2: Pipelined Cache Output Pin Description

5.2 Cache Controller

5.2.1 Cache Controller Functionality

- Control the main activity in the pipelined cache unit.
- Output desired data when READ HIT.
- Update data when WRITE HIT.
- Read data from flash memory to cache RAM when CACHE MISS.
- Output control and status signal to write data back from FIFO to cache RAM.
- Output control and status signal to evict dirty data from cache RAM to FIFO.
- Output control and status signal to processor pipelines and flash memory.

5.2.2 Cache Controller Block Diagram

Figure 5-5 below shows the block diagram of the cache controller.

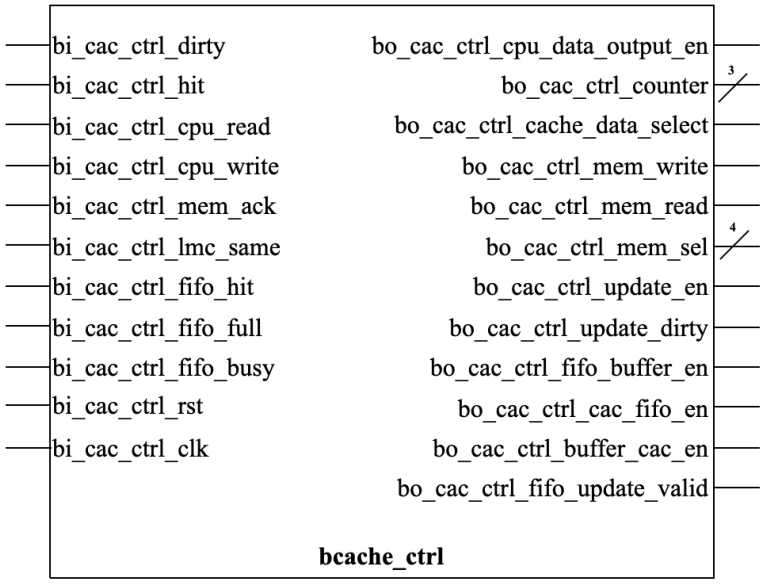

Figure 5-2: Block diagram of Cache Controller

5.2.3 Pin Description of the Cache Controller

Input Pin Description

Pin Name	**:**	bicac_ctrl_clk	**Pin Class**	**:** Global	**Pin Size**	**:** 1 bit
Source to Destination	**:**	External ➔ upipelined_cache ➔ bcache_ctrl				
Pin Function	**:**	To synchronize the signals in the cache controller.				
Pin Name	**:**	bi_cac_ctrl_rst	**Pin Class**	**:** Global	**Pin Size**	**:** 1 bit
Source to Destination	**:**	External ➔ upipelined_cache ➔ bcache_ctrl				
Pin Function	**:**	To reset the cache controller.				
Pin Name	**:**	bicac_ctrl_lmc_ same	**Pin Class**	**:** Status	**Pin Size**	**:** 1 bit
Source to Destination	**:**	umem_arbiter ➔ upipelined_cache ➔ bcache_ctrl				
Pin Function	**:**	Indicates the configuration of flash memory is same when HIGH.				
Pin Name	**:**	bicac_ctrl_mem _ack	**Pin Class**	**:** Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	umem_arbiter ➔ upipelined_cache ➔ bcache_ctrl				
Pin Function	**:**	To acknowledge status of the flash memory. HIGH: Data from flash memory is ready. LOW: Flash memory is ready to receive data.				
Pin Name	**:**	bicac_ctrl_cpu_ read	**Pin Class**	**:** Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	uctrl_path ➔ upipelined_cache ➔ bcache_ctrl				
Pin Function	**:**	Enable read from cache RAM				
Pin Name	**:**	bicac_ctrl_cpu_ write	**Pin Class**	**:** Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	uctrl_path ➔ upipelined_cache ➔ bcache_ctrl				
Pin Function	**:**	Enable write to cache RAM				
Pin Name	**:**	bicac_ctrl_hit	**Pin Class**	**:** Status	**Pin Size**	**:** 1 bit
Source to Destination	**:**	upipelined_cache ➔ bcache_ctrl				
Pin Function	**:**	Indicates cache hit when HIGH				
Pin Name	**:**	bicac_ctrl_dirty	**Pin Class**	**:** Status	**Pin Size**	**:** 1 bit
Source to Destination	**:**	upipelined_cache ➔ bcache_ctrl				
Pin Function	**:**	Indicates the data accessed is dirty.				
Pin Name	**:**	bicac_ctrl_fifo_ busy	**Pin Class**	**:** Status	**Pin Size**	**:** 1 bit
Source to Destination	**:**	bFIFO ➔ bcache_ctrl				
Pin Function	**:**	Indicates FIFO is busy writing data into flash memory when HIGH.				
Pin Name	**:**	bicac_ctrl_fifo_ full	**Pin Class**	**:** Status	**Pin Size**	**:** 1 bit

Source to Destination	**:**	bFIFO ➔ bcache_ctrl
Pin Function	**:**	Indicates FIFO is full when HIGH.
Pin Name	**:**	bicac_ctrl_fifo_hit **Pin Class :** Status **Pin Size :** 1 bit
Source to Destination	**:**	bFIFO ➔ bcache_ctrl
Pin Function	**:**	Indicates latest copy of data is found in FIFO when HIGH.

Table 5-3: Cache Controller Input Pin Description

Output Pin Description

Pin Name	**:**	bocac_ctrl_cpu_data_output_en **Pin Class :** Control **Pin Size :** 1 bit
Source to Destination	**:**	bcache_ctrl ➔ upipelined_cache
Pin Function	**:**	Indicates that data is enabled to output to the data path unit.
Pin Name	**:**	bocac_ctrl_counter **Pin Class :** Control **Pin Size :** 3 bits
Source to Destination	**:**	bcache_ctrl ➔ upipelined_cache
Pin Function	**:**	Count the data when transferring a block of data (8 words).
Pin Name	**:**	bocac_ctrl_cache_data_select **Pin Class :** Control **Pin Size :** 1 bit
Source to Destination	**:**	bcache_ctrl ➔ upipelined_cache ➔bcache_ram
Pin Function	**:**	Choose data from flash memory to cache RAM when HIGH Choose data from data path unit to cache RAM when LOW
Pin Name	**:**	bocac_ctrl_mem_read **Pin Class :** Control **Pin Size :** 1 bit
Source to Destination	**:**	bcache_ctrl ➔ upipelined_cache
Pin Function	**:**	Indicates to read from flash memory when HIGH
Pin Name	**:**	bo_cac_ctrl_mem_write **Pin Class :** Control **Pin Size :** 1 bit
Source to Destination	**:**	bcache_ctrl ➔ bfifo_ctrl
Pin Function	**:**	Indicates to write to flash memory when HIGH
Pin Name	**:**	bocac_ctrl_mem_sel **Pin Class :** Control **Pin Size :** 4 bits
Source to Destination	**:**	bcache_ctrl ➔ upipelined_cache ➔ umem_arbiter
Pin Function	**:**	To mask which byte of the data from/to the flash memory.

Pin Name	**:**	bocac_ctrl_update_en	**Pin Class**	**:**	Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	bcache_ctrl ➔ upipelined_cache					
Pin Function	**:**	Enable update of cache RAM when HIGH					
Pin Name	**:**	bocac_ctrl_update_dirty	**Pin Class**	**:**	Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	bcache_ctrl ➔ upipelined_cache					
Pin Function	**:**	Enable update of dirty bits in cache RAM when HIGH					
Pin Name	**:**	bocac_ctrl_fifo_buffer_en	**Pin Class**	**:**	Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	bcache_ctrl ➔ upipelined_cache					
Pin Function	**:**	Enable to write data back from FIFO to temporary buffer when HIGH					
Pin Name	**:**	bocac_ctrl_cac_fifo_en	**Pin Class**	**:**	Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	bcache_ctrl ➔ upipelined_cache					
Pin Function	**:**	Enable to evict data from cache RAM to FIFO block when HIGH					
Pin Name	**:**	bocac_ctrl_buffer_cac_en	**Pin Class**	**:**	Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	bcache_ctrl ➔ upipelined_cache					
Pin Function	**:**	Enable to move data from temporary buffer to cache RAM when HIGH.					
Pin Name	**:**	bocac_ctrl_fifo_update_valid	**Pin Class**	**:**	Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	bcache_ctrl ➔ upipelined_cache					
Pin Function	**:**	Enable update of valid bits of data in FIFO block when HIGH.					

Table 5-4: Cache Controller Output Pin Description

5.2.4 Microarchitecture Drawing of Cache Controller

Figure 5-6 below shows the microarchitecture drawing of the cache controller. The cache controller developed by seniors is modified and modelled using Registered Mealy Machine Style to improve the logic delay of the cache controller.

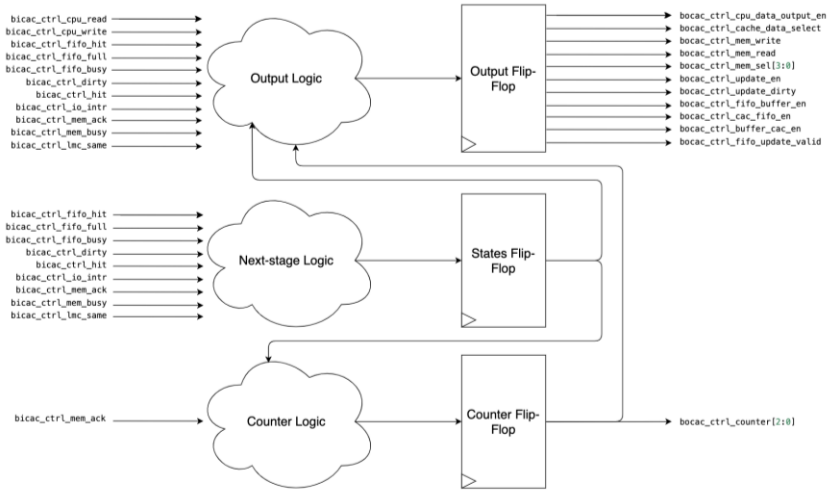

Figure 5-3**:** Microarchitecture Drawing of Cache Controller

5.2.5 Cache Controller State Diagram

Figure 5-7 below shows the cache controller state diagram for both read and write operation. A new state “WAIT_FIFO” is added as a “delay” cycle to wait one cycle for FIFO controller to return to IDLE state. Without this state, the FIFO controller will still be in the REMOVE_DATA state when the cache controller enters the BLOCK_EVICT_2 state. This will lead to lost of data when the first block of data is evicted from cache ram to FIFO block.

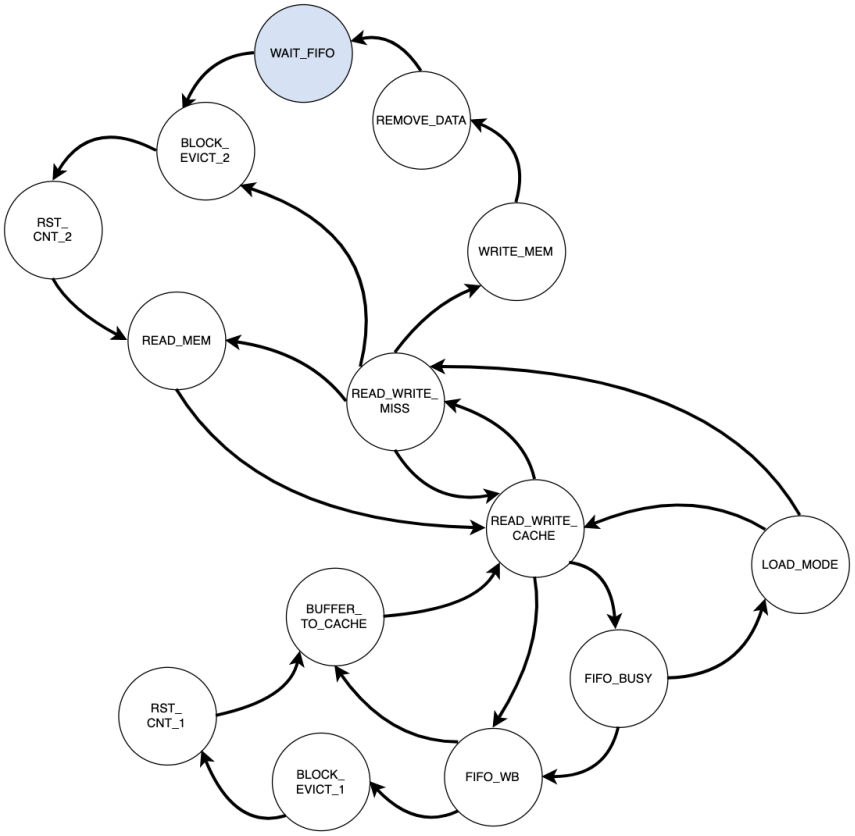

Figure 5-4: Cache Controller State Diagram [13]

5.2.6 Cache Controller State Definition

Table 5-5 shows the Cache Controller State Definition.

State Name	State Definition
READ_WRITE_CACHE	Read from cache or write to cache when CACHE HIT.
FIFO_BUSY	FIFO busy writing data to flash memory.
RST_CNT_1	Reset and prepare ready counter for transferring data from temporary buffer to cache RAM after cache RAM evicted data to FIFO.
FIFO_WB	FIFO writes back data to temporary buffer.
LOAD_MODE	Check and load flash memory configuration
READ_WRITE_MISS	CACHE MISS
REMOVE_DATA	Remove a data from FIFO
RST_CNT_2	Reset and prepare ready counter for reading flash memory after cache RAM evicted data to FIFO.
BUFFER_TO_CACHE	Move data from temporary buffer to cache RAM.
BLOCK_EVICT_1	Cache RAM evicts dirty data to FIFO to receive latest copy of data from FIFO.
BLOCK_EVICT_2	Cache RAM evicts dirty data to FIFO to receive latest copy of data from flash memory.
WRITE_MEM	Write data from FIFO to flash memory if FIFO full.
READ_MEM	Read data from flash memory.
WAIT_FIFO	Wait one cycle for FIFO controller to return to IDLE state so that FIFO is able to receive a new copy of data from cache ram without lost of data.

Table 5-5**:** Cache Controller State Definition

5.3 Forwarding Block

5.3.1 Forwarding Block Functionality

- To generate forward control signal based on the presence instruction in each pipeline stage.

5.3.2 Forwarding Block Block Diagram

Figure 5-5 below shows the block diagram of the forwarding block.

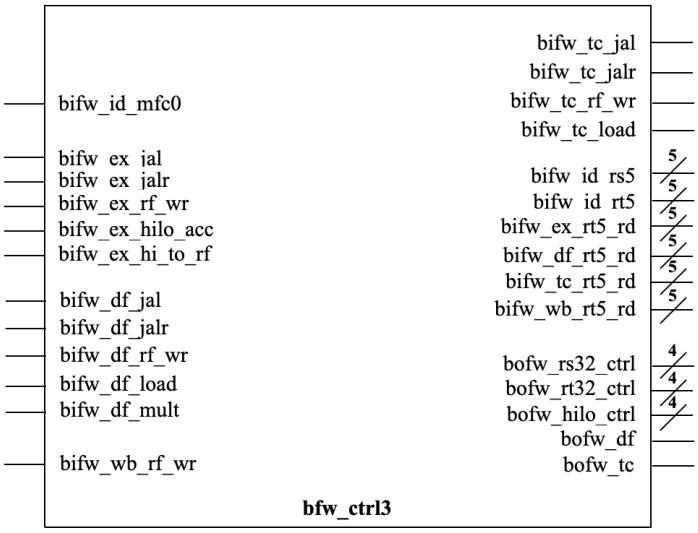

Figure 5-5: Block Diagram of the Forwarding Block

5.3.3 Pin Description of the Forwarding Block

Input Pin Description

Pin Name	**:**	bifw_id_mfc0	**Pin Class**	**:** Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	ucp ➔ udp ➔ bfw_ctrl				
Pin Function	**:**	Indicate the mfc0 instruction is in ID stage.				
Pin Name	**:**	bifw_ex_jal	**Pin Class**	**:** Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	ucp ➔ udp ➔ bfw_ctrl				
Pin Function	**:**	Indicate the jal instruction is in EX stage.				
Pin Name	**:**	bifw_ex_jalr	**Pin Class**	**:** Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	ucp ➔ udp ➔ bfw_ctrl				
Pin Function	**:**	Indicate the jalr instruction is in EX stage.				
Pin Name	**:**	bifw_ex_rf_wr	**Pin Class**	**:** Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	ucp ➔ udp ➔ bfw_ctrl				
Pin Function	**:**	Indicate the enable write to Register File operation is in EX stage.				
Pin Name	**:**	bifw_ex_hilo_acc	**Pin Class**	**:** Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	ucp ➔ udp ➔ bfw_ctrl				
Pin Function	**:**	Indicate the mflo or mfhi instruction is in EX stage.				
Pin Name	**:**	bifw_ex_hi_to_rf	**Pin Class**	**:** Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	ucp ➔ udp ➔ bfw_ctrl				
Pin Function	**:**	Indicate the mfhi instruction is in EX stage.				
Pin Name	**:**	bifw_df_jal	**Pin Class**	**:** Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	ucp ➔ udp ➔ bfw_ctrl				
Pin Function	**:**	Indicate the jal instruction is in DF stage.				
Pin Name	**:**	bifw_df_jalr	**Pin Class**	**:** Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	ucp ➔ udp ➔ bfw_ctrl				
Pin Function	**:**	Indicate the jalr instruction is in DF stage.				
Pin Name	**:**	bifw_df_rf_wr	**Pin Class**	**:** Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	ucp ➔ udp ➔ bfw_ctrl				
Pin Function	**:**	Indicate the enable write to Register File operation is in DF stage.				
Pin Name	**:**	bifw_df_load	**Pin Class**	**:** Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	ucp ➔ udp ➔ bfw_ctrl				
Pin Function	**:**	Indicate the load instruction is in DF stage.				
Pin Name	**:**	bifw_df_mult	**Pin Class**	**:** Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	ucp ➔ udp ➔ bfw_ctrl				
Pin Function	**:**	Indicate the mult or multu instruction is in DF stage.				

Pin Name	**:**	bifw_tc_jal	**Pin Class**	**:**	Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	ucp ➔ udp ➔ bfw_ctrl					
Pin Function	**:**	Indicate the jal instruction is in TC stage.					
Pin Name	**:**	bifw_tc_jalr	**Pin Class**	**:**	Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	ucp ➔ udp ➔ bfw_ctrl					
Pin Function	**:**	Indicate the jalr instruction is in TC stage.					
Pin Name	**:**	bifw_tc_rf_wr	**Pin Class**	**:**	Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	ucp ➔ udp ➔ bfw_ctrl					
Pin Function	**:**	Indicate the enable write to Register File operation is in TC stage.					
Pin Name	**:**	bifw_tc_load	**Pin Class**	**:**	Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	ucp ➔ udp ➔ bfw_ctrl					
Pin Function	**:**	Indicate the load instruction is in TC stage.					
Pin Name	**:**	bifw_wb_rf_wr	**Pin Class**	**:**	Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	ucp ➔ udp ➔ bfw_ctrl					
Pin Function	**:**	To indicate the enable write to Register File operation is in TC stage.					
Pin Name	**:**	bifw_id_rs5	**Pin Class**	**:**	Addr.	**Pin Size**	**:** 5 bits
Source to Destination	**:**	upipelined_cache (icache) / uboot_rom ➔ udp ➔ bfw_ctrl					
Pin Function	**:**	Carry the address of source register in ID stage.					
Pin Name	**:**	bifw_id_rt5	**Pin Class**	**:**	Addr.	**Pin Size**	**:** 5 bits
Source to Destination	**:**	upipelined_cache (icache) / uboot_rom ➔ udp ➔ bfw_ctrl					
Pin Function	**:**	Carry the address of target register in ID stage.					
Pin Name	**:**	bifw_ex_rt5_rd5	**Pin Class**	**:**	Addr.	**Pin Size**	**:** 5 bits
Source to Destination	**:**	upipelined_cache (icache) / uboot_rom ➔ udp ➔ bfw_ctrl					
Pin Function	**:**	Carry the address of destination register in EX stage.					
Pin Name	**:**	bifw_df_rt5_rd5	**Pin Class**	**:**	Addr.	**Pin Size**	**:** 5 bits
Source to Destination	**:**	upipelined_cache (icache) / uboot_rom ➔ udp ➔ bfw_ctrl					
Pin Function	**:**	Carry the address of destination register in DF stage.					
Pin Name	**:**	bifw_tc_rt5_rd5	**Pin Class**	**:**	Addr.	**Pin Size**	**:** 5 bits
Source to Destination	**:**	upipelined_cache (icache) / uboot_rom ➔ udp ➔ bfw_ctrl					
Pin Function	**:**	Carry the address of destination register in TC stage.					
Pin Name	**:**	bifw_wb_rt5_rd5	**Pin Class**	**:**	Addr.	**Pin Size**	**:** 5 bits
Source to Destination	**:**	upipelined_cache (icache) / uboot_rom ➔ udp ➔ bfw_ctrl					
Pin Function	**:**	Carry the address of destination register in WB stage.					

Table 5-6: Forwarding Block Input Pin Description

Output Pin Description

Pin Name	**:**	bofw_rs32_ctrl	**Pin Class**	**:**	Control	**Pin Size**	**:** 4 bits
Source to Destination	**:**	bfw_ctrl ➔ udp					
Pin Function	**:**	Indicates the forward control signal for the rs path.					
Pin Name	**:**	bofw_rt32_ctrl	**Pin Class**	**:**	Control	**Pin Size**	**:** 4 bits
Source to Destination	**:**	bfw_ctrl ➔ udp					
Pin Function	**:**	Indicates the forward control signal for the rt path.					
Pin Name	**:**	bofw_hilo_ctrl	**Pin Class**	**:**	Control	**Pin Size**	**:** 4 bits
Source to Destination	**:**	bfw_ctrl ➔ udp					
Pin Function	**:**	Indicates the forward control signal for the HILO path.					
Pin Name	**:**	bofw_df	**Pin Class**	**:**	Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	bfw_ctrl ➔ udp					
Pin Function	**:**	1: Forward data from DF stage to EX stage. 0: No data forwarding.					
Pin Name	**:**	bofw_tc	**Pin Class**	**:**	Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	bfw_ctrl ➔ udp ➔ upipelined_cache2 (dcache)					
Pin Function	**:**	1: Forward data from TC stage to DF stage. 0: No data forwarding.					

Table 5-7: Forwarding Block Output Pin Description

5.4 Interlock Block

5.4.1 Interlock Block Functionality

- To generate pipeline interlock and flush control signal based on the presence instruction in each pipeline stage.

5.4.2 Interlock Block Block Diagram

Figure 5-5 below shows the block diagram of the interlock block.

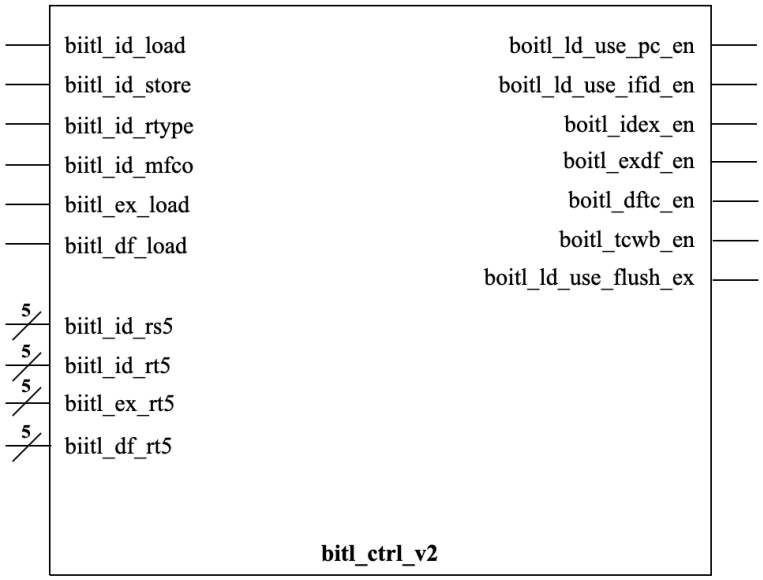

Figure 5-6: Block Diagram of the Interlock Block

5.4.3 Pin Description of the Interlock Block

Input Pin Description

Pin Name	**:**	biitl_id_load	**Pin Class**	**:** Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	ucp ➔ udp ➔ bitl_ctrl				
Pin Function	**:**	Indicate the load instruction is in ID stage.				
Pin Name	**:**	biitl_id_store	**Pin Class**	**:** Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	ucp ➔ udp ➔ bitl_ctrl				
Pin Function	**:**	Indicate the store instruction is in ID stage.				
Pin Name	**:**	biitl_id_rtype	**Pin Class**	**:** Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	ucp ➔ udp ➔ bitl_ctrl				
Pin Function	**:**	Indicate the R-type instruction is in ID stage.				
Pin Name	**:**	biitl_id_mfc0	**Pin Class**	**:** Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	ucp ➔ udp ➔ bitl_ctrl				
Pin Function	**:**	Indicate the mfc0 instruction is in ID stage.				
Pin Name	**:**	biitl_ex_load	**Pin Class**	**:** Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	ucp ➔ udp ➔ bitl_ctrl				
Pin Function	**:**	Indicate the load instruction is in EX stage.				
Pin Name	**:**	biitl_df_load	**Pin Class**	**:** Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	ucp ➔ udp ➔ bitl_ctrl				
Pin Function	**:**	Indicate the load instruction is in DF stage.				
Pin Name	**:**	biitl_id_rs5	**Pin Class**	**:** Addr.	**Pin Size**	**:** 5 bits
Source to Destination	**:**	upipelined_cache (icache) / uboot_rom ➔ udp ➔ bitl_ctrl				
Pin Function	**:**	Carry the address of source register in ID stage.				
Pin Name	**:**	biitl_id_rt5	**Pin Class**	**:** Addr.	**Pin Size**	**:** 5 bits
Source to Destination	**:**	upipelined_cache (icache) / uboot_rom ➔ udp ➔ bitl_ctrl				
Pin Function	**:**	Carry the address of target register in ID stage.				
Pin Name	**:**	biitl_df_rt5	**Pin Class**	**:** Addr.	**Pin Size**	**:** 5 bits
Source to Destination	**:**	upipelined_cache (icache) / uboot_rom ➔ udp ➔ bitl_ctrl				
Pin Function	**:**	Carry the address of target (destination) register in DF stage.				
Pin Name	**:**	biitl_ex_rt5	**Pin Class**	**:** Addr.	**Pin Size**	**:** 5 bits
Source to Destination	**:**	upipelined_cache (icache) / uboot_rom ➔ udp ➔ bitl_ctrl				
Pin Function	**:**	Carry the address of target (destination) register in EX stage.				

Table 5-8: Interlock Block Input Pin Description

Output Pin Description

Pin Name	**:**	boitl_ld_use_pc_en	**Pin Class**	**:**	Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	bitl_ctrl ➔ udp					
Pin Function	**:**	Stall PC register when deasserted.					
Pin Name	**:**	boitl_ld_use_ifid_en	**Pin Class**	**:**	Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	bitl_ctrl ➔ udp					
Pin Function	**:**	Stall IFIS and ISID pipeline register when deasserted.					
Pin Name	**:**	boitl_idex_en	**Pin Class**	**:**	Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	bcache_ctrl ➔ upipelined_cache					
Pin Function	**:**	Reserved for future development, temporary always enable.					
Pin Name	**:**	boitl_exdf_en	**Pin Class**	**:**	Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	bcache_ctrl ➔ upipelined_cache					
Pin Function	**:**	Reserved for future development, temporary always enable.					
Pin Name	**:**	boitl_dftc_en	**Pin Class**	**:**	Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	bcache_ctrl ➔ upipelined_cache					
Pin Function	**:**	Reserved for future development, temporary always enable.					
Pin Name	**:**	boitl_tcwb_en	**Pin Class**	**:**	Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	bcache_ctrl ➔ upipelined_cache					
Pin Function	**:**	Reserved for future development, temporary always enable.					
Pin Name	**:**	boitl_ld_use_flush_ex	**Pin Class**	**:**	Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	bcache_ctrl ➔ upipelined_cache					
Pin Function	**:**	Flush IDEX pipeline register when asserted.					

Table 5-9: Interlock Block Output Pin Description

5.4.4 Internal Operation

For Load-Use Instruction related to uram, loaded data is only available at the end of DF stage.

Instruction		Clock number								
		1	2	3	4	5	6	7	8	9
add	$t0, $t1, $t2	IF	IS	ID	EX	DF	TC	WB		
ld	$s0, ……		IF	IS	ID	EX	DF	TC	WB	
sub	$s1, $s0……			IF	IS	ID	**Stall**	EX	TC	WB
and	$s2, $s0……				IF	IS	**Stall**	ID	EX	DF

Table 5-10: Load instruction (uram) followed by an immediate use results in a 1-cycle stall.

For Load-Use Instruction related to dcache, loaded data is only available at the end of TC stage.

Instruction		Clock number								
		1	2	3	4	5	6	7	8	9
add	$t0, $t1, $t2	IF	IS	ID	EX	DF	TC	WB		
ld	$s0, ……		IF	IS	ID	EX	DF	TC	WB	
sub	$s1, $s0……			IF	IS	ID	**Stall**	**Stall**	EX	TC
and	$s2, $s0……				IF	IS	**Stall**	**Stall**	ID	EX

Table 5-11: Load instruction (dcache) followed by an immediate use results in a 2-cycle stall.

→ : Indicates the data forwarding path.

5.5 Address Decoder Block

5.4.1 Address Decoder Block Functionality

- To enable the data access to a specific memory device and I/O registers based on the address decoded from the instruction.

5.4.2 Address Decoder Block Block Diagram

Figure 5-5 below shows the block diagram of the address decoder block.

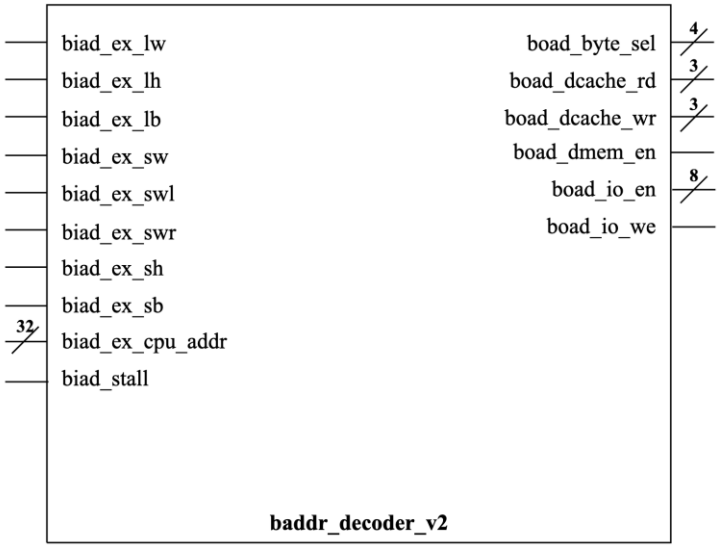

Figure 5-7: Block Diagram of the Address Decoder Block

5.4.3 Pin Description of the Address Decoder Block

Input Pin Description

Pin Name	**:**	biad_ex_lw	**Pin Class**	**:** Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	bitl_ctrl ➔ udp ➔ baddr_decoder				
Pin Function	**:**	Indicate the lw or lwl or lwr instruction in EX stage.				
Pin Name	**:**	biad_ex_lh	**Pin Class**	**:** Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	bitl_ctrl ➔ udp ➔ baddr_decoder				
Pin Function	**:**	Indicate the lh or lhu instruction in EX stage.				
Pin Name	**:**	biad_ex_lb	**Pin Class**	**:** Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	bitl_ctrl ➔ udp ➔ baddr_decoder				
Pin Function	**:**	Indicate the lb or lbu instruction in EX stage.				
Pin Name	**:**	biad_ex_sw	**Pin Class**	**:** Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	bitl_ctrl ➔ udp ➔ baddr_decoder				
Pin Function	**:**	Indicate the sw instruction in EX stage.				
Pin Name	**:**	biad_ex_swl	**Pin Class**	**:** Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	bitl_ctrl ➔ udp ➔ baddr_decoder				
Pin Function	**:**	Indicate the swl instruction in EX stage.				
Pin Name	**:**	biad_ex_swr	**Pin Class**	**:** Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	bitl_ctrl ➔ udp ➔ baddr_decoder				
Pin Function	**:**	Indicate the swr instruction in EX stage.				
Pin Name	**:**	biad_ex_sh	**Pin Class**	**:** Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	bitl_ctrl ➔ udp ➔ baddr_decoder				
Pin Function	**:**	Indicate the sh instruction in EX stage.				
Pin Name	**:**	biad_ex_sb	**Pin Class**	**:** Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	bitl_ctrl ➔ udp ➔ baddr_decoder				
Pin Function	**:**	Indicate the sb instruction in EX stage.				
Pin Name	**:**	biad_ex_cpu_addr	**Pin Class**	**:** Control	**Pin Size**	**:** 32 bits
Source to Destination	**:**	bitl_ctrl ➔ udp ➔ baddr_decoder				
Pin Function	**:**	Used to decide which memory device to be accessed.				
Pin Name	**:**	biad_stall	**Pin Class**	**:** Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	bitl_ctrl ➔ udp ➔ baddr_decoder				
Pin Function	**:**	Deassert write enable signal to the memory device when CPU stall.				

Table 5-12: Address Decoder Block Input Pin Description

Output Pin Description

Pin Name	**:**	boad_byte_sel	**Pin Class**	**:**	Control	**Pin Size**	**:** 4 bits
Source to Destination	**:**	baddr_decoder ➔ udp ➔ uram					
Pin Function	**:**	Select any one or more bytes to be output.					
Pin Name	**:**	boad_dcache_rd	**Pin Class**	**:**	Control	**Pin Size**	**:** 3 bits
Source to Destination	**:**	baddr_decoder ➔ udp ➔ upipelined_cache (dcache)					
Pin Function	**:**	Indicate types of load instruction to determine data to be read.					
Pin Name	**:**	boad_dcache_wr	**Pin Class**	**:**	Control	**Pin Size**	**:** 3 bits
Source to Destination	**:**	baddr_decoder ➔ udp ➔ upipelined_cache (dcache)					
Pin Function	**:**	Indicate types of store instruction to determine data to be written.					
Pin Name	**:**	boad_dmem_en	**Pin Class**	**:**	Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	baddr_decoder ➔ udp ➔ uram					
Pin Function	**:**	Enable uram for read and write operation.					
Pin Name	**:**	boad_iomem_we	**Pin Class**	**:**	Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	baddr_decoder ➔ udp ➔ uram / I/O devices					
Pin Function	**:**	Enable write access to RAM or I/O register.					
Pin Name	**:**	boad_io_en	**Pin Class**	**:**	Control	**Pin Size**	**:** 1 bit
Source to Destination	**:**	baddr_decoder ➔ udp ➔ uram / I/O devices					
Pin Function	**:**	Enable I/O devices for read and write operation.					

Table 5-13: Address Decoder Block Output Pin Description

Chapter 6: Test and Verification

6.1 Pipelined Cache Unit (D-Cache) Test

6.1.1 Pipelined Cache Unit (D-Cache) Test Plan

Test	Expected Output	Result

Test case 1: Reset
Input
1st Clock Cycle
tb_uicac_rst <= 1'b1;
 	
2nd Clock Cycle
tb_uicac_rst <= 1'b0;
 	
// Wait for 1 clock cycle
	Next 1st Clock cycle
	All the signals are reset to their respective initial values.
		PASS

Test case 2: Write Miss followed by Read Hit
Input
1st Clock Cycle
tb_uicac_cpu_addr <=
32'h8001_F800;
tb_uicac_cpu_data <=
32'h8888_8888;
tb_uicac_cpu_write <= 3'b100;
 	
2nd Clock Cycle
tb_uicac_cpu_addr <=
32'h8001_F80C;
tb_uicac_cpu_write <= 3'b000;
tb_uicac_cpu_read <= 3'b100;
 	
for (i=0; i<8; i=i+1)
(2+i)th Clock Cycle
tb_uicac_mem_ack <= 1'b1;
tb_uicac_mem_data_rd
<= 32'h1111_1111 + i;
 	
// Wait for 5 clock cycles
	Next 1st – 10th Clock cycle
	Cache miss (write miss) situation occurred.
	Processor is stalled to read in memory from flash memory to D-Cache.
	
	Next 11th Clock cycle
	Processor is resumed.
	
	Next 12th Clock cycle
	Data (32'h8888_8888) with address (32'h8001_F800) is written into D-Cache.
	Processor is stalled to delay read operation as cache ram is busy.
	
	Next 13th Clock cycle
	Data (32'h1111_1114) of address (32'h8001_F80C) is read.
		PASS

Test case 3: Read Hit followed by Read Hit
Input
1st Clock Cycle
tb_uicac_cpu_addr <= 32'h8001_F804;
tb_uicac_cpu_read <= 3'b100;
 	
2nd Clock Cycle
tb_uicac_cpu_addr <= 32'h8001_F808;
 	
// Wait for 1 clock cycle
	Next 1st Clock cycle
	Data (32'h1111_1112) of address (32'h8001_F804) is read.
	
	Next 2nd Clock cycle
	Data (32'h1111_1113) of address (32'h8001_F808) is read.
		PASS

Test case 4: Write Miss followed by Read Hit
Input
1st Clock Cycle
tb_uicac_cpu_addr <= 32'h8001_F880;
tb_uicac_cpu_data <= 32'h6666_6666;
tb_uicac_cpu_write <= 3'b100;
 	
2nd Clock Cycle
tb_uicac_cpu_addr <= 32'h8001_F884;
tb_uicac_cpu_data <= 32'h0000_0000;
tb_uicac_cpu_write <= 3'b000;
tb_uicac_cpu_read <= 3'b100;
 	
3rd – 11th Clock Cycle
// Wait for 9 clock cycles
 	
for (i=0; i<8; i=i+1)
(11+i)th Clock Cycle
tb_uicac_mem_ack <= 1'b1;
tb_uicac_mem_data_rd <= 32'h2222_2221 + i;
 	
20th Clock Cycle
tb_uicac_mem_ack <= 1'b0
 	
// Wait for 4 clock cycles
	Next 1st – 19th Clock cycle
	Cache miss (write miss) situation occurred.
	Processor is stalled to evict dirty data from cache ram to FIFO block and read in the intended block of memory from flash memory.
	
	Next 20th Clock cycle
	Processor is resumed.
	
	Next 21th Clock cycle
	Data (32'h6666_6666) with address (32'h8001_F880) is written into D-Cache.
	Processor is stalled to delay read operation as cache ram is busy.
	
	Next 22th Clock cycle
	Data (32'h2222_2222) of address (32'h8001_F884) is read.
		PASS

Test case 5: Read Miss FIFO Hit followed by Read Hit
Input
1st Clock Cycle
tb_uicac_cpu_addr <= 32'h8001_F810;
tb_uicac_cpu_read <= 3'b100;
 	
2nd Clock Cycle
tb_uicac_cpu_addr <= 32'h8001_F800;
 	
// Wait for 21 clock cycles
	Next 1st – 20th Clock cycle
	Cache miss (read miss) situation occurred.
	Processor is stalled to evict dirty data from cache ram to FIFO block and read in the intended block of memory from FIFO block.
	
	Next 21th Clock cycle
	Processor is resumed.
	Data (32'h1111_1115) of address (32'h8001_F810) is read.
	
	Next 22th Clock cycle
	Data (32'h8888_8888) of address (32'h8001_F800) is read.
		PASS

Test case 6: Write Hit followed by Write Hit
Input
1st Clock Cycle
tb_uicac_cpu_addr <= 32'h8001_F820;
tb_uicac_cpu_data <= 32'h8686_8686;
tb_uicac_cpu_write <= 3'b100;
 	
2nd Clock Cycle
tb_uicac_cpu_addr <= 32'h8001_F840;
tb_uicac_cpu_data <= 32'h6868_6868;
tb_uicac_cpu_write <= 3'b100;
 	
// Wait for 1 clock cycle
	Next 2nd Clock cycle
	Data (32'h8686_8686) with address (32'h8001_F820) is written into D-Cache.
	
	Next 3rd Clock cycle
	Data (32'h6868_6868) with address (32'h8001_F840) is written into D-Cache.
		PASS

Test case 7: Write Hit followed by Read Miss FIFO Miss
Input
1st Clock Cycle
tb_uicac_cpu_addr <= 32'h8001_F860;
tb_uicac_cpu_data <= 32'h8888_8888;
tb_uicac_cpu_write <= 3'b100;
 	
2nd Clock Cycle
tb_uicac_cpu_addr <= 32'h8001_F8E0;
tb_uicac_cpu_data <= 32'h0000_0000;
tb_uicac_cpu_write <= 3'b000;
tb_uicac_cpu_read <= 3'b100;
 	
3rd – 12th Clock Cycle
// Wait for 10 clock cycles
 	
for (i=0; i<8; i=i+1)
(12+i)th Clock Cycle
tb_uicac_mem_ack <= 1'b1;
tb_uicac_mem_data_rd <= 32'h6666_6661 + i;
// Wait for 10 clock cycles
	Next 1st Clock cycle
	Write hit take place in TC stage.
	
	Next 2nd Clock cycle
	Data (32'h8888_8888) with address (32'h8001_F860) is written into D-Cache.
	
	Next 2nd – 20th Clock cycle
	Cache miss (read miss) situation occurred.
	Processor is stalled to evict dirty data from cache ram to FIFO block and read in the intended block of memory from flash memory.
	
	Next 21th Clock cycle
	Processor is resumed.
	Data (32'h6666_6661) of address (32'h8001_F8E0) is read.
		PASS

Test case 8: Read Miss FIFO Miss followed by Read Hit (I)
Input
1st Clock Cycle
tb_uicac_cpu_addr <= 32'h8001_F8C8;
tb_uicac_cpu_read <= 3'b100;
 	
2nd Clock Cycle
tb_uicac_cpu_addr <= 32'h8001_F8DC;
tb_uicac_cpu_read <= 3'b100;
 	
3rd – 11th Clock Cycle
// Wait for 9 clock cycles
 	
for (i=0; i<8; i=i+1)
(11+i)th Clock Cycle
tb_uicac_mem_ack <= 1'b1;
tb_uicac_mem_data_rd <= 32'h7777_7771 + i;
// Wait for 3 clock cycles
	Next 1st – 19th Clock cycle
	Cache miss (read miss) situation occurred.
	Processor is stalled to evict dirty data from cache ram to FIFO block and read in the intended block of memory from flash memory.
	
	Next 20th Clock cycle
	Processor is resumed.
	Data (32'h7777_7773) of address (32'h8001_F8C8) is read.
	
	Next 21th Clock cycle
	Data (32'h7777_7778) of address (32'h8001_F8DC) is read.
		PASS

Test case 9: Read Miss FIFO Miss followed by Read Hit (II)
Input
1st Clock Cycle
tb_uicac_cpu_addr <= 32'h8001_F8BC;
tb_uicac_cpu_read <= 3'b100;
 	
2nd Clock Cycle
tb_uicac_cpu_addr <= 32'h8001_F8A0;
tb_uicac_cpu_read <= 3'b100;
 	
3rd – 11th Clock Cycle
// Wait for 9 clock cycles
 	
for (i=0; i<8; i=i+1)
(11+i)th Clock Cycle
tb_uicac_mem_ack <= 1'b1;
tb_uicac_mem_data_rd <= 32'h8888_8881 + i;
 	
// Wait for 3 clock cycles
	Next 1st – 19th Clock cycle
	Cache miss (read miss) situation occurred.
	Processor is stalled to evict dirty data from cache ram to FIFO block and read in the intended block of memory from flash memory.
	
	Next 20th Clock cycle
	Processor is resumed.
	Data (32'h8888_8888) of address (32'h8001_F8BC) is read.
	
	Next 21th Clock cycle
	Data (32'h8888_8881) of address (32'h8001_F8A0) is read.
		PASS

Test case 10: Write Miss FIFO Hit followed by Read Hit
Input
1st Clock Cycle
tb_uicac_cpu_addr <= 32'h8001_F880;
tb_uicac_cpu_data <= 32'hFFFF_FFFF;
tb_uicac_cpu_write <= 3'b100;
 	
2nd Clock Cycle
tb_uicac_cpu_data <= 32'h1010_1010;
tb_uicac_cpu_write <= 3'b000;
tb_uicac_cpu_read <= 3'b100;
 	
// Wait for 21 clock cycles
	Next 1st – 20th Clock cycle
	Cache miss (write miss) situation occurred.
	Processor is stalled to evict dirty data from cache ram to FIFO block and read in the intended block of memory from FIFO block.
	
	Next 21th Clock cycle
	Processor is resumed.
	
	Next 22th Clock cycle
	Data (32'hFFFF_FFFF) with address (32'h8001_F880) is written into D-Cache.
	Processor is stalled to delay read operation as cache ram is busy.
	
	Next 20th Clock cycle
	Processor is resumed.
	Data (32'hFFFF_FFFF) of address (32'h8001_F880) is read.
		PASS

Test case 11: Read Miss FIFO Miss followed by Write Hit
Input
1st Clock Cycle
tb_uicac_cpu_addr <= 32'h8001_F980;
tb_uicac_cpu_read <= 3'b100;
 	
2nd Clock Cycle
tb_uicac_cpu_addr <= 32'h8001_F98C;
tb_uicac_cpu_data <= 32'hAAAA_AAAA;
tb_uicac_cpu_read <= 3'b000;
tb_uicac_cpu_write <= 3'b100;
 	
3rd Clock Cycle
tb_uicac_mem_ack <= 1'b1;
 	
4th – 11th Clock Cycle
// Wait for 8 clock cycles
tb_uicac_mem_ack <= 1'b0;
 	
12th – 21th Clock Cycle
// Wait for 10 clock cycles
 	
for (i=0; i<8; i=i+1)
(21+i)th Clock Cycle
tb_uicac_mem_ack <= 1'b1;
tb_uicac_mem_data_rd <= 32'hAAAA_AAA1 + i;
 	
// Wait for 3 clock cycles
	Next 1st – 29th Clock cycle
	Cache miss (read miss) situation occurred.
	Processor is stalled to evict dirty data from FIFO block to flash memory to free out space to hold dirty data evicted from cache ram to FIFO block.
	The intended block of memory is also read from flash memory.
	
	Next 30th Clock cycle
	Processor is resumed.
	Data (32'hAAAA_AAA1) of address (32'h8001_F980) is read.
	
	Next 31th Clock cycle
	Write hit take place in TC stage.
	
	Next 32th Clock cycle
	Data (32'hAAAA_AAAA) with address (32'h8001_F98C) is written into D-Cache.
		PASS

Table 6-1: Pipelined Cache Unit (D-Cache) Test Plan

6.1.2 Pipelined Cache Unit (D-Cache) Test Simulation Result

Test 1: Reset

Figure 6-1 shows the simulation result for Test 1: Reset.

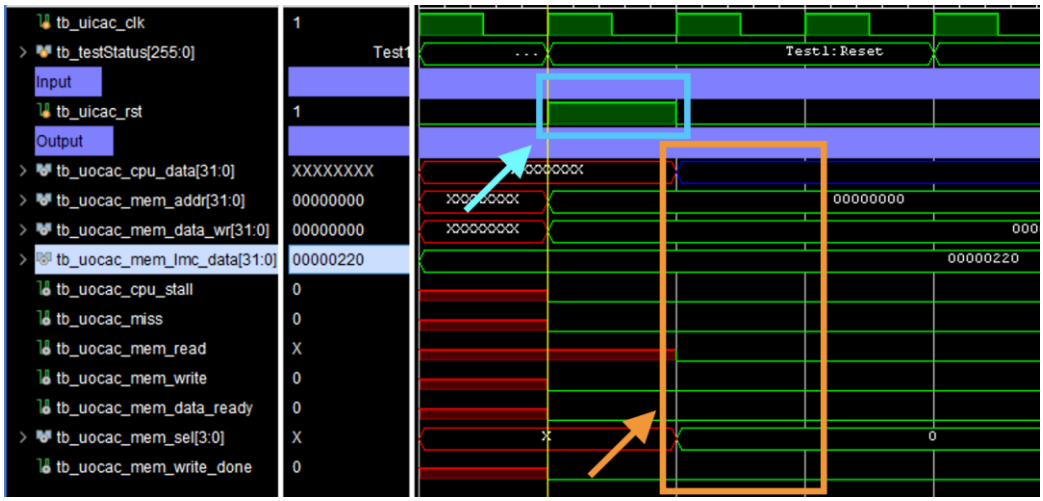

Figure 6-1**:** Simulation Result for Test 1: Reset.

- The uicac_rst is asserted in the 1st clock cycle (blue rectangle) then deasserted in the 2nd clock cycle.
- All the signals are reset to their respective initial values in the 2nd clock cycle (orange rectangle).

Test 2: Write Miss followed by Read Hit

Figure 6-2 shows the simulation result for Test 2: Write Miss followed by Read Hit.

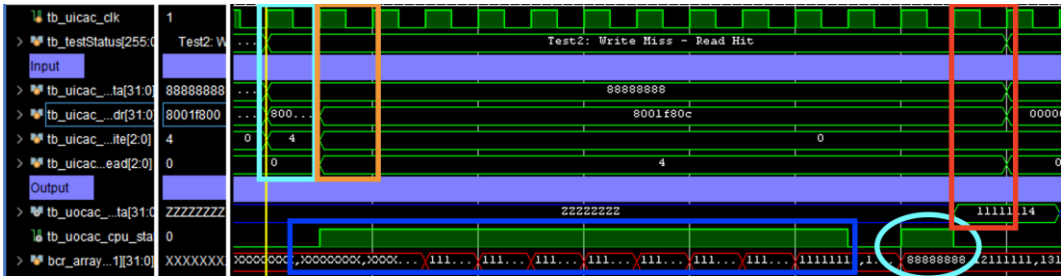

Figure 6-2**:** Simulation Result for Test 2: Write Miss followed by Read Hit.

- In the 1st clock cycle, *32'h8888_8888* is written to the dcache with address *32'h8001_f800* (light blue rectangle).
- In the 2nd clock cycle, data existed in the address *32'h8001_f80c* is read (orange rectangle).
- There is a cache miss situation, implying that the address *32'h8001_f800* and its data is not present in the cache ram.
- The processor is stalled to read in the block of data from the flash memory (dark blue rectangle).
- The processor is later resumed and the the data *32'h8888_8888* is written into the cache ram in the next clock cycle (blue circle).
- As the cache ram is busy writing in data, the processor is stalled again for one cycle.
- After all, the data *(32'h1111_1114)* of address *32'h8001_f80c* is read and output to the processor from the dcache (red rectangle).

Test 3: Read Hit followed by Read Hit

Figure 6-3 shows the simulation result for Test 3: Read Hit followed by Read Hit.

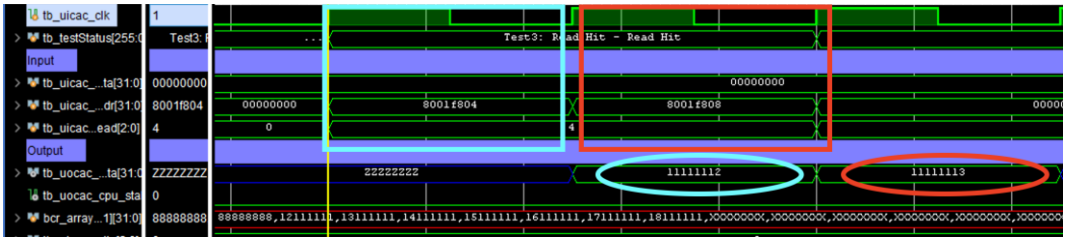

Figure 6-3: Simulation Result for Test 3: Read Hit followed by Read Hit.

- In the 1st clock cycle, data existed in the address *32'h8001_f804* is read (blue rectangle).
- In the 2nd clock cycle, data existed in the address *32'h8001_f808* is read (red rectangle).
- The data (*32'h1111_1112*) of address *32'h8001_f804* is read and output to the processor from the dcache in the 2nd clock cycle since it is a cache hit (blue circle).
- The data (*32'h1111_1113*) of address *32'h8001_f808* is read and output to the processor from the dcache in the 3rd clock cycle since it is a cache hit (red circle).

Test 4: Write Miss followed by Read Hit

Figure 6-4 shows the simulation result for Test 4: Write Miss followed by Read Hit.

Figure 6-4: Simulation Result for Test 4: Write Miss followed by Read Hit.

- In the 1st clock cycle, *32'h6666_6666* is written to the dcache with address *32'h8001_f880* (light blue rectangle).
- In the 2nd clock cycle, data existed in the address *32'h8001_f884* is read (orange rectangle).
- There is a cache miss situation, implying that the address *32'h8001_f880* and its data is not present in the cache ram.
- The processor is stalled (red arrow) to read in the block of data from the flash memory (yellow rectangle).
- However, before that, there is a block of dirty data with also index = *2'b00* existed in the cache ram.
- The cache ram evicted the dirty block of data into the FIFO block in advance (dark blue rectangle).
- The processor is later resumed and the data *32'h6666_6666* is written into the dcache in the next clock cycle (blue circle).
- As the dcache is busy writing in data, the processor is stalled again for one cycle.
- After all, the data (*32'h2222_2222*) of address *32'h8001_f884* is read and output to the processor from the dcache (red rectangle).

Test 5: Read Miss FIFO Hit followed by Read Hit

Figure 6-5 shows the simulation result for Test 5: Read Miss FIFO Hit followed by Read Hit.

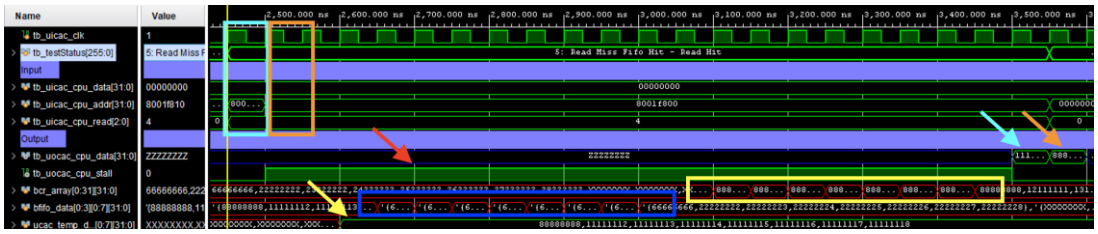

Figure 6-5: Simulation Result for Test 5: Read Miss FIFO Hit followed by Read Hit.

- In the 1st clock cycle, data existed in the address *32'h8001_f810* is read (light blue rectangle).
- In the 2nd clock cycle, data existed in the address *32'h8001_f800* is read (orange rectangle).
- There is a cache miss situation, implying that the address *32'h8001_f810* and its data is not present in the cache ram.
- The processor is stalled to read in the block of data (red arrow).
- The dcache recognized that the latest copy of the valid intended data is in the FIFO block.
- The intended data is first evicted from the FIFO block to the cache temporary buffer (yellow arrow).
- In the next clock cycle, the dirty block of data with also index = *2'b00* is evicted by the cache ram to the FIFO block (blue rectangle).
- Later, the valid copy of data is written back from the temporary buffer back to the cache ram for read operation to perform (yellow rectangle).
- After all, the processor is resumed, and the data (32'h1111_1115) of address *32'h8001_f810* (blue arrow) and the data (*32'h8888_8888*) of address *32'h8001_f800* (orange arrow) are read and output to the processor from the dcache.

Test 6: Write Hit followed by Write Hit

Figure 6-6 shows the simulation result for Test 6: Write Hit followed by Write Hit.

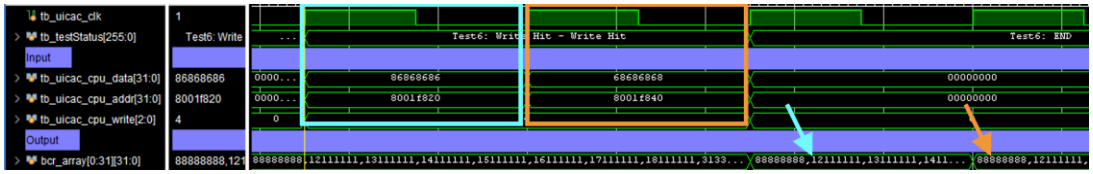

Figure 6-6: Simulation Result for Test 6: Write Hit followed by Write Hit.

- In the 1st clock cycle, *32'h8686_8686* is written to the dcache with address *32'h8001_f820* (blue rectangle).
- In the 2nd clock cycle, *32'h6868_6868* is written to the dcache with address *32'h8001_f840* (orange rectangle).
- The write instruction of data *(32'h8686_8686)* to address *32'h8001_f820* is passed to the TC stage in the 2nd clock cycle and successfully written to the cache ram in the 3rd clock cycle since it is a cache hit (blue arrow).
- The write instruction of data *(32'h6868_6868)* to address *32'h8001_f840* is passed to the TC stage in the 3rd clock cycle and successfully written to the cache ram in the 4th clock cycle since it is a cache hit (orange arrow).

Test 7: Write Hit followed by Read Miss FIFO Miss

Figure 6-7 shows the simulation result for Test 7: Write Hit followed by Read Miss FIFO Miss.

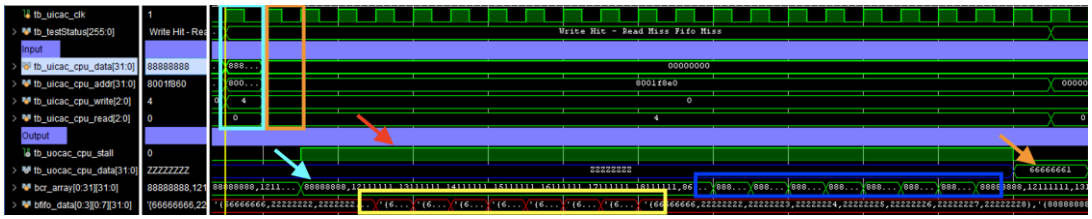

Figure 6-7: Simulation Result for Test 7: Write Hit followed by Read Miss FIFO Miss.

- In the 1st clock cycle, *32'h8888_8888* is written to the dcache with address *32'h8001_f860* (light blue rectangle).
- In the 2nd clock cycle, data existed in the address *32'h8001_f8e0* is read (orange rectangle).
- The write instruction of data *(32'h8888_8888)* to address *32'h8001_f860* is passed to the TC stage in the 2nd clock cycle and successfully written to the cache ram in the 3rd clock cycle since it is a cache hit (blue arrow).
- For the read operation, there is a cache miss situation, implying that the address *32'h8001_f8e0* and its data is not present in the cache ram.
- The processor is stalled (red arrow) to read in the block of data from the flash memory (dark blue rectangle).
- However, before that, there is a block of dirty data with also index = *2'b11* existed in the cache ram.
- The cache ram evicted the dirty block of data into the FIFO block in advance (yellow rectangle).
- After all, the processor is resumed and the data (*32'h6666_6661*) of address *32'h8001_f8e0* is read and output to the processor from the dcache (orange arrow).

Test 8: Read Miss FIFO Miss followed by Read Hit (I)

Figure 6-8 shows the simulation result for Test 8: Read Miss FIFO Miss followed by Read Hit (I).

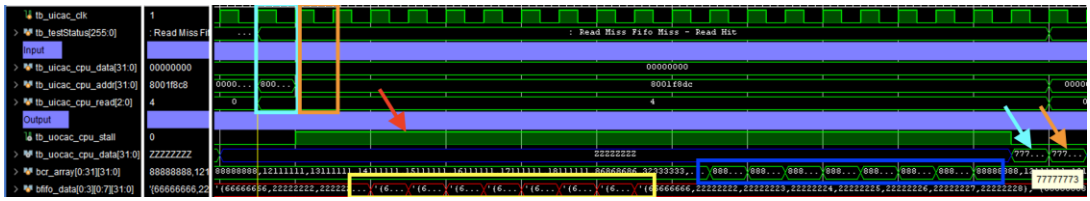

Figure 6-8: Simulation Result for Test 8: Read Miss FIFO Miss followed by Read Hit (I).

- In the 1st clock cycle, data existed in the address *32'h8001_f8c8* is read (light blue rectangle).
- In the 2nd clock cycle, data existed in the address *32'h8001_f8dc* is read (orange rectangle).
- There is a cache miss situation, implying that the address *32'h8001_f8c8* and its data is not present in the cache ram.
- The processor is stalled (red arrow) to read in the block of data from the flash memory (dark blue rectangle).
- However, before that, there is a block of dirty data with also index = *2'b10* existed in the cache ram.
- The cache ram evicted the dirty block of data into the FIFO block in advance (yellow rectangle).
- After all, the processor is resumed and the data (*32'h7777_7773*) of address *32'h8001_f8c8* is read and output to the processor from the dcache (blue arrow).
- Later, the data (*32'h7777_7778*) of address *32'h8001_f8dc* is read and output to the processor from the dcache since it is a cache hit (orange arrow).

Test 9: Read Miss FIFO Miss followed by Read Hit (II)

Figure 6-9 shows the simulation result for Test 9: Read Miss FIFO Miss followed by Read Hit (II).

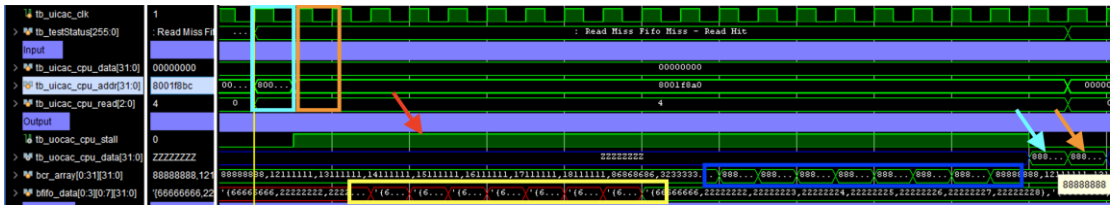

Figure 6-9: Simulation Result for Test 9: Read Miss FIFO Miss followed by Read Hit (II).

- In the 1st clock cycle, data existed in the address *32'h8001_f8bc* is read (light blue rectangle).
- In the 2nd clock cycle, data existed in the address *32'h8001_f8a0* is read (orange rectangle).
- There is a cache miss situation, implying that the address *32'h8001_f8bc* and its data is not present in the cache ram.
- The processor is stalled (red arrow) to read in the block of data from the flash memory (dark blue rectangle).
- However, before that, there is a block of dirty data with also index = *2'b01* existed in the cache ram.
- The cache ram evicted the dirty block of data into the FIFO block in advance (yellow rectangle).
- After all, the processor is resumed and the data (*32'h8888_8888*) of address *32'h8001_f8bc* is read and output to the processor from the dcache (blue arrow).
- Later, the data (*32'h8888_8881*) of address *32'h8001_f8a0* is read and output to the processor from the dcache since it is a cache hit (orange arrow).

Test 10: Write Miss FIFO Hit followed by Read Hit

Figure 6-10 shows the simulation result for Test 10: Write Miss FIFO Hit followed by Read Hit.

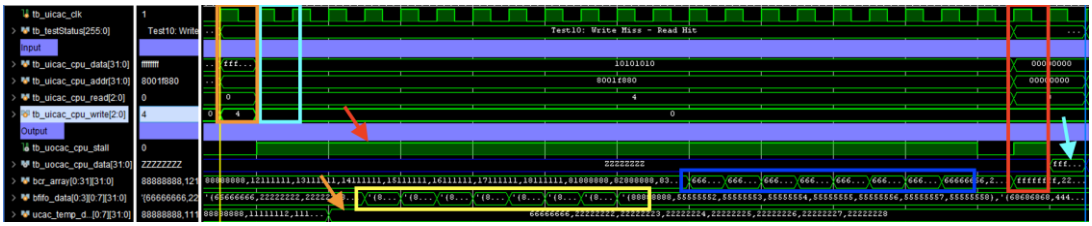

Figure 6-10: Simulation Result for Test 10: Write Miss FIFO Hit followed by Read Hit.

- In the 1st clock cycle, *32'hffff_ffff* is written to the dcache with address *32'h8001_f880* (orange rectangle).
- In the 2nd clock cycle, data existed in the address *32'h8001_f880* is read (light blue rectangle).
- There is a cache miss situation, implying that the address *32'h8001_f880* and its data is not present in the cache ram.
- The processor is stalled to read in the block of data (red arrow).
- The dcache recognized that the latest copy of the valid intended data is in the FIFO block.
- The intended data is first evicted from the FIFO block to the cache temporary buffer (orange arrow).
- In the next clock cycle, the dirty block of data with also index = *2'b00* is evicted by the cache ram to the FIFO block (yellow rectangle).
- Later, the valid copy of data is written back from the temporary buffer back to the cache ram for write operation to perform (yellow rectangle).
- After all, the processor is resumed, the data *32'hffff_ffff* is written into the dcache in the next clock cycle (red rectangle).
- As the dcache is busy writing in data, the processor is stalled again for one cycle.
- After all, the data (*32'hffff_ffff*) of address *32'h8001_f880* is read and output to the processor from the dcache (blue arrow).

Test 11: Read Miss FIFO Miss followed by Write Hit

Figure 6-11 and 6-12 shows the simulation result for Test 11: Read Miss FIFO Miss followed by Write Hit.

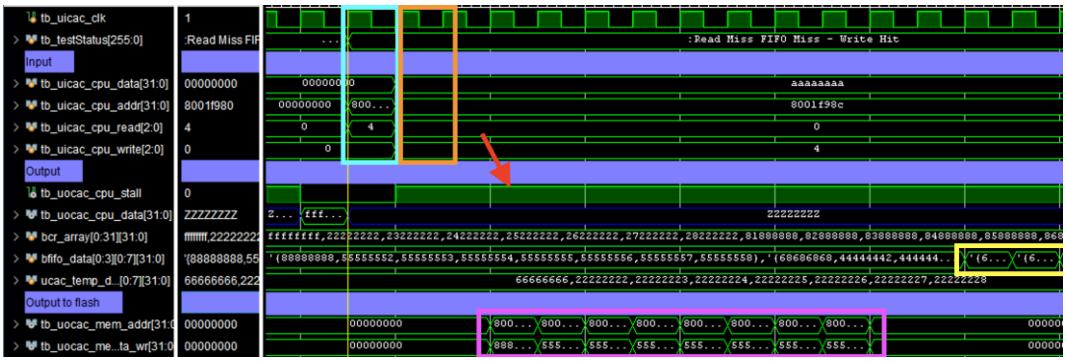

Figure 6-11: Simulation Result I for Test 11: Read Miss FIFO Miss followed by Write Hit.

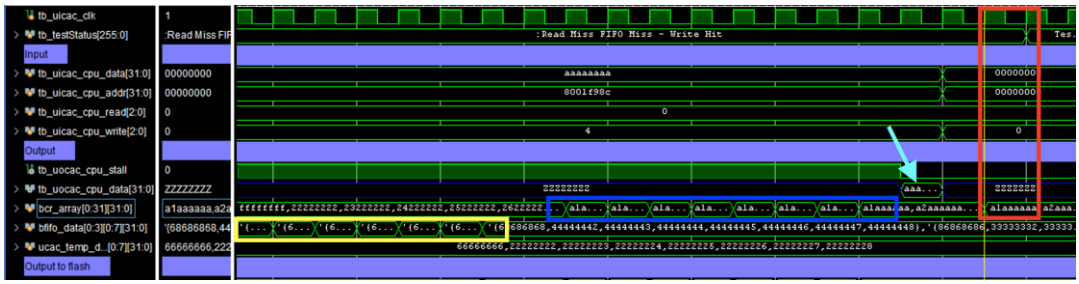

Figure 6-12: Simulation Result II for Test 11: Read Miss FIFO Miss followed by Write Hit.

- In the 1st clock cycle, data existed in the address *32'h8001_f980* is read (light blue rectangle).
- In the 2nd clock cycle, *32'haaaa_aaaa* is written to the dcache with address *32'h8001_f98c* (orange rectangle).
- There is a cache miss situation, implying that the address *32'h8001_f980* and its data is not present in the cache ram.
- The processor is stalled to read in the block of data (red arrow) from the flash memory (dark blue rectangle).
- However, before that, there is a block of dirty data with also index = *2'b00* existed in the cache ram.
- The cache ram has to evict the dirty block of data into the FIFO block in advance (yellow rectangle).

- At the moment, the FIFO block is full, indicating that it has to first write back the valid and dirty data back to the flash memory in order to receive new block of data (pink rectangle).
- After all, the processor is resumed and the data (*32'haaaa_aaa1*) of address *32'h8001_f980* is read and output to the processor from the dcache (blue arrow).
- Later, the data *32'haaaa_aaaa* is written into the dcache with address *32'h8001_f98c* since it is a cache hit (red rectangle).

6.2 CPU Data Hazard Forwarding Test

6.2.1 CPU Data Hazard Forwarding Test Plan

Name	Instruction		Hex Code	Description	Expected Output	Result
ID.rs and ID.rt Route Forwarding Test	addi	$s0, $zero, 20	0x20100014	No Forwarding	$s0 = 0x0000_0014	PASS
	addi	$s1, $zero, -8	0x2011fff8	No Forwarding	$s1 = 0xffff_fff8	PASS
	addi	$t0, $s1, 108	0x2228006c	ID.rs forward from EX	$t0 = 0x0000_0064	PASS
	addiu	$s2, $s1, 2	0x26320002	ID.rs forward from DF	$s2 = 0xffff_fffa	PASS
	sub	$s3, $s2, $t0	0x02489822	ID.rs forward from EX	$s3 = 0xffff_ff96	PASS
	subu	$s4, $s2, $t0	0x0248a023	ID.rs forward from DF	$s4 = 0xffff_ff96	PASS
	addu	$s5, $s3, $s3	0x0273a821	ID.rs forward from DF ID.rt forward from DF	$s5 = 0xffff_ff2c	PASS
	and	$t0, $s2, $s3	0x02534024	ID.rs forward from WB ID.rt forward from TC	$t0 = 0xffff_ff92	PASS
	andi	$t1, $t0, 15	0x3109000f	ID.rs forward from EX	$t1 = 0x0000_0002	PASS
	nor	$t2, $t0, $t1	0x01095027	ID.rs forward from DF ID.rt forward from EX	$t2 = 0x0000_006d	PASS
	or	$t3, $t1, $t2	0x012a5825	ID.rs forward from DF ID.rt forward from EX	$t3 = 0x0000_006f	PASS
	ori	$t3, $t3, 16	0x356b0010	ID.rs forward from EX	$t3 = 0x0000_007f	PASS
	sll	$t3, $t3, 10	0x000b5a80	ID.rs forward from EX	$t3 = 0x0001_fc00	PASS
	srl	$t3, $t3, 10	0x000b5a82	ID.rs forward from EX	$t3 = 0x0000_007f	PASS
	sra	$t3, $t3, 6	0x000b5983	ID.rs forward from EX	$t3 = 0x0000_0001	PASS

Table 6-2: CPU Data Hazard Forwarding Test Plan

6.2.3 CPU Data Hazard Forwarding Test Simulation Result

Table 6-4 shows the forwarding value used to indicate which forwarding operation to be carried out.

```
`define FWRD_EX      `FWRD_ALB_NB'b0100
`define FWRD_DF      `FWRD_ALB_NB'b0101
`define FWRD_TC      `FWRD_ALB_NB'b0110
`define FWRD_WB      `FWRD_ALB_NB'b0111
```

Table 6-3: Forwarding Operation based on the Forwarding Value

Figure 6-13 – 6-15 shows the simulation result for ID.rs and ID.rt Route Forwarding Test.

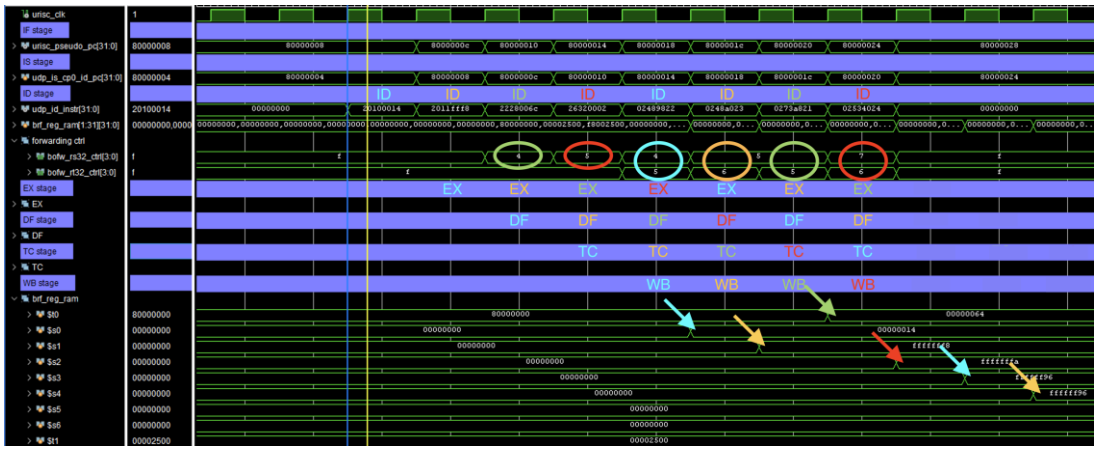

Figure 6-13: Simulation Result I for ID.rs and ID.rt Route Forwarding Test.

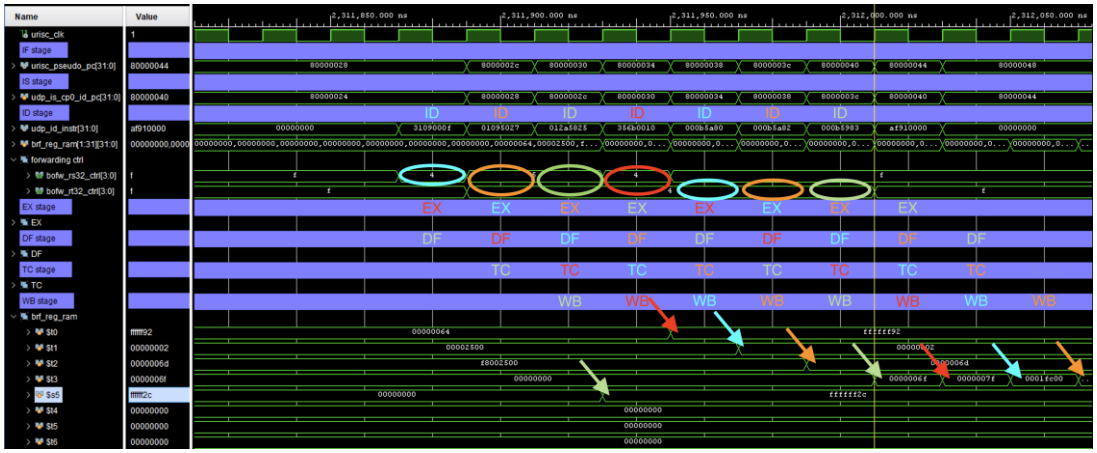

Figure 6-14: Simulation Result II for ID.rs and ID.rt Route Forwarding Test.

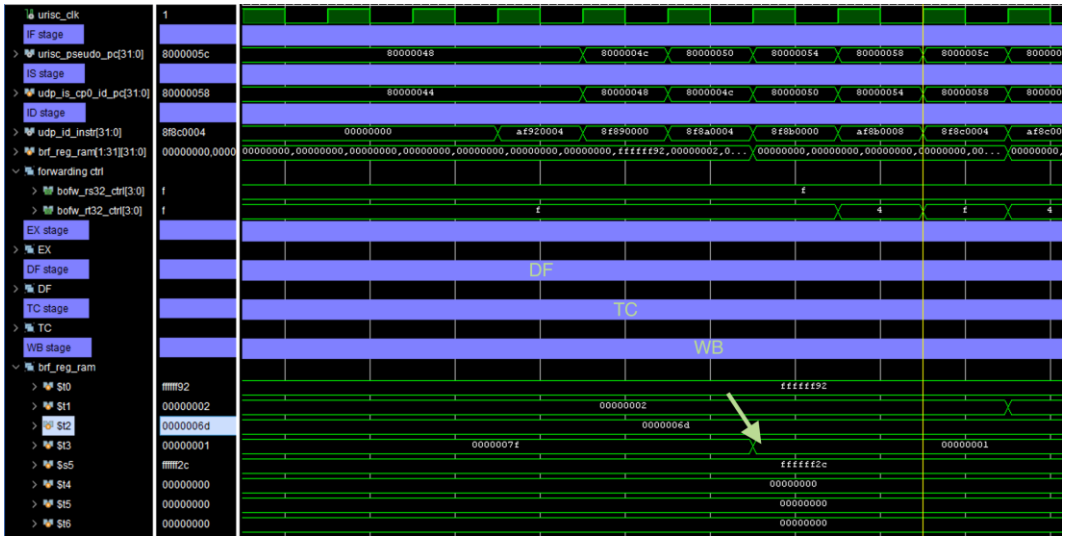

Figure 6-15: Simulation Result III for ID.rs and ID.rt Route Forwarding Test.

- From figure 6-13 – 6-15, we are able to observe that each instruction propagated from ID stage to WB stage.
- Each instruction is assigned with one colour and is indicated with its current stage at a particular clock cycle.
- The circles show the forwarding value used to determine the forwarding operation for ID.rs and ID.rt route during the execution (instruction decoding) of a particular instruction in ID stage.
- The arrows indicate the final outcome (value written into specific location in the register file) of each respective instruction.

6.3 CPU – D-Cache Integration Test

6.3.1 CPU – D-Cache Integration Test Plan

Name	Instruction		Hex Code	Description	Expected Output	Result
dcache store (sw)	lui or	$s6, 0x8001 $s6, $s6, 0xF800	0x3c168001 0x36d6f800	Load D-Cache starting address (0x8001_f800) into $s6	$s6 = 0x8001_f800	PASS
	sw	$s1,0 ($s6)	0xaed10000	Store $s1 content into location 0x8001_f800	dcache[0]= 0xf8ff_ffff	PASS
	sw	$s2,4 ($s6)	0xaed20004	Store $s2 content into location 0x8001_f804	dcache[1] = 0xfaff_ffff	PASS
dcache load (lw)	lw	$t2,0 ($s6)	0x8eca0000	Load content at location 0x8001_f800 into $t2	$t1 = 0xffff_fff8	PASS
	lw	$t1,4 ($s6)	0x8ec90004	Load content at location 0x8001_f804 into $t1	$t2 = 0xffff_fffa	PASS
dcache load-store	lw	$t3,4 ($s6)	0x8ecb0004	Load content at location 0x8001_f804 into $t3	$t3 = 0xffff_fffa	PASS
	sw	$t3,8 ($s6)	0xaecb0008	Store $t3 content into location 0x0x8001_f808 DF.rt forward from TC	dcache[2] = 0xfaff_ffff	PASS
	lw	$t4,0 ($s6)	0x8ecc0000	Load content at location 0x8001_f800 into $t4	$t4 = 0xffff_fff8	PASS
	sw	$t4,8 ($s6)	0xaecc0008	Store $t4 content into location 0x0x8001_f808 EX.rt forward from DF	dcache[2] = 0xf8ff_ffff	PASS
dcache load-use	lw	$t5, 0 ($s6)	0x8ecd0000	Load content at location 0x8001_f800 into $t5	$t5 = 0xffff_fff8	PASS
	lw	$t6, 4 ($s6)	0x8ece0004	Load content at location 0x8001_f800 into $t6	$t6 = 0xffff_fffa	PASS
	add	$t8, $t5,$t6	0x01aec020	Stall 2 clock cycles ID.rs forward from WB ID.rt forward from TC	$t8 = 0xffff_fff2	PASS
dcache sb, lb, lbu	addi	$t0, $zero, 0x99	0x20080099	Prepare value in $t0	$t0 = 0x0000_0099	PASS
	sb	$t0, 9 ($s6)	0xa2c80009	Store $t0 byte content into location 0x8001_f808	dcache[2] = 0xf8ff9988	PASS
	addi	$t0, $zero, 0xaa	0x200800aa	Prepare value in $t0	$t0 = 0x0000_00aa	PASS
	sb	$t0,10 ($s6)	0xa2c8000a	Store $t0 byte content into location 0x8001_f809	dcache[2] = 0xf8aa9988	PASS
	lb	$t0, 9 ($s6)	0x82c80009	Load byte content at location 0x8001_f809 into $t0	$t0 = 0xffff_ff99	PASS
	lb	$t0,10 ($s6)	0x82c8000a	Load byte content at location 0x8001_f80a into $t0	$t0 = 0xffff_ffaa	PASS
	lbu	$t0, 9 ($s6)	0x92c80009	Load unsigned byte content at location 0x8001_f809 into $t0	$t0 = 0x0000_0099	PASS
	lbu	$t0,10 ($s6)	0x92c8000a	Load unsigned byte content at location 0x8001_f80a into $t0	$t0 = 0x0000_00aa	PASS

Table 6-4: CPU – D-Cache Integration Test Plan

6.3.2 CPU – D-Cache Integration Test Simulation Result

Notes:

- The arrows indicate the final outcome of each respective instruction.
- Each instruction is associated with a specific colour and is innotated by the pipeline stage the instruction is currently located in.

D-Cache Store (sw) Test

Figure 6-16 and 6-17 shows the simulation result for D-Cache Store (sw) Test.

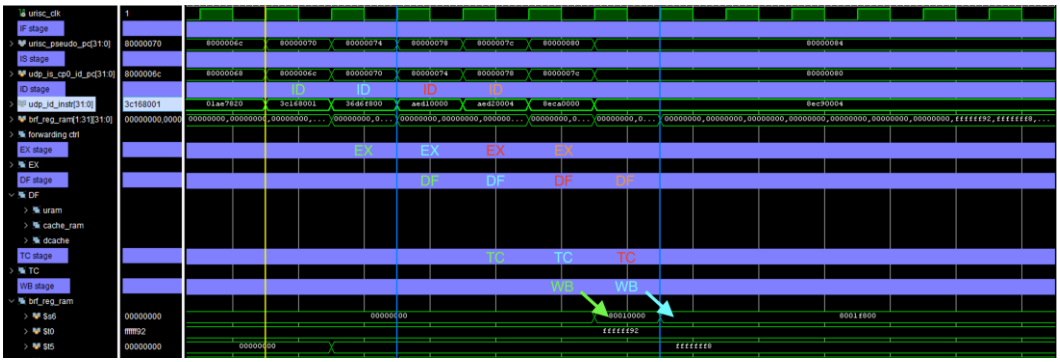

Figure 6-16: Simulation Result I for D-Cache Store (sw) Test.

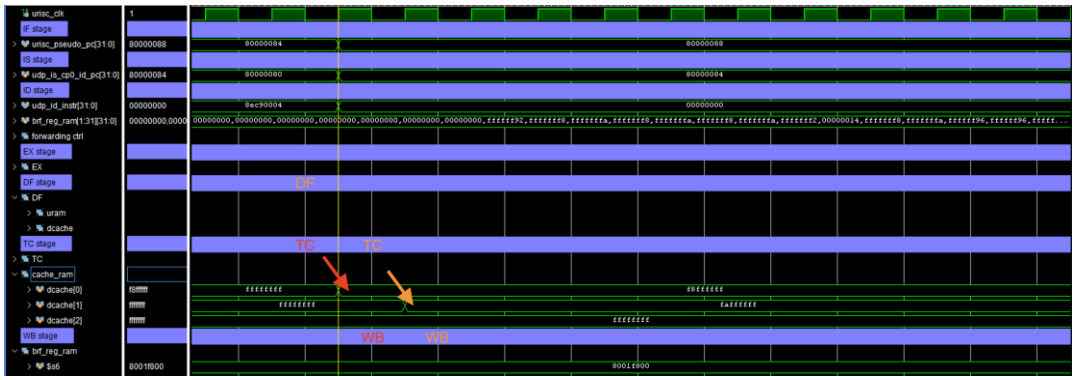

Figure 6-17: Simulation Result II for D-Cache Store (sw) Test.

- Firstly, the starting address of the .data section of the flash memory (*0x8001_f800*) is written into $s6 using instruction hex code *0x3c168000* (green colour) and *0x36d6f800* (blue colour).
- Instruction hex code *0xaed10000* (red colour) is used to store $s1 content *(0xffffffff8)* into location *0x8001_f800* (dcache[0]).
- Instruction hex code *0xaed20004* (orange colour) is used to store $s2 content *(0xfffffffa)* into location *0x8001_f804* (dcache[1]).

D-Cache Load (lw) Test

Figure 6-18 – 6-20 shows the simulation result for D-Cache Load (lw) Test.

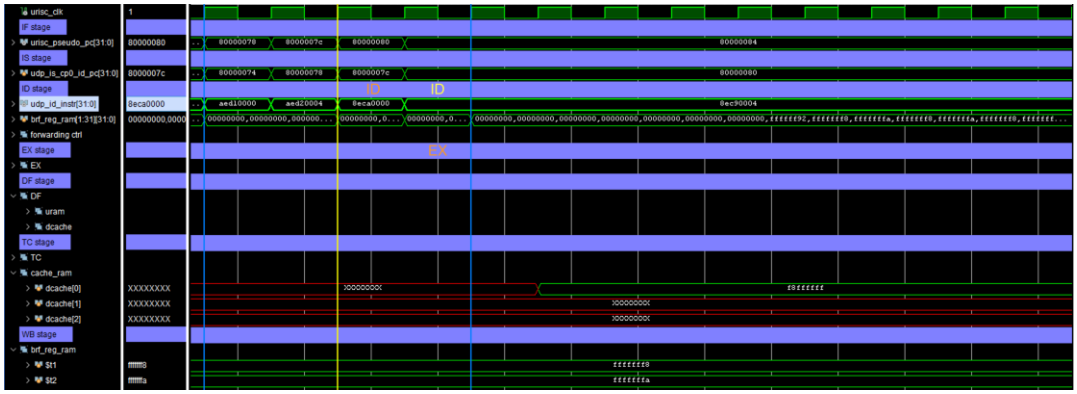

Figure 6-18: Simulation Result I for D-Cache Load (lw) Test.

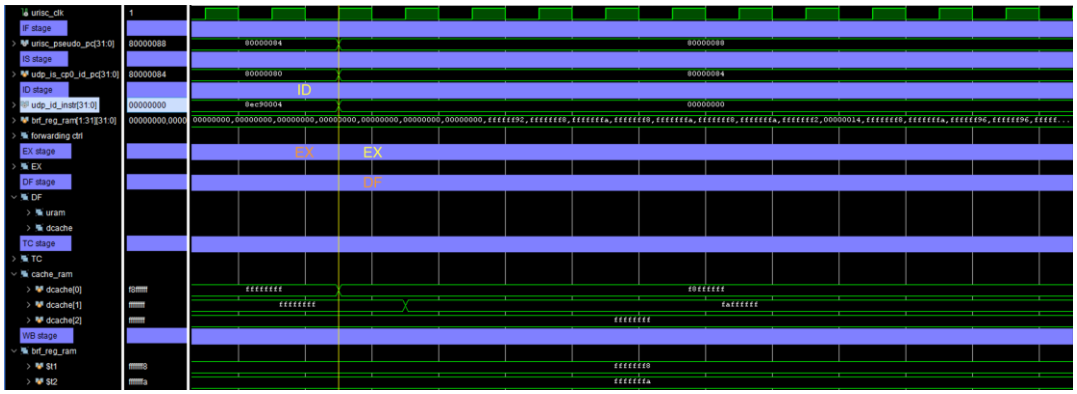

Figure 6-19: Simulation Result II for D-Cache Load (lw) Test.

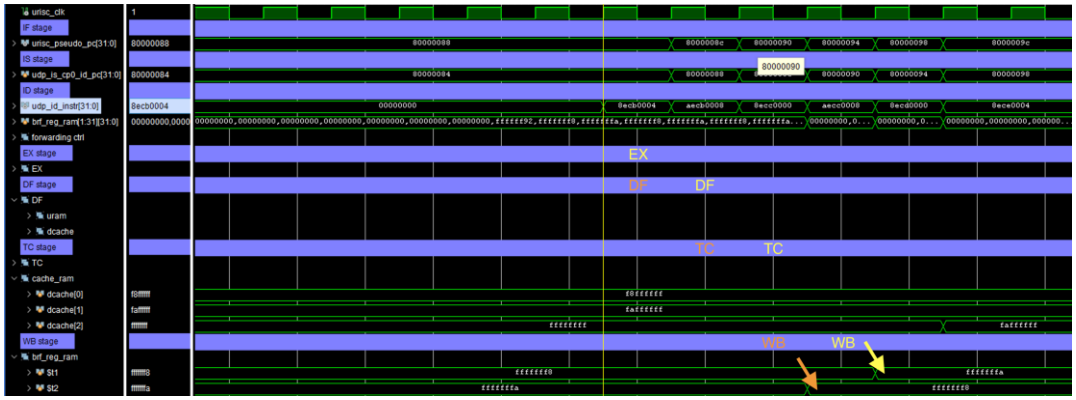

Figure 6-20: Simulation Result III for D-Cache Load (lw) Test.

- Instruction hex code *0x8eca0000* (orange colour) is used to load content *(0xffffffff8)* at location *0x8001_f800* (dcache[0]) into $t2.
- Instruction hex code *0x8ec90004* (yellow colour) is used to load content *(0xffffffffa)* at location *0x8001_f804* (dcache[1]) into $t1.

D-Cache Load-Store Test

Figure 6-21 shows the simulation result for D-Cache Load-Store Test.

Figure 6-21: Simulation Result for D-Cache Load-Store Test.

- Instruction hex code *0x8ecb0004* (yellow colour) is used to load content *(0xfffffffa)* at location *0x8001_f804* (dcache[1]) into $t3.
- Instruction hex code *0xaecb0008* (orange colour) is used to store $t3 content *(0xfffffffa)* into location *0x8001_f808* (dcache[2]).
- *bofw_df* is asserted to forward latest $t3 data from TC stage (load instruction) to DF stage (store instruction).
- Instruction hex code *0x8ecc0000* (blue colour) is used to load content *(0xfffffff8)* at location *0x8001_f800* (dcache[0]) into $t4.
- Instruction hex code *0xaecc0008* (green colour) is used to store $t4 content *(0xfffffff8)* into location *0x8001_f808* (dcache[2]).
- *bofw_df* is asserted to forward latest $t3 data from TC stage (load instruction) to DF stage (store instruction).
- The orange circle shows that the pipeline processor is stalled for one clock cycle.
- It is due to that the d-cache cache ram is busy writing in data (*0xaecb0008* store instruction) when the *0x8ecc0000* load instruction is attempting to read out data from it.

D-Cache Load-Use Test

Figure 6-22 and 6-23 shows the simulation result for D-Cache Load-Use Test.

Figure 6-22: Simulation Result I for D-Cache Load-Use Test.

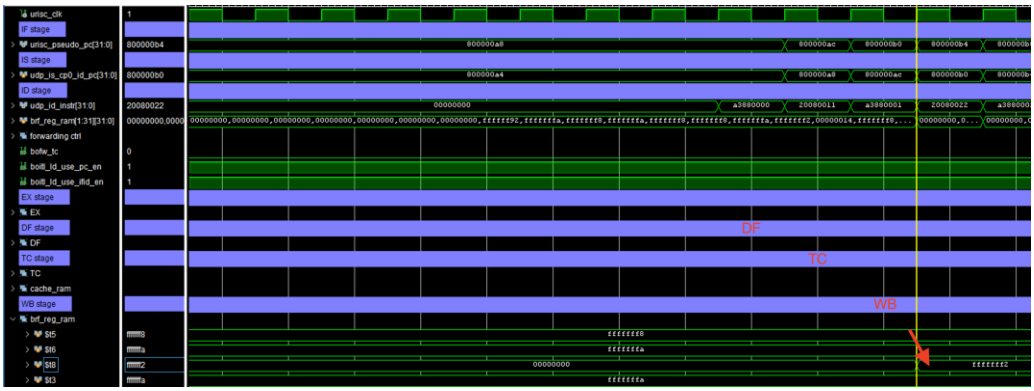

Figure 6-23: Simulation Result II for D-Cache Load-Use Test.

- Instruction hex code *0x8ecd0000* (green colour) is used to load content (*0xffffffff8*) at location *0x8001_f800* (dcache[0]) into $t5.
- Instruction hex code 0x8ece0004 (blue colour) is used to load content (*0xffffffffa*) at location *0x8001_f804* (dcache[1]) into $t6.
- Instruction hex code *0x01aec020* (red colour) adds the $t5 content (*0xffffffff8*) and $t6 (*0xffffffffa*) content and stores the result in $t8.
- As the add instruction used the $t6 contents which is not yet ready, data hazard takes place.
- The program counter, IFIS and IFID pipeline register are interlock for two clock cycle, at the same time the IDEX pipeline register is flushed with zeroes.
- This allows the *0x8ece0004* (load instruction) to propagate and execute till the TC stage in advance where the loaded memory is later forwarded to the ID stage for add instruction.

- The green circle shows that the pipeline processor is stalled as the cache ram is busy writing in data when the *0x8ecd0000* load instruction is attempting to read out data from it.

D-Cache SB, LB, LBU Test

Figure 6-24 shows the simulation result for D-Cache SB Test.

Figure 6-24: Simulation Result for D-Cache SB Test.

- Instruction hex code *0x20080099* (red colour) prepares the the data *(0x00000099)* ready in $t0.
- Instruction hex code *0xa2c80009* (orange colour) is used to store $t0 byte content *(0x99)* into location *0x8001_f809* (dcache[2][1]).
- Instruction hex code *0x200800aa* (yellow colour) prepares the the data *(0x000000aa)* ready in $t0.
- Instruction hex code *0xa2c8000a* (green colour) is used to store $t0 byte content *(0xaa)* into location *0x8001_f80a* (dcache[2][2]).

Figure 6-25 shows the simulation result for D-Cache LB Test.

Figure 6-25: Simulation Result for D-Cache LB Test.

- Instruction hex code *0x82c80009* (yellow colour) is used to load signed byte content *(0x99)* at location *0x8001_f809* (dcache[2][1])) into $t0 *(0xffffff99)*.
- Instruction hex code *0x82c8000a* (blue colour) is used to load signed byte content *(0xaa)* at location *0x8001_f80a* (dcache[2][2])) into $t0 *(0xffffffaa)*.

Figure 6-26 shows the simulation result for D-Cache LBU Test.

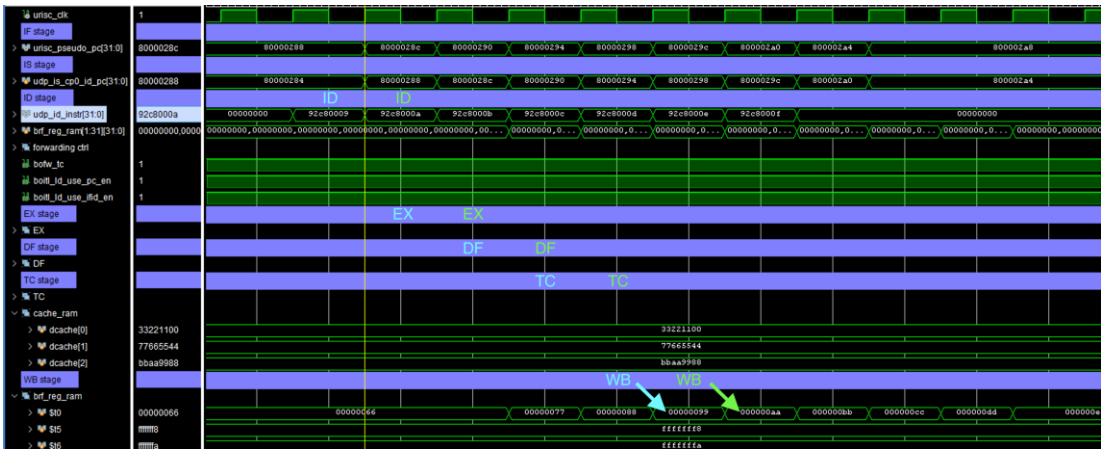

Figure 6-26: Simulation Result for D-Cache LBU Test.

- Instruction hex code *0x92c80009* (blue colour) is used to load unsigned byte content *(0x99)* at location *0x8001_f809* (dcache[2][1])) into $t0 *(0x00000099)*.
- Instruction hex code *0x92c8000a* (green colour) is used to load unsigned byte content *(0xaa)* at location *0x8001_f80a* (dcache[2][2])) into $t0 *(0x000000aa)*.

Chapter 7: Synthesis and Implementation

Synthesis and implementation of the 7-stage pipeline processor should be performed by using Xilinx Vivado once its behavioral simulation is successfully done and verified. In order to compare the timing analysis result of this project with the existing 6-stage pipeline processor and 5-stage pipeline processor, we have to first synthesize and implement it by using Xilinx Vivado. The FPGA board used for the synthesis and implementation is Artix-7: Arty A7-100T where its default part is XC7A100TCSG324-1.

7.1 Synthesis and Implementation Settings

The default synthesis settings by Xilinx Vivado should be modified before running it. The *-flatten_ hierarchy* option should be configured to *none* so that the synthesis tool will not flatten the hierarchy. This insists that the output of synthesis has the exact same hierarchy as its original RTL [15]. Figure 7-1 below shows the synthesis setting required.

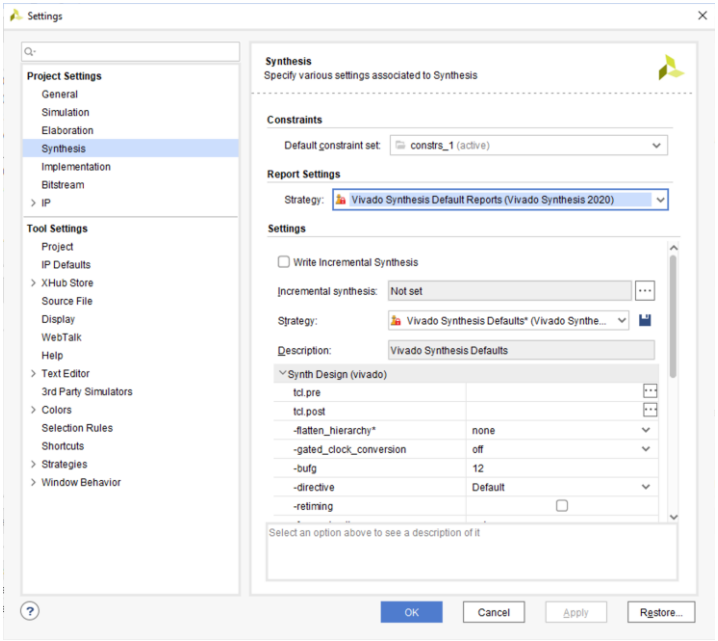

Figure 7-1: Synthesis Setting required for this Project

The default implementation settings by Xilinx Vivado should also be modified before running the implementation. The *-opt_design* option should be *disabled* so that the logical design is not optimized. By disabling the *-opt_design*, Vivado will not perform its default optimization like Retarget, Constant Propagation, Sweep and Block RAM Power optimizations on your design [16]. Figure 7-2 below shows the implementation setting required.

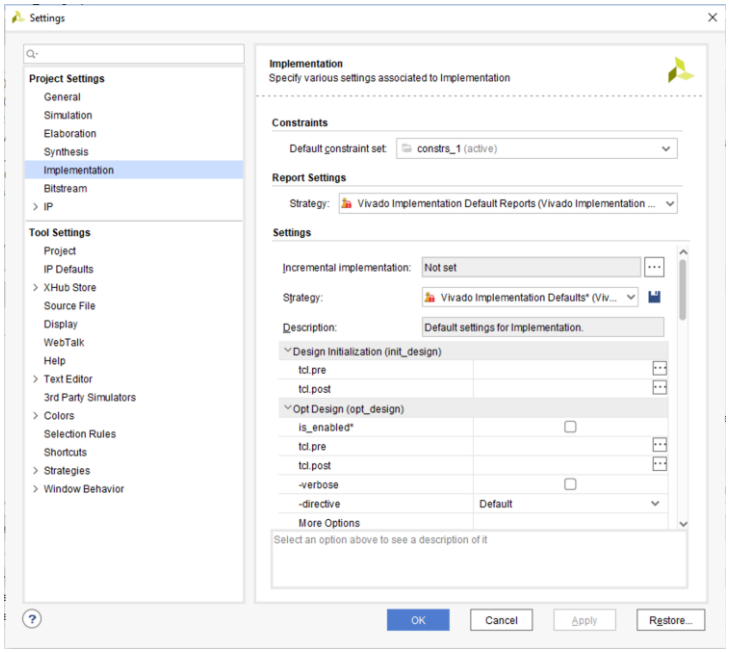

Figure 7-2: Implementation Setting required for this Project

7.2 Timing Analysis

Once the synthesis and implementation are done by using Xilinx Vivado, a TCL script developed by seniors could be run from the console in the Implementation windows to directly obtain the timing delay for each stage of the pipeline processors. The format of the console command is “source <location of the script file>. A timing delay file is obtained where the information is categorized into 5 columns as shown in the table below.

Location	Where the cell or port is placed on the device
Delay Type	The unisim primitive and the particular timing arc followed by the path.
Incr(ns)	The value of the incremental delay associated to a unisim primitive timing arc or a net. It can also show of a constraint such as input/output delay or clock uncertainty.
Path(ns)	The accumulated delay after each segment of the path. On a given line, its value is the accumulated value from the previous + the incremental delay of the current line.
Netlist Resource(s)	The name of the netlist object traversed.

Table 7-1: Definition of Information in Timing Delay File [12]

7.3 Timing Delay of 7-Stage Pipeline Processor

Table 7-2 shows the timing delay of the 7-stage pipeline processor. The full timing delay details can be found in *Appendix B*.

Pipeline Stage	Functional Unit	Component Delay (ns)
DF	D-Cache	12.106
	URAM	13.248
TC	D-Cache	12.128
	Datapath Unit	7.137

Table 7-2: Component Delay of Significant Functional Units in DF and TC stage

Pipeline Stage	IF	IS	ID	EX	DF	TC	WB
Timing Delay (ns)	6.9140	11.918	12.368	14.795	13.248	12.128	3.2230

Table 7-3: Timing Delay of the 7-stage Pipeline Processor

From the timing delay shown in Table 7-3 above, the clock rate of the newly developed 7-stage pipeline processor is determined using the longest time delay of the pipeline stages, which is 14.795ns from EX stage. The clock rate is calculated as below.

$$Clock\ rate\ of\ 7-stage\ pipeline\ processor = \frac{1}{14.795ns} = 67.590MHz$$

7.4 Timing Delay of 6-Stage Pipeline Processor

Table 7-4 shows the timing delay of the 6-stage pipeline processor. The full timing delay details can be found in *Appendix C*.

Pipeline Stage	IF	IS	ID	EX	MEM	WB
Timing Delay (ns)	7.126	13.063	11.889	13.638	17.511	3.402

Table 7-4: Timing Delay of the 6-stage Pipeline Processor

From the timing delay shown in Table 7-4 above, the clock rate of the existing 6-stage pipeline processor is determined using the longest time delay of the pipeline stages, which is 17.511ns from MEM stage. The clock rate is calculated as below.

$$Clock\ rate\ of\ 6-stage\ pipeline\ processor = \frac{1}{17.511ns} = 57.107MHz$$

7.5 Timing Delay of 5-Stage Pipeline Processor

Table 7-5 shows the timing delay of the 5-stage pipeline processor.

Pipeline Stage	IF	ID	EX	MEM	WB
Timing Delay (ns)	14.118	12.551	14.717	18.262	3.332

Table 7-5: Timing Delay of the 5-stage Pipeline Processor

From the timing delay shown in Table 7-5 above, the clock rate of the existing 5-stage pipeline processor is determined using the longest time delay of the pipeline stages, which is 17.511ns from MEM stage. The clock rate is calculated as below.

$$Clock\ rate\ of\ 6-stage\ pipeline\ processor = \frac{1}{18.262ns} = 54.759MHz$$

Chapter 8: Conclusion and Future Work

8.1 Conclusion

In conclusion, all the objectives of this project have been fully achieved. Previously, in the existing RISC 32-bit pipeline processor, the data cache unit contributed a large timing delay for the MEM stages. In this project, the new 7-stage pipeline processor designed and implemented counters this problem. The MEM stage of the existing pipeline processor is decomposed into two new stages which known as DF and TC stage. *Chapter 5* of this report shows the comprehensive documentation about the microarchitecture design specifications of the 7-stage pipeline processor.

Besides, a complete test plan is also created during this project to verify its functional correctness. All of the simulation results can be found in *Chapter 6* of this report. Lastly, the 7-stage pipeline processor developed is synthesized and implemented using the FPGA technology in order to retrieve the timing delay of each pipeline stage. The related information should be available in *Chapter 7* of this project.

The timing delay has a significant drop from the existing 17.511ns (MEM stage of the 6-stage pipeline processor) into 13.248ns (DF stage) and 12.128ns (TC stage). The overall timing delay for each processor pipeline stage is now considered balance. Currently, the newly developed 7-stage pipeline processor runs at a higher processor clock rate which is 18% faster than the existing 6-stage pipeline processor and 23% faster than the existing 5-stage pipeline processor.

8.2 Future Work

In future, the on-board testing of the newly developed 7-stage pipeline processor may need to be carried out. Currently, the 7-stage pipeline processor is only synthesized and implemented into the Artix-7: Arty A7-100T board using the Vivado Design Suite tools to obtain its timing delay for each stage. The onboard testing should be further carried out to assure that it can operate safely at the processor clock rate proposed in this report.

Besides, the pipelined cache unit developed could be further reviewed and modified in order to make it functions as both Instruction Cache (I-Cache) and Data Cache (D-Cache). Last but not least, the SDRAM, Memory Management Unit (MMU) and the Translation Lookaside Buffer (TLB) developed by seniors could be integrated to the existing 7-stage pipelined processor in order to achieve an 8-stage pipelined processor.

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Appendices A: Testbench for Pipelined Cache Unit

```
//####################################################################
/*
        Project/Module : tb_ucache
        File name : tb_ucache.v
        Author : Choo Jia Zheng
        Code type : Verilog
        Description : Testbench for cache unit (without pipeline)
*/
//####################################################################

`default_nettype none


module tb_ucache();

//output
wire [31:0]    tb_uocac_cpu_data;
wire [31:0]    tb_uocac_mem_addr;
wire [31:0]     tb_uocac_mem_data_wr;
wire [31:0]    tb_uocac_mem_lmc_data;
wire               tb_uocac_cpu_stall;
wire           tb_uocac_miss;
wire           tb_uocac_mem_read;
wire               tb_uocac_mem_write;
wire           tb_uocac_mem_data_ready;
wire [3:0]      tb_uocac_mem_sel;
wire            tb_uocac_mem_write_done;

//input
reg [31:0]     tb_uicac_cpu_addr;
reg [31:0]     tb_uicac_cpu_data;
reg [2:0]      tb_uicac_cpu_read; //{word,halfword,byte}
reg [2:0]      tb_uicac_cpu_write;//{word,halfword,byte}
reg [31:0]     tb_uicac_mem_data_rd;
reg            tb_uicac_mem_ack;
reg            tb_uicac_mem_lmc_same;
reg             tb_uicac_reconfig;
reg             tb_uicac_cp0_exc_flag;
reg             tb_uicac_mem_busy;
reg             tb_uicac_fw_load_data;
reg            tb_uicac_rst;
reg            tb_uicac_clk;

//register for testbench
reg [255:0]     tb_testStatus;
integer         tb_i;

//connection
ucache #(32,8,4,25,2,3,2)     //#(256,8,32,22,5,3,2)
data_cache
(
//output
.uocac_cpu_data             (tb_uocac_cpu_data),
.uocac_mem_addr             (tb_uocac_mem_addr),
.uocac_mem_data_wr          (tb_uocac_mem_data_wr),
.uocac_mem_lmc_data         (tb_uocac_mem_lmc_data),
.uocac_cpu_stall            (tb_uocac_cpu_stall),
.uocac_miss                 (tb_uocac_miss),
.uocac_mem_read             (tb_uocac_mem_read),
.uocac_mem_write            (tb_uocac_mem_write),
.uocac_mem_data_ready       (tb_uocac_mem_data_ready),
.uocac_mem_sel              (tb_uocac_mem_sel),
.uocac_mem_write_done       (tb_uocac_mem_write_done),

//input
.uicac_cpu_addr             (tb_uicac_cpu_addr),
.uicac_cpu_data             (tb_uicac_cpu_data),
.uicac_cpu_read             (tb_uicac_cpu_read),
.uicac_cpu_write            (tb_uicac_cpu_write),
.uicac_mem_data_rd          (tb_uicac_mem_data_rd),
.uicac_mem_ack              (tb_uicac_mem_ack),
.uicac_mem_lmc_same         (tb_uicac_mem_lmc_same),
```

```
.uicac_reconfig             (tb_uicac_reconfig),
.uicac_cp0_exc_flag         (tb_uicac_cp0_exc_flag),
.uicac_mem_busy             (tb_uicac_mem_busy),
.uicac_fw_load_data         (tb_uicac_fw_load_data),
.uicac_rst                  (tb_uicac_rst),
.uicac_clk                  (tb_uicac_clk)
);

//Clock waveform generation.
initial tb_uicac_clk                <= 1'b1;
always #25 tb_uicac_clk    = ~tb_uicac_clk;

initial begin
//code here
//------------------------Initialization------------------------------
@(posedge tb_uicac_clk);
tb_testStatus             <= "Initialization";
tb_uicac_cpu_addr         <= 32'b0;
tb_uicac_cpu_data         <= 32'b0;
tb_uicac_cpu_read         <= 3'b0;
tb_uicac_cpu_write        <= 3'b0;
tb_uicac_mem_data_rd      <= 32'b0;
tb_uicac_mem_ack          <= 1'b0;
tb_uicac_mem_lmc_same     <= 1'b0;
tb_uicac_reconfig         <= 1'b0;
tb_uicac_cp0_exc_flag     <= 1'b0;
tb_uicac_mem_busy         <= 1'b0;
tb_uicac_fw_load_data     <= 1'b0;
tb_uicac_rst              <= 1'b0;

//------------------------Test 1: Reset Test------------------------------
@(posedge tb_uicac_clk);
tb_testStatus             <= "Test1:Reset";
tb_uicac_rst              <= 1'b1;

@(posedge tb_uicac_clk);
tb_uicac_rst              <= 1'b0;

@(posedge tb_uicac_clk);

//------------------------Test 2: Write Miss - Read Hit-------------------------------
       -
@(posedge tb_uicac_clk);
tb_testStatus             <= "Test2: Write Miss - Read Hit";     //addr: 8001_F800
       data: 8888_8888
tb_uicac_cpu_addr         <= 32'h8001_F800;
tb_uicac_cpu_data         <= 32'h8888_8888;
tb_uicac_cpu_write        <= 3'b100;

@(posedge tb_uicac_clk);                                        //addr: 8001_F80C
       data: 1111_1114
tb_uicac_cpu_addr         <= 32'h8001_F80C;
tb_uicac_cpu_write        <= 3'b000;
tb_uicac_cpu_read         <= 3'b100;

for (tb_i=0; tb_i<8; tb_i=tb_i+1) begin
@(posedge tb_uicac_clk);
tb_uicac_mem_ack          <= 1'b1;
tb_uicac_mem_data_rd      <= 32'h1111_1111 + tb_i;
end

repeat(5)@(posedge tb_uicac_clk);
tb_testStatus             <= "Test2: END";
tb_uicac_cpu_read        <= 3'b000;
tb_uicac_cpu_addr         <= 32'h0000_0000;
tb_uicac_cpu_data         <= 32'h0000_0000;
tb_uicac_mem_ack          <= 1'b0;
@(posedge tb_uicac_clk);

//------------------------Test 3: Read Hit - Read Hit-------------------------------
@(posedge tb_uicac_clk);
tb_testStatus             <= "Test3: Read Hit - Read Hit";      //addr: 8001_F804
       data: 1111_1112
```

```
tb_uicac_cpu_addr         <= 32'h8001_F804;                    //addr: 8001_F808
       data: 1111_1113
tb_uicac_cpu_read         <= 3'b100;

@(posedge tb_uicac_clk);
tb_uicac_cpu_addr         <= 32'h8001_F808;

@(posedge tb_uicac_clk);
tb_testStatus             <= "Test3: END";
tb_uicac_cpu_read        <= 3'b000;
tb_uicac_cpu_addr         <= 32'h0000_0000;
@(posedge tb_uicac_clk);

//----------------------Test 4: Write Miss FIFO Miss-------------------------
@(posedge tb_uicac_clk);
tb_testStatus             <= "Test4: Write Miss - Read Hit";    //addr: 8001_F880
       data: 6666_6666
tb_uicac_cpu_addr         <= 32'h8001_F880;                    //addr: 8001_F884
       data: 2222_2222
tb_uicac_cpu_data         <= 32'h6666_6666;
tb_uicac_cpu_write         <= 3'b100;

@(posedge tb_uicac_clk);
tb_uicac_cpu_addr         <= 32'h8001_F884;
tb_uicac_cpu_data         <= 32'h0000_0000;
tb_uicac_cpu_write        <= 3'b000;
tb_uicac_cpu_read         <= 3'b100;

repeat(9)@(posedge tb_uicac_clk);

for (tb_i=0; tb_i<8; tb_i=tb_i+1) begin
@(posedge tb_uicac_clk);
tb_uicac_mem_ack          <= 1'b1;
tb_uicac_mem_data_rd      <= 32'h2222_2221 + tb_i;
end

@(posedge tb_uicac_clk);
tb_uicac_mem_ack          <= 1'b0;

repeat(4)@(posedge tb_uicac_clk);
tb_testStatus             <= "Test4: END";
tb_uicac_cpu_addr         <= 32'h0000_0000;
tb_uicac_cpu_read         <= 3'b000;
tb_uicac_cpu_data         <= 32'h0000_0000;
@(posedge tb_uicac_clk);

//------------------------Test 5: Read Miss FiFo Hit - Read Hit-----------------------
       ---------
@(posedge tb_uicac_clk);
tb_testStatus             <= "Test5: Read Miss Fifo Hit - Read Hit";
tb_uicac_cpu_addr         <= 32'h8001_F810;                    //addr: 8001_F810
       data: 1111_1115
tb_uicac_cpu_read         <= 3'b100;

@(posedge tb_uicac_clk);
tb_uicac_cpu_addr         <= 32'h8001_F800;                    //addr: 8001_F800
       data: 8888_8888

repeat(21)@(posedge tb_uicac_clk);
tb_testStatus             <= "Test5: END";
tb_uicac_cpu_addr         <= 32'h0000_0000;
tb_uicac_cpu_read         <= 3'b000;
@(posedge tb_uicac_clk);

//----------------------Load memory->index=01 - Read Hit-------------------------
@(posedge tb_uicac_clk);
tb_testStatus             <= "Load memory->index=01 - Read Hit";
tb_uicac_cpu_addr         <= 32'h8001_F820;                    //addr: 8001_F820
       data: 3333_3331
tb_uicac_cpu_read         <= 3'b100;

@(posedge tb_uicac_clk);
tb_uicac_cpu_addr         <= 32'h8001_F828;                    //addr: 8001_F820
       data: 3333_3333
```

```
for (tb_i=0; tb_i<8; tb_i=tb_i+1) begin
@(posedge tb_uicac_clk);
tb_uicac_mem_ack          <= 1'b1;
tb_uicac_mem_data_rd      <= 32'h3333_3331 + tb_i;
end

@(posedge tb_uicac_clk);
tb_uicac_mem_ack          <= 1'b0;

repeat(2)@(posedge tb_uicac_clk);
tb_testStatus             <= "Load memory->index=01: END";
tb_uicac_cpu_addr         <= 32'h0000_0000;
tb_uicac_cpu_read         <= 3'b000;
@(posedge tb_uicac_clk);

//----------------------Load memory->index=10 - Read Hit-------------------------
@(posedge tb_uicac_clk);
tb_testStatus             <= "Load memory->index=10 - Read Hit";
tb_uicac_cpu_addr         <= 32'h8001_F840;                    //addr: 8001_F820
       data: 4444_4441
tb_uicac_cpu_read         <= 3'b100;

@(posedge tb_uicac_clk);
tb_uicac_cpu_addr         <= 32'h8001_F84C;                    //addr: 8001_F820
       data: 4444_4444

for (tb_i=0; tb_i<8; tb_i=tb_i+1) begin
@(posedge tb_uicac_clk);
tb_uicac_mem_ack          <= 1'b1;
tb_uicac_mem_data_rd      <= 32'h4444_4441 + tb_i;
end

@(posedge tb_uicac_clk);
tb_uicac_mem_ack          <= 1'b0;

repeat(2)@(posedge tb_uicac_clk);
tb_testStatus             <= "Load memory->index=10: END";
tb_uicac_cpu_addr         <= 32'h0000_0000;
tb_uicac_cpu_read         <= 3'b000;
@(posedge tb_uicac_clk);

//----------------------Load memory->index=11 - Read Hit-------------------------
@(posedge tb_uicac_clk);
tb_testStatus             <= "Load memory->index=11 - Read Hit";
tb_uicac_cpu_addr         <= 32'h8001_F87C;                    //addr: 8001_F87C
       data: 5555_5558
tb_uicac_cpu_read         <= 3'b100;

@(posedge tb_uicac_clk);
tb_uicac_cpu_addr         <= 32'h8001_F860;                    //addr: 8001_F860
       data: 5555_5551

for (tb_i=0; tb_i<8; tb_i=tb_i+1) begin
@(posedge tb_uicac_clk);
tb_uicac_mem_ack          <= 1'b1;
tb_uicac_mem_data_rd      <= 32'h5555_5551 + tb_i;
end

@(posedge tb_uicac_clk);
tb_uicac_mem_ack          <= 1'b0;

repeat(2)@(posedge tb_uicac_clk);
tb_testStatus             <= "Load memory->index=11: END";
tb_uicac_cpu_addr         <= 32'h0000_0000;
tb_uicac_cpu_read         <= 3'b000;
@(posedge tb_uicac_clk);

//-----------------------Test 6: Write Hit - Write Hit ------------------------------
       --
@(posedge tb_uicac_clk);
tb_testStatus             <= "Test6: Write Hit - Write Hit";
tb_uicac_cpu_addr         <= 32'h8001_F820;                    //addr: 8001_F820
       data: 8686_8686
```

```
tb_uicac_cpu_data         <= 32'h8686_8686;
tb_uicac_cpu_write        <= 3'b100;

@(posedge tb_uicac_clk);
tb_uicac_cpu_addr         <= 32'h8001_F840;                    //addr: 8001_F840
       data: 6868_6868
tb_uicac_cpu_data         <= 32'h6868_6868;
tb_uicac_cpu_write        <= 3'b100;

@(posedge tb_uicac_clk);
tb_testStatus             <= "Test6: END";
tb_uicac_cpu_addr         <= 32'h0000_0000;
tb_uicac_cpu_data         <= 32'h0000_0000;
tb_uicac_cpu_write        <= 3'b000;
@(posedge tb_uicac_clk);

//-----------------------Test 7: Write Hit - Read Miss Fifo Miss--------------------
       ----------
@(posedge tb_uicac_clk);
tb_testStatus             <= "Test7: Write Hit - Read Miss Fifo Miss";
tb_uicac_cpu_addr         <= 32'h8001_F860;                    //addr: 8001_F860
       data: 8888_8888
tb_uicac_cpu_data         <= 32'h8888_8888;
tb_uicac_cpu_write        <= 3'b100;

@(posedge tb_uicac_clk);
tb_uicac_cpu_addr         <= 32'h8001_F8E0;                    //addr: 8001_F860
       data: 8888_8888
tb_uicac_cpu_data         <= 32'h0000_0000;                    //index=11
tb_uicac_cpu_write        <= 3'b000;
tb_uicac_cpu_read         <= 3'b100;

repeat(10)@(posedge tb_uicac_clk);

for (tb_i=0; tb_i<8; tb_i=tb_i+1) begin
@(posedge tb_uicac_clk);
tb_uicac_mem_ack          <= 1'b1;
tb_uicac_mem_data_rd      <= 32'h6666_6661 + tb_i;
end

repeat(3)@(posedge tb_uicac_clk);
tb_testStatus             <= "Test7: END";
tb_uicac_cpu_addr         <= 32'h0000_0000;
tb_uicac_cpu_read         <= 3'b000;
tb_uicac_mem_ack          <= 1'b0;
@(posedge tb_uicac_clk);

//----------------------Test 8: Read Miss Fifo Miss - Read Hit-----------------------
       -
@(posedge tb_uicac_clk);
tb_testStatus             <= "Test8: Read Miss Fifo Miss - Read Hit";
tb_uicac_cpu_addr         <= 32'h8001_F8C8;                    //addr: 8001_F8C8
       data: 7777_7773
tb_uicac_cpu_read         <= 3'b100;                           //index=10

@(posedge tb_uicac_clk);
tb_uicac_cpu_addr         <= 32'h8001_F8DC;                    //addr: 8001_F8C8
       data: 7777_7778
tb_uicac_cpu_read         <= 3'b100;                           //index=10

repeat(9)@(posedge tb_uicac_clk);

for (tb_i=0; tb_i<8; tb_i=tb_i+1) begin
@(posedge tb_uicac_clk);
tb_uicac_mem_ack          <= 1'b1;
tb_uicac_mem_data_rd      <= 32'h7777_7771 + tb_i;
end

repeat(3)@(posedge tb_uicac_clk);
tb_testStatus             <= "Test8: END";
tb_uicac_cpu_addr         <= 32'h0000_0000;
tb_uicac_cpu_read         <= 3'b000;
tb_uicac_mem_ack          <= 1'b0;
@(posedge tb_uicac_clk);
```

```
//----------------------Test 9: Read Miss Fifo Miss - Read Hit-----------------------
       -
@(posedge tb_uicac_clk);
tb_testStatus             <= "Test9: Read Miss Fifo Miss - Read Hit";
tb_uicac_cpu_addr         <= 32'h8001_F8BC;                    //addr: 8001_F8BC
       data: 8888_8888
tb_uicac_cpu_read         <= 3'b100;                           //index=01

@(posedge tb_uicac_clk);
tb_uicac_cpu_addr         <= 32'h8001_F8A0;                    //addr: 8001_F8A0
       data: 8888_8881
tb_uicac_cpu_read         <= 3'b100;                           //index=01

repeat(9)@(posedge tb_uicac_clk);

for (tb_i=0; tb_i<8; tb_i=tb_i+1) begin
@(posedge tb_uicac_clk);
tb_uicac_mem_ack          <= 1'b1;
tb_uicac_mem_data_rd      <= 32'h8888_8881 + tb_i;
end

repeat(3)@(posedge tb_uicac_clk);
tb_testStatus             <= "Test9: END";
tb_uicac_cpu_addr         <= 32'h0000_0000;
tb_uicac_cpu_read         <= 3'b000;
tb_uicac_mem_ack          <= 1'b0;
@(posedge tb_uicac_clk);

//-----------------------Test 10: Write Miss Fifo Hit - Read Hit--------------------
       -----------
@(posedge tb_uicac_clk);
tb_testStatus             <= "Test10: Write Miss - Read Hit";
tb_uicac_cpu_addr         <= 32'h8001_F880;                     //addr: 8001_F880
       data: 6666_6666 -> FFFF_FFFF
tb_uicac_cpu_data         <= 32'hFFFF_FFFF;
tb_uicac_cpu_write        <= 3'b100;

@(posedge tb_uicac_clk);
tb_uicac_cpu_data         <= 32'h1010_1010; //purposely try with the value (not
       significant)
tb_uicac_cpu_write        <= 3'b000;
tb_uicac_cpu_read         <= 3'b100;

repeat(21)@(posedge tb_uicac_clk);
tb_testStatus             <= "Test10: END";
tb_uicac_cpu_addr         <= 32'h0000_0000;
tb_uicac_cpu_data         <= 32'h0000_0000;
tb_uicac_cpu_read         <= 3'b000;
@(posedge tb_uicac_clk);

//----------------------Test 11: Read Miss Fifo Miss - Read Hit----------------------
       --
@(posedge tb_uicac_clk);
tb_testStatus             <= "Test11 :Read Miss FIFO Miss - Write Hit";
tb_uicac_cpu_addr         <= 32'h8001_F980;                    //addr: 8001_F980
       data: AAAA_AAA1
tb_uicac_cpu_read         <= 3'b100;                           //addr: 8001_F98C
       data: AAAA_AAA4 -> AAAA_AAAA

@(posedge tb_uicac_clk);
tb_uicac_cpu_addr         <= 32'h8001_F98C;
tb_uicac_cpu_data         <= 32'hAAAA_AAAA;
tb_uicac_cpu_read         <= 3'b000;
tb_uicac_cpu_write        <= 3'b100;

@(posedge tb_uicac_clk);
tb_uicac_mem_ack          <= 1'b1;  //asserted to imitate writing memory into flash
       memory

repeat(8)@(posedge tb_uicac_clk);
tb_uicac_mem_ack          <= 1'b0;  //deasserted to imitate end of writing memory into
       flash memory
```

```
repeat(10)@(posedge tb_uicac_clk);

for (tb_i=0; tb_i<8; tb_i=tb_i+1) begin
@(posedge tb_uicac_clk);
tb_uicac_mem_ack          <= 1'b1;
tb_uicac_mem_data_rd      <= 32'hAAAA_AAA1 + tb_i;
end

repeat(3)@(posedge tb_uicac_clk);
tb_uicac_cpu_addr         <= 32'h0000_0000;
tb_uicac_cpu_data         <= 32'h0000_0000;
tb_uicac_mem_ack          <= 1'b0;
tb_uicac_cpu_write        <= 3'b000;


repeat(2)@(posedge tb_uicac_clk);
tb_testStatus                   <= "Test Conpleted Successfully!";
repeat(2)@(posedge tb_uicac_clk);
$stop;
end
endmodule
```

Appendices B: Timing Delay Details of 32-bit 7-Stage Pipeline Processor

```
---> IF Delay <-------------------------------------------------------------------------
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~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~IFIS~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
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  ---------------------------------------------------------------------    -------------
------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  ---------------------------------------------------------------------    -------------
------
    SLICE_X47Y71         FDRE (Prop_fdre_C_Q)         0.456     9.160 f
u_datapath/uodp_if_pseudo_pc_reg[2]/Q
                         net (fo=7, routed)           1.491    10.652
u_datapath/uodp_if_pseudo_pc[2]
    SLICE_X51Y73                                                    f
u_datapath/bp_i_52/I0
    SLICE_X51Y73         LUT1 (Prop_lut1_I0_O)        0.124    10.776 r
u_datapath/bp_i_52/O
                         net (fo=1, routed)           0.000    10.776
u_datapath/bp_i_52_n_2
    SLICE_X51Y73                                                    r
u_datapath/bp_i_40/S[1]
    SLICE_X51Y73         CARRY4 (Prop_carry4_S[1]_CO[3])
                                                      0.550    11.326 r
u_datapath/bp_i_40/CO[3]
                         net (fo=1, routed)           0.000    11.326
u_datapath/bp_i_40_n_2
    SLICE_X51Y74                                                    r
u_datapath/bp_i_39/CI
    SLICE_X51Y74         CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.114    11.440 r
u_datapath/bp_i_39/CO[3]
                         net (fo=1, routed)           0.009    11.449
u_datapath/bp_i_39_n_2
    SLICE_X51Y75                                                    r
u_datapath/bp_i_38/CI
    SLICE_X51Y75         CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.114    11.563 r
u_datapath/bp_i_38/CO[3]
                         net (fo=1, routed)           0.000    11.563
u_datapath/bp_i_38_n_2
    SLICE_X51Y76                                                    r
u_datapath/bp_i_37/CI
    SLICE_X51Y76         CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.114    11.677 r
u_datapath/bp_i_37/CO[3]
                         net (fo=1, routed)           0.000    11.677
u_datapath/bp_i_37_n_2
    SLICE_X51Y77                                                    r
u_datapath/bp_i_36/CI
    SLICE_X51Y77         CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.114    11.791 r
u_datapath/bp_i_36/CO[3]
                         net (fo=1, routed)           0.000    11.791
u_datapath/bp_i_36_n_2
    SLICE_X51Y78                                                    r
u_datapath/bp_i_35/CI
    SLICE_X51Y78         CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.114    11.905 r
u_datapath/bp_i_35/CO[3]
                         net (fo=1, routed)           0.000    11.905
u_datapath/bp_i_35_n_2
    SLICE_X51Y79                                                    r
u_datapath/bp_i_34/CI
    SLICE_X51Y79         CARRY4 (Prop_carry4_CI_O[3])
                                                      0.329    12.234 r
u_datapath/bp_i_34/O[3]
```

```
                         net (fo=2, routed)          1.300    13.534
u_datapath/bp/bibp_if_pc4[28]
    SLICE_X51Y81                                                     r
u_datapath/bp/bobp_if_next_pc[28]_INST_0_i_2/I1
    SLICE_X51Y81         LUT6 (Prop_lut6_I1_O)       0.306    13.840 r
u_datapath/bp/bobp_if_next_pc[28]_INST_0_i_2/O
                         net (fo=1, routed)          0.810    14.650
u_datapath/bp/bobp_if_next_pc[28]_INST_0_i_2_n_2
    SLICE_X52Y81                                                     r
u_datapath/bp/bobp_if_next_pc[28]_INST_0/I2
    SLICE_X52Y81         LUT5 (Prop_lut5_I2_O)       0.124    14.774 r
u_datapath/bp/bobp_if_next_pc[28]_INST_0/O
                         net (fo=1, routed)          0.721    15.495
u_datapath/ubp_next_pc[28]
    SLICE_X53Y79                                                     r
u_datapath/uodp_if_pseudo_pc[28]_i_1/I1
    SLICE_X53Y79         LUT6 (Prop_lut6_I1_O)       0.124    15.619 r
u_datapath/uodp_if_pseudo_pc[28]_i_1/O
                         net (fo=1, routed)          0.000    15.619
u_datapath/p_1_in[28]
    SLICE_X53Y79         FDSE                                        r
u_datapath/uodp_if_pseudo_pc_reg[28]/D
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from u_datapath/uodp_if_pseudo_pc_reg to
u_datapath/uodp_if_pseudo_pc_reg:
  Data Path Delay:        6.914ns  (logic 2.583ns (37.358%)  route 4.331ns (62.642%))
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~IFIS~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~

---> IS Delay <-------------------------------------------------------------------
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~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~ISID(icache)~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~

  -------------------------------------------------------------------    -------------
------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X51Y68         FDRE (Prop_fdre_C_Q)        0.456     9.161 r
icache/ucac_is_reg_block_offset_reg[0]/Q
                         net (fo=2, routed)          0.812     9.974
icache/ucac_is_reg_block_offset[0]
    SLICE_X51Y66                                                     r
icache/cache_cell_i_40/I2
    SLICE_X51Y66         LUT6 (Prop_lut6_I2_O)       0.124    10.098 r
icache/cache_cell_i_40/O
                         net (fo=128, routed)        3.330    13.428
icache/cache_cell/bcr_array_reg_0_255_0_0/A0
    SLICE_X42Y59                                                     r
icache/cache_cell/bcr_array_reg_0_255_0_0/RAMS64E_D/ADR0
    SLICE_X42Y59         RAMS64E (Prop_rams64e_ADR0_O)
                                                     0.124    13.552 r
icache/cache_cell/bcr_array_reg_0_255_0_0/RAMS64E_D/O
                         net (fo=1, routed)          0.000    13.552
icache/cache_cell/bcr_array_reg_0_255_0_0/OD
    SLICE_X42Y59                                                     r
icache/cache_cell/bcr_array_reg_0_255_0_0/F7.B/I0
    SLICE_X42Y59         MUXF7 (Prop_muxf7_I0_O)     0.241    13.793 r
icache/cache_cell/bcr_array_reg_0_255_0_0/F7.B/O
                         net (fo=1, routed)          0.000    13.793
icache/cache_cell/bcr_array_reg_0_255_0_0/O0
    SLICE_X42Y59                                                     r
icache/cache_cell/bcr_array_reg_0_255_0_0/F8/I0
    SLICE_X42Y59         MUXF8 (Prop_muxf8_I0_O)     0.098    13.891 r
icache/cache_cell/bcr_array_reg_0_255_0_0/F8/O
                         net (fo=2, routed)          1.152    15.043
icache/cache_cell/bcr_dout0[0]
```

```
    SLICE_X45Y62                                                      r
icache/cache_cell/bocr_dout[24]_INST_0_i_1/I2
    SLICE_X45Y62         LUT3 (Prop_lut3_I2_O)        0.319    15.362 r
icache/cache_cell/bocr_dout[24]_INST_0_i_1/O
                         net (fo=1, routed)           0.347    15.709
icache/cache_cell/bocr_dout[24]_INST_0_i_1_n_2
    SLICE_X44Y62                                                      r
icache/cache_cell/bocr_dout[24]_INST_0/I0
    SLICE_X44Y62         LUT1 (Prop_lut1_I0_O)        0.124    15.833 r
icache/cache_cell/bocr_dout[24]_INST_0/O
                         net (fo=1, routed)           0.501    16.333
icache/cache_cell_n_10
    SLICE_X45Y62                                                      r
icache/ucac_id_mem_data[24]_i_1/I0
    SLICE_X45Y62         LUT2 (Prop_lut2_I0_O)        0.124    16.457 r
icache/ucac_id_mem_data[24]_i_1/O
                         net (fo=1, routed)           0.000    16.457
icache/ucac_is_mem_data[24]
    SLICE_X45Y62         FDRE                                        r
icache/ucac_id_mem_data_reg[24]/D
  ----------------------------------------------------------------    -------------
------
  Below shown the delay from icache/ucac_is_reg_block_offset_reg to
icache/ucac_id_mem_data_reg:
  Data Path Delay:        7.752ns  (logic 1.610ns (20.769%)  route 6.142ns (79.231%))

  ----------------------------------------------------------------    -------------
------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  ----------------------------------------------------------------    -------------
------
    SLICE_X51Y69         FDRE (Prop_fdre_C_Q)         0.456     9.160 r
icache/ucac_is_reg_index_reg[0]/Q
                         net (fo=33, routed)          0.581     9.742
icache/ucac_is_reg_index[0]
    SLICE_X54Y69                                                      r
icache/cache_cell_i_37/I0
    SLICE_X54Y69         LUT4 (Prop_lut4_I0_O)        0.124     9.866 r
icache/cache_cell_i_37/O
                         net (fo=151, routed)         2.919    12.785
icache/cache_cell/bcr_array_reg_0_255_23_23/A3
    SLICE_X60Y61                                                      r
icache/cache_cell/bcr_array_reg_0_255_23_23/RAMS64E_D/ADR3
    SLICE_X60Y61         RAMS64E (Prop_rams64e_ADR3_O)
                                                      0.124    12.909 r
icache/cache_cell/bcr_array_reg_0_255_23_23/RAMS64E_D/O
                         net (fo=1, routed)           0.000    12.909
icache/cache_cell/bcr_array_reg_0_255_23_23/OD
    SLICE_X60Y61                                                      r
icache/cache_cell/bcr_array_reg_0_255_23_23/F7.B/I0
    SLICE_X60Y61         MUXF7 (Prop_muxf7_I0_O)      0.241    13.150 r
icache/cache_cell/bcr_array_reg_0_255_23_23/F7.B/O
                         net (fo=1, routed)           0.000    13.150
icache/cache_cell/bcr_array_reg_0_255_23_23/O0
    SLICE_X60Y61                                                      r
icache/cache_cell/bcr_array_reg_0_255_23_23/F8/I0
    SLICE_X60Y61         MUXF8 (Prop_muxf8_I0_O)      0.098    13.248 r
icache/cache_cell/bcr_array_reg_0_255_23_23/F8/O
                         net (fo=2, routed)           0.972    14.220
icache/cache_cell/bcr_dout0[23]
    SLICE_X57Y62                                                      r
icache/cache_cell/bocr_dout[15]_INST_0_i_1/I2
    SLICE_X57Y62         LUT3 (Prop_lut3_I2_O)        0.347    14.567 r
icache/cache_cell/bocr_dout[15]_INST_0_i_1/O
                         net (fo=1, routed)           0.652    15.219
icache/cache_cell/bocr_dout[15]_INST_0_i_1_n_2
    SLICE_X57Y62                                                      r
icache/cache_cell/bocr_dout[15]_INST_0/I0
    SLICE_X57Y62         LUT1 (Prop_lut1_I0_O)        0.354    15.573 r
icache/cache_cell/bocr_dout[15]_INST_0/O
                         net (fo=1, routed)           0.267    15.839
icache/cache_cell_n_19
```

```
    SLICE_X57Y62                                                        r
icache/ucac_id_mem_data[15]_i_1/I0
    SLICE_X57Y62         LUT2 (Prop_lut2_I0_O)        0.332    16.171 r
icache/ucac_id_mem_data[15]_i_1/O
                         net (fo=1, routed)           0.000    16.171
icache/ucac_is_mem_data[15]
    SLICE_X57Y62         FDRE                                           r
icache/ucac_id_mem_data_reg[15]/D
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from icache/ucac_is_reg_index_reg to
icache/ucac_id_mem_data_reg:
  Data Path Delay:        7.467ns  (logic 2.076ns (27.803%)  route 5.391ns (72.197%))
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~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~ISID(icache)~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
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~~~~~~~~~~~~~~~~~~~~~~~~~~ISID(branch predictor)~~~~~~~~~~~~~~~~~~~~~~~~~~
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------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X49Y75         FDRE (Prop_fdre_C_Q)         0.456     9.154 r
u_datapath/bp/bbp_is_pc_index_reg[1]/Q
                         net (fo=321, routed)         2.548    11.702
u_datapath/bp/bbp_tag_ram_1_reg_0_15_6_11/ADDRB1
    SLICE_X38Y85                                                        r
u_datapath/bp/bbp_tag_ram_1_reg_0_15_6_11/RAMB/RADR1
    SLICE_X38Y85         RAMD32 (Prop_ramd32_RADR1_O)
                                                      0.152    11.854 r
u_datapath/bp/bbp_tag_ram_1_reg_0_15_6_11/RAMB/O
                         net (fo=1, routed)           0.994    12.848
u_datapath/bp/bbp_is_hit_way[1]1[8]
    SLICE_X43Y85                                                        r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_28/I1
    SLICE_X43Y85         LUT6 (Prop_lut6_I1_O)        0.348    13.196 r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_28/O
                         net (fo=1, routed)           0.000    13.196
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_28_n_2
    SLICE_X43Y85                                                        r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_22/S[2]
    SLICE_X43Y85         CARRY4 (Prop_carry4_S[2]_CO[3])
                                                      0.398    13.594 r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_22/CO[3]
                         net (fo=1, routed)           0.000    13.594
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_22_n_2
    SLICE_X43Y86                                                        r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_20/CI
    SLICE_X43Y86         CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.114    13.708 r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_20/CO[3]
                         net (fo=1, routed)           0.000    13.708
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_20_n_2
    SLICE_X43Y87                                                        r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_14/CI
    SLICE_X43Y87         CARRY4 (Prop_carry4_CI_CO[0])
                                                      0.271    13.979 f
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_14/CO[0]
                         net (fo=1, routed)           0.551    14.530
u_datapath/bp/bbp_is_hit_way[1]0
    SLICE_X43Y90                                                        f
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_6/I1
    SLICE_X43Y90         LUT2 (Prop_lut2_I1_O)        0.373    14.903 r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_6/O
                         net (fo=37, routed)          0.610    15.513
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_6_n_2
    SLICE_X43Y89                                                        r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_7/I3
    SLICE_X43Y89         LUT6 (Prop_lut6_I3_O)        0.124    15.637 r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_7/O
```

```
                         net (fo=34, routed)          1.913    17.550
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_7_n_2
    SLICE_X48Y76                                                        r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_2/I3
    SLICE_X48Y76         LUT5 (Prop_lut5_I3_O)        0.118    17.668 f
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_2/O
                         net (fo=32, routed)          1.125    18.794
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_2_n_2
    SLICE_X48Y75                                                        f
u_datapath/bp/bobp_if_next_pc[15]_INST_0/I1
    SLICE_X48Y75         LUT5 (Prop_lut5_I1_O)        0.326    19.120 r
u_datapath/bp/bobp_if_next_pc[15]_INST_0/O
                         net (fo=1, routed)           0.578    19.698
u_datapath/ubp_next_pc[15]
    SLICE_X54Y75                                                        r
u_datapath/uodp_if_pseudo_pc[15]_i_2/I1
    SLICE_X54Y75         LUT5 (Prop_lut5_I1_O)        0.124    19.822 r
u_datapath/uodp_if_pseudo_pc[15]_i_2/O
                         net (fo=1, routed)           0.670    20.492
u_datapath/uodp_if_pseudo_pc[15]_i_2_n_2
    SLICE_X54Y75                                                        r
u_datapath/uodp_if_pseudo_pc[15]_i_1/I2
    SLICE_X54Y75         LUT4 (Prop_lut4_I2_O)        0.124    20.616 r
u_datapath/uodp_if_pseudo_pc[15]_i_1/O
                         net (fo=1, routed)           0.000    20.616
u_datapath/p_1_in[15]
    SLICE_X54Y75         FDRE                                           r
u_datapath/uodp_if_pseudo_pc_reg[15]/D
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from u_datapath/bp/bbp_is_pc_index_reg to
u_datapath/uodp_if_pseudo_pc_reg:
  Data Path Delay:        11.918ns  (logic 2.928ns (24.569%)  route 8.990ns (75.431%))
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~~~~~~~~~~~~~~~~~~~~~~~~~~ISID(branch predictor)~~~~~~~~~~~~~~~~~~~~~~~~~~
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---> ID Delay <--------------------------------------------------------------------
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~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~IDEX(icache)~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
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  -------------------------------------------------------------------    -------------
------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X64Y62         FDRE (Prop_fdre_C_Q)         0.456     9.169 r
icache/ucac_id_valid_reg/Q
                         net (fo=36, routed)          1.551    10.720
icache/ucac_id_valid
    SLICE_X48Y67                                                        r
icache/uocac_cpu_data[26]_INST_0/I3
    SLICE_X48Y67         LUT5 (Prop_lut5_I3_O)        0.124    10.844 r
icache/uocac_cpu_data[26]_INST_0/O
                         net (fo=1, routed)           0.669    11.513
urisc_cache_instr[26]
    SLICE_X48Y67                                                        r
u_ctrlpath_i_6/I4
    SLICE_X48Y67         LUT5 (Prop_lut5_I4_O)        0.124    11.637 r
u_ctrlpath_i_6/O
                         net (fo=38, routed)          1.370    13.007
u_ctrlpath/b_mc/bimc_opcode[0]
    SLICE_X32Y68                                                        r
u_ctrlpath/b_mc/bomc_undef_inst_INST_0_i_1/I0
    SLICE_X32Y68         LUT6 (Prop_lut6_I0_O)        0.124    13.131 f
u_ctrlpath/b_mc/bomc_undef_inst_INST_0_i_1/O
                         net (fo=1, routed)           0.695    13.826
u_ctrlpath/b_mc/bomc_undef_inst_INST_0_i_1_n_2
    SLICE_X32Y68                                                        f
u_ctrlpath/b_mc/bomc_undef_inst_INST_0/I0
```

```
    SLICE_X32Y68         LUT6 (Prop_lut6_I0_O)        0.124    13.950 r
u_ctrlpath/b_mc/bomc_undef_inst_INST_0/O
                         net (fo=9, routed)           0.992    14.942
u_datapath/b_cp0/bicp0_undef_instr
    SLICE_X44Y70                                                  r
u_datapath/b_cp0/bocp0_exc_flag_INST_0/I1
    SLICE_X44Y70         LUT4 (Prop_lut4_I1_O)        0.152    15.094 r
u_datapath/b_cp0/bocp0_exc_flag_INST_0/O
                         net (fo=95, routed)          1.108    16.201
urisc_cp0_exc_flag
    SLICE_X56Y74                                                  r
u_datapath_i_59/I2
    SLICE_X56Y74         LUT3 (Prop_lut3_I2_O)        0.332    16.533 f
u_datapath_i_59/O
                         net (fo=30, routed)          2.458    18.992
SPI_controller/uispi_pipe_stall
    SLICE_X12Y87                                                  f
SPI_controller/TX_BUFFER16X8_i_2/I0
    SLICE_X12Y87         LUT3 (Prop_lut3_I0_O)        0.124    19.116 r
SPI_controller/TX_BUFFER16X8_i_2/O
                         net (fo=4, routed)           0.427    19.543
SPI_controller/uspi_wr_SPISR1
    SLICE_X12Y88                                                  r
SPI_controller/TX_BUFFER16X8_i_1/I4
    SLICE_X12Y88         LUT5 (Prop_lut5_I4_O)        0.124    19.667 r
SPI_controller/TX_BUFFER16X8_i_1/O
                         net (fo=11, routed)          0.796    20.463
SPI_controller/TX_BUFFER16X8/biFIFO_push
    SLICE_X12Y95                                                  r
SPI_controller/TX_BUFFER16X8/bFIFO_count[4]_i_1/I2
    SLICE_X12Y95         LUT3 (Prop_lut3_I2_O)        0.117    20.580 r
SPI_controller/TX_BUFFER16X8/bFIFO_count[4]_i_1/O
                         net (fo=5, routed)           0.502    21.082
SPI_controller/TX_BUFFER16X8/bFIFO_count[4]_i_1_n_2
    SLICE_X11Y95         FDRE                                     r
SPI_controller/TX_BUFFER16X8/bFIFO_count_reg[1]/CE
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from icache/ucac_id_valid_reg/Q to
SPI_controller/TX_BUFFER16X8/bFIFO_count_reg:
  Data Path Delay:        12.368ns  (logic 1.801ns (14.562%)  route 10.567ns
(85.438%))

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------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X64Y62         FDRE (Prop_fdre_C_Q)         0.456     9.169 r
icache/ucac_id_valid_reg/Q
                         net (fo=36, routed)          1.551    10.720
icache/ucac_id_valid
    SLICE_X48Y67                                                  r
icache/uocac_cpu_data[26]_INST_0/I3
    SLICE_X48Y67         LUT5 (Prop_lut5_I3_O)        0.124    10.844 r
icache/uocac_cpu_data[26]_INST_0/O
                         net (fo=1, routed)           0.669    11.513
urisc_cache_instr[26]
    SLICE_X48Y67                                                  r
u_ctrlpath_i_6/I4
    SLICE_X48Y67         LUT5 (Prop_lut5_I4_O)        0.124    11.637 r
u_ctrlpath_i_6/O
                         net (fo=38, routed)          1.370    13.007
u_ctrlpath/b_mc/bimc_opcode[0]
    SLICE_X32Y68                                                  r
u_ctrlpath/b_mc/bomc_undef_inst_INST_0_i_1/I0
    SLICE_X32Y68         LUT6 (Prop_lut6_I0_O)        0.124    13.131 f
u_ctrlpath/b_mc/bomc_undef_inst_INST_0_i_1/O
                         net (fo=1, routed)           0.695    13.826
u_ctrlpath/b_mc/bomc_undef_inst_INST_0_i_1_n_2
    SLICE_X32Y68                                                  f
u_ctrlpath/b_mc/bomc_undef_inst_INST_0/I0
```

```
    SLICE_X32Y68         LUT6 (Prop_lut6_I0_O)        0.124    13.950 r
u_ctrlpath/b_mc/bomc_undef_inst_INST_0/O
                         net (fo=9, routed)           0.992    14.942
u_datapath/b_cp0/bicp0_undef_instr
    SLICE_X44Y70                                                  r
u_datapath/b_cp0/bocp0_exc_flag_INST_0/I1
    SLICE_X44Y70         LUT4 (Prop_lut4_I1_O)        0.152    15.094 r
u_datapath/b_cp0/bocp0_exc_flag_INST_0/O
                         net (fo=95, routed)          1.108    16.201
urisc_cp0_exc_flag
    SLICE_X56Y74                                                  r
u_datapath_i_59/I2
    SLICE_X56Y74         LUT3 (Prop_lut3_I2_O)        0.332    16.533 f
u_datapath_i_59/O
                         net (fo=30, routed)          2.458    18.992
SPI_controller/uispi_pipe_stall
    SLICE_X12Y87                                                  f
SPI_controller/TX_BUFFER16X8_i_2/I0
    SLICE_X12Y87         LUT3 (Prop_lut3_I0_O)        0.124    19.116 r
SPI_controller/TX_BUFFER16X8_i_2/O
                         net (fo=4, routed)           0.427    19.543
SPI_controller/uspi_wr_SPISR1
    SLICE_X12Y88                                                  r
SPI_controller/TX_BUFFER16X8_i_1/I4
    SLICE_X12Y88         LUT5 (Prop_lut5_I4_O)        0.124    19.667 r
SPI_controller/TX_BUFFER16X8_i_1/O
                         net (fo=11, routed)          0.796    20.463
SPI_controller/TX_BUFFER16X8/biFIFO_push
    SLICE_X12Y95                                                  r
SPI_controller/TX_BUFFER16X8/bFIFO_FIFOreg_reg_0_15_6_7_i_1/I0
    SLICE_X12Y95         LUT2 (Prop_lut2_I0_O)        0.124    20.587 r
SPI_controller/TX_BUFFER16X8/bFIFO_FIFOreg_reg_0_15_6_7_i_1/O
                         net (fo=16, routed)          0.345    20.932
SPI_controller/TX_BUFFER16X8/bFIFO_FIFOreg_reg_0_15_0_5/WE
    SLICE_X12Y97         RAMD32                                   r
SPI_controller/TX_BUFFER16X8/bFIFO_FIFOreg_reg_0_15_0_5/RAMA/WE
  ----------------------------------------------------------------    -------------
------
  Below shown the delay from icache/ucac_id_valid_reg/Q to
SPI_controller/TX_BUFFER16X8/bFIFO_FIFOreg_reg_0_15_0_5/RAMA/WE:
  Data Path Delay:        12.218ns  (logic 1.808ns (14.797%)  route 10.410ns
(85.203%))
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~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~IDEX(icache)~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
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~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~IDEX(branch predictor)~~~~~~~~~~~~~~~~~~~~~~~~~~
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------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  ----------------------------------------------------------------    -------------
------
    SLICE_X47Y87         FDRE (Prop_fdre_C_Q)         0.419     9.133 f
u_datapath/bp/bbp_id_pred_reg[1]/Q
                         net (fo=6, routed)           1.324    10.457
u_datapath/bp/p_0_in213_in
    SLICE_X40Y83                                                  f
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_10/I0
    SLICE_X40Y83         LUT6 (Prop_lut6_I0_O)        0.299    10.756 r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_10/O
                         net (fo=33, routed)          0.603    11.360
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_10_n_2
    SLICE_X43Y83                                                  r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4/I3
    SLICE_X43Y83         LUT5 (Prop_lut5_I3_O)        0.124    11.484 f
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4/O
                         net (fo=34, routed)          1.232    12.715
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4_n_2
    SLICE_X54Y77                                                  f
u_datapath/bp/bobp_id_nop_ifid_INST_0/I1
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```
    SLICE_X54Y77         LUT2 (Prop_lut2_I1_O)        0.124    12.839 r
u_datapath/bp/bobp_id_nop_ifid_INST_0/O
                         net (fo=4, routed)           0.774    13.614
icache/uicac_bp_flush
    SLICE_X54Y76                                                 r
icache/ucac_id_reg_index[4]_i_1/I0
    SLICE_X54Y76         LUT3 (Prop_lut3_I0_O)        0.124    13.738 r
icache/ucac_id_reg_index[4]_i_1/O
                         net (fo=68, routed)          1.535    15.272
icache/ucac_id_tag0
    SLICE_X64Y62         FDRE                                    r
icache/ucac_id_valid_reg/R
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from u_datapath/bp/bbp_id_pred_reg to
icache/ucac_id_valid_reg/R:
  Data Path Delay:        6.558ns  (logic 1.090ns (16.622%)  route 5.468ns (83.378%))

  -------------------------------------------------------------------    -------------
------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X47Y87         FDRE (Prop_fdre_C_Q)         0.419     9.133 f
u_datapath/bp/bbp_id_pred_reg[1]/Q
                         net (fo=6, routed)           1.324    10.457
u_datapath/bp/p_0_in213_in
    SLICE_X40Y83                                                 f
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_10/I0
    SLICE_X40Y83         LUT6 (Prop_lut6_I0_O)        0.299    10.756 r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_10/O
                         net (fo=33, routed)          0.603    11.360
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_10_n_2
    SLICE_X43Y83                                                 r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4/I3
    SLICE_X43Y83         LUT5 (Prop_lut5_I3_O)        0.124    11.484 f
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4/O
                         net (fo=34, routed)          1.232    12.715
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4_n_2
    SLICE_X54Y77                                                 f
u_datapath/bp/bobp_id_nop_ifid_INST_0/I1
    SLICE_X54Y77         LUT2 (Prop_lut2_I1_O)        0.124    12.839 r
u_datapath/bp/bobp_id_nop_ifid_INST_0/O
                         net (fo=4, routed)           0.774    13.614
icache/uicac_bp_flush
    SLICE_X54Y76                                                 r
icache/ucac_id_reg_index[4]_i_1/I0
    SLICE_X54Y76         LUT3 (Prop_lut3_I0_O)        0.124    13.738 r
icache/ucac_id_reg_index[4]_i_1/O
                         net (fo=68, routed)          1.503    15.241
icache/ucac_id_tag0
    SLICE_X63Y62         FDRE                                    r
icache/ucac_id_dirty_reg/R
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from u_datapath/bp/bbp_id_pred_reg to
icache/ucac_id_dirty_reg/R:
  Data Path Delay:        6.527ns  (logic 1.090ns (16.701%)  route 5.437ns (83.299%))

  -------------------------------------------------------------------    -------------
------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X47Y87         FDRE (Prop_fdre_C_Q)         0.419     9.133 f
u_datapath/bp/bbp_id_pred_reg[1]/Q
                         net (fo=6, routed)           1.324    10.457
u_datapath/bp/p_0_in213_in
    SLICE_X40Y83                                                 f
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_10/I0
    SLICE_X40Y83         LUT6 (Prop_lut6_I0_O)        0.299    10.756 r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_10/O
```

```
                         net (fo=33, routed)         0.603    11.360
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_10_n_2
    SLICE_X43Y83                                                    r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4/I3
    SLICE_X43Y83         LUT5 (Prop_lut5_I3_O)       0.124    11.484 f
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4/O
                         net (fo=34, routed)         1.232    12.715
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4_n_2
    SLICE_X54Y77                                                    f
u_datapath/bp/bobp_id_nop_ifid_INST_0/I1
    SLICE_X54Y77         LUT2 (Prop_lut2_I1_O)       0.124    12.839 r
u_datapath/bp/bobp_id_nop_ifid_INST_0/O
                         net (fo=4, routed)          0.774    13.614
icache/uicac_bp_flush
    SLICE_X54Y76                                                    r
icache/ucac_id_reg_index[4]_i_1/I0
    SLICE_X54Y76         LUT3 (Prop_lut3_I0_O)       0.124    13.738 r
icache/ucac_id_reg_index[4]_i_1/O
                         net (fo=68, routed)         1.310    15.048
icache/ucac_id_tag0
    SLICE_X55Y63         FDRE                                       r
icache/ucac_id_mem_data_reg[6]/R
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from u_datapath/bp/bbp_id_pred_reg to
icache/ucac_id_mem_data_reg:
  Data Path Delay:        6.333ns  (logic 1.090ns (17.211%)  route 5.243ns (82.789%))

  -------------------------------------------------------------------    -------------
------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X47Y87         FDRE (Prop_fdre_C_Q)        0.419     9.133 f
u_datapath/bp/bbp_id_pred_reg[1]/Q
                         net (fo=6, routed)          1.324    10.457
u_datapath/bp/p_0_in213_in
    SLICE_X40Y83                                                    f
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_10/I0
    SLICE_X40Y83         LUT6 (Prop_lut6_I0_O)       0.299    10.756 r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_10/O
                         net (fo=33, routed)         0.603    11.360
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_10_n_2
    SLICE_X43Y83                                                    r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4/I3
    SLICE_X43Y83         LUT5 (Prop_lut5_I3_O)       0.124    11.484 f
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4/O
                         net (fo=34, routed)         1.232    12.715
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4_n_2
    SLICE_X54Y77                                                    f
u_datapath/bp/bobp_id_nop_ifid_INST_0/I1
    SLICE_X54Y77         LUT2 (Prop_lut2_I1_O)       0.124    12.839 r
u_datapath/bp/bobp_id_nop_ifid_INST_0/O
                         net (fo=4, routed)          0.774    13.614
u_datapath/uodp_bp_flush_id
    SLICE_X54Y76                                                    r
u_datapath/udp_cp0_id_pc[31]_i_1/I2
    SLICE_X54Y76         LUT3 (Prop_lut3_I2_O)       0.150    13.764 r
u_datapath/udp_cp0_id_pc[31]_i_1/O
                         net (fo=63, routed)         1.145    14.909
u_datapath/udp_cp0_id_pc0
    SLICE_X45Y73         FDRE                                       r
u_datapath/udp_id_pc4_reg[2]/R
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from u_datapath/bp/bbp_id_pred_reg to
u_datapath/udp_id_pc4_reg:
  Data Path Delay:        6.195ns  (logic 1.116ns (18.016%)  route 5.079ns (81.984%))
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~~~~~~~~~~~~~~~~~~~~~~~~~~IDEX(branch predictor)~~~~~~~~~~~~~~~~~~~~~~~~~~
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~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~IDEX~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
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  -------------------------------------------------------------------    -------------
------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X48Y71         FDRE (Prop_fdre_C_Q)         0.419     9.123 r
u_datapath/udp_id_pc4_reg[1]/Q
                         net (fo=3, routed)           1.107    10.230
u_datapath/udp_id_pc4[1]
    SLICE_X45Y72                                                      r
u_datapath/bp_i_48/S[0]
    SLICE_X45Y72         CARRY4 (Prop_carry4_S[0]_CO[3])
                                                      0.831    11.061 r
u_datapath/bp_i_48/CO[3]
                         net (fo=1, routed)           0.000    11.061
u_datapath/bp_i_48_n_2
    SLICE_X45Y73                                                      r
u_datapath/bp_i_47/CI
    SLICE_X45Y73         CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.114    11.175 r
u_datapath/bp_i_47/CO[3]
                         net (fo=1, routed)           0.000    11.175
u_datapath/bp_i_47_n_2
    SLICE_X45Y74                                                      r
u_datapath/bp_i_46/CI
    SLICE_X45Y74         CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.114    11.289 r
u_datapath/bp_i_46/CO[3]
                         net (fo=1, routed)           0.009    11.298
u_datapath/bp_i_46_n_2
    SLICE_X45Y75                                                      r
u_datapath/bp_i_45/CI
    SLICE_X45Y75         CARRY4 (Prop_carry4_CI_O[3])
                                                      0.313    11.611 r
u_datapath/bp_i_45/O[3]
                         net (fo=2, routed)           0.650    12.261
u_datapath/bp/bibp_id_br_taddr[16]
    SLICE_X46Y76                                                      r
u_datapath/bp/bobp_if_next_pc[16]_INST_0_i_3/I4
    SLICE_X46Y76         LUT6 (Prop_lut6_I4_O)        0.306    12.567 r
u_datapath/bp/bobp_if_next_pc[16]_INST_0_i_3/O
                         net (fo=1, routed)           0.565    13.132
u_datapath/bp/bobp_if_next_pc[16]_INST_0_i_3_n_2
    SLICE_X48Y76                                                      r
u_datapath/bp/bobp_if_next_pc[16]_INST_0/I4
    SLICE_X48Y76         LUT5 (Prop_lut5_I4_O)        0.124    13.256 r
u_datapath/bp/bobp_if_next_pc[16]_INST_0/O
                         net (fo=1, routed)           0.843    14.099
u_datapath/ubp_next_pc[16]
    SLICE_X54Y78                                                      r
u_datapath/uodp_if_pseudo_pc[16]_i_3/I1
    SLICE_X54Y78         LUT5 (Prop_lut5_I1_O)        0.124    14.223 r
u_datapath/uodp_if_pseudo_pc[16]_i_3/O
                         net (fo=1, routed)           0.483    14.706
u_datapath/uodp_if_pseudo_pc[16]_i_3_n_2
    SLICE_X54Y78                                                      r
u_datapath/uodp_if_pseudo_pc[16]_i_1/I2
    SLICE_X54Y78         LUT4 (Prop_lut4_I2_O)        0.116    14.822 r
u_datapath/uodp_if_pseudo_pc[16]_i_1/O
                         net (fo=1, routed)           0.000    14.822
u_datapath/p_1_in[16]
    SLICE_X54Y78         FDRE                                         r
u_datapath/uodp_if_pseudo_pc_reg[16]/D
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from u_datapath/udp_id_pc4_reg to
u_datapath/uodp_if_pseudo_pc_reg:
  Data Path Delay:        6.118ns  (logic 2.461ns (40.226%)  route 3.657ns (59.774%))
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~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~IDEX~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
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---> EX Delay <-------------------------------------------------------------------------------
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~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~EXDF~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
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  ------------------------------------------------------------------    -------------
------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  ------------------------------------------------------------------    -------------
------
    SLICE_X32Y69         FDRE (Prop_fdre_C_Q)         0.456     9.169 r
u_datapath/udp_ex_alb_src_reg/Q
                         net (fo=32, routed)          1.712    10.881
u_datapath/udp_ex_alb_src
    SLICE_X15Y82                                                      r
u_datapath/b_alb_i_8/I1
    SLICE_X15Y82         LUT3 (Prop_lut3_I1_O)        0.124    11.005 f
u_datapath/b_alb_i_8/O
                         net (fo=74, routed)          1.832    12.837
u_datapath/b_alb/bialb_op_b[24]
    SLICE_X8Y56                                                       f
u_datapath/b_alb/boalb_out[8]_INST_0_i_6/I2
    SLICE_X8Y56          LUT5 (Prop_lut5_I2_O)        0.150    12.987 f
u_datapath/b_alb/boalb_out[8]_INST_0_i_6/O
                         net (fo=4, routed)           0.884    13.871
u_datapath/b_alb/boalb_out[8]_INST_0_i_6_n_2
    SLICE_X11Y55                                                      f
u_datapath/b_alb/boalb_out[2]_INST_0_i_4/I0
    SLICE_X11Y55         LUT6 (Prop_lut6_I0_O)        0.328    14.199 f
u_datapath/b_alb/boalb_out[2]_INST_0_i_4/O
                         net (fo=2, routed)           0.580    14.778
u_datapath/b_alb/boalb_out[2]_INST_0_i_4_n_2
    SLICE_X13Y54                                                      f
u_datapath/b_alb/boalb_out[1]_INST_0_i_1/I3
    SLICE_X13Y54         LUT5 (Prop_lut5_I3_O)        0.124    14.902 f
u_datapath/b_alb/boalb_out[1]_INST_0_i_1/O
                         net (fo=1, routed)           0.426    15.328
u_datapath/b_alb/b_alb_shift_out[1]
    SLICE_X12Y54                                                      f
u_datapath/b_alb/boalb_out[1]_INST_0/I0
    SLICE_X12Y54         LUT5 (Prop_lut5_I0_O)        0.124    15.452 f
u_datapath/b_alb/boalb_out[1]_INST_0/O
                         net (fo=35, routed)          2.556    18.008
u_datapath/b_alb_n_32
    SLICE_X34Y87                                                      f
u_datapath/uodp_ex_dm_store[15]_INST_0_i_1/I1
    SLICE_X34Y87         LUT3 (Prop_lut3_I1_O)        0.148    18.156 f
u_datapath/uodp_ex_dm_store[15]_INST_0_i_1/O
                         net (fo=12, routed)          0.844    19.000
u_datapath/uodp_ex_dm_store[15]_INST_0_i_1_n_2
    SLICE_X34Y84                                                      f
u_datapath/uodp_ex_dm_store[1]_INST_0_i_1/I0
    SLICE_X34Y84         LUT6 (Prop_lut6_I0_O)        0.328    19.328 r
u_datapath/uodp_ex_dm_store[1]_INST_0_i_1/O
                         net (fo=1, routed)           0.424    19.752
u_datapath/uodp_ex_dm_store[1]_INST_0_i_1_n_2
    SLICE_X33Y85                                                      r
u_datapath/uodp_ex_dm_store[1]_INST_0/I5
    SLICE_X33Y85         LUT6 (Prop_lut6_I5_O)        0.124    19.876 r
u_datapath/uodp_ex_dm_store[1]_INST_0/O
                         net (fo=18, routed)          2.269    22.145
data_ram/uiram_wb_din[1]
    SLICE_X6Y61                                                       r
data_ram/uram_array_reg_0_i_26/I2
    SLICE_X6Y61          LUT3 (Prop_lut3_I2_O)        0.152    22.297 r
data_ram/uram_array_reg_0_i_26/O
                         net (fo=1, routed)           0.290    22.587
data_ram/uram_array_reg_0_i_26_n_2
    SLICE_X6Y61                                                       r
data_ram/uram_array_reg_0_i_16/I4
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    SLICE_X6Y61          LUT5 (Prop_lut5_I4_O)        0.348    22.935 r
data_ram/uram_array_reg_0_i_16/O
                         net (fo=1, routed)           0.574    23.509
data_ram/p_1_in[1]
    RAMB36_X0Y12         RAMB36E1                                     r
data_ram/uram_array_reg_0/DIADI[1]
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from u_datapath/udp_ex_alb_src_reg/Q to
data_ram/uram_array_reg_0/DIADI:
  Data Path Delay:        14.795ns  (logic 2.406ns (16.262%)  route 12.389ns
(83.738%))

  -------------------------------------------------------------------    -------------
------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X32Y69         FDRE (Prop_fdre_C_Q)         0.456     9.169 r
u_datapath/udp_ex_alb_src_reg/Q
                         net (fo=32, routed)          1.584    10.754
u_datapath/udp_ex_alb_src
    SLICE_X15Y82                                                 r
u_datapath/b_alb_i_16/I1
    SLICE_X15Y82         LUT3 (Prop_lut3_I1_O)        0.152    10.906 r
u_datapath/b_alb_i_16/O
                         net (fo=72, routed)          1.817    12.722
u_datapath/b_alb/bialb_op_b[16]
    SLICE_X3Y57                                                  r
u_datapath/b_alb/boalb_out[23]_INST_0_i_11/I4
    SLICE_X3Y57          LUT5 (Prop_lut5_I4_O)        0.358    13.080 r
u_datapath/b_alb/boalb_out[23]_INST_0_i_11/O
                         net (fo=4, routed)           0.636    13.716
u_datapath/b_alb/boalb_out[23]_INST_0_i_11_n_2
    SLICE_X4Y58                                                  r
u_datapath/b_alb/boalb_out[19]_INST_0_i_5/I1
    SLICE_X4Y58          LUT6 (Prop_lut6_I1_O)        0.326    14.042 r
u_datapath/b_alb/boalb_out[19]_INST_0_i_5/O
                         net (fo=2, routed)           0.624    14.666
u_datapath/b_alb/boalb_out[19]_INST_0_i_5_n_2
    SLICE_X5Y60                                                  r
u_datapath/b_alb/boalb_out[18]_INST_0_i_1/I1
    SLICE_X5Y60          LUT6 (Prop_lut6_I1_O)        0.124    14.790 r
u_datapath/b_alb/boalb_out[18]_INST_0_i_1/O
                         net (fo=1, routed)           0.899    15.688
u_datapath/b_alb/boalb_out[18]_INST_0_i_1_n_2
    SLICE_X8Y59                                                  r
u_datapath/b_alb/boalb_out[18]_INST_0/I0
    SLICE_X8Y59          LUT6 (Prop_lut6_I0_O)        0.124    15.812 r
u_datapath/b_alb/boalb_out[18]_INST_0/O
                         net (fo=5, routed)           1.409    17.221
u_datapath/addr_decoder/biad_ex_cpu_addr[18]
    SLICE_X12Y73                                                 r
u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_5/I3
    SLICE_X12Y73         LUT4 (Prop_lut4_I3_O)        0.148    17.369 r
u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_5/O
                         net (fo=1, routed)           0.590    17.960
u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_5_n_2
    SLICE_X9Y72                                                  r
u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_3/I4
    SLICE_X9Y72          LUT5 (Prop_lut5_I4_O)        0.328    18.288 r
u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_3/O
                         net (fo=4, routed)           0.909    19.197
u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_3_n_2
    SLICE_X8Y77                                                  r
u_datapath/addr_decoder/boad_io_en[4]_INST_0/I4
    SLICE_X8Y77          LUT6 (Prop_lut6_I4_O)        0.124    19.321 r
u_datapath/addr_decoder/boad_io_en[4]_INST_0/O
                         net (fo=3, routed)           1.275    20.596
UART_controller/uiua_wb_w_stb
    SLICE_X8Y89                                                  r
UART_controller/btx_i_2/I0
```

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    SLICE_X8Y89          LUT4 (Prop_lut4_I0_O)        0.148    20.744 f
UART_controller/btx_i_2/O
                         net (fo=1, routed)           0.452    21.196
UART_controller/btx_i_2_n_2
    SLICE_X8Y89                                                   f
UART_controller/btx_i_1/I3
    SLICE_X8Y89          LUT4 (Prop_lut4_I3_O)        0.328    21.524 r
UART_controller/btx_i_1/O
                         net (fo=2, routed)           0.898    22.422
UART_controller/btx/asynfifo_r1_3/ip_en_w
    SLICE_X5Y94                                                   r
UART_controller/btx/asynfifo_r1_3/fifomem_b1_i_1/I0
    SLICE_X5Y94          LUT2 (Prop_lut2_I0_O)        0.119    22.541 r
UART_controller/btx/asynfifo_r1_3/fifomem_b1_i_1/O
                         net (fo=21, routed)          0.507    23.048
UART_controller/btx/asynfifo_r1_3/fifomem_b1/r_fifomem_reg_0_3_0_5/WE
    SLICE_X6Y93          RAMD32                                   r
UART_controller/btx/asynfifo_r1_3/fifomem_b1/r_fifomem_reg_0_3_0_5/RAMA/WE
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from u_datapath/udp_ex_alb_src_reg/Q to
UART_controller/btx/asynfifo_r1_3/fifomem_b1/r_fifomem_reg_0_3_0_5/RAMA/WE:
  Data Path Delay:        14.334ns  (logic 2.735ns (19.080%)  route 11.599ns
(80.920%))

  -------------------------------------------------------------------    -------------
------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X32Y69         FDRE (Prop_fdre_C_Q)         0.456     9.169 r
u_datapath/udp_ex_alb_src_reg/Q
                         net (fo=32, routed)          1.584    10.754
u_datapath/udp_ex_alb_src
    SLICE_X15Y82                                                  r
u_datapath/b_alb_i_16/I1
    SLICE_X15Y82         LUT3 (Prop_lut3_I1_O)        0.152    10.906 r
u_datapath/b_alb_i_16/O
                         net (fo=72, routed)          1.817    12.722
u_datapath/b_alb/bialb_op_b[16]
    SLICE_X3Y57                                                   r
u_datapath/b_alb/boalb_out[23]_INST_0_i_11/I4
    SLICE_X3Y57          LUT5 (Prop_lut5_I4_O)        0.358    13.080 r
u_datapath/b_alb/boalb_out[23]_INST_0_i_11/O
                         net (fo=4, routed)           0.636    13.716
u_datapath/b_alb/boalb_out[23]_INST_0_i_11_n_2
    SLICE_X4Y58                                                   r
u_datapath/b_alb/boalb_out[19]_INST_0_i_5/I1
    SLICE_X4Y58          LUT6 (Prop_lut6_I1_O)        0.326    14.042 r
u_datapath/b_alb/boalb_out[19]_INST_0_i_5/O
                         net (fo=2, routed)           0.624    14.666
u_datapath/b_alb/boalb_out[19]_INST_0_i_5_n_2
    SLICE_X5Y60                                                   r
u_datapath/b_alb/boalb_out[18]_INST_0_i_1/I1
    SLICE_X5Y60          LUT6 (Prop_lut6_I1_O)        0.124    14.790 r
u_datapath/b_alb/boalb_out[18]_INST_0_i_1/O
                         net (fo=1, routed)           0.899    15.688
u_datapath/b_alb/boalb_out[18]_INST_0_i_1_n_2
    SLICE_X8Y59                                                   r
u_datapath/b_alb/boalb_out[18]_INST_0/I0
    SLICE_X8Y59          LUT6 (Prop_lut6_I0_O)        0.124    15.812 r
u_datapath/b_alb/boalb_out[18]_INST_0/O
                         net (fo=5, routed)           1.409    17.221
u_datapath/addr_decoder/biad_ex_cpu_addr[18]
    SLICE_X12Y73                                                  r
u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_5/I3
    SLICE_X12Y73         LUT4 (Prop_lut4_I3_O)        0.148    17.369 r
u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_5/O
                         net (fo=1, routed)           0.590    17.960
u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_5_n_2
    SLICE_X9Y72                                                   r
u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_3/I4
```

```
    SLICE_X9Y72          LUT5 (Prop_lut5_I4_O)        0.328    18.288 r
u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_3/O
                         net (fo=4, routed)           0.909    19.197
u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_3_n_2
    SLICE_X8Y77                                                   r
u_datapath/addr_decoder/boad_io_en[4]_INST_0/I4
    SLICE_X8Y77          LUT6 (Prop_lut6_I4_O)        0.124    19.321 r
u_datapath/addr_decoder/boad_io_en[4]_INST_0/O
                         net (fo=3, routed)           1.275    20.596
UART_controller/uiua_wb_w_stb
    SLICE_X8Y89                                                   r
UART_controller/btx_i_2/I0
    SLICE_X8Y89          LUT4 (Prop_lut4_I0_O)        0.148    20.744 f
UART_controller/btx_i_2/O
                         net (fo=1, routed)           0.452    21.196
UART_controller/btx_i_2_n_2
    SLICE_X8Y89                                                   f
UART_controller/btx_i_1/I3
    SLICE_X8Y89          LUT4 (Prop_lut4_I3_O)        0.328    21.524 r
UART_controller/btx_i_1/O
                         net (fo=2, routed)           0.898    22.422
UART_controller/btx/asynfifo_r1_3/ip_en_w
    SLICE_X5Y94                                                   r
UART_controller/btx/asynfifo_r1_3/fifomem_b1_i_1/I0
    SLICE_X5Y94          LUT2 (Prop_lut2_I0_O)        0.119    22.541 r
UART_controller/btx/asynfifo_r1_3/fifomem_b1_i_1/O
                         net (fo=21, routed)          0.507    23.048
UART_controller/btx/asynfifo_r1_3/fifomem_b1/r_fifomem_reg_0_3_0_5/WE
    SLICE_X6Y93          RAMD32                                   r
UART_controller/btx/asynfifo_r1_3/fifomem_b1/r_fifomem_reg_0_3_0_5/RAMA_D1/WE
  ----------------------------------------------------------------    -------------
------
  Below shown the delay from u_datapath/udp_ex_alb_src_reg/Q to
UART_controller/btx/asynfifo_r1_3/fifomem_b1/r_fifomem_reg_0_3_0_5/RAMA_D1/WE:
  Data Path Delay:        14.334ns  (logic 2.735ns (19.080%)  route 11.599ns
(80.920%))

  ----------------------------------------------------------------    -------------
------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  ----------------------------------------------------------------    -------------
------
    SLICE_X32Y69         FDRE (Prop_fdre_C_Q)         0.456     9.169 r
u_datapath/udp_ex_alb_src_reg/Q
                         net (fo=32, routed)          1.584    10.754
u_datapath/udp_ex_alb_src
    SLICE_X15Y82                                                  r
u_datapath/b_alb_i_16/I1
    SLICE_X15Y82         LUT3 (Prop_lut3_I1_O)        0.152    10.906 r
u_datapath/b_alb_i_16/O
                         net (fo=72, routed)          1.817    12.722
u_datapath/b_alb/bialb_op_b[16]
    SLICE_X3Y57                                                   r
u_datapath/b_alb/boalb_out[23]_INST_0_i_11/I4
    SLICE_X3Y57          LUT5 (Prop_lut5_I4_O)        0.358    13.080 r
u_datapath/b_alb/boalb_out[23]_INST_0_i_11/O
                         net (fo=4, routed)           0.636    13.716
u_datapath/b_alb/boalb_out[23]_INST_0_i_11_n_2
    SLICE_X4Y58                                                   r
u_datapath/b_alb/boalb_out[19]_INST_0_i_5/I1
    SLICE_X4Y58          LUT6 (Prop_lut6_I1_O)        0.326    14.042 r
u_datapath/b_alb/boalb_out[19]_INST_0_i_5/O
                         net (fo=2, routed)           0.624    14.666
u_datapath/b_alb/boalb_out[19]_INST_0_i_5_n_2
    SLICE_X5Y60                                                   r
u_datapath/b_alb/boalb_out[18]_INST_0_i_1/I1
    SLICE_X5Y60          LUT6 (Prop_lut6_I1_O)        0.124    14.790 r
u_datapath/b_alb/boalb_out[18]_INST_0_i_1/O
                         net (fo=1, routed)           0.899    15.688
u_datapath/b_alb/boalb_out[18]_INST_0_i_1_n_2
    SLICE_X8Y59                                                   r
u_datapath/b_alb/boalb_out[18]_INST_0/I0
```

```
    SLICE_X8Y59          LUT6 (Prop_lut6_I0_O)        0.124    15.812 r
u_datapath/b_alb/boalb_out[18]_INST_0/O
                         net (fo=5, routed)           1.409    17.221
u_datapath/addr_decoder/biad_ex_cpu_addr[18]
    SLICE_X12Y73                                                      r
u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_5/I3
    SLICE_X12Y73         LUT4 (Prop_lut4_I3_O)        0.148    17.369 r
u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_5/O
                         net (fo=1, routed)           0.590    17.960
u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_5_n_2
    SLICE_X9Y72                                                       r
u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_3/I4
    SLICE_X9Y72          LUT5 (Prop_lut5_I4_O)        0.328    18.288 r
u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_3/O
                         net (fo=4, routed)           0.909    19.197
u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_3_n_2
    SLICE_X8Y77                                                       r
u_datapath/addr_decoder/boad_io_en[4]_INST_0/I4
    SLICE_X8Y77          LUT6 (Prop_lut6_I4_O)        0.124    19.321 r
u_datapath/addr_decoder/boad_io_en[4]_INST_0/O
                         net (fo=3, routed)           1.275    20.596
UART_controller/uiua_wb_w_stb
    SLICE_X8Y89                                                       r
UART_controller/btx_i_2/I0
    SLICE_X8Y89          LUT4 (Prop_lut4_I0_O)        0.148    20.744 f
UART_controller/btx_i_2/O
                         net (fo=1, routed)           0.452    21.196
UART_controller/btx_i_2_n_2
    SLICE_X8Y89                                                       f
UART_controller/btx_i_1/I3
    SLICE_X8Y89          LUT4 (Prop_lut4_I3_O)        0.328    21.524 r
UART_controller/btx_i_1/O
                         net (fo=2, routed)           0.898    22.422
UART_controller/btx/asynfifo_r1_3/ip_en_w
    SLICE_X5Y94                                                       r
UART_controller/btx/asynfifo_r1_3/fifomem_b1_i_1/I0
    SLICE_X5Y94          LUT2 (Prop_lut2_I0_O)        0.119    22.541 r
UART_controller/btx/asynfifo_r1_3/fifomem_b1_i_1/O
                         net (fo=21, routed)          0.507    23.048
UART_controller/btx/asynfifo_r1_3/fifomem_b1/r_fifomem_reg_0_3_0_5/WE
    SLICE_X6Y93          RAMD32                                       r
UART_controller/btx/asynfifo_r1_3/fifomem_b1/r_fifomem_reg_0_3_0_5/RAMB/WE
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from u_datapath/udp_ex_alb_src_reg/Q to
UART_controller/btx/asynfifo_r1_3/fifomem_b1/r_fifomem_reg_0_3_0_5/RAMB/WE:
  Data Path Delay:        14.334ns  (logic 2.735ns (19.080%)  route 11.599ns
(80.920%))

  -------------------------------------------------------------------    -------------
------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X32Y69         FDRE (Prop_fdre_C_Q)         0.456     9.169 r
u_datapath/udp_ex_alb_src_reg/Q
                         net (fo=32, routed)          1.584    10.754
u_datapath/udp_ex_alb_src
    SLICE_X15Y82                                                      r
u_datapath/b_alb_i_16/I1
    SLICE_X15Y82         LUT3 (Prop_lut3_I1_O)        0.152    10.906 r
u_datapath/b_alb_i_16/O
                         net (fo=72, routed)          1.817    12.722
u_datapath/b_alb/bialb_op_b[16]
    SLICE_X3Y57                                                       r
u_datapath/b_alb/boalb_out[23]_INST_0_i_11/I4
    SLICE_X3Y57          LUT5 (Prop_lut5_I4_O)        0.358    13.080 r
u_datapath/b_alb/boalb_out[23]_INST_0_i_11/O
                         net (fo=4, routed)           0.636    13.716
u_datapath/b_alb/boalb_out[23]_INST_0_i_11_n_2
    SLICE_X4Y58                                                       r
u_datapath/b_alb/boalb_out[19]_INST_0_i_5/I1
```

```
    SLICE_X4Y58          LUT6 (Prop_lut6_I1_O)        0.326    14.042 r
u_datapath/b_alb/boalb_out[19]_INST_0_i_5/O
                         net (fo=2, routed)           0.624    14.666
u_datapath/b_alb/boalb_out[19]_INST_0_i_5_n_2
    SLICE_X5Y60                                                   r
u_datapath/b_alb/boalb_out[18]_INST_0_i_1/I1
    SLICE_X5Y60          LUT6 (Prop_lut6_I1_O)        0.124    14.790 r
u_datapath/b_alb/boalb_out[18]_INST_0_i_1/O
                         net (fo=1, routed)           0.899    15.688
u_datapath/b_alb/boalb_out[18]_INST_0_i_1_n_2
    SLICE_X8Y59                                                   r
u_datapath/b_alb/boalb_out[18]_INST_0/I0
    SLICE_X8Y59          LUT6 (Prop_lut6_I0_O)        0.124    15.812 r
u_datapath/b_alb/boalb_out[18]_INST_0/O
                         net (fo=5, routed)           1.409    17.221
u_datapath/addr_decoder/biad_ex_cpu_addr[18]
    SLICE_X12Y73                                                  r
u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_5/I3
    SLICE_X12Y73         LUT4 (Prop_lut4_I3_O)        0.148    17.369 r
u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_5/O
                         net (fo=1, routed)           0.590    17.960
u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_5_n_2
    SLICE_X9Y72                                                   r
u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_3/I4
    SLICE_X9Y72          LUT5 (Prop_lut5_I4_O)        0.328    18.288 r
u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_3/O
                         net (fo=4, routed)           0.909    19.197
u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_3_n_2
    SLICE_X8Y77                                                   r
u_datapath/addr_decoder/boad_io_en[4]_INST_0/I4
    SLICE_X8Y77          LUT6 (Prop_lut6_I4_O)        0.124    19.321 r
u_datapath/addr_decoder/boad_io_en[4]_INST_0/O
                         net (fo=3, routed)           1.275    20.596
UART_controller/uiua_wb_w_stb
    SLICE_X8Y89                                                   r
UART_controller/btx_i_2/I0
    SLICE_X8Y89          LUT4 (Prop_lut4_I0_O)        0.148    20.744 f
UART_controller/btx_i_2/O
                         net (fo=1, routed)           0.452    21.196
UART_controller/btx_i_2_n_2
    SLICE_X8Y89                                                   f
UART_controller/btx_i_1/I3
    SLICE_X8Y89          LUT4 (Prop_lut4_I3_O)        0.328    21.524 r
UART_controller/btx_i_1/O
                         net (fo=2, routed)           0.898    22.422
UART_controller/btx/asynfifo_r1_3/ip_en_w
    SLICE_X5Y94                                                   r
UART_controller/btx/asynfifo_r1_3/fifomem_b1_i_1/I0
    SLICE_X5Y94          LUT2 (Prop_lut2_I0_O)        0.119    22.541 r
UART_controller/btx/asynfifo_r1_3/fifomem_b1_i_1/O
                         net (fo=21, routed)          0.507    23.048
UART_controller/btx/asynfifo_r1_3/fifomem_b1/r_fifomem_reg_0_3_0_5/WE
    SLICE_X6Y93          RAMD32                                   r
UART_controller/btx/asynfifo_r1_3/fifomem_b1/r_fifomem_reg_0_3_0_5/RAMB_D1/WE
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from u_datapath/udp_ex_alb_src_reg/Q to
UART_controller/btx/asynfifo_r1_3/fifomem_b1/r_fifomem_reg_0_3_0_5/RAMB_D1/WE:
  Data Path Delay:        14.334ns  (logic 2.735ns (19.080%)  route 11.599ns
(80.920%))
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---> DF Delay <-----------------------------------------------------------------
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    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X14Y75         FDRE (Prop_fdre_C_Q)         0.518     9.228 r
u_datapath/udp_df_alb_out_reg[2]/Q
                         net (fo=39, routed)          2.116    11.344
GPIO_PORT32/uigpio_wb_r_addr[0]
    SLICE_X3Y98                                                    r
GPIO_PORT32/uogpio_wb_r_dout[4]_INST_0_i_1/I2
    SLICE_X3Y98          LUT5 (Prop_lut5_I2_O)        0.152    11.496 r
GPIO_PORT32/uogpio_wb_r_dout[4]_INST_0_i_1/O
                         net (fo=1, routed)           0.567    12.064
GPIO_PORT32/uogpio_wb_r_dout[4]_INST_0_i_1_n_2
    SLICE_X4Y97                                                    r
GPIO_PORT32/uogpio_wb_r_dout[4]_INST_0/I0
    SLICE_X4Y97          LUT1 (Prop_lut1_I0_O)        0.326    12.390 r
GPIO_PORT32/uogpio_wb_r_dout[4]_INST_0/O
                         net (fo=1, routed)           0.971    13.361
GPIO_PORT32_n_29
    SLICE_X7Y89                                                    r
u_datapath_i_183/I4
    SLICE_X7Y89          LUT6 (Prop_lut6_I4_O)        0.124    13.485 r
u_datapath_i_183/O
                         net (fo=1, routed)           0.889    14.374
u_datapath_i_183_n_2
    SLICE_X11Y86                                                   r
u_datapath_i_119/I0
    SLICE_X11Y86         LUT2 (Prop_lut2_I0_O)        0.124    14.498 r
u_datapath_i_119/O
                         net (fo=1, routed)           0.446    14.945
u_datapath_i_119_n_2
    SLICE_X11Y85                                                   r
u_datapath_i_54/I0
    SLICE_X11Y85         LUT2 (Prop_lut2_I0_O)        0.124    15.069 r
u_datapath_i_54/O
                         net (fo=4, routed)           1.313    16.381
u_datapath/uidp_mdata[4]
    SLICE_X32Y74                                                   r
u_datapath/udp_fw_data_df_rt32[4]_i_1/I0
    SLICE_X32Y74         LUT5 (Prop_lut5_I0_O)        0.124    16.505 r
u_datapath/udp_fw_data_df_rt32[4]_i_1/O
                         net (fo=2, routed)           0.989    17.494
u_datapath/udp_fw_data_ex_rt32[4]
    SLICE_X36Y87                                                   r
u_datapath/uodp_ex_dm_store[4]_INST_0_i_1/I4
    SLICE_X36Y87         LUT5 (Prop_lut5_I4_O)        0.118    17.612 r
u_datapath/uodp_ex_dm_store[4]_INST_0_i_1/O
                         net (fo=1, routed)           0.436    18.049
u_datapath/uodp_ex_dm_store[4]_INST_0_i_1_n_2
    SLICE_X36Y87                                                   r
u_datapath/uodp_ex_dm_store[4]_INST_0/I5
    SLICE_X36Y87         LUT6 (Prop_lut6_I5_O)        0.326    18.375 r
u_datapath/uodp_ex_dm_store[4]_INST_0/O
                         net (fo=18, routed)          1.529    19.903
data_ram/uiram_wb_din[4]
    SLICE_X11Y82                                                   r
data_ram/uram_array_reg_0_i_23/I2
    SLICE_X11Y82         LUT3 (Prop_lut3_I2_O)        0.152    20.055 r
data_ram/uram_array_reg_0_i_23/O
                         net (fo=1, routed)           0.436    20.492
data_ram/uram_array_reg_0_i_23_n_2
    SLICE_X11Y82                                                   r
data_ram/uram_array_reg_0_i_13/I4
    SLICE_X11Y82         LUT5 (Prop_lut5_I4_O)        0.326    20.818 r
data_ram/uram_array_reg_0_i_13/O
                         net (fo=1, routed)           1.141    21.959
data_ram/p_1_in[4]
    RAMB36_X0Y12         RAMB36E1                                  r
data_ram/uram_array_reg_0/DIADI[4]
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from u_datapath/udp_df_alb_out_reg to
data_ram/uram_array_reg_0/DIADI:
```

```
  Data Path Delay:        13.248ns  (logic 2.414ns (18.221%)  route 10.834ns
(81.779%))

  ----------------------------------------------------------------------    -------------
------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  ----------------------------------------------------------------------    -------------
------
    SLICE_X14Y75         FDRE (Prop_fdre_C_Q)         0.518     9.228 r
u_datapath/udp_df_alb_out_reg[2]/Q
                         net (fo=39, routed)          2.116    11.344
GPIO_PORT32/uigpio_wb_r_addr[0]
    SLICE_X3Y98                                                       r
GPIO_PORT32/uogpio_wb_r_dout[4]_INST_0_i_1/I2
    SLICE_X3Y98          LUT5 (Prop_lut5_I2_O)        0.152    11.496 r
GPIO_PORT32/uogpio_wb_r_dout[4]_INST_0_i_1/O
                         net (fo=1, routed)           0.567    12.064
GPIO_PORT32/uogpio_wb_r_dout[4]_INST_0_i_1_n_2
    SLICE_X4Y97                                                       r
GPIO_PORT32/uogpio_wb_r_dout[4]_INST_0/I0
    SLICE_X4Y97          LUT1 (Prop_lut1_I0_O)        0.326    12.390 r
GPIO_PORT32/uogpio_wb_r_dout[4]_INST_0/O
                         net (fo=1, routed)           0.971    13.361
GPIO_PORT32_n_29
    SLICE_X7Y89                                                       r
u_datapath_i_183/I4
    SLICE_X7Y89          LUT6 (Prop_lut6_I4_O)        0.124    13.485 r
u_datapath_i_183/O
                         net (fo=1, routed)           0.889    14.374
u_datapath_i_183_n_2
    SLICE_X11Y86                                                      r
u_datapath_i_119/I0
    SLICE_X11Y86         LUT2 (Prop_lut2_I0_O)        0.124    14.498 r
u_datapath_i_119/O
                         net (fo=1, routed)           0.446    14.945
u_datapath_i_119_n_2
    SLICE_X11Y85                                                      r
u_datapath_i_54/I0
    SLICE_X11Y85         LUT2 (Prop_lut2_I0_O)        0.124    15.069 r
u_datapath_i_54/O
                         net (fo=4, routed)           1.313    16.381
u_datapath/uidp_mdata[4]
    SLICE_X32Y74                                                      r
u_datapath/udp_fw_data_df_rt32[4]_i_1/I0
    SLICE_X32Y74         LUT5 (Prop_lut5_I0_O)        0.124    16.505 r
u_datapath/udp_fw_data_df_rt32[4]_i_1/O
                         net (fo=2, routed)           0.989    17.494
u_datapath/udp_fw_data_ex_rt32[4]
    SLICE_X36Y87                                                      r
u_datapath/uodp_ex_dm_store[4]_INST_0_i_1/I4
    SLICE_X36Y87         LUT5 (Prop_lut5_I4_O)        0.118    17.612 r
u_datapath/uodp_ex_dm_store[4]_INST_0_i_1/O
                         net (fo=1, routed)           0.436    18.049
u_datapath/uodp_ex_dm_store[4]_INST_0_i_1_n_2
    SLICE_X36Y87                                                      r
u_datapath/uodp_ex_dm_store[4]_INST_0/I5
    SLICE_X36Y87         LUT6 (Prop_lut6_I5_O)        0.326    18.375 r
u_datapath/uodp_ex_dm_store[4]_INST_0/O
                         net (fo=18, routed)          1.531    19.905
data_ram/uiram_wb_din[4]
    SLICE_X11Y82                                                      r
data_ram/uram_array_reg_1_i_4/I2
    SLICE_X11Y82         LUT3 (Prop_lut3_I2_O)        0.152    20.057 r
data_ram/uram_array_reg_1_i_4/O
                         net (fo=1, routed)           1.453    21.511
data_ram/p_1_in[20]
    RAMB36_X0Y11         RAMB36E1                                     r
data_ram/uram_array_reg_1/DIADI[4]
  ----------------------------------------------------------------------    -------------
------
  Below shown the delay from u_datapath/udp_df_alb_out_reg to
data_ram/uram_array_reg_1/DIADI:
```

```
  Data Path Delay:        12.800ns  (logic 2.088ns (16.312%)  route 10.712ns
(83.688%))
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~DFTC~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~

---> TC Delay <-----------------------------------------------------------------
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~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~TCWB~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~

  -------------------------------------------------------------------    -------------
------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X56Y83         FDRE (Prop_fdre_C_Q)         0.518     9.220 r
u_datapath/udp_tc_dcache_rd_reg[0]/Q
                         net (fo=42, routed)          0.986    10.206
u_datapath/udp_tc_dcache_rd[0]
    SLICE_X56Y82                                                      r
u_datapath/b_fw_i_2/I2
    SLICE_X56Y82         LUT3 (Prop_lut3_I2_O)        0.124    10.330 r
u_datapath/b_fw_i_2/O
                         net (fo=1, routed)           1.469    11.799
u_datapath/b_fw/bifw_tc_load
    SLICE_X39Y70                                                      r
u_datapath/b_fw/bofw_tc_INST_0/I3
    SLICE_X39Y70         LUT6 (Prop_lut6_I3_O)        0.124    11.923 r
u_datapath/b_fw/bofw_tc_INST_0/O
                         net (fo=33, routed)          3.085    15.008
dcache/uicac_fw_load_data
    SLICE_X64Y88                                                      r
dcache/ucac_tc_cpu_data_tristate_oe[16]_i_1/I1
    SLICE_X64Y88         LUT3 (Prop_lut3_I1_O)        0.150    15.158 r
dcache/ucac_tc_cpu_data_tristate_oe[16]_i_1/O
                         net (fo=1, routed)           0.572    15.730
dcache/ucac_df_cpu_data[16]
    SLICE_X64Y88         FDRE                                         r
dcache/ucac_tc_cpu_data_tristate_oe_reg[16]/D
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from u_datapath/udp_tc_dcache_rd_reg to
dcache/ucac_tc_cpu_data_tristate_oe_reg:
  Data Path Delay:        7.027ns  (logic 0.916ns (13.035%)  route 6.111ns (86.965%))

  -------------------------------------------------------------------    -------------
------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X52Y81         FDRE (Prop_fdre_C_Q)         0.456     9.154 f
u_datapath/udp_tc_lwl_reg/Q
                         net (fo=16, routed)          1.663    10.818
u_datapath/udp_tc_lwl
    SLICE_X56Y83                                                      f
u_datapath/udp_id_fw_rt32_reg[23]_i_11/I3
    SLICE_X56Y83         LUT5 (Prop_lut5_I3_O)        0.124    10.942 f
u_datapath/udp_id_fw_rt32_reg[23]_i_11/O
                         net (fo=24, routed)          2.137    13.079
u_datapath/udp_id_fw_rt32_reg[23]_i_11_n_2
    SLICE_X54Y86                                                      f
u_datapath/udp_id_fw_rt32_reg[11]_i_6/I5
    SLICE_X54Y86         LUT6 (Prop_lut6_I5_O)        0.124    13.203 r
u_datapath/udp_id_fw_rt32_reg[11]_i_6/O
                         net (fo=1, routed)           0.844    14.047
u_datapath/udp_id_fw_rt32_reg[11]_i_6_n_2
    SLICE_X54Y86                                                      r
u_datapath/udp_id_fw_rt32_reg[11]_i_2/I2
```

```
    SLICE_X54Y86         LUT6 (Prop_lut6_I2_O)        0.124    14.171 r
u_datapath/udp_id_fw_rt32_reg[11]_i_2/O
                         net (fo=3, routed)           1.540    15.712
u_datapath/udp_id_fw_rt32_reg[11]_i_2_n_2
    SLICE_X33Y73                                                      r
u_datapath/udp_wb_to_rf[11]_i_1/I3
    SLICE_X33Y73         LUT4 (Prop_lut4_I3_O)        0.124    15.836 r
u_datapath/udp_wb_to_rf[11]_i_1/O
                         net (fo=1, routed)           0.000    15.836
u_datapath/udp_wb_to_rf[11]_i_1_n_2
    SLICE_X33Y73         FDRE                                         r
u_datapath/udp_wb_to_rf_reg[11]/D
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from u_datapath/udp_tc_lwl_reg/Q to
u_datapath/udp_wb_to_rf_reg:
  Data Path Delay:        7.137ns  (logic 0.952ns (13.339%)  route 6.185ns (86.661%))
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~TCWB~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
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~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~TCWB(dcache)~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~

  -------------------------------------------------------------------    -------------
------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X58Y78         FDRE (Prop_fdre_C_Q)         0.518     9.218 r
dcache/ucac_tc_cpu_addr_reg[15]/Q
                         net (fo=7, routed)           1.771    10.989
dcache/b_fifo/bififo_tag_compare[8]
    SLICE_X67Y77                                                      r
dcache/b_fifo/bofifo_hit_INST_0_i_38/I2
    SLICE_X67Y77         LUT6 (Prop_lut6_I2_O)        0.124    11.113 r
dcache/b_fifo/bofifo_hit_INST_0_i_38/O
                         net (fo=1, routed)           0.000    11.113
dcache/b_fifo/bofifo_hit_INST_0_i_38_n_2
    SLICE_X67Y77                                                      r
dcache/b_fifo/bofifo_hit_INST_0_i_17/S[2]
    SLICE_X67Y77         CARRY4 (Prop_carry4_S[2]_CO[3])
                                                      0.398    11.511 r
dcache/b_fifo/bofifo_hit_INST_0_i_17/CO[3]
                         net (fo=1, routed)           0.000    11.511
dcache/b_fifo/bofifo_hit_INST_0_i_17_n_2
    SLICE_X67Y78                                                      r
dcache/b_fifo/bofifo_hit_INST_0_i_9/CI
    SLICE_X67Y78         CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.114    11.625 r
dcache/b_fifo/bofifo_hit_INST_0_i_9/CO[3]
                         net (fo=1, routed)           0.000    11.625
dcache/b_fifo/bofifo_hit_INST_0_i_9_n_2
    SLICE_X67Y79                                                      r
dcache/b_fifo/bofifo_hit_INST_0_i_5/CI
    SLICE_X67Y79         CARRY4 (Prop_carry4_CI_CO[0])
                                                      0.271    11.896 f
dcache/b_fifo/bofifo_hit_INST_0_i_5/CO[0]
                         net (fo=1, routed)           0.754    12.650
dcache/b_fifo/temp22_out
    SLICE_X66Y82                                                      f
dcache/b_fifo/bofifo_hit_INST_0_i_1/I5
    SLICE_X66Y82         LUT6 (Prop_lut6_I5_O)        0.373    13.023 f
dcache/b_fifo/bofifo_hit_INST_0_i_1/O
                         net (fo=286, routed)         1.071    14.094
dcache/b_fifo/bofifo_hit_INST_0_i_1_n_2
    SLICE_X72Y82                                                      f
dcache/b_fifo/bofifo_wb_data[280]_i_5/I1
    SLICE_X72Y82         LUT2 (Prop_lut2_I1_O)        0.152    14.246 r
dcache/b_fifo/bofifo_wb_data[280]_i_5/O
                         net (fo=283, routed)         5.635    19.881
dcache/b_fifo/bofifo_wb_data[280]_i_5_n_2
```

```
    SLICE_X47Y108                                                     r
dcache/b_fifo/bofifo_wb_data[89]_i_2/I1
    SLICE_X47Y108        LUT4 (Prop_lut4_I1_O)        0.332    20.213 r
dcache/b_fifo/bofifo_wb_data[89]_i_2/O
                         net (fo=1, routed)           0.492    20.705
dcache/b_fifo/bofifo_wb_data[89]_i_2_n_2
    SLICE_X48Y109                                                     r
dcache/b_fifo/bofifo_wb_data[89]_i_1/I4
    SLICE_X48Y109        LUT5 (Prop_lut5_I4_O)        0.124    20.829 r
dcache/b_fifo/bofifo_wb_data[89]_i_1/O
                         net (fo=1, routed)           0.000    20.829
dcache/b_fifo/p_40_out[89]
    SLICE_X48Y109        FDRE                                         r
dcache/b_fifo/bofifo_wb_data_reg[89]/D
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from dcache/ucac_tc_cpu_addr_reg to
dcache/b_fifo/bofifo_wb_data_reg:
  Data Path Delay:        12.128ns  (logic 2.406ns (19.838%)  route 9.722ns (80.162%))
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~TCWB(dcache)~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~TCWB(dcache ctrl)~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~

  -------------------------------------------------------------------    -------------
------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X73Y84         FDRE (Prop_fdre_C_Q)         0.456     9.248 r
dcache/b_cache_ctrl/bocac_ctrl_cac_fifo_en_reg/Q
                         net (fo=924, estimated)      1.468    10.716
dcache/ucac_fifo_write
    SLICE_X60Y83                                                      r
dcache/cache_cell_i_37/I1
    SLICE_X60Y83         LUT2 (Prop_lut2_I1_O)        0.124    10.840 r
dcache/cache_cell_i_37/O
                         net (fo=33, routed)          1.094    11.935
dcache/cache_cell/bicr_cpu_read_reg[2]
    SLICE_X63Y86                                                      r
dcache/cache_cell/bocr_dout[7]_INST_0_i_1/I5
    SLICE_X63Y86         LUT6 (Prop_lut6_I5_O)        0.124    12.059 r
dcache/cache_cell/bocr_dout[7]_INST_0_i_1/O
                         net (fo=1, routed)           0.582    12.641
dcache/cache_cell/bocr_dout[7]_INST_0_i_1_n_2
    SLICE_X64Y86                                                      r
dcache/cache_cell/bocr_dout[7]_INST_0/I0
    SLICE_X64Y86         LUT1 (Prop_lut1_I0_O)        0.149    12.790 r
dcache/cache_cell/bocr_dout[7]_INST_0/O
                         net (fo=1, routed)           0.439    13.228
dcache/cache_cell_n_27
    SLICE_X64Y86                                                      r
dcache/uocac_cpu_data[7]_INST_0_i_1/I0
    SLICE_X64Y86         LUT2 (Prop_lut2_I0_O)        0.358    13.586 r
dcache/uocac_cpu_data[7]_INST_0_i_1/O
                         net (fo=3, routed)           1.244    14.830
dcache/ucac_sram_dout[7]
    SLICE_X57Y86                                                      r
dcache/uocac_cpu_data[7]_INST_0/I2
    SLICE_X57Y86         LUT3 (Prop_lut3_I2_O)        0.360    15.190 r
dcache/uocac_cpu_data[7]_INST_0/O
                         net (fo=3, routed)           0.600    15.790
u_datapath/uidp_cache_data[7]
    SLICE_X57Y83                                                      r
u_datapath/udp_id_fw_rt32_reg[14]_i_8/I0
    SLICE_X57Y83         LUT6 (Prop_lut6_I0_O)        0.332    16.122 r
u_datapath/udp_id_fw_rt32_reg[14]_i_8/O
                         net (fo=7, routed)           1.495    17.618
u_datapath/udp_id_fw_rt32_reg[14]_i_8_n_2
    SLICE_X54Y88                                                      r
u_datapath/udp_id_fw_rt32_reg[9]_i_2/I3
```

```
    SLICE_X54Y88         LUT6 (Prop_lut6_I3_O)        0.124    17.742 r
u_datapath/udp_id_fw_rt32_reg[9]_i_2/O
                         net (fo=3, routed)           1.756    19.498
u_datapath/udp_id_fw_rt32_reg[9]_i_2_n_2
    SLICE_X30Y74                                                      r
u_datapath/udp_wb_to_rf[9]_i_1/I3
    SLICE_X30Y74         LUT4 (Prop_lut4_I3_O)        0.124    19.622 r
u_datapath/udp_wb_to_rf[9]_i_1/O
                         net (fo=1, routed)           0.000    19.622
u_datapath/udp_wb_to_rf[9]_i_1_n_2
    SLICE_X30Y74         FDRE                                         r
u_datapath/udp_wb_to_rf_reg[9]/D
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from dcache/b_cache_ctrl/bocac_ctrl_cac_fifo_en_reg/Q to
u_datapath/udp_wb_to_rf_reg:
  Data Path Delay:        10.829ns  (logic 2.151ns (19.863%)  route 8.678ns (80.137%))
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~~~~~~~~~TCWB(dcache ctrl)~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~

---> WB Delay <---------------------------------------------------------------------
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~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~WBEND~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~

  -------------------------------------------------------------------    -------------
------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X40Y70         FDRE (Prop_fdre_C_Q)         0.456     9.166 r
u_datapath/udp_wb_rf_wr_reg/Q
                         net (fo=98, routed)          2.767    11.933
u_datapath/b_rf/brf_reg_ram_reg_r1_0_31_18_23/WE
    SLICE_X46Y79         RAMD32                                       r
u_datapath/b_rf/brf_reg_ram_reg_r1_0_31_18_23/RAMA/WE
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from u_datapath/udp_wb_rf_wr_reg/Q to
u_datapath/b_rf/brf_reg_ram_reg_r1_0_31_18_23/RAMA/WE:
  Data Path Delay:        3.223ns  (logic 0.456ns (14.150%)  route 2.767ns (85.850%))

  -------------------------------------------------------------------    -------------
------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X40Y70         FDRE (Prop_fdre_C_Q)         0.456     9.166 r
u_datapath/udp_wb_rf_wr_reg/Q
                         net (fo=98, routed)          2.767    11.933
u_datapath/b_rf/brf_reg_ram_reg_r1_0_31_18_23/WE
    SLICE_X46Y79         RAMD32                                       r
u_datapath/b_rf/brf_reg_ram_reg_r1_0_31_18_23/RAMA_D1/WE
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from u_datapath/udp_wb_rf_wr_reg/Q to
u_datapath/b_rf/brf_reg_ram_reg_r1_0_31_18_23/RAMA_D1/WE:
  Data Path Delay:        3.223ns  (logic 0.456ns (14.150%)  route 2.767ns (85.850%))

  -------------------------------------------------------------------    -------------
------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X40Y70         FDRE (Prop_fdre_C_Q)         0.456     9.166 r
u_datapath/udp_wb_rf_wr_reg/Q
                         net (fo=98, routed)          2.767    11.933
u_datapath/b_rf/brf_reg_ram_reg_r1_0_31_18_23/WE
```

```
    SLICE_X46Y79         RAMD32                                              r
u_datapath/b_rf/brf_reg_ram_reg_r1_0_31_18_23/RAMB/WE
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from u_datapath/udp_wb_rf_wr_reg/Q to
u_datapath/b_rf/brf_reg_ram_reg_r1_0_31_18_23/RAMB/WE:
  Data Path Delay:        3.223ns  (logic 0.456ns (14.150%)  route 2.767ns (85.850%))

  -------------------------------------------------------------------    -------------
------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X40Y70         FDRE (Prop_fdre_C_Q)         0.456     9.166 r
u_datapath/udp_wb_rf_wr_reg/Q
                         net (fo=98, routed)          2.767    11.933
u_datapath/b_rf/brf_reg_ram_reg_r1_0_31_18_23/WE
    SLICE_X46Y79         RAMD32                                      r
u_datapath/b_rf/brf_reg_ram_reg_r1_0_31_18_23/RAMB_D1/WE
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from u_datapath/udp_wb_rf_wr_reg/Q to
u_datapath/b_rf/brf_reg_ram_reg_r1_0_31_18_23/RAMB_D1/WE:
  Data Path Delay:        3.223ns  (logic 0.456ns (14.150%)  route 2.767ns (85.850%))

  -------------------------------------------------------------------    -------------
------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X40Y70         FDRE (Prop_fdre_C_Q)         0.456     9.166 r
u_datapath/udp_wb_rf_wr_reg/Q
                         net (fo=98, routed)          2.767    11.933
u_datapath/b_rf/brf_reg_ram_reg_r1_0_31_18_23/WE
    SLICE_X46Y79         RAMD32                                      r
u_datapath/b_rf/brf_reg_ram_reg_r1_0_31_18_23/RAMC/WE
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from u_datapath/udp_wb_rf_wr_reg/Q to
u_datapath/b_rf/brf_reg_ram_reg_r1_0_31_18_23/RAMC/WE:
  Data Path Delay:        3.223ns  (logic 0.456ns (14.150%)  route 2.767ns (85.850%))
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~WBEND~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
```

Appendices C: Timing Delay Details of 32-bit 6-Stage Pipeline Processor

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  -------------------------------------------------------------------    -------------
------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X59Y108        FDRE (Prop_fdre_C_Q)         0.456     9.164 r
u_datapath/uodp_if_pseudo_pc_reg[2]/Q
                         net (fo=7, routed)           1.206    10.371
u_datapath/uodp_if_pseudo_pc[2]
    SLICE_X57Y108                                                     r
u_datapath/bp_i_48/DI[1]
    SLICE_X57Y108        CARRY4 (Prop_carry4_DI[1]_CO[3])
                                                      0.507    10.878 r
u_datapath/bp_i_48/CO[3]
                         net (fo=1, routed)           0.000    10.878
u_datapath/bp_i_48_n_2
    SLICE_X57Y109                                                     r
u_datapath/bp_i_47/CI
    SLICE_X57Y109        CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.114    10.992 r
u_datapath/bp_i_47/CO[3]
                         net (fo=1, routed)           0.000    10.992
u_datapath/bp_i_47_n_2
    SLICE_X57Y110                                                     r
u_datapath/bp_i_46/CI
    SLICE_X57Y110        CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.114    11.106 r
u_datapath/bp_i_46/CO[3]
                         net (fo=1, routed)           0.000    11.106
u_datapath/bp_i_46_n_2
    SLICE_X57Y111                                                     r
u_datapath/bp_i_45/CI
    SLICE_X57Y111        CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.114    11.220 r
u_datapath/bp_i_45/CO[3]
                         net (fo=1, routed)           0.000    11.220
u_datapath/bp_i_45_n_2
    SLICE_X57Y112                                                     r
u_datapath/bp_i_44/CI
    SLICE_X57Y112        CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.114    11.334 r
u_datapath/bp_i_44/CO[3]
                         net (fo=1, routed)           0.000    11.334
u_datapath/bp_i_44_n_2
    SLICE_X57Y113                                                     r
u_datapath/bp_i_43/CI
    SLICE_X57Y113        CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.114    11.448 r
u_datapath/bp_i_43/CO[3]
                         net (fo=1, routed)           0.000    11.448
u_datapath/bp_i_43_n_2
    SLICE_X57Y114                                                     r
u_datapath/bp_i_42/CI
    SLICE_X57Y114        CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.114    11.562 r
u_datapath/bp_i_42/CO[3]
                         net (fo=1, routed)           0.000    11.562
u_datapath/bp_i_42_n_2
    SLICE_X57Y115                                                     r
u_datapath/bp_i_41/CI
    SLICE_X57Y115        CARRY4 (Prop_carry4_CI_O[0])
                                                      0.235    11.797 r
u_datapath/bp_i_41/O[0]
                         net (fo=2, routed)           1.197    12.993
u_datapath/bp/bibp_if_pc4[29]
```

```
    SLICE_X57Y120                                                      r
u_datapath/bp/bobp_if_next_pc[29]_INST_0_i_2/I5
    SLICE_X57Y120       LUT6 (Prop_lut6_I5_O)        0.299    13.292 r
u_datapath/bp/bobp_if_next_pc[29]_INST_0_i_2/O
                        net (fo=1, routed)           0.517    13.809
u_datapath/bp/bobp_if_next_pc[29]_INST_0_i_2_n_2
    SLICE_X56Y120                                                      r
u_datapath/bp/bobp_if_next_pc[29]_INST_0/I2
    SLICE_X56Y120       LUT6 (Prop_lut6_I2_O)        0.124    13.933 r
u_datapath/bp/bobp_if_next_pc[29]_INST_0/O
                        net (fo=1, routed)           0.466    14.399
u_datapath/ubp_next_pc[29]
    SLICE_X58Y119                                                      r
u_datapath/uodp_if_pseudo_pc[29]_i_3/I3
    SLICE_X58Y119       LUT6 (Prop_lut6_I3_O)        0.124    14.523 f
u_datapath/uodp_if_pseudo_pc[29]_i_3/O
                        net (fo=1, routed)           0.444    14.967
u_datapath/uodp_if_pseudo_pc[29]_i_3_n_2
    SLICE_X58Y117                                                      f
u_datapath/uodp_if_pseudo_pc[29]_i_2/I5
    SLICE_X58Y117       LUT6 (Prop_lut6_I5_O)        0.124    15.091 r
u_datapath/uodp_if_pseudo_pc[29]_i_2/O
                        net (fo=1, routed)           0.593    15.684
u_datapath/uodp_if_pseudo_pc[29]_i_2_n_2
    SLICE_X58Y116                                                      r
u_datapath/uodp_if_pseudo_pc[29]_i_1/I3
    SLICE_X58Y116       LUT4 (Prop_lut4_I3_O)        0.150    15.834 r
u_datapath/uodp_if_pseudo_pc[29]_i_1/O
                        net (fo=1, routed)           0.000    15.834
u_datapath/p_1_in[29]
    SLICE_X58Y116       FDSE                                           r
u_datapath/uodp_if_pseudo_pc_reg[29]/D
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from u_datapath/uodp_if_pseudo_pc_reg to
u_datapath/uodp_if_pseudo_pc_reg:
  Data Path Delay:        7.126ns  (logic 2.703ns (37.934%)  route 4.423ns (62.066%))
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~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~ISID(icache)~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
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    Location            Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X43Y100       FDRE (Prop_fdre_C_Q)         0.456     9.171 r
icache/ucac_is_reg_index_reg[0]/Q
                        net (fo=33, routed)          1.396    10.567
icache/ucac_is_reg_index[0]
    SLICE_X33Y96                                                       r
icache/cache_cell_i_37/I0
    SLICE_X33Y96        LUT4 (Prop_lut4_I0_O)        0.153    10.720 r
icache/cache_cell_i_37/O
                        net (fo=151, routed)         2.849    13.568
icache/cache_cell/bcr_array_reg_0_255_26_26/A3
    SLICE_X38Y87                                                       r
icache/cache_cell/bcr_array_reg_0_255_26_26/RAMS64E_D/ADR3
    SLICE_X38Y87        RAMS64E (Prop_rams64e_ADR3_O)
                                                     0.327    13.895 r
icache/cache_cell/bcr_array_reg_0_255_26_26/RAMS64E_D/O
                        net (fo=1, routed)           0.000    13.895
icache/cache_cell/bcr_array_reg_0_255_26_26/OD
    SLICE_X38Y87                                                       r
icache/cache_cell/bcr_array_reg_0_255_26_26/F7.B/I0
    SLICE_X38Y87        MUXF7 (Prop_muxf7_I0_O)      0.241    14.136 r
icache/cache_cell/bcr_array_reg_0_255_26_26/F7.B/O
                        net (fo=1, routed)           0.000    14.136
icache/cache_cell/bcr_array_reg_0_255_26_26/O0
```

```
    SLICE_X38Y87                                                       r
icache/cache_cell/bcr_array_reg_0_255_26_26/F8/I0
    SLICE_X38Y87         MUXF8 (Prop_muxf8_I0_O)      0.098    14.234 r
icache/cache_cell/bcr_array_reg_0_255_26_26/F8/O
                         net (fo=1, routed)           0.987    15.221
icache/cache_cell/bcr_dout0[26]
    SLICE_X40Y91                                                       r
icache/cache_cell/bocr_dout[2]_INST_0_i_2/I1
    SLICE_X40Y91         LUT6 (Prop_lut6_I1_O)        0.319    15.540 r
icache/cache_cell/bocr_dout[2]_INST_0_i_2/O
                         net (fo=1, routed)           0.424    15.965
icache/cache_cell/bocr_dout[2]_INST_0_i_2_n_2
    SLICE_X43Y92                                                       r
icache/cache_cell/bocr_dout[2]_INST_0_i_1/I4
    SLICE_X43Y92         LUT5 (Prop_lut5_I4_O)        0.124    16.089 r
icache/cache_cell/bocr_dout[2]_INST_0_i_1/O
                         net (fo=1, routed)           0.474    16.562
icache/cache_cell/bocr_dout[2]_INST_0_i_1_n_2
    SLICE_X43Y92                                                       r
icache/cache_cell/bocr_dout[2]_INST_0/I0
    SLICE_X43Y92         LUT1 (Prop_lut1_I0_O)        0.124    16.686 r
icache/cache_cell/bocr_dout[2]_INST_0/O
                         net (fo=1, routed)           0.514    17.200
icache/cache_cell_n_32
    SLICE_X40Y93                                                       r
icache/ucac_id_mem_data[2]_i_1/I0
    SLICE_X40Y93         LUT2 (Prop_lut2_I0_O)        0.124    17.324 r
icache/ucac_id_mem_data[2]_i_1/O
                         net (fo=1, routed)           0.000    17.324
icache/ucac_is_mem_data[2]
    SLICE_X40Y93         FDRE                                          r
icache/ucac_id_mem_data_reg[2]/D
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from icache/ucac_is_reg_index_reg to
icache/ucac_id_mem_data_reg:
  Data Path Delay:        8.608ns  (logic 1.966ns (22.838%)  route 6.642ns (77.162%))
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~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~ISID(icache)~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
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predictor)~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
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------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X59Y104        FDRE (Prop_fdre_C_Q)         0.456     9.165 r
u_datapath/bp/bbp_is_pc_index_reg[1]/Q
                         net (fo=321, routed)         1.680    10.846
u_datapath/bp/bbp_tag_ram_1_reg_0_15_6_11/ADDRC1
    SLICE_X56Y102                                                      r
u_datapath/bp/bbp_tag_ram_1_reg_0_15_6_11/RAMC/RADR1
    SLICE_X56Y102        RAMD32 (Prop_ramd32_RADR1_O)
                                                      0.153    10.999 r
u_datapath/bp/bbp_tag_ram_1_reg_0_15_6_11/RAMC/O
                         net (fo=1, routed)           0.953    11.952
u_datapath/bp/bbp_is_hit_way[1]1[10]
    SLICE_X57Y103                                                      r
u_datapath/bp/bbp_id_hit_way[1]_i_15/I1
    SLICE_X57Y103        LUT6 (Prop_lut6_I1_O)        0.331    12.283 r
u_datapath/bp/bbp_id_hit_way[1]_i_15/O
                         net (fo=1, routed)           0.000    12.283
u_datapath/bp/bbp_id_hit_way[1]_i_15_n_2
    SLICE_X57Y103                                                      r
u_datapath/bp/bbp_id_hit_way_reg[1]_i_10/S[3]
    SLICE_X57Y103        CARRY4 (Prop_carry4_S[3]_CO[3])
                                                      0.401    12.684 r
u_datapath/bp/bbp_id_hit_way_reg[1]_i_10/CO[3]
```

```
                         net (fo=1, routed)          0.000    12.684
u_datapath/bp/bbp_id_hit_way_reg[1]_i_10_n_2
    SLICE_X57Y104                                                    r
u_datapath/bp/bbp_id_hit_way_reg[1]_i_4/CI
    SLICE_X57Y104        CARRY4 (Prop_carry4_CI_CO[3])
                                                     0.114    12.798 r
u_datapath/bp/bbp_id_hit_way_reg[1]_i_4/CO[3]
                         net (fo=1, routed)          0.000    12.798
u_datapath/bp/bbp_id_hit_way_reg[1]_i_4_n_2
    SLICE_X57Y105                                                    r
u_datapath/bp/bbp_id_hit_way_reg[1]_i_2/CI
    SLICE_X57Y105        CARRY4 (Prop_carry4_CI_CO[0])
                                                     0.271    13.069 r
u_datapath/bp/bbp_id_hit_way_reg[1]_i_2/CO[0]
                         net (fo=1, routed)          1.581    14.650
u_datapath/bp/bbp_is_hit_way[1]0
    SLICE_X49Y123                                                    r
u_datapath/bp/bbp_id_hit_way[1]_i_1/I0
    SLICE_X49Y123        LUT2 (Prop_lut2_I0_O)       0.373    15.023 r
u_datapath/bp/bbp_id_hit_way[1]_i_1/O
                         net (fo=38, routed)         0.804    15.827
u_datapath/bp/bbp_is_hit_way[1]
    SLICE_X47Y123                                                    r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_7/I3
    SLICE_X47Y123        LUT6 (Prop_lut6_I3_O)       0.124    15.951 r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_7/O
                         net (fo=34, routed)         1.019    16.970
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_7_n_2
    SLICE_X49Y120                                                    r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_1/I3
    SLICE_X49Y120        LUT5 (Prop_lut5_I3_O)       0.150    17.120 r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_1/O
                         net (fo=32, routed)         2.351    19.471
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_1_n_2
    SLICE_X60Y111                                                    r
u_datapath/bp/bobp_if_next_pc[15]_INST_0/I0
    SLICE_X60Y111        LUT6 (Prop_lut6_I0_O)       0.326    19.797 r
u_datapath/bp/bobp_if_next_pc[15]_INST_0/O
                         net (fo=1, routed)          0.670    20.467
u_datapath/ubp_next_pc[15]
    SLICE_X60Y111                                                    r
u_datapath/uodp_if_pseudo_pc[15]_i_3/I3
    SLICE_X60Y111        LUT6 (Prop_lut6_I3_O)       0.124    20.591 f
u_datapath/uodp_if_pseudo_pc[15]_i_3/O
                         net (fo=1, routed)          0.501    21.092
u_datapath/uodp_if_pseudo_pc[15]_i_3_n_2
    SLICE_X61Y111                                                    f
u_datapath/uodp_if_pseudo_pc[15]_i_2/I0
    SLICE_X61Y111        LUT6 (Prop_lut6_I0_O)       0.124    21.216 f
u_datapath/uodp_if_pseudo_pc[15]_i_2/O
                         net (fo=1, routed)          0.433    21.649
u_datapath/uodp_if_pseudo_pc[15]_i_2_n_2
    SLICE_X61Y111                                                    f
u_datapath/uodp_if_pseudo_pc[15]_i_1/I3
    SLICE_X61Y111        LUT4 (Prop_lut4_I3_O)       0.124    21.773 r
u_datapath/uodp_if_pseudo_pc[15]_i_1/O
                         net (fo=1, routed)          0.000    21.773
u_datapath/p_1_in[15]
    SLICE_X61Y111        FDRE                                        r
u_datapath/uodp_if_pseudo_pc_reg[15]/D
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from u_datapath/bp/bbp_is_pc_index_reg to
u_datapath/uodp_if_pseudo_pc_reg:
  Data Path Delay:        13.063ns  (logic 3.071ns (23.509%)  route 9.992ns (76.491%))
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~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~ISID(branch
predictor)~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
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~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~IDEX(icache)~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
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    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  ----------------------------------------------------------------------    -------------
------
    SLICE_X47Y99         FDRE (Prop_fdre_C_Q)         0.456     9.183 f
icache/ucac_id_tag_reg/Q
                         net (fo=37, routed)          1.303    10.486
icache/ucac_id_tag_reg_n_2
    SLICE_X39Y97                                                      f
icache/uocac_cpu_data[30]_INST_0/I4
    SLICE_X39Y97         LUT5 (Prop_lut5_I4_O)        0.152    10.638 f
icache/uocac_cpu_data[30]_INST_0/O
                         net (fo=1, routed)           0.452    11.090
urisc_cache_instr[30]
    SLICE_X42Y99                                                      f
u_ctrlpath_i_2/I4
    SLICE_X42Y99         LUT5 (Prop_lut5_I4_O)        0.326    11.416 f
u_ctrlpath_i_2/O
                         net (fo=41, routed)          1.388    12.805
u_ctrlpath/b_mc/bimc_opcode[4]
    SLICE_X45Y108                                                     f
u_ctrlpath/b_mc/bomc_jump_INST_0/I2
    SLICE_X45Y108        LUT6 (Prop_lut6_I2_O)        0.124    12.929 r
u_ctrlpath/b_mc/bomc_jump_INST_0/O
                         net (fo=39, routed)          1.384    14.313
u_datapath/bp/bibp_id_jump
    SLICE_X45Y123                                                     r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_14/I0
    SLICE_X45Y123        LUT2 (Prop_lut2_I0_O)        0.124    14.437 r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_14/O
                         net (fo=2, routed)           1.145    15.581
u_datapath/bp/p_12_out
    SLICE_X49Y109                                                     r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_10/I5
    SLICE_X49Y109        LUT6 (Prop_lut6_I5_O)        0.124    15.705 r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_10/O
                         net (fo=34, routed)          0.868    16.574
u_datapath/bp/bbp_id_mispred_untaken
    SLICE_X54Y110                                                     r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4/I3
    SLICE_X54Y110        LUT4 (Prop_lut4_I3_O)        0.150    16.724 r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4/O
                         net (fo=35, routed)          1.074    17.798
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4_n_2
    SLICE_X58Y105                                                     r
u_datapath/bp/bbp_id_pc_index[3]_i_1/I3
    SLICE_X58Y105        LUT4 (Prop_lut4_I3_O)        0.354    18.152 r
u_datapath/bp/bbp_id_pc_index[3]_i_1/O
                         net (fo=45, routed)          2.337    20.489
u_datapath/bp/bbp_id_read_hit0
    SLICE_X40Y133        FDRE                                         r
u_datapath/bp/bbp_id_lru_reg[0][0]/R
  ----------------------------------------------------------------------    -------------
------
  Below shown the delay from icache/ucac_id_tag_reg/Q to u_datapath/bp/bbp_id_lru_reg:
  Data Path Delay:        11.762ns  (logic 1.810ns (15.389%)  route 9.952ns (84.611%))

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------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  ----------------------------------------------------------------------    -------------
------
    SLICE_X41Y95         FDRE (Prop_fdre_C_Q)         0.456     9.187 r
icache/ucac_id_cpu_read_reg_reg[2]/Q
                         net (fo=38, routed)          1.111    10.297
icache/ucac_id_cpu_read_reg[2]
    SLICE_X42Y99                                                      r
icache/uocac_cpu_data[21]_INST_0/I1
    SLICE_X42Y99         LUT5 (Prop_lut5_I1_O)        0.124    10.421 f
icache/uocac_cpu_data[21]_INST_0/O
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```
                         net (fo=1, routed)          0.689    11.111
urisc_cache_instr[21]
    SLICE_X42Y99                                                       f
u_datapath_i_5/I4
    SLICE_X42Y99         LUT5 (Prop_lut5_I4_O)       0.124    11.235 f
u_datapath_i_5/O
                         net (fo=84, routed)         3.181    14.416
u_datapath/b_itl/biitl_id_rs5[0]
    SLICE_X33Y125                                                      f
u_datapath/b_itl/boitl_ld_use_ifid_en_INST_0_i_6/I0
    SLICE_X33Y125        LUT5 (Prop_lut5_I0_O)       0.124    14.540 f
u_datapath/b_itl/boitl_ld_use_ifid_en_INST_0_i_6/O
                         net (fo=1, routed)          0.464    15.003
u_datapath/b_itl/boitl_ld_use_ifid_en_INST_0_i_6_n_2
    SLICE_X33Y121                                                      f
u_datapath/b_itl/boitl_ld_use_ifid_en_INST_0_i_3/I0
    SLICE_X33Y121        LUT6 (Prop_lut6_I0_O)       0.124    15.127 f
u_datapath/b_itl/boitl_ld_use_ifid_en_INST_0_i_3/O
                         net (fo=2, routed)          1.397    16.524
u_datapath/b_itl/boitl_ld_use_pc_en30_in
    SLICE_X34Y105                                                      f
u_datapath/b_itl/boitl_ld_use_ifid_en_INST_0/I3
    SLICE_X34Y105        LUT5 (Prop_lut5_I3_O)       0.146    16.670 r
u_datapath/b_itl/boitl_ld_use_ifid_en_INST_0/O
                         net (fo=53, routed)         2.125    18.795
u_datapath/uodp_itl_ifid_en
    SLICE_X61Y117                                                      r
u_datapath/udp_cp0_id_pc[31]_i_2/I2
    SLICE_X61Y117        LUT3 (Prop_lut3_I2_O)       0.354    19.149 r
u_datapath/udp_cp0_id_pc[31]_i_2/O
                         net (fo=126, routed)        1.471    20.620
u_datapath/udp_cp0_id_pc[31]_i_2_n_2
    SLICE_X63Y103        FDRE                                          r
u_datapath/udp_is_cp0_id_pc_reg[10]/CE
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from icache/ucac_id_cpu_read_reg_reg to
u_datapath/udp_is_cp0_id_pc_reg:
  Data Path Delay:        11.889ns  (logic 1.452ns (12.212%)  route 10.437ns
(87.788%))
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~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~IDEX(icache)~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
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predictor)~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
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    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X47Y123        FDRE (Prop_fdre_C_Q)        0.419     9.114 f
u_datapath/bp/bbp_id_pred_reg[1]/Q
                         net (fo=36, routed)         3.365    12.479
u_datapath/bp/p_0_in213_in
    SLICE_X49Y109                                                      f
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_13/I0
    SLICE_X49Y109        LUT2 (Prop_lut2_I0_O)       0.327    12.806 r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_13/O
                         net (fo=1, routed)          0.154    12.961
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_13_n_2
    SLICE_X49Y109                                                      r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_10/I4
    SLICE_X49Y109        LUT6 (Prop_lut6_I4_O)       0.326    13.287 r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_10/O
                         net (fo=34, routed)         0.868    14.155
u_datapath/bp/bbp_id_mispred_untaken
    SLICE_X54Y110                                                      r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4/I3
    SLICE_X54Y110        LUT4 (Prop_lut4_I3_O)       0.150    14.305 r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4/O
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                         net (fo=35, routed)          1.074    15.379
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4_n_2
    SLICE_X58Y105                                                     r
u_datapath/bp/bobp_id_nop_ifid_INST_0/I0
    SLICE_X58Y105        LUT2 (Prop_lut2_I0_O)        0.328    15.707 r
u_datapath/bp/bobp_id_nop_ifid_INST_0/O
                         net (fo=4, routed)           0.860    16.567
icache/uicac_bp_flush
    SLICE_X57Y102                                                     r
icache/ucac_id_reg_index[4]_i_1/I0
    SLICE_X57Y102        LUT3 (Prop_lut3_I0_O)        0.124    16.691 r
icache/ucac_id_reg_index[4]_i_1/O
                         net (fo=68, routed)          1.528    18.219
icache/ucac_id_tag0
    SLICE_X35Y92         FDRE                                         r
icache/ucac_id_mem_data_reg[14]/R
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from u_datapath/bp/bbp_id_pred_reg to
icache/ucac_id_mem_data_reg:
  Data Path Delay:        9.523ns  (logic 1.674ns (17.578%)  route 7.849ns (82.422%))

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    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X47Y123        FDRE (Prop_fdre_C_Q)         0.419     9.114 f
u_datapath/bp/bbp_id_pred_reg[1]/Q
                         net (fo=36, routed)          3.365    12.479
u_datapath/bp/p_0_in213_in
    SLICE_X49Y109                                                     f
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_13/I0
    SLICE_X49Y109        LUT2 (Prop_lut2_I0_O)        0.327    12.806 r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_13/O
                         net (fo=1, routed)           0.154    12.961
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_13_n_2
    SLICE_X49Y109                                                     r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_10/I4
    SLICE_X49Y109        LUT6 (Prop_lut6_I4_O)        0.326    13.287 r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_10/O
                         net (fo=34, routed)          0.868    14.155
u_datapath/bp/bbp_id_mispred_untaken
    SLICE_X54Y110                                                     r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4/I3
    SLICE_X54Y110        LUT4 (Prop_lut4_I3_O)        0.150    14.305 r
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4/O
                         net (fo=35, routed)          1.074    15.379
u_datapath/bp/bobp_if_next_pc[31]_INST_0_i_4_n_2
    SLICE_X58Y105                                                     r
u_datapath/bp/bbp_id_pc_index[3]_i_1/I3
    SLICE_X58Y105        LUT4 (Prop_lut4_I3_O)        0.354    15.733 r
u_datapath/bp/bbp_id_pc_index[3]_i_1/O
                         net (fo=45, routed)          2.337    18.070
u_datapath/bp/bbp_id_read_hit0
    SLICE_X40Y133        FDRE                                         r
u_datapath/bp/bbp_id_lru_reg[0][0]/R
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from u_datapath/bp/bbp_id_pred_reg to
u_datapath/bp/bbp_id_lru_reg:
  Data Path Delay:        9.375ns  (logic 1.576ns (16.811%)  route 7.799ns (83.189%))
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~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~IDEX(branch
predictor)~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
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    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X39Y105        FDRE (Prop_fdre_C_Q)         0.456     9.174 r
u_datapath/udp_ex_imm32_reg[6]/Q
                         net (fo=65, routed)          1.743    10.918
u_datapath/udp_ex_shamt[0]
    SLICE_X14Y110                                                 r
u_datapath/b_alb_i_26/I0
    SLICE_X14Y110        LUT3 (Prop_lut3_I0_O)        0.150    11.068 r
u_datapath/b_alb_i_26/O
                         net (fo=75, routed)          1.491    12.559
u_datapath/b_alb/bialb_op_b[6]
    SLICE_X29Y100                                                 r
u_datapath/b_alb/boalb_out[7]_INST_0_i_8/I1
    SLICE_X29Y100        LUT3 (Prop_lut3_I1_O)        0.328    12.887 r
u_datapath/b_alb/boalb_out[7]_INST_0_i_8/O
                         net (fo=1, routed)           0.000    12.887
u_datapath/b_alb/boalb_out[7]_INST_0_i_8_n_2
    SLICE_X29Y100                                                 r
u_datapath/b_alb/boalb_out[7]_INST_0_i_4/S[2]
    SLICE_X29Y100        CARRY4 (Prop_carry4_S[2]_CO[3])
                                                      0.398    13.285 r
u_datapath/b_alb/boalb_out[7]_INST_0_i_4/CO[3]
                         net (fo=1, routed)           0.000    13.285
u_datapath/b_alb/boalb_out[7]_INST_0_i_4_n_2
    SLICE_X29Y101                                                 r
u_datapath/b_alb/boalb_out[11]_INST_0_i_4/CI
    SLICE_X29Y101        CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.114    13.399 r
u_datapath/b_alb/boalb_out[11]_INST_0_i_4/CO[3]
                         net (fo=1, routed)           0.000    13.399
u_datapath/b_alb/boalb_out[11]_INST_0_i_4_n_2
    SLICE_X29Y102                                                 r
u_datapath/b_alb/boalb_out[15]_INST_0_i_4/CI
    SLICE_X29Y102        CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.114    13.513 r
u_datapath/b_alb/boalb_out[15]_INST_0_i_4/CO[3]
                         net (fo=1, routed)           0.000    13.513
u_datapath/b_alb/boalb_out[15]_INST_0_i_4_n_2
    SLICE_X29Y103                                                 r
u_datapath/b_alb/boalb_out[19]_INST_0_i_4/CI
    SLICE_X29Y103        CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.114    13.627 r
u_datapath/b_alb/boalb_out[19]_INST_0_i_4/CO[3]
                         net (fo=1, routed)           0.000    13.627
u_datapath/b_alb/boalb_out[19]_INST_0_i_4_n_2
    SLICE_X29Y104                                                 r
u_datapath/b_alb/boalb_out[23]_INST_0_i_4/CI
    SLICE_X29Y104        CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.114    13.741 r
u_datapath/b_alb/boalb_out[23]_INST_0_i_4/CO[3]
                         net (fo=1, routed)           0.000    13.741
u_datapath/b_alb/boalb_out[23]_INST_0_i_4_n_2
    SLICE_X29Y105                                                 r
u_datapath/b_alb/boalb_out[27]_INST_0_i_4/CI
    SLICE_X29Y105        CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.114    13.855 r
u_datapath/b_alb/boalb_out[27]_INST_0_i_4/CO[3]
                         net (fo=1, routed)           0.000    13.855
u_datapath/b_alb/boalb_out[27]_INST_0_i_4_n_2
    SLICE_X29Y106                                                 r
u_datapath/b_alb/boalb_out[31]_INST_0_i_2/CI
    SLICE_X29Y106        CARRY4 (Prop_carry4_CI_O[3])
                                                      0.313    14.168 r
u_datapath/b_alb/boalb_out[31]_INST_0_i_2/O[3]
                         net (fo=3, routed)           0.672    14.839
u_datapath/b_alb/p_0_in
    SLICE_X39Y104                                                 r
u_datapath/b_alb/boalb_ovfs_INST_0/I3
    SLICE_X39Y104        LUT5 (Prop_lut5_I3_O)        0.306    15.145 r
u_datapath/b_alb/boalb_ovfs_INST_0/O
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                         net (fo=44, routed)          0.807    15.952
u_datapath/b_cp0/bicp0_sovf
    SLICE_X49Y103                                                     r
u_datapath/b_cp0/bocp0_exc_flag_INST_0/I4
    SLICE_X49Y103        LUT6 (Prop_lut6_I4_O)        0.124    16.076 r
u_datapath/b_cp0/bocp0_exc_flag_INST_0/O
                         net (fo=143, routed)         2.618    18.694
u_datapath/uodp_cp0_exc_flag
    SLICE_X10Y102                                                     r
u_datapath/uodp_mem_io_en[4]_i_2/I0
    SLICE_X10Y102        LUT2 (Prop_lut2_I0_O)        0.124    18.818 r
u_datapath/uodp_mem_io_en[4]_i_2/O
                         net (fo=299, routed)         3.538    22.356
u_datapath/uodp_mem_io_en[4]_i_2_n_2
    SLICE_X59Y122        FDRE                                         r
u_datapath/udp_cp0_ex_pc_reg[19]/CE
  -------------------------------------------------------------------    -------------
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  Below shown the delay from u_datapath/udp_ex_imm32_reg to
u_datapath/udp_cp0_ex_pc_reg:
  Data Path Delay:        13.638ns  (logic 2.769ns (20.304%)  route 10.869ns
(79.696%))

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    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X39Y105        FDRE (Prop_fdre_C_Q)         0.456     9.174 r
u_datapath/udp_ex_imm32_reg[6]/Q
                         net (fo=65, routed)          1.743    10.918
u_datapath/udp_ex_shamt[0]
    SLICE_X14Y110                                                     r
u_datapath/b_alb_i_26/I0
    SLICE_X14Y110        LUT3 (Prop_lut3_I0_O)        0.150    11.068 r
u_datapath/b_alb_i_26/O
                         net (fo=75, routed)          1.491    12.559
u_datapath/b_alb/bialb_op_b[6]
    SLICE_X29Y100                                                     r
u_datapath/b_alb/boalb_out[7]_INST_0_i_8/I1
    SLICE_X29Y100        LUT3 (Prop_lut3_I1_O)        0.328    12.887 r
u_datapath/b_alb/boalb_out[7]_INST_0_i_8/O
                         net (fo=1, routed)           0.000    12.887
u_datapath/b_alb/boalb_out[7]_INST_0_i_8_n_2
    SLICE_X29Y100                                                     r
u_datapath/b_alb/boalb_out[7]_INST_0_i_4/S[2]
    SLICE_X29Y100        CARRY4 (Prop_carry4_S[2]_CO[3])
                                                      0.398    13.285 r
u_datapath/b_alb/boalb_out[7]_INST_0_i_4/CO[3]
                         net (fo=1, routed)           0.000    13.285
u_datapath/b_alb/boalb_out[7]_INST_0_i_4_n_2
    SLICE_X29Y101                                                     r
u_datapath/b_alb/boalb_out[11]_INST_0_i_4/CI
    SLICE_X29Y101        CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.114    13.399 r
u_datapath/b_alb/boalb_out[11]_INST_0_i_4/CO[3]
                         net (fo=1, routed)           0.000    13.399
u_datapath/b_alb/boalb_out[11]_INST_0_i_4_n_2
    SLICE_X29Y102                                                     r
u_datapath/b_alb/boalb_out[15]_INST_0_i_4/CI
    SLICE_X29Y102        CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.114    13.513 r
u_datapath/b_alb/boalb_out[15]_INST_0_i_4/CO[3]
                         net (fo=1, routed)           0.000    13.513
u_datapath/b_alb/boalb_out[15]_INST_0_i_4_n_2
    SLICE_X29Y103                                                     r
u_datapath/b_alb/boalb_out[19]_INST_0_i_4/CI
    SLICE_X29Y103        CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.114    13.627 r
u_datapath/b_alb/boalb_out[19]_INST_0_i_4/CO[3]
                         net (fo=1, routed)           0.000    13.627
u_datapath/b_alb/boalb_out[19]_INST_0_i_4_n_2
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    SLICE_X29Y104                                                           r
u_datapath/b_alb/boalb_out[23]_INST_0_i_4/CI
    SLICE_X29Y104        CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.114    13.741 r
u_datapath/b_alb/boalb_out[23]_INST_0_i_4/CO[3]
                         net (fo=1, routed)           0.000    13.741
u_datapath/b_alb/boalb_out[23]_INST_0_i_4_n_2
    SLICE_X29Y105                                                           r
u_datapath/b_alb/boalb_out[27]_INST_0_i_4/CI
    SLICE_X29Y105        CARRY4 (Prop_carry4_CI_O[2])
                                                      0.239    13.980 r
u_datapath/b_alb/boalb_out[27]_INST_0_i_4/O[2]
                         net (fo=1, routed)           1.209    15.189
u_datapath/b_alb/boalb_out[27]_INST_0_i_4_n_7
    SLICE_X28Y118                                                           r
u_datapath/b_alb/boalb_out[26]_INST_0/I3
    SLICE_X28Y118        LUT6 (Prop_lut6_I3_O)        0.302    15.491 r
u_datapath/b_alb/boalb_out[26]_INST_0/O
                         net (fo=3, routed)           0.994    16.485
u_datapath/addr_decoder/biad_ex_cpu_addr[26]
    SLICE_X30Y115                                                           r
u_datapath/addr_decoder/boad_io_en[1]_INST_0_i_1/I0
    SLICE_X30Y115        LUT4 (Prop_lut4_I0_O)        0.150    16.635 r
u_datapath/addr_decoder/boad_io_en[1]_INST_0_i_1/O
                         net (fo=2, routed)           0.839    17.474
u_datapath/addr_decoder/boad_io_en[1]_INST_0_i_1_n_2
    SLICE_X13Y105                                                           r
u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_2/I5
    SLICE_X13Y105        LUT6 (Prop_lut6_I5_O)        0.328    17.802 r
u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_2/O
                         net (fo=3, routed)           0.476    18.278
u_datapath/addr_decoder/boad_io_en[4]_INST_0_i_2_n_2
    SLICE_X12Y109                                                           r
u_datapath/addr_decoder/boad_io_en[4]_INST_0/I4
    SLICE_X12Y109        LUT6 (Prop_lut6_I4_O)        0.124    18.402 r
u_datapath/addr_decoder/boad_io_en[4]_INST_0/O
                         net (fo=3, routed)           0.854    19.256
UART_controller/uiua_wb_w_stb
    SLICE_X8Y120                                                            r
UART_controller/btx_i_2/I0
    SLICE_X8Y120         LUT4 (Prop_lut4_I0_O)        0.116    19.372 f
UART_controller/btx_i_2/O
                         net (fo=1, routed)           0.467    19.840
UART_controller/btx_i_2_n_2
    SLICE_X8Y121                                                            f
UART_controller/btx_i_1/I3
    SLICE_X8Y121         LUT4 (Prop_lut4_I3_O)        0.328    20.168 r
UART_controller/btx_i_1/O
                         net (fo=2, routed)           0.908    21.076
UART_controller/btx/asynfifo_r1_3/ip_en_w
    SLICE_X4Y125                                                            r
UART_controller/btx/asynfifo_r1_3/fifomem_b1_i_1/I0
    SLICE_X4Y125         LUT2 (Prop_lut2_I0_O)        0.119    21.195 r
UART_controller/btx/asynfifo_r1_3/fifomem_b1_i_1/O
                         net (fo=21, routed)          0.759    21.954
UART_controller/btx/asynfifo_r1_3/fifomem_b1/r_fifomem_reg_0_3_0_5/WE
    SLICE_X2Y122         RAMD32                                             r
UART_controller/btx/asynfifo_r1_3/fifomem_b1/r_fifomem_reg_0_3_0_5/RAMA/WE
  -------------------------------------------------------------------    -------------
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  Below shown the delay from u_datapath/udp_ex_imm32_reg to
UART_controller/btx/asynfifo_r1_3/fifomem_b1/r_fifomem_reg_0_3_0_5/RAMA/WE:
  Data Path Delay:        13.236ns  (logic 3.494ns (26.399%)  route 9.742ns (73.601%))
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    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
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  -------------------------------------------------------------------    -------------
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    SLICE_X9Y101         FDRE (Prop_fdre_C_Q)         0.456     9.182 r
u_datapath/udp_mem_alb_out_reg[5]/Q
                         net (fo=47, routed)          1.561    10.744
dcache/ucac_tag_ram_reg_0_3_5_5/A0
    SLICE_X10Y93                                                      r
dcache/ucac_tag_ram_reg_0_3_5_5/SP/ADR0
    SLICE_X10Y93         RAMS32 (Prop_rams32_ADR0_O)
                                                      0.124    10.868 r
dcache/ucac_tag_ram_reg_0_3_5_5/SP/O
                         net (fo=5, routed)           1.077    11.945
dcache/bififo_data0[5]
    SLICE_X10Y99                                                      r
dcache/uocac_cpu_stall_INST_0_i_15/I0
    SLICE_X10Y99         LUT6 (Prop_lut6_I0_O)        0.124    12.069 r
dcache/uocac_cpu_stall_INST_0_i_15/O
                         net (fo=1, routed)           0.000    12.069
dcache/uocac_cpu_stall_INST_0_i_15_n_2
    SLICE_X10Y99                                                      r
dcache/uocac_cpu_stall_INST_0_i_8/S[1]
    SLICE_X10Y99         CARRY4 (Prop_carry4_S[1]_CO[3])
                                                      0.533    12.602 r
dcache/uocac_cpu_stall_INST_0_i_8/CO[3]
                         net (fo=1, routed)           0.001    12.603
dcache/uocac_cpu_stall_INST_0_i_8_n_2
    SLICE_X10Y100                                                     r
dcache/uocac_cpu_stall_INST_0_i_6/CI
    SLICE_X10Y100        CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.117    12.720 r
dcache/uocac_cpu_stall_INST_0_i_6/CO[3]
                         net (fo=1, routed)           0.000    12.720
dcache/uocac_cpu_stall_INST_0_i_6_n_2
    SLICE_X10Y101                                                     r
dcache/uocac_cpu_stall_INST_0_i_1/CI
    SLICE_X10Y101        CARRY4 (Prop_carry4_CI_CO[0])
                                                      0.254    12.974 r
dcache/uocac_cpu_stall_INST_0_i_1/CO[0]
                         net (fo=3, routed)           0.874    13.848
dcache/ucac_hit1
    SLICE_X5Y98                                                       r
dcache/b_cache_ctrl_i_2/I0
    SLICE_X5Y98          LUT5 (Prop_lut5_I0_O)        0.367    14.215 r
dcache/b_cache_ctrl_i_2/O
                         net (fo=19, routed)          0.609    14.824
dcache/b_cache_ctrl/bicac_ctrl_hit
    SLICE_X2Y96                                                       r
dcache/b_cache_ctrl/bocac_ctrl_cpu_data_output_en_INST_0/I1
    SLICE_X2Y96          LUT4 (Prop_lut4_I1_O)        0.117    14.941 r
dcache/b_cache_ctrl/bocac_ctrl_cpu_data_output_en_INST_0/O
                         net (fo=2, routed)           0.629    15.570
dcache/cache_cell/bicr_cpu_data_output_en
    SLICE_X4Y101                                                      r
dcache/cache_cell/enz_31_INST_0/I0
    SLICE_X4Y101         LUT4 (Prop_lut4_I0_O)        0.348    15.918 r
dcache/cache_cell/enz_31_INST_0/O
                         net (fo=64, routed)          1.232    17.150    dcache_n_156
    SLICE_X9Y107                                                      r
u_datapath_i_162/I3
    SLICE_X9Y107         LUT6 (Prop_lut6_I3_O)        0.124    17.274 r
u_datapath_i_162/O
                         net (fo=1, routed)           1.008    18.281
u_datapath_i_162_n_2
    SLICE_X10Y113                                                     r
u_datapath_i_97/I1
    SLICE_X10Y113        LUT2 (Prop_lut2_I1_O)        0.150    18.431 r
u_datapath_i_97/O
                         net (fo=1, routed)           0.430    18.861
u_datapath_i_97_n_2
    SLICE_X10Y113                                                     r
u_datapath_i_43/I0
    SLICE_X10Y113        LUT2 (Prop_lut2_I0_O)        0.355    19.216 r
u_datapath_i_43/O
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                         net (fo=7, routed)          0.840    20.057
u_datapath/uidp_mdata[15]
    SLICE_X10Y111                                                      r
u_datapath/uodp_ex_dm_store[31]_INST_0_i_4/I1
    SLICE_X10Y111        LUT3 (Prop_lut3_I1_O)       0.148    20.205 r
u_datapath/uodp_ex_dm_store[31]_INST_0_i_4/O
                         net (fo=17, routed)         0.813    21.017
u_datapath/uodp_ex_dm_store[31]_INST_0_i_4_n_2
    SLICE_X9Y114                                                       r
u_datapath/uodp_ex_dm_store[27]_INST_0_i_2/I1
    SLICE_X9Y114         LUT6 (Prop_lut6_I1_O)       0.328    21.345 r
u_datapath/uodp_ex_dm_store[27]_INST_0_i_2/O
                         net (fo=5, routed)          0.894    22.239
u_datapath/data4[27]
    SLICE_X12Y117                                                      r
u_datapath/uodp_ex_dm_store[27]_INST_0_i_1/I0
    SLICE_X12Y117        LUT3 (Prop_lut3_I0_O)       0.150    22.389 r
u_datapath/uodp_ex_dm_store[27]_INST_0_i_1/O
                         net (fo=3, routed)          0.633    23.023
u_datapath/udp_fw_data_ex_rt32[27]
    SLICE_X10Y115                                                      r
u_datapath/uodp_ex_dm_store[19]_INST_0/I0
    SLICE_X10Y115        LUT6 (Prop_lut6_I0_O)       0.348    23.371 r
u_datapath/uodp_ex_dm_store[19]_INST_0/O
                         net (fo=7, routed)          1.252    24.623
dcache/uicac_cpu_data[19]
    SLICE_X5Y94                                                        r
dcache/cache_cell_i_13/I4
    SLICE_X5Y94          LUT5 (Prop_lut5_I4_O)       0.124    24.747 r
dcache/cache_cell_i_13/O
                         net (fo=1, routed)          0.790    25.537
dcache/cache_cell/bicr_din[19]
    SLICE_X6Y94                                                        r
dcache/cache_cell/bcr_array_reg_i_6/I0
    SLICE_X6Y94          LUT3 (Prop_lut3_I0_O)       0.153    25.690 r
dcache/cache_cell/bcr_array_reg_i_6/O
                         net (fo=1, routed)          0.547    26.237
dcache/cache_cell/bcr_array_reg_i_6_n_2
    RAMB18_X0Y38         RAMB18E1                                      r
dcache/cache_cell/bcr_array_reg/DIADI[11]
  -------------------------------------------------------------------    -------------
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  Below shown the delay from u_datapath/udp_mem_alb_out_reg to
dcache/cache_cell/bcr_array_reg/DIADI:
  Data Path Delay:        17.511ns  (logic 4.320ns (24.671%)  route 13.191ns
(75.329%))
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    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X32Y123        FDSE (Prop_fdse_C_Q)        0.456     9.158 r
u_datapath/udp_wb_rt5_rd5_reg[1]/Q
                         net (fo=98, routed)         2.946    12.104
u_datapath/b_rf/brf_reg_ram_reg_r2_0_31_0_5/ADDRD1
    SLICE_X42Y105        RAMD32                                        r
u_datapath/b_rf/brf_reg_ram_reg_r2_0_31_0_5/RAMA/WADR1
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from u_datapath/udp_wb_rt5_rd5_reg to
u_datapath/b_rf/brf_reg_ram_reg_r2_0_31_0_5/RAMA/WADR1:
  Data Path Delay:        3.402ns  (logic 0.456ns (13.406%)  route 2.946ns (86.594%))

  -------------------------------------------------------------------    -------------
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    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X32Y123        FDSE (Prop_fdse_C_Q)         0.456     9.158 r
u_datapath/udp_wb_rt5_rd5_reg[1]/Q
                         net (fo=98, routed)          2.946    12.104
u_datapath/b_rf/brf_reg_ram_reg_r2_0_31_0_5/ADDRD1
    SLICE_X42Y105        RAMD32                                        r
u_datapath/b_rf/brf_reg_ram_reg_r2_0_31_0_5/RAMA_D1/WADR1
  -------------------------------------------------------------------    -------------
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  Below shown the delay from u_datapath/udp_wb_rt5_rd5_reg to
u_datapath/b_rf/brf_reg_ram_reg_r2_0_31_0_5/RAMA_D1/WADR1:
  Data Path Delay:        3.402ns  (logic 0.456ns (13.406%)  route 2.946ns (86.594%))

  -------------------------------------------------------------------    -------------
------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X32Y123        FDSE (Prop_fdse_C_Q)         0.456     9.158 r
u_datapath/udp_wb_rt5_rd5_reg[1]/Q
                         net (fo=98, routed)          2.946    12.104
u_datapath/b_rf/brf_reg_ram_reg_r2_0_31_0_5/ADDRD1
    SLICE_X42Y105        RAMD32                                        r
u_datapath/b_rf/brf_reg_ram_reg_r2_0_31_0_5/RAMB/WADR1
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from u_datapath/udp_wb_rt5_rd5_reg to
u_datapath/b_rf/brf_reg_ram_reg_r2_0_31_0_5/RAMB/WADR1:
  Data Path Delay:        3.402ns  (logic 0.456ns (13.406%)  route 2.946ns (86.594%))

  -------------------------------------------------------------------    -------------
------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X32Y123        FDSE (Prop_fdse_C_Q)         0.456     9.158 r
u_datapath/udp_wb_rt5_rd5_reg[1]/Q
                         net (fo=98, routed)          2.946    12.104
u_datapath/b_rf/brf_reg_ram_reg_r2_0_31_0_5/ADDRD1
    SLICE_X42Y105        RAMD32                                        r
u_datapath/b_rf/brf_reg_ram_reg_r2_0_31_0_5/RAMB_D1/WADR1
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from u_datapath/udp_wb_rt5_rd5_reg to
u_datapath/b_rf/brf_reg_ram_reg_r2_0_31_0_5/RAMB_D1/WADR1:
  Data Path Delay:        3.402ns  (logic 0.456ns (13.406%)  route 2.946ns (86.594%))

  -------------------------------------------------------------------    -------------
------
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------    -------------
------
    SLICE_X32Y123        FDSE (Prop_fdse_C_Q)         0.456     9.158 r
u_datapath/udp_wb_rt5_rd5_reg[1]/Q
                         net (fo=98, routed)          2.946    12.104
u_datapath/b_rf/brf_reg_ram_reg_r2_0_31_0_5/ADDRD1
    SLICE_X42Y105        RAMD32                                        r
u_datapath/b_rf/brf_reg_ram_reg_r2_0_31_0_5/RAMC/WADR1
  -------------------------------------------------------------------    -------------
------
  Below shown the delay from u_datapath/udp_wb_rt5_rd5_reg to
u_datapath/b_rf/brf_reg_ram_reg_r2_0_31_0_5/RAMC/WADR1:
  Data Path Delay:        3.402ns  (logic 0.456ns (13.406%)  route 2.946ns (86.594%))
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WEEKLY LOG

FINAL YEAR PROJECT WEEKLY REPORT

(Project II)

Trimester, Year: Y3T3	**Study week no.: Week 2**
Student Name & ID: Choo Jia Zheng, 18ACB03197	
Supervisor: Mr. Lee Heng Yew	
Project Title: Design of A 7-Stage Pipeline RISC Processor (Mem Stage)	

1. WORK DONE

- Studied the existing RISC 5-stage pipeline processor system specifications.
- Studied the existing 5-stage datapath unit, udp (Kiat, 2018)
- Studied the existing 6-stage datapath unit, udp (Teng, 2021)
- Run simulation, synthesis and implementation on the existing pipeline processor model.
- Learnt TCL Scripting to obtain Timing Delay for each processor pipeline stage.

2. WORK TO BE DONE

- Decompose the dcache unit into 2 separate stages. (RTL modelling)
- Develop testbench for the new pipelined dcache unit
- Perform functional test and verification on the new dcache unit. (Simulation Test)
- Decompose the datapath unit into 7 stages. (RTL modelling)
- Modify the address decoder block

3. PROBLEMS ENCOUNTERED

- Certain seniors' works are lack of documentation. Need additional time to identify and learnt the knowledge solely from the RTL coding before modifying it.

4. SELF EVALUATION OF THE PROGRESS

- Currently all my progress is on time and is following the proposed FYP II Gantt Chart.

Heng Yew

Supervisor's signature

Student's signature

FINAL YEAR PROJECT WEEKLY REPORT

(Project II)

Trimester, Year: Y3T3	**Study week no.: Week 4**
Student Name & ID: Choo Jia Zheng, 18ACB03197	
Supervisor: Mr. Lee Heng Yew	
Project Title: Design of A 7-Stage Pipeline RISC Processor (Mem-Stage)	

1. WORK DONE

- Decomposed the dcache unit into 2 separate stages. (RTL modelling)
- Developed testbench for the new pipelined dcache unit
- Performed functional test and verification on the new dcache unit. (Simulation Test)
- Decomposed the datapath unit into 7 stages. (RTL modelling)
- Modified the address decoder block

2. WORK TO BE DONE

- Modify the forwarding block
- Modify the interlock block
- Modify CPU testbench and create instruction hex file that include dcache read and write test.
- Perform functional test and verification on the newly developed 7-stage pipeline processor. (Simulation Test)

3. PROBLEMS ENCOUNTERED

- Certain seniors' works are lack of documentation. Need additional time to identify and learnt the knowledge solely from the RTL coding before modifying it.

4. SELF EVALUATION OF THE PROGRESS

- Currently all my progress is on time and is following the proposed FYP II Gantt Chart.

Heng Yew

Supervisor's signature

Student's signature

FINAL YEAR PROJECT WEEKLY REPORT

(Project II)

Trimester, Year: Y3T3	**Study week no.: Week 6**
Student Name & ID: Choo Jia Zheng, 18ACB03197	
Supervisor: Mr. Lee Heng Yew	
Project Title: Design of A 7-Stage Pipeline RISC Processor (Mem-Stage)	

1. WORK DONE

- Modified the forwarding block
- Modified the interlock block
- Modified CPU testbench and created instruction hex file that include dcache read and write test.
- Performed functional test and verification on the newly developed 7-stage pipeline processor. (Simulation Test)

2. WORK TO BE DONE

- Run synthesis and implementation of the developed 7-stage pipeline processor
- Generate the timing delay for each stage using TCL scripting.

3. PROBLEMS ENCOUNTERED

- Certain seniors' works are lack of documentation. Need additional time to identify and learnt the knowledge solely from the RTL coding before modifying it.

4. SELF EVALUATION OF THE PROGRESS

- Currently all my progress is on time and is following the proposed FYP II Gantt Chart.

Heng Yew

Supervisor's signature

Student's signature

FINAL YEAR PROJECT WEEKLY REPORT

(Project II)

Trimester, Year: Y3T3	**Study week no.: Week 8**
Student Name & ID: Choo Jia Zheng, 18ACB03197	
Supervisor: Mr. Lee Heng Yew	
Project Title: Design of A 7-Stage Pipeline RISC Processor (Mem-Stage)	

1. WORK DONE

- Run synthesis and implementation of the developed 7-stage pipeline processor
- Generated the timing delay for each stage using TCL scripting.
- Modified some designs in order to reduce the routing delay in the design
- Rerun simulation test and regenerated the new timing delay.

2. WORK TO BE DONE

- Start writing FYP II report.
- Prepare FYP II poster.

3. PROBLEMS ENCOUNTERED

- Timing delay generated is not as expected due to the routing delay.
- Certain seniors' works are lack of documentation. Need additional time to identify and learnt the knowledge solely from the RTL coding before modifying it.

4. SELF EVALUATION OF THE PROGRESS

- Currently all my progress is on time and is following the proposed FYP II Gantt Chart.

Heng Yew

Supervisor's signature

Student's signature

FINAL YEAR PROJECT WEEKLY REPORT

(Project II)

Trimester, Year: Y3T3	**Study week no.: Week 10**
Student Name & ID: Choo Jia Zheng, 18ACB03197	
Supervisor: Mr. Lee Heng Yew	
Project Title: Design of A 7-Stage Pipeline RISC Processor (Mem-Stage)	

1. WORK DONE

- Complete 80% FYP II report.

2. WORK TO BE DONE

- Continue writing the report.
- Prepare FYP II poster.

3. PROBLEMS ENCOUNTERED

- Study week is packed with other assignment from other courses, causing delay in writing the FYP II report.
- Certain seniors' works are lack of documentation. Need additional time to identify and learnt the knowledge solely from the RTL coding before modifying it.

4. SELF EVALUATION OF THE PROGRESS

- Currently my progress is left behind the schedule as proposed in the Gantt Chart. Need to put in more effort.

Heng Yew

Supervisor's signature

Student's signature

FINAL YEAR PROJECT WEEKLY REPORT

(Project II)

Trimester, Year: Y3T3	**Study week no.: Week 12**
Student Name & ID: Choo Jia Zheng, 18ACB03197	
Supervisor: Mr. Lee Heng Yew	
Project Title: Design of A 7-Stage Pipeline RISC Processor (Mem-Stage)	

1. WORK DONE

- Complete FYP II draft report and sent to supervisor for checking.

2. WORK TO BE DONE

- Prepare for FYP II presentation.

3. PROBLEMS ENCOUNTERED

- Certain seniors' works are lack of documentation. Need additional time to identify and learnt the knowledge solely from the RTL coding before modifying it.

4. SELF EVALUATION OF THE PROGRESS

- Currently all my progress is on time and is following the proposed FYP II Gantt Chart.

Heng Yew

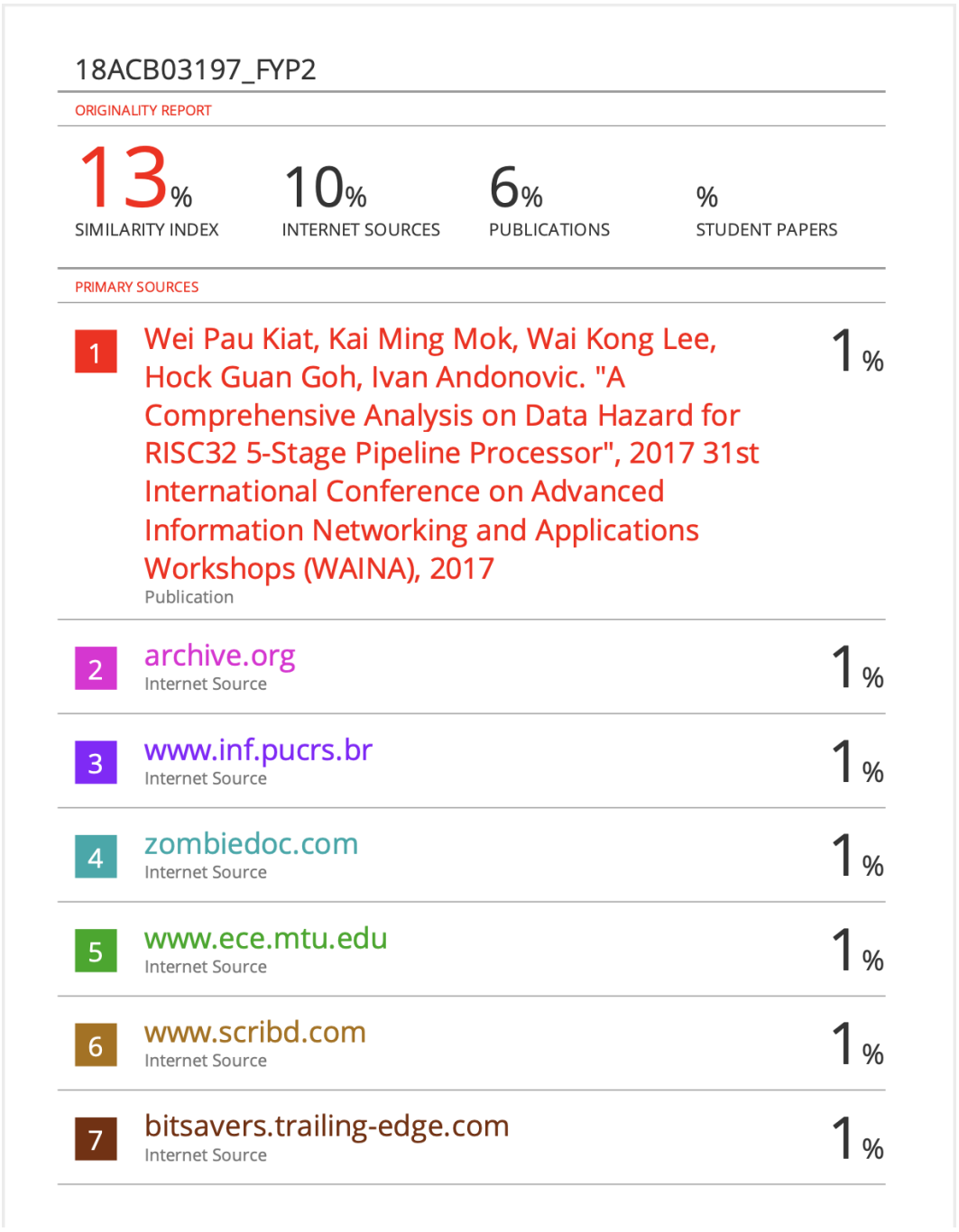
Supervisor's signature

Student's signature

POSTER


DESIGN OF A 7-STAGE PIPELINE RISC PROCESSOR (MEM STAGE)
By: Choo Jia Zheng
Supervised by: Mr Lee Heng Yew
Moderated by: Ts Ooi Joo On
Special Thanks : Mr Mok Kai Ming
INTRODUCTION
A basic pipeline processor is built in FICT, UTAR by CT seniors.
RISC – Reduced Instruction Set Computer
5-stages: IF, ID, EX, MEM, WB
MIPS-ISA compatible
Pipeline: Instructions are overlapped in execution. Performance improved by increasing CPU throughput
OBJECTIVES
To design and implement a 7-stage pipeline processor by splitting the components in the MEM stage of the basic 5-stage pipeline processor to achieve a higher processor clock rate.
To develop a complete test plan to test and verify the functional correctness of the 7-stage pipeline processor designed.
To synthesis and implement the 7-stage pipeline processor using the FPGA technology.
DISCUSSION
The performance of the existing 6-stage pipeline processor is reduced due to the imbalance timing delay among the pipeline stages
The clock rate of the processor must be the longest delay among the pipeline stages for the instruction to execute without error.
MEM stage has the longest delay – 17.511ns where the maximum clock rate of the processor could only be 57.107MHz
Further pipelining the MEM stage is necessary.
METHODOLOGY
Top-down methodology is used
uArch Specification is determined, Partitioning
Unit and block level specification modelling and verification
Logic synthesis for FPGA
Implement a physical design
CONCLUSION
All the project objectives are achieved.
Data Cache is decomposed into 2 stages
7-stage pipeline processor is successfully designed and developed.
Longest timing delay is reduced which lead to the increase in performance for the pipeline processor
New processor clock rate: 67.590Mhz
RESULTS
Pipeline Stage | IF | IS | ID | EX | DF | TC | WB
Timing Delay (ns) | 6.9140 | 11.918 | 12.368 | 14.795 | 13.248 | 12.128 | 3.2230
UTAR
UNIVERSITI TUNKU ABDUL RAHMAN
Bachelor of Information System (Hons) Computer Engineering
Faculty of Information and Communication Technology (Perak)

PLAGIARISM CHECK RESULT



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PRIMARY SOURCES

1	Wei Pau Kiat, Kai Ming Mok, Wai Kong Lee, Hock Guan Goh, Ivan Andonovic. "A Comprehensive Analysis on Data Hazard for RISC32 5-Stage Pipeline Processor", 2017 31st International Conference on Advanced Information Networking and Applications Workshops (WAINA), 2017 Publication	1%
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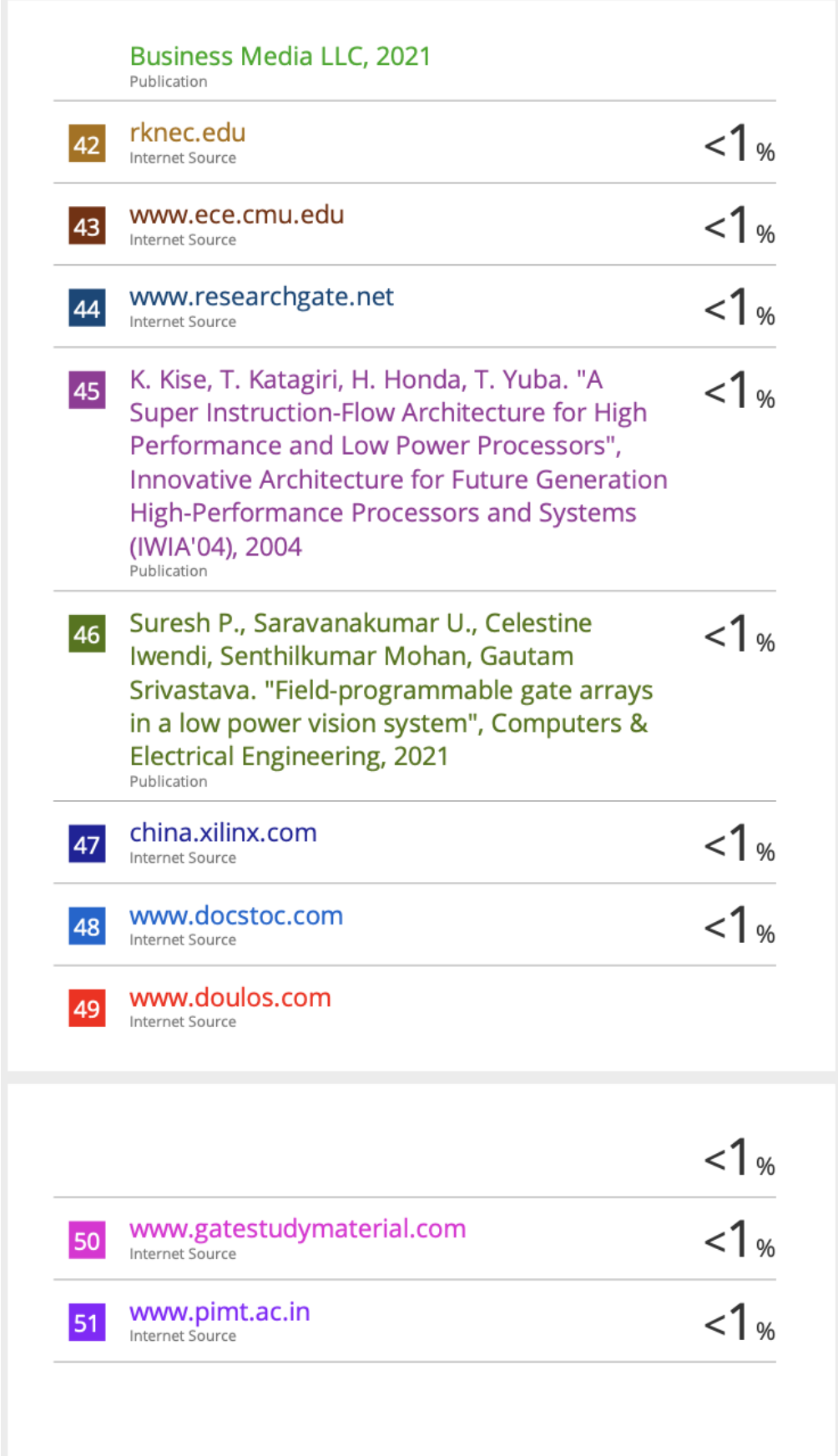

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Full Name(s) of Candidate(s)	CHOO JIA ZHENG
ID Number(s)	18ACB03197
Programme / Course	Bachelor of Information Technology (Honours) Computer Engineering
Title of Final Year Project	Design of a 7-Stage RISC Pipeline Processor (MEM Stage)

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Note Supervisor/Candidate(s) is/are required to provide softcopy of full set of the originality report to Faculty/Institute

Based on the above results, I hereby declare that I am satisfied with the originality of the Final Year Project Report submitted by my student(s) as named above.

Heng Yew

Signature of Supervisor	Signature of Co-Supervisor
Name: Mr Lee Heng Yew	Name:
Date: 18th APRIL 2022	Date:

UNIVERSITI TUNKU ABDUL RAHMAN

FACULTY OF INFORMATION & COMMUNICATION TECHNOLOGY (KAMPAR CAMPUS)

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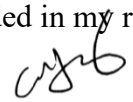

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