POWER MANAGEMENT UNIT FOR LOW POWER WIRELESS SENSOR NETWORK

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A project report submitted in partial fulfilment of the requirements for the award of Bachelor of Engineering (Honours) Electrical and Electronics Engineering

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April 2022

DECLARATION

I hereby declare that this project report is based on my original work except for citations and quotations which have been duly acknowledged. I also declare that it has not been previously and concurrently submitted for any other degree or award at UTAR or other institutions.

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APPROVAL FOR SUBMISSION

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ACKNOWLEDGEMENTS

Firstly, I would like to express my very great appreciation to Dr. Khaw Mei Kum, my final year project supervisor, for her valuable guidance and expert advice in doing this project. In addition, the willingness of sparing her time to share her knowledge and experience.

Besides, I would like to thank Mr. Khoo from Mentor Graphics for his guidance during the FYP part one too. Without him, I wouldn't know much about the EDA tools.

Lastly, I would like to thank my family and friends for supporting me through the completion of this project.

ABSTRACT

Wireless sensor networks play an important role in monitoring the condition of the railway structure in the railway transport industry. However, a commercial wireless sensor node is not very promising for this application since the batteries will degrade over a certain time. Moreover, these wireless sensors that were used to monitor the condition of railways were usually deployed in harsh environments such as rural railways, hence making the battery changing process harder. The importance of this study is to provide an infinite power source for the wireless sensor nodes in railway monitoring applications by designing a power management unit (PMU) that manages the harvested power effectively. The available ambient energies were studied and an electromagnetic kinetic energy harvester was chosen and modelled. The PMU is targeted to regulate the harvested energies from the passing trains (harvested by a Electromagnetic Kinetic Energy Harvester) and outputs a stable 3.3 V to the loads. The PMU proposed in this study includes a rectifier and buck converter and it was constructed in 45nm CMOS technology. The performance of the PMU proposed has been analysed and proven to achieve an efficiency of more than 80% and a power of 36 mW was successfully generated which is sufficient to power the wireless sensor. This approach results in low power consumption, low output current and voltage ripple.

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LIST OF SYMBOLS / ABBREVIATIONS

WSN	Wireless Sensor Network
PMU	Power Management Unit

CHAPTER 1

INTRODUCTION

1.1 General Introduction

Wireless sensor network (WSN) has gained worldwide attention ever since the Industry Revolution 4.0 emphasizes that the Internet of Things (IoT) technologies will be utilised for object tracking, and structure-health monitoring. In an automated monitoring system, wireless sensor networks play an important role as it is an essential part of data acquisition in the Industrial Revolution 4.0 thanks to its ability to be deployed without communication structures. Wireless sensor network technology enables a sensor network to carry out its monitoring and tracking purposes. A wireless sensor network allows its nodes to communicate with and control one another. It can be used to monitor infrastructure such as buildings and railways wirelessly. Modern railways aim to provide a safe and sustainable form of transport worldwide. In order to provide a high level of safety for trains, a reliable railway infrastructure maintained in a good condition is crucial for safe and smooth transportation. To achieve that, preventive maintenance and scheduled maintenance techniques are recently being used for trackside infrastructure, where the critical deformation and defects of the railway can be detected. However, the traditional way of continuous condition monitoring could be a very hard and costly solution as the railway is usually located in a rural area which is very hard to reach. Current developments in wireless sensor network technologies have resulted in a significantly smaller size, higher efficiency, and lower energy consumption. Thus, wire sensors in railway applications are often being abandoned and replaced by wireless alternatives.

1.2 Problem Statement

However, a wireless sensor network needs a huge amount of energy to supply the wireless sensor nodes for the continual process of sensing, data reading, data storing, computing, actuating and data transmission. Although some of the proposed network minimizes power consumption based on protocols as well as communication methods to prolong the working period of wireless sensor nodes powered by batteries, this solution is not promising since batteries will degrade over a certain period. The energy consumption of wireless sensor networks is a significant concern as the energy of a battery is limited. Even though energy is an important resource in every wireless device, the energy issue in wireless sensor networks is more vital. Moreover, a wireless sensor network usually consists of many nodes and are deployed in very hard-to-reach areas such as railways making the replacement of the battery become more challenging and costly.

1.3 Importance of the Study

Many studies have been carried out on an energy harvesting system that rely on multiple sources to extend the wireless sensor network's lifetime. However, the trade-off of implementing a hybrid energy harvesting system is that a more complex power management unit (PMU) must be introduced to process the multiple input energies and power up the wireless sensor networks efficiently.

According to Panatik, *et al*. (2016), low power wireless sensor networks should be self-sustainable, reliable, maintenance-free, and operate with required perpetuity. As the quantity of nodes in a wireless sensor system increases, the maintenance of the wireless sensor network can be a burden and inconvenient since the locations of wireless sensor nodes are usually difficult or even impossible to reach. However, most commercially available wireless sensor nodes are power-hungry and powered by batteries that only have a limited lifetime. As a wireless sensor node requires a huge amount of energy when operating, the battery will be exhausted quickly resulting in energy scarcity. According to Sakya, *et al*. (2020), due to limited life of the batteries and high-power consumption of energy, the high frequency of battery replacement is a vital issue for wireless sensor networks.

The importance of this study is to extend the wireless sensor network's lifetime by designing a power management unit (PMU) that manages the harvested power effectively. A high-efficient power management circuit can increase the stability of the wireless sensor network.

1.4 Aim and Objectives

The aim of this study is to propose a power management unit design to power the wireless sensor node with the harvested ambient energy as well as:

- To study the characteristics of the available ambient energy and developing a model for energy harvesting suitable for the WSN.
- To design a power management unit to manage the harvested energy for railways monitoring without the aid of batteries.
- To analyse the effectiveness of the proposed PMU at regulating the harvested energies.

1.5 Scope and Limitation of the Study

The study focused on a PMU design that can manage multiple input energy harvesting sources and multiple output loads effectively. The scope of this study includes just the power management circuit instead of the energy harvesting unit and the wireless sensor nodes. The study focuses on managing the input power sources from the energy harvesting unit to power the wireless sensor nodes. Thus, there are two limitations in this study one of which includes the components of a wireless sensor node will not be designed in this study as it will be used as a testbench to study the performance of the designed PMU. Another limitation in this study is the components of an energy harvester such as electromagnetic energy harvester will not be designed. The energy harvested will be modelled as an input for the PMU to power the wireless sensor nodes.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Wireless sensor devices can be powered through direct energy sources or batteries. An indoor wireless sensor network can be powered by many energy sources whereas outdoor sensor or mobile sensor networks can be powered by a battery supply. To reduce the dependency of wireless sensor networks on batteries, several energy harvesting techniques from the surrounding environment were introduced. Making use of the energy harvesting technique as an alternative energy source to replace batteries is the most promising solution to develop an autonomous wireless sensor network (Kamalinejad, *et al*., 2015). Some research even introduced a hybrid energy harvesting system by combining multiple ambient energy sources.

2.2 Literature Review

In order to find the most suitable energy harvesting technology for monitoring the railway condition, the following sections of this literature review will be divided into 3 parts. The first section is a study of different energy harvesting techniques which will outline the range of commonly exploited energy sources. The output waveform of each type of energy harvester will be studied to further understand the waveform characteristic of the harvested energy. The second part extensively discusses the previous works on power management circuit design for wireless sensor networks, and the last part provides a summary of the loads in a typical wireless sensor node that will be used as a testbench in this study.

2.2.1 Energy Harvesting Sources

Energy harvester is an environmental-friendly, autonomous technology that generates energy from any available energy sources like radio frequency and mechanical energy that are present in the environment. The generated energy will then be used to regulate energy management systems such as rectifiers and kept in an energy reservoir such as battery or load as shown in Figure 2.1 (Dixit, *et al*., 2017).

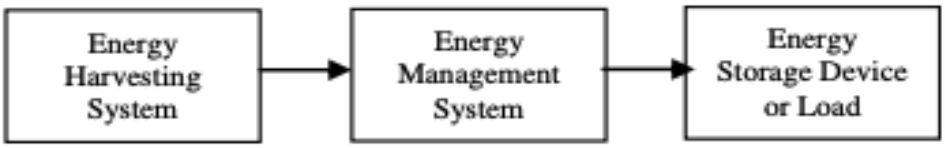

Figure 2.1: Conventional System of an Energy Harvester. (Dixit, et al., 2017).

According to Philip and Singh (2020), energy sources can be categorized into two main groups which are ambient natural energy and artificial energy as presented in Figure 2.2. Ambient energy sources such as solar, wind, thermal energy etc. are freely available in the surrounding environment. Thus, adapting these energy sources can provide sufficient and unlimited energy to power wireless sensor networks for an infinite amount of time. However, artificial energy such as heat, vibration, and pressure are not freely available in the surrounding, but the power density is higher than the energy harvested from ambient sources (Dixit *et al*., 2017).

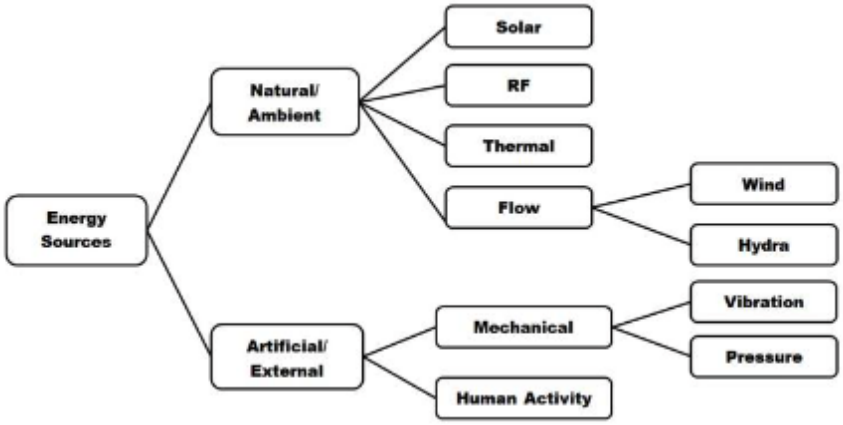

Figure 2.2: Energy Harvesting Sources. (Dixit, et al., 2017).

The electrical and physical properties such as power density, voltage generated, maximum power generated, voltage generated, form-factor, and cost need to be taken into consideration when selecting the type of energy harvester in a system as it will determine the overall sustainability and the stability of the system (Mitcheson *et al*., 2008).

2.2.2 Mechanical Energy Harvester

Vibration generates mechanical energy through capturing the mechanical movement from the environment. This kind of mechanical source can be turned into usable DC electrical energy through three same principle yet slightly different mechanisms: piezoelectric, electromagnetic, and electrostatic (Dixit *et al*., 2017). Many researchers adapt this kind of energy harvesting method in many applications like aerospace, deep sea, mining, and human movement as it is green, deployable, and cost-efficient for harvesting power in wireless sensor network applications.

A. Piezoelectric

The piezoelectric generates electrical potential gradient when there is mechanical stress applied on it. When there is mechanical stress like motion, and vibration applied on it, an electric field will be formed. The electric field produced is dependent on the applied stress (Lee, *et al*. 2016).

Piezoelectric received a lot of attention among the three mechanisms due to its high-power densities and simple mechanism. In addition, unlike the electrostatic harvester, usable output voltage can be directly obtained from piezoelectric energy harvester (Erturk, *et al*., 2011).

There has been a lot of proposed work using piezoelectric methods to power wireless sensor networks such as Yang, *et al*. (2015), developed an energy harvesting system using piezoelectric that can harvest mechanical energy from a single-pressing button. The energy harvesting system can generate 160 μJ at 2.5V to send a signal over a distance to a transceiver. Besides, Zhu, *et al*. (2012) conducted a study on the vibration frequency distribution on the various surface roads. They found out that a wide frequency distribution is found in all the vibration captured. They made a conclusion that the resonant frequency of a cantilever beam is the key to maximize the amount of the energy harvested through the piezoelectric harvester.

B. Electromagnetic

Electromagnetic energy harvesters generate energy through electromagnetic induction. The electromagnetic generators provide the advantage of reliable technology as they can work on low frequencies, less mechanical damping and can be easily implemented in both macro and micro scale. However, electromagnetic energy harvesters are only suitable to be applied as a low power source as they provide a low power output. The output power of this energy harvesting method can be related to the flux density, coil impedance, load impedance and the number of coils turns. The output power of electromagnetic energy harvesters decreases at micro-electromechanical systems due to the small size of magnet, and coil (Dixit, *et al*., 2017). According to Hudak and Amactucci (2008), because of strong magnetic fields which can interfere with the electronics components, this kind of energy harvester technology may be complicated to integrate with microelectronics like wireless sensor networks.

When compared to other methods, electromagnetic harvesting method is not widely used in wireless sensor network applications due to its nature. Several improvements have been done such as Kulah and Najafi (2004) improved the system by adding a transformer to increase the induced voltage. However, the device size was still a main problem for integrated micro-electromechanical system technology. In addition, Ching, *et al*., (2012) designed an electromagnetic energy harvester that was optimized to have a lower resonant frequency of 110 Hz. The proposed design can supply an output of 4.4 V and 830 μW with an acceleration of 96 ms^{-2}.

The waveform generated by an electromagnetic kinetic energy harvester is highly dependent on the received kinetic energy. If the kinetic energy available is predicted, this kind of energy harvesting technology can generate a very decent amount of power. Hadas, *et al*., (2021) implemented a kinetic electromagnetic energy harvester that aims to harvest energy from the passing trains. The waveform generated by the harvester is shown in Figure 2.3 below.

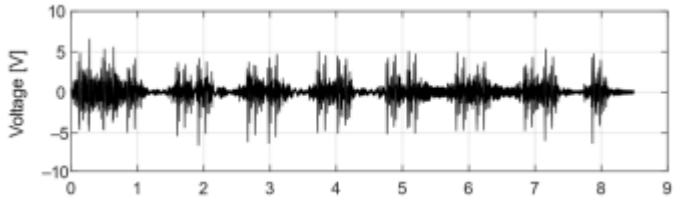

Figure 2.3: Voltage generated from a 80 km/h passing train.

C. Electrostatic

The electrostatic harvesting method generates voltage based on the change in capacitance in a system, but it requires an initial start-up voltage in advance (Pasquale, *et al*., 2009). Cevik, *et al*. (2015) explained that the harvested energy is provided with the work done against the electrostatic force between the plates of the capacitor used. Due to the advantage of high output voltage, simplicity in terms of its mechanism, and the ease to integrate with microelectronic devices, electrostatic methods are one of the most popular methods in small scale energy harvesters. However, energy generated by electrostatic harvesters is low in energy density (Hudak and Amactucci, 2008). As aforementioned, the electrostatic transducer requires two power sources to start-up the energy harvesting process. Therefore, a passive electrostatic energy harvester is suitable to apply as an auxiliary supply source, and it is very hard to achieve a maintenance-free wireless sensor node design. Many efforts have been carried out to bypass the external power supply required to start-up the electrostatic generator. However, the generated output power is very low making the electrostatic energy harvester not very suitable to be used to supply the wireless sensor network (Tang, *et al*., 2018).

2.2.3 Thermal Energy Harvester

Harvesting energy from thermal sources is a very reliable solution as it captures freely available heat in the environment and converts it to usable electrical energy to power up devices. Moreover, due to no moving parts in this energy harvesting system, they are way more durable than the mechanical vibration energy harvester. According to Kishore and Priya (2018), thermal energy harvesters are one of the most suitable energy harvesters for autonomous

wireless sensor network applications as they require very little maintenance and can be implemented in remote areas due to the factors mentioned above. The most common energy harvesting for wireless sensor application is thermoelectric and pyroelectric.

A. Thermoelectric

Thermoelectric generates energy based on the Seebeck Effect and generates voltage based on the temperature gradient at the joining of two different conductors. Generally, the higher the temperature difference between the two conductors, the higher the amount of energy that will be generated. The open circuit voltage depends on the temperature difference of the two conductors, and the material properties which are the Seebeck coefficients. In a nutshell, the generated output is proportional to the temperature difference and thermoelectric material.

According to Shaikh and Zeadally (2016), the performance of a thermoelectric under a low temperature difference working environment is not very ideal. However, in a high temperature difference working environment, the generated power density is highly dependent on the temperature gradient.

To achieve a constant voltage and a stable power, a stable temperature gradient must be maintained. Otherwise, when the thermoelectric harvesting unit is placed in a stable temperature difference environment, it will stop generating power. Even though the thermoelectric energy harvester has many advantages such as longer lifetime as it only contains stationary parts, and high efficiency in high temperature difference, they are very hard to be implemented in an outdoor environment where temperature is spatially uniform.

Donnelly. M (2019) designed a thermoelectric generator (TEG) that is supplied on the hot side by a sinusoidally time varying temperature between 75 °C and 100 °C. The thermoelectric energy harvester is shown in the Figure 2.4 and Figure 2.5 below. From the Figure 2.4 below, the TEG generates a higher peak voltage of up to 1.9 V when the temperature captured is above 88 °C. A constant little voltage of above 0.7 V is generated if the temperature captured is under 88 °C.

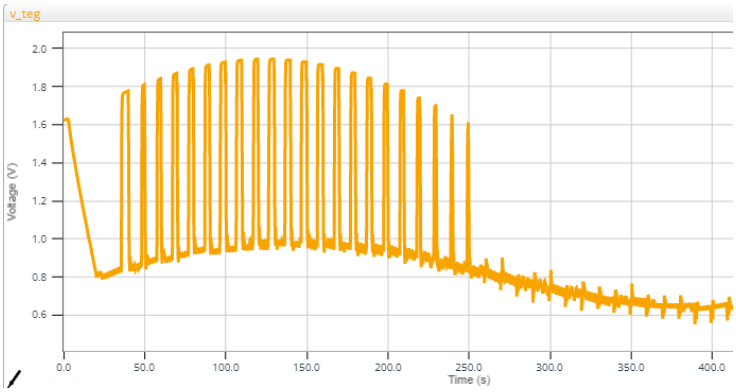

Figure 2.4: Harvested energy by thermoelectric generator.

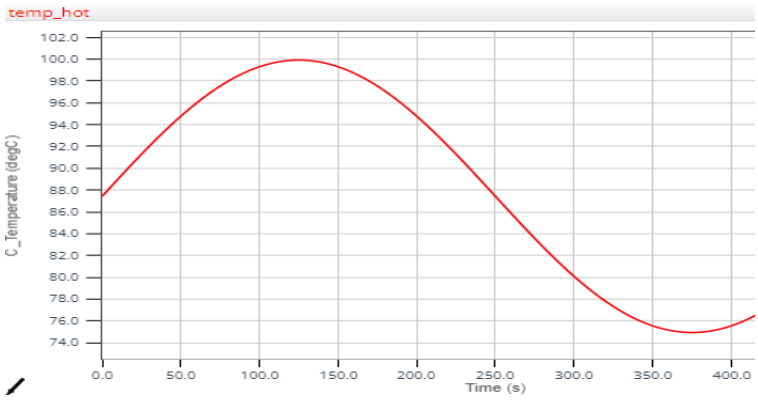

Figure 2.5: Temperature captured by the TEG.

B. Pyroelectric

Pyroelectric harvesting method generates energy based on the pyroelectric effect where it generates alternating current electricity depending on the difference of the polarisation as the material is heated or cooled. No electricity will be generated if the temperature gradient is constant. Therefore, to provide a constant voltage, a constant temperature gradient must be introduced to the harvesting device. The advantages of this technology are low cost, wide spectrum response with high sensitivity, and long-life due to the fact that it contains only stationary parts.

Although pyroelectric energy harvesters are suitable to be used in a broad range of temperatures, deploying them in a suitable environment could be challenging and difficult. Another challenging

problem on pyroelectric harvester is the efficiency of the system is highly reliant on the material selection and structure.

2.2.4 Solar Energy Harvester

Photovoltaic effect is where solar energy is being converted into usable electrical energy. The energy conversion efficiency of a photovoltaic harvester relies on the efficiency of the cell and the light intensity (Akhtar, *et al*., 2015). The solar harvesting method is a very promising technique to power the sensor nodes. According to Tabbakh *et al*. (2010), photovoltaic is suitable for wireless sensor network application as it is a mature technology and reliable.

The existing solar harvesting technology can be applied in many scenarios. However, the drawback of this technology is solar energy only available during the daytime and may only last for a short period even if it is stored efficiently. In addition, the photovoltaic cell needs to be aligned with the solar source to achieve maximum conversion efficiency. To overcome this, Wiliams *et al*. (2017), introduced an adaptive solar tracker that can automatically track the solar source and align the cells to achieve optimum position. Secondly, a maximum power point tracker should be applied in this technology to ensure the system is harvesting solar energy at its maximum power point.

As one of the most popular energy harvesting methods in small-scale energy harvesting technology, many research have been conducted on the capabilities of the solar energy harvester. Mathuna *et al*. (2008) conducted a study to investigate the efficiency of various solar cells at several different illumination levels. He found out that for a sunny outdoor condition with an illumination level of 500 Wm^3, the harvesting unit has an efficiency range around 15% to 25%. However, for an indoor environment with an illumination level of 10 Wm^3, the conversion efficiency is only around 2% to 10%. Thus, it is clearly shown that this kind of harvesting technology has a better performance at outdoor application.

The output waveform generated from a solar energy harvester is highly dependent on the weather, area of the solar panel and the solar irradiance. Furthermore, the solar irradiance cannot be predicted and it

varies everyday depending on the latitude and climate. The Figure 2.6 below shows the energy harvested of a solar panel simulated in a very ideal situation (Akbar, *et al*., 2017). The solar panel used in his design is roughly 100 cm^2. In certain conditions, the solar panel size is too big making it not suitable to deploy in a very hard to reach area like forest. The size of the solar panel should be taken into consideration as it will affect the power generated.

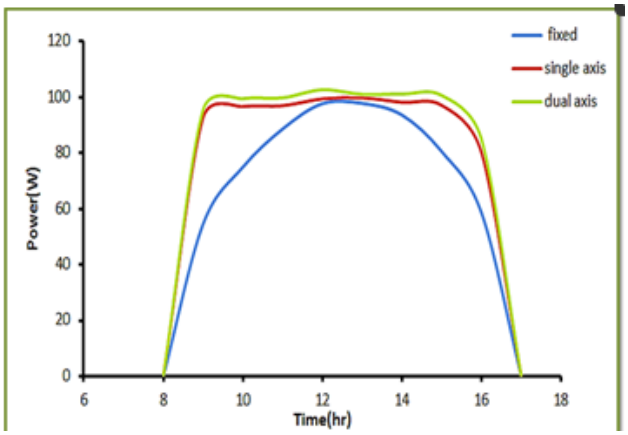

Figure 2.6: Energy harvested by solar energy harvester.

2.2.5 Radiofrequency Harvester

A radiofrequency harvester converts received transmitted radio waves into a device usable DC power source. The radio frequency harvester is a very popular solution to power the wireless sensor network as it has a small size, long lifetime due to no moving parts, and the cost of production is relatively low. Furthermore, a survey conducted by Pinuela, *et al*. (2013) concluded that radio frequency energy has a more consistent present than the other types of energy harvesting method. The conversion efficiency of this technology depends on the distance between the transmission source and receiver. The energy of the harvested radio frequency will decrease as the distance of the receiver and the transmission source becomes further (Shaikh and Zeadally, 2016).

The source of radio frequency can be categorized into two main groups which are dedicated sources and ambient sources. Dedicated sources are designed to supply predictable energy to specific sensor

devices in a designed coverage (Kamalinejad, *et al*., 2015). On the other hand, the ambient sources are anticipated radio frequency sources that are unrelated to wireless sensor networks and can be harvested from a lot of transmission infrastructure in the surroundings such as broadcast stations of TV, cellular base stations, and radio towers (Shakh and Zeadally, 2016). According to Muncuk, *et al*. (2018), dedicated sources are said to be more suitable for indoor wireless sensor network applications where ambient radio frequency sources are scarce. Due to the increase of penetration of wireless networking and broadcasting infrastructure in urban areas, the ambient radio frequency is said to be more reliable as it can provide higher energy density in a heavily urbanised area.

Generally, Muncuk, *et al*. (2018) found that the ambient radio frequency energy harvesting is a very promising technique to power wireless sensor nodes that is deployed in highly developed city and semi-urban areas. The study focused on the multiband radio frequency harvesting in the city of Boston and he developed a circuit that can harvest from 3 different bands which are LTE at 700 Mhz, GSM at 850 Mhz, and also ISM at 900 Mhz with a 45% conversion efficiency.

The waveform generated by radiofrequency has a sine wave waveform (Perinot and Caironi, 2018). The amplitude and frequency of the generated sine wave is dependent on the type of the radiofrequency harvested.

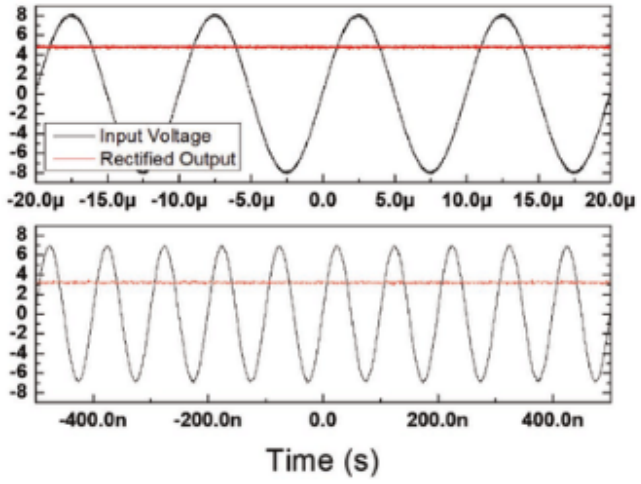

Figure 2.7: Waveform generated by the RF harvester.

2.2.6 Summary of Energy Harvester

There are factors that need to be taken into consideration when it comes to selecting a harvesting method for an application. Each kind of harvesting technology has their advantages and their drawbacks as shown in the Table 2.1 below. Thus, it is necessary to consider all the factors such as the available ambient energy sources with consideration of the node's location, function, and their power consumption to achieve a better reliability of the wireless sensor network system. For the wireless sensor nodes for trackside applications, mechanical vibration energy harvester is a very promising harvesting technology as the output waveform generated can be predicted easily.

Table 2.1: Summary of Energy Harvester.

Energy harvested	Technique	Application	Advantages	Disadvantages	Power Density
Mechanical	Piezoelectric	Industrial machinery; Transportation;	Operate at low frequencies	Needs resonant frequency matching; Contains moving part; Low output voltage; AC only;	330 μW/cm^3 (Shenck and Paradiso, 2001)
	Electromagnetic		-	Needs resonant frequency matching; Contains moving part; Needs startup voltage; AC only;	184 μW/cm^3 @ 10 Hz (Zorlu, et al., 2011)
	Electrostatic		High voltage output; High power density;	Needs resonant frequency matching; Contains moving part; Needs startup voltage; AC only;	0.021 μW/mm^3 @ 105 Hz (Sheu, et al., 2011)

				Not effective at low frequency;	
Thermal	Thermoelectric	Waste heat; Domestic heater;	High reliability; Long-life span;	Requires constant thermal gradient; Low conversion efficiency;	150 mW @ 34 Temp Gradient (Lu and Yang ,2011)
	Pyroelectric		Low-cost; Long-lie span;	Requires constant temperature gradient;	34 nW/cm^2 @ 30 Temp Gradient (Sultan, et al., 2018)
Solar	Photovotaic	Sunlight; Artificial Light;	Mature tech; Predictable; No moving parts;	Depant on the weather; Natural prediction limited;	15 mW/cm^2 @ 100 mW/cm^2 Illuminance level (Mathuana, et al.,2018)
Radio Frequency		Urban; Semi-urban; Dedicated transmitter setup;	Freely available; No moving parts;	Requires tuning to frequency bands; Inconsistant if non-dedicated;	88 µW @ 900Mhz (Roberto, et.al., 2019)

2.3 Power Management System

According to Prauzek, *et al*. (2018), there are three main methods to manage the incoming energy from energy harvesters which are batteryless harvesting system, hybrid harvesting system, and battery-supplemented system. The batteryless harvesting system harvests energy from ambient sources and then supplies them directly to the nodes. Thus, the nodes will only awake when the harvested energy is enough to power the sensor nodes. This system is simple and reliable as it avoids the usage of storing elements. On the other hand, the hybrid harvesting system consists of a storage module such as a capacitor as an auxiliary element. Lastly, the battery-supplemented harvesting system consists of a battery as the main reservoir to store the harvested energy. The limitation of this system is battery replacement would be required after serving for a period. The selection of the method depends on the operation modes of the wireless sensor nodes.

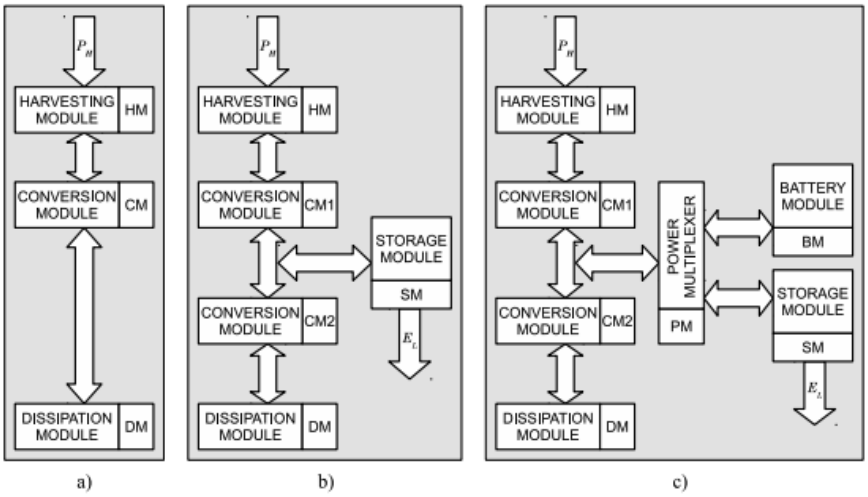

Figure 2.8: (a) Batteryless harvesting system; (b) Hybrid Harvesting System; (c) Battery-supplemented System. (Prauzek, et al., 2018).

2.3.1 Previous work on PMU Design

To overcome the battery lifetime problem in a battery-supplemented wireless sensor node system powered by a solar harvester, Shaltout, *et al*. (2016) proposed a power management circuit that bypass the battery charger when the solar harvesters are not able to supply sufficient power to charge the battery. Figure 2.9 is a simplified block diagram of a conventional wireless sensor node

powered by a battery charged by a solar harvester. The proposed power management circuit is shown in Figure 2.10.

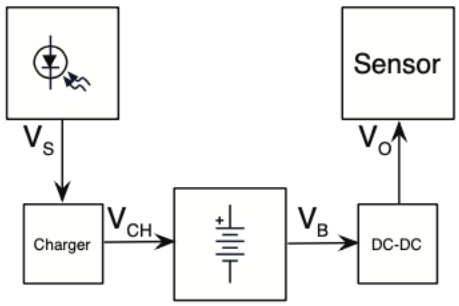

Figure 2.9: Block Diagram of Conventional Battery Charged WSN System. (Shaltout, et al., 2016).

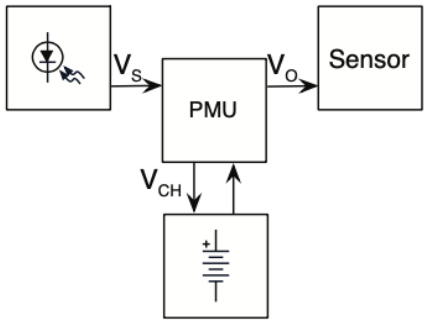

Figure 2.10: Proposed System. (Shaltout, et al., 2016).

Shaltout claimed that the proposed power management system design can be utilized not only to recharge the batteries but also provide power to the sensors when possible. However, the proposed design can be very bulky since it contains a battery module and the battery will degrade after a certain period of time making the wireless sensor network not reliable. Roberto, *et al*. (2019) suggested that to achieve the energy harvesting requirement for the next generation, a System on Chip (SoC) approach will provide alternative methods for powering a maintenance-free wireless sensor network.

Chew, *et al*. (2019) presented an adaptive power management circuit to power a wireless sensor network efficiency by using the energy harvested from piezoelectric energy harvester. Several techniques were used in this approach to maximize the energy transfer from the harvester. He pointed out that even though many of the studies focuses on the MPPT capability of the system, but the harvested energy will then be transferred to an energy reservoir such as

capacitors and such configuration is not energy efficiency as the energy will be continuously drained by the load attached causing the leftover energy to be unable to initiate the wireless sensor nodes. Thus, he proposed a low power consumption circuit that can power up the system directly with just the harvested energy without any external start up provided.

The proposed system consists of several main components including a full wave rectifier, an analogue control circuit namely ACC, a DC-DC converter, a storage capacitor, as well as an energy aware system. The schematic of the circuit is shown below.

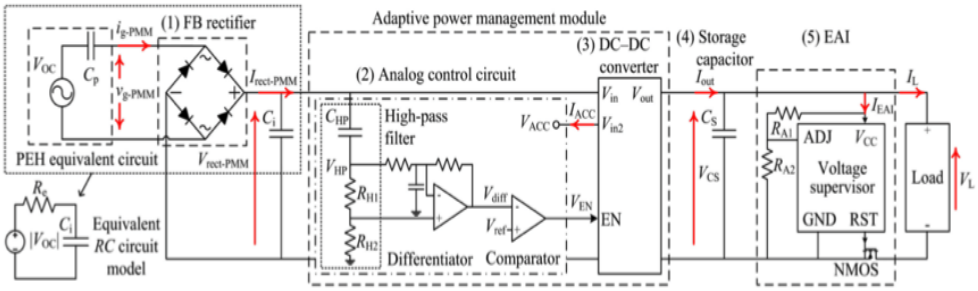

Figure 2.11: Schematic circuit diagram of the proposed system. (Chew, 2019).

The operation of the circuit can be divided into three stages as in Figure 2.12. At stage 1, the ACC disabled the DC-DC converter making half of the harvested energy, $V_{OC/2}$ from piezoelectric can be charged up by the smoothing capacitor, C_I. At stage 2, the ACC will then send a high signal "V_{EN}" to enable the DC-DC converter to work. Once the $V_{rect\text{-}PMM}$ falls below the $V_{OC/2}$, the circuit will return to Stage 1 and the circuit will alternate between these two stages until the storage capacitor is charged up. When the storage capacitor is fully charged, stage 3 will occur where the NMOS will be turned ON by the RST of the voltage supervisor in order for the load to be connected to the ground. A closed circuit will be formed causing the storage capacitor to charge the load.

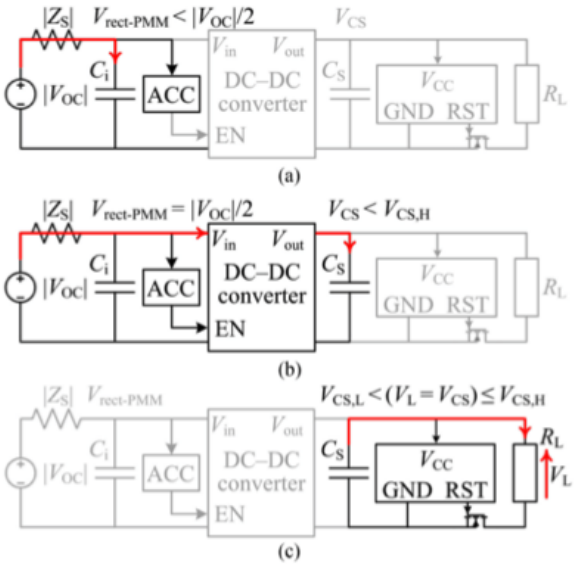

Figure 2.12: (a) Stage 1. (b) Stage 2. (c) Stage 3. (Chew, 2019).

Due to the simplicity of the proposed circuit, this approach achieved an overall efficiency of 78% in most scenarios and the power management circuit consumes only 5.16 µW while operating. However, the system does not consist of any voltage regulator. The output voltage is directly supplied from the storage capacitor in the system ranging from 2.0 V to 3.28 V.

Ferro, *et al*. (2019) presented a SoC solution for micro energy harvesting. Ferro and his co-author designed a power management unit fabricated in 0.18 µm CMOS technology including a 1mm^2 on chip solar cell as shown in Figure 2.13. The proposed micro energy harvesting system has a very small form-factor of 1.575 mm^2 and consists of an auxiliary charge pump to increase the voltage level to meet the requirement of the circuit. This implemented System on Chip manages the harvested energy intelligently. Moreover, the whole system is very light-weight, has a small form-factor, battery less, and self-sustainable. The highlight of this design is the PMU doesn't require any external kick off to start-up with a harvested power of 2.38 nW. Despite having a small form-factor, the design can handle an input ranging from nW to µW. The block diagram of the proposed power management unit is shown in Figure 2.14 below. The system consumes about 6.57 µW while operating and has an efficiency of 57%.

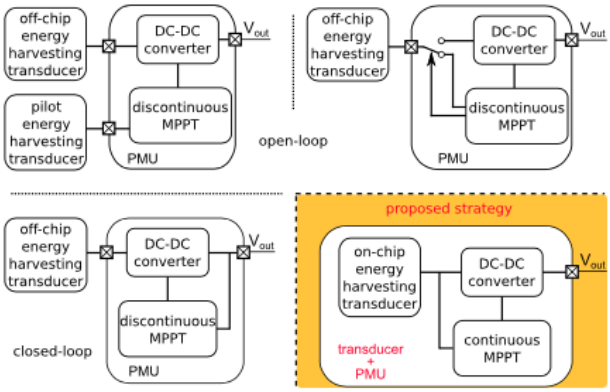

Figure 2.13: Traditional Energy Harvesting Strategy and the Proposed Strategy. (Bottom Right) (Ferro, et al. 2019).

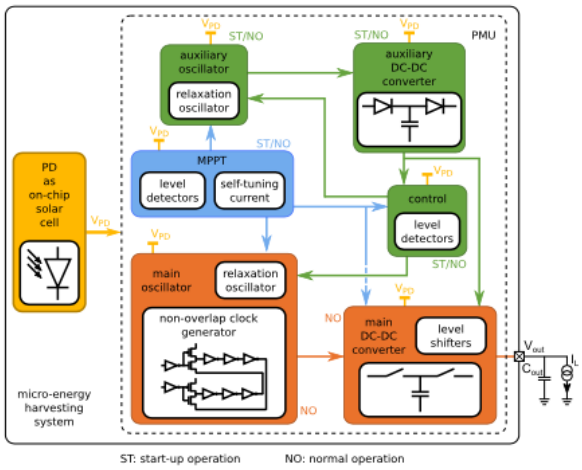

Figure 2.14: Block Diagram of the proposed PMU. (Ferro, et al., 2019).

On the other hand, Roy, *et al*. (2015) presented a batteryless integrated energy harvesting system (SoC) for physiological sensing on the body. The technology used in the design is 130 nm architecture. The designed SoC contains an integrated energy harvesting system, an extremely low-power RF full transceiver as well as a power management unit that powers several hardware. An integrated boost converter with maximum power point tracking control and a SIMO DC-DC regulator were implemented in the system to extract the maximum energy from the harvesting source before sending it to the SoC. The boost converter will charge the voltage to a higher level before it is stored in an external capacitor which then serves as the input to the SIMO regulator. The power management system is shown in Figure 2.15. The power management unit system claims to have an efficiency of 74.9% which can regulate output of 0.2 V to 0.35 V, 0.5 V, and 1.2V. The outputs will be

compared to a reference voltage. Once the voltage of VDD12 is less than the reference voltage, the peak inductor control circuit will then be activated to ramp up the inductor current and power the output via I_{LS}. The same mechanism occurs for VDD05 and VDD_var. At the point of V_X, a zero-detection comparator as in Figure 2.16 monitors the voltage and enables as soon as the voltage of V_X reaches a value lower than zero. For instance, when the V_X drops below zero, the comparator is enabled with 'EN' and 'OFF' is equal to '0', causing the LS in Figure 2.15 goes high. Opposingly, when the V_x reaches a value greater than 0 V, the comparator goes low to drive the LS low. With the effort to avoid higher static current consumed during comparison, the comparator designed in this work is duty-cycled by controlling the EN signal. The proposed system consumed 6.45 µW while operating and the overall system efficiency is 75%.

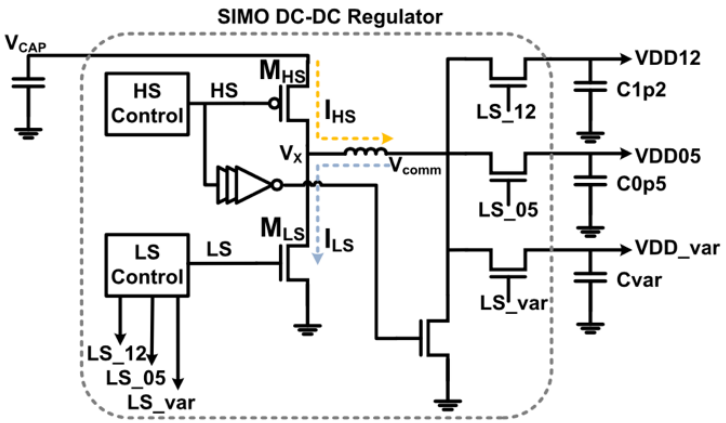

Figure 2.15: Power Management Circuit in the proposed system. (Roy, et al., 2015).

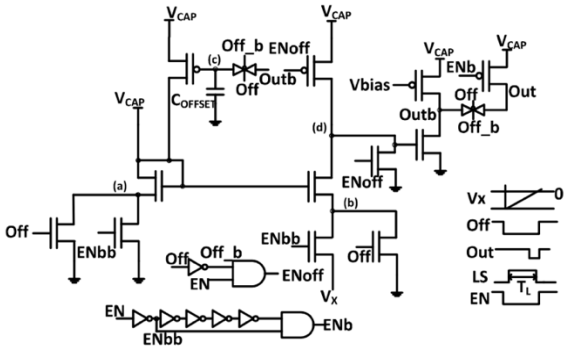

Figure 2.16: The Zero Detection Circuit. (Roy, et al., 2015).

In the work presented by Zhang, *et al*. (2013), they developed a baterryless energy harvesting body sensor node fabricated in 130nm CMOS technology. The power management system designed in the wireless sensor node is shown in Figure 2.17. The V_{BOOST} is the voltage rectified and boosted after it was generated by the harvesting module. In a condition where V_{BOOST} is decreasing, the System on Chip must switch its mode to a lower power consumption state to prevent node blackout until the harvested energy is abundant again. Therefore, a digital power management (DPM) was introduced into the SoC to control the node by monitoring the V_{BOOST} through the analogue-digital converter. The digital power management system will select the node to operate in 'stoplight' fashion based on the programmable digital threshold values by referring to the V_{CAP_DIG} value.

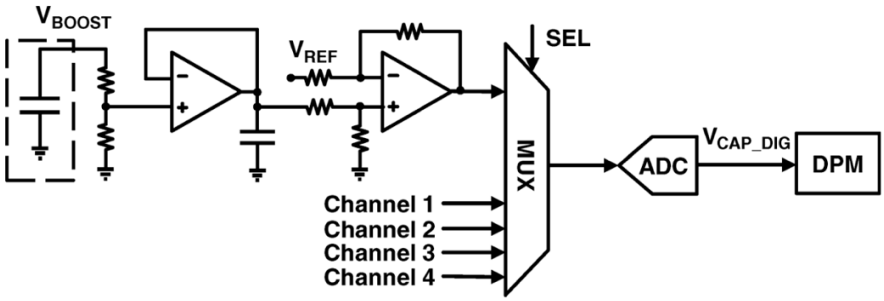

Figure 2.17: Power Management Circuit used in the system. (Zhang, et al., 2013).

Table 2.2: 'Stoplight' instruction of the DPM. (Zhang, et al., 2013).

	Inst. MEM	AFE	Data MEM	Accel. Blocks	Transmit
Red	On	Off	Off	Off	Off
Yellow	On	On	On	On	Duty Cycle
Green	On	On	On	On	On

The normal operation is green mode where the V_{BOOST} is greater than 1.3 V. When the V_{BOOST} value is between 1.1 V to 1.3 V, yellow mode will be enabled. Lastly when the V_{BOOST} drops below 1.1 V, red mode will be activated. This kind of power management solution is flexible as the programmer can set the mode threshold values for any possible transitions. However, the proposed solution consumes 19 μW and has a very low end-to-end efficiency at 38%.

In the previous work done by Shrivastava, *et al*. (2014), a single input multiple output energy harvesting system was designed and fabricated under the 130nm CMOS process technology. The proposed system can harvest energy from a solar cell with 0.38 V input voltage and power 4 outputs at 4 different voltage levels. It provides multiple output voltage at 1.2 V, 1.5 V, 3.3 V, and 5 V (for battery) by adapting the SIMO regulator. As the power generated by the harvesting system is not enough for the system to power for activities such as radio frequency transmission, the harvested energy will first be stored at an energy reservoir such as a capacitor. All converters in this designed system operate in a discontinuous conduction mode using a pulse frequency modulation scheme for higher efficiency at low power loads. All converters in the system generate two signals which are the "busy' and 'ready'. Enable signals (EN) will be generated by the digital controller depending on the priority based on the program to control the converter. The proposed system achieves an efficiency of 80% while delivering an output voltage of 1.2 V.

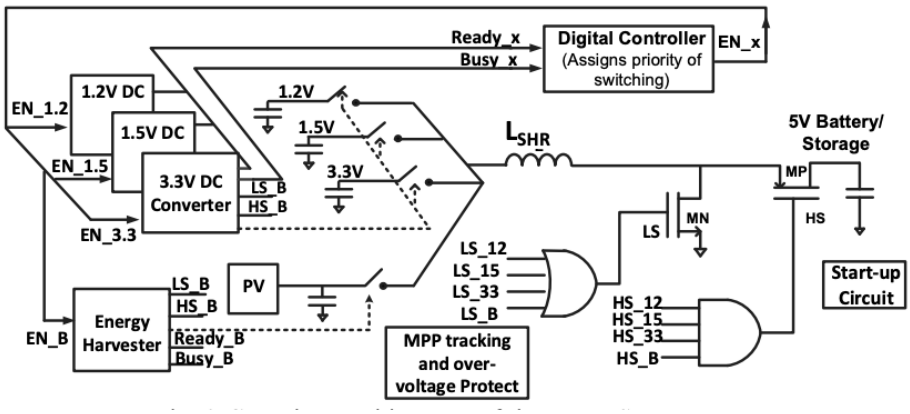

Figure 2.18: Block Diagram of the proposed system. (Shrivastava, et al. 2014).

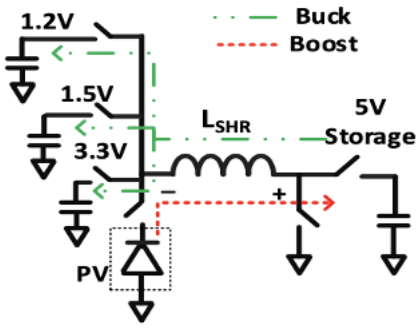

Figure 2.19: SIMO Structure of the system.

Mui, Khaw and Yasin (2020) presented a design methodology to make a dual input triple output power management circuit that manages the power harvested from radio frequency waves and piezoelectric harvester. In his approach, most of the parts of the system were analogue circuit such as rectifiers, voltage dividers, voltage regulators, PMOS, and NMOS switches. The only digital part in the proposed circuit was the power management unit as shown in the figure below.

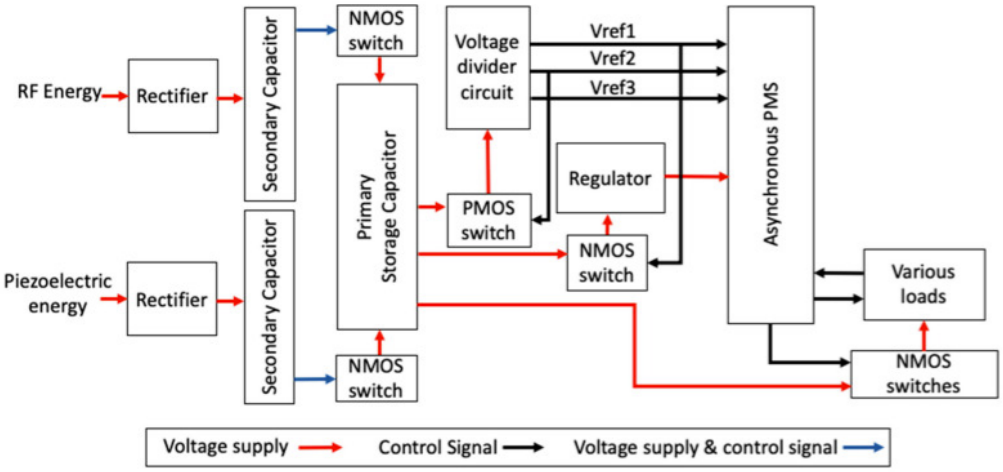

Figure 2.20: Block Diagram of the proposed circuit. (Mui, Khaw and Yasin, 2020).

The harvested energy will be rectified and stored in the secondary capacitor. Once the secondary storage capacitor is fully charged, the NMOS switch will transfer the energy to the primary storage capacitor. The voltage will be sent to the voltage divider, voltage regulator, and loads respectively. The voltage divider in the proposed system works as a reference to monitor the amount of voltage that is available at the primary storage. On the other hand, the voltage regulator supplies power to the power management system. The whole system used up only 12 μW during operation with an efficiency of up to 87.73%.

2.3.2 Summary of Previous work on PMU Design

Each of the proposed designs, especially their functionality was studied. The solution proposed by Shaltout, *et al*. (2016) was not very ideal since the size is bulky as it contains a battery. While in the work of Chew, *et al*. (2019), no voltage regulator was implemented in his design. Thus, the stability of the output might be affected. Ferro, *et al*. (2019) proposed a SoC approach for the wireless sensor node. However, the efficiency of the proposed PMU is achieving 57%. Table 2.3 below summarized all the proposed PMU studied in this paper.

Table 2.3: Summary of the studied proposed PMU.

Author		Shaltout (’16)	Chew (’19)	Ferro (’19)	Roy (’15)	Zhang (’13)	Shrivastava (’14)	Mui (’20)
Harvested Energy		Solar	PEH	Solar	TEG & Solar	RF & Solar	Solar	RF & PEH
Battery less		No	Yes	Yes	Yes	Yes	No	Yes
Integrated PMU		No	No	Yes	Yes	Yes	Yes	Yes
Technology (µm)		N/A	N/A	0.18	0.13	0.13	0.13	0.09
Number of Inputs		1	1	1	1	2	1	2
Number of Outputs		1	1	1	3	3	4	3
Power Management Unit	Circuitry	Mixed	Analog	Mixed	Mixed	Mixed	Mixed	Mostly Analog
	Architecture	DC-DC converter	Full-wave bridge rectifier, Analogue Control Circuit, DC-DC converter	MPPT, Charge Pump, DC-DC Converter	Boost Converter, SIMO DC-DC Regulator, Digital Power Management	Boost Converter, Rectifier, Digital Power Management	Boost Converter, Buck Converter, SIMO DC-DC Regulator	Rectifier, Voltage Divider Circuit, Voltage Regulator, Digital PMS
	Cold Start Circuit	N/A	N/A	@ 0.0024 µW	N/A	N/A	@ 0.38 µW	N/A
	Regulated Output Voltage (V)	5	2 – 3.28	N/A	0.5, 1.2, Variable	1.35 V	1.2, 1.5, 3.3, 5.0	N/A
	End-to-end Efficiency	0.7	0.76	0.57	0.75 @ 1.2V	0.38 @ 1.35 V	0.8 @ 1.2 V	0.87
	Power Consm. (µW)	N/A	5.16	6.57	6.45	19	N/A	12
Notes		The system is bulky	No voltage regulator used	Low PMU efficiency				

2.4 Wireless Sensor Nodes

The design of a wireless sensor network relies on the application and the environment, objectives, and system constraints (Yick, *et al*., 2008). However, there are many challenges in wireless sensor networks such as deployment, reliability, self-sustainability, maintenance, data processing, and energy consumption. Many research has been conducted to push the limit of the wireless sensor nodes' sustainability as the wireless sensor nodes are usually limited in power. To overcome this vital issue, some of them proposed new communication protocols, better storage schemes, and an operating system with higher efficiency.

Wireless sensors in railway monitoring have been widely studied and it has high potential to be used for long-term monitoring the health of the structure of railway. Nelson *et al.* developed a mechanical energy harvester that harvests energy from railway by a passing train to power the sensor nodes for railway structure monitoring. Chen *et al*. proposed a system that will only wake the measuring sensors when there is an approaching train detected. On the other hand, another similar approach used a strain gauge to sense any approaching train and wake the system if any changes are detected. A number of authors have developed many communication protocols in order to reduce the power consumption of the wireless sensor node.

However, commercial wireless sensor nodes are usually power-hungry as shown in Table 2.4 and powered by batteries that require battery replacement over certain periods. The commercially available wireless sensor nodes require an average power of up to 12 mW to operate, causing the battery to deplete even more rapidly. Furthermore, as the quantity of nodes in a wireless sensor network system gets higher, the maintenance and battery replacement of the wireless sensor network can be problematic and inconvenient since the locations of sensor nodes are usually hard to reach.

Table 2.4: Commercial wireless sensor nodes.

Operating Conditions	Manufactures		
	Intel IMote2	Waspmote	Jennic JN5139
Radio Standard	IEEE 802.15.4	IEEE 802.15.4/ Zigbee	IEEE 802.15.4/ Zigbee
Range (m)	30	500	1000
Voltage supply (V)	3.2	3.3	2.7 V ~ 3.6V
Average Power (mW)	12	1	3

Bradai, *et al.*, (2022) developed a wireless sensor node for predictive maintenance of a structure. The sensor node proposed contains a RF transceiver to transmit data and a SoC microcontroller. During active mode, the node will collect the vibration waveform and transmit it through the RF transmitter. Based on an experiment conducted in the study, the node consumes around 5 mA while measuring the vibration information and approximately 20 mA while sending the data to the base station.

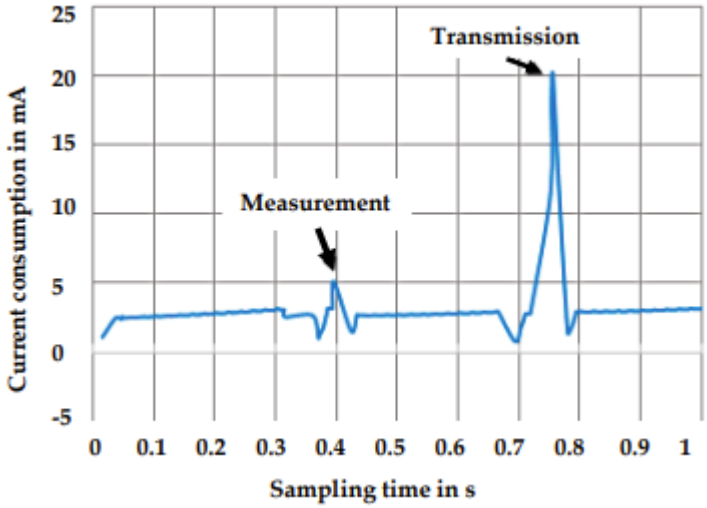

Figure 2.21: Current consumption of the proposed sensor node.

2.5 Rectifiers

In an energy harvesting system, most of the delivered voltage is an alternating irregular current (AC) and not direct current (DC) that is suitable to feed the sensors. Thus, an electronic interface is extremely needed to allow a voltage compatibility between the energy harvester and the electric load. In piezoelectric energy harvester systems (PEHs), the rectification stage often contains an AC-DC converter to rectify the voltage into a usable voltage to power up the loads. Therefore, the rectifier is a very important part to generate a stable DC power required with an appropriate voltage level which is needed by the target devices. The rectified DC output voltage levels highly depend on the rectifier design. The prime challenges in the design of the rectifier in the recent studies is on the percentage conversion efficiency (PCE). The higher the PCE rate, the higher the efficiency of the rectifier.

Conventional rectifiers use a Dickson's circuit or known as differential drive rectifier which usually suffers from efficiency drop because of the turn-on voltage of the diode (Usami. M, 2007). This problem is magnified when this design is implemented in integrated circuits because an additional step is required to provide a Schottky diode which has a very low turn-on voltage (Dickson. J, 1976). There are many different topologies available for the differential drive rectifier.

You. K, (2011), implemented a simple yet high efficiency differential drive rectifier which contains a cross-coupled charge pump to boost the low input DC voltages. He claimed that the proposed structure has advantages in low reverse leakage current and voltage drop across the MOSFET diode. Figure 2.22 and Figure 2.23 shows the schematic diagram of the proposed n-stage differential drive rectifier as well as the cross-coupled charge pump circuit.

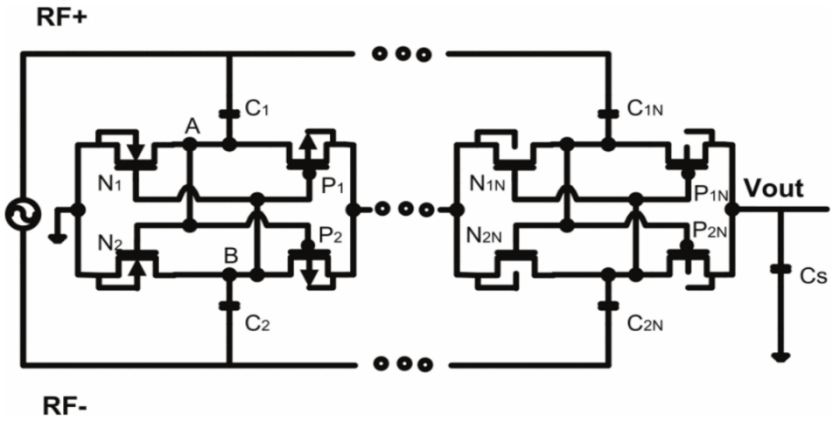

Figure 2.22: Schematic diagram of a n-stage differential drive rectifier.

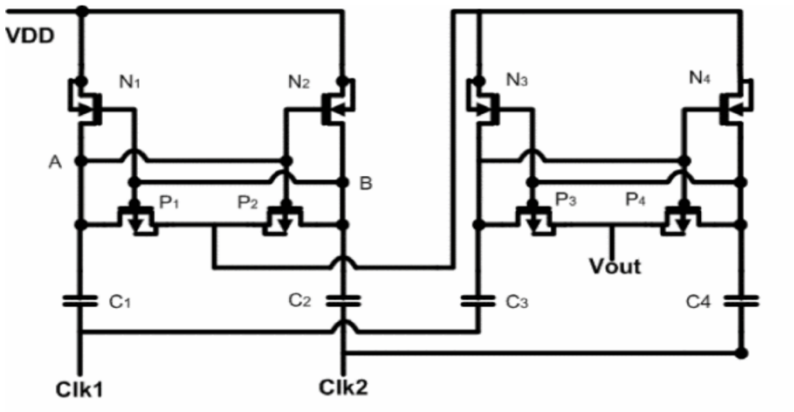

Figure 2.23: Schematic diagram of the Cross-coupled Charge Pump.

The proposed design consists of a differential drive rectifier and a cross-coupled charge pump with a clock generator to increase the voltage generated. The system was fabricated in a 0.13 μm CMOS process. In his proposed design, with an input power of 0.25mW, the converter can output a stable voltage at 2.05 V with a load of 100 KΩ. The highest efficiency of the converter system is about 74%.

On the other hand, Pratim. M and Kumar. K (2018) designed a TG based high frequency rectifier and fabricated it in a 45 nm CMOS process. The proposed design is actually a modified version of the charge pump aforementioned with the use of a transmission gate to produce a higher output power. The working principle is simple as the NMOS pass transistor can pass the negative voltage effectively with lesser propagation time while the PMOS

pass transistor can pass the positive voltage effectively. Thus, transmission can be a good solution as when the circuit is subjected to encounter with both the voltage levels. Figure 2.24 below shows the schematic diagram of the proposed TG based rectifier. The designed rectifier achieved PCE at 80% at -2dBm while the PCE is 40% at -5dBm in single stage realization. However, when the input power decreases, the power loss in the converter becomes significantly higher due to the leakage current issue.

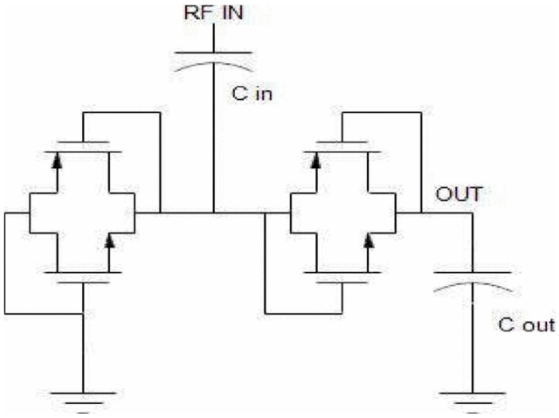

Figure 2.24: Schematic diagram of the proposed TG Rectifier design.

Mohd, A. (2018) proposed a multi-stage NMOS rectifier to convert the AC signal into a usable DC signal. Figure below shows the proposed multilevel NMOS rectifier. Every stage in the circuit consists of two NMOS transistors, a coupling capacitor as well as a multiplying capacitor. The proposed rectifier converts the AC input in both positive and negative cycles. At first, when the AC signal is in the negative cycle, the V_{DS} of the NM1 is in the negative region making it reverse biased and thus it is turned off. On the other hand, the NM2 transistor is in one state while it is forward biased. This will result in the current going through NM2 to charge the capacitor. According to Mohd. A. (2018), by cascading more stages of the NMOS rectifier, a higher DC output voltage can be obtained. However, as more stages are implemented in this design, the power loss will become higher due to the power loss of the diodes.

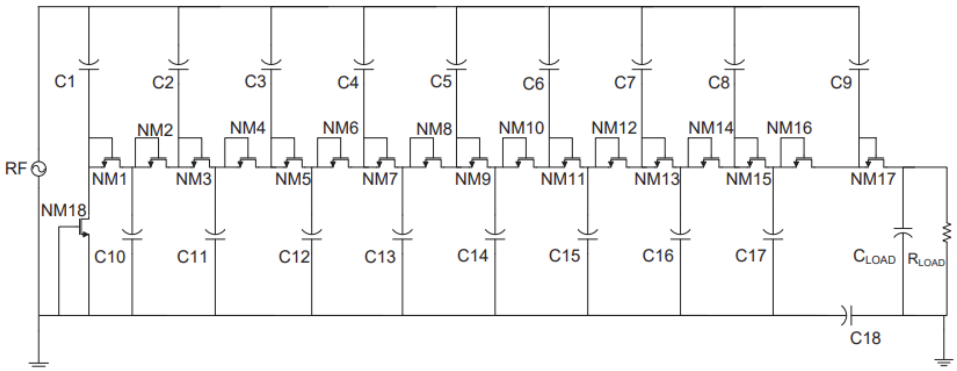

Figure 2.25: Schematic diagram of the proposed n-stage RF to DC rectifier.

In a nutshell, rectifiers, as one of the important blocks of the energy harvesting system, there are many different approaches to design a rectifier. The key to design a good rectifier for an energy harvesting system is to design based on the specification required such as the type and level of the input voltage. The conventional differential drive rectifiers are very mature technology and have a simple design while offering higher PCE. However, the implementation of Schottky diode in standard CMOS processes is hard as well. The main problem of the conventional design is the finite threshold voltage of the transistors. This is a very vital issue especially for ultra-low power operation where the input signal is smaller than the threshold voltage of the devices.

2.6 Buck Converter

Buck converter is a kind of switching mode power supply which is commonly used for stepping-down the DC voltage level. The buck converter also known as DC-to-DC power converter which steps down the input voltage to a desired output voltage level. In a conventional buck converter, switch controller block and power block are the two main parts of its circuit. There are two main types of method to control switching which are Voltage Mode Control (VCM) and Continuous Conduction Mode (CMC) (Marian. K, n.d.). Both of them can be implemented with Pulse Width Modulation (PWM) as well as the Pulse Frequency Modulation (PFM) depending on the application. The details and differences among VCM and CMC as well as the control technique such as PWM and PFM will be discussed in the following section.

2.6.1 Voltage Mode Control (VMC) vs Current Mode Control (CMC)

In order to regulate the buck converter's output voltage, there are two main types of feedback control loop topologies which are voltage mode control and current control mode respectively. The voltage control mode consists of only one feedback loop which is called voltage control loop. This kind of mode is named due to the duty cycle being directly controlled by voltage reference and feedback voltage from the output. The architecture of a VMC buck converter is illustrated in the following Figure 2.26.

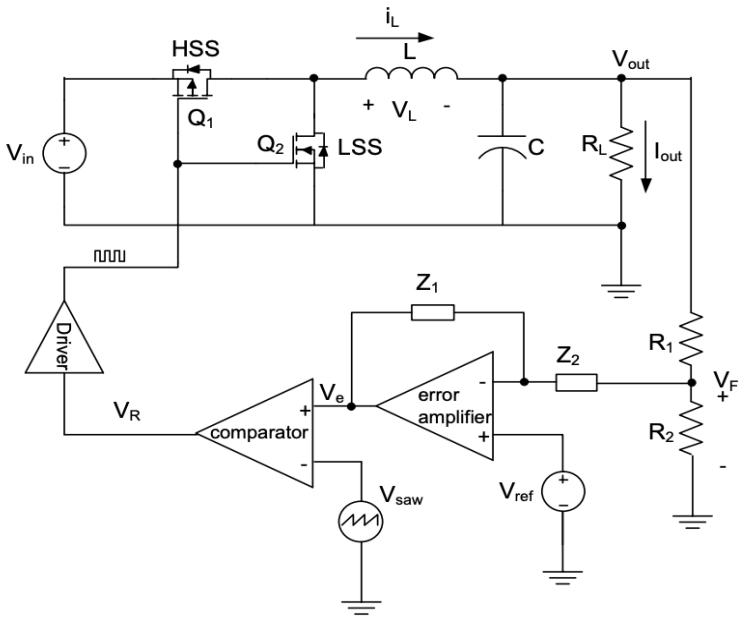

Figure 2.26: PWM buck converter with VCM technique.

On the other hand, the CMC consists of 2 feedback loops which are internal feedback loop and external feedback loop. The internal feedback loop is called a current loop which responds and controls the peak current of the inductor. The external loop is called a voltage loop which regulates the output voltage. The working principle of CMC is the internal current loop monitor and responds to the inductor current by adjusting the duty cycle. While the external voltage loop provides a reference voltage for the internal current loop every time there is a change in the output voltage. These two processes will keep repeating until a certain point where the output voltage is stabilized and regulated.

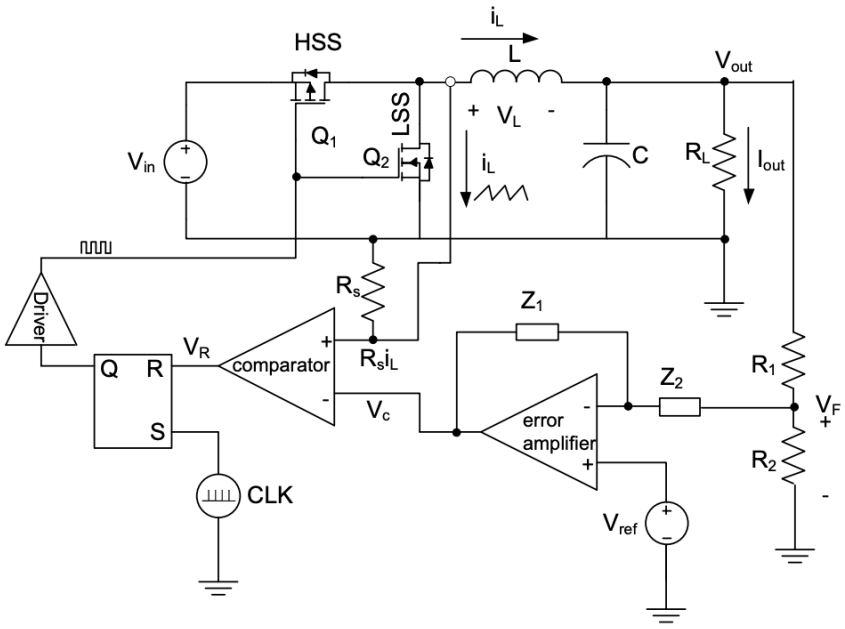

Figure 2.27: PWM buck converter with CMC technique.

In a nutshell, both of the control modes have their advantages and disadvantages. The CMC can provide a better stability and as the phase margin can be compensated with just a type 2 compensation circuit. For the VCM, a type 3 compensator is required in order to improve the phase margin of the buck converter. However, the power loss in CMC technique is relatively higher due to the extra current loop that makes the complexity of the system increase.

2.6.2 Pulse Width Modulation vs Pulse Frequency Modulation

Pulse width modulation (PWM) is a method of reducing the average power delivered by changing the timing of how long it stays on and off. The PWM waveform varies according to the output power desired (Lee. M and Chen. Y, 2017). For instance, the figure below illustrates the PWM signal with different duty cycle. The duty cycle in PWM means the percentage ratio of how long it turns on compared to when it is turned off.

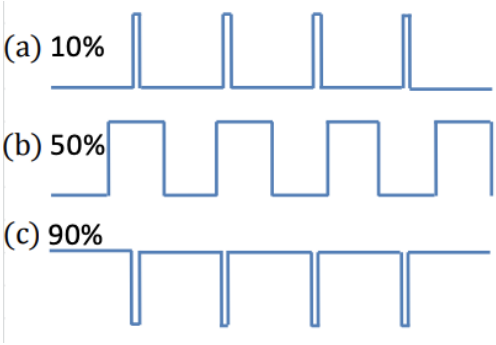

Figure 2.28: Duty cycle with: (a)10%, (b) 50%, (c) 90%.

On the other hand, the pulse frequency modulation is a control method that is somehow similar to the PWM aforementioned. The major difference between them is the PFM employs constant time variable frequency instead of fixed frequency pulses to control the output power supplied to the load. The following figure depicts the PFM for different levels of current.

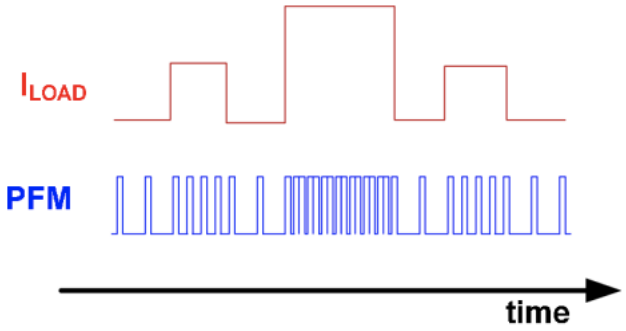

Figure 2.29: PFM Waveform.

In general, PWM control technique is proven to be more efficient especially for high output power where the duty cycle is longer. The efficiency of PWM will reduce drastically when this technique is used for low output power application due to the switching loss. The PFM controlling circuit is more

complex if compared to PWM technique due to its high electromagnetic interface. Thus, PWM control technique is often preferred over the PFM control technique (Vijayaraghavan. G, 2009).

2.6.3 Previous work onn Buck Converter

An open loop buck converter that is controlled by using pulse width modulation is shown in the Figure 2.30 below. The PWM signals will control the switch S1 and switch S2 to turn on and off. The output voltage will become the same as the input voltage when the switch S1 is closed. On the other hand, the output voltage will become 0 when the switch S1 is opened. By using the similar concept, the average output voltage can be controlled by adjusting the on period of both of the switches. However, in an open loop buck converter design, the output is not maintained at constant as there is no feedback circuit in the design. Thus, as the generated output voltage is not continuously measured and fed into the control circuit, the buck converter without feedback can be improved by adding a feedback part which is very crucial in stabilizing the generated output voltage whenever the load resistance changes (Sudarshan, *et. al*, 2018).

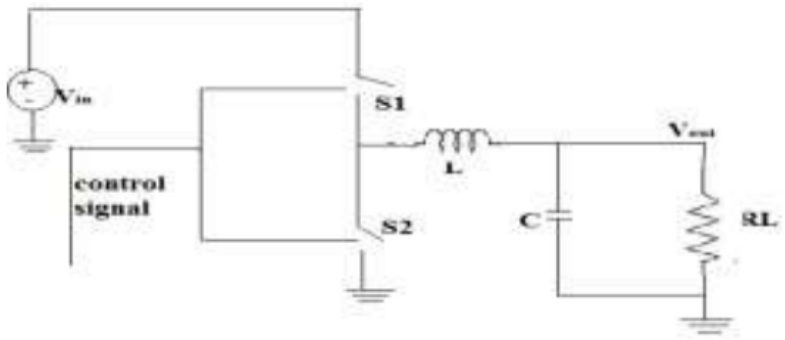

Figure 2.30: Open-loop buck converter.

Lu, *et al*., (2010) developed a voltage mode control buck converter using PWM techniques with 0.18μm CMOS technology. The proposed buck converter works with a digital error amplifier which allows a lower input voltage than other conventional buck converters. The design is claimed to have an efficiency of 90% at certain conditions where the input voltage is 1V and the generated output voltage is 0.5V. Figure below illustrates a simplified structure of the proposed voltage mode control buck converter.

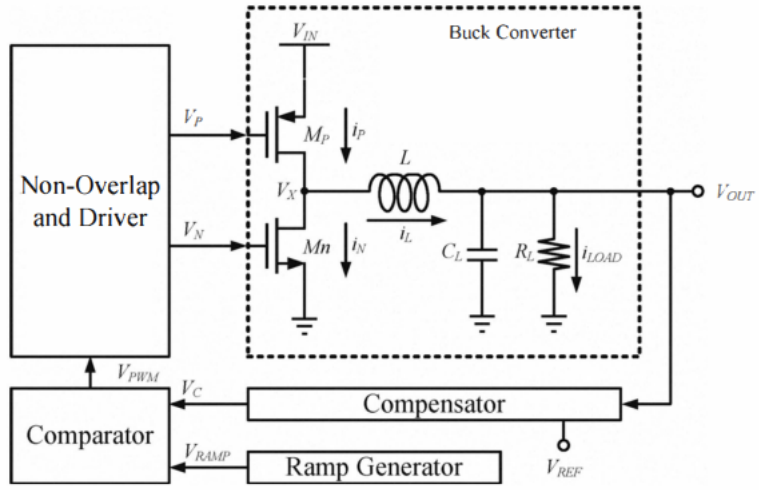

Figure 2.31: Schematic diagram of Voltage Mode Control Buck Converter.

The circuitry for PWM control buck converter includes a compensator, a comparator and a ramp generator. The working principle of closed-loop buck converter above is relatively simple. The PMOS and NMOS transistors act as a switch respectively while the inductor and capacitor work as a filter. The output signal of V_{PWM} is to control the PMOS and NMOS to turn on and off according to the condition. While the PMOS conducts, the current is equal to the inductor current. The current will keep increases according to the inductor value and output voltage signal. The ramp generator generates ramp signal and the comparator will compare it to the control voltage, $V_{C.}$ The comparator will output a high signal if the ramp signal is higher than the control voltage. If the voltage generated from the comparator is high, it will turn off the PMOS and turn on the NMOS. By using the similar concepts, the switch will keep on and off stepping down the input voltage to a desired output voltage.

To further improve the efficiency of the PWM controlled buck converter, Prateek, et al. (2014) proposed to reduce the large area overhead induced by the conventional spiral inductors in the buck converter. She proposed to replace the conventional spiral inductor with through-silicon-vias (TSV) inductors in buck converter with PWM feedback. The efficiency and the area overhead were investigated in this study. The buck converter was simulated in 45nm technology in Cadence Virtuoso. They found out that there is almost no huge

difference in terms of efficiency among the two different inductors when the output range is in 0 V to 600 mA. However, the inductor area has been reduced by 4 times making the whole area smaller.

CHAPTER 3

METHODOLOGY AND WORK PLAN

3.1 System Specifications

The study aims to develop a power management integrated circuit to manage the power harvested to power the wireless sensor node effectively. The methodology of this study includes only the design of PMU and will not cover the components design of the energy harvesting unit and the wireless sensor node.

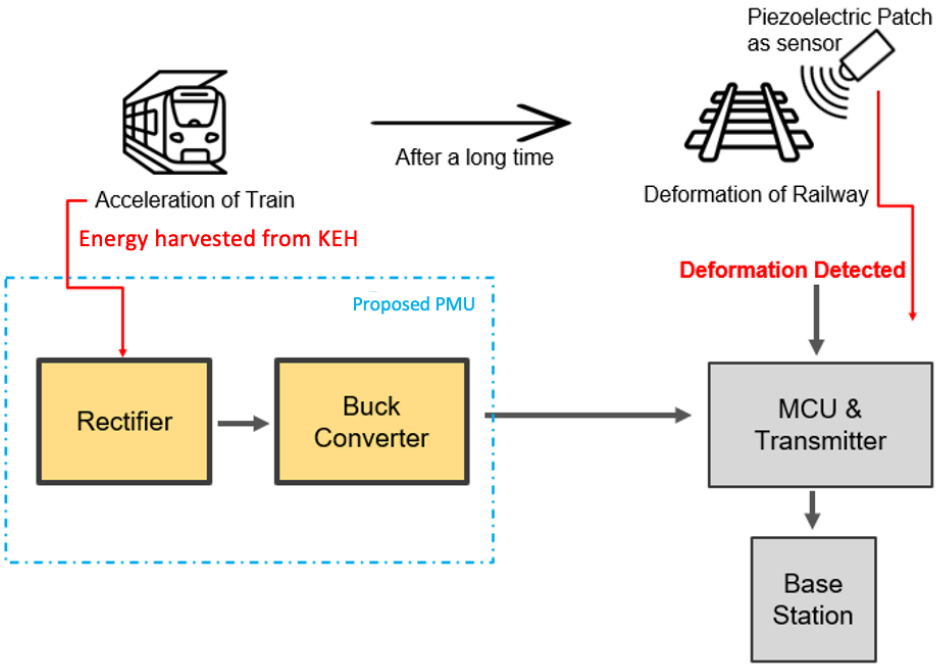

Figure 3.1: Proposed wireless sensor system.

The Figure 3.1 above shows the proposed solution to monitor the health structure of the railway. Whenever a train passes, the voltage generated by the kinetic electromagnetic energy harvester will be regulated by the proposed PMU before feed into the microcontroller. The deformation of the railway will be detected by the piezoelectric patch which acts as a sensor in this system. However, the piezoelectric patch does not require any power to work. Therefore, the load in this configuration will be just the microcontroller and the transmitter.

Among all of the types of energy harvester discussed in Chapter 2, kinetic energy harvesting solutions are promising as they are capable of providing sufficient energy by generating kinetic energy from vibrations from the passing train into electricity. Therefore, an energy harvester that harvests electromagnetic energy from passing trains designed by Hadas. Z, et al, (2021) was adopted in this study. In the study conducted by him, he simulated that the developed electromagnetic kinetic energy harvester can harvest up to an average of 29.3 mW. Several peaks above 600 mW were obtained in the simulation. The voltage waveform generated is shown in the figure below.

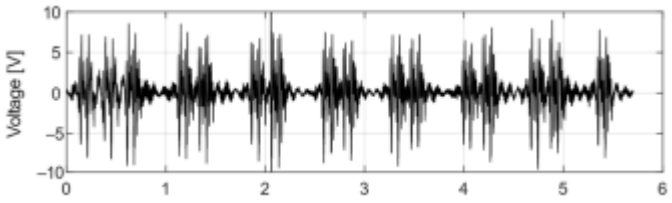

Figure 3.2: Voltage generated from the KEH source.

The hardware specification of the wireless sensor node is described in the following table.

Table 3.1: Specification of the wireless sensor loads.

Components	**Values**
MCU	MSP430 + CC1101
Operating Input Voltage	$3\ V - 3.3V$
ADC	12 bits
Operating Frequency	$86\ MHz$
Current drain	Active mode: 160 $\mu A\ /Mhz$ Standby mode: 2.0 μA Off-mode: 1.0 μA
Feature	Ultra-Low Power Consumption

3.2 Design Methodology

The PMU design in this study will be developed by using Cadence Virtuoso EDA Tool provided. The circuit will be designed using the GPDK 045 library with a 45 nm CMOS technology library. The Cadence Virtuoso custom design platform allows users to design all logic cells and layout manually. Therefore, due to high optimization capability of custom design, it is believed that custom design can have a better performance than Application Specific Integrated Circuit (ASIC) design. The Cadence Virtuoso IC design platform allows the proposed PMU design to achieve a lower power dissipation and higher custom design flexibility. In general, the Cadence Virtuoso is a good tool to develop custom design as it provides a user-friendly environment and functionality to drive simulation from a schematic. It also can detect errors in design while simulating analysis and it provides a debugging function as well.

3.3 Work Plan

The project can be separated into two parts where the first part of this project or known as 'FYP 1" is carried out in May 2021 to September 2021 with a duration of 13 weeks. After that, the second part of the project was carried out in the January semester of 2022, approximately 13 weeks of duration. The flow chart of this project is described in Table 3.2.

In the first part of the project, FYP 1, the focus is on studying different types of available energy harvesting technology and the block diagrams of PMUs. Due to the nature of energy harvesting where the power harvested usually is limited to micron watts, the PMIU for this application becomes very drastically crucial. In FYP 1, majority of the time were spent on research and information gathering for the literature review. Different types of energy harvesting method were analysed and studied. They were compared with each other in terms of their advantages and disadvantages such as availability, power generated, reliability, cost and their drawbacks. After that, some recent works on PMU for low power devices were studied as well to understand the design methodology of the PMIU. The design of some block designs such as rectifier, boost converter, buck converter, and low-dropout regulator were studied and tested for the suitability to be implemented in the proposed PMIU. Among the designs studied some of them were chosen to implement in the proposed design

and some of them were chosen for comparison against the proposed design. In order to familiarise and adapt to the Mentor Graphics EDA tool (Silterra 0.13-µm CMOS process). However, in the midst of the project, the license of the Mentor Graphics EDA tool expired and it was replaced by Cadence Virtuoso (GPDK 45nm CMOS process).

On the other hand, in the second part of the project, the signal waveform generated by the piezoelectric energy harvester was simulated by using PWL source in Cadence Virtuoso. After that, the block designs such as rectifier and buck-converter were designed and constructed. Each of the block diagrams was broken down into some smaller parts in order to make it easier to manage and design. Each of the independent blocks was constructed, simulated and analysed independently. Lastly, the results were analysed, compared and discussed after obtaining satisfying results. Table 3.2 and Table 3.3 shows the Gantt Chart for the first part and second part of the project. A simplified flow chart that highlights workflow of Part 1 and Part 2 is included in Figure 3.3 as well.

Table 3.2: Work plan for FYP Part 1.

No.	Project Activities	W1	W2	W3	W4	W5	W6	W7	W8	W9	W10	W11	W12	W13	W14
M1	Project Planning														
M2	Problem and Objective Defining														
M3	Literature Review														
M4	Progress Report Preparation														
M5	Oral Presentation														

Table 3.3: Work plan for FYP 2.

No.	Project Activities	W1	W2	W3	W4	W5	W6	W7	W8	W9	W10	W11	W12	W13	W14
M1	Study on the PMU components														
M2	Design Components that used in PMU														
M3	Familiarizing Mentor Graphics														
M4	Modelling the Harvested Energy														
M5	Build and the designed PMU														
M6	Verify the PMU to work														
M7	Simulation and Result Analysis														
M8	Improvements on the PMU														
M9	Report and Poster Preparation														
M10	Oral Presentation Preparation														

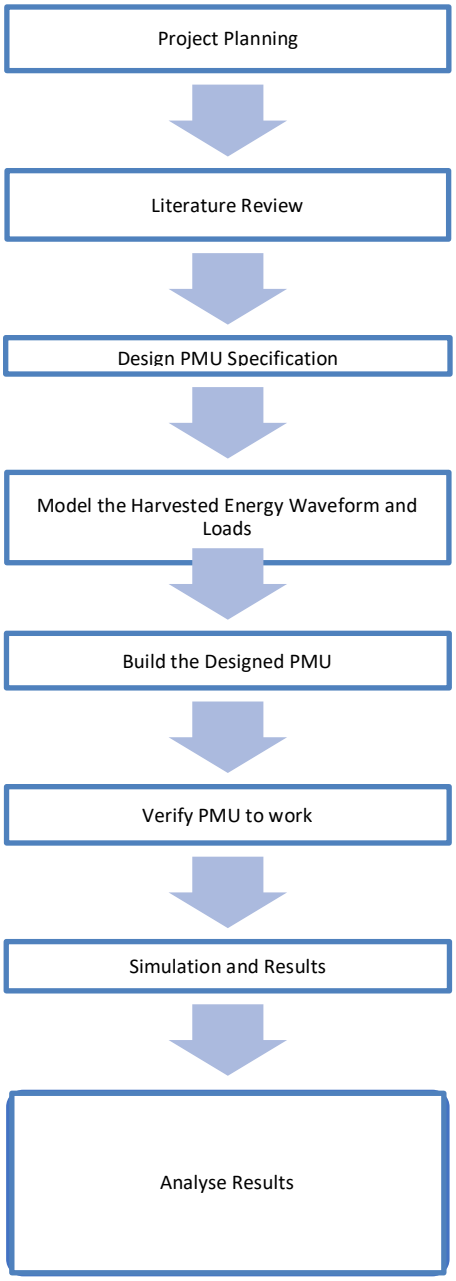

Figure 3.3: Flowchart of Project Planning (Combining Part 1 and 2).

3.4 Proposed PMU Design

The block diagram of the proposed system is shown in Figure 3.4. All the modules from the input sources to the output loads are shown below. The input sources is electromagnetic electric energy. The harvested energy will then be rectified first by the rectifier. After that, the rectified voltage is too high to feed into the load. It must be stepped down before feeding into the loads. A PWM voltage control mode buck converter is required to step down the voltage level to 3.3V. Any deformation detected from the railway can be expressed in the form of voltage waveform and the ADC will converts the signal into digital signal before the transmitter send the signal to the nearest base station.

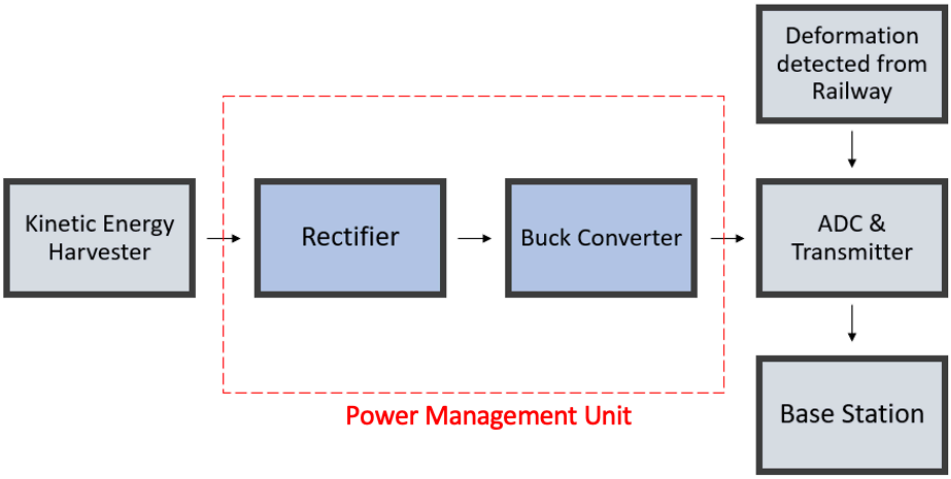

Figure 3.4: Block Diagram of the Proposed System.

To make sure the voltage level harvested by the harvesting unit is sufficient, the PMU should not consume too much power and the power losses must be kept at minimum. Besides, the design of rectifier and buck regulator will be further studied for improvement of the system

3.5 Proposed Rectifier Design

A conventional differential drive rectifier was selected in the design of the rectifier due to its simplicity and high-power conversion efficiency (PCE). The issues of conventional differential drive rectifiers based on Schottky diodes where the on resistance is relatively small can be avoided by implementing multistage configurations (Mahmoud. M, 2016). Therefore, in order to achieve a smaller turn-on voltage, the diode connected MOS transistor is applied. In this design, the average power generated from the mechanical vibration in rails is relatively high. Thus, a conventional differential drive rectifier as shown in the figure below is safe to use in this application.

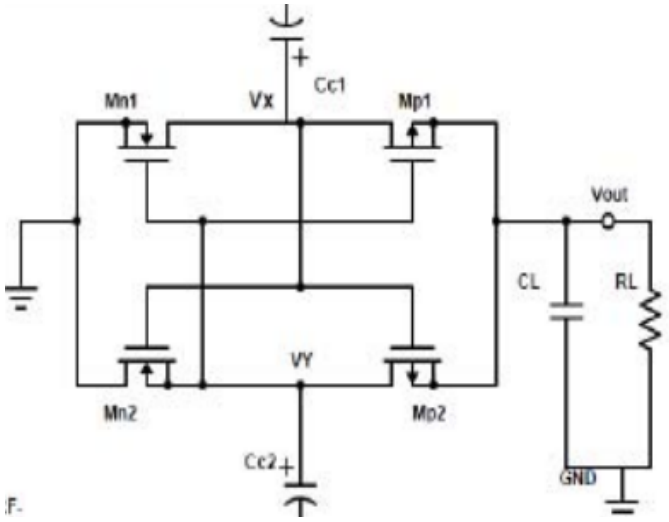

Figure 3.5: Single stage Conventional Rectifier.

The figure above shows the schematic diagram of a single stage differential drive rectifier. The positive and negative input will first go through capacitor Cc1 and Cc2, which act as fly capacitors. While on the other hand the CL is load capacitor and RL is the load resistance. The rectifier also acts as a voltage multiplier. As observed in Figure 3.5, the converter consists of 2 cross-coupled CMOS rectifiers. While one is in forward conduction mode, the other one is in reverse conduction mode in a half cycle. For the next half cycle, the conduction modes reverses and the rectifier now is in the charging phase where the capacitor was charged. The stored charge is delivered to the load while it is in the discharging phase (Chouhan. S, 2016).

The various parameters such as circuit designs, W/L ratio of transistors, input and output loading will affect the power conversion efficiency (PCE) of a converter. The L value for NMOS and PMOS transistors were selected at the minimum length of the technology which are 45nm. According to Lawrence. L and Antony. K (2017), the best-balanced ratio for the NMOS and PMOS for rectifier operation will be 5. Therefore, the W/L ratio of NMOS and PMOS were selected as 5. Thus, the width of the NMOS will be 120nm and for the PMOS will be 600nm. The differential drive rectifier will be constructed in 45nm technology. The Table 3.4 below shows the values selected for each element in the circuit.

Table 3.4: Parameters for the Components in the proposed Rectifier.

Parameters	**Designed Differential Drive Rectifier**
V_{in}	V_{Piezo}
W_p (nm)	120
W_n (nm)	600
L	45
C_{c1} (nf)	5
C_{c2} (nf)	5
R_L (K)	1000
C_L (nf)	5

3.6 Proposed Buck Converter Design

Many factors need to be taken into consideration while designing a buck converter such as power conversion rate, settling time, output voltage ripples. The design of the buck converter such as the specification of the buck converter, proposed schematic diagram of the buck converter, and the parameters of the buck converter will be discussed in the following sections. The specifications of the desired buck converter were listed in the following table.

Table 3.5: Specification of the designed Buck converter.

CMOS Technology (nm)	45
Input voltage (V)	6.75
Output voltage (V)	3.3
Input Power (mW)	45
Efficiency (min)	> 60%
Output capacitor ESR (mΩ)	75
Inductor DCR (mΩ)	50

In this study, the buck converter proposed is used for low power application in the range of milli-watt. Designing unnecessary blocks and circuits in the feedback loop of the buck converter can cause the converter to consume too much energy. Thus, the strategy is to keep the design of the buck converter simple, so that a higher efficiency of the converter can be achieved. Therefore, in this study, voltage mode control approach is preferred over the current control mode due to its simplicity yet efficiency to ensure the overall performance of the buck converter in its best condition.

PWM control technique is widely used as it provides high stability and yet is simple to implement. In a buck converter with PWM control technique, the converter is working at a fixed frequency, and the duty cycle is adjusted according to the desired output voltage. The voltage error is amplified through an error amplifier. The comparator will compare the error voltage and the ramp voltage to generate a square wave output at the designed operating frequency and duty cycle (Mok. P, 2007). When the output voltage is above the reference voltage, the duty cycle of the converter will be adjusted to a shorter period so

that the NMOS switches will be conducting longer. Similarly, when the output voltage is below the reference voltage, the duty cycle will be lengthened in order to make the PMOS switches to conduct longer. The PWM control technique is often implemented in buck converters as it is an effective control method which can improve the efficiency of the buck converter by monitoring the output voltage. The figure below shows the proposed design of the buck converter schematic diagram.

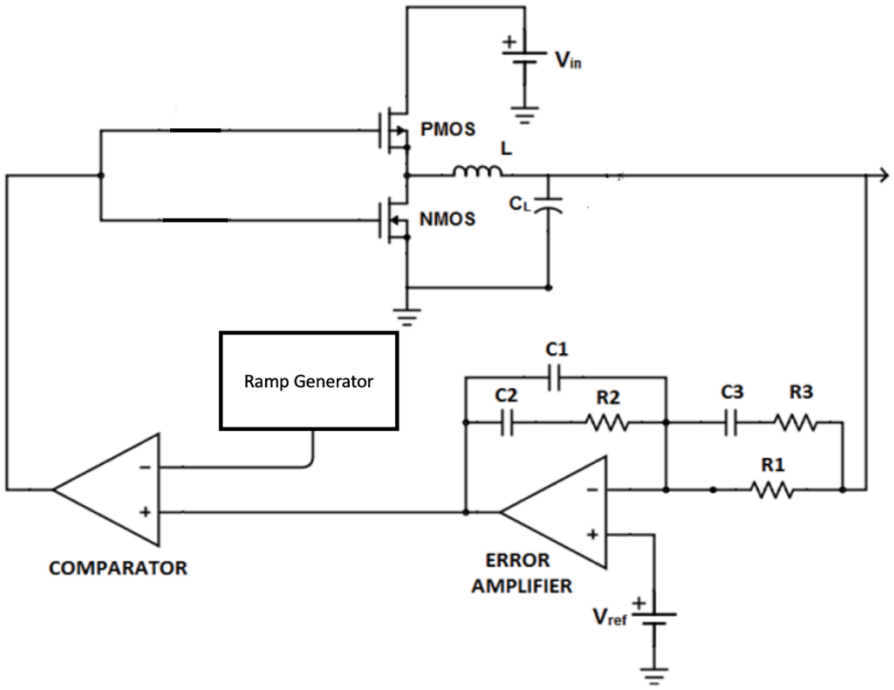

Figure 3.6: Schematic Diagram of Proposed Buck Converter.

In order to reduce the area of the chip as much as possible, the transistor sizing used is downsized. PMOS transistors and NMOS transistors were sized 6 µm and 2.9 µm respectively. The switching frequency of this buck converter was chosen as 20 MHz to reduce the size of the filter which are mainly contributed from inductor and capacitor. A faster transient response can be obtained by simply increasing the switching frequency of the converter. However, higher switching frequency will head to lower efficiency of the buck converter as the switching loss increases as well. Thus, in order to meet the buck converter's specification, an operational switching frequency of 20 MHz is chosen.

3.6.1 Sizing of Inductor and Capacitor

The inductor and capacitor in a buck converter play an important role in providing stable current to the load whenever the PWM signal changes. They both act as a filter where the inductor will constantly switch at the same as the PWM signals. The inductor is responsible for superimposing some ripples on the current sent to the output. Thus, the sizing of the inductor and capacitor are important, and it needs to be chosen wisely in order for the buck converter to reach a better PCE.

- Inductor Sizing

  The inductor current can be obtained through Faraday's law.

$$V_L = L\frac{di_L}{dt} \tag{3.1}$$

  For $0 < t \leq D.t$, where V_i and V_o are input and output voltage respectively,

$$i_L = \frac{V_i - V_o}{L}t \tag{3.2}$$

  Thus, the peak current can be obtained as shown below.

$$\Delta i_L = i_L(DT) = \frac{V_i - V_o}{L}D.T = \frac{V_o\,(1-D)}{L\,(f_s)} \tag{3.3}$$

  The peak-to-peak ripple current of the inductor can be obtained:

$$\Delta i_{L(max)} = \frac{V_o\,(1-D_{min})}{L_{min}\,(f_s)} \tag{3.4}$$

  Where L_{min} is the minimum inductor size, f_s is the average output voltage, f_s is the switching frequency, D_{min} is the minimum duty cycle and $\Delta i_{L(max)}$ is the minimum inductor current.

Therefore, the minimum inductor value can be obtained through:

$$L_{min} = \frac{V_o\ (1 - D_{min})}{\Delta i_{L(max)}\ (f_s)} \tag{3.5}$$

Based on the design specification as aforementioned, we know that

$$V_{out} = 3.3\ V$$

$$V_{in} = 6.75\ V$$

$$D_{min} = \frac{V_{out}}{V_{in}} = \frac{3.3}{6.75} = 0.49$$

$$f_s = 20\ MHz$$

$$\Delta i_{L(max)} = 5\ mA$$

Therefore, by substituting the specifications stated above into the formula (3.5):

$$L_{min} = \frac{3.3\ (1 - 0.49)}{5m\ (20M)} = 16\ \mu H \tag{3.6}$$

From the equation above, the inductor size is inversely proportional with the switching frequency. As the switching frequency becomes higher, the size of the inductor becomes smaller. However, the power loss in the switches needs to be taken into consideration as the switching frequency becomes higher, the power loss will increase which will result in a noticeable drop of PCE of the converter. Thus, a good balance must be achieved in between these two parameters. The inductor size chosen is a bit larger as larger size of inductor can improve the efficiency of the converter. Therefore, the inductor size chosen is 20 µH.

- Capacitor Sizing

The capacitor in the buck converter is used to smooth out the output voltage ripple before feeding into the load. Figure below illustrates the voltage ripple waveform of the capacitor in a buck converter.

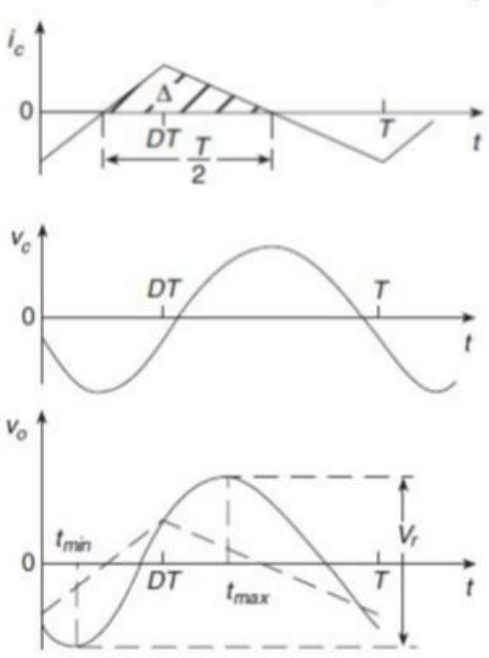

Figure 3.7: Voltage Ripple in the Capacitor.

According to Sudharshan, *et.al* (2018), the peak-to-peak ripple voltage of the capacitor in a buck converter can be obtained through:

$$V_{CPP} = \frac{\Delta i_{L(max)}}{8 f_s C} \tag{3.7}$$

By substituting the $\Delta i_{L(max)}$ with the equation expressed above,

$$V_{CPP} = \frac{V_o\ (1 - D_{min})}{8 f_s^2 LC} \tag{3.8}$$

Therefore, by setting the V_{CPP} as 0.1mV, the minimum size of the capacitor can be obtained through:

$$C_{min} = \frac{V_o\,(1-D_{min})}{8f_s^2 L V_{CPP}} = \frac{\Delta i_{L(max)}}{8f_s V_{CPP}} = \frac{5m}{8(20M)(0.1m)} = 0.3125\ \mu F \quad (3.9)$$

The capacitor is chosen as 0.33 µF.

The parameters chosen for the designed buck converter were summarised in the following table.

Table 3.6: Specifications of the calculated components.

Components	Values
L	$16\ \mu H$
C	$0.33\ \mu F$
f_s	$20\ MHz$

3.6.2 Type 3 Compensator Values

In order to make the buck converter to have enough phase margin to position the poles and zeros at the desired location, the components value of a type 3 compensator needs to be calculated (Lee. S, 2014).

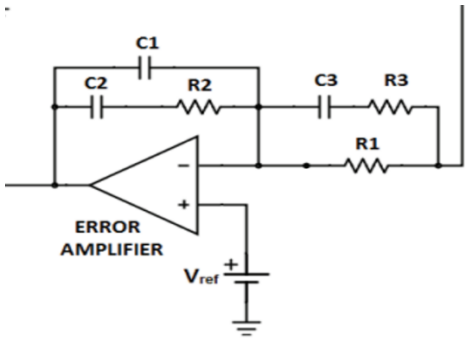

Figure 3.8: Type 3 Compensator used in the proposed design.

- According to Lee. S (2014), the equivalent series resistance zero frequency can be obtained through:

$$f_{ESR} = \frac{1}{2\pi(ESR)(C)} = \frac{1}{2\pi(75m)(0.33u)} = 6.43\ MHz \quad (3.10)$$

- The double pole frequency of the filter can be calculated as:

$$f_{LC} = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{(20u)(0.33)}} = 72\ kHz \quad (3.11)$$

- Assume that R_1 is equal to 2 kΩ and the desired bandwidth is equal to 30% of the switching frequency, 30% x 20 MHz = 6 MHz

- R_2, R_3, C_1, C_2, and C_3 can be obtained as below.

$$R_2 = \left(\frac{BW}{f_{LC}}\right)\left(\frac{\Delta V_{saw}}{V_{in}}\right)R_1 = \left(\frac{6M}{72K}\right)\left(\frac{0.5}{6.75}\right)(2K) = 12k\Omega \quad (3.12)$$

$$C_2 = \frac{1}{\pi(R_2)(f_{LC})} = \frac{1}{\pi(12K)(72k)} = 368\ pF \quad (3.13)$$

$$C_1 = \frac{1}{2\pi(R_2)(f_{ESR})} = \frac{1}{2\pi(12K)(6.43M)} = 2.06\ pF \quad (3.14)$$

$$R_3 = \frac{1}{(\frac{f_{SW}}{2f_{LC}})-1} = \frac{1}{(\frac{20M}{2(72k)})-1} = 14.5\ \Omega \quad (3.15)$$

$$C_3 = \frac{1}{\pi(R_3)(f_{SW})} = \frac{1}{\pi(14.5)(20M)} = 1097\ pF \quad (3.16)$$

Table 3.7: Specifications of calculated components.

Components	Values
R_1	$2\ k\Omega$
R_2	$12\ k\Omega$
R_3	$14.5\ \Omega$
C_1	$2.06\ pF$
C_2	$368\ pF$
C_3	$1097\ pF$

3.6.3 Error Amplifier and Comparator

A two-stage amplifier designed by Pancholi. S and Meena. R (2016) was selected and applied as an error amplifier and comparator in this study. The schematic diagram done in Cadence Virtuoso is shown in the Figure 3.9 below. The reference voltage is connected to one of the inputs of the error amplifier while the other one's input is connected to the feedback voltage from the buck converter's output. The error amplifier compares and amplifies the difference between the two inputs.

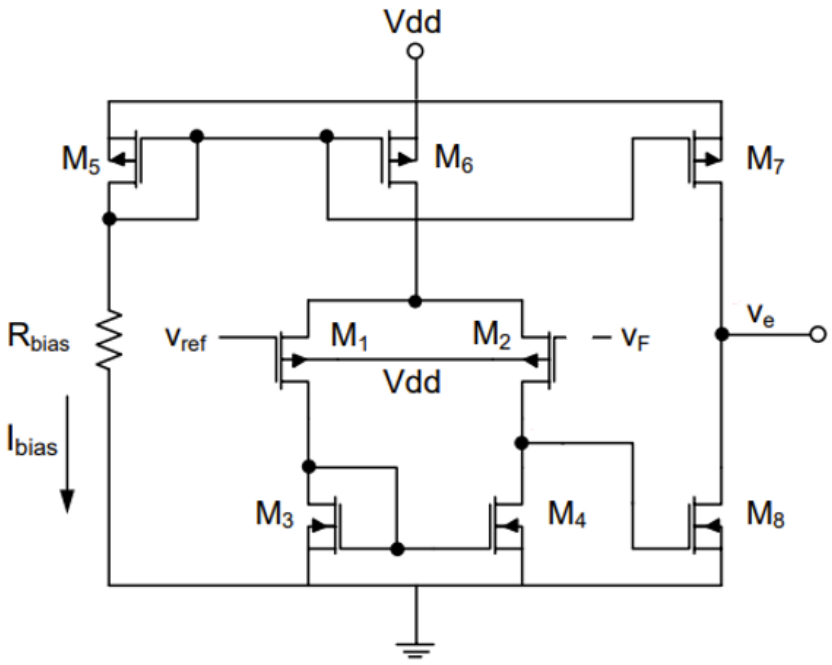

Figure 3.9: Schematic Diagram of the proposed Error Amplifier.

According to Pancholi. S and Meena. R (2016), in order to achieve high voltage gain, the M1, M2 and M8 were sized accordingly to improve the voltage regulation. High gain is important in an error amplifier as the difference between the both inputs must be kept at minimum (Brusev. T, *et.al.*, 2008). The ratio of width to length of the NMOS and PMOS transistors were selected wisely as the ratio increases, the output power will increase as well. The width-to-length ratio of the transistors were shown in the Table 3.8 below.

Table 3.8: W/L Ratio used in the amplifier design.

Transistors	W/L Ratio
M1	6
M2	6
M3	8
M4	8
M5	38
M6	38
M7	7
M8	7

3.6.4 Ramp Generator

The ramp generator in a buck converter plays an important role in switching control. The ramp generator was constructed using the piecewise linear voltage source in analoglib. The ramp generator was designed to have a lower voltage of 0 V and an upper voltage of 2 V. Besides, as the switching frequency selected for the buck converter is 20 MHz, by doing a simple calculation, $T = \frac{1}{f}$. The period of the ramp should be 50ns. The ramp generator was designed to have a period of 50 ns with a ramp rise time of 47.5 ns and a ramp fall time of 2.5 ns. The following figures illustrate the symbol of the generated ramp generator and its output waveform.

Figure 3.10: Symbol of the ramp generator.

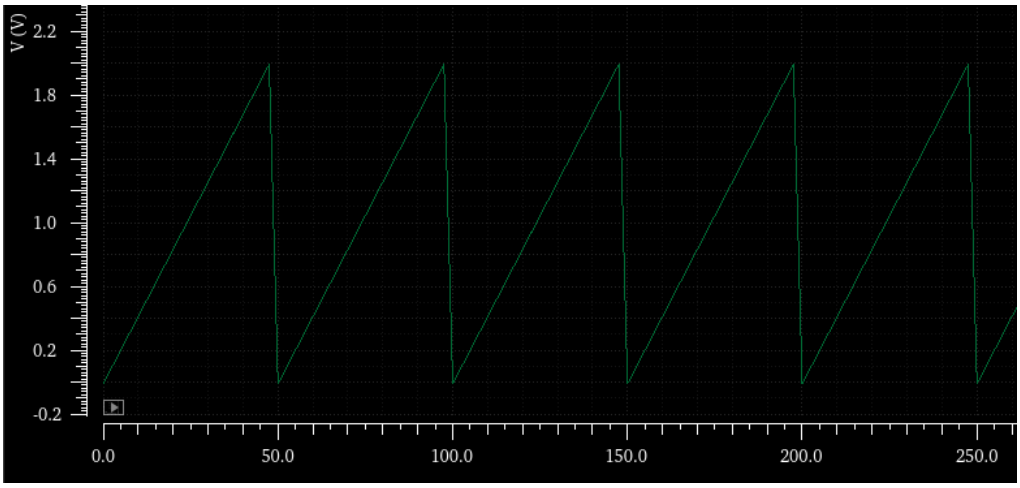

Figure 3.11: Ramp voltage generated by the ramp generator.

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Introduction

In this chapter, the performance of the design block will be analysed and discussed. The efficiency of rectifier and buck converter design in the previous chapter will be compared to other designs accordingly. The harvested electromagnetic kinetic energy by the energy harvester designed by Hadas. Z, et al, (2021) was modelled in Cadence Virtuoso using the piecewise linear voltage from analoglib. For the rectifier, the output voltage at different loads were simulated and analysed. The configuration with the highest output power was chosen. Furthermore, the number of stages of the rectifier was compared and the results were analysed. On the other hand, the ripple of the output voltage from the buck converter, the settling time, and the efficiency were analysed and discussed.

4.2 Diffrential Drive Rectifier

The harvested kinetic energy generated by the passing train is fed into the rectifier to turn into a usable DC voltage. The proposed rectifier is simulated in Cadence Virtuoso using 45nm Technology. The electromagnetic kinetic energy harvester developed by Hadas. Z, et al, (2021) was adopted in this study. The simulated input is shown in the Figure 4.1 below. The input of the proposed rectifier was connected to the energy harvester modelled using piecewise linear voltage source in Cadence Virtuoso.

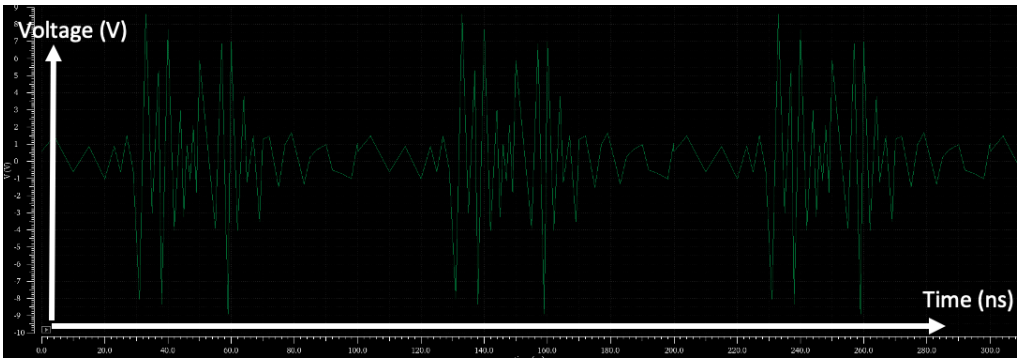

Figure 4.1: Simulated voltage harvested by a passing train at 110 km/h.

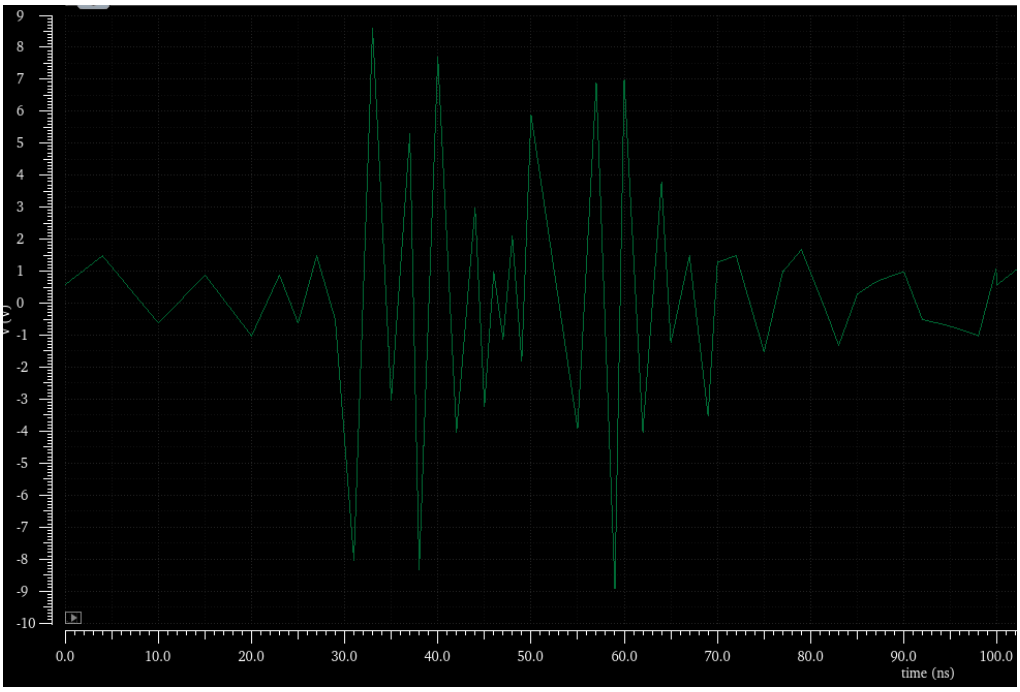

Figure 4.2: Closer look of the simulated voltage.

Figure 4.3 shows the schematic diagram of the proposed differential drive rectifier where its input is connected to the output of the simulated energy harvester. The output of the rectifier is connected to a smoothing capacitor to reduce the ripples of the output voltage. A load resistor was connected to the output of the rectifier to analyse the performance of the rectifier.

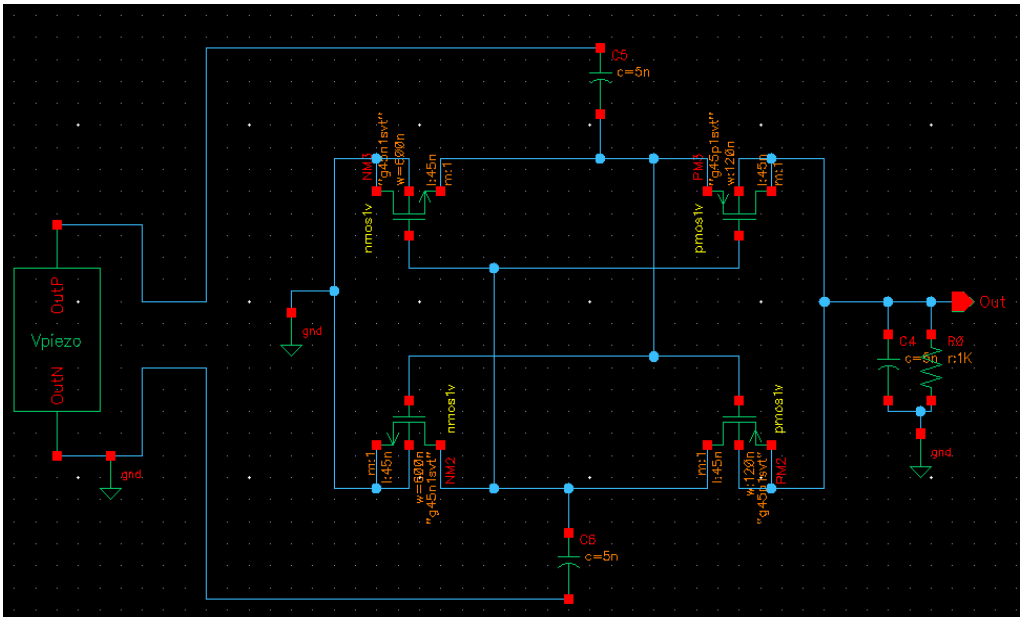

Figure 4.3: Schematic Diagram of the proposed rectifier.

The constructed rectifier design was simulated under Virtuoso Analog Design Environment (ADE L). The waveform generated is shown below.

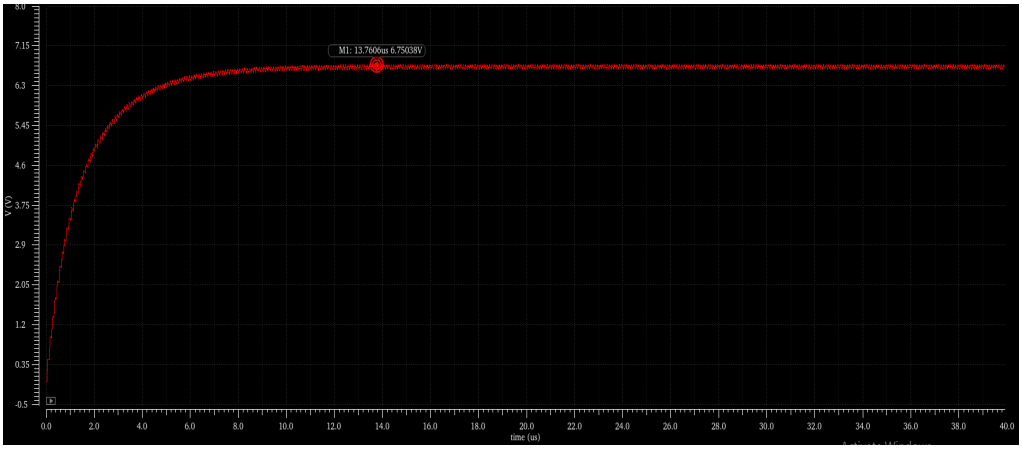

Figure 4.4: Simulated output waveform of the proposed rectifier.

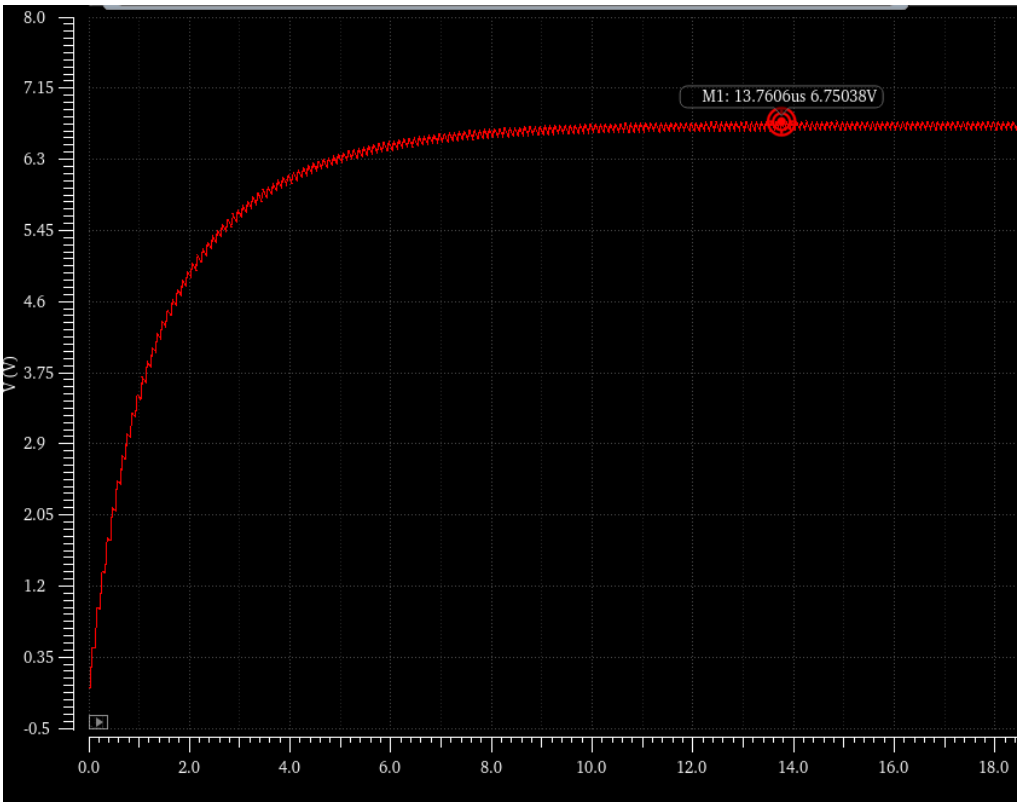

Figure 4.5: Closer look of the simulated output voltage of the rectifier.

From the figure above, the proposed rectifier generates 45 mW with a load resistance of 1kΩ. The time required for the rectifier to reach its steady state at 6.75 V is about 13.7 µs. The 5 nF filtering capacitor connected along with the load resistor helps smoothen the ripple output voltage effectively.

Figure 4.6 and Figure 4.7 shows the output current and output voltage ripples of the rectifier respectively. The measured ripple of the current and voltage are 0.1 mA and 0.1 V accordingly.

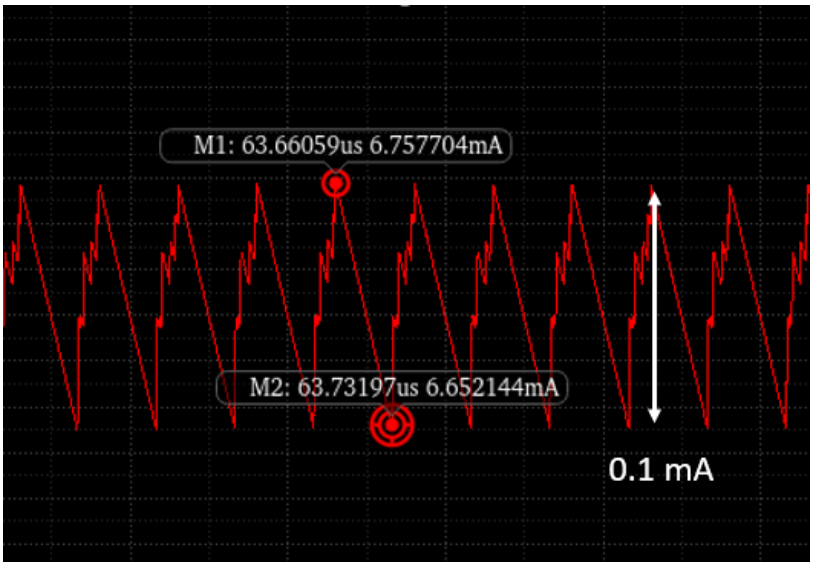

Figure 4.6: Ripple of load current.

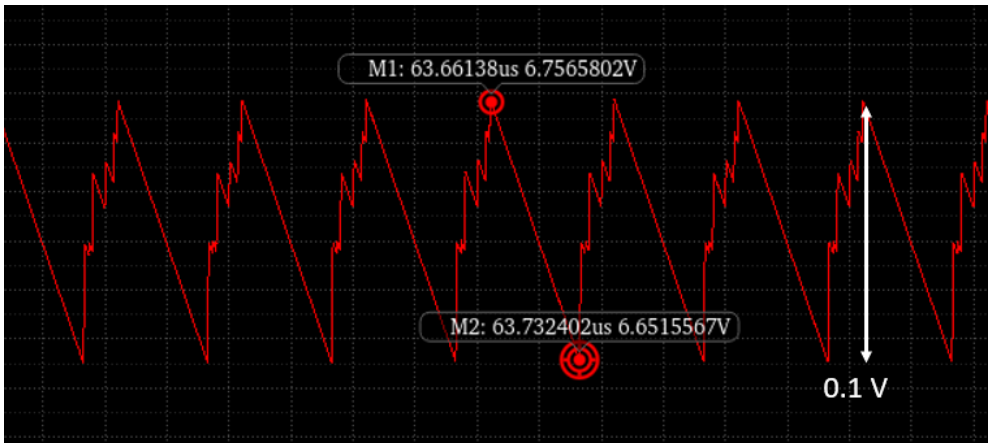

Figure 4.7: Ripple of output voltage.

To further study the efficiency of the proposed rectifier, a 2-stage differential drive rectifier was constructed and simulated under the same condition to compare the performance with the single stage rectifier. The circuit parameters used in the 2-stage rectifier are the same as the single stage rectifier.

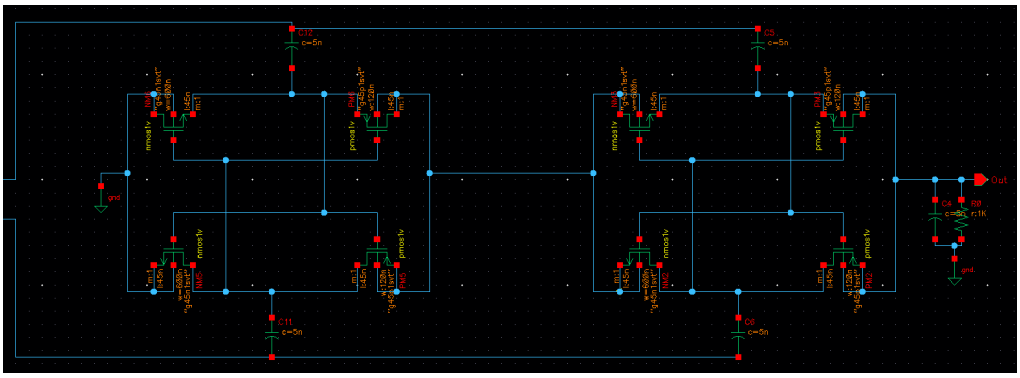

Figure 4.8: Proposed Rectifier in 2-stage configuration.

Next, a test will be conducted on the load resistance and the power generated by varying the load resistance from 625 to 1M to find out the maximum output power that can be achieved by two of the rectifiers.

Table 4.1: Single Stage Rectifier vs 2-Stage Rectifier.

Load Resistance (Ω)	Single Stage DDR		2-Stage DDR	
	V_{out}, V	I_L, mA	V_{out}, V	I_L, mA
625	5.73	7.45	5.14	7.12
1k	6.72	6.73	6.32	6.32
10k	9.97	1.00	9.43	0.94
100k	10.74	0.11	9.67	0.10
1M	10.83	0.01	9.87	0.01

According to the results obtained, the single stage rectifier has a slightly higher output current and voltage across the different resistive load ranges. The highest output current, I_L and the highest output voltage, V_{OUT} were recorded at resistive load of 1 kΩ and 10 MΩ respectively for both of the rectifiers. This means that the rectifiers were working correctly as it obeys the Ohm's Law where a drop in resistance will result in an increasing level of current. Next, the power generated by both of the rectifiers were compared side-by-side.

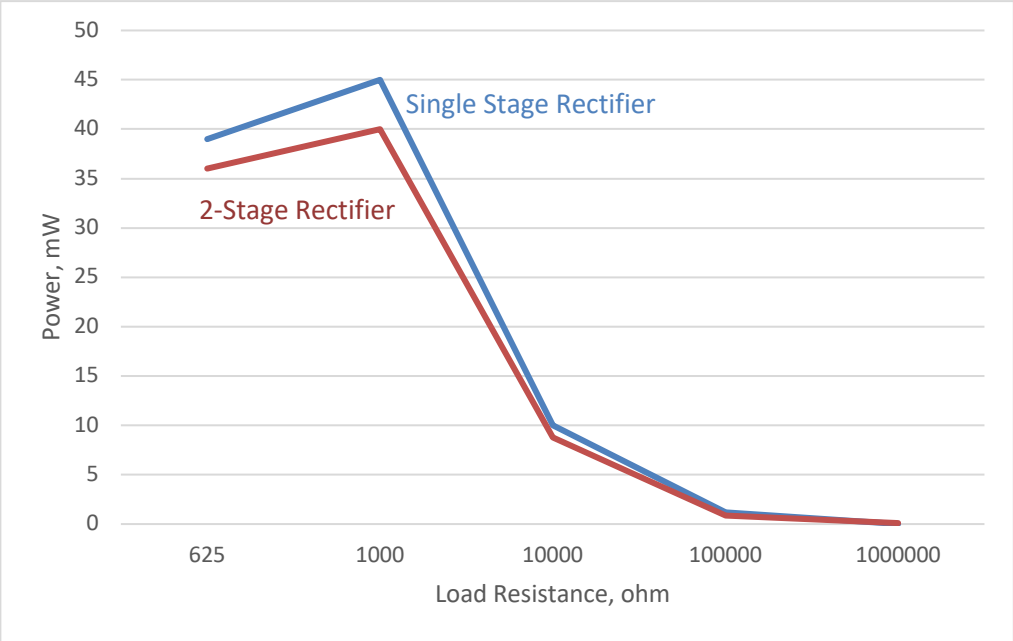

Figure 4.9: Output power of both rectifier across different loads.

The Figure 4.9 above shows the output power after rectification of both rectifiers. The single stage rectifier has a higher output power if compared to the two-stage rectifier. This is due to the power loss in the two-stage rectifier is higher resulting in a decrease in the efficiency. Highest output power for single stage rectifiers is recorded at 45 mW at 1 kΩ. In a nutshell, the single stage rectifier has a more significant performance than the 2-stage rectifier due to lower power losses. Thus, the single stage differential drive rectifier was selected. The symbol of the single stage rectifier was generated.

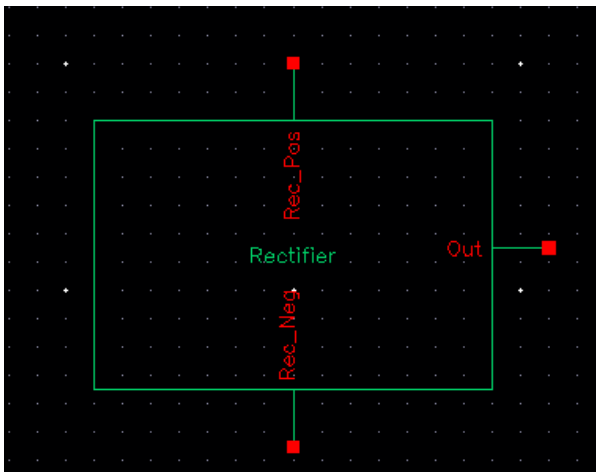

Figure 4.10: Symbol of Rectifier created.

4.3 Buck Converter Simulation Results

The output voltage generated by the rectifier is fed into the buck converter to step down into a voltage level of 3.3V. The proposed buck converter is constructed in Cadence Virtuoso using 45nm Technology. All the parameters were calculated in the previous chapter. The block circuits inside the buck converter were constructed separately into an error amplifier, comparator, and ramp generator to make the design and analysis work easier.

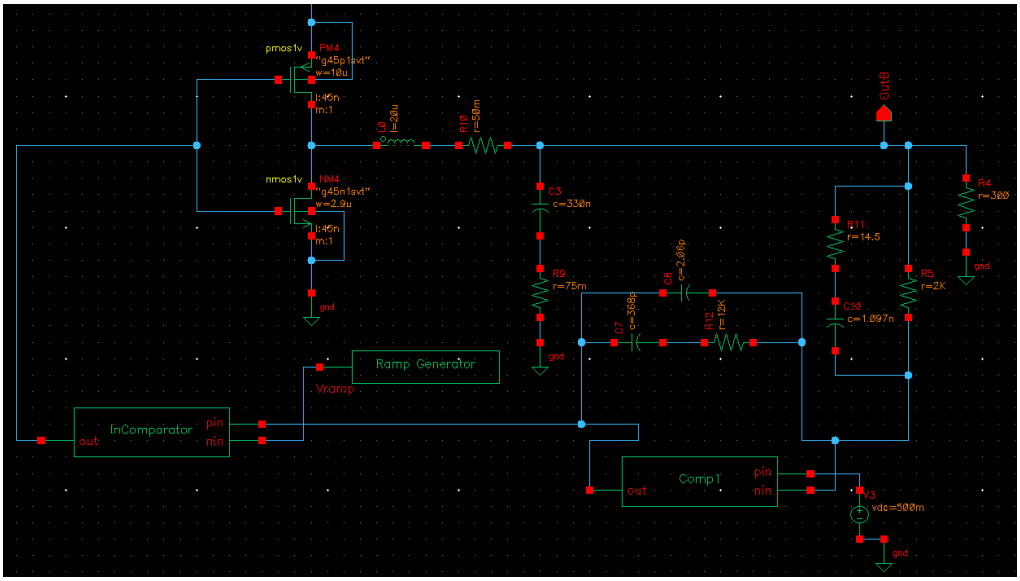

Figure 4.11: Schematic diagram constructed for Buck Converter.

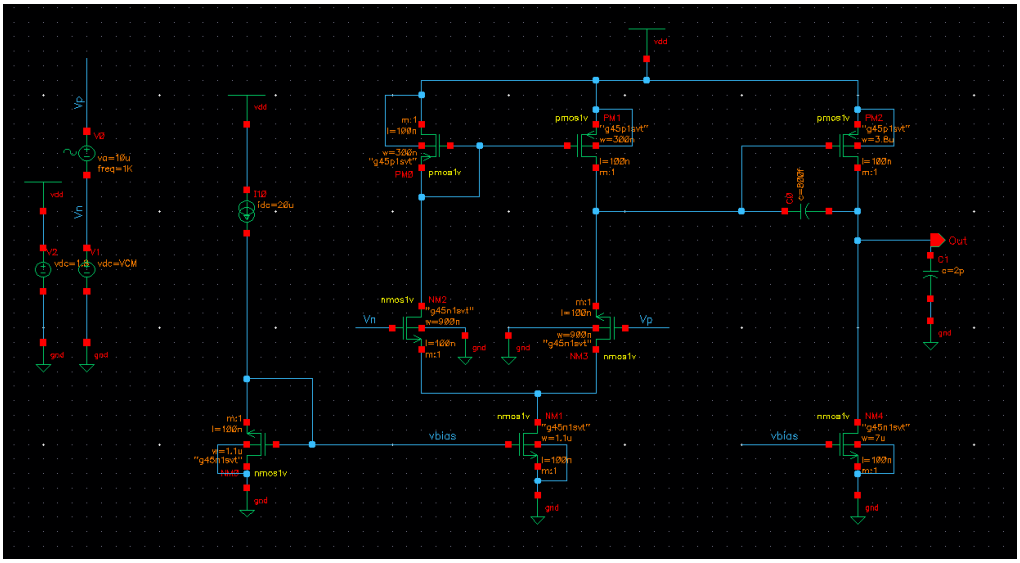

Figure 4.12: Schematic diagram of the constructed Op-amp

Figure 4.11 shows the schematic diagram of the proposed voltage control mode buck converter where its input is connected to the output of the proposed rectifier. Figure 4.12 shows the constructed schematic diagram of the error amplifier adopted from Pancholi. S and Meena. R (2016). The output voltage of the buck converter will feedback to the 'Comp1' error amplifier. The error amplifier compares the output feedback voltage and the reference voltage. If there are any differences between the 2 voltages, the error amplifier will produce an error signal. The error signal generated and the ramp voltage will then be compared by the comparator ("Incomparator" in the Figure 4.11 above). If the error signal is higher than the ramp signal, the output of the comparator will be low. Otherwise, when the error signal is lower than the ramp signal, the comparator will output a high signal in order to adjust the switching of duty cycle as shown in the figure below.

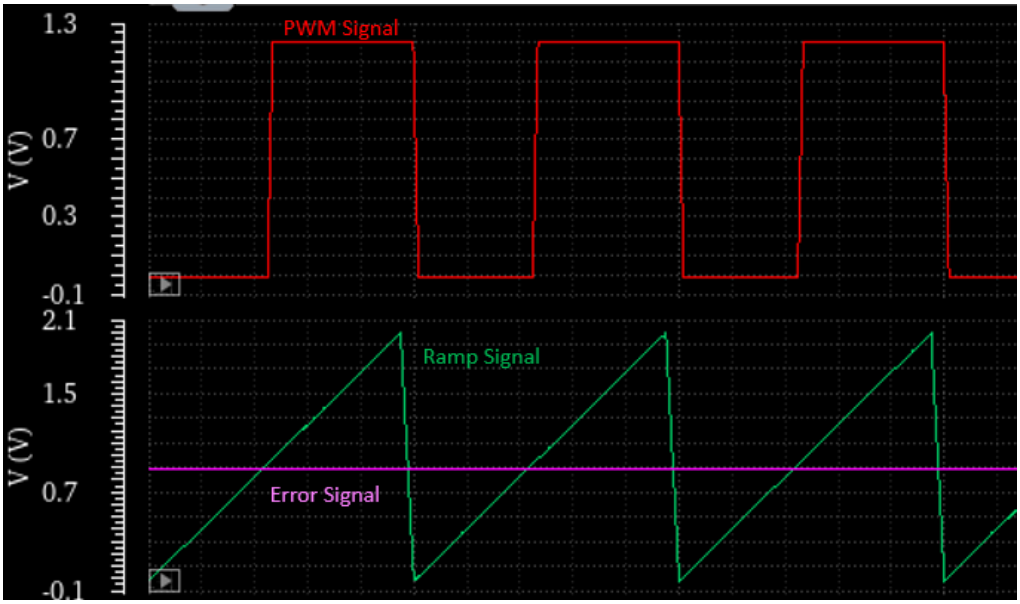

Figure 4.13: PWM waveform generated by the comparator.

The output of the buck converter is shown below. The output voltage of the buck converter reaches its steady state at 3.3V at 0.45 ms. The reason for the system to take 450 µs to reach its steady state might be caused by the large size of the capacitor as the time to charge it increases. Moreover, the input voltage of the buck converter is from the rectifier. Since the rectifier also required about 13.7 µs to reach its steady state, the buck converter will require longer time to stabilize the output voltage. However, a settling time of 450 µs still can provide a smooth transient response of the system. The proposed buck converter can step down the 6.75 V voltage rectified by the rectifier to 3.3 V smoothly with efficiency of 80.67 %.

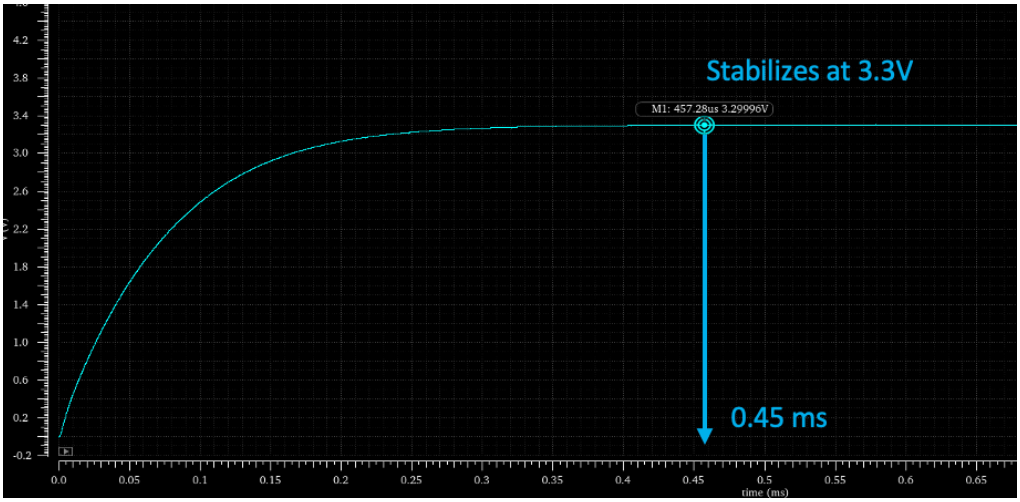

Figure 4.14: Simulated output waveform of the proposed buck converter.

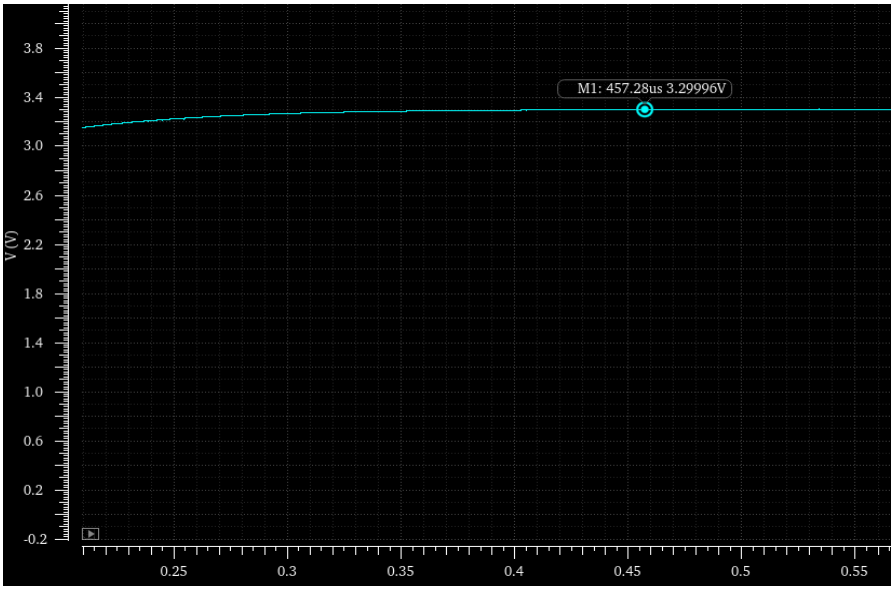

Figure 4.15: Closer look of the output waveform.

Figure 4.16 and Figure 4.17 shows the output current and output voltage ripples waveforms of the buck converter. The measured ripple of the output current and voltage are 0.1 mA and 0.1 V respectively.

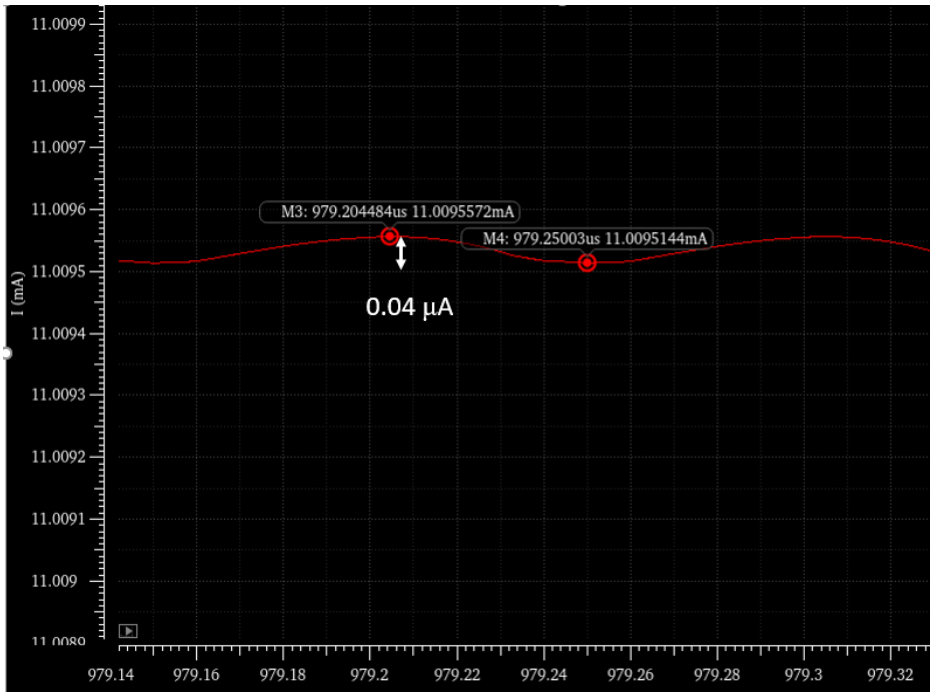

Figure 4.16: Ripple of load current.

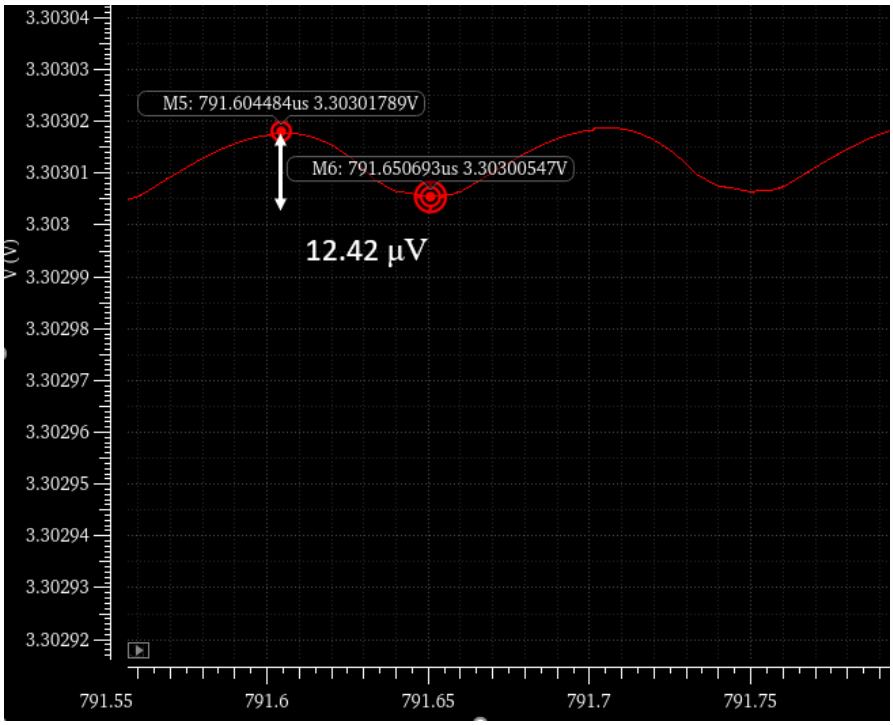

Figure 4.17: Ripple of output voltage.

The Table 4.2 below summarises the performance of the proposed buck converter. The buck converter proposed can step down the 6.75 V generated from the rectifier into a stable 3.3V voltage with the efficiency of 80.67 which meets the specification required at the beginning. The settling time needed for the output voltage to stabilize was around 450 µs. Moreover, the voltage and current ripples generated were very stable as the fluctuations were very little. In general, the proposed buck converter works well within the designed specifications. The symbol of the buck converter was created.

Table 4.2: Summary of the designed Buck Converter.

Specifications	
R_L (Ω)	300
Input Voltage (V)	6.75
Output Voltage (V)	3.30
Average Input Power (mW)	45.0
Average Output Power (mW)	36.3
Settling Time (µs)	450
Voltage Ripple (µV)	12.42
Current Ripple (µA)	0.04
Efficiency (%)	80.67

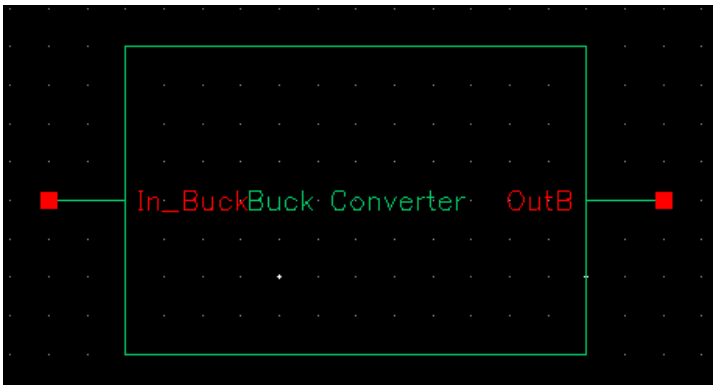

Figure 4.18: Symbol of Buck Converter created.

4.4 Summary

The voltage generated form the electromagnetic kinetic energy harvester by Hadas. Z, et al, (2021) was modelled in Cadence Virtuoso using the piecewise linear voltage from analoglib. The generated AC voltage from the passing train was then turned into a usable DC voltage by the proposed rectifier. The generated voltage was around 6.75 V with power of 45 mW. According to the studies made in Chapter 2, most of the commercially available wireless sensor nodes are operating at voltage of 3.3 V. Thus, a buck converter was proposed in order to step down the voltage into 3.3 V. The buck converter hits a high efficiency of 80.67 % at switching frequency of 20 MHz. The efficiency achieved is compared side-by-side with others designs in the Table 4.3. This is due to the downsizing of the MOS switches resulting in low parasitic output capacitance which can reduce power losses due to capacitive losses. In this study, the simplicity of each of the block circuits designed was the key strategy to reduce unnecessary power loss. In general, the proposed power management design meets the expectation set at the beginning of the previous chapter.

Table 4.3: Comparison of the PMU designed.

Author		Shaltout ('16)	Chew ('19)	This Work
Harvested Energy		Solar	PEH	KEH
Battery less		No	Yes	Yes
Integrated PMU		No	No	Yes
Technology (μm)		N/A	N/A	45
Number of Inputs		1	1	1
Number of Outputs		1	1	1
Power Management Unit	Circuitry	Mixed	Analog	Analog
	Architecture	DC-DC converter	Full-wave bridge rectifier, Analogue Control Circuit, DC-DC converter	Differential Drive Rectifier, Buck converter

	Regulated Output Voltage (V)	5	2 – 3.28	3.3
	End-to-end Efficiency	0.7	0.76	0.80

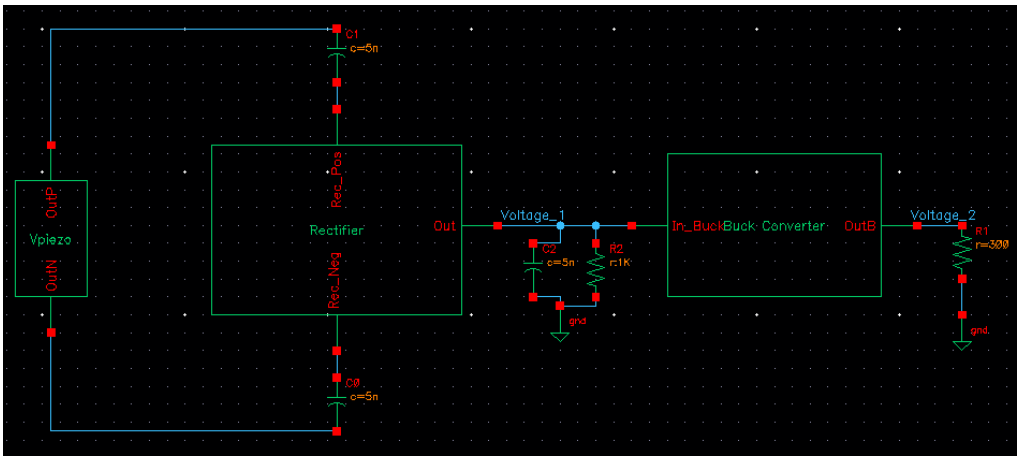

Figure 4.19: Block Diagram of the proposed PMU design.

CHAPTER 5

PROBLEMS AND RECOMMENDED SOLUTIONS

5.1 Conclusion

The characteristics of the available ambient energies were studied and an electromagnetic kinetic energy harvester was chosen and modelled. The PMU is targeted to regulate the harvested energies from the passing train (harvested by a Electromagnetic Kinetic Energy Harvester) and outputs a stable 3.3 V to the loads. The PMU proposed in this study includes a rectifier and buck converter and it was constructed in 45nm CMOS technology.

The PMU proposed is validated through schematic design simulation. A schematic level of the differential drive rectifier and a PWM voltage control mode buck converter was implemented in 45nm CMOS technology using Cadence Virtuoso. The simulation result shows the implemented rectifier and buck converter works efficiently with low ripple output voltage and load current. The performance of the PMU proposed has been analysed and proven to achieve an efficiency of more than 80% and a power of 36 mW was successcuflly generated which is sufficient to power the wireless sensor. This approach results in low power consumption, low output current and voltage ripple.This proves that the PMU design dissipates less power due to the simplicity of the design. Adding any extra blocks will lead to a higher power loss in the design. Even though the proposed PMU contains only simple blocks, the power generated from the PMU is far enough to power some low power wireless sensor node as described in Chapter 2. All of the objectives of this study were achieved. The details of the designed PMU were listed and compared to other designs in Table 4.2 in the previous chapter.

5.2 Future Work

Even though the efficiency of the proposed PMU is greater than 80%, it still can be improved. The power generated from the proposed PMU is around 36 mW which is still not enough for some power-hungry wireless sensor. To solve this, one can increase the power provided to the wireless sensor by adding a

supercapacitor to the design. Furthermore, another piece of advice for future work is to design the layout of the proposed PMU to determine the area of the chip and its power consumption. Also, the ramp generator used in this study can be replaced by another more efficient approach. Lastly, to reduce the layout size, a smaller process technology such as 5 nm, and 3 nm can be considered to replace the 45m process technology used in this study.

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