POWER MANAGEMENT FOR AMBIENT ENERGY HARVESTING IN PASSIVE INTEGRATED CIRCUIT

LOO KA FEI VIERI

A project report submitted in partial fulfilment of the requirements for the award of Bachelor of Electrical and Electronic Engineering with Honours

Lee Kong Chian Faculty of Engineering and Science
Universiti Tunku Abdul Rahman

May 2023

DECLARATION

I hereby declare that this project report is based on my original work except for citations and quotations which have been duly acknowledged. I also declare that it has not been previously and concurrently submitted for any other degree or award at UTAR or other institutions.

Signature : 

Name : Loo Ka Fei Vieri

ID No. : 19UEB04702

Date : 1st May 2023

APPROVAL FOR SUBMISSION

I certify that this project report entitled **"POWER MANAGEMENT FOR AMBIENT ENERGY HARVESTING IN PASSIVE INTEGRATED CIRCUIT"** was prepared by **LOO KA FEI VIERI** has met the required standard for submission in partial fulfilment of the requirements for the award of Bachelor of Electrical and Electronic Engineering with Honours at Universiti Tunku Abdul Rahman.

Approved by,

Signature : 

Supervisor : Dr. Khaw Mei Kum

Date : 18th May 2023

Signature :

Co-Supervisor :

Date :

ACKNOWLEDGEMENTS

I would like to thank everyone who had contributed to the successful completion of this project. I would like to express my gratitude to my research supervisor, Dr. Khaw Mei Kum for her invaluable advice, guidance and her enormous patience throughout the development of the research.

ABSTRACT

A sensor node plays a crucial role in the IoT network as it receives and transmits data from the environment to users. However, battery-powered sensor node can be bulky and requires frequent maintenance. The aforementioned issues can be solved by integrating ambient energy harvesting feature into the power management IC (PMIC) to eliminate the dependency on external power supply. PMIC is a unit that manages the power conversion from the harvested energies and provides stable power to other block units to operate within the sensor node. As the advancement in IoT field has led to the significant reduction in power consumption of sensor node, it becomes more practical to integrate ambient energy harvesting into the device.

The objectives of this project include the design of a low-powered PMIC to support the power requirement of four commercial components typically found within a sensor node, which consist of a temperature sensor, an accelerometer, an A/D converter, and a microcontroller with transceiver. The PMIC will be designed to supply output voltage of 1 V to the loads, with total power demand of 906.32 μW. Reviews on ambient sources such as solar, radio frequency (RF), human motion and thermal are conducted to study their potential to be used for energy harvesting purposes. Furthermore, the next objective is to integrate the proposed PMIC with ambient energy harvesting feature. Such IC will be designed using 32 nm CMOS technology provided by the Predictive Technology Model (PTM).

There are a total of eight blocks within the proposed PMIC, which include charge pump, cross-connected differential drive rectifier, bandgap core, comparator, voltage-controlled oscillator, ramp generator, switch controller unit and DC-DC converter with auxiliary unit. The PMIC will initially require RF (after rectification) to power the bandgap core which generates stable biasing voltage and reference current to other units. Harvested energy from solar, motion and thermal will be stored in primary storages. Those energy are allowed to flow into DC-DC converter when a minimum voltage of 0.1 V is measured across the storage. The boost topology-based converter steps up the harvested voltage to 1 V, aided with auxiliary unit as its feedback system.

The simulation results showed the PMIC is capable of supplying an output power of 913.64 μW to the loads with a power consumption of 5 μW. Though its average output voltage was recorded at 898.17 mV with a ripply voltage of 33.73 mV. A low-dropout regulator and energy profile tracker unit are suggested to be included for future work improvements.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF SYMBOLS / ABBREVIATIONS

T	temperature, K
W/L	ratio of width to length of MOS
V_{th}	threshold voltage, V
V_{REF}	reference voltage, V
V_{PP}	peak to peak voltage, V
V_{OUT}	output voltage, V
IoT	Internet of Things
WSN	Wireless Sensor Node
IP	Intellectual Property
ECG	Electrocardiagram
EMG	Electromyography
AES	Advanced Encyption Standard
MCU	Microcontroller Unit
ITU	International Telecommunication Union
GSM900	Global System for Mobile Communication at 900-1800 MHz
PMU	Power Management Unit
PMIC	Power Management Integrated Circuit
PMS	Power Management System
IC	Integrated Circuit
SoC	System on Chip
CMOS	Complimentary Metal Oxide Semiconfuctor
MOS	Metal Oxide Semiconductor
NMOS	N-Channel Metal Oxide Semiconductor
PMOS	P-Channel Metal Oxide Semiconductor
PV	Photovoltaic
RF	Radio Frequency
TEG	Thermoeletric Generator
PZT	Lead Zirconate Titanate
AC	Alternating Current

DC	Direct Current
MPPT	Maximum Power Point Tracking
MPP	Maximum Power Point
CCDD	Cross-Connected Differential Drive
SC	Switched Capacitor
SI	Switched Inductor
PWM	Pulse Width Modulation
PFM	Pulse Frequency Modulation
SPICE	Simulation Program with Integrated Circuit Emphasis
PTM	Predictive Technology Model

LIST OF APPENDICES

CHAPTER 1

INTRODUCTION

1.1 General Introduction

Rapid evolution of the Internet of Things (IoT) has been heavily relying on sensing technologies to collect data for various purposes. Sensors are electronic units that receives external information and processes it into a signal that can be distinguished by both humans and machines (OMRON Electronic Components, 2022). For instance, sensors can be used to collect data on temperature, humidity, and light, which can then be used to improve the environment in a building. As IoT continues to develop, the importance of sensing technologies will only continue to grow.

Nowadays sensors are usually integrated with microcontroller to form a sensor node, with each node able to communicate with the rest of the nodes. In general, the components within a sensor node may comprise of sensor, microcontroller, transceivers, and power management unit (PMU) (Mascarenas et al., 2007). The integrations of sensor node within a network are known as Wireless Sensor Network (WSN), which can be used in many fields such as smart supermarket, surveillance system and healthcare monitoring system. Compared with the traditional sensor network, WSN has more functionalities and can be adopted for complex applications (Okpara et al., 2020).

A power management IC, also known as PMIC, is a dedicated unit responsible for managing and supplying stable power to all block units within a device. This unit has been undergoing development to improve its power consumption, making it suitable for passive IC technology. Passive ICs are capable of harvesting ambient energy and converting it into usable electricity, operating without the need for a battery. This can be beneficial for long-running sensors in IoT-related projects. According to the latest market research presented by Technavio in 2022, the energy harvesting device market is forecasted to achieve a Compound Annual Growth Rate (CAGR) of 17%. This market trend demonstrates the growing popularity of integrating energy harvesting features to provide uninterrupted power supply to IoT sensor nodes.

This paper will present the design of a PMIC that features ambient energy harvesting, fulfilling the power demand of low-power electronic components used in IoT.

1.2 Importance of the Study

Long-lasting sensor nodes are currently demanded in IoT networks to reduce the frequency of replacing batteries. This is particularly important if there is a large number of sensor nodes installed in places that are difficult to be reached, as it could incur significant maintenance costs.

Additionally, replacing conventional battery-powered devices with more sustainable alternatives is important in reducing the overall size of components used in the IoT networks. In fact, many devices used in this field are recently shifting to operate in low power mode, making it much easier for engineers to integrate the automated power harvesting feature to support the continuous operation of the devices.

Furthermore, there exists small amounts of stray energy in the forms of sunlight radiation, heat and radio frequency are available in the environment. These forms of available energy can be harvested and converted to electricity, which can potentially become alternative of batteries as those are not environmentally friendly. However, the harvested energy is not directly compatible with most electronic devices as they may require specific voltage level to operate. Thus, the harvested energy has to be further processed by a PMIC, to make it suitable for the devices.

1.3 Problem Statement

Conventional battery powered sensors have still often been used in the market as it does not include any complicated design in the IC structure and its manufacturing cost is considerably cheap. However, most of the devices use non-rechargeable electrochemical cells with limited energy stored within it. According to a comparison study between battery and energy harvesting by Penella (2019), the power density of a battery has a linear drop against time while the ambient source has constant power density over the time as shown in Figure 1.1.

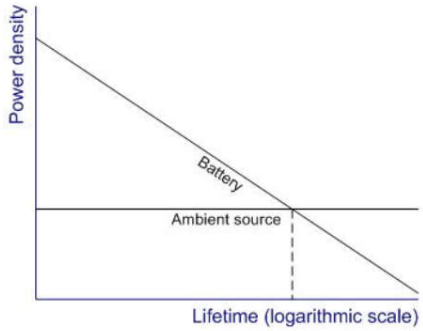


Figure 1.1: Power Density of Battery and Ambient Source Against Time

The passive IC with stray energy harvesting also has its own drawbacks where the power density of this energy is very small. The magnitude of energy mainly depends on the environment such as the amount of sunlight exposure or whether it is nearby to any broadcasting stations. Solar is the most commonly used in energy harvesting as it has the highest power density among the other ambient sources. However, such energy is only available during daytime and must be under the exposure of sunlight. Thus, a passive IC that solely relies on a single ambient source will have severe disadvantages such as not having sufficient energy to fulfil the power demand of a device.

In the design of PMIC, its power consumption becomes the important element in determining the lifespan of a device. A high-powered PMIC may not be suitable to integrate with ambient energy harvesting as the available power density of ambient sources may be insufficient.

1.4 Aim and Objectives

Based on the aforementioned issues, this project aims to design a PMIC as an interface unit to multiple ambient source transducers, which scavenges the stray energy from environment to usable electrical energy. The proposed PMIC should exhibit low power consumption to support the small ambient energy harvesting feature. In general, the objectives of this project are listed as the followings:

- To design a low power PMIC to support the power requirement of commercial devices using 32 nm CMOS technology.

- To study the existing ambient energy sources for energy harvesting feature.
- To integrate ambient energy harvesting capability to achieve a fully passive PMIC.

1.5 Scope and Limitation of the Study

The scope of this project will mainly cover the development of power management strategy for ambient energy harvesting, for the application of a passive IC. The proposed PMIC will be designed in LTspice utilising the state-of-the-art 32 nm CMOS technology provided by PTM. However, due to the time constraints, the transducers such as antenna and PV cells will not be designed. Instead, the expected waveforms of the transducers will be modelled as inputs to the designed system. Furthermore, the physical layout of the IC will not be designed or fabricated in this project.

The initial stage of the project will involve an analysis of past research to study the existing techniques in designing power management circuitry. Upon completion of design, the unit will be evaluated in terms of power consumption and functionality. Another goal of this project is to supply sufficient power to some commercial devices used in the IoT. These devices will be modelled with respective equivalent resistances to emulate its actual current drawn.

1.6 Contribution of the Study

This project will contribute to the development of PMIC for low-powered IoT devices by improving the existing power management circuitry. An advanced MOS technology, such as 32 nm CMOS will be adopted to reduce the die area and power consumption.

The innovation of a PMIC featuring ambient energy harvesting may contribute to the 12^{th} goal of Sustainable Development Goal, which aims to ensure sustainable consumption. Solar, human movements, and even stray signals lost from cellular base stations can be scavenged as alternative sources of energy. Reduction in the use of battery may lead to a reduction in waste, which potentially helps to address land pollution.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

This chapter will provide an overview on some of the commonly employed ambient energy sources for powering IoT devices. The selection of appropriate energy sources for the proposed PMIC will be discussed based on factors such as availability and power density. The basic structure of a power management system will be explained, along with its key components and functions. In addition, there will be a section that reviews and analyses the existing PMICs that incorporate ambient energy harvesting feature. Such analysis will provide insights into the current state-of-the-art and identify the potential opportunities for the proposed design.

2.2 Review on Ambient Energy Sources

2.2.1 Solar

Solar is the most commonly used in supplying power to passive ICs as it is readily available in open area. This technology involves the conversion of electrostatic radiation, or sunlight, emitted by the sun to usable electricity. The module responsible for scavenging this energy is called Photovoltaic (PV) cell. When photons, carried by light, collide with the surface of a PV cell, they induce an internal electrical field that prompts the movement of electric charges, resulting in the generation of electricity.

Kim et al. (2014) found out that the outdoor sunlight has power density of 100 $mWcm^{-2}$ and could output 0.5 V with a single silicon-based PV cell. According to research carried out by Vullers at al. (2009) and Politi et al. (2021), the power density generated by natural light from windows can range from 0.1 to 0.7 $mWcm^{-2}$. However, due to the low power efficiency, which is typically up to 30 % as maximum, a large area of PV modules is needed to scavenge sufficient solar energy.

The efficiency can become worse as the surrounding conditions such as temperature and light exposure tend to vary over the time. Maximum Power Point Tracking (MPPT) has been employed to solve such issue. It is a

technique that allows PMIC to extract the maximum power point (MPP) from PV cells by dynamically controlling output voltage and current (Lueangamornsiri et al., 2016). Nahak and Pal (2017) demonstrated the usage of MPPT aided with various algorithms such as modified perturb and observe, artificial neural network and fuzzy logic controller. The output of MPPT was used to control the duty cycle of switching transistor in DC-DC converter to ensure the harvester system operates in maximum power mode.

2.2.2 RF

Current rapid development of telecommunication technology has undoubtedly led to the emission of RF energy to the environment. The wasted RF energy from cellular base stations or even from induction heat appliances can be harvested to power a passive IC.

RF radiation can be categorised by different frequency ranges, which correspond to particular bands of the electromagnetic spectrum. The International Telecommunication Union (ITU) separates such spectrum into multiple bands for the public services as shown in Table 2.1. In Malaysia, 470 - 694 MHz are allocated for Television broadcasting services, while 925 - 960 MHz (GSM900) and 1805 - 1880 MHz (GSM1800) are allocated for cellular mobile services (MCMC, 2022).

To harvest energy from the UHF band, it is expected to deal with a relatively low power density level as compared with other ambient sources. Sufiah et al. (2010) conducted an evaluation of RF radiation exposure on 10 sites around Kuala Lumpur and Selangor. The results of the studies showed that the RF exposure could be up to 0.724 μWcm^{-2}, with the majority of radiation being contributed by the cellular GSM900 stations. It can be explained by the fact there is a larger number of such stations being built around the site. Another factor that affects the power density is the distance between the transmitter and the harvester. According to Visser, Reniers and Theeuwes (2008), RF power density in the range between 0.01 μWcm^{-2} and 0.3 μWcm^{-2} was recorded at a distance ranging from 25 m to 100 m from a GSM900 station.

Table 2.1: Frequency Bands in RF Spectrum (Radio Frequency Bands, n.d.)

Frequency Range	Band Name	Application / Service
3 - 30 kHz	VLF	Marine Navigation
30 - 300 kHz	LF	Marine Navigation
300 kHz - 3 MHz	MF	Aviation Radio
3 - 30 MHz	HF	Shortwave Radio
30 - 300 MHz	VHF	FM Radio
300 MHz - 3 GHz	UHF	Cellular, Wi-Fi, 4G
3 – 30 GHz	SHF	Satellite Communication, 5G
30 – 300 GHz	EHF	Satellite Communication

2.2.3 Thermal

Thermal energy harvesting involves the conversion of temperature differences into electricity through the use of thermoelectric devices. Such a device utilises the Seebeck effect which is the production of electrical potential difference between two dissimilar semiconductors with each being placed in region with different temperature.

The thermoelectric is suitable for application that uses human body heat as the energy source to power the wearable devices embedded with sensors and transceivers. According to Leonov (2013), the author integrated a thermoelectric harvester to a shirt to study the power generated from a person in a day. When a person leaves the building with low ambient temperature for outdoor biking, the harvested power was increased significantly from 1 mW to 4 mW due to the huge change in ambient temperature as shown in Figure 2.1. It was also concluded that the power harvested from thermoelectric depends on the body heat, sweating rate and air flow exposed to the person rather than the metabolic rate of a person.

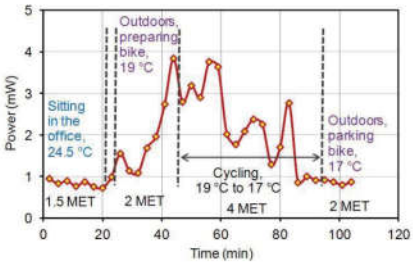


Figure 2.1: Power Harvested from Shirt Integrated with Thermoelectric Harvester Recorded by Leonov (2013)

2.2.4 Vibration

Electrical energy can also be extracted from kinetic energy in the form of mechanical strain or vibration which is known as direct piezoelectric effect (Sezer and Koç, 2021). Due to this mechanism, the piezoelectric harvester can be advantageous especially for healthcare devices such as smart health watches and wearable ECG monitors.

Unlike other energy sources, the motional energy can be harvested without depending on external conditions such as sunny daytime for solar energy scavenging. In the recent paper published by Liu, et al. (2021), the power density harvested from piezoelectric transducers that attached at shoulder and arm was recorded at 14.3 $mWcm^{-3}$ and 4.92 $mWcm^{-3}$ respectively. It summarised that the motional movement of the wrist can yield the highest power density. However, the study also mentioned that most of the piezoelectric materials can only harvest energy in the range of nW up to µW.

2.3 Overview of PMIC Structure

Modern electronic devices are integrated with PMIC for efficient power conversion and distribution. It can be considered as an Intellectual Property (IP) block which has been separately designed and verified before integrating with a larger system. Such system is often examined by its capability in regulating voltage to various components without consuming much power from the sources as well as having self-starting feature (Vullers, 2009).

In general, the blocks within PMIC mainly consist of voltage converter and voltage regulator as stated by El-Nozahi et al. (2010). Voltage converters can be divided into DC-DC and AC-DC converters depending on

the type of energy sources. It is responsible for converting voltage from a source to another voltage with different magnitude that matches with the load. On the other hand, a voltage regulator unit is responsible for supplying constant output voltage under conditions such as voltage changing at its input and current drawing from the load.

Unless the ambient energy source is solar, an AC-DC converter unit is usually being used in PMIC to rectify the alternating voltage from the harvester to DC voltage. Such a unit is often known as a rectifier, and it has been designed in many different topologies. One of the topologies is the cross-connected differential drive (CCDD) rectifier which was employed by Lee et al. (2018). Although the design is small and simple, its efficiency is limited by the MOS threshold voltage. Another rectifier is based on Dickson charge pump which is commonly used in harvesting RF energy. Marshall, Morys and Durgin (2015) demonstrated the usage of this rectifier to both rectify and boost the stray RF that has low magnitude. Unlike the first topology, this rectifier is usually bulky as it needs to be cascaded for certain stages to obtain the required output voltage level.

DC-DC converter can be divided into switched inductor (SI) converter (buck, boost and buck-boost) and switched capacitor (SC) converter. Buck converter generates voltage that is lower than its input, boost converter steps up voltage, while buck-boost converter is able to operate both. Chowdary, Singh and Chatterjee (2016) integrated a buck-boost converter unit into their PMIC that was able to receive output from three harvesters simultaneously with only requiring a single off-chip inductor. Though, low powered auxiliary circuits such as oscillator and comparator are needed to guarantee a design with high efficiency. On the other hand, Seeman, Sanders and Rabaey (2007) employed two SC converters that separately generates 0.7 V and 2.1 V from a battery with voltage level at 1.2 V. SC converter is usually smaller in size as compared with SI converter but may have significant parasitic losses under high switching frequency condition (Seeman and Sanders, 2008).

2.4 Review on Existing PMIC

According to research conducted by Lhermet et al. (2008), the authors proposed a PMIC that harvests RF and thermal energies. The unit includes an

asynchronous finite state machine that controls the priority of two resources. The load of the system, which is a micro-battery, is required to be charged at 27 µA. Its performance was recorded to achieve a power transfer efficiency of 78%. However, such a design was unable to harvest energy from two ambient sources simultaneously.

A passive powered body sensor node fabricated in 130 nm CMOS technology was proposed by Zhang et al. (2013). The system was designed to support the processing of body sensors such as ECG and EMG as well as to power a RF transmitter to send processed data using harvested energy from both RF and thermoelectric. The system rectifies and steps up the small, harvested voltage (in mV) to 1.35 V and charges a temporary storage capacitor. From the capacitor, the stored voltage is then converted to multiple regulated voltages to power different loads.

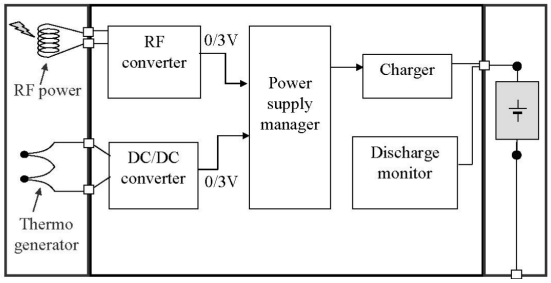


Figure 2.2: PMIC Unit Proposed by Lhermet et al. (2008)

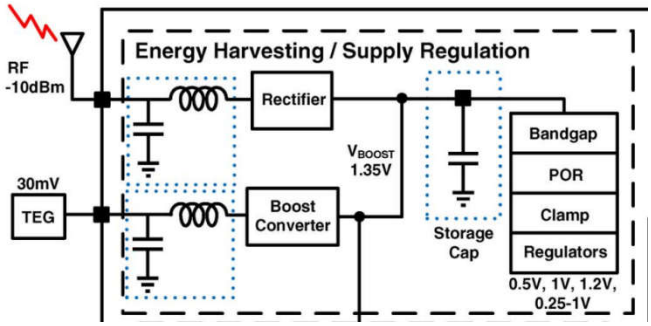


Figure 2.3: PMIC Unit Proposed by Zhang et al. (2013)

Similarly, the ambient energy harvesting feature was also integrated into biomedical application as proposed by Huang et al. (2014). The authors designed a passive SoC that harvests solar and RF energies for physiological sensors that measures parameters such glucose, temperature, protein, and pH

values. A rectifier unit was included to convert the harvested RF energy at 1 MHz to a certain DC voltage. A SC voltage circuit was implemented to combine the harvested DC voltage from both sources. A Pulse Frequency Modulation (PFM) based boost regulator was adopted to boost the combined voltage to a single voltage level at 1.8 V. Upon the data collection from the sensors, the PMIC will also provide energy to its built-in OOK transmitter with a total power consumption of 762 µW for data sending. The experimental results showed that the built-in sensors and transmitter were able to be powered by the harvested energies.

Aktakka and Najafi (2014) proposed a CMOS based autonomous vibrational energy harvester. The scavenged AC voltage will undergo two-stage rectification with low voltage drop at 30 mV before being stored to a temporary storage with capacitance value of 4.7 µF. A trickle charger was incorporated to transfer the rectified voltage intermittently to the permanent reservoir. The vibration harvester was measured to be able to output 24.1 µW with 6.1 V_{PP} to the power management circuitry under 0.5 g vibration input. The overall system was able to charge a 20 mF capacitor from 0 V to 1.35 V within 19 minutes with a low internal power consumption at 0.5 µW.

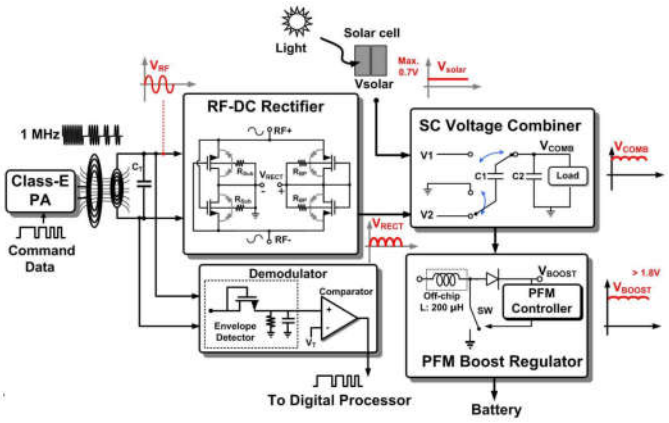


Figure 2.4: Block Diagram of PMIC for Biomedical Sensor Node Proposed by Huang et al. (2014)

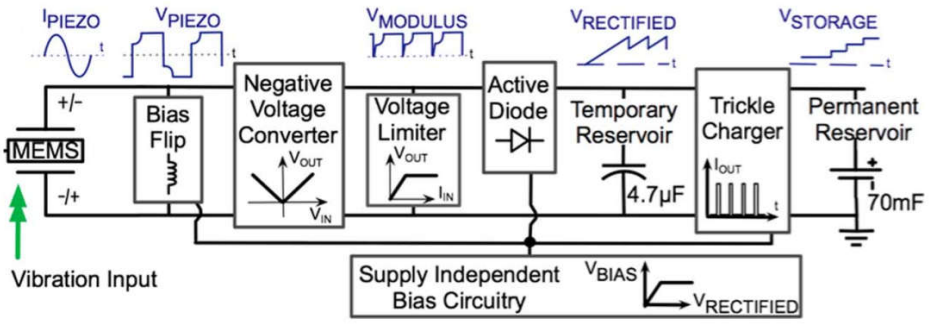


Figure 2.5: PMIC Developed by Aktakka and Najafi (2014)

Mui, Khaw and Yasin (2020) proposed a PMIC for a dual-input-triple-output energy harvester as shown in Figure 2.6, which scavenges RF energy and vibrational energy to electrical energy. Each harvested AC voltage from the ambient sources will be converted to DC voltage through a full wave rectifier before being stored in the secondary capacitor. Once any of the secondary capacitors is charged to a certain level, the energy will then be transferred to the primary capacitor through a NMOS. A voltage divider produces three reference voltages to the asynchronous PMS. A regulator is added to provide stable supply to the PMS unit. The PMS unit basically distributes the harvested energy to the loads by controlling the NMOS switch. The validation results showed that the proposed system was capable of supplying power to three loads including AES, MCU and RF transceiver with power consumptions of 52.6 µW, 70 µW and 98 µW, respectively.

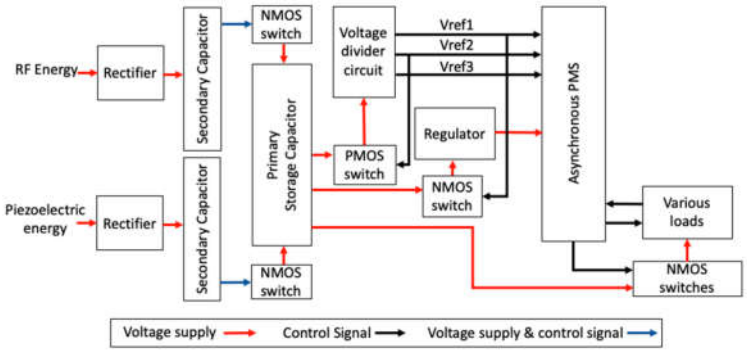


Figure 2.6: lock Diagram of PMIC Proposed by Mui et al. (2020)

2.5 Summary

Based on Table 2.2, there were indeed numerous PMICs designed to power different types of applications. Four ambient energy sources were reviewed in the previous section. Solar has the highest power density among the energy sources, followed by motion, thermal and RF. However, solar may require a large number of PV cells which leads to bulky design. It is also found out that RF and thermal sources may have potential to be used as alternative energy as those are readily available in the environment despite their small power density. In this study, a PMIC with four inputs will be designed to power the selected loads, which will be introduced in the subsequent chapter. Both CCDD rectifier and charge pump will be employed to convert the harvested AC voltage from transducers. An inductor-based converter will be used to boost the rectified voltage, integrated with low powered auxiliary circuits. Other block units will also be added which can be the contributions made in this paper.

Table 2.2: Summary of Past Research on PMIC Design

References	Technology	Sources	Application	Voltage Supply	Output Power
Lhermet et al. (2008)	0.18 µm	RF, TEG	Battery	-	27 µA (charge current)
Zhang et al. (2013)	130 nm	RF,TEG	Body Sensor Node	1.35 V	280 µW
Aktakka and Najafi (2014)	0.18 µm	PZT	Battery	1.8 V	81.7 µW
Huang et al. (2014)	0.35 µm	PV, RF	Body Sensor Node	1.8 V	942.90 µW
Mui, Khaw and Yasin (2020)	90 nm	RF, PZT	AES, MCU, RF Transceiver	1.2 V	220.36 µW

CHAPTER 3

METHODOLOGY AND WORK PLAN

3.1 Introduction

A passive PMIC integrated with ambient energy harvesting features will be designed to power some of the commercial electronic devices. Specifications of ambient sources will be mentioned, which are used as inputs of the design to power the selected loads with each having specific power demand. LTspice will be used to both design the transistor level schematics and simulate the functions of the proposed design. This chapter will also cover the concept description of the proposed PMIC, followed by the design procedures of each building block.

3.2 Sources and Loads Specifications

According to the reviews conducted in the previous chapter, the energy harvested from the ambient sources could be sufficient to supply power for applications with low power consumption. The outputs of harvester elements such as RF and vibration transducers are not suitable to be the direct power supply to the loads. Hence, a PMIC is needed to manage and convert the harvested power to a usable form of power. Table 3.1 shows the outputs of four ambient harvesters which will be used as inputs to the design. For general purpose usage, the proposed PMIC should be capable of handling different types of ambient sources.

Table 3.1: Inputs Specifications of Proposed PMIC

Ambient Sources	Output of Harvesters
RF	-25 to 0 dBm @ 915 MHz
PZT	2.82 V_{PP} @ 120 Hz
TEV	0.22 to 0.45 V
PV	0.5 V

Multiple devices with different functions and power requirements are chosen as the output loads of the proposed PMIC, which are shown in Table 3.2. These are the devices used for IoT application that typically comprises sensors (temperature sensor and accelerometer), signal processing unit (A/D converter), microcontroller and transceivers. For simulation purposes, each load will be represented as resistive loads with specific current consumption. The equivalent resistances for each load are shown in Table 3.3.

Table 3.2: Power Demands of the Selected Loads

Selected Loads / Electronic Devices	**Power Demand (µW)**
MAX30208 Temperature Sensor	241.00
KX022 Accelerometer	36.00
ADS1114 A/D Converter	368.00
eZ430-RF2500 Microcontroller with Transceiver	261.32

Table 3.3: Equivalent Resistance for each Loads

Selected Loads / Electronic Devices	**Equivalent Resistance (kΩ)**
MAX30208 Temperature Sensor	3.3
KX022 Accelerometer	22.5
ADS1114 A/D Converter	2.2
eZ430-RF2500 Microcontroller with Transceiver	3.1

3.3 LTspice

LTspice is a SPICE-based, which stands for Simulation Program with Integrated Circuit Emphasis, circuit simulator software that is used for designing schematics and simulating performance analysis of a design. It provides stable circuit simulation given with schematics editor, symbol editor,

waveform viewer, and a huge library of active and passive components. Netlist information can be extracted and saved in .net file from the graphical schematics (in .asc file).

Figure 3.1: Logo of LTspice

3.4 State-of-the-Art CMOS Technology by PTM

Predictive Technology Model (PTM) is a platform, developed by the Nanoscale Integration and Modelling (NIMO) Group at Arizona State University (ASU), that provides SPICE models of a variety of CMOS technologies, for used in any SPICE-based simulator programs. As stated in the objectives, a 32 nm PTM model for CMOS will be chosen to design each block in the PMIC. Such technology is chosen as the design only involves low power application (from nW up to µW), as well as being beneficial to develop an IC with minimal sizing. To use such technology in LTspice, its model is imported to the schematic editor as shown in Figure 3.2.

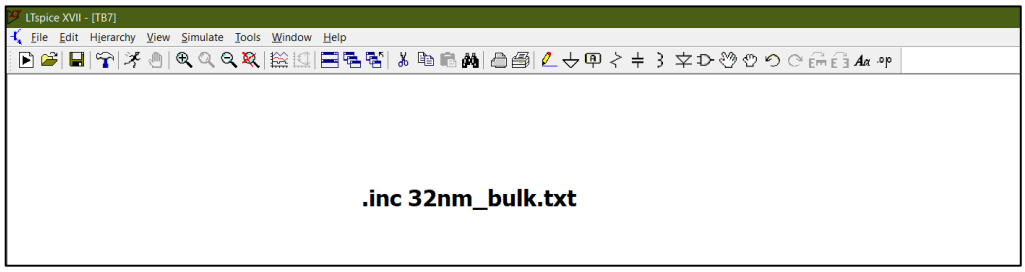


Figure 3.2: Import of the 32 nm CMOS model in LTspice Schematic Editor

3.5 Description of Proposed PMIC

Figure 3.3 illustrates the whole block diagram of the proposed PMIC for ambient energy harvesting purposes. As mentioned earlier, the system will be designed to power multiple loads using the energy harvested from RF, vibration, thermal difference, and sunlight. The scope of this project will not

involve the designing of harvester circuits, instead, the expected outputs of the harvesters will be taken as the direct inputs to the PMIC. Such design will feature a total of 10 pins, each with a specific definition as outlined in Table 3.4, which provides the information on the purpose of each pin. Inductor and capacitor used for DC-DC conversion are not included to minimise the die area of PMIC.

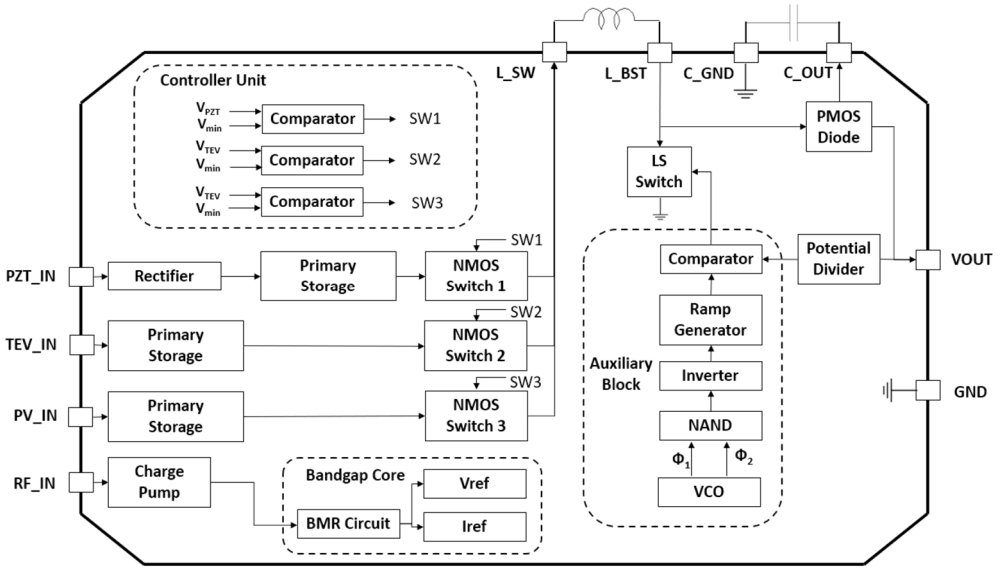


Figure 3.3: Block Diagram of Proposed PMIC

Table 3.4: Pin List of Proposed PMIC

Pin	Pin Definition
PZT_IN	Output voltage from piezoelectric harvester
TEV_IN	Output voltage from thermal harvester
PV_IN	Output voltage from photovoltaic module
RF_IN	Output voltage from RF harvester (typically in the form of antenna + LC Circuit)
L_SW	Connection of off-chip boost converter's inductor at harvested voltage node
L_BST	Connection of off-chip boost converter's inductor at switching node

C_OUT	Storage capacitor (typically in μF range)
C_GND	Ground point of capacitor
VOUT	Output voltage to load
GND	Ground point

The initial process involves the storage of the harvested energy in the primary storage units. Since the output voltage of a piezoelectric harvester takes the form of AC voltage, a rectifier unit is added to convert it to DC voltage to charge the primary storage. NMOS switch acts as a pass transistor that allows or blocks current flowing from the storage to the DC-DC converter. The NMOS switch controller unit continuously monitors the primary storage's voltage level. If the voltage across the primary storage exceeds a specific level such as 0.1 V, the unit will turn ON the NMOS switch. Unlike the other ambient source, the energy scavenged from RF source will only be used to power the bandgap core, which generates both reference voltage and current to support the operation of the PMIC.

A DC-DC converter, implemented in boost regulator topology, is used to step up the low-amplitude voltage to 1 V. The output voltage will be sampled by the potential divider, which generates a feedback voltage. An auxiliary block functions as a negative feedback system to ensure a constant output voltage by controlling the duty cycle of Pulse Width Modulation (PWM) signal to the gate of the switching transistor, denoted as LS Switch.

3.6 Design Procedures of Analog and Digital Blocks

3.6.1 Charge Pump

Charge pump is a type of rectifier commonly used in RFID application that both rectifies and steps up the low-amplitude input AC voltage. Figure 3.4 shows the conventional schematic of a single stage charge pump which will be applied in the design. In fact, the working principle of this circuit was originally derived from the Dickson charge pump, as shown in Figure 3.5, that used to generate voltage higher than its input. The changes were made to eliminate the need of any clock signal to the charge pump.

Considering the single stage circuit in Figure 3.4. During the negative half cycle, C1 will be charged to V1 as D1 is forward biased. During the next half cycle, D1 is reverse biased while D2 is forward biased. C2 will be charged up to 2V1, resulting in an output voltage to be twice the input voltage in the single stage charge pump.

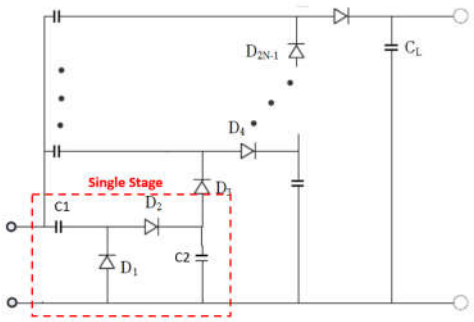


Figure 3.4: Schematic of Proposed N-Stage Charge Pump

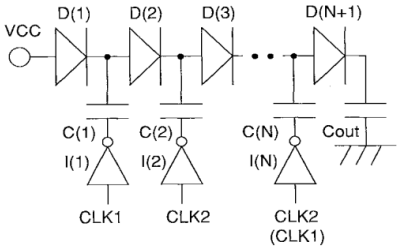


Figure 3.5: Dickson Charge Pump

In practical terms, the actual output voltage will be lower than the expected value due to the forward drop (in the range of 0.3 to 0.7 V) of the diode. Thus, diode connected NMOS, as shown in Figure 3.6, will be used to replace the diode. Besides reducing the overall size, it also reduces the voltage drop down to the threshold voltage V_{th} of NMOS.

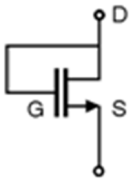


Figure 3.6: Diode-Connected NMOS

The width-to-length (W/L) ratio of MOS will highly affect the efficiency of the charge pump. To achieve optimal power transfer from the RF source, W/L ratio of NMOS should be high for low threshold voltage. The output voltage of the N-stage charge pump can be approximated as $(V_{RF} - V_{th})(N+1)$. Hence, given with the lowest RF input of -20 dBm, which corresponds to voltage amplitude of 0.465 V, a four-stage charge pump is required to generate 1 V for the bandgap core. Table 3.5 summarises the parameters of the proposed charge pump.

Table 3.5: Parameters of Proposed Charge Pump

Parameters	Value
W/L ratio of NMOS	2.4 µm / 32 nm
Flying capacitor	0.1 pF
Output capacitor	1 pF
V_{th} of NMOS	0.247 V
Number of stages	4
Minimum output voltage	1 V

3.6.2 CCDD Rectifier

A cross-connected differential drive (CCDD) rectifier is used to rectify the AC voltage generated from the PZT harvester. Figure 3.7 illustrates the structure of the rectifier, which consists of PMOS (MP1 and MP2) and NMOS (MN1 and MN2). During the positive half cycle, where V+ >> V-, MP1 and MN2 turn ON while MN1 and MP2 turn OFF. The current from the harvester will flow through MP1 to VOUT, then flow from GND back to the harvester through MN2 as shown by the red arrows. During the negative half cycle, where V+ << V-, MP2 and MN1 turn ON while others turn OFF. Similar to the previous condition, the current flows in the same direction through the VOUT and GND nodes, resulting a DC output voltage.

In designing this unit, the W/L ratio of PMOS is adjusted to be twice larger than that of NMOS as PMOS has larger ON-resistance. The parameters of such rectifier are shown in Table 3.6.

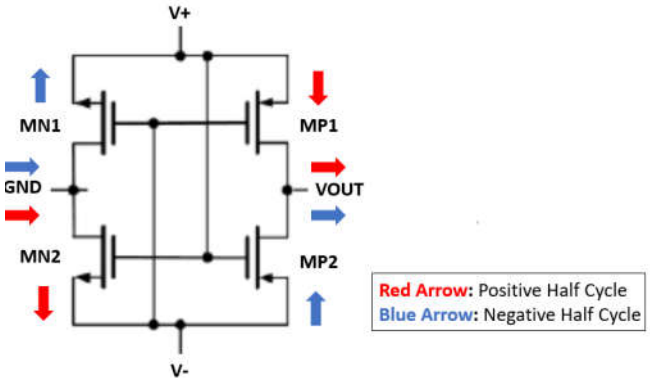


Figure 3.7: Schematic of CCDD Rectifier

Table 3.6: Parameters of CCDD Rectifier

Parameters	Value
W/L ratio of NMOS	0.75 µm / 32 nm
W/L ratio of PMOS	1.50 µm / 32 nm

3.6.3 Bandgap Core

A bandgap core is an essential block that generates biasing voltage, current source, and current sink to other blocks for normal operation. The performance of such a block is often evaluated based on its capability in producing stable output voltage and current, regardless of variation in operating conditions such as temperature, supply voltage and load impedance.

The proposed bandgap core will be based on the concept of Beta-Multiplier reference circuit as shown in Figure 3.8. According to a study conducted by Liu and Baker (1998), VREF and IREF were formulated as:

$$V_{REF} = \frac{2}{R\beta}\left(1 - \frac{1}{\sqrt{K}}\right) + V_{TH,MN1} \quad (3.1)$$

$$I_{REF} = \frac{2}{R^2\beta}\left(1 - \frac{1}{\sqrt{K}}\right)^2 \quad (3.2)$$

β, known as transconductance parameter, is the product of MOS surface mobility μ_0, capacitance per unit area of the gate oxide C_{ox}, and W/L ratio of MN1, while K indicates the number of MN1 connecting in parallel configuration. The above equation shows that the references are independent of the supply voltage.

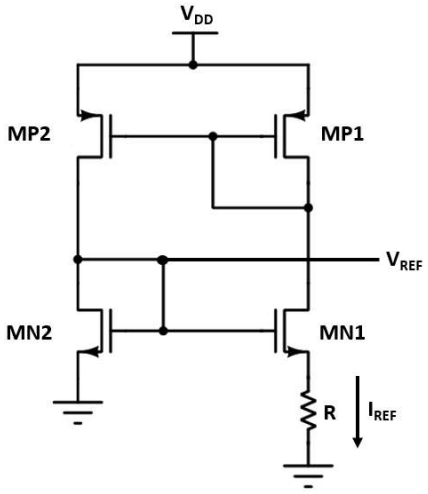


Figure 3.8: Beta-Multiplier Reference Circuit

Under variation in temperature, the threshold voltage of MOS has negative temperature coefficient, while the resistance of resistor has positive temperature coefficient. Beta-Multiplier circuit is designed in a way that uses both components to generate a constant reference by cancelling out their temperature dependencies. The above equation is further derived to obtain the temperature coefficient as

$$\frac{\partial V_{REF}}{\partial T} = \frac{\partial V_{TH,MN1}}{\partial T} - \frac{2}{R\beta}\left(1 - \frac{1}{\sqrt{K}}\right)\left(\frac{1}{R}\frac{\partial R}{\partial T} + \frac{1}{K\mu_0 C_{ox}(T)}\frac{\partial K\mu_0 C_{ox}(T)}{\partial T}\right) \qquad (3.3)$$

In general, the temperature coefficient, whether it is positive or negative, can be tuned by the values of R and K.

Figure 3.9 illustrates the proposed Beta-Multiplier based bandgap circuit. Unlike the previous circuit, an operational amplifier (OA) is added to generate a stable V_{BIAS} by ensuring drain voltage at MN2 is equal to the drain voltage at MN1, hence a constant IREF is obtained. The generated biasing

voltages are used to bias another PMOS and NMOS, with similar W/L ratio, to mirror the I_{REF}. Table 3.7 lists out the parameters of the proposed bandgap circuit.

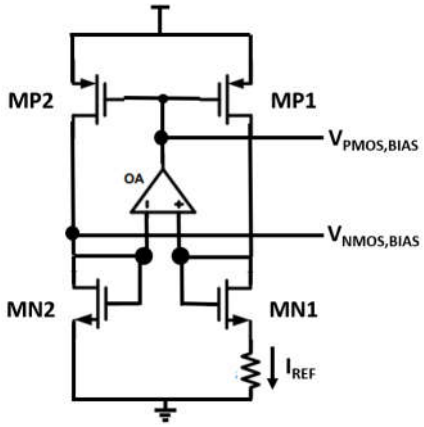


Figure 3.9: Schematic of Proposed Bandgap Core

Table 3.7: Parameters of Proposed Bandgap Core

Parameter	Value
Operating Voltage	1 V
W/L ratio of MP1 and MP2	0.96 µm / 0.064 µm
W/L ratio of MN1 and MN2	0.16 µm / 0.064 µm
Number of parallel MN1	4
Resistance of R	60 kΩ

3.6.4 Voltage Controller Oscillator (VCO)

A VCO is a unit that produces an output oscillating signal with frequency determined by its input voltage. The basic structure of a ring oscillator, which is a commonly deployed oscillator topology, is shown in Figure 3.10. It consists of an odd number of NOT gates (requiring three NOT gates as minimum) connecting in a loop, with the output of the last gate being fed back to the gate of the first gate. A NOT gate can be designed by simply connecting a PMOS in series with a NMOS as shown in Figure 3.11.

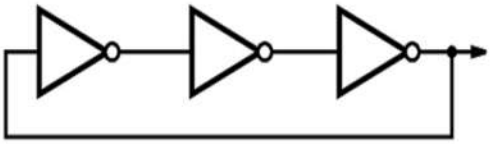


Figure 3.10: Ring Oscillator

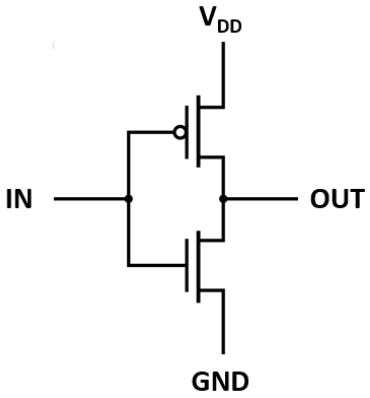


Figure 3.11: CMOS-Based NOT Gate

Figure 3.12 shows the proposed design for VCO using the concept of ring oscillator. Current limiting feature is added by having PMOS and NMOS as current source and current sink respectively, to minimise the current consumption of the VCO. By considering Table 3.8, both input voltage and the value of each C_L will be adjusted to achieve a stable output voltage oscillating at 10 kHz, with peak-to-peak voltage V_{PP} of 1 V.

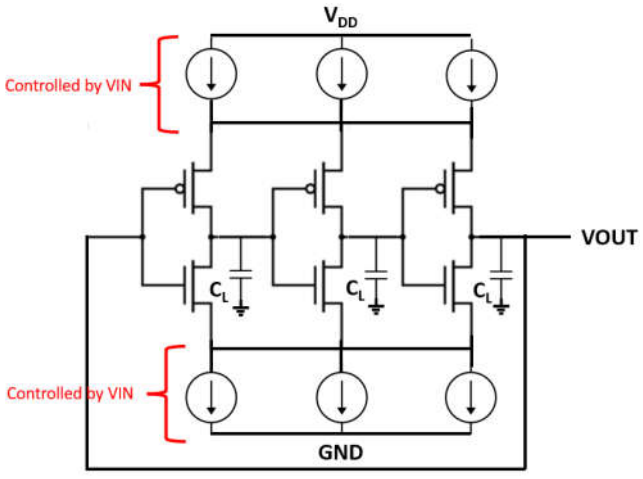


Figure 3.12: Schematic of Proposed VCO with Current Limiting Feature

Table 3.8: Parameters of Proposed VCO

Parameter	Value
Operating voltage	1 V
Oscillating frequency	10 kHz
Output voltage	1 V_{PP} sine wave
Number of NOT gates	3
W/L ratio of current source PMOS	0.2 µm / 1 µm
W/L ratio of current sink NMOS	0.1 µm / 1 µm
W/L ratio of PMOS	0.8 µm / 0.128 µm
W/L ratio of NMOS	0.4 µm / 0.128 µm

3.6.5 Comparator

Comparator is a digital block that compares two input signals and outputs a single digital signal, either is "1" (HIGH state) or "0" (LOW state). It typically consists of two input terminals, denoted as V+ and V-, and an output terminal as illustrated in Figure 3.13. When V+ is greater than V-, VOUT outputs HIGH; When V+ is smaller than V-, VOUT outputs LOW. Such a unit will be mainly used in generating PWM signals for the switching transistor in DC-DC converter and controlling the switching of NMOS pass transistors in switch controller block.

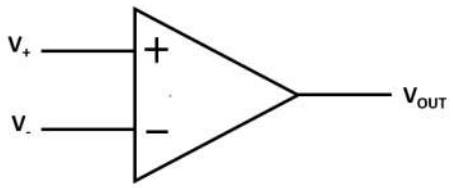


Figure 3.13: Symbol of Digital Comparator

Figure 3.14 shows the building blocks of the comparator adopted from Hathwalia (2014). The pre-amplifying block, as shown in Figure 3.15, is basically a differential amplifier that outputs I_{O+} and I_{O-} by amplifying the

difference between V+ and V-. For example, when V+ is greater than V-, MN1 conducts more current than MN2. Since MP1 and MP3 form a current mirror, MP3 should mirror the current flowing through MP1 and MN1. The mirrored current I_{O+} is expected to be larger than half of I_{REF}, and thus resulting I_{O+} to be greater than I_{O-}.

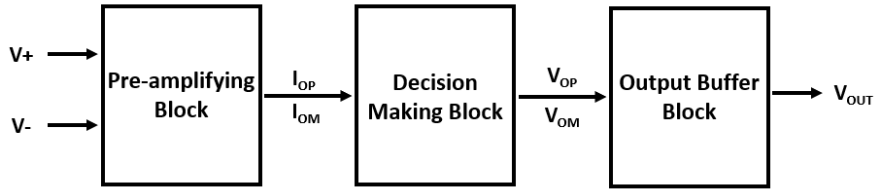


Figure 3.14: Three Blocks of Proposed Comaparator

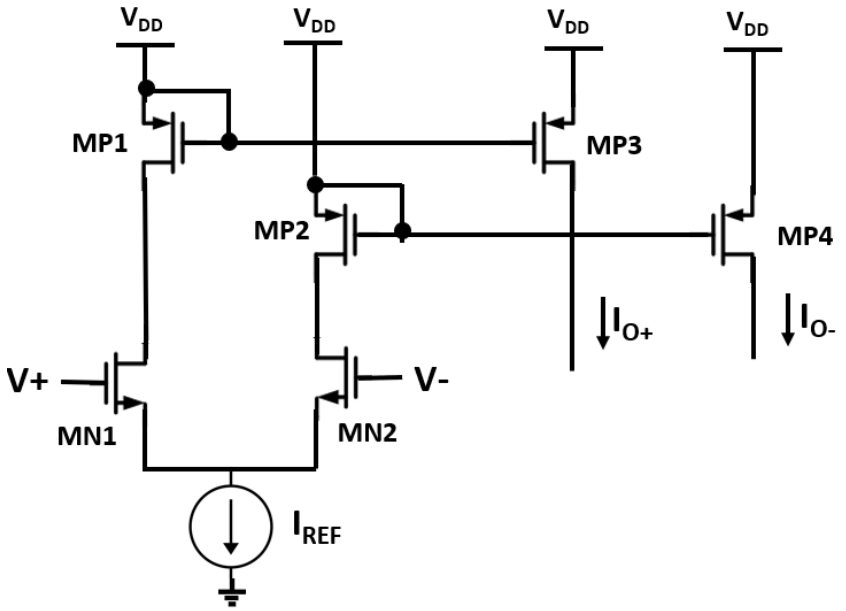


Figure 3.15: Schematic of Pre-Amplifying Block

The decision-making block, as shown in Figure 3.16, determines the sensitivity of the comparator. When I_{O+} is significantly greater than I_{O-}, MN3 and MN5 turn ON, while MN4 and MN6 turn OFF. Under this condition, since the gate and drain terminals of MN3 are shorted together, the values of V_{O+} and V_{O-} are given by:

$$V_{O+} = \sqrt{\frac{2I_{O+}}{\mu_0 C_{ox}(\frac{W}{L})_{MN3}}} + V_{THN} \qquad (3.4)$$

$$V_{O-} \approx 0 \qquad (3.5)$$

As MN3 and MN5 (so as MN4 and MN6) form a current mirror, the relationship between I_{O+} and I_{O-} can be represented as

$$\frac{I_{O-}}{I_{O+}} = \frac{(\frac{W}{L})_{MN5}}{(\frac{W}{L})_{MN3}} = \frac{(\frac{W}{L})_{MN6}}{(\frac{W}{L})_{MN4}} \qquad (3.6)$$

The W/L ratio of all NMOS will be set to be equal to obtain non-hysteresis comparator, so that it will respond to any small difference between V_{O+} and V_{O-}.

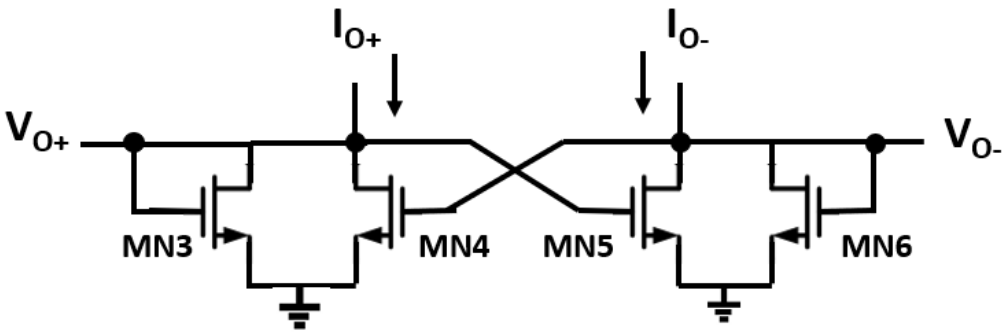


Figure 3.16: Schematic of Decision-Making Block

Due to the limited swing of V_{O+} and V_{O-}, the last stage involves an output buffer which converts those signals to digital outputs. Figure 3.17 shows the output buffer circuit designed by Duwada, Saxena and Baker (2006) for the proposed comparator. This topology also adopts a differential amplifier, the only difference is that MN9 is self-biased which eliminates the need of biasing voltage. In overall, the parameters of the proposed comparator are listed in Table 3.9.

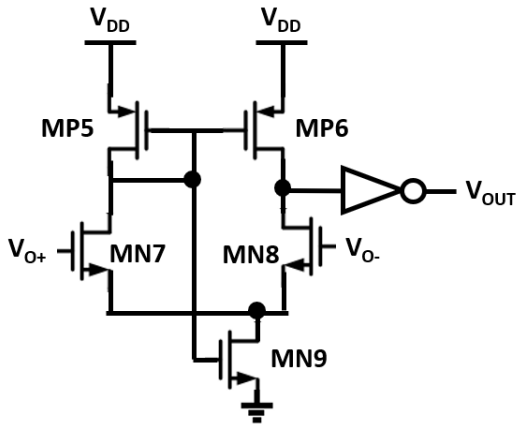


Figure 3.17: Schematic of Output Buffer Block

Table 3.9: Parameters of Proposed Comparator

Parameter	Value
Operating voltage	1 V
Reference Current I_{REF}	10 nA
W/L ratio of NMOS	0.32 µm / 64 nm
W/L ratio of PMOS	0.63 µm / 64 nm

3.6.6 Ramp Generator

Ramp signal, also known as sawtooth signal, is required in producing PWM signal to control the switching of transistors in the DC-DC converter. Based on Figure 3.18, an ideal ramp signal consists of a slow rising voltage followed by an immediate fall of voltage. The main idea of generating a ramp signal involves the initial charging of a capacitor with a current source. Once a specific voltage is reached, a transistor connecting across the capacitor is turned ON to allow the current being discharged to the ground. When the voltage drops to 0 V, the transistor is turned OFF which allows the procedure to repeat.

Figure 3.18: Waveform of Ramp Signal

Figure 3.19 shows the proposed schematic of the ramp generator block. Two sinusoidal signals with slightly different phases, formed by the designed VCO, are fed into the inputs of AND gate, resulting in an output digital signal with a short pulse width. The AND gate is built using CMOS as shown in Figure 3.20. It is important to minimise the pulse width of the signal. In fact, as shown in Figure 3.21, the pulse width corresponds to the time interval of each cycle, thus reducing it as much as possible will form an almost ideal ramp signal. The generated signal is then used to turn ON the MN1 for the current of C1 to discharge through it. Table 3.10 shows the design specifications and parameters of the ramp generator.

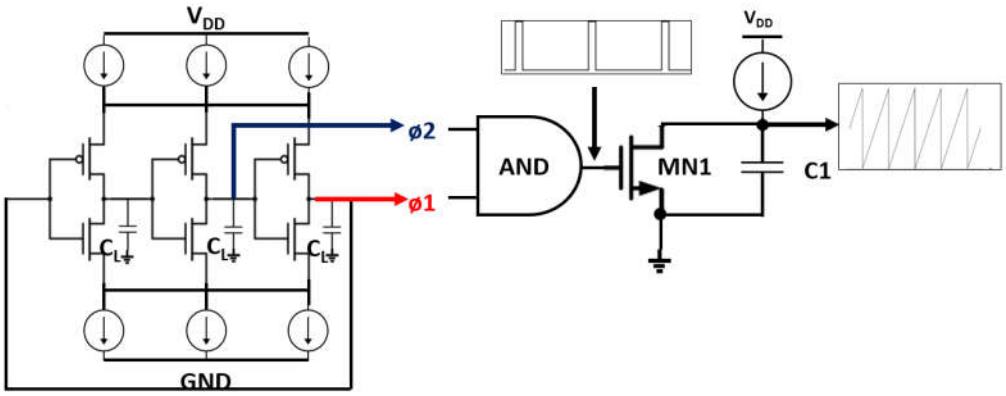


Figure 3.19: Schematic of Proposed Ramp Generator

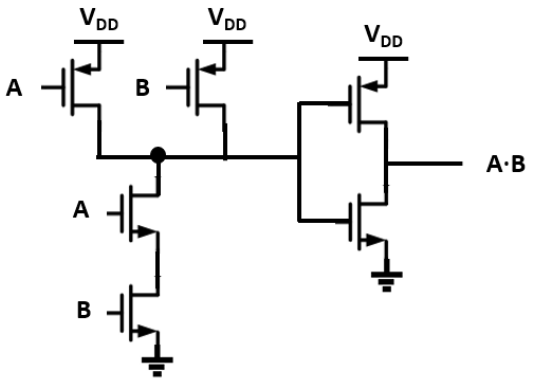


Figure 3.20: Schematic of 2-Input AND Gate

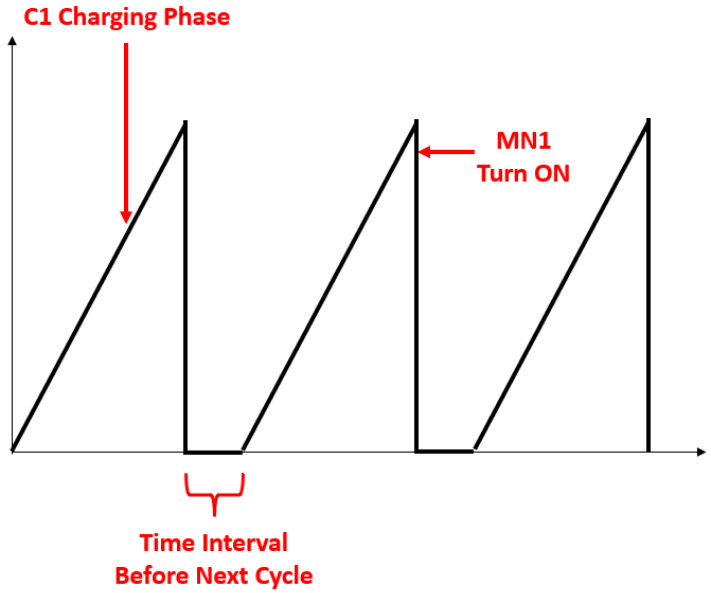


Figure 3.21: Theoretical Ramp Signal Formed by Proposed Design

Table 3.10: Design Specification and Parameters of Ramp Generator

Parameter	Value
Operating voltage	1 V
Reference current	80 nA
Frequency of ramp signal	10 kHz
Amplitude of ramp signal	1 V
W/L ratio of NMOS for AND gate	0.2 µm / 1 µm

W/L ratio of PMOS for AND gate	0.8 µm / 0.128 µm
W/L ratio of NMOS for NOT gate	0.1 µm / 1 µm
W/L ratio of PMOS for NOT gate	0.8 µm / 0.128 µm
W/L ratio of MN1	0.1 µm / 64 nm
C1	7 pF

3.6.7 NMOS Switch Controller Unit

The NMOS switch controller unit is designed to manage the power flow between the primary storage containing the harvested energy and input of the DC-DC converter. It is done by outputting digital signal to the gate of the NMOS pass transistor, which is large in size for low turn-on resistance.

The schematic of the switch controller unit is depicted in Figure 3.22, which comprises three comparators, with a fixed reference voltage of 0.1 V at each positive terminal. NMOS is specifically chosen over PMOS as it has relatively lower turn-on resistance due to it having higher electron mobility. As described earlier, each comparator will continuously monitor the voltage across the primary storage. When the voltage level exceeds 0.1 V, the current stored from the harvester will be transferred to the DC-DC converter for voltage conversion purposes. By default, the NMOS pass transistor will be in OFF state by setting 0 V at its gate terminal.

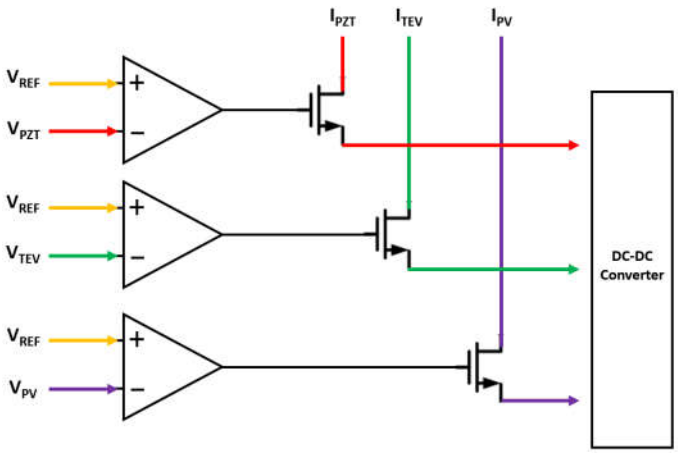


Figure 3.22: Schematic of Proposed Switch Controller

3.6.8 DC-DC Converter

The proposed DC-DC converter deploys the boost regulator topology which steps up the output voltage of each harvester to a higher voltage level. It should be noted that the PMIC in this project will solely generate a fix output voltage level of 1 V, to four different loads as mentioned in the earlier section.

Figure 3.23 depicts the 4-input boost converter with a potential divider circuit at its output node. The inductance value of the shared inductor should be kept within a reasonable range, to keep the converter to operate in discontinuous current mode (DCM). By doing so, it could reduce the average switching loss, which may ultimately lead to higher power transfer efficiency. The function of a diode in boost converter is to avoid reverse current flow from load to the input side. Instead of using a typically used diode, a diode connected PMOS (by shorting its gate and drain terminals together) is utilised to minimise the overall size of the design.

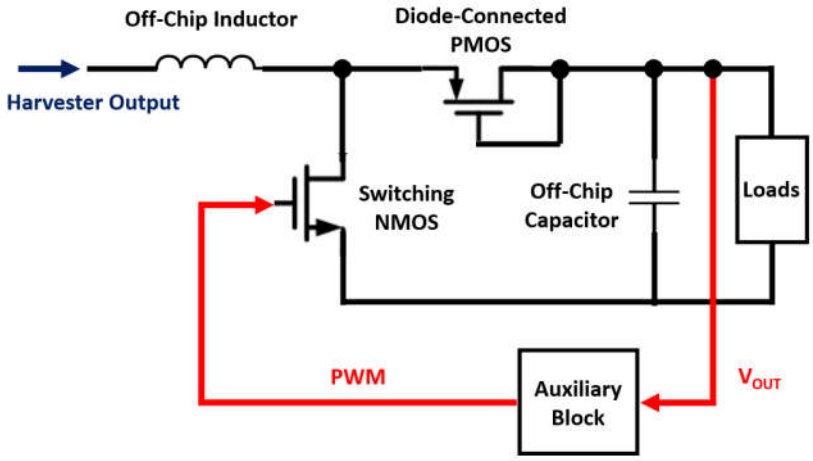


Figure 3.23: Schematic of Proposed Boost Converter

An auxiliary block, with its detailed block diagram shown in Figure 3.24, maintains the output voltage at 1 V by sampling the voltage and outputs PWM signal to control the switching transistor. Potential divider circuit is made up of multiple diode-connected NMOS connecting in series. It is often desirable to use NMOS with a small W/L ratio minimise the current loading effect during sampling. The PWM signal is then formed by comparing the ramp signal with the sampled voltage.

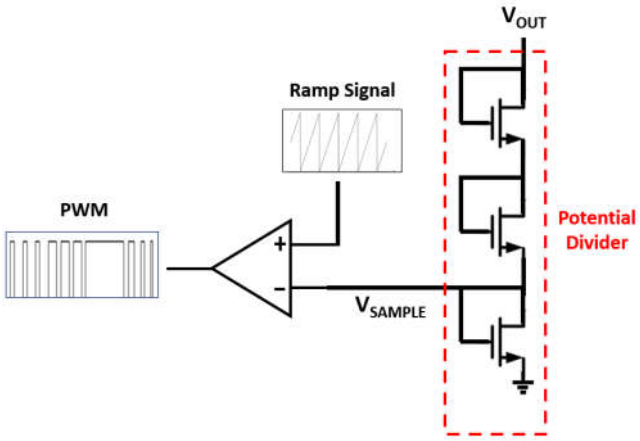


Figure 3.24: Schematic of Proposed Auxiliary Block

Table 3.11: Design Specifications and Parameters of Proposed Boost Converter

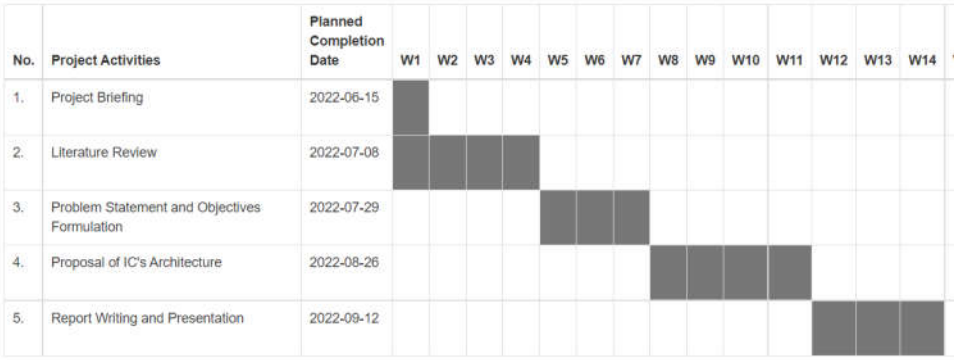
Parameter	Value
Output voltage	1 V
Output current	36 – 368 µA
ON-Resistance of Switching NMOS	≤ 1 Ω
W/L ratio of Diode-Connected PMOS	980 µm / 32 nm
Off-Chip Inductance	50 µH
Off-Chip Capacitance	2.22 µF
Frequency of PWM signal	10 kHz

3.7 Project Planning

In general, this project is divided into two stages. The first stage mainly focuses on reviewing the past research related to the design of PMIC features with energy harvesting, as well as proposing the architecture of the PMIC to achieve the pre-mentioned objectives. Figure 3.25 shows the Gantt chart of the first stage of the project. Total duration of the first stage is 14 weeks, starting from 15th June 2022 to 12th September 2022.

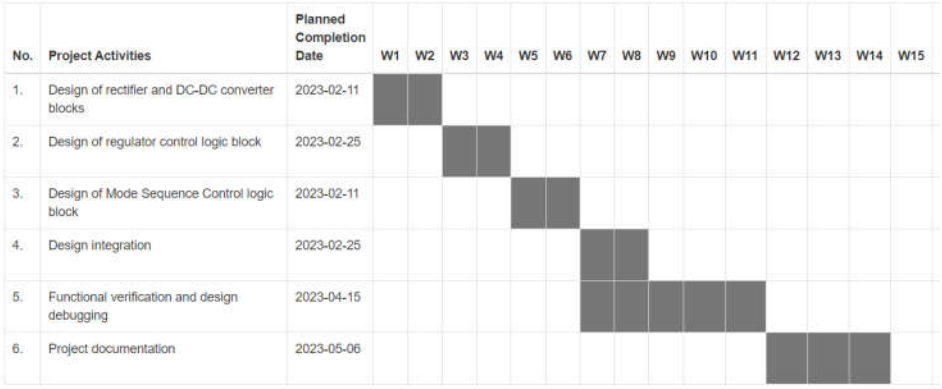
The second stage involves the real implementation of PMIC design using the LTspice simulator software. Figure 3.26 shows the Gantt chart of the

second stage of the project. Similarly, the total duration of this stage is 14 weeks, starting from 11th February 2023 to 6th May 2023.



No.	Project Activities	Planned Completion Date	W1	W2	W3	W4	W5	W6	W7	W8	W9	W10	W11	W12	W13	W14
1.	Project Briefing	2022-06-15														
2.	Literature Review	2022-07-08														
3.	Problem Statement and Objectives Formulation	2022-07-29														
4.	Proposal of IC's Architecture	2022-08-26														
5.	Report Writing and Presentation	2022-09-12														

Figure 3.25: Gantt Chart of the First Stage of Project



No.	Project Activities	Planned Completion Date	W1	W2	W3	W4	W5	W6	W7	W8	W9	W10	W11	W12	W13	W14	W15
1.	Design of rectifier and DC-DC converter blocks	2023-02-11															
2.	Design of regulator control logic block	2023-02-25															
3.	Design of Mode Sequence Control logic block	2023-02-11															
4.	Design integration	2023-02-25															
5.	Functional verification and design debugging	2023-04-15															
6.	Project documentation	2023-05-06															

Figure 3.26: Gantt Chart of the Second Stage of Project

Before designing the system, the output waveforms of ambient energy harvesters are determined as those will be used as inputs to the PMIC. The proposed PMIC is divided into multiple blocks, with each block having its unique functionalities. During the design stage of each block, its schematic will be built using the ideal analogue and digital components provided by the software library. This step is important to verify the practicality of the concept. Once the concept is verified, the schematic will be further designed using the 32 nm CMOS model provided by the PTM. In other words, this process involves converting the schematic into a transistor-level schematic using CMOS technology. The schematic will then be tested to ensure its functionality and output characteristics match with the design specifications. Once all the block prototypes are finished, the blocks will be integrated

together to verify any faults that may occur. Optimisations are made on the PMIC to further improve its performance. The procedures of the PMIC design are summarised as shown in Figure 3.27.

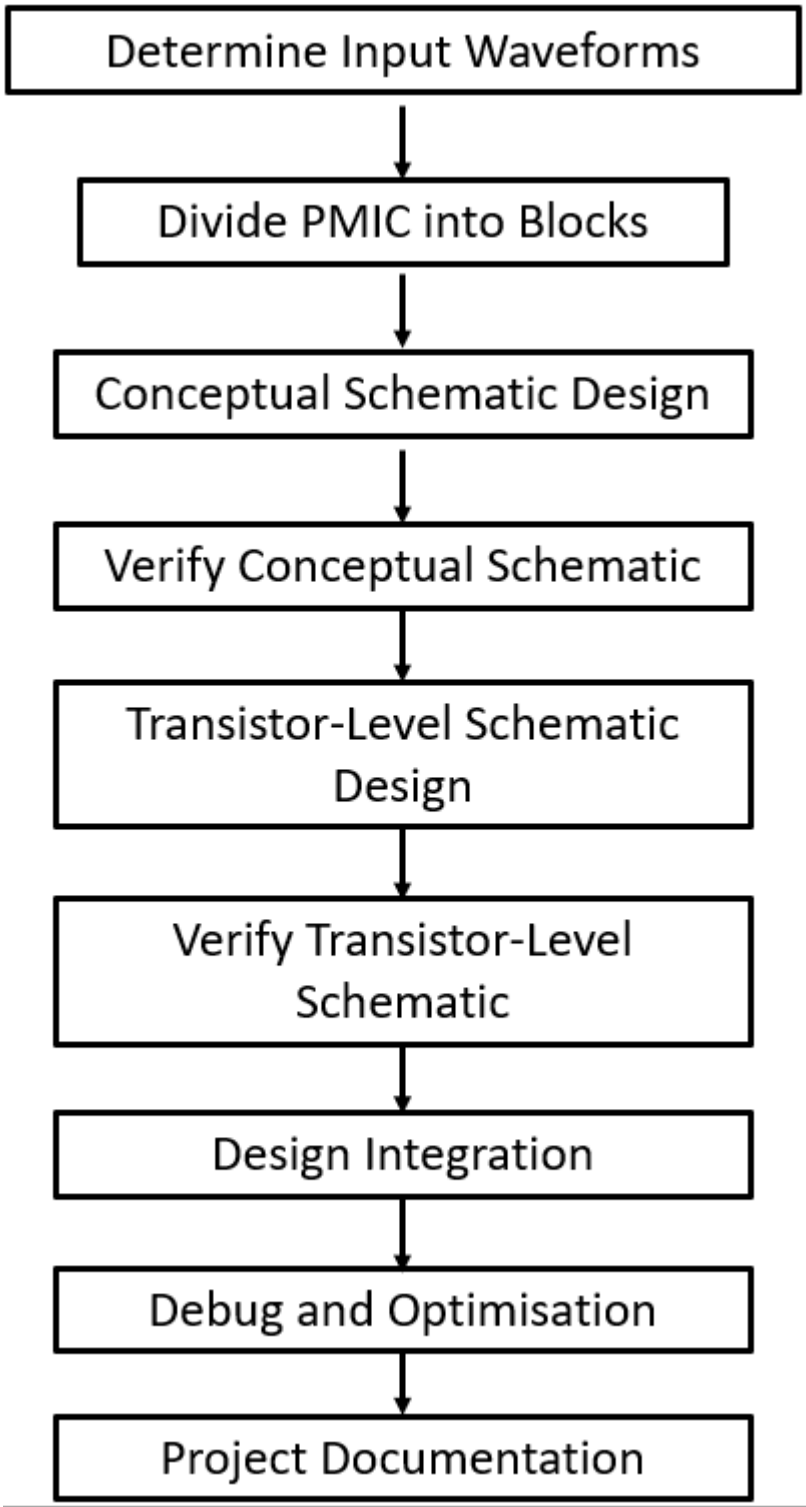


Figure 3.27: Flowchart of PMIC Design Stage

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Introduction

There were a total of eight blocks being introduced in the previous chapter. Each of the blocks was designed using the PTM 32 nm CMOS technology. This chapter will first cover the evaluation on each of the blocks within the proposed PMIC. Once all of the designed blocks match with the pre-defined specifications, a final stage of evaluation and optimisation will be made on the integrated design. Besides measuring the output power generated by the designed PMIC, its total power consumption will also be measured, which will be compared with other PMICs that were proposed in the past studies.

4.2 Evaluation on Analog and Digital Blocks

4.2.1 Charge Pump

The proposed CMOS-based 4-stage charge pump circuit is shown in Figure 4.1. The capacitance of C1 to C7 is set to be a small value so that the design can produce an output voltage within a short amount of time. Each of the diodes was replaced with diode-connected NMOS to reduce the forward voltage drop during the rectification process.

Table 4.1 presents the simulation results when the charge pump was fed with input RF power from -25 to 0 dBm, under two different loading conditions. As the input power increases, the settling time $T_{settling}$ reduces significantly, indicating shorter time taken for the output voltage to reach a stable state. Considering the charge pump being loaded with 1 MΩ, the output voltage initially increased from 0.707 V to 1.035 V. The output voltage started to decrease to 0.873 V when its input power was further increased. This trend may be due to the fact that the output had exceeded the maximum voltage capability, although the output current had increased. In general, the overall output voltage under loaded condition (1 MΩ) was relatively lower that the output under unloaded condition, due to the current drawn by the presence of load.

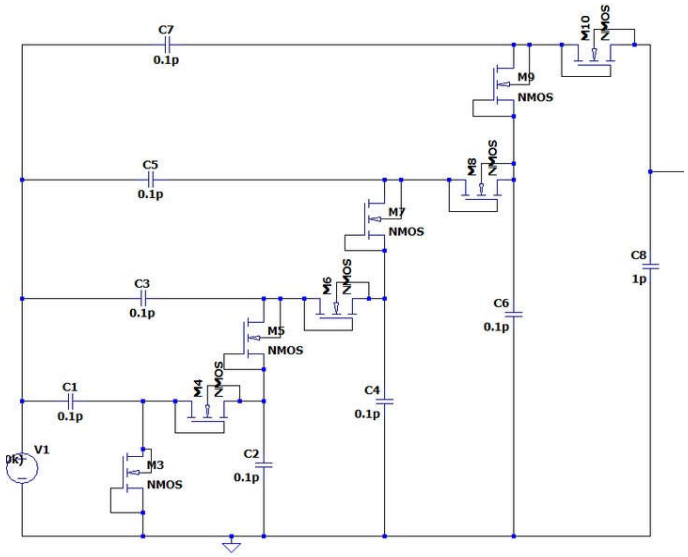


Figure 4.1: Schematic Design of 4-Stage Charge Pump

Table 4.1: Simulation Results Under Unloaded and Loaded Conditions

	$R_L = \infty$		R_L = 1 Mc	
P_{IN} (dBm)	**V_{DC} (V)**	**$T_{Settling}$ (ns)**	**V_{DC} (V)**	**$T_{Settling}$ (ns)**
-25	1.045	1560	0.707	810
-20	1.094	580	0.960	500
-15	1.093	225	1.035	230
-10	1.050	100	1.030	100
-5	0.985	52	0.975	46
0	0.875	32	0.873	29

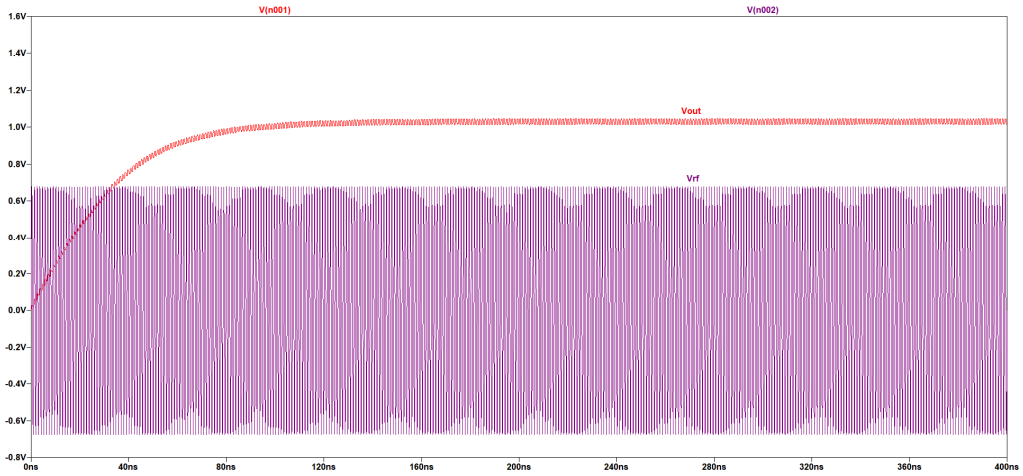


Figure 4.2: Output Waveforms of Charge Pump (Denoted as V_{out}) given with Input Voltage of 1.354 V_{PP} (Denoted as V_{rf})

4.2.2 CCDD Rectifier

The CCDD rectifier was tested with PZT input voltage of 2.42 V_{PP}, and its simulation results were tabulated in Table 4.2. As the loading resistance R_L increased from 10 kΩ to 100 kΩ, the rectified voltage also increased from 0.613 V to 0.620 V. Under this condition, the current flowing out from the output was reduced, resulting in a slower charging rate for the loading capacitor C1. Hence, this causes the rising in the ripple output voltage V_{RIPPLE}.

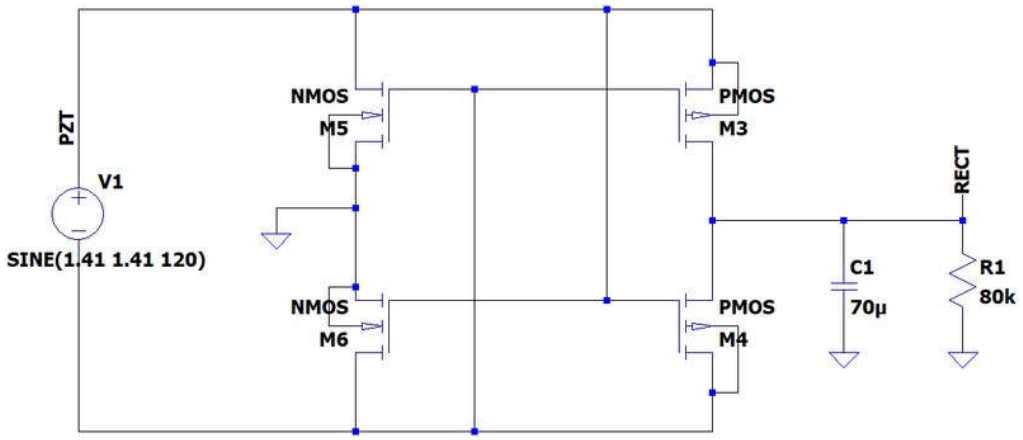


Figure 4.3: Schematic Design of CCDD Rectifier

Table 4.2: Simulation Results of CCDD Rectifier

R_L (kΩ)	V_{RECT} (V)	V_{RIPPLE} (mV)
10	0.613	21.933
30	0.618	23.779
50	0.619	23.945
80	0.620	24.202
100	0.620	24.287

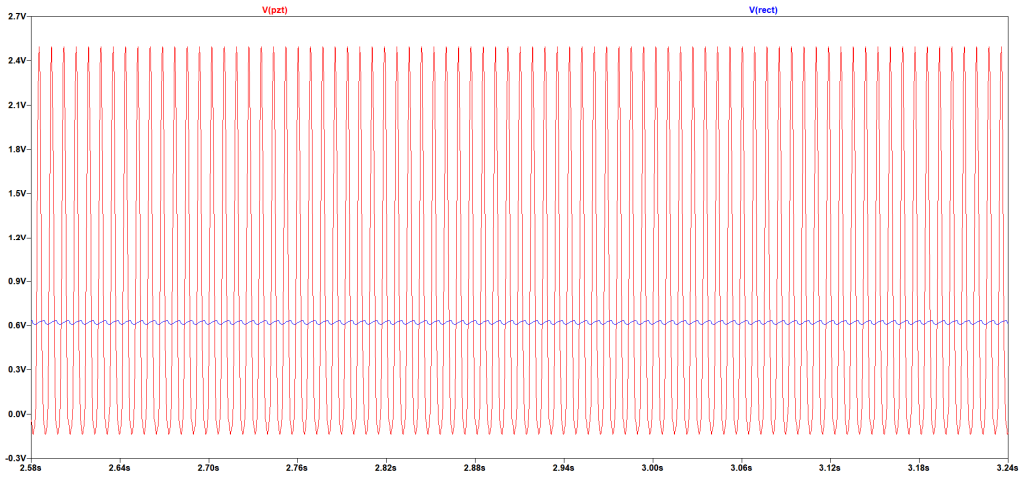


Figure 4.4: Output Waveform of CCDD Rectifier (Denoted as V_{rect}) given with Input Voltage V_{pzt} of 2.42 V_{PP}

4.2.3 Bandgap Core

Figure 4.5 shows the schematic of the proposed bandgap core circuit. M1 and M4 formed an operational amplifier that responds to the difference in drain voltage at M7 and M8, to ensure the current flowing through R1 is the same as the current flowing through M7. Since the required gate voltage of M7 should be higher than that of M8, three NMOS with similar sizing (M9 to M11) were connected in parallel with M8 to reduce its effective threshold voltage. Furthermore, M12 and M13 were connected in such ways to function as capacitors, ensuring smooth output voltages for biasing purposes.

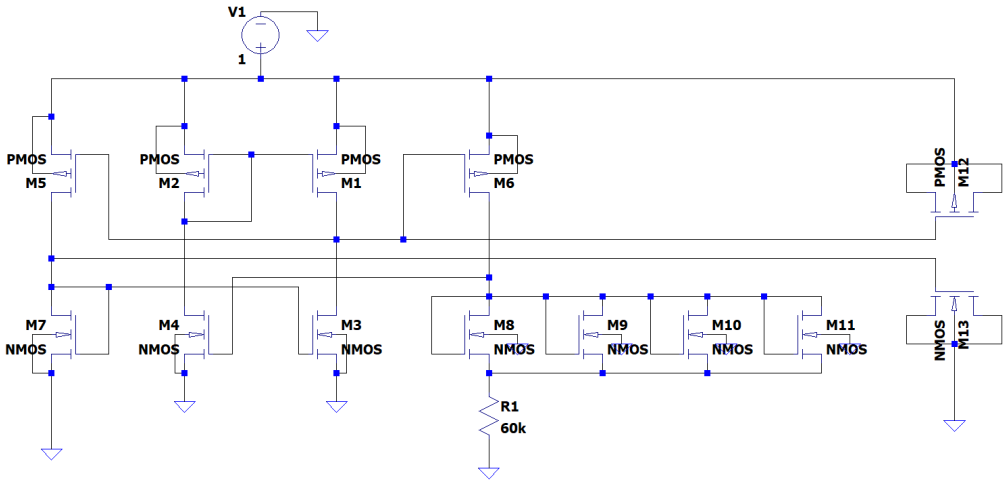


Figure 4.5: Schematic of Bandgap Core

The designed bandgap core was then tested under temperature varied from 283 K (10 ºC) to 323 K (50 ºC). Based on Figure 4.6 and Table 4.3, the reference current IREF increases from 0.917 µA to 1.036 µA. These results indicates that the proposed bandgap has a positive temperature coefficient of 2.983 nA/K. If the value of R1 is altered to 1 kΩ, the design had shown a negative temperature coefficient of -0.537 nA/K, which was due to the fact that the temperature coefficient of M8 dominated the coefficient of R1.

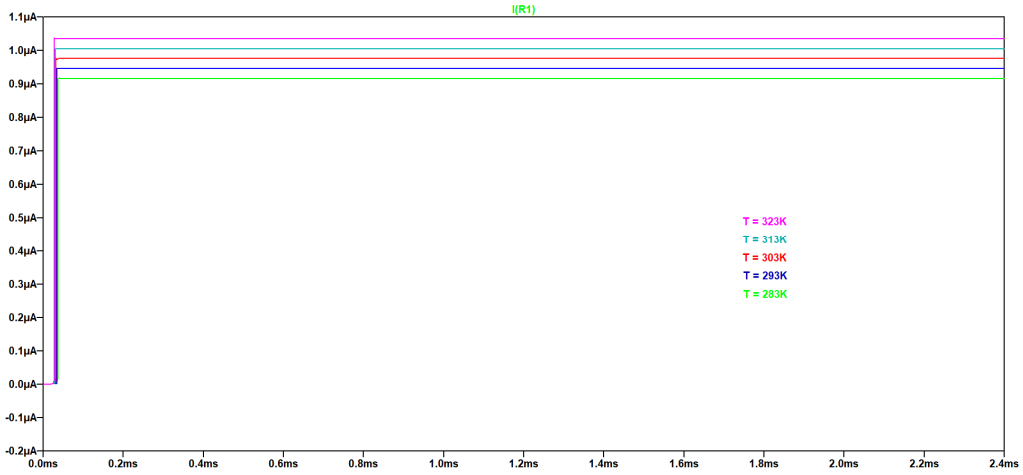


Figure 4.6: Reference Current Under Temperature Variation

Table 4.3: Tabulation of Results Under Temperature Variation

	Reference Current I_{REF} (µA)	
Temperature (K)	**R1 = 60 kΩ**	**R1 = 1 kΩ**
283	0.917	69.890
293	0.946	63.340
303	0.976	57.620
313	1.006	52.760
323	1.036	48.400

Next, with the value of R1 fixed at 60 kΩ, the bandgap was tested under the supply voltage was varied from 0.5 V to 2.5 V. Based on Figure 4.7, the design started to supply a constant I_{REF} of 966.8 nA at 0.6 V. When the supply voltage exceeded 1.3 V, I_{REF} was no longer kept at constant value and started to increase beyond it. In general, the optimal operating range for this design is between 0.6 V to 1.3 V.

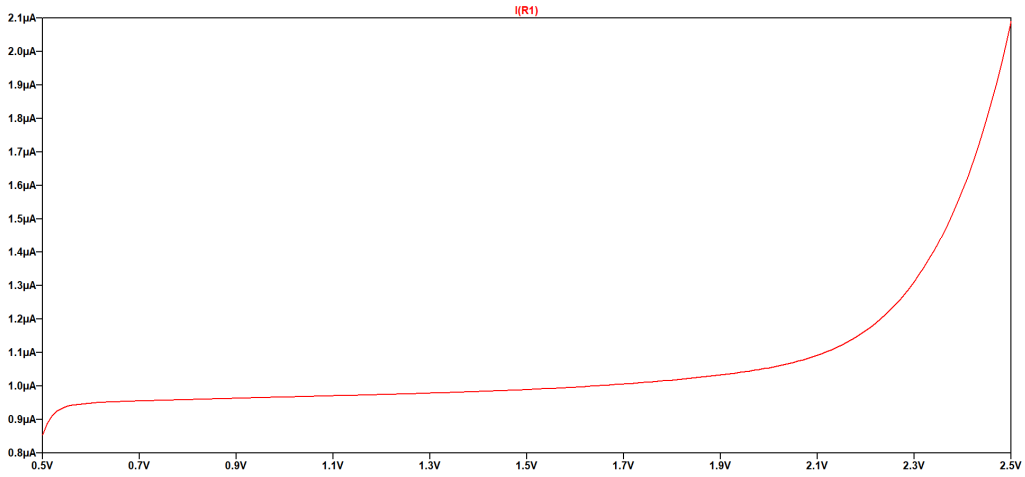


Figure 4.7: Reference Current Under Supply Voltage Variation

4.2.4 Comparator

Figure 4.8 depicts the comparator designed using CMOS, that involves pre-amplifying circuit (M1, M38, M39, M40, M1), decision making circuit (M20, M21, M22, M23, M24, M25) and output buffer circuit (M26, M27, M28, M29,

M30, M31, M32). The reference current sink was modelled by M1, with its gate being biased by the bandgap core.

The designed comparator was tested under two conditions to determine its capability to respond to fast signals. The first condition was setting the reference voltage V_{REF} at 0.3 V, and a sine wave with V_{PP} of 0.5 V oscillating at 10 kHz as the input voltage V_{IN}. Figure 4.9 shows that the comparator responded well to the input signal. However, based on Figure 4.10, there was an offset voltage of 17.51 mV for the comparator to output HIGH, while Figure 4.11 shows an offset voltage of 3.13 mV for the comparator to output LOW. This difference may be due to the M31, a PMOS, has a higher threshold voltage than M32.

When the frequency of the input signal was increased to 100 kHz, as shown in Figure 4.12, the comparator took 481.4 ns to respond to the difference between the signals. Although this is slower than the response time for a 10 kHz signal, it is still considered sufficient for the design's intended use.

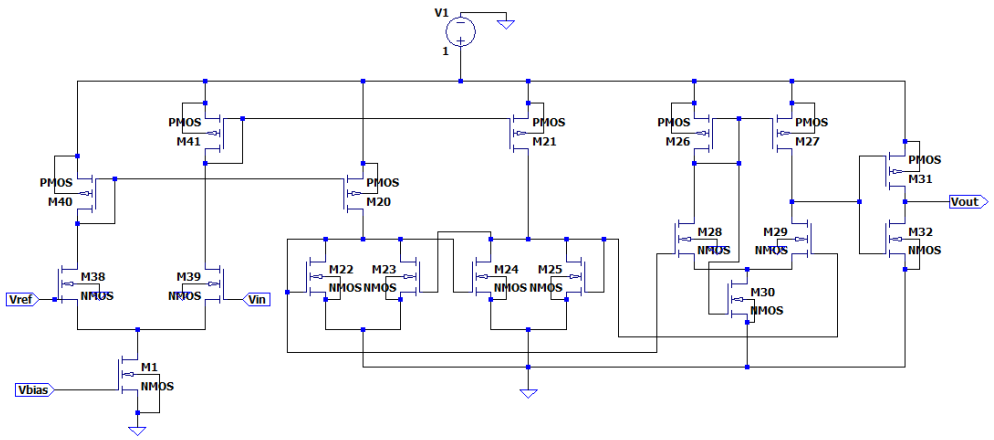


Figure 4.8: Schematic Design of Comparator

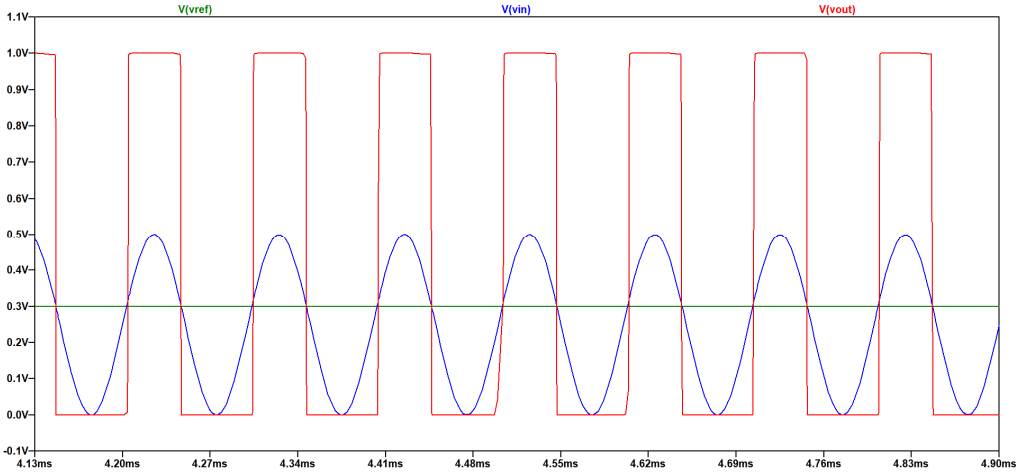


Figure 4.9: Outpus Waveforms of Comparator Under the First Condition

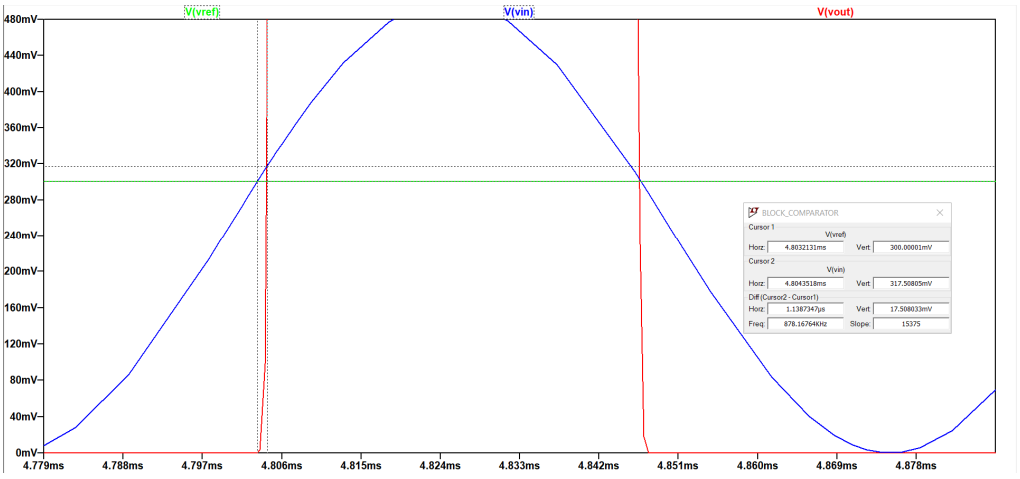


Figure 4.10: Measurement of Offset Voltage to Reach HIGH State

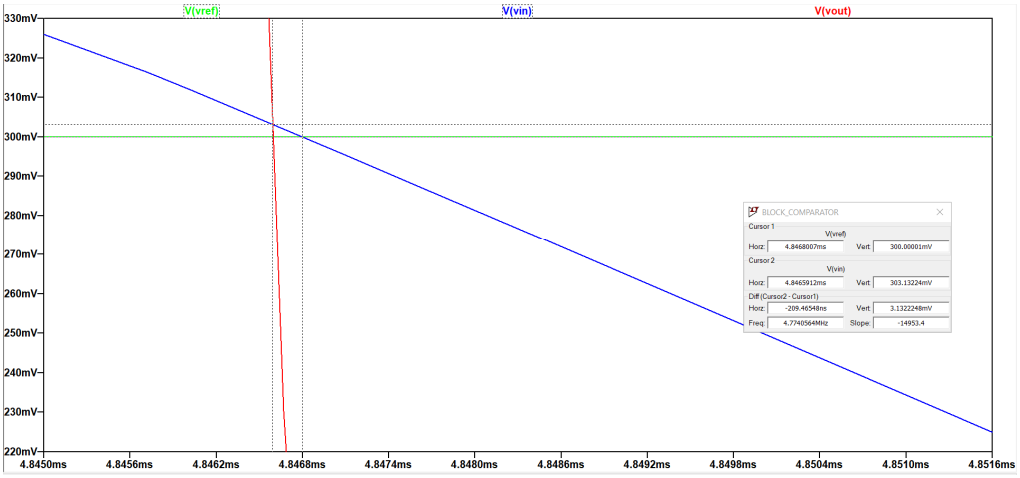


Figure 4.11: Measurement of Offset Voltage to Reach LOW State

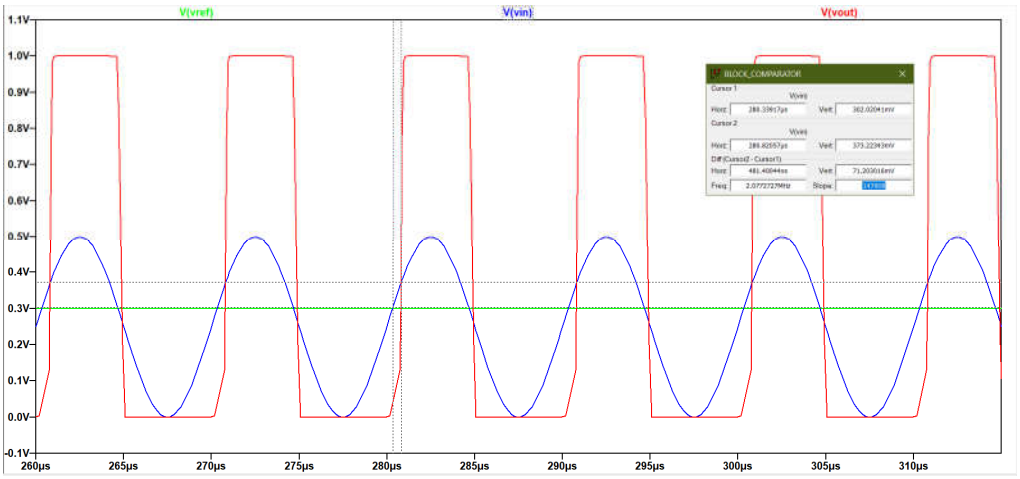


Figure 4.12: Output Waveform Under the Second Condition

4.2.5 Voltage Controlled Oscillator

The schematic designs of a VCO with current limiting feature and a conventional oscillator are shown in Figures 4.13 and 4.14 respectively. By biasing the M2 with voltage at 0.5 V, the current flowing through M1 and M2 is 64.31 nA. M15, M16, M19, M20, M23 and M24 are connected in such a way to mirror the current flow through the M1. Thus, it limits the current consumed by each of the NOT gate.

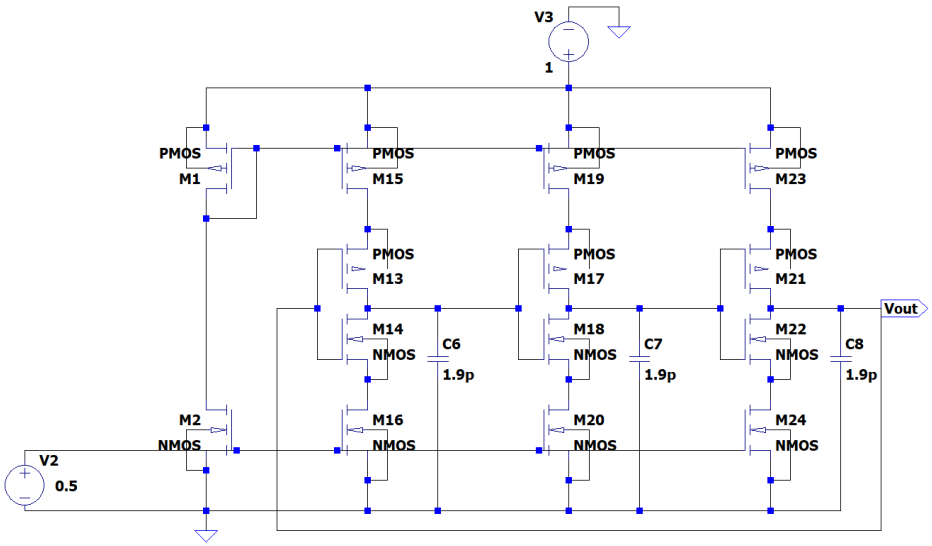


Figure 4.13: Schematic Design of VCO with Current Limiting Feature

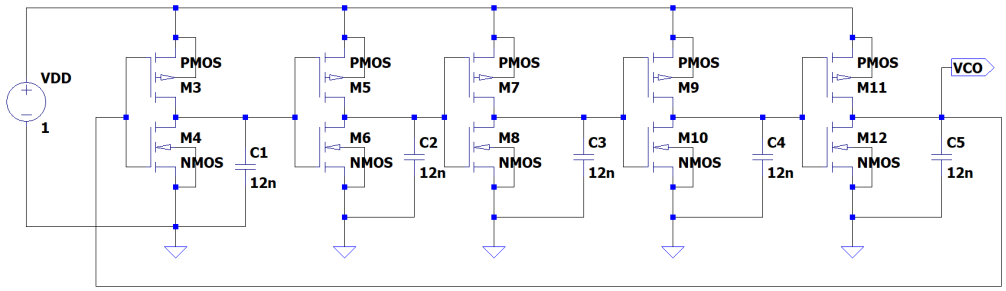


Figure 4.14: Schematic Design of Conventional Oscillator

Based on Table 4.4, both designs had similar results in terms of voltage amplitude and frequency, but the proposed VCO had shown significant lower current consumption as compared with the conventional oscillator. Besides, the value of capacitor required by the proposed design to generate a 10 kHz signal was much lower, indicating that it is smaller in size.

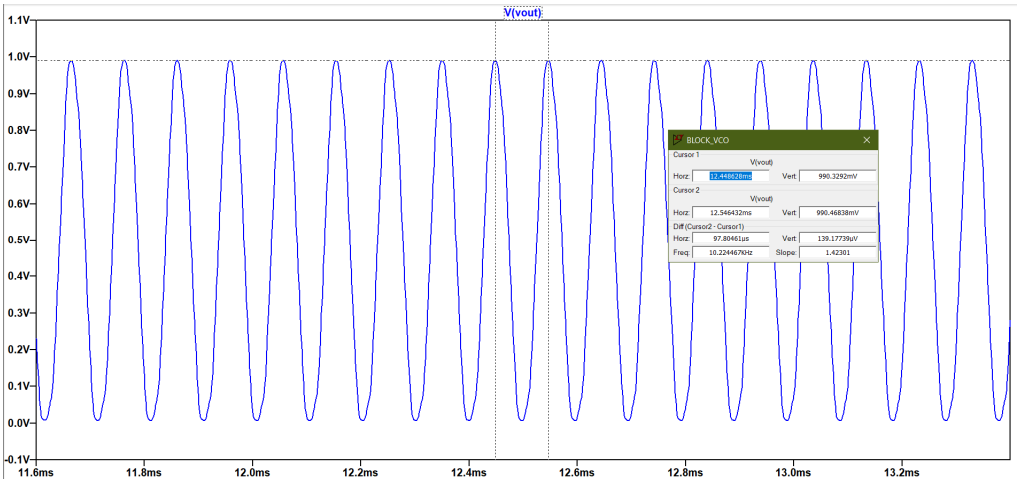


Figure 4.15: Output Waveform of VCO with Current Limiting Feature

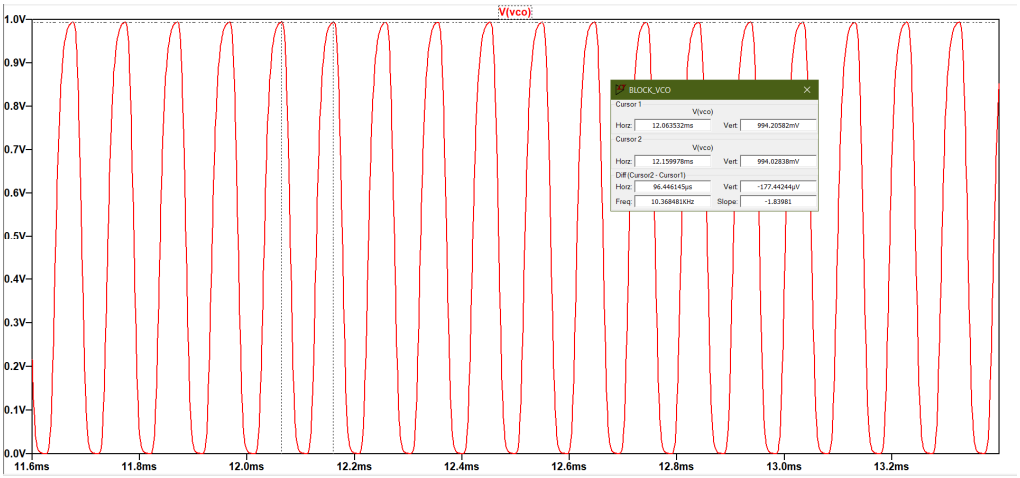


Figure 4.16: Output Waveform of Conventional Oscillator

Table 4.4: Comparison of Conventional Oscillator and Proposed VCO

	Conventional Oscillator	**VCO with Current Limiting Feature**
Amplitude (mV)	994.21	990.47
Frequency (kHz)	10.37	10.22
Current Consumption (µA)	635.56	0.16

4.2.6 Ramp Generator

The designed VCO block was then used in the ramp generator block, as shown in Figure 4.17, to produce two oscillating signals with a slight phase difference. Based on Figure 4.18, the resulting pulse signal had a pulse width of 9.06 µs. M22 was biased to form a 85.53 nA current source, which was used to charge the C4. As a result, the generated ramp signal is shown in Figure 4.19. The pulse width of the pulse signal needed to be reduced as much as possible to minimise the time interval for each subsequent cycle. Figure 4.20 shows that a steeper rising edge of ramp signal was obtained when the value of C4 was increased to 8 pF. However, the amplitude of the signal had decreased to 936.85 mV, which is undesirable as it could reduce the available range of PWM's duty cycle

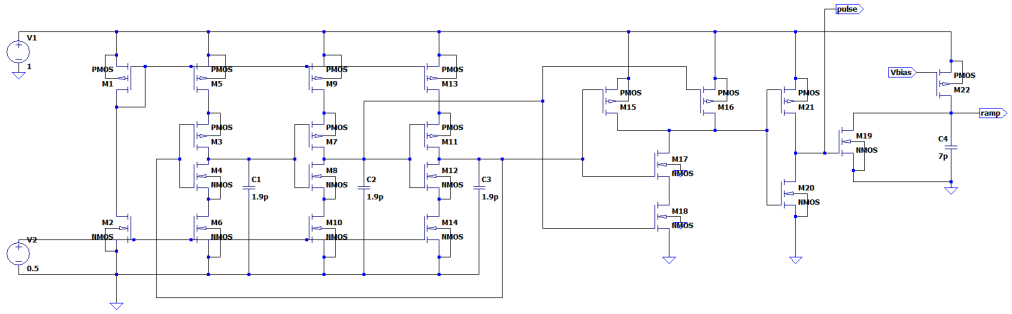


Figure 4.17: Schematic Design of Ramp Generator

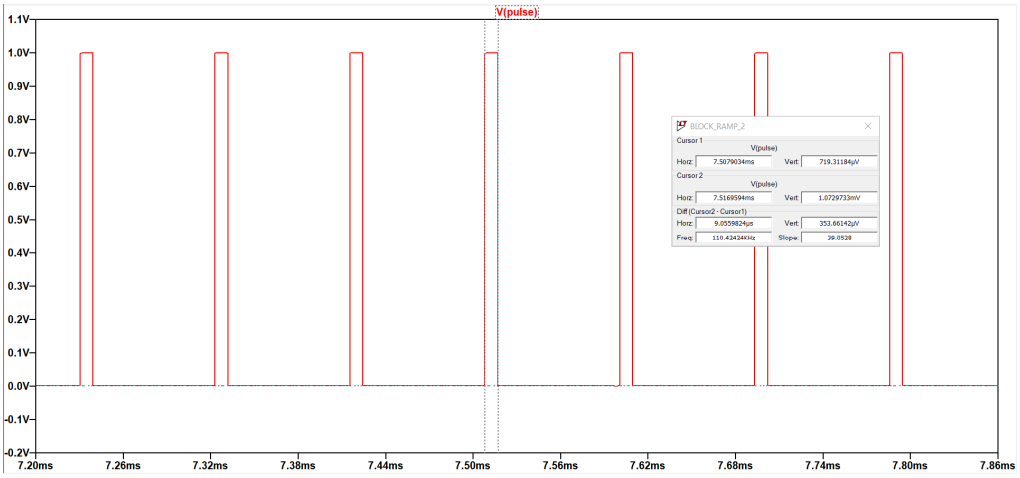


Figure 4.18: Pulse Signal Formed by AND Gate

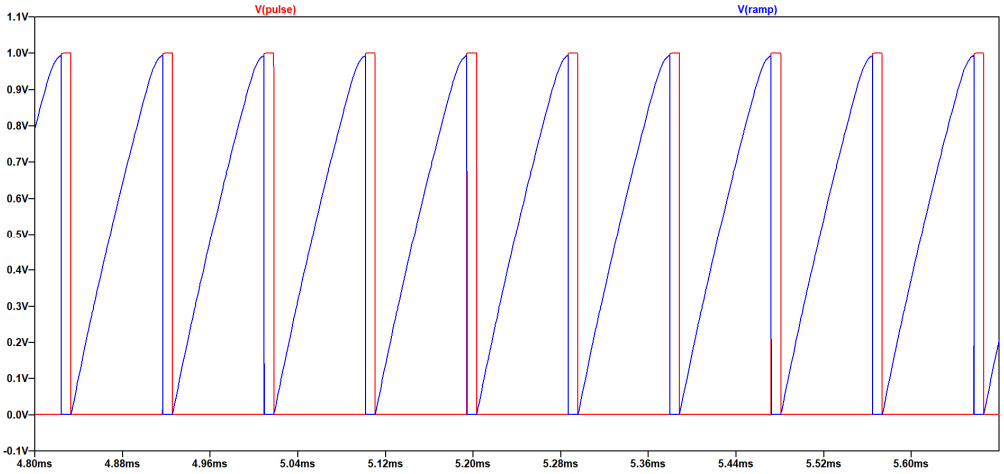


Figure 4.19: Output Ramp Signal When C4 = 7 pF

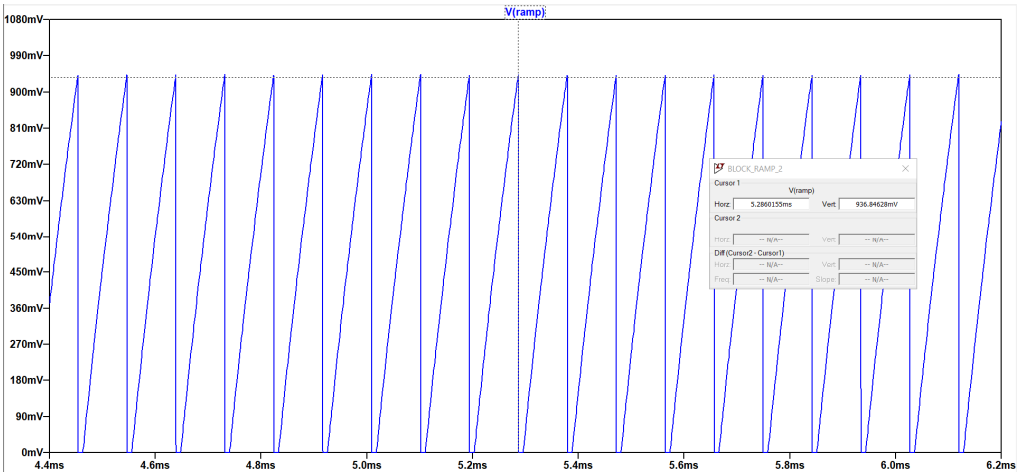


Figure 4.20: Output Ramp Signal When C4 = 8 pF

4.2.7 NMOS Switch Controller Unit

This block basically consisted of three comparators, with each positive terminal connecting to V_{REF} of 0.1 , while each negative terminal connecting to temporary storage of each transducer output. Its schematic is as shown in Figure 4.21. The functionality of such a unit was tested by inserting random source signals denoted as V_{SOURCE_1}, V_{SOURCE_2} and V_{SOURCE_3}. Figures 4.22 to 4.24 show that the designed controller unit is able to respond to the changes in the source signals. Each output of the controller unit was denoted as V_{SW1}, V_{SW2} and V_{SW3}. The HIGH output state was used to turn ON the NMOS pass transistor to allow current flowing from temporary storage into the input of DC-DC converter

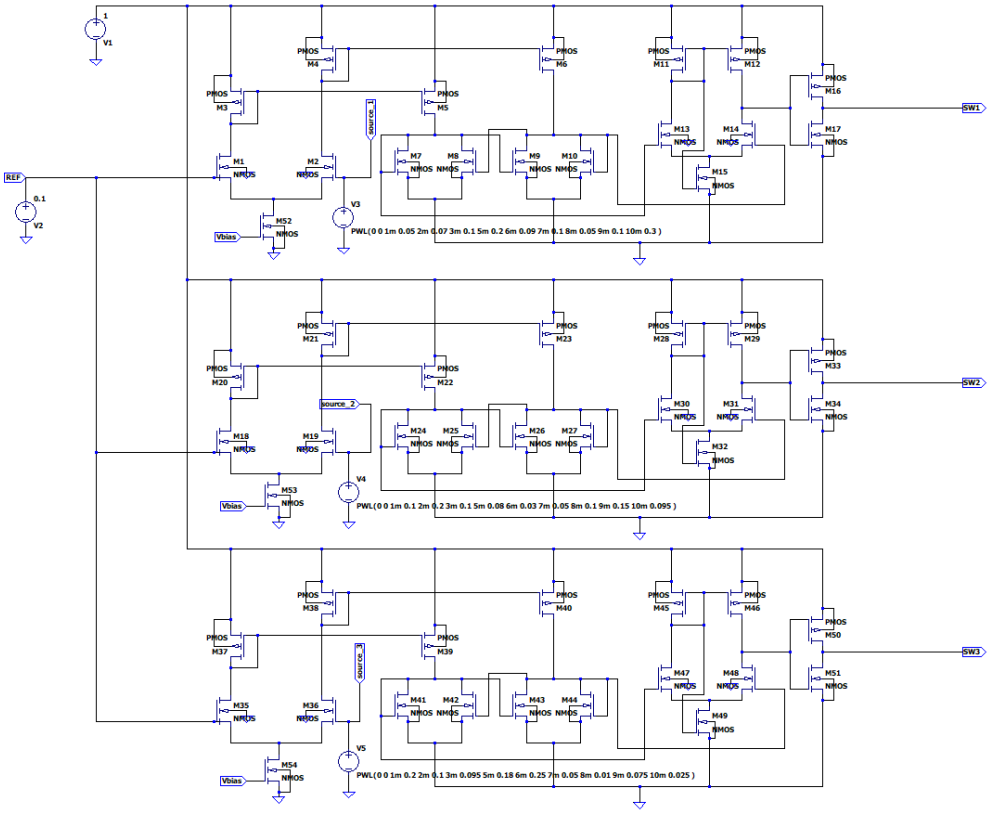


Figure 4.21: Schematic Design of NMOS Switch Controller

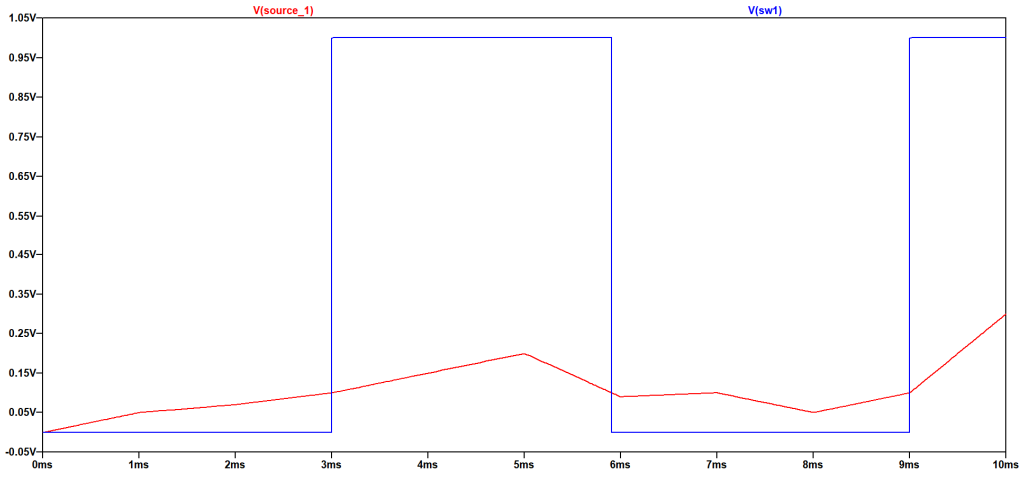


Figure 4.22: Waveform of V_{SW1} Given With V_{SOURCE_1}

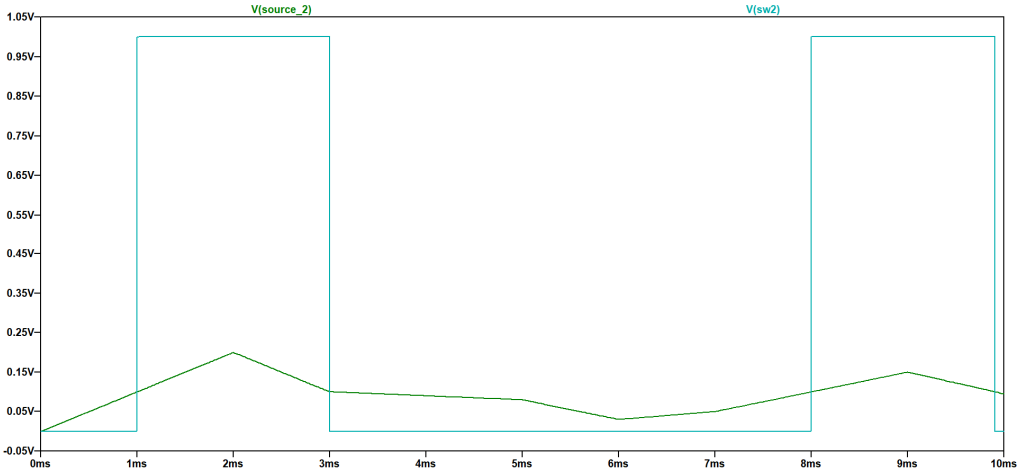


Figure 4.23: Waveform of V_{SW2} Given with V_{SOURCE_2}

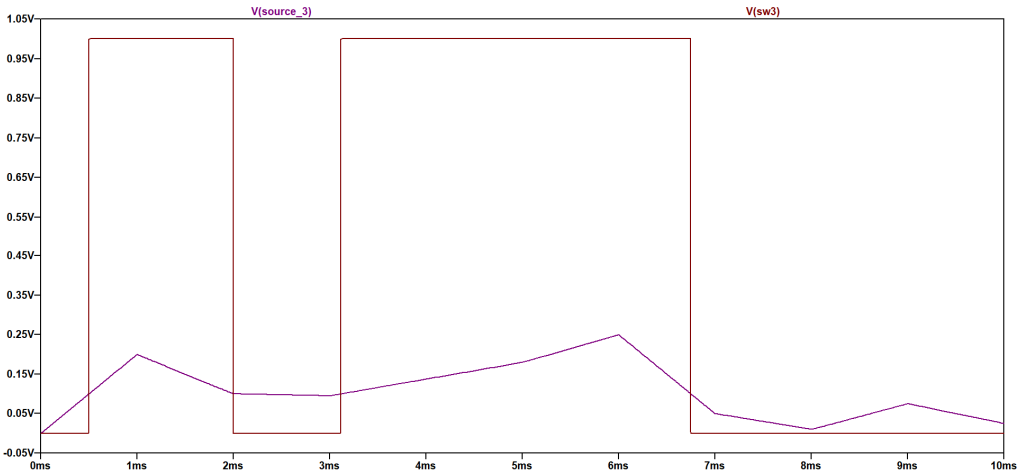


Figure 4.24: Waveform of V_{SW3} Given with V_{SOURCE_3}

4.3 Output Simulation Test

Figure 4.25 shows the schematic design of a DC-DC converter that implements boost regulator topology. R5 to R8 are the equivalent resistances of the selected loads as mentioned in the earlier chapter. This unit was designed to step up its input voltage to a higher voltage level at 1 V. The auxiliary circuit which functions as a feedback circuit is shown in Figure 4.26. A potential divider formed by M64 to M66 samples a portion of the output voltage with minimal current drawn. A designed comparator was used to compare the ramp signal with the sampled output voltage to generate PWM signal. The duty cycle of the PWM signal determines the turn ON time of M125, which is essential to ensure a stable output voltage from the converter.

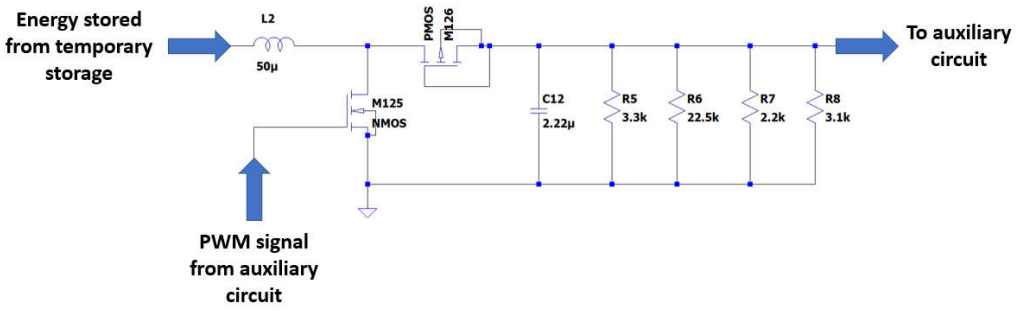


Figure 4.25: Schematic of DC-DC Converter

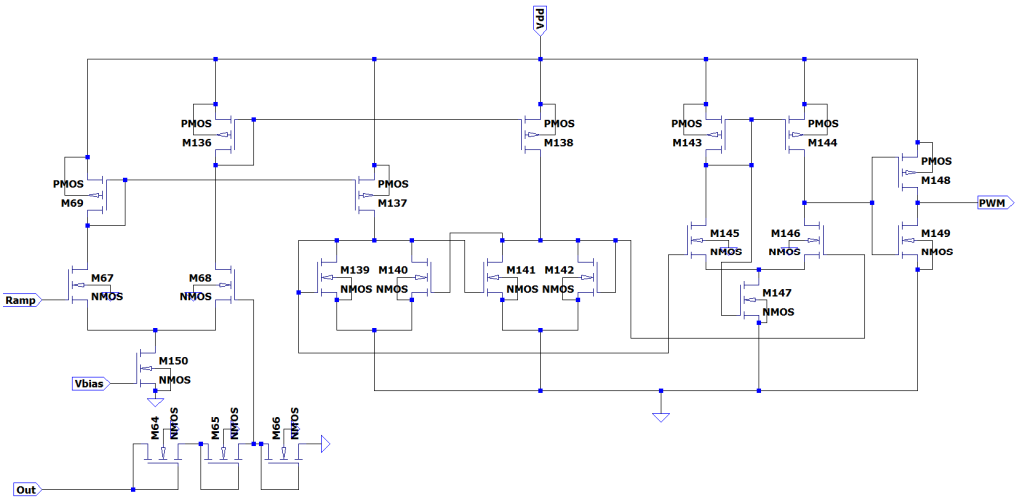


Figure 4.26: Schematic of Auxiliary Circuit

When all blocks are integrated together, the simulation results when loaded with the four selected loads are shown in Figures 4.27 and 4.28. The measured output average voltage was 898.17 mV, with ripple voltage of 33.73 mV. In terms of the output power, Table 4.5 shows that the PMIC was able to supply sufficient power to the selected loads, with total output power of 913.64 µW. The high ripple voltage may be due to the presence of reverse current flow through the M126. The width of M126 was set to be large to reduce the forward voltage drop, however this practice increased the risk of current flowing back from load to the source, which caused the huge fluctuation in output voltage.

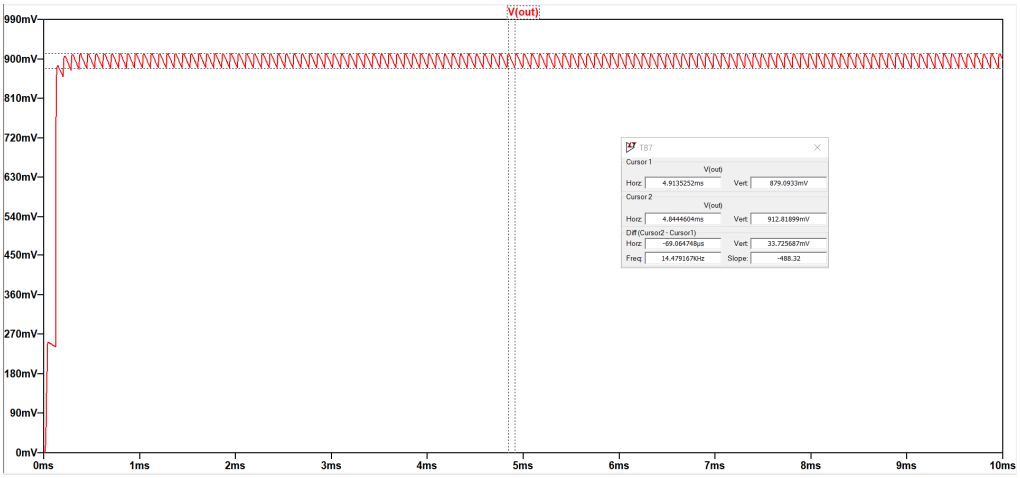


Figure 4.27: Output Voltage of Integrated PMIC

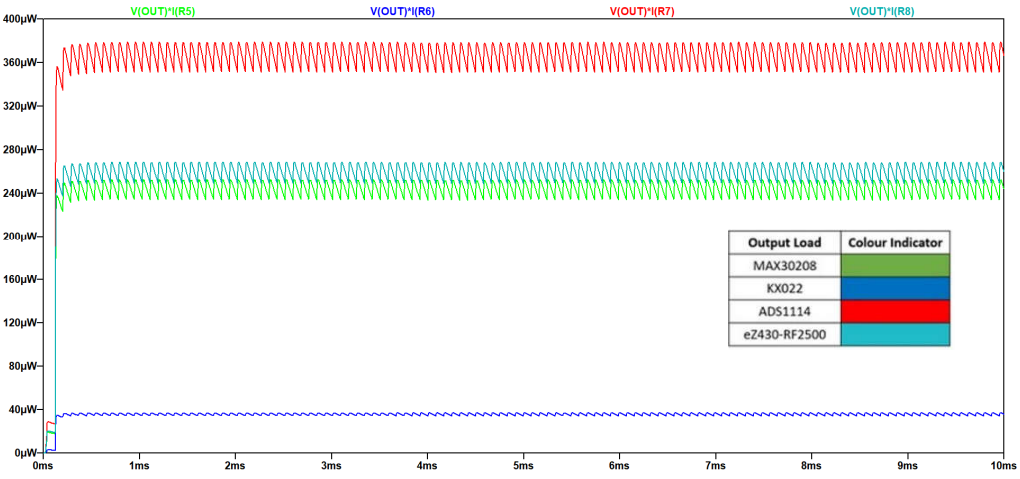


Figure 4.28: Output Power of Integrated PMIC

Table 4.5: Comparison of Load Power Demand and Power Supplied by PMIC

Output Load / Devices	Typical Power Demand (µW)	Power Supplied by PMIC (µW)
MAX30208 Temperature Sensor	241.00	246.18
KX022 Accelerometer	36.00	36.11
ADS1114 A/D Converter	368.00	369.28
eZ430-RF2500 Microcontroller with Transceiver	261.32	262.07

Furthermore, the integrated PMIC was tested under temperature changed from 10 ºC to 50 ºC. When the design was loaded with 22.5 kΩ, the output voltage decreased from 991.78 mV to 931.57 mV, which indicated a negative temperature coefficient of -1.51 mV/ ºC.

Table 4.6: Temperature Test on Integrated PMIC

Temperature (ºC)	Output Voltage (mV) @ Load = 22.5 kΩ
10	991.78
20	976.12
30	960.71
40	946.05
50	931.57

4.4 Power Consumption of PMIC

The power consumption of each designed block is presented in Table 4.7. The bandgap core unit consumed the most current among the other blocks, with a power consumption of 3.96 µW. This is because the bandgap core generates the required voltage and reference current for the rest of the units to operate within the PMIC. To conclude, the total power consumption of the designed PMIC is 5089.14 nW, which can be rounded off to 5 µW. Note that the power consumptions of VCO and AND gate are excluded from the calculation, as both are used within the ramp generator block.

Table 4.7: Power Consumption of Each Block Unit

Blocks	Power Consumption (nW)
Bandgap Core (Beta-Multiplier Circuit)	3962.93
Voltage Controlled Oscillator	155.45
AND Gate	1.96
Ramp Generator	328.52
Comparator	162.36
Potential Divider	148.32
Controller Unit	487.01

4.5 Summary

All blocks within the designed PMIC were evaluated, which included charge pump, CCDD rectifier, bandgap core, comparator, VCO, ramp generator, NMOS switch controller and DC-DC converter with auxiliary circuit. The PMIC was able to supply sufficient power with total output power of 913.64 µW, to the selected loads with total demand power of 906.32 µW. However, its output voltage was measured at 898.17 mV, which is lower than the expected output voltage of 1 V. When loaded with 22.5 kΩ, the design was shown to have a temperature coefficient of -1.51 mV/ ºC. The measured total power consumption was approximately 5 µW, which is considered to be low as compared to other previous works as shown in Table 4.8.

Table 4.8: Comparison of Works

	Zhang et al. (2013)	Huang et al. (2014)	Mui, Khaw and Yasin (2020)	**This Work**
Technology	130nm CMOS	0.35µm CMOS	90nm CMOS	32nm CMOS
Application	Body Sensor Node	Body Sensor Node	General IoT Devices	General IoT Devices
Sources	RF,TEV	RF, PV	RF, PZT	RF, PZT,TEV,PV
Voltage Supply	1.35 V	1.8 V	1.2 V	~1 V
Output Power	19 µW	942.9 µW	396 µW	913.63 µW
Power Consumption	-	45 µW	12 µW	5 µW

CHAPTER 5

CONCLUSIONS AND RECOMMENDATIONS

5.1 Conclusions

Sensor nodes are an important component in IoT networks that are used to collect data from the environment. Long lifespan and small in size become the main criteria in determining its value in the market. However, most sensor nodes are still dependent on the battery as the power supply, which has limited power capacity and also leads to bulky appearance. A passive device or IC with low power consumption can harvest energy from the ambient sources, by integrating a low power PMIC. This project involved the design of a PMIC that features ambient energy harvesting using 32 nm CMOS technology.

The proposed PMIC can be powered by four different ambient transducers, which scavenges energy from sources including RF base station, motion, thermal difference and solar. A total of eight block units were included into the design, which consisted of a charge pump, CCDD rectifier, bandgap core, comparator, VCO, ramp generator, NMOS switch controller and DC-DC converter. The performance of the design was evaluated by supplying power to four kinds of electronic components, including a temperature sensor (MAX30208), an accelerometer (KX022), a signal processor (ADS1114) and a microcontroller with embedded transmitter (eZ430-RF2500).

Based on the evaluation results, it was shown that the design was capable of generating a total output power of 913.64 μW, which excceds the total power demanded by the loads at 906.32 μW. However, the design was only able to generate an average output voltage of 898.17 mV, which is lower than the targeted output voltage of 1 V. The design was subjected to a temperature test when it was loaded with 22.5 kΩ, resulting in a temperature coefficient of -1.51 mV/ ºC.

In conclusion, despite having low power density, it was demonstrated that the ambient sources have potential to be used as alternatives to batteries. The power consumption of electronic components will be reduced along with

the advancement in technology, making it more feasible to integrate those with the energy harvesting in the near future.

5.2 Recommendations for Future Work

Even though the proposed PMIC was able to generate sufficient power to the loads, the output ripple was significant which may cause instability to the electronic components. It is suggested to integrate a low-power low dropout regulator (LDO) to provide a much stable output voltage, as well as to generate multiple voltage levels to support devices with different operating voltage.

Besides, the selected loads were modelled to emulate its average power demand. In practice, a device may have different operating modes, with each drawing a certain amount of current. For future work, the load can be represented with a variable current sink that follows the energy profile, for better accuracy in performance validation.

REFERENCES

Aktakka, E.E. and Najafi, K., 2014. A Micro Inertial Energy Harvesting Platform with Self-Supplied Power Management Circuit For Autonomous Wireless Sensor Nodes. *IEEE Journal of Solid-State Circuits*, *49*(9), pp.2017-2029.

Chowdary, G., Singh, A. and Chatterjee, S., 2016. An 18 nA, 87% Efficient Solar, Vibration and RF Energy-Harvesting Power Management System with a Single Shared Inductor. *IEEE Journal of solid-state circuits*, 51(10), pp. 2501-2513.

El-Nozahi, M., Amer, A., Torres, J., Entesari, K. and Sánchez-Sinencio, E., 2010. High PSR Low Drop-Out Regulator with Feed-Forward Ripple Cancellation Technique. *IEEE Journal of Solid-State Circuits*, 45(3), pp. 565-577.

Huang, Y.J., Tzeng, T.H., Lin, T.W., Huang, C.W., Yen, P.W., Kuo, P.H., Lin, C.T. and Lu, S.S., 2014. A Self-Powered CMOS Reconfigurable Multi-Sensor SoC for Biomedical Applications. *IEEE Journal of Solid-State Circuits*, 49(4), pp.851-866.

Kim, S., Vyas, R., Bito, J., Niotaki, K., Collado, A., Georgiadis, A. and Tentzeris, M.M., 2014. Ambient RF Energy-Harvesting Technologies for Self-Sustainable Standalone Wireless Sensor Platforms. *Proceedings of the IEEE*, 102(11), pp.1649-1666.

Lee, D., Kim, T., Kim, S., Byun, K. and Kwon, K., 2018. A CMOS rectifier with 72.3% RF-to-DC Conversion Efficiency Employing Tunable Impedance matching network for ambient RF energy harvesting. *International SoC Design Conference (ISOCC)*, pp. 259-260.

Leonov, V., 2013. Thermoelectric Energy Harvesting of Human Body Heat for Wearable Sensors. *IEEE Sensors Journal*, 13(6), pp. 2284-2291.

Lhermet, H., Condemine, C., Plissonnier, M., Salot, R., Audebert, P. and Rosset, M., 2008. Efficient Power Management Circuit: From Thermal Energy Harvesting to Above-IC Microbattery Energy Storage. *IEEE Journal of solid-state circuits*, 43(1), pp.246-255.

Liu, Y., Khanbareh, H., Halim, M.A., Feeney, A., Zhang, X., Heidari, H. and Ghannam, R., 2021. Piezoelectric Energy Harvesting for Self-Powered Wearable Upper Limb Applications. *Nano Select*, *2*(8), pp.1459-1479.

Lueangamornsiri, T., Thongpull, K., Chalermyanont, K. and Wichakool, W., 2016. Design and Development of a Stand-Alone Solar Energy Harvesting System by MPPT and Quick Battery Charging. *13th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology*, pp. 1-5.

Marshall, B.R., Morys, M.M. and Durgin, G.D., 2015. Parametric Analysis and Design Guidelines of RF-to-DC Dickson Charge Pumps for RFID Energy Harvesting. *IEEE International Conference on RFID (RFID)*, pp. 32-39.

Mascarenas, D.L., Todd, M.D., Park, G. and Farrar, C.R., 2007. Development of an Impedance-Based Wireless Sensor Node for Structural Health Monitoring. *Smart Materials and Structures*, 16(6), p.2137.

MCMC, 2020. *Spectrum Plan*. Available through: https://www.mcmc.gov.my/skmmgovmy/media/General/MCMC-Spectrum-Plan-2022.pdf [Accessed 10 March 2023].

Mui, K.M., Khaw, M.K. and Mohd-Yasin, F., 2020. Power Management IC for a Dual-Input-Triple-Output Energy Harvester. *Micromachines*, *11*(10), p.937.

Nahak, T. and Pal, Y., 2016. Comparison Between Conventional, and Advance Maximum Power Point tracking Techniques for Photovoltaic Power System. *IEEE 7th Power India International Conference*, pp. 1-5.

Okpara, C.R., Idigo, V.E. and Oguchienti, S.M., 2020. Wireless Sensor Networks for Environmental Monitoring: A Review. *Int. J. Eng*. Trends Technol, 68(1), pp.68-71.

Omron, 2022. What is IoT?. Available through: https://components.omron.com/us-en/solutions/iot

Penella, M.T., Albesa, J. and Gasulla, M., 2009. Powering Wireless Sensor Nodes: Primary Batteries Versus Energy Harvesting. *IEEE Instrumentation and Measurement Technology Conference*, pp. 1625-1630.

Politi, B., Parola, S., Gademer, A., Pegart, D., Piquemil, M., Foucaran, A. and Camara, N., 2021. Practical PV Energy Harvesting Under Real Indoor Lighting Conditions. *Solar Energy*, 224, pp.3-9.

Seeman, M.D. and Sanders, S.R., 2008. Analysis and Optimization of Switched-Capacitor DC–DC Converters. *IEEE Transactions on Power Electronics*, 23(2), pp.841-851.

Seeman, M.D., Sanders, S.R. and Rabaey, J.M., 2007. An ultra-low-power Power Management IC for Wireless Sensor Nodes. *IEEE Custom Integrated Circuits Conference*, pp. 567-570.

Sezer, N. and Koç, M., 2021. A Comprehensive Review on the State-of-The-Art of Piezoelectric Energy Harvesting. *Nano Energy*, *80*, pp. 105567.

Sufiah, S.S., Ismail, A., Din, N.M. and Jamaludin, M.Z., 2010. Radio Frequency Radiation Evaluation of Transmitting Devices in VHF/UHF Band. *IEEE Student Conference on Research and Development (SCOReD)*, pp. 117-120.

Technavio, 2022. *Energy Harvesting Devices Market*. Retrieved from https://www.prnewswire.com/news-releases/energy-harvesting-devices-market-.html

Terasense, n.d. *Radio Frequency Bands*. Available through: https://terasense.com/terahertz-technology/radio-frequency-bands/ [Accessed 10 March 2023].

Visser, H.J., Reniers, A.C. and Theeuwes, J.A., 2008. Ambient RF energy scavenging: GSM and WLAN Power Density Measurements. *38th European Microwave Conference*, pp. 721-724.

Vullers, R.J.M., Van Schaijk, R., Doms, I., Van Hoof, C. and Mertens, R., 2009. Micropower Energy Harvesting. *Solid-State Electronics*, *53*(7), pp.684-693.

Vullers, R.J.M., van Schaijk, R., Doms, I., Van Hoof, C. and Mertens, R., 2009. Micropower Energy Harvesting. *Solid-State Electronics*, *53*(7), pp. 684-693.

Zhang, Y., Zhang, F., Shakhsheer, Y., Silver, J.D., Klinefelter, A., Nagaraju, M., Boley, J., Pandey, J., Shrivastava, A., Carlson, E.J. and Wood, A., 2012. A Batteryless 19μW MICS/ISM-Band Energy Harvesting Body Sensor Node SoC for ExG Applications. *IEEE Journal of Solid-State Circuits*, 48(1), pp.199-213.

APPENDICES

Appendix 1: CMOS Model

```
* PTM 32nm NMOS

.model  nmos  nmos  level = 54

+version = 4.0          binunit = 1          paramchk= 1          mobmod  = 0
+capmod  = 2            igcmod  = 1          igbmod  = 1          geomod  = 1
+diomod  = 1            rdsmod  = 0          rbodymod= 1          rgatemod= 1
+permod  = 1            acnqsmod= 0          trnqsmod= 0

+tnom    = 27           toxe    = 1.65e-9    toxp    = 1.0e-9     toxm    = 1.65e-9
+dtox    = 0.65e-9      epsrox  = 3.9        wint    = 5e-009     lint    = 2.7e-009
+ll      = 0            wl      = 0          lln     = 1          wln     = 1
+lw      = 0            ww      = 0          lwn     = 1          wwn     = 1
+lwl     = 0            wwl     = 0          xpart   = 0          toxref  = 1.65e-9
+xl      = -14e-9
+vth0    = 0.5088       k1      = 0.4        k2      = 0.0        k3      = 0
+k3b     = 0            w0      = 2.5e-006   dvt0    = 1          dvt1    = 2
+dvt2    = 0            dvt0w   = 0          dvt1w   = 0          dvt2w   = 0
+dsub    = 0.1          minv    = 0.05       voffl   = 0          dvtp0   = 1.0e-011
+dvtp1   = 0.1          lpe0    = 0          lpeb    = 0          xj      = 1.0e-008
+ngate   = 2e+020       ndep    = 4.12e+018  nsd     = 2e+020     phin    = 0
+cdsc    = 0.000        cdscb   = 0          cdscd   = 0          cit     = 0
+voff    = -0.13        nfactor = 2.3        eta0    = 0.0042     etab    = 0
+vfb     = -0.55        u0      = 0.0389     ua      = 6e-010     ub      = 1.2e-018
+uc      = 0            vsat    = 178470     a0      = 1.0        ags     = 0
+a1      = 0            a2      = 1.0        b0      = 0          b1      = 0
+keta    = 0.04         dwg     = 0          dwb     = 0          pclm    = 0.02
+pdiblc1 = 0.001        pdiblc2 = 0.001      pdiblcb = -0.005     drout   = 0.5
+pvag    = 1e-020       delta   = 0.01       pscbe1  = 8.14e+008  pscbe2  = 1e-007
+fprout  = 0.2          pdits   = 0.01       pditsd  = 0.23       pditsl  = 2.3e+006
+rsh     = 5            rdsw    = 150        rsw     = 75         rdw     = 75
+rdswmin = 0            rdwmin  = 0          rswmin  = 0          prwg    = 0
+prwb    = 0            wr      = 1          alpha0  = 0.074      alpha1  = 0.005
+beta0   = 30           agidl   = 0.0002     bgidl   = 2.1e+009   cgidl   = 0.0002
+egidl   = 0.8

+aigbacc = 0.012        bigbacc = 0.0028     cigbacc = 0.002
+nigbacc = 1            aigbinv = 0.014      bigbinv = 0.004      cigbinv = 0.004
+eigbinv = 1.1          nigbinv = 3          aigc    = 0.012      bigc    = 0.0028
+cigc    = 0.002        aigsd   = 0.012      bigsd   = 0.0028     cigsd   = 0.002
+nigc    = 1            poxedge = 1          pigcd   = 1          ntox    = 1
```

```
+xrcrg1  = 12          xrcrg2  = 5
+cgso    = 0.85e-010   cgdo    = 0.85e-010   cgbo    = 2.56e-011   cgdl    = 2.653e-10
+cgsl    = 2.653e-10   ckappas = 0.03        ckappad = 0.03        acde    = 1
+moin    = 15          noff    = 0.9         voffcv  = 0.02

+kt1     = -0.11       kt1l    = 0           kt2     = 0.022       ute     = -1.5
+ua1     = 4.31e-009   ub1     = 7.61e-018   uc1     = -5.6e-011   prt     = 0
+at      = 33000

+fnoimod = 1           tnoimod = 0

+jss     = 0.0001      jsws    = 1e-011      jswgs   = 1e-010      njs     = 1
+ijthsfwd= 0.01        ijthsrev= 0.001       bvs     = 10          xjbvs   = 1
+jsd     = 0.0001      jswd    = 1e-011      jswgd   = 1e-010      njd     = 1
+ijthdfwd= 0.01        ijthdrev= 0.001       bvd     = 10          xjbvd   = 1
+pbs     = 1           cjs     = 0.0005      mjs     = 0.5         pbsws   = 1
+cjsws   = 5e-010      mjsws   = 0.33        pbswgs  = 1           cjswgs  = 3e-010
+mjswgs  = 0.33        pbd     = 1           cjd     = 0.0005      mjd     = 0.5
+pbswd   = 1           cjswd   = 5e-010      mjswd   = 0.33        pbswgd  = 1
+cjswgd  = 5e-010      mjswgd  = 0.33        tpb     = 0.005       tcj     = 0.001
+tpbsw   = 0.005       tcjsw   = 0.001       tpbswg  = 0.005       tcjswg  = 0.001
+xtis    = 3           xtid    = 3

+dmcg    = 0e-006      dmci    = 0e-006      dmdg    = 0e-006      dmcgt   = 0e-007
+dwj     = 0.0e-008    xgw     = 0e-007      xgl     = 0e-008

+rshg    = 0.4         gbmin   = 1e-010      rbpb    = 5           rbpd    = 15
+rbps    = 15          rbdb    = 15          rbsb    = 15          ngcon   = 1

* PTM 32nm PMOS

.model  pmos  pmos  level = 54

+version = 4.0         binunit = 1           paramchk= 1           mobmod  = 0
+capmod  = 2           igcmod  = 1           igbmod  = 1           geomod  = 1
+diomod  = 1           rdsmod  = 0           rbodymod= 1           rgatemod= 1
+permod  = 1           acnqsmod= 0           trnqsmod= 0

+tnom    = 27          toxe    = 1.75e-009   toxp    = 1.0e-009    toxm    = 1.75e-009
+dtox    = 0.75e-9     epsrox  = 3.9         wint    = 5e-009      lint    = 2.7e-009
+ll      = 0           wl      = 0           lln     = 1           wln     = 1
```

```
+lw      = 0           ww      = 0           lwn     = 1           wwn     = 1
+lwl     = 0           wwl     = 0           xpart   = 0           toxref  = 1.75e-009
+xl      = -14e-9
+vth0    = -0.450      k1      = 0.4         k2      = -0.01       k3      = 0
+k3b     = 0           w0      = 2.5e-006    dvt0    = 1           dvt1    = 2
+dvt2    = -0.032      dvt0w   = 0           dvt1w   = 0           dvt2w   = 0
+dsub    = 0.1         minv    = 0.05        voffl   = 0           dvtp0   = 1e-011
+dvtp1   = 0.05        lpe0    = 0           lpeb    = 0           xj      = 1.0e-008
+ngate   = 2e+020      ndep    = 3.07e+018   nsd     = 2e+020      phin    = 0
+cdsc    = 0.000       cdscb   = 0           cdscd   = 0           cit     = 0
+voff    = -0.126      nfactor = 2.3         eta0    = 0.0042      etab    = 0
+vfb     = 0.55        u0      = 0.00355     ua      = 2.0e-009    ub      = 0.5e-018
+uc      = 0           vsat    = 70000       a0      = 1.0         ags     = 1e-020
+a1      = 0           a2      = 1           b0      = 0           b1      = 0
+keta    = -0.047      dwg     = 0           dwb     = 0           pclm    = 0.1
+pdiblc1 = 0.001       pdiblc2 = 0.001       pdiblcb = 3.4e-008    drout   = 0.6
+pvag    = 1e-020      delta   = 0.01        pscbe1  = 8.14e+008   pscbe2  = 9.58e-007
+fprout  = 0.2         pdits   = 0.08        pditsd  = 0.23        pditsl  = 2.3e+006
+rsh     = 5           rdsw    = 150         rsw     = 75          rdw     = 75
+rdswmin = 0           rdwmin  = 0           rswmin  = 0           prwg    = 0
+prwb    = 0           wr      = 1           alpha0  = 0.074       alpha1  = 0.005
+beta0   = 30          agidl   = 0.0002      bgidl   = 2.1e+009    cgidl   = 0.0002
+egidl   = 0.8

+aigbacc = 0.012       bigbacc = 0.0028      cigbacc = 0.002
+nigbacc = 1           aigbinv = 0.014       bigbinv = 0.004       cigbinv = 0.004
+eigbinv = 1.1         nigbinv = 3           aigc    = 0.69        bigc    = 0.0012
+cigc    = 0.0008      aigsd   = 0.0087      bigsd   = 0.0012      cigsd   = 0.0008
+nigc    = 1           poxedge = 1           pigcd   = 1           ntox    = 1

+xrcrg1  = 12          xrcrg2  = 5
+cgso    = 0.85e-010   cgdo    = 0.85e-010   cgbo    = 2.56e-011   cgdl    = 2.653e-10
+cgsl    = 2.653e-10   ckappas = 0.03        ckappad = 0.03        acde    = 1
+moin    = 15          noff    = 0.9         voffcv  = 0.02

+kt1     = -0.11       kt1l    = 0           kt2     = 0.022       ute     = -1.5
+ua1     = 4.31e-009   ub1     = 7.61e-018   uc1     = -5.6e-011   prt     = 0
+at      = 33000

+fnoimod = 1           tnoimod = 0

+jss     = 0.0001      jsws    = 1e-011      jswgs   = 1e-010      njs     = 1

+ijthsfwd= 0.01        ijthsrev= 0.001       bvs     = 10          xjbvs   = 1
+jsd     = 0.0001      jswd    = 1e-011      jswgd   = 1e-010      njd     = 1
+ijthdfwd= 0.01        ijthdrev= 0.001       bvd     = 10          xjbvd   = 1
+pbs     = 1           cjs     = 0.0005      mjs     = 0.5         pbsws   = 1
+cjsws   = 5e-010      mjsws   = 0.33        pbswgs  = 1           cjswgs  = 3e-010
+mjswgs  = 0.33        pbd     = 1           cjd     = 0.0005      mjd     = 0.5
+pbswd   = 1           cjswd   = 5e-010      mjswd   = 0.33        pbswgd  = 1
+cjswgd  = 5e-010      mjswgd  = 0.33        tpb     = 0.005       tcj     = 0.001
+tpbsw   = 0.005       tcjsw   = 0.001       tpbswg  = 0.005       tcjswg  = 0.001
+xtis    = 3           xtid    = 3

+dmcg    = 0e-006      dmci    = 0e-006      dmdg    = 0e-006      dmcgt   = 0e-007
+dwj     = 0.0e-008    xgw     = 0e-007      xgl     = 0e-008

+rshg    = 0.4         gbmin   = 1e-010      rbpb    = 5           rbpd    = 15
+rbps    = 15          rbdb    = 15          rbsb    = 15          ngcon   = 1
```