COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) CHARGE PUMP WITH TEMPERATURE VARIATION FOR SELF-POWERED APPLICATIONS

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A project report submitted in partial fulfilment of the requirements for the award of Master Of Engineering (Electronic Systems)

Faculty Of Engineering And Green Technology
Universiti Tunku Abdul Rahman

August 2023

DECLARATION

I hereby declare that this project report is based on my original work except for citations and quotations which have been duly acknowledges. I also declared that it has not been previously and concurrently submitted for any other master or award at UTAR or other institutions.

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APPROVAL FOR SUBMISSION

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Date : 15 August 2023

Specially dedicated to my beloved parents, my cherished husband, my dear family, my respected supervisor, and my wonderful friends.

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ABSTRACT

This research introduces an innovative CMOS charge pump topology that addresses the challenge of maintaining a steady 1V output voltage across a wide temperature range. Through the integration of a closed-loop regulation circuit, the charge pump demonstrates remarkable stability and tolerance to temperature changes, ensuring consistent performance in self-powered devices. Furthermore, the successful integration of a MOSFET-based DC-to-DC converter within the charge pump mechanism achieves efficient voltage boosting, enhancing output stability. Rigorous simulations validate the design's feasibility and suitability for real-world self-powered applications. This study contributes to the advancement of self-powered devices by offering a reliable solution for voltage regulation under varying temperature conditions.

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CHAPTER 1

INTRODUCTION

1.1 Background

A charge pump is a circuit which utilize capacitors as the energy-storage elements that generates either a higher voltage source or a lower voltage source for several different applications such as switched capacitor circuit, to program and erase data in flash memory, as well as radio frequency identification (RFID). This paper aims to design a charge pump circuit which act as DC-to-DC converter in self-powered applications in the complementary metal-oxide-semiconductor (CMOS) process with a variety of temperature. Figure 1 shows the charge pump made up with NMOS and PMOS respectively. The circuit in this study will use an unconventional charge transfer switch comprised of a pair of NMOS and PMOS transistor which respective gates are coupled to the charge pump's internal nodes.

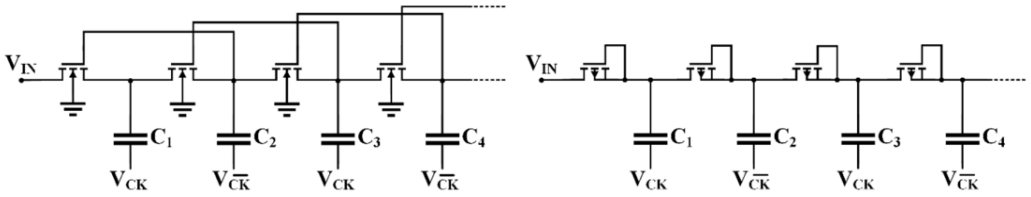

Figure 1: Dickson charge pump using NMOS (left) and PMOS (right)

The needs for high performance Very Large-Scale Integration (VLSI) circuits are growing, which has led to higher current densities and more power being dissipated. A substantial percentage of electricity is turned to heat, which causes the heat density to increase exponentially. As a result, controlling and measuring temperature are essential in many applications. The existence of temperature variation may help in designing the circuit with steady performance throughout the study of this paper.

Self-powered applications indicates that it can continue to function without an external power source by capturing energy from its surroundings while in use. In this age of the world, there are majority of devices that need a minimizing on energy utilization which offer a higher level of convenience to the user. Technology that operates on its own offers a sustainable energy supply for wearable and portable devices.

For example, these powering alternatives are not workable solutions for IoT devices installed in remote locations with poor accessibility. Therefore, the need of self-powered application which harvest energy from ambient source is a workable solution to this example of problem mentioned by Kjellby *et al*. (2018). The design and prototype implementation of a self-powered Internet of Things (IoT) device that uses energy harvesting from a small solar panel for remote applications are shown in this work. The device can operate for a year on a fully charged battery and has a transmission range of 1.8 km. It includes extremely low power temperature, humidity, and light sensors. Overall, this study offers useful insights into the development and evaluation of a self-powered Internet of Things (IoT) device that makes use of ambient energy harvesting.

1.2 Problem Statement

There are two types of MOSFETs: NMOS and PMOS which both has their own advantages and disadvantages. For instance, NMOS are faster, but PMOS are less prone to noise. NMOS is used more often due to its advantages, however many applications also require the polarization characteristic of the PMOS. That being the case, here comes the implementation of CMOS which used both NMOS and PMOS. The term "complementary" refers to the idea that p-type and n-type MOSFET pairings, which are complementary and symmetrical, are typically used in pairs for logic operations in typical digital designs using CMOS technology. High noise immunity and low static power consumption are two significant CMOS device properties. While one of the pair's transistors is always off, the series combination only uses a considerable amount of power while transitioning between the on and off states.

Circuit density and clock speed increases have resulted in higher power consumption, which has brought thermal concerns to the foreground of VLSI design. Variations in temperature frequently change the MOSFETs' saturation velocity, carrier mobility and threshold voltage, which impacts how well CMOS circuit's function. The subsequent fluctuations in current can result in self-heating and elevated leakage current, both of which are harmful to the system's performance and dependability. As a result, the need of designing the circuit with a variation of temperature is essential to make sure constant output of CMOS charge pump is maintain while the temperature being diverse.

Energy harvesting may be possible to eliminate the requirement for routine battery replacement or recharging but according to Ballo *et al*. (2019) the output of energy harvester is only few hundred of millivolts or less. Therefore, power management integrated circuit (PMIC) will be applied by combining energy harvester with a CMOS charge pump which will act as DC-to-DC converter.

1.3 Objectives

1. To develop a CMOS charge pump topology that generates a steady state output voltage which is 1V despite being fed with a diverse range of temperature.
2. To design a CMOS charge pump with fully integrated MOSFET which act as DC-to-DC converter to step up the low input voltage for a higher constant output voltage.
3. To create a testbenches and simulate the CMOS charge pump for a self-powered application to verify its performanc

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Power autonomy in IoT nodes is attained by scavenging energy from the environment using transducers. However, the circuit where these transducers are used is frequently not suitable for direct feeding. As a result, this paper will use a PMIC by which consists of clock generation and charge pump to increase conversion efficiency.

A type of DC-DC converter known as a charge pump circuit, also known as a charge pump regulator, uses switched-capacitor techniques to either raise or lower an input voltage level. As seen in Figure 2, these circuit blocks primarily comprise capacitors and switches (clock-controlled field-effect transistors, or FETs), and they function by precisely timing and manipulating these switches to take use of capacitors' charge transfer properties.

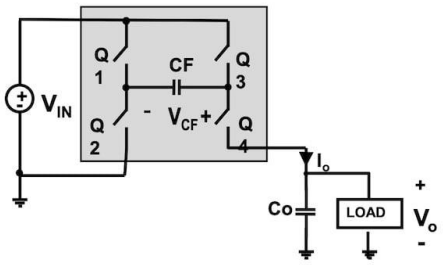

Figure 2: Circuit of Charge Pump Regulator

Besides that, the existence of temperature variation may help in designing the circuit with steady performance throughout the study of this paper. The speed of electron motion is influenced by temperature, which also affects how electricity flows across an electrical circuit. A spike in circuit resistance caused by an increase in temperature is what causes this. Similarly, resistance decreases as temperature rises. That being so, further study was made in this literature review which review the past few years of researchers' work about the energy harvesting and PMIC, CMOS charge pump and temperature in circuit design.

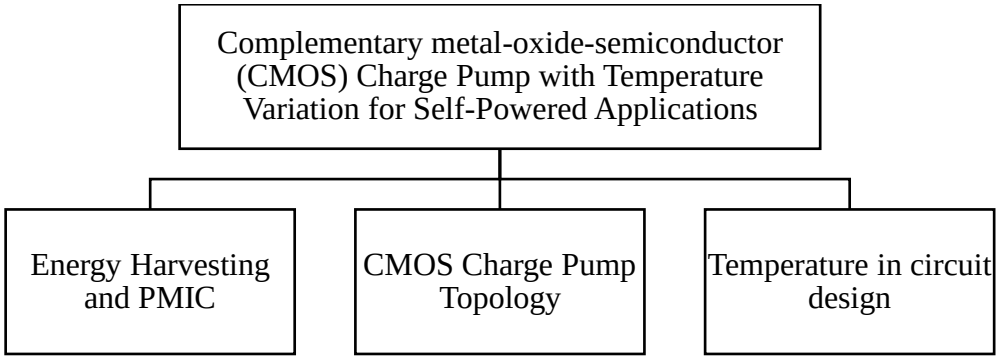

Figure 3: Chart of literature review

2.2 Energy Harvesting and PMIC

With the use of transducers like thermoelectric generators (TEG), photovoltaic (PV) cells, thermoelectric generators (TEG), and sensors, IoT nodes can become power autonomous. Because of this, especially when the energy harvester's output is only a few hundred millivolts or fewer, these transducers are frequently not suited for feeding directly to the circuit. To increase conversion efficiency Ballo *et al*. (2019), use a PMIC by utilizing charge pump to increase the output of the energy harvester.

Figure below shows a simple block diagram of PMIC. An external transducer's input voltage, V_{IN}, powers a DC-DC converter and a clock generator block. The converter is then regulated to produce an output voltage that is perfectly stable or to reduce power consumption depending on the required load current.

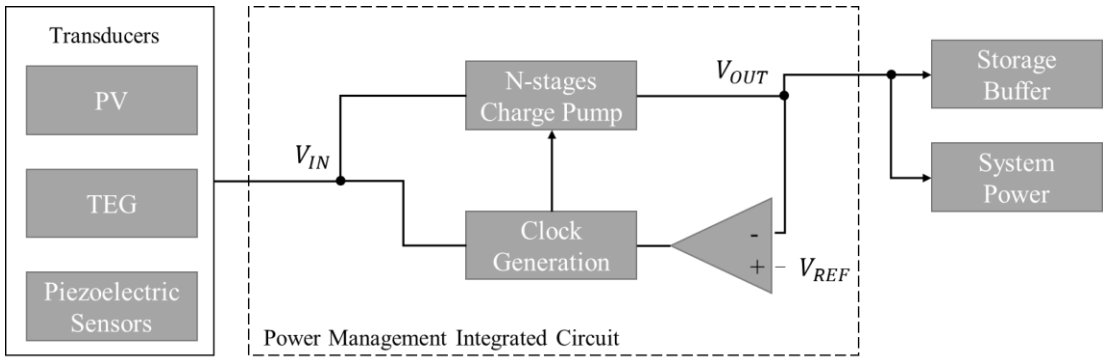

Figure 4: Block Diagram of PMIC by Ballo et al. (2019)

The DC-DC converter and the clock generator are the two primary parts of a PMIC. These blocks must also allow for self-startup in critical situations, low voltage and low power levels supplied external energy harvester. Switched inductor or switched capacitor converters can be used to create the DC-DC converter. SI converters are ideal for high power applications (usually larger than 100 mW), but their implementation calls for hefty off-chip inductors. Since SC converters may be fully integrated on-chip, they are a better solution for low-power and low-area applications

like IoT nodes. Typically, voltage multipliers or charge pumps are used to describe SC converters with voltage gains greater than one (charge pumps).

According to Ulaganathan *et al*. (2012) transducers do not produce a steady output due to fluctuations in the operating conditions. As a result, PMIC are used by energy harvesters to increase conversion efficiency. The DC-DC converter and the clock generator, which permits self-startup, are essential parts of PMIC. The charge pump increases the low output voltage (VIN) from the energy scavengers to supply the power supply voltage for the target application as well as for storage in the buffer. The five-stage ring oscillator (RO) and phase generator (PG) circuits produce the control signals needed for the charge pump to operate. To give the converter power autonomy, these circuits are powered directly from VIN. By adjusting the frequency of operation or the number of conversion stages in the charge pump, the output control block is used in the PMC to deliver maximum power transfer (MPT) from the charge pump to the load.

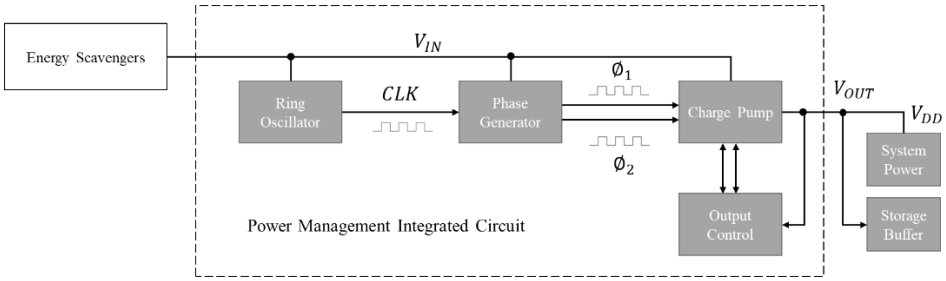

Figure 5: Block Diagram of PMIC by Ulaganathan et al. (2012)

This design uses NAND gates to build a standard non-overlapping (NOV) phase generator to supply the clock phases for the various charge pump stages. The loss of charge caused by reverse currents travelling from later stages to earlier stages along the charge pump is eliminated by the NOV clocks. The DC-DC boost converter uses an architecture based on the linear charge-pump Because the number of charge pump stages may be adjusted, linear charge-pump enable low voltage operation and flexible boost ratios.

2.3 CMOS Charge Pump Topology

In this study, Rahman *et al*. (2021) discusses design methodologies that have progressed from diode-connected structures to dynamic clock voltage scaling charge pumps with a focus on low voltage strategies and charge pump topologies for low power applications. Charge pump circuits can be used in low-power applications in the CMOS process to handle continuous power supply reduction, cheap implementation costs, and excellent efficiency. By using voltage multiplication and integrating an additional diode-capacitor voltage stage in series, the power supply voltage can be increased. The three frequently utilized applications—memory, DC-DC converters, and energy harvesting areas—are identified using various design methodologies, and their results are displayed below.

Table 1: Summary of charge pump Topology by Rahman et al. (2021)

Design Topology	**Process (µm)**	**Supply Voltage (V)**	**Output Voltage (V)**	**Applications**
Boost converter scheme	0.13	0.27	1.4	energy harvesting with PV cell
Cross-coupled body bias	0.18	0.32	2.04	energy harvesting
Cross-coupled with DBB	0.13	0.15	0.619	Low voltage energy harvesting
Single-clock tree topology	0.18	0.39-0.43	1	Microscale solar energy harvesting
Closed loop control	0.18	5	16.95	Sensor based micro gyroscope

A charge pump circuit is also necessary for energy collecting devices in order to enhance voltages for the process. Compared to memory devices, this sector does not require a significant increase in voltage. Therefore, compared to other charge pump circuits based on low voltage applications, such as RFID transponder memory, NVM, DC-DC converters, PLL devices, etc., the

pumping efficiency levels in these topologies are not that much greater. Additionally, these topologies have called for additional circuitry, which ultimately expands the total chip size and power dissipation.

As claimed by Ballo *et al*. (2019) in their study, in the most recent study, charge pumps have been extensively employed to transmit the electric energy that is harvested from the surrounding environment towards a storage buffer and to adjust the voltage levels between two or more functional blocks. Figure below depicts the general block diagram of an N-stage charge pump, with each i-th stage consisting of a charge transfer switch (CTS) and a pumping capacitor, C. The output stage is made up of the final pair, CTS, and CL. CTS is to draw attention to the block's primary objective, which is to permanently transfer charge from the input to the output. Among the different potential charge pump architectures, the circuit topology of the CTS serves as the primary source of diversity and is, of course, a crucial issue to consider.

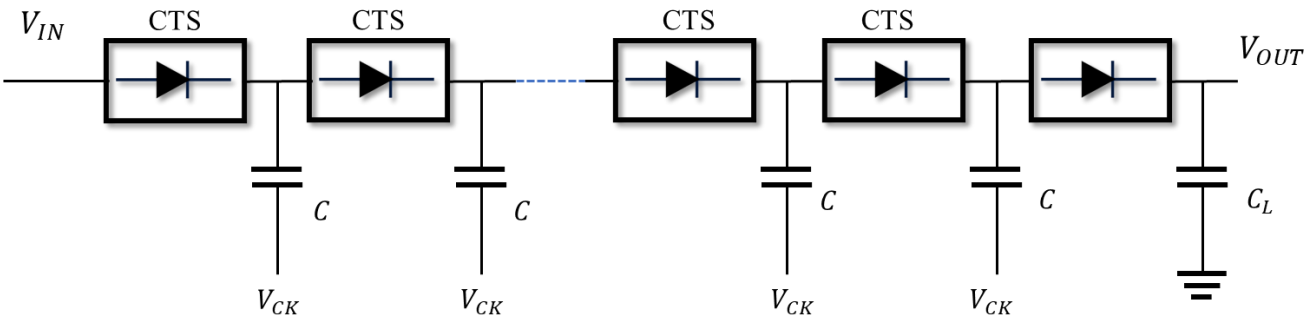

Figure 6: General Block Diagram of CTS and Capacitor

The individual application, the CMOS technology, and the design requirements all have a role in which topology is chosen among those described in this study (Ballo *et al*., 2019). Following a review of the previous section, some broad recommendations are given. The design of auxiliary circuits, particularly the clock generator and drivers, needs special consideration because of how much power they consume and how that could affect the charge pump as a whole.

Table 2: Summary of charge pump Topology by Ballo et al. (2019)

Topology	Cross-coupled/composite	Cross-coupled	Bootstrap	Dickson-with DGB	Cross-coupled with BGB	Cross-coupled DBB	Bootstrap			Adiabatic		Adaptive
Stages	6 parallel 24	3	10	4	6	3	3	5	1	3	7	
Aux Circuit	Start up circuit	Clock Booster 3X	Clock Booster 2X	Dynamic G Control	Backward G Biasing	Dynamic B Control	`-	Split-merge four-brances	`-	Low-threshold diode in every CTS		`-
Technology (nm)	130	65	65	65	180	130	130	130	180	130		65
Min. Supply (mV)	70	150	100	550	320	150	270	500	390	125		120
Clock Frequency (MHz)	0.04	15.2	10	1.8	0.45	0.25	0.8	2.5	23	0.36		1
Total Pumping Capacitor (pF)	46.08	22.5	1001	160	288	36000*	150	310	500	96	224	286
Load Capacitor (pF)	10000*	30	100	400	50.7	10000*	500	800	4000*	100		`-
Load Current at Peak (uA)	12	1.74	0.76	10	`-	21	5	30	620	0.1		3.9
Max Output Power (uW)	15	1.5	6.6	4.7	`-	10.5	7	75	650	0.061	0.035	3
Peak VCE (%)	50	80	76	96	89	86	65	93	93	70	80	58
Peak n (%)	58	38.8	33	66	`-	34 **	58	78.6 **	76	59	62	38.8
Area (mm2)	0.6	0.032	1.32	0.17	0.14	0.066*	0.42	0.98	0.48	0.15	0.1	0.78

*off-chip capacitor ** external clock generator

Based on study written by Librado & Hora (2022) cross-coupled charge pump or voltage doubler (CCVD)/multiplier architectures, which are general terms for capacitive-based DC-DC converters, do away with large off-chip components and auxiliary circuits while offering a low-start-up up-conversion feature with a small form factor and low manufacturing cost. Its ability to start entirely electrically is still what makes it stand out from other upconverters. The circuits' growing conduction loss, reversion loss, deadtime restrictions, and constrained voltage conversion ratios are this architecture's downsides.

Using an integrated clock booster and a 4-phase clocking scheme, the proposed design eliminates all reversion losses, eliminates the need for level shifters for PMOS gate control, eliminates voltage overstress and breakdown difficulties, and scales the design to be as efficient as possible. Additionally, the suggested architecture incorporates a Forward Body Bias (FBB) method to account for low-input power situations. The suggested charge pump can accept inputs as low as 250mV and is implemented utilising TSMC's 65nm manufacturing technology.

Table 3: Comparison of Librado & Hora (2022)'s charge pump with others

	Technology	Number of Stages	Max Conversion Ratio	Minimum Input	Maximum Output voltage**	Flying Capacitor	Output Capacitor	Pumping Frequency	Peak Voltage Conversion Efficiency	Settling Time	Peak Power Conversion Efficiency
[1]	120nm	1	1.99	1.2 V*	2.4 V*	210pF	200pF	50MHz	---	---	88.16 %
[12]	45nm	2	2.94	800mV*	---	2.1n F	500pF	60MHz	97.5-98%	---	---
[13]	180nm	1	1.96	---	---	48pF	24pF	10MHz	---	---	57 %
[14]	180nm	3	3.2	3.3 V*	10.5 V	400pF	100pF	67 MHz	---	---	69 %
This Study	**65nm**	**1**	**1.99**	**250mV**	**990mV**	**30pF**	**50pF**	**20MHz**	**99.04 %**	**105.42 ns**	**90.9 %**
		2	**2.97**		**1.484V**				**98.93%**	**254 ns**	**80.95 %**
		3	**3.94**		**1.972 V**				**98.86%**	**1.49 us**	**77.47 %**

**Tested input only, no specified min. input ** at peak efficiency*

As stated in paper studied by Ballo *et al*. (2019) the Dickson charge pump (Dcharge pump) is a frequently used boost DC-DC converter in a variety of applications due to its simple topology, low sensitivity to parasitic effects, and strong driving capabilities. They claimed that the output steady-state voltage, pumping time, and output voltage ripple are the three main design constraints

of a Dcharge pump, which may be used to determine the minimal number of stages and pumping capacitance required.

In order to maximize charge pump performance, both for the slow switching limit regime and the fast-switching limit regime, the CTS resistance is a critical design parameter that must be reduced. The resistance in practical CTS implementations is either a triode-region NMOS transistor, as in the bootstrapped switches on the Dcharge pump, or it is a series of complementary triode-region NMOS and PMOS transistors, as in the latching charge pump.

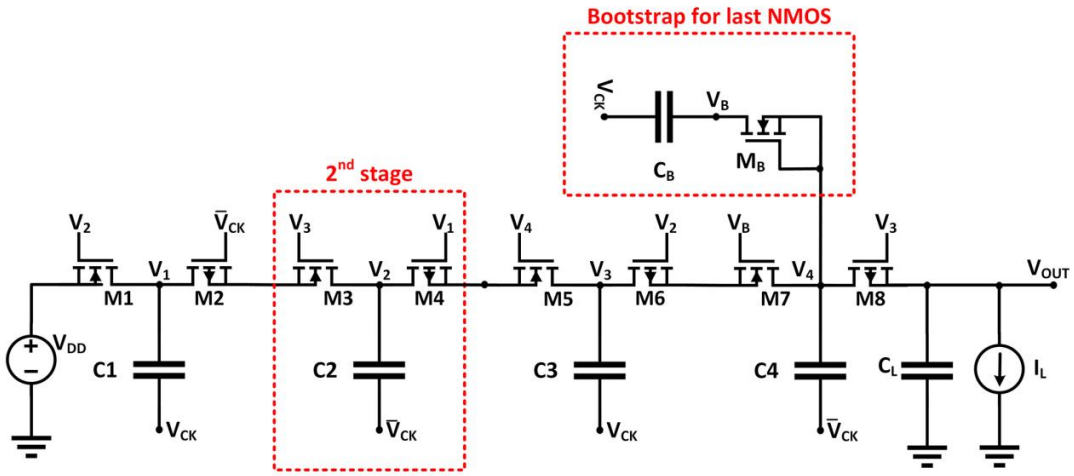

Figure 7: Charge pump topology by Ballo et al. (2019).

The leftmost red dashed box in the above diagram represents the series combination of an NMOS and a PMOS transistor that makes up each CTS. Each transistor's bulk terminal is connected to the source terminal during the conduction phase. Node V1, the output voltage of the stage before PMOS, drives the gate of PMOS, while node V3, the output voltage of the stage following NMOS, is connected to the NMOS gate voltage.

This structure is consistently repeated along the charge pump with the exception of the first stage, where the gate voltage of the PMOS is connected to a negated clock signal, and the final stage, where a small capacitive auxiliary MOSFET is added to bootstrap the gate voltage of the

NMOS in order to maintain the same performance as the other CTSs (MB and CB in the rightmost red dashed box in the above diagram). Even though the recommended charge pump's VCE slightly decreases at voltages close to the MOS threshold voltage because of reverse losses, it nevertheless operates with good current driving range, power efficiency, and speed. Additionally, it performs well at very low input voltage.

In a paper published in 2016, Dadhich *et al*. compared the Dickson charge pump and the charge pump circuit with cross-connected NMOS cells, two of the most admired charge pump architectures. The comparison was done while taking the output voltage, power usage, delay, output current, and conversion ratio into account. The input clock signal, power supply voltage, storage capacitance per stage, and number of stages are same for the two charge pumps.

The table below shows an experimental comparison between two of the most often used charge pump structures, the Dickson and cross-linked charge pumps. According to the theoretical description, the Dickson charge pump's output voltage is roughly 34.7% lower than that of the cross-connected NMOS cells when the power supply voltage is 5V. The comparison finding demonstrates that the cross-connected NMOS cell charge pump offers gains in terms of output voltage, power consumption, delay voltage conversion ratio, and current driving abilities. Authors discovered that the optimum performance of NMOS cross-connected cells charge pump.

Table 4: Comparison of Dickson charge pump with Cross Connected NMOS charge pump

	Type of charge pump	
	Dickson	**Cross connected NMOS cells**
Output voltage, V	9.5	16.44
Power consumption, uW	334	4974
Delay, ns	1.77	0.50
Current, mA	1.5	200
Conversion ratio, r	1.9	3.28

In this study by Badal *et al*. (2019), an improved charge pump circuit utilizing the current mirror technique and an inverter is proposed to address the current requirement of low power consumption, zero current mismatch, and zero net charges. The lowest current mismatch is attained using the low voltage NMOS cascade mirror technology and additional transistors connected to the output node through the mirror transistors. The post-layout result demonstrates that the suggested charge pump circuit consumes just 0.178 W and offers 0% current mismatch at 1.8 V supply voltage with a pumping capacitor of 0.1 pF. The charge pump circuit can be utilized extensively in a variety of low power wireless electronic devices including the transceiver, disk read/write channels for high-speed data transfer, clock synthesis, synchronization, jitter reduction, etc.

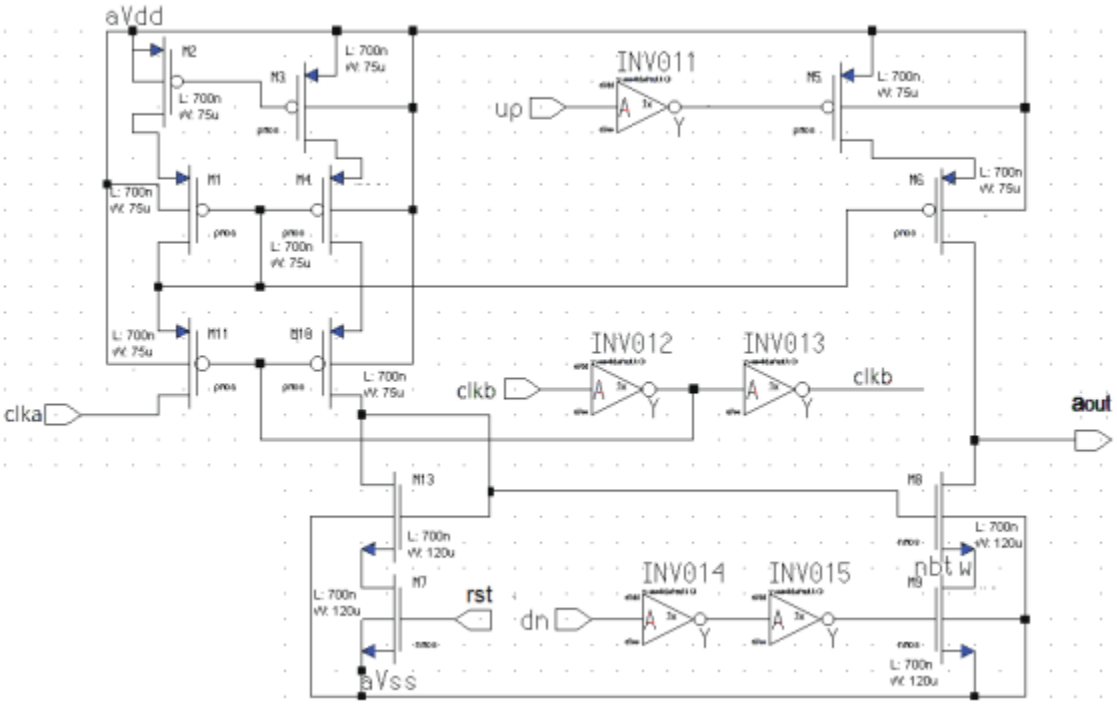

Figure 8: Charge pump topology of cascade mirror technique by Badal et al. (2019)

The paper introduces a novel approach to designing a low voltage charge pump with remarkable pumping efficiency (Yim *et al*., 2018). The proposed circuit adopts a 2-branch cross-coupled structure, interconnecting two charge pump branches to enhance performance. This cross-coupling technique offers significant benefits, including improved charge transfer efficiency and

overall circuit reliability. By employing PMOS transistors as Charge Transfer Switches (CTS), the circuit effectively overcomes undesirable effects like body effect and threshold voltage drops commonly encountered in charge pump designs. The use of PMOS transistors ensures more efficient and reliable charge transfer, leading to overall performance enhancement.

Incorporating inverters to control the gate of the CTS PMOS further boosts the pumping efficiency. Careful timing of NMOS and PMOS transistors during clock transitions prevents unwanted charge transfer between voltage nodes. The resulting short overlapping period allows for rapid gate control due to cross-coupled wiring and interactions between present and previous stages, leading to superior pumping efficiency compared to traditional charge pump circuits. Extensive simulations demonstrate the effectiveness of the proposed design, showcasing its superiority over existing circuits. With improved pumping efficiency, enhanced charge transfer, and minimal voltage losses, the proposed charge pump design presents a promising solution for low voltage applications where efficient energy conversion is crucial.

2.4 Temperature in Circuit Design

Della Corte *et al*. (2018) perform an experimental analysis to determine the effect of temperature variation on the conversion efficiency of ultrahigh-frequency energy harvesters based on diode-capacitor Dickson charge pumps, which are frequently used in self-energizing circuits, such as in radio frequency identification tags or wireless sensor nodes. The changing rectification ratio—specifically, the ratio of the forward and reverse current flowing through the low barrier height Schottky diodes, both of which show a positive derivative with T—shows that the harvester conversion efficiency at 868 MHz is temperature dependent. Schottky diodes, which are widely utilized in this application and are readily available, are used for this. The experimental results showed that temperatures between 25 °C and 85 °C can have a considerable impact on circuit efficiency. The research has shown that a temperature change can be especially harmful at low

incident power levels, where even a slight drop in conversion efficiency can render a wirelessly powered circuit unworkable.

The circuit proposed by Bahramali and Lopez-Vallejo (2018) consist of a Dickson charge pump and a series of stacked diode-connected CMOS components. With this setup, the writers have developed a novel method to generate a Dickson charge pump reference voltage of 1.515V that exhibits stable behavior over a wide range of temperatures. The circuit was created using normal CMOS components and simulated using Cadence utilizing a commercial 40nm technology. The suggested circuit has a temperature coefficient of 88 PPM/C and consumes 235nW of power over the range of -10 °C to 125 °C.

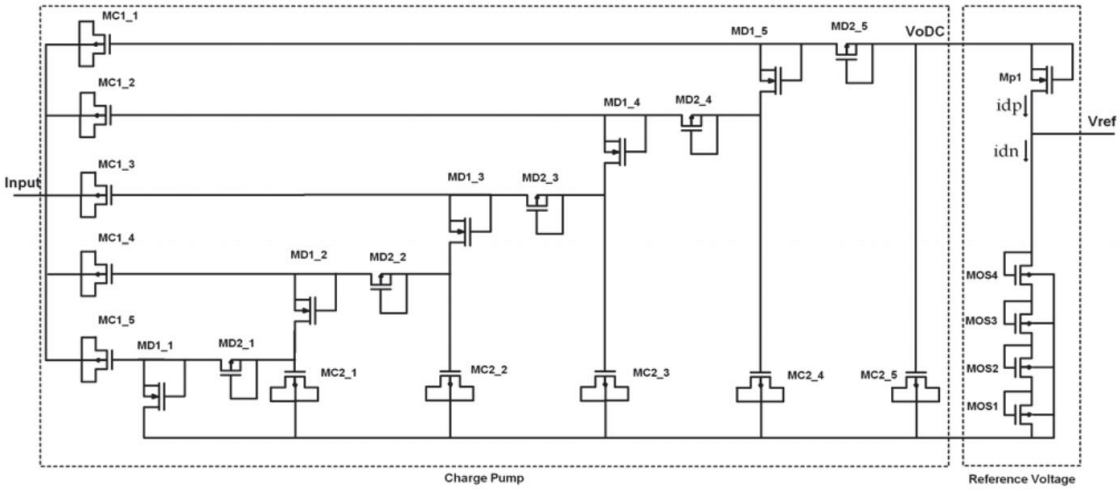

Figure 9: CMOS charge pump Topology by Bahramali and Lopez-Vallejo (2018)

By utilizing an incorporated Dickson charge pump, the suggested circuit by Bahramali, Lopez-Vallejo, and Barrio (2019) is able to transform an RFID (radio frequency identification) harvested input voltage with an amplitude of 800 mV into a DC level of 2 V. In this way, the circuit is supplied with the necessary supply voltage in addition to a fresh method for making it temperature resilient. Devices made of semiconductors are always sensitive to temperature variations. The current method for eliminating a reference voltage's temperature sensitivity is to

combine a PTAT (proportional to absolute temperature) voltage with a CTAT (complementary to absolute temperature) voltage. This results in a zero-temperature coefficient voltage. Here, the charge pump serves two functions. It serves as the circuit's power source in the first place. The reference voltage becomes self-powered as a result. The CTAT characteristic of the reference voltage circuit is offset by its PTAT characteristic.

Li *et al*. (2019) propose a high-voltage temperature-insensitive charge pump in their article. Utilizing triple-well NMOS (n-type metal-oxide-semiconductor) transistors, the output voltage can be increased above the breakdown voltage of an n-well/substrate diode without the use of BCD (bipolar-CMOS-DMOS) technology. To lessen the output voltage's sensitivity to temperature variations, closed-loop regulation is achieved by continuously adjusting the pumping clock's amplitude. In addition, a wide range of output levels can be programmed linearly by altering the reference voltage. A 0.18-m conventional CMOS (complementary metal-oxide-semiconductor) fabrication method was used to create the entire circuit. According to measurements, the output voltage has a linear adjustable range between around 13 and 16.95 volts, and results from temperature tests show that the output voltage's greatest changes at 40 to 80 degrees Celsius are less than 1.1%.

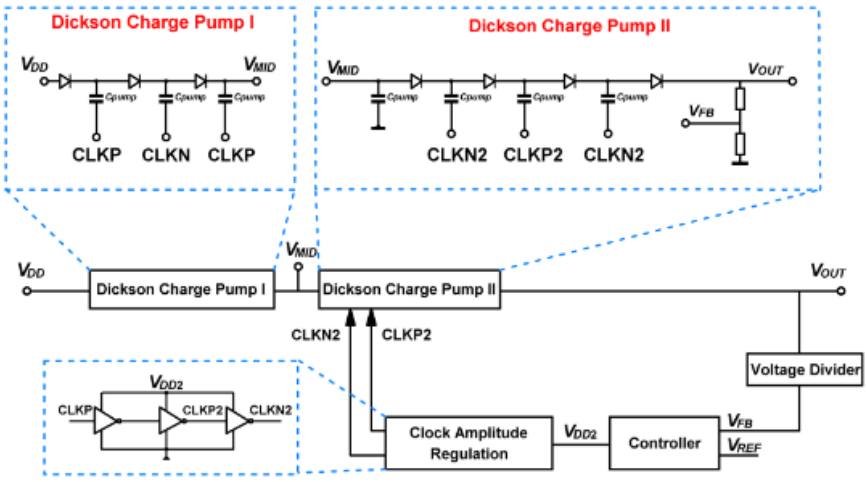

Figure 10: Charge pump topology using NMOS by Li et al. (2019)

2.5 Summary

2.5.1 Energy Harvesting and PMIC

Authors	Summary
Ballo *et al*. (2019)	• Circuit cannot directly take the voltage of transducers as the output is only a few hundred mV or less. • PMIC is used to increase the conversion efficiency; DC-DC converter and clock generator are primary part of PMIC. • Switched capacitor is a better solution for low power and low area applications.
Ulaganathan *et al*. (2012)	• Transducers do not produce a steady output due to fluctuations in the operating conditions. • Ring oscillator and phase generator circuits produce the control signals needed for the charge pump to operate. • Uses linear charge-pump which enable low voltage operation and flexible boost ratios.

2.5.2 CMOS Charge Pump Topology

Authors	Summary

Rahman *et al*. (2021)	• Charge pump in CMOS process can manage.
	  ○ Continuous power supply reduction
	  ○ Low implementation cost
	  ○ High efficiency
	• Increment in power supply voltage can achieve by additional one diode-capacitor voltage stage in series.
	• Cross-coupled body bias and cross-coupled with DBB are suitable for energy harvesting

Ballo *et al*. (2019)	• Charge pump – consists of CTS and pumping capacitor. • Particular attention to the design auxiliary circuit (clock generator & drivers) ○ Power consumption can degrade power conversion of overall charge pump.

	• Cross coupled, Bootstrap.
	  ○ Min supply (mV): 70; 150
	  ○ Clock frequency (MHz): 0.04; 0.25

Librado & Hora (2022)	• Cross couple charge pump
	• Drawbacks: conduction loss, reversion loss, deadtime restrictions, and constrained voltage conversion ratios
	• To overcome:
	  ○ Using an integrated clock booster and a 4-phase clocking scheme
	  ○ Incorporates Forward Body Biased method
	• Can accept inputs as low as 250mV

Ballo *et al*. (2019)	• Dickson charge pump with bootstrapped switches and latched Dcharge pumps (also known as dual-branch cross-coupled) • Extra MOSFET and capacitor – able to eliminate Vth • Offer high performance at very low input voltage
Dadhich *et al*. (2016)	• Compare Dickson charge pump and charge pump with cross connected NMOS • Charge pump with cross connected NMOS improve ○ Output voltage, power consumption, delay voltage conversion ratio and current driving capabilities
Badal *et al*. (2019)	• Presents enhanced charge pump with current mirror and inverter for low power consumption and precision. • Utilizes NMOS cascade mirror technique and extra transistors for minimal current mismatch. • Post-layout results showcase zero current mismatch at 1.8V supply with 0.1 pF capacitor, consuming only 0.178 µW. • Ideal for Reader-less RFID and diverse low-power wireless applications.
Yim *et al*. (2018)	• Introduces efficient low voltage charge pumping. • Uses 2-branch cross-coupled setup for improved performance. • PMOS transistors overcome issues, enhancing efficiency. • Simulations show superiority over existing designs.

2.5.3 Temperature in Circuit Design

Authors	Summary
Della Corte *et al*. (2018)	• Frequency: 868MHz, Temperature: 25 °C - 85 °C affect circuit efficiency • Efficiency is temperature dependent due to changing rectification ratio
Bahramali and Lopez-Vallejo (2018)	• Dickson charge pump and a series of stacked diode-connected CMOS • Circuit has: o a temperature coefficient of 88 PPM/C o consumes 235nW of power over the range of -10 °C to 125 °C. o reference voltage = 1.515V
Bahramali, Lopez-Vallejo, and Barrio (2019)	• Input voltage: 800mV, output voltage: 2V • Cancelling the temperature sensitivity of a reference voltage is to add a CTAT – to cancel its temperature dependence
Li *et al*. (2019)	• Use triple-well NMOS transistor • Control pumping clock's amplitude continuously o · To lessen the sensitivity of the output voltage to temperature variations

CHAPTER 3

METHODOLOGY

3.1 Block Diagram

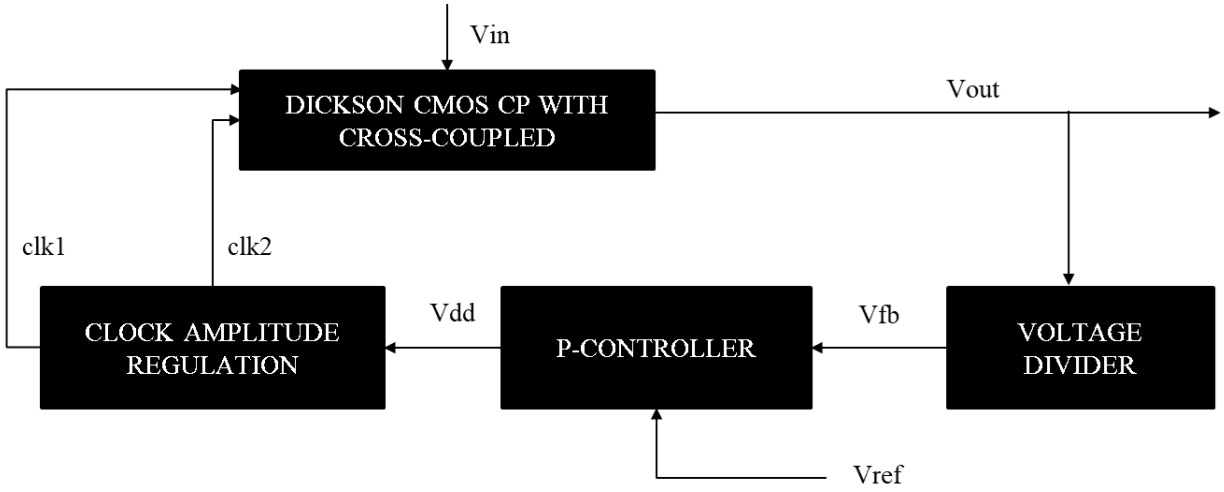

Figure 11: Block diagram of CMOS Charge Pump with Temperature Variations for Self-Powered Applications

The Dickson CMOS Charge Pump with Cross-Coupled configuration is shown in the diagram (Li *et al.*, 2019). The output voltage (Vout) is produced using this setup, which is specifically designed to raise the input voltage (Vin) to a greater level. In many electrical applications where greater voltage levels are necessary for optimum device performance, this

voltage boosting procedure is crucial especially an energy harvester application for a self-powered device where it produce a very low voltage input.

Cross-coupling is essential to the operation of this charge pump. This method connects the input of one stage with the output of the next stage. This unique configuration creates a voltage boosting relay where each stage gradually increases the voltage. The charge pump gathers energy from the input voltage and accumulates it to give the amplified output through this cross-coupled architecture.

The clock signals, suitably designated as clk1 and clk2, power this circuit. The charging and discharging cycles within each step are coordinated by these clock signals. The capacitors' alternating nature causes them to build up and release charge, which ultimately aids in the voltage amplification process. A smooth energy transfer cycle between stages depends on the synchronized execution of these clock signals.

Additional modules that are integrated into this charge pump architecture serve crucial roles in adjusting and regulating its behaviour. The clock signals' amplitudes are controlled by the clock amplitude regulation module, which makes sure they are constant and ideal for efficient charge transfer. This module is essential for attaining accurate voltage boosting since it keeps correct clock amplitudes.

The P-controller, also known as a proportional controller, establishes a control loop that gives the charge pump's operation an extra layer of intelligence. It works by comparing the feedback voltage with a reference voltage via a feedback mechanism. Any voltage discrepancies are indicated by an error signal produced by this comparison. The amplitude of this error signal is then changed to modify clk1 and clk2's clock amplitudes. The P-controller works to reduce any differences between the required reference voltage and the actual output voltage through this closed-loop regulation.

A closed-loop control system continuously monitors its output and uses the data as feedback to modify and maintain the target output, or setpoint. The proportional controller generates an error signal after comparing the Vfb and Vref and before adjusting the clock amplitudes in the charge pump. The charge pump can continuously optimize its performance and maintain the output voltage near the required value thanks to this feedback loop.

The architecture in this study qualifies as a closed-loop control system by including feedback control components like the proportional controller and clock amplitude regulator, allowing it to self-regulate and maintain a constant output voltage despite changes in operating conditions. Despite variances in temperature, this system guarantees a consistent and regulated output voltage.

The Voltage Divider module is essential for the P-controller to operate properly. To create the Vfb, this module splits the amplified output voltage (Vout). It creates a voltage reference that replicates the output voltage by doing this. The P-controller's comparison mechanism relies on this feedback voltage to help regulate and maintain the output voltage within the specified range.

Overall, the Dickson CMOS Charge Pump with Cross-Coupled design exemplifies a complex interaction between clock signals, voltage division, feedback control, and energy transfer mechanisms. This combination of modules and ideas results in a voltage boosting method that is effective and efficient and is necessary for powering various electronic systems and gadgets that need greater operating voltages. The charge pump's design not only exemplifies cutting-edge engineering but also highlights the complexity required to provide precise and controlled voltage amplification.

3.2 Flowchart

Figure 12 shows the step-by-step procedure for building a CMOS Charge Pump specifically suited for self-powered applications. Cadence Virtuoso simulator software will be used for both the schematic design and simulation. Estimating the values for each component element based on the design requirements and charge pump component parameters is the first step in this design procedure. Iterative optimization through several simulations is the key component of the charge pump design process until the required charge pump performance is obtained.

Power consumption, the charge pump's capacity to step up a low input voltage to 1V, and its ability to keep a consistent output even when exposed to temperature changes are important factors influencing its performance. The circuit is thoroughly evaluated, modified as necessary, and the component characteristics are correctly altered to guarantee the charge pump complies with these crucial parameters. It is critical to revaluate and modify the circuit's design and parameters as necessary if it doesn't operate as expected. The optimization method, however, presents an inherent challenge because changing the circuit design to improve one performance parameter may unintentionally cause other performance parameters to degrade. To strike a balance and produce an overall efficient charge pump design that complies with the necessary criteria, this necessitates caution and care throughout the design process.

The CMOS Charge Pump can be precisely customized to give the best performance in Self-Powered Applications by successfully navigating through this extensive design and optimization process. A strong charge pump will be produced by carefully considering power consumption, voltage step-up capabilities, and temperature resilience. This pump will be able to provide dependable power supply solutions in a variety of self-powered electronic systems and applications. The Cadence Virtuoso simulator was used as a potent tool to precisely simulate and fine-tune the charge pump design, enabling the achievement of the desired parameters and raising the overall effectiveness and efficiency of the charge pump.

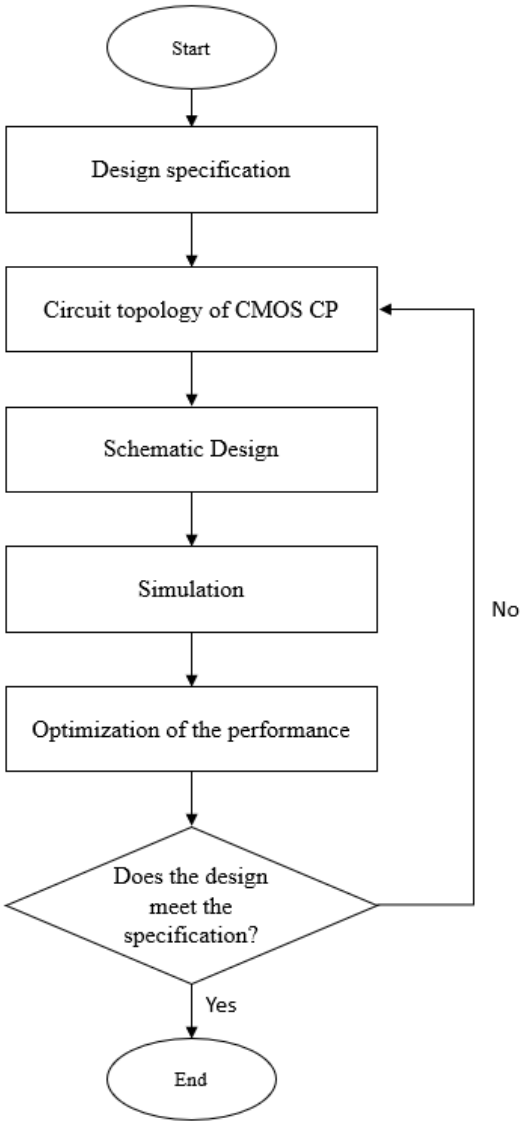

Figure 12: Methodology for CMOS Charge Pump with Temperature Variation for Self-Powered Device

CHAPTER 4

PROPOSED DESIGN

4.1 Charge Pump Circuit

The first proposed design A that being experiment was shown in Figure 13. This circuit consists of both NMOS and PMOS transistor as well as capacitors. The Dickson CMOS charge pump is a circuit configuration that utilizes a combination of capacitors and transistors to efficiently boost or step up the input voltage to a higher level. This design leverages the principle of charge transfer between capacitors through controlled switching of transistors. Capacitors store electrical charge, and by alternately connecting them in series and parallel configurations using transistors, the voltage across the capacitors accumulates and results in an elevated output voltage. The Dickson charge pump is known for its simplicity and effectiveness in voltage multiplication, making it valuable for applications where a higher voltage level is required than the available input voltage. This approach finds applications in diverse fields such as power management, voltage conversion, and energy harvesting due to its ability to generate higher output voltages without the need for external power sources.

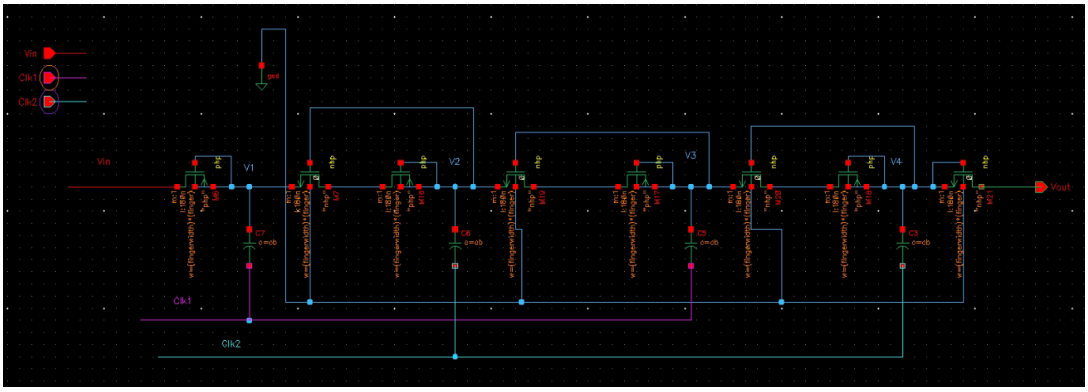

Figure 13: Design A - Dickson CMOS charge pump

Due to its restrictions, proposed design A only produces an output voltage that from input voltage of 0.5V to 732.021mV, according to the performance evaluation. Due to this restriction, it was decided to use a cross-coupled Dickson charge pump. This decision was made due to the cross-coupled Dickson configuration's enhanced ability to achieve larger output voltages, as seen by its capacity to reach 2.1579V. The next chapter will go further and provide a thorough analysis of these results, providing a thorough understanding of the justification for this choice and its ramifications for the functioning of the entire system.

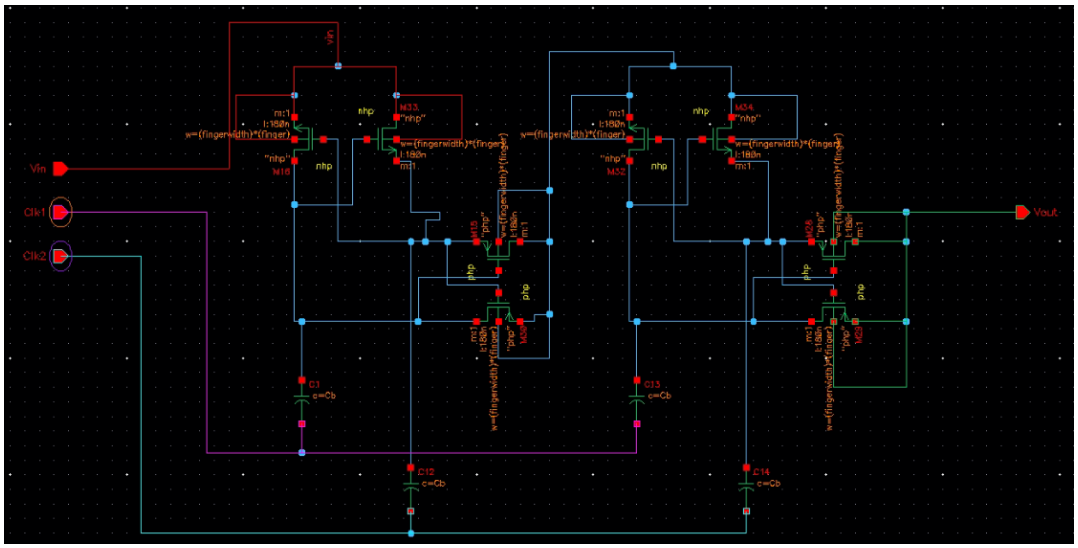

Figure 14: Design B - Dickson with cross-coupled CMOS charge pump

The final design for subsequent studies is depicted in the image in Figure 14 above. In this architecture, CMOS transistors are cross coupled together. This approach was chosen because, as Rahman *et al*. (2021) have shown, it is excellent for capturing energy, particularly when we have modest inputs like 250mV. We also considered the findings from Librado & Hora (2022), who demonstrated that connecting specific transistors can enhance the performance of variables such as output voltage, power consumption, and current strength. Design B became the preferred option for the suggested design as a result of this cross-connected approach being used on it.

Based on paper written by Bose *et al*. (2019) to address the issues challenges faced in conventional Dickson charge pumps, particularly at low input voltages., a proposed cross-coupled charge pump is introduced, featuring gate boosting of switches using outputs from preceding stages. The charge pump consists of two sections, each comprising six-stage complementary dual-phase charge pumps.

In this cross-coupled arrangement, the positive charge pump boosts the gate drive of NMOS switches in one area while the negative charge pump boosts the gate drive of PMOS switches in the other section. This is accomplished by employing a dynamic level-shifting circuit to couple complementary outputs from several stages. The conductivity of switches is increased by the enhanced gate signals, which increases charge transfer effectiveness at low input voltage levels. Dynamic level-shifting must be carefully designed in order to prevent reverse charge flow. Utilizing NAND gates and inverters running on a sub-100 mV supply, non-overlapping clock phases are produced. Both positive and negative voltages are supported by triple-well MOS transistors, and appropriate connections are created to guarantee reverse-bias of junctions under all circumstances. Comparatively to traditional Dickson charge pumps, this cross-coupled charge pump design offers increased charge transfer efficiency and greater power output, making it more appropriate for low input voltage applications.

Based on the papers studied in Literature Review, the final proposed design of the charge pump, known as Design B, incorporates the cross-coupled technique to leverage its various

benefits. Design B is anticipated to demonstrate higher performance qualities because of using the cross-coupled technique, making it ideal for energy harvesting systems and self-powered applications. Design B is positioned as a promising solution for self-powered electronic devices and other energy-efficient applications due to its capacity to accept low input voltages as well as general improvements in important parameters like power consumption, current driving capabilities, output voltage, delay voltage conversion ratio, and current driving capabilities. The performance of Design B will be validated and optimized by additional testing and simulations using the Cadence Virtuoso simulator software, ensuring that it satisfies the required criteria and offers an effective and dependable charge pump solution.

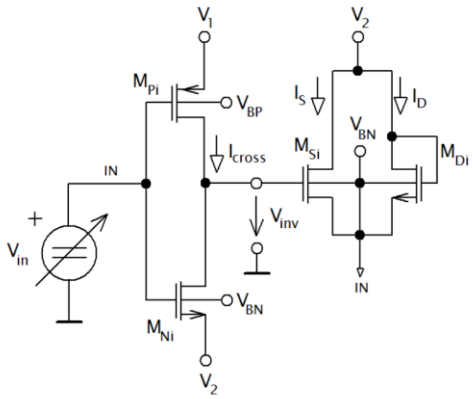

Figure 15: Cross-coupled charge pump (Marek, Hospodka, and Šubrt, 2017)

The cross-coupled charge pump works in multiple stages, with each stage consisting of a pair of inverters. Here is a step-by-step explanation of how the charge pump operates (Marek, Hospodka, and Šubrt, 2017):

Stage 1: The input voltage is applied to the gates of the PMOS and NMOS transistors in the first inverter. The output voltage is taken from the drains of these transistors. The inverter cross current, Icross and the switch current, Is flow through this stage.

Stage 2: The second inverter's transistor gates receive the output voltage from Stage 1 as their input voltage. These transistors' drains provide Stage 2 with its output voltage. Once more, the switch current and inverter cross current pass through this stage.

Stages 3 and up: The output voltage from the stage before is fed as the input voltage to the transistor gates in the step after. For each succeeding stage, this procedure is repeated.

The cross-coupled charge pump works by using the switch current and inverter cross current to produce an output voltage greater than the input voltage. The voltage levels of the input and output terminals dictate the precise voltage levels and currents in each step.

A viable and effective option for self-powered applications and energy harvesting systems, the cross-coupled configuration of the CMOS Charge Pump enables increased power efficiency, decreased ripple in the output voltage, and dependable operation of the transistors. The latch-based charge transfer mechanism and the usage of complementary clocks make the cross-coupled CMOS Charge Pump an attractive option for different low-power electronic applications.

4.2 Test Bench

The suggested charge pump circuit's testbench is an essential tool for assessing the circuit's operation and performance. It makes it possible to thoroughly analyze how the circuit behaves under various operating circumstances and input scenarios. The testbench's objective is to evaluate the reaction of the charge pump to various voltage inputs as well as the effect of the charge pump's dual clock functioning on the voltage output.

There are two testbenches that being proposed here to test with a wide range of temperature of -40ºC until 40ºC:

1. **Testbench TB1:** This testbench is employed during the first semester of the project. It is characterized by the utilization of a Dickson Charge pump configuration, incorporating solely two clocks, voltage input, and a load component. Notably, this system operates within an open-loop framework, facilitating initial testing and evaluation. This testbench is used to test both proposed design A and B.
2. **Testbench TB2**: During the second semester, the project shifts its focus to the deployment of Testbench TB2. Unlike TB1, this testbench exhibits an expanded design. It encompasses not only the Dickson charge pump but also incorporates essential components such as a voltage divider, a proportional controller, and a clock amplitude regulator. A significant departure from the open-loop structure, this configuration operates within a closed-loop system, effectively harnessing feedback mechanisms to optimize and regulate the performance of the charge pump circuitry.

The results obtained from these two testbenches will be discussed in more detail in the next chapter. The outcome from Testbench TB1 was examined, which involves a simpler setup with a Dickson Charge pump and a few components, as well as the results from Testbench TB2, which includes more elements like a voltage divider, proportional controller, and clock amplitude regulator in a closed-loop setup.

Testbench TB1

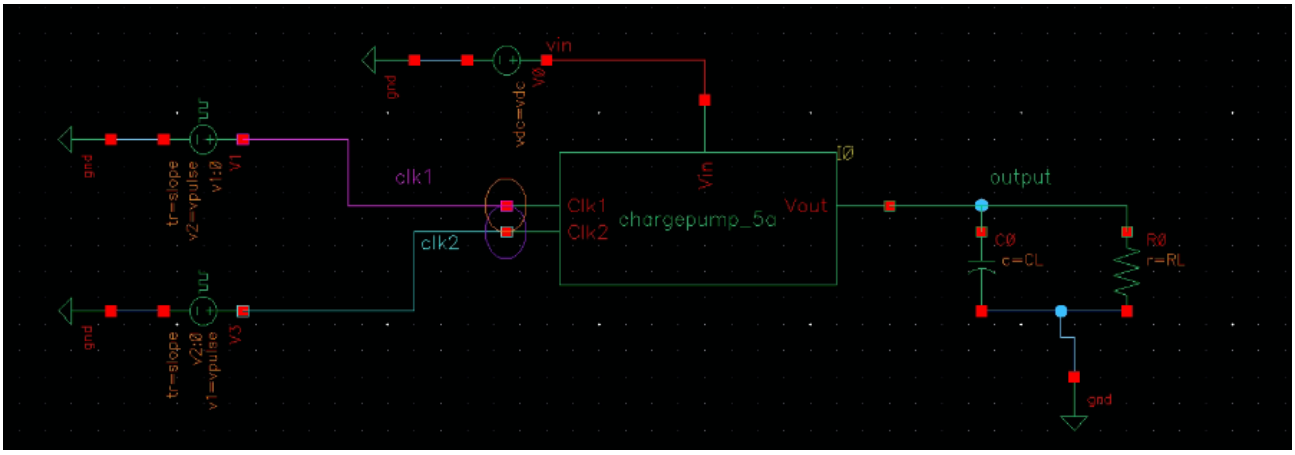

Figure 16: Testbench of CMOS Charge Pump with Temperature Variation for Self-Powered Applications (temperature sensitive) – Testbench TB1

Based on Figure 16 by which is the testbench without any circuit to make the charge pump insensitive to temperature, the first input to the testbench is the voltage input, which serves as the primary power source for the charge pump circuit. This voltage input simulates the real-world scenario where the charge pump would typically operate with different temperature. The two clocks used in the testbench are the positive clock, clk1 and the negative clock, clk2. The clk1 determines when the charge transfer switches are turned on and active, allowing the charge pump to transfer charge effectively between capacitors and generate an output voltage. Conversely, clk2 controls the turn-off phase of the switches, ensuring proper switching and avoiding unwanted charge transfer during clock transitions.

The voltage output of the charge pump is connected to both a load capacitor and a load resistor. The load capacitor represents the capacitive load that the charge pump must drive, mimicking the conditions it would face in practical applications. The load resistor, on the other hand, represents the resistive load that the charge pump must overcome while driving the output voltage. By including both capacitive and resistive loads in the testbench, the circuit's performance under varying load conditions can be thoroughly evaluated.

During the simulation of the testbench, the behavior of the charge pump circuit is observed concerning its output voltage with respect to the input voltage and clock signals. This analysis helps to determine the charge pump's efficiency in transferring charge and generating the desired output voltage. It also enables the identification of any potential voltage droop or ripple in the output due to the switching action of the charge pump. The testbench results are then thoroughly analyzed and compared against expected performance metrics and design goals. If the proposed charge pump circuit exhibits higher pumping efficiency, reduced ripple, and stable output voltage under various input and load conditions, it validates the effectiveness of the cross-coupled structure and the use of PMOS transistors as charge transfer switches.

Testbench TB2

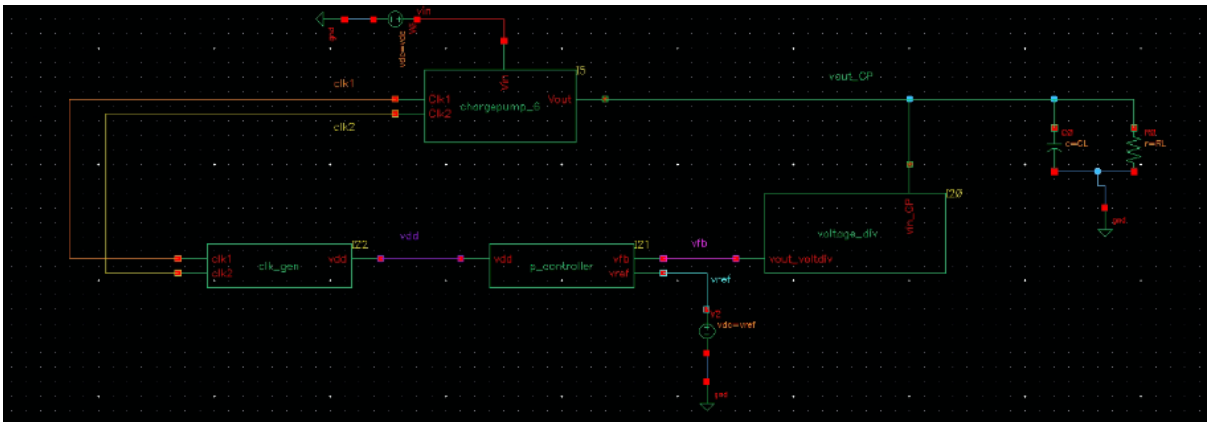

Figure 17: Testbench of CMOS Charge Pump with Temperature Variation for Self-Powered Applications (temperature insensitive) – Testbench TB2

The testbench described above is an essential part of the charge pump design based on the block diagram presented in Chapter 3. This testbench was being used in further simulation to make the charge pump insensitive to temperature. It comprises three crucial components: a voltage divider, Proportional Controller, and a Clock Amplitude Regulator (Li *et al*., 2019).

Voltage Divider

In line with the research of Ballo, Grasso, and Palumbo (2020), in a sensor circuits, when the output voltage of the sensor must be scaled down to meet the input range of an analog-to-digital converter (ADC), voltage dividers are frequently used. The sensor output voltage can be divided by a voltage divider to a level that is suitable for the ADC's accurate measurement.

In charge pump applications, a voltage divider could be required to modify the charge pump circuit's output voltage level. The output voltage of the charge pump can be divided to a specific level using the voltage divider. For instance, a voltage divider can be used to scale down the charge pump's output voltage to match the input voltage needs of the load or storage device when designing a regulated charge pump for energy harvesting applications (Kim, Kim, and Kim, 2011) By doing this, the output voltage is ensured to be within the range that the associated components can tolerate.

The voltage divider plays a fundamental role in sampling the output voltage, Vout and providing the feedback voltage, Vfb for further processing. After obtaining VFB, it is compared with a reference voltage, Vref to determine any deviations from the desired output voltage level. This comparison serves as a critical feedback mechanism, allowing the Proportional Controller to make precise adjustments to the charge pump's operation. The Proportional Controller utilizes the error signal generated by comparing VFB with VREF and employs a proportional gain to determine the required changes in the clock amplitudes.

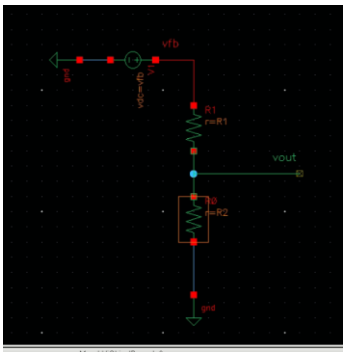

Figure 18: Schematic diagram of voltage divider

Proportional Controller – Operational amplifier

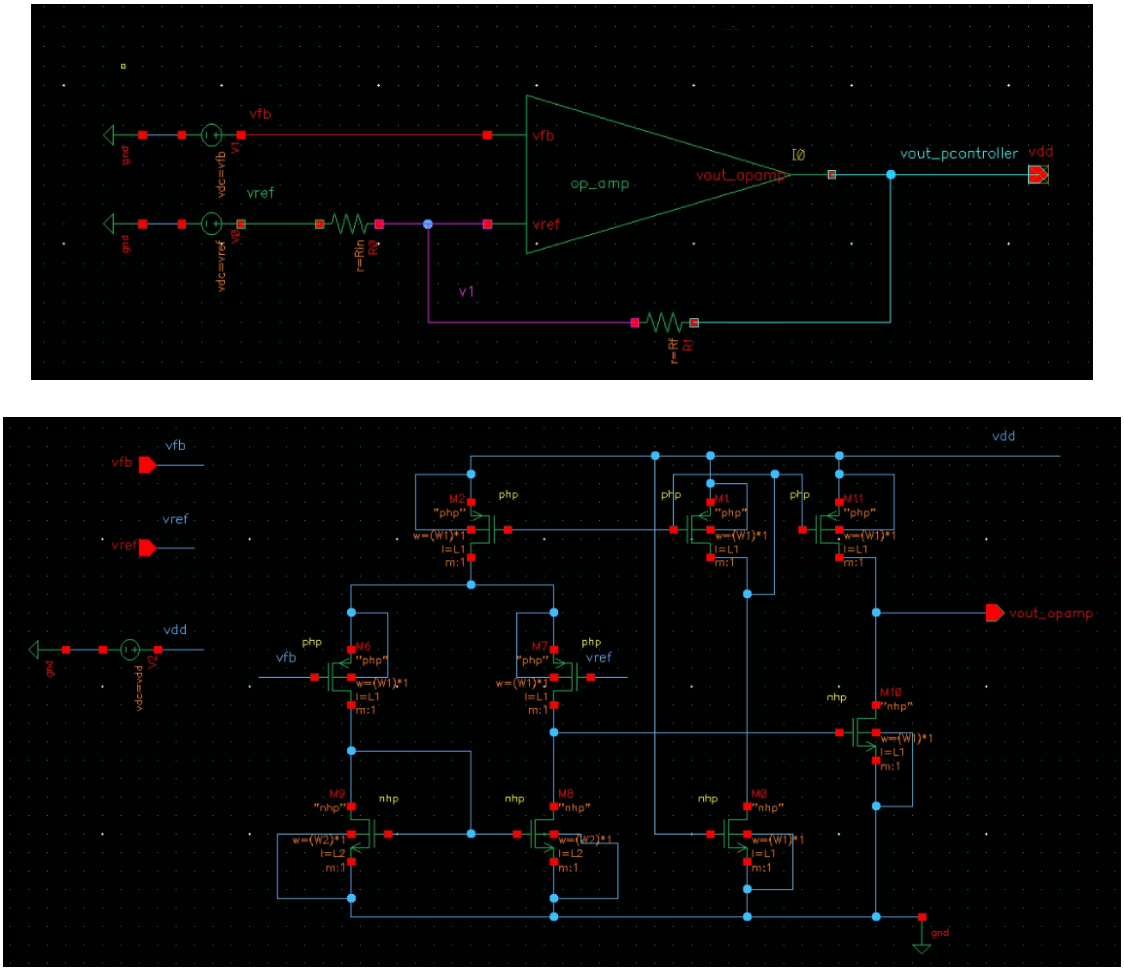

Figure 19: Schematic diagram of proportional controller (above) and operational amplifier (below)

One of the fundamental approaches to the field of control systems is proportional control. The output signal of the system and the input signal of the P controller continue to be proportionate. Its primary goal is to calibrate the system's open-loop gain, which improves the system's steady-state performance precision while reducing internal inertia and accelerating overall responsiveness. The integral control law or the derivative control law are frequently used in conjunction with the proportional control strategy when designing system calibrations because their combination creates a more robust and efficient control mechanism. Aligned with the analysis by Wang, Zhou, & Ma (2019) reveals that proportional control consistently generates static error and cannot be avoided.

The Proportional Controller's output, based on the error signal and the proportional gain, is then used to regulate the up level of the clk1 and clk2 clock signals. Through this clock amplitude regulation, the charge pump's switching behaviour is finely controlled to maintain the output voltage at a fixed value. By continuously monitoring and adjusting the clock amplitudes, any variations in the output voltage are corrected, ensuring the charge pump consistently delivers the desired voltage level.

In a P controller system, the operational amplifier is responsible for comparing the two inputs: the feedback voltage and the reference voltage. The operational amplifier amplifies the voltage difference between these two inputs to generate the error signal. The error signal represents the deviation of the output voltage from the desired value (setpoint). The P controller, on the other hand, uses this error signal to regulate the waveform or output voltage of the system. It adjusts the clock amplitudes of the charge pump based on the error signal to minimize the error and maintain the output voltage close to the reference voltage.

So, the operational amplifier’s primary function is to compare the feedback and reference voltages and amplify the resulting difference, while the P controller's role is to use the amplified error signal to control the charge pump's operation and regulate the output waveform. The combination of these two components enables effective feedback control and ensures a stable and regulated output voltage in the P controller system.

Clock Amplitude Regulator – Not Gate

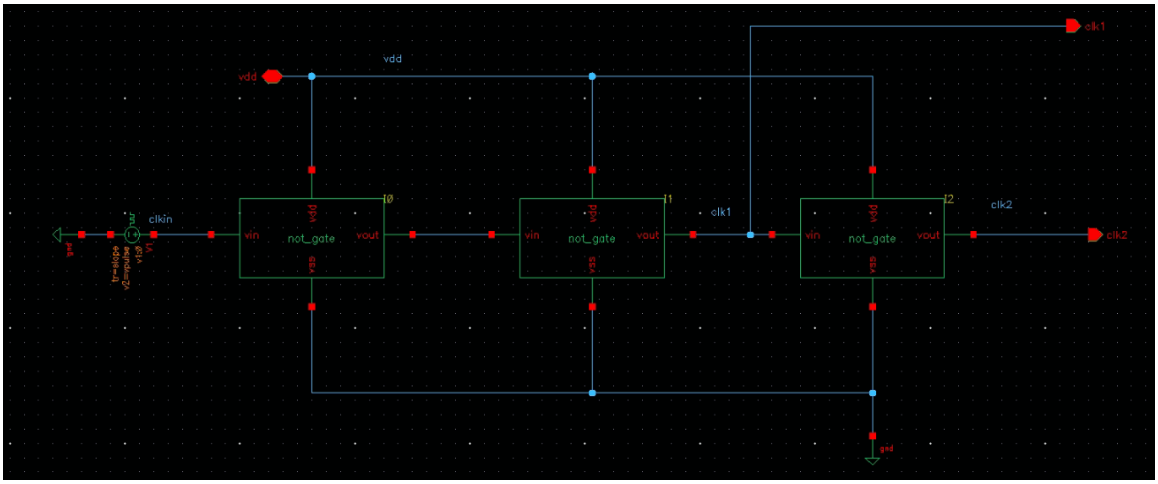

Figure 20: Schematic diagram of clock amplitude regulator

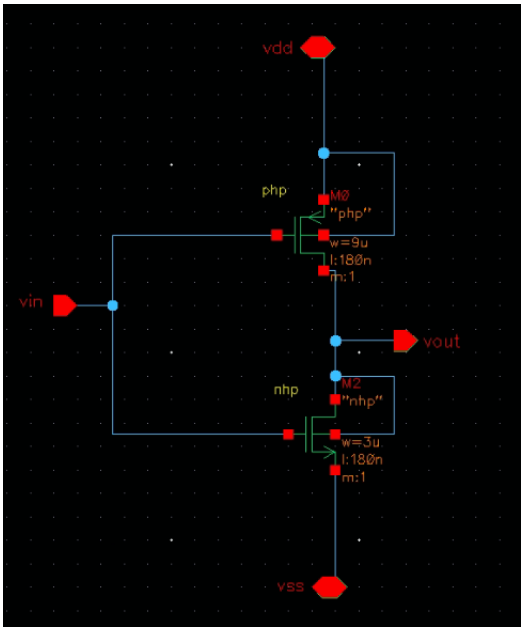

Figure 21: Schematic diagram of NOT gate

An oscillator circuit called a ring oscillator has an odd number of inverter stages connected in a loop. Reflecting the findings of Yoon, Carreon-Bautista, & Sánchez-Sinencio (2018), Each inverter stage is made up of a transistor pair (M1 and M2) that continuously oscillates by switching

back and forth between the on and off states. The loop is completed by feeding the output of the last inverter step back into the input of the first stage.

A ring oscillator's main objective is to produce a signal that continuously oscillates at a frequency set by the time taken to complete each inverter stage. It frequently serves a variety of functions in digital systems, including clock generation, frequency synthesis, and timing generation. This clock amplitude regulation mechanism is crucial in achieving a stable and precise output voltage. It enables the charge pump to respond dynamically to changes in temperature fluctuations. The Proportional Controller's ability to fine-tune the clock amplitudes in real-time ensures that the charge pump operates efficiently and reliably under various operating conditions.

On the other hand, a ring oscillator structure was used in this study, with inspiration from Li *et al*. The three inverters that make up the ring oscillator, a key part of the research, each serve as a not gate in a series. To be more precise, a continuous feedback loop is created when the output of the first inverter is used as the input for the next inverter. The output of the second and third inverters are used to strategically derive the clock signals, designated as clk1 and clk2, respectively.

Overall, the testbench variables are thoughtfully designed to provide a thorough and accurate assessment of the proposed charge pump circuit's performance under realistic conditions, covering voltage levels, clock characteristics, and operating frequencies encountered in practical applications. By evaluating the charge pump against these variables, the testbench can validate the circuit's efficiency, stability, and suitability for low voltage applications with high pumping efficiency.

CHAPTER 5

RESULT & DISCUSSION

This chapter will explain the result and discussion of each two testbenches where:

Testbench TB1: This test was done in the first semester. It used a simple setup with a Dickson Charge pump, two clocks, voltage input, and a load. This system tested things out without a feedback loop, helping us understand the basics.

Testbench TB2: In the second semester, we focused on Testbench TB2. This one was more advanced than the first. It not only had a Dickson charge pump but also included important parts like a voltage divider, a proportional controller, and a clock amplitude regulator. Unlike the first test, this one had a feedback loop, which helped us fine-tune the charge pump's performance and control how it works.

5.1 Simulation using Testbench TB1

The testbench for evaluating the proposed charge pump circuit incorporates various variables to comprehensively assess its performance. These variables, as shown in the table below, are carefully chosen to mimic real-world operating conditions and to stress-test the charge pump circuit under different scenarios. Table below shows the variable that the testbench used. The

voltage input and voltage pulse for both clocks are 500mV where the charge pump will pump the voltage into 1V. The clocks had a slope of 5n, delay of 1n, period of 1/frequency and a duty cycle of half of period. The frequency of the testbench is 1MHz.

Table 5: Values of component and variable for proposed charge pump topology

Variable	Value
Vin	0.5V
Vpulse	0.5V
Capacitor load, CL	40pF
Resistor load, RL	700kOhm
Slope	5n
Delay	1n
Frequency	10MHz
Period	1/frequency
Duty cycle	Period/2

Table 6: Value of finger, finger width and capacitor boost for proposed charge pump topology.

Variable	Value
Finger	2
Finger width	5 µm
Capacitor boost, Cb	2pF

Table 6 displays the capacitor values utilized in each of the designs discussed earlier, consistently set at 2pF. Additionally, the transistor width for all designs was maintained at 10 µm. The results obtained from simulations of Design A and Design B were taken at a time interval of

25 µs. These simulation outcomes are documented in the subsequent table, Table 7. The findings in Table 7 confirm the superior output voltage generation of the cross-coupled charge pump when compared to the standard Dickson CMOS charge pump. As a result of this performance superiority, the cross-coupled charge pump was selected as the final topology for this study, as illustrated in Figure 14.

Table 7: Result for Design A and Design B

Circuit	Voltage output
Design A – Dickson CMOS charge pump	732.021mV
Design B – Dickson with cross-coupled CMOS charge pump	2.1579V

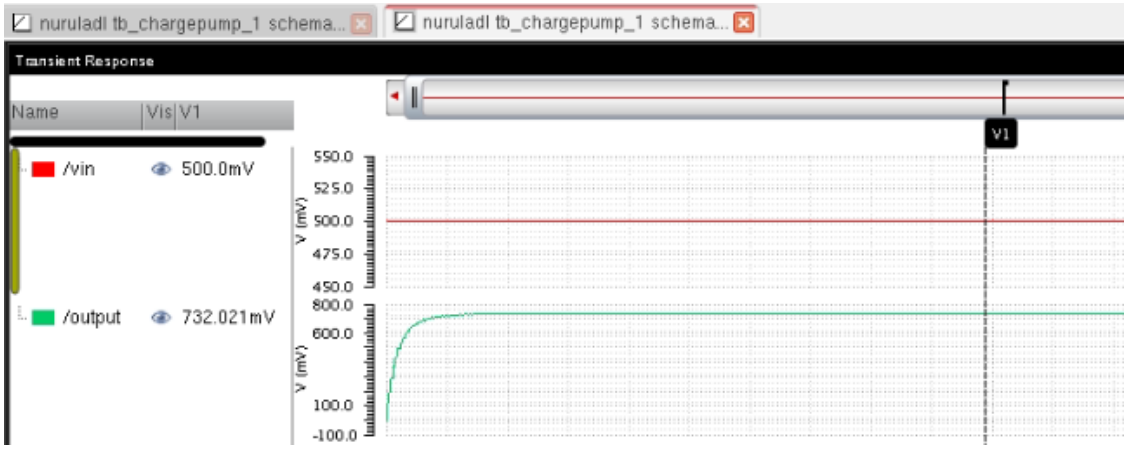

Figure 22: Result of Dickson CMOS charge pump at time = 25 µs

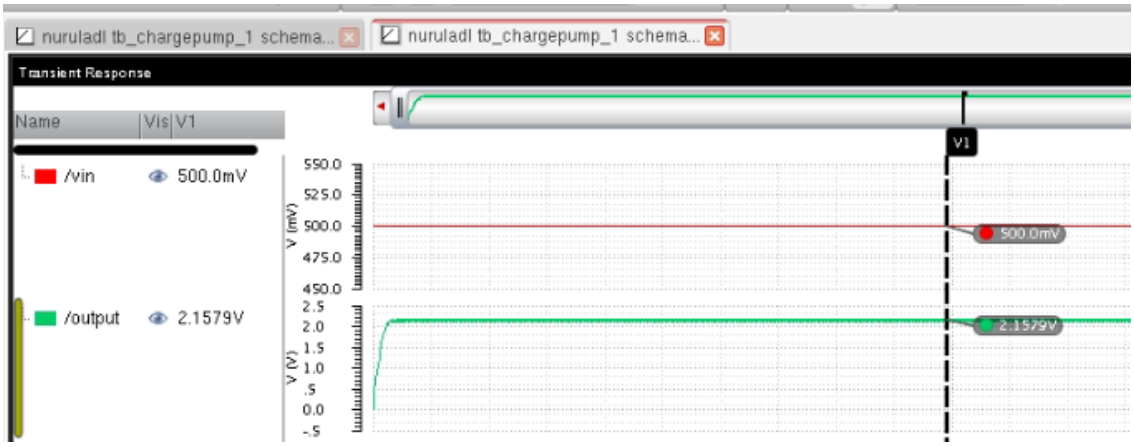

Figure 23: Dickson with cross-coupled CMOS charge pump at time = 25 µs

As mentioned in one of this paper's objectives that the charge pump would need to provide a voltage output of 1V. Therefore, the value of width, capacitor's boost and resistor's load were adjusted accordingly to achieve 1V and being illustrated in consequence graph. The initial output voltage was 2.1584V which are above of the needed output voltage. Hence, the experiment was done with larger width to achieve a near possible 1V. The experiment of adjusting value of width, capacitor's boost and resistor's load were described in below graph and table respectively. For the final experiment that used Proposed Design B, the proposed circuit will take the width of 40 µm, resistor's load of 700kOhms and boost capacitor of 0.8pF. All this experiment's result was taken at time 25 µs

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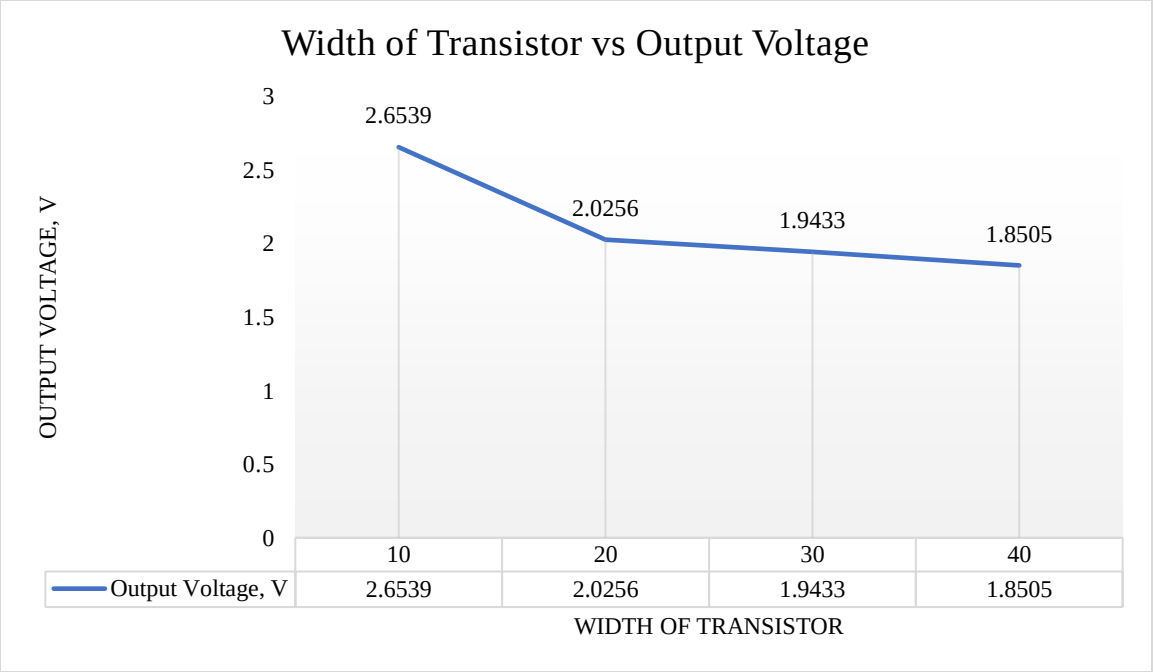


Figure 24: Graph of width of transistor and output voltage

The graph above displayed in Figure 24 provides a visual representation of how the width of a transistor changes, ranging from 10 µm to 40 µm. Interestingly, as the width of the transistor grows larger, the output voltage tends to decrease. In the pursuit of achieving an output voltage of 1V, a crucial requirement for this charge pump design, it becomes evident that opting for a transistor width of 40 µm holds significance. This choice is particularly notable because it corresponds to the lowest output value, aligning seamlessly with the desired 1V output voltage target. Thus, this specific width of 40 µm is strategically identified as the optimal option to fulfil the charge pump topology's voltage requirement.

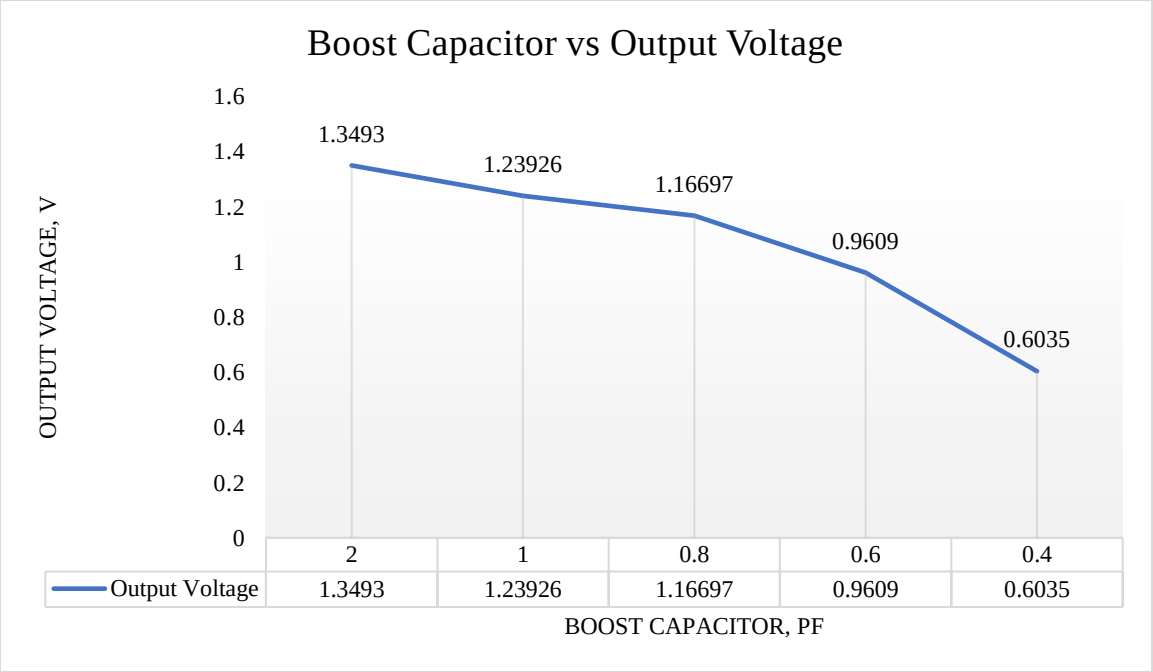


Figure 25: Graph of boost capacitor and output voltage

Once the decision regarding the transistor width had been settled, an experiment was carried out to determine the appropriate value for the boost capacitor, which is a critical component in the charge pump. The experimentation spanned a range, commencing with a value of 2pF and descending to 0.4pF. After meticulous analysis, the optimal value of the boost capacitor was determined to be 0.8pF. This choice is rooted in its proximity to the desired 1V output voltage. Selecting a boost capacitor value that is nearer to the target output voltage underscores the precision and effectiveness of this decision, further enhancing the overall performance of the charge pump system.

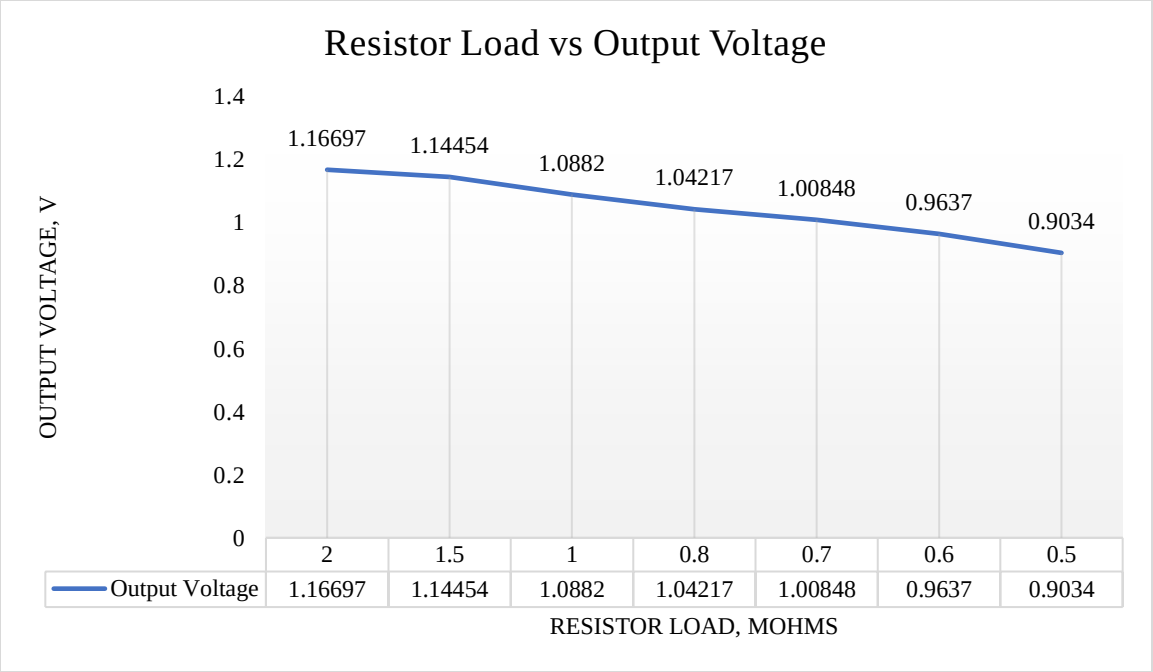


Figure 26: Graph of resistor load and output voltage

Continuing in the direction indicated by the graph illustrated in Figure 26, the subsequent step is to ascertain the suitable value for the resistor load within the circuit. The experimentation encompassed two values: an initial testing with a 2Mohm resistor load, followed by a subsequent reduction to 500kOhms. After comprehensive analysis, the selected resistor load value is 700kOhms. This resistor load value aligns harmoniously with the objective of generating an output voltage of around 1V. Specifically, this configuration yields an output voltage measuring approximately 1.00848V, affirming the alignment of the chosen resistor load with the desired outcome. This meticulous selection of the resistor load value contributes to optimizing the charge pump's performance in achieving the targeted output voltage.

The subsequent table provides an overview of the definitive values assigned to each individual component within the circuit, along with the corresponding variables integrated into the testbench. This comprehensive compilation aims to facilitate experimentation by assessing the resulting output voltage under the influence of varying temperature inputs within the circuit.

Table 8: Final Value of Each Component and Variable for Proposed Design B

Variable	Value
Width of transistor	40µm
Capacitor boost	0.8pF
Capacitor load	40pF
Resistor load	700kOhms
Vin	0.5V
Vpulse	0.5V
Capacitor load, CL	40pF
Resistor load, RL	700kOhm
Slope	5n
Delay	1n
Frequency	10MHz
Period	1/frequency
Duty cycle	Period/2

This comprehensive set of values ensures the systematic experimentation of the circuit, offering valuable insights into the behavior of the output voltage when subjected to temperature fluctuations. The integration of these specific component values and variables serves to optimize the accuracy and precision of the assessment, ultimately contributing to a deeper comprehension of the charge pump's performance characteristics.

To investigate the impact of temperature variations, the circuit underwent experimentation across a range of temperatures. Notably, the output voltage exhibited a consistent trend of diminishing in tandem with decreasing temperatures. This relationship is evident in both the visual representation provided by the graph below and the corresponding data captured within the accompanying table. This substantial correspondence between temperature and output voltage underscores the circuit's sensitivity to thermal changes and underscores the importance of accounting for temperature effects when analysing its performance.

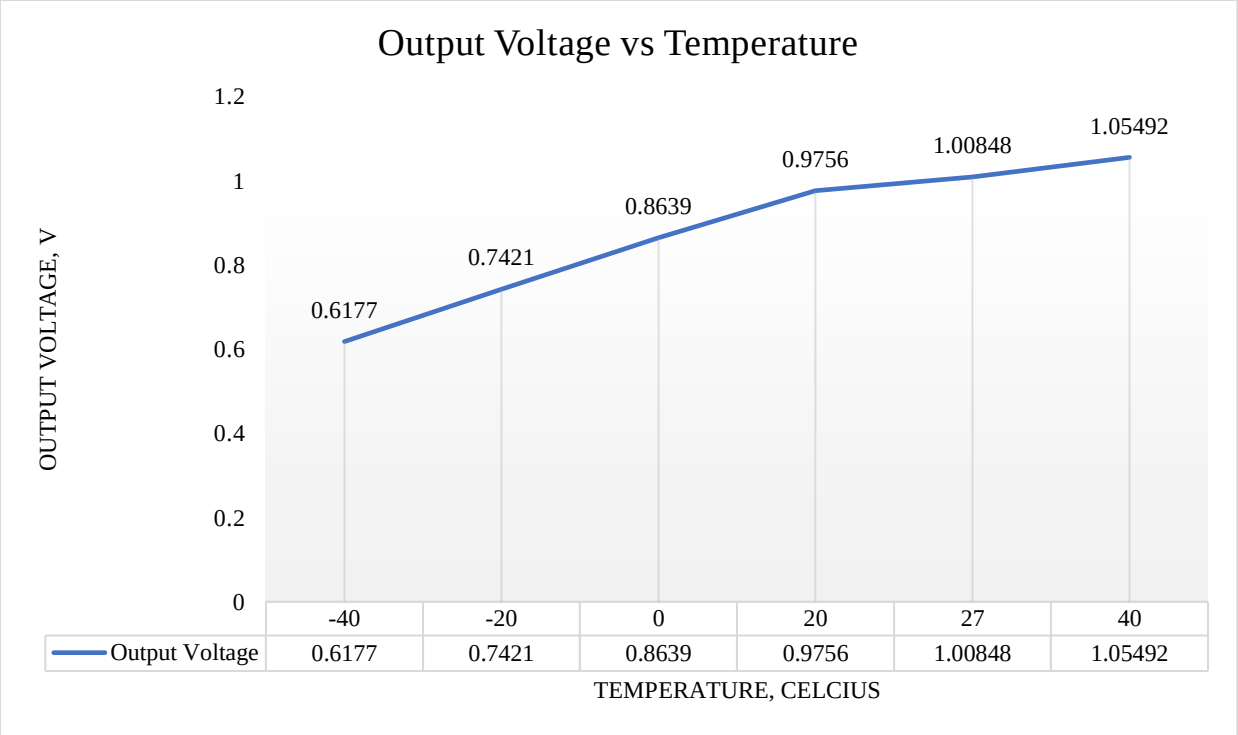


Figure 27: Graph of temperature and output voltage

The graph depicted above offers insight into the output voltage's behavior across a comprehensive temperature spectrum, ranging from -40 to 40 degrees Celsius. Evidently, the output voltage exhibits an irregular pattern as the temperature varies. Notably, at the default temperature of 27 degrees Celsius, the output voltage settles at 1.00848V. It's crucial to highlight that this temperature-based experimentation retained consistent component and variable values, ensuring a controlled setting. Additionally, the outcome measurements were taken at a fixed time point, specifically 25 µs. This comprehensive approach enables the evaluation of the circuit's response to temperature fluctuations under standardized conditions, unveiling the impact of varying thermal conditions on the output voltage's stability.

5.2 Simulation Using Testbench TB2

As the project progresses further, the focus shifts to the implementation of Testbench TB2, which displays an enhanced design. The Dickson charge pump itself is included, along with other essential components including a voltage divider, a proportional controller, and a clock amplitude regulator. This clearly differs from the previous open-loop layout. Instead, this newly designed configuration works as a closed-loop system, employing feedback mechanisms to skilfully regulate and keep an eye on the charge pump circuitry's operational efficacy.

- **Voltage Divider**

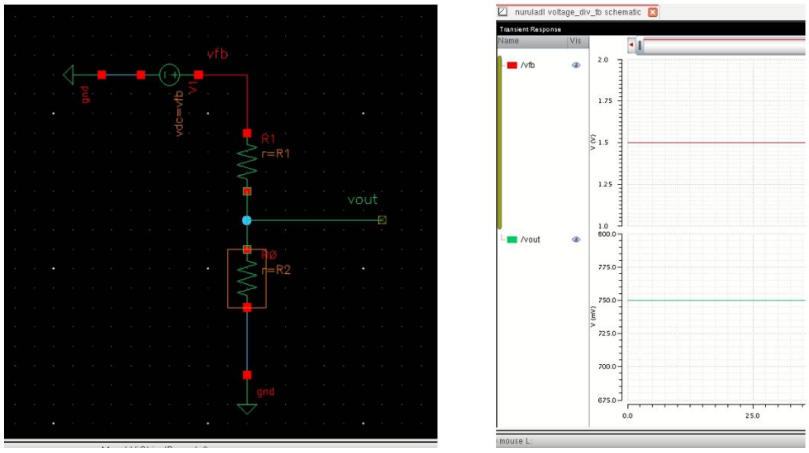


Figure 28: Schematic diagram and simulation of voltage divider

Table 9: Value of voltage divider

Variable	Value
Resistors, R1 & R2	20M Ohms
Vout_CP	1.5V
Vout	0.75V

The table gives an overview of the important variables and their associated values in a particular circuit or system. The first column relates to the resistors R1 and R2, each of which has a resistance value of 20 megaohms (M). These resistors play an important function in the circuit, such as voltage division or impedance management, which affect the distribution of voltage and current.

In keeping with the investigation of Li *et al*. (2019), the value of resistors should be large due to load capacity of the charge pump is weak. They used R1 and R2 are 119.0304 MΩ and 12.5005 MΩ, respectively. The simulation started with the same value as the paper, but the value was changed to 20MΩ for each resistor to make the output of circuit approximately to 1V.

Continuing, "Vout_CP" stands for the charge pump circuit's output voltage, which is 1.5 volts (V). The table above represents the amount of voltage that the charge pump produces or delivers, and it is essential for determining how well the circuit works. Finally, "Vout" refers to the overall output voltage, which is defined as 0.75 volts (V). This voltage value represents the system's overall output or, sometimes, the output of a particular circuit stage.

- **Proportional Controller**

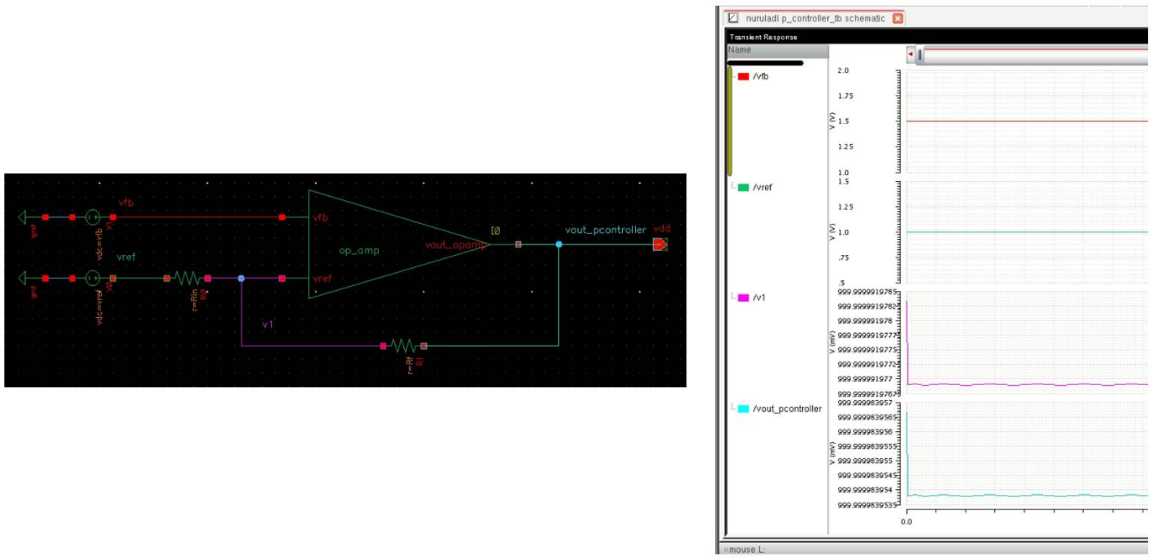


Figure 29: Schematic diagram and result for proportional controller

Variable	Value
Feedback resistor, Rf (P-controller)	200K Ohm
Input resistor, Rin (P-controller)	200K Ohm
Voltage reference, Vref (P-Controller)	1V
Voltage feedback, Vfb	1.5V
Vout_pcontroller	0.99999999 V (~1V)

Figure 30: Values for proportional controller

In the context of a proportional controller (P-controller) configuration, the key variables and their corresponding values are listed in the table that is being given. In this configuration, a system is controlled utilizing proportional control ideas. The information in the table provided sheds light on the numerous factors at play:

The values set for the "Feedback resistor, Rf" and the "Input resistor, Rin" are both 200K ohms. The impedance and characteristics of the feedback and input channels are controlled by these resistors, which play crucial roles in the P-controller setup and influence the controller's behavior. As a vital reference point for the controller's functionality, the "Voltage reference, Vref" is set to 1V. By using this reference voltage as a standard against which to compare the system's performance, the P-controller can produce the right control signals.

A feedback voltage of 1.5V is denoted by the phrase "voltage feedback, Vfb". This voltage serves as the system's output or response, which the controller compares to the required reference voltage to help the control loop make the necessary corrections. The output voltage is roughly 0.99999999 V, or practically 1V, according to the setting "Vout_pcontroller". This shows that despite little variations, the proportional controller was able to keep the output voltage near to the ideal reference level.

The table summarizes the essential elements of a P-controller configuration, illuminating the function of the input and feedback resistors, the reference voltage, the feedback voltage, and the obtained output. The controller's capacity to keep the system's output in step with the reference voltage is highlighted by this design, demonstrating how well proportional control principles work to regulate and stabilize the system.

- **Operational Amplifier**

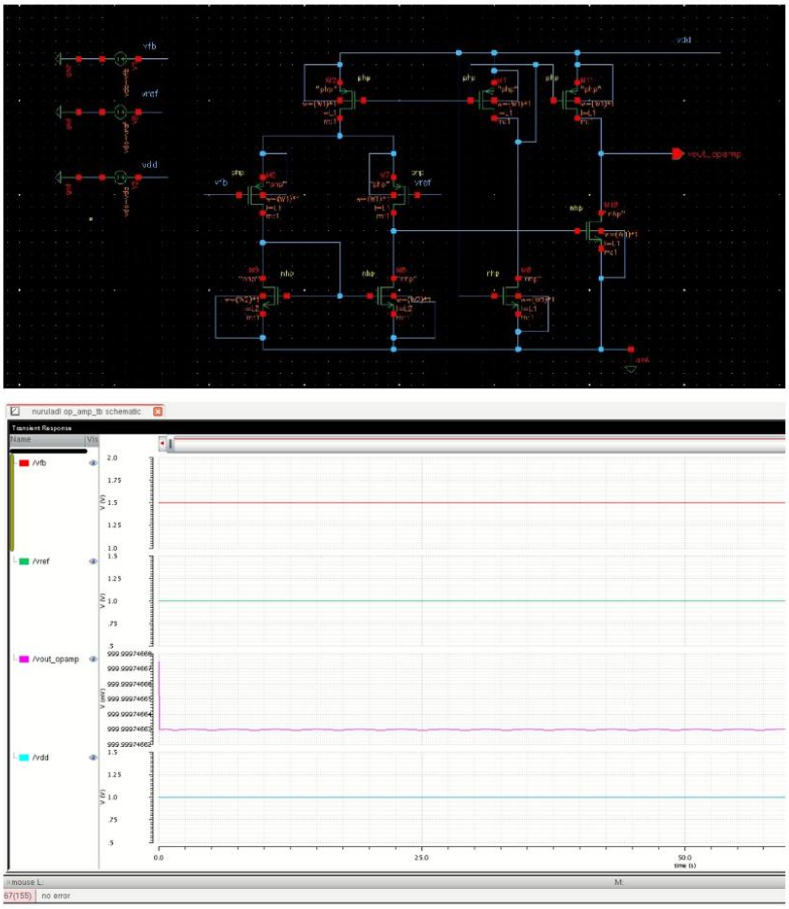


Figure 31: Schematic diagram and result for operational amplifier

In the context of an operational amplifier configuration, the key variables and their corresponding values are listed in the table that is provided. This configuration involves the precise transistor operational amplifier settings and associated voltages, providing information about the properties of the operational amplifier system.

It is specified that the "Width of transistor, W1" and "Width of transistor, W2" be 8 micrometers (u) and 16 micrometers (u), respectively. The transistors' size within the operational amplifier circuit are determined by these widths, which affects their conductance and overall

performance. Both the "Length of transistor, L1" and the "Length of transistor, L2" have the unit "micrometer" and are 8 u. In the operational amplifier architecture, the length of the transistors is just as important in defining their electrical characteristics as is their width.

At 1.5V, the "Voltage feedback, Vfb" is set. This voltage, which stands for the feedback signal from the operational amplifier's output, is crucial in shaping the behavior of the operational amplifier to match the intended performance. The value of the word "Voltage reference, Vref" is 1.0V. This reference voltage acts as a benchmark for the performance of the operational amplifier and is frequently compared to other signals to identify discrepancies or corrections.

Operational amplifier output voltage of 0.999999V, or roughly 1V, is what the value "Voltage output of Operational amplifier, Vout_opamp" denotes. This shows that the operational amplifier has successfully produced an output voltage that is extremely near to the desired 1V level.

Together, the table gives information about the precise factors affecting the transistor sizes, feedback and reference voltages, and output levels of the operational amplifier. These specifics shed light on the subtleties of the operational amplifier's functioning and demonstrate how well it can convert input signals into output signals while precisely preserving the proper reference and feedback levels.

Table 10: Values of operational amplifiers

Variable	Value
Width of transistor, W1 (Operational amplifier)	8u
Width of transistor, W2 (Operational amplifier)	16u
Length of transistor, L1 (Operational amplifier)	8u
Length of transistor, L2 (Operational amplifier)	8u
Voltage feedback, Vfb	1.5V
Voltage reference, Vref	1.0V
Voltage output of Operational amplifier, Vout_opamp	0.999999V (~1V)

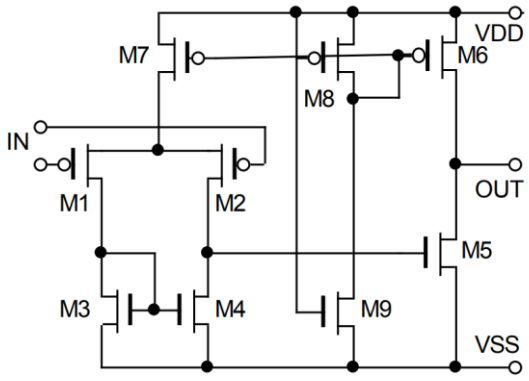


Figure 32: Circuit for operational amplifier by Kuzmicz et al.

An essential element in analogue circuits that amplifies the input signal is the operational amplifier. It typically includes an output stage, gain stages, and differential input stages. The operational amplifier works based on the negative feedback principle, whereby a portion of the output signal is given back to the input to regulate the total gain and effectiveness of the amplifier.

Aligned with the analysis by Kuzmicz *et al.*, two transistors which act as amplifier are M3 and M4, typically configured as a long-tailed pair, make up the differential input stage of the

operational amplifier and magnify the voltage difference between the two input terminals. High input impedance and common-mode rejection are provided by this stage, enabling the operational amplifier to block common-mode signals and enhance the differential signal.

Except for M3 and M4, all transistors have minimum sizes (for MOSFETs W/L=1). Two minimal size transistors connected in parallel are used to implement both M3 and M4 (effective W/L=2). As a result, all transistors have widths of 8u and lengths of 16u, except for M3 and M4, which have 16u widths. Due to the implementation of M3 and M4 in the operational amplifier as two minimum size transistors linked in parallel, which results in an effective W/L ratio of 2, they have distinct W/L ratios. This was done to ensure that both amplifiers received the same supply current.

- **Clock Generator – Not Gate**

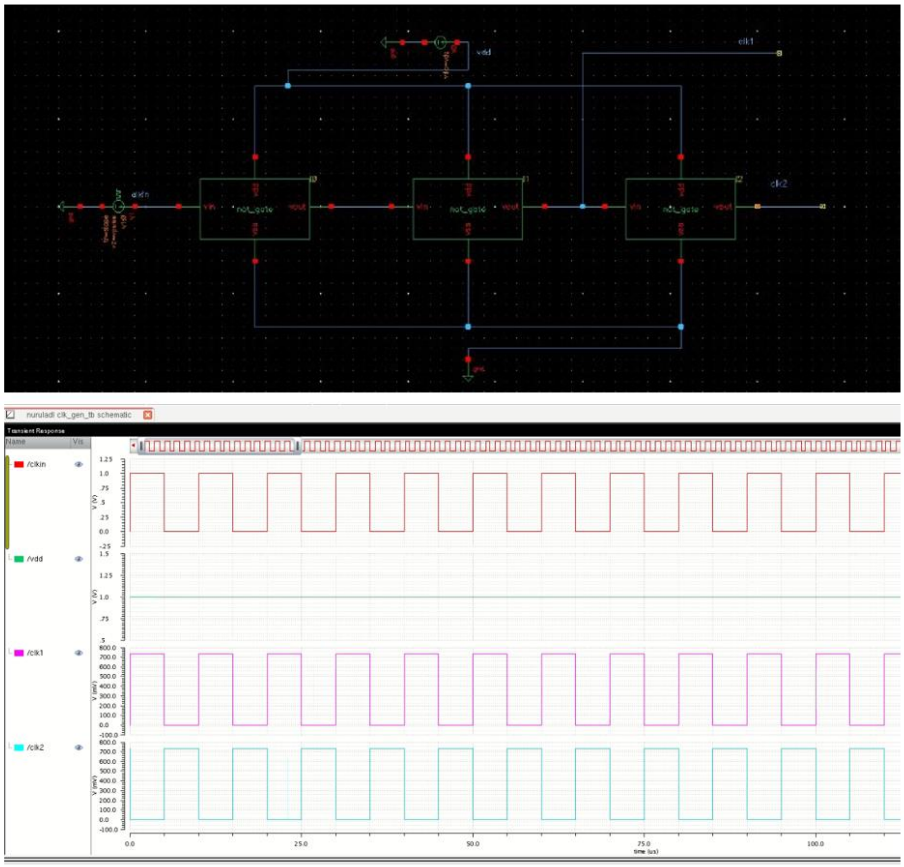


Figure 33: Schematic diagram and result for clock amplitude generator

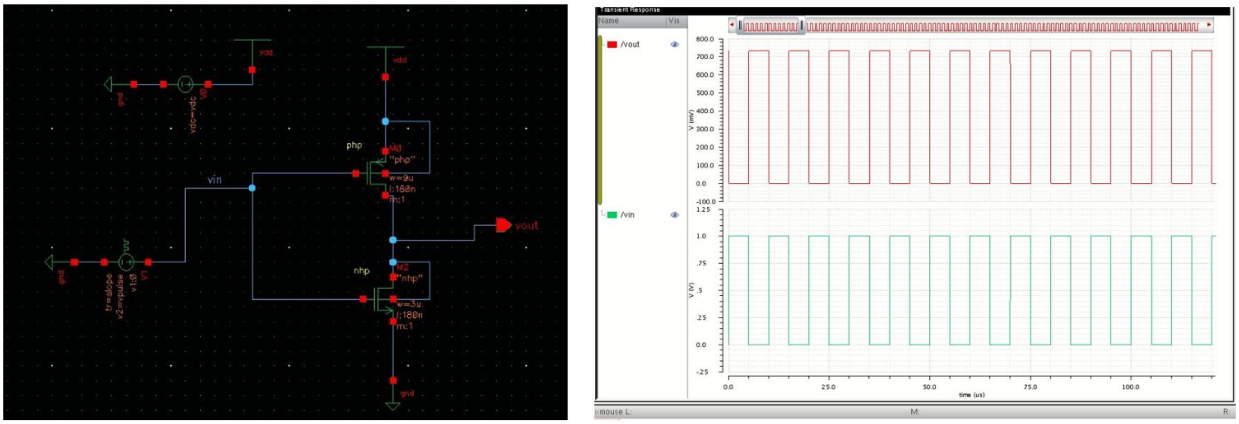


Figure 34; Schematic diagram and result for NOT gate

Table 11: Values of Testbench 2

Variable	Value
Width of transistor (Charge Pump)	40 µm
Capacitor boost (Charge Pump)	0.8pF
Capacitor load	40pF
Resistor load	700kOhms
Vin	0.5V
Vpulse	0.5V
Capacitor load, CL	40pF
Resistor load, RL	700kOhm
Slope	5n
Delay	1n
Frequency	10MHz
Period	1/frequency
Duty cycle	Period/2
Resistors, R1 & R2 (Voltage Divider)	20M
Feedback resistor, Rf (P-controller)	200K Ohm
Input resistor, Rin (P-controller)	200K Ohm
Voltage reference, Vref (P-Controller)	1V
Width of transistor, W1 (Operational amplifier)	8u
Width of transistor, W2 (Operational amplifier)	16u
Length of transistor, L1 (Operational amplifier)	8u
Length of transistor, L2 (Operational amplifier)	8u

Table 11 presented a parameter and values for each component in the CMOS Charge Pump system. This system is excellent for self-powered devices because it is made to operate in a temperature-variable environment. The values for each row in the table correspond to a particular element or feature, and they provide insight into how the system behaves and functions in various scenarios.

The simulation started with the charge pump's fundamental parts and the transistor's width, which is 40 µm. This variable is crucial for the conductivity and overall performance of the transistor in the charge pump. The capacitor's role in amplifying voltage levels within the charge pump is also described, with the capacitor boost value being defined as 0.8 picofarads (pF). Effective energy transfer requires this improvement.

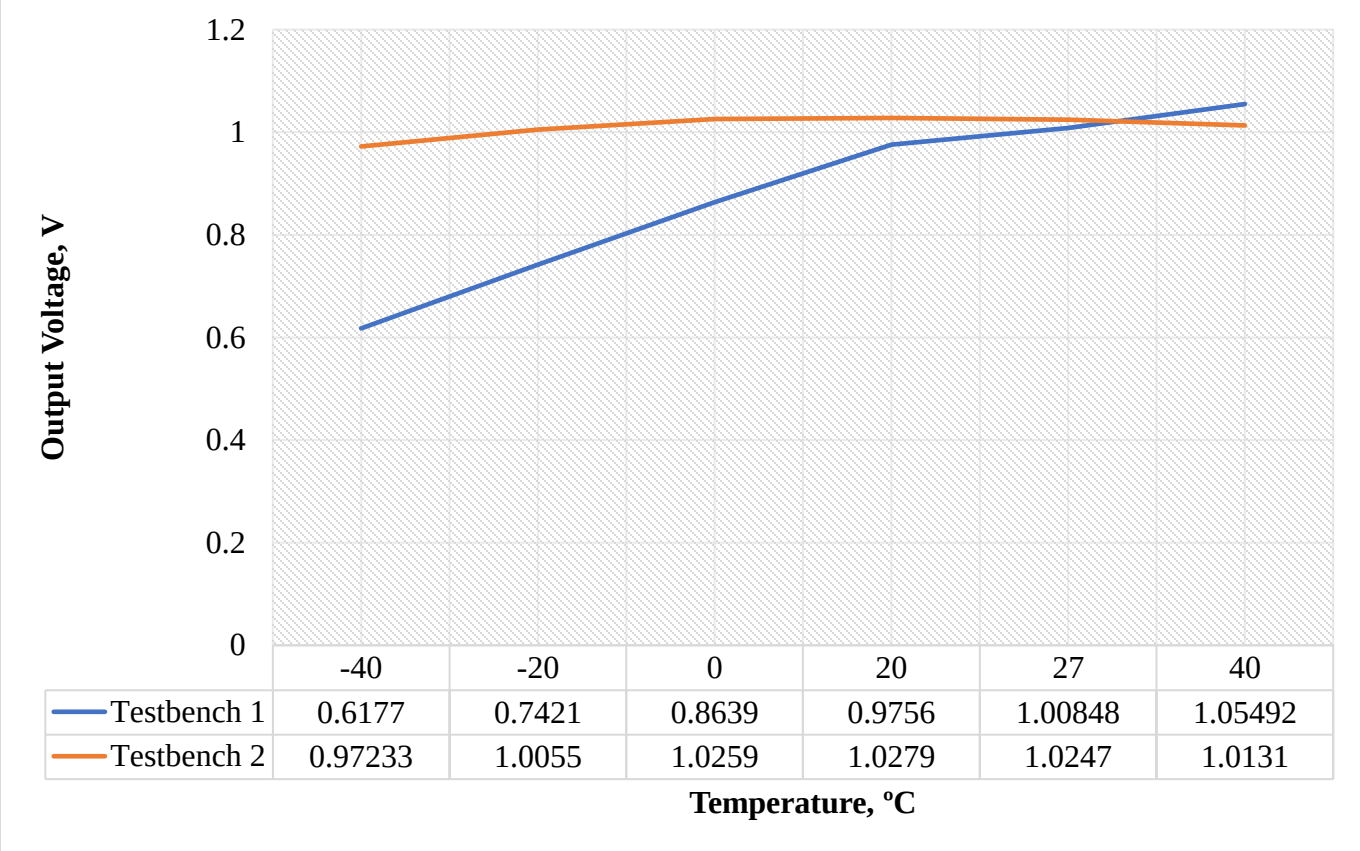
The capacitor load and resistor load, with values of 40 picofarads (pF) and 700 kilohms (k), respectively, are also highlighted in the table. These variables affect the system's load-carrying capability and impedance-management capabilities. They are crucial in determining the output and discharge properties of the system.

As the system's initial source of power, Vin, the input voltage, is determined to be 0.5 volts (V). A pulse or transient input specifically designed for the circuit's operation could be represented by Vpulse, which is stated at 0.5 volts (V). Then, the clock properties of the system are described. The delay is given as 1 nanosecond, denoting a time pause within the circuit, and the slope is given as 5 nanoseconds, showing the rate of change. These numbers reveal any inherent time lags as well as how quickly the system adapts to changes. The rate of oscillation within the circuit is indicated as 10 megahertz (MHz), which is an important factor in the behavior of periodic systems.

The proportional controller is discussed in the table as the circuit is running in a closed loop system to make it temperature insensitive. Values are assigned to the voltage reference, input resistor and feedback resistor illustrating their functions in system regulation. To modify the open-

loop gain, enhance steady-state accuracy, and quicken the system's responsiveness, proportional control is frequently used.

The table also explores the system's operational amplifiers. In the processing of signals, these amplifiers are crucial. The width and length of the transistors in the operational amplifier, precisely, are fixed at 8 µm and 16 µm for W1 and W2, respectively, and at 8 µm for L1 and L2, respectively. These variables affect transistor behavior in the Operational amplifier circuit, which affects how well the system functions.



	-40	-20	0	20	27	40
Testbench 1	0.6177	0.7421	0.8639	0.9756	1.00848	1.05492
Testbench 2	0.97233	1.0055	1.0259	1.0279	1.0247	1.0131

Figure 35: Graph voltage output vs temperature for Testbench 1 (Blue) and Testbench 2 (Orange)

The performance of a CMOS charge pump designed to cope with temperature variations is described in the accompanying Figure 35, which is in line with the goals of a self-powered device. The objective of this device is to maintain a constant state output voltage of 1V over a wide

temperature range. The study's goals include creating a reliable CMOS charge pump design that satisfies this demand and incorporates MOSFETs to allow voltage conversion from a lower input to a greater constant output voltage.

The information in the table compares the results of two test benches, designated as Testbench 1 and Testbench 2, to show how the charge pump behaves under various temperature settings. These test benches serve as experimental platforms for analyzing the charge pump's responsiveness to temperature changes.

The results recorded cover a temperature range of -40 to 40 degrees Celsius and illustrate the charge pump's responses at various temperatures. As temperatures rise, the results in the Testbench 1 column constantly trend upward, suggesting an increase in the output voltage. Meanwhile, the results in Testbench 2 were seen to reach an approximately of 1V despite a wide range of temperature.

The achievement of the first objective is demonstrated by the alignment with the intended output voltage despite temperature variations. The charge pump is well suited for self-powered devices operating in a variety of environmental situations since it can keep a consistent output voltage of about 1V despite severe temperature changes.

Additionally, the design's performance in obtaining a greater constant output voltage is improved using completely integrated MOSFETs to function as a DC-to-DC converter. The charge pump successfully proves its proficiency in voltage conversion, which is in line with the second goal, by smoothly ramping up the input voltage.

Table 12: Variation of Temperature and Corresponding Voltage Output

Temperature, ºC	Voltage Output, V
-40	0.97233
-35	0.98148
-30	0.990084
-27	0.99493
-25	0.99812
-20	1.0055
-15	1.0121
-10	1.01779
-5	1.0224
0	1.0259
5	1.02826
10	1.0294
15	1.02932
20	1.0279
25	1.0258
27 – default	1.0247
30	1.0228
35	1.0185
40	1.0131

The table illustrate that the simulated charge pump's performance characteristics under various thermal circumstances by providing insights into how it behaves over a range of temperatures. The charge pump's response to temperature changes and how steady its output is over this spectrum may both be evaluated using this simulation. Voltage Output (V) and Temperature (°C) are the two columns in the table. The voltage output that goes along with each row reflects the charge pump's response at the temperature that row corresponds to. This collection of information gives a thorough picture of the charge pump's operation in various heat conditions.

The table's temperature range, which includes both extreme cold and mild heat, ranges from -40°C to 40°C. The 5°C steps make it possible to evaluate the charge pump's efficiency over time in detail. The column "27 - default," which denotes the default temperature of 27°C, at which the simulation was run, provides one key which is voltage output is at 1.0247 volts. The output of the charge pump is stable at this set temperature, as evidenced that the charge pump's resistance to small temperature variations by showing that its voltage output is constant within a 5% range at 1.0247 volts.

It becomes clear that there are changes when the voltage output is examined at different temperatures. The range of these differences, however, shows that the charge pump can respond to temperature changes while still retaining a voltage output that is quite close to the intended level. The charge pump's efficient temperature compensation mechanisms are demonstrated by its capacity to adjust its output in response to temperature changes.

5.3 Comparison

Table 13: Comparison with previous researchers

Parameter	**This work**	**Li *et al*. (2019)**	**Shen, Bose, and Johnston (2017)**
Process	0.18um CMOS	0.18um CMOS	0.13um CMOS
Supply voltage	0.5V	5V	1.8V
Closed loop approach	Clock amplitude	Clock amplitude	Digital control
Temperature variation	-40ºC – 40 ºC	-40 ºC – 80 ºC	N/A

Three different study studies are compared in the table that is being given. Each parameter provides information about the methodologies, technological requirements, and experimental setups used in these studies. The research done by Li *et al*. (2019) and the current work both use a 0.18-m CMOS process in terms of the "Process" parameter. The study by Shen, Bose, and Johnston (2017), in contrast, makes use of a more refined 0.13m CMOS technology. Different levels of integration and performance capabilities are represented by this differentiation in process technology.

The "Supply Voltage" parameter highlights important variations between the works. With a focus on energy efficiency, "this work" functions at a noticeably low supply voltage of 0.5V. In contrast, Li *et al*. (2019) use a 5V supply voltage, which could potentially provide better performance but at the expense of increased power consumption. With a supply voltage of 1.8V, Shen, Bose, and Johnston (2017) strike a middle ground between power efficiency and performance.

The "Closed Loop Approach" highlights the strategies employed to regulate the systems. "This work" and Li *et al*. (2019) both adopt closed-loop approaches centered around clock amplitude control. However, Shen, Bose, and Johnston (2017) deviate by employing a closed-loop configuration driven by digital control, showcasing diversity in control methodologies.

The works also vary in temperature variation, an important factor in electronic gadgets. The term "this work" denotes a thorough assessment of a reasonable operating range, taking into account a temperature ranges from -40°C to 40°C. This range is widened by Li *et al*. (2019), who may be looking at more extreme conditions, to -40°C to 80°C. The breadth of Shen, Bose, and Johnston's (2017) temperature testing is not stated because the temperature variation data for their study is not provided.

CONCLUSION

This research effectively addresses the challenge of maintaining a steady state output voltage of 1V over a wide temperature range by using a novel CMOS charge pump topology. Using cutting-edge temperature adjustment techniques by adding a close loop regulation circuit, the charge pump displayed outstanding stability and tolerance to temperature changes. This achievement is especially helpful for self-powered devices since it ensures consistent and reliable performance independent of changing environmental conditions.

A successful design and integration of a fully integrated MOSFET-based DC-to-DC converter within the CMOS charge pump mechanism was another noteworthy breakthrough. By integrating MOSFETs as efficient switching components, the charge pump was able to accomplish its fundamental goal of boosting low input voltages to a higher and more steady output voltage. This innovative technique has significant potential for applications requiring stable power supply levels, even when input voltages change.

A thorough analysis of the CMOS charge pump's performance using demanding testbench and in-depth simulations designed for self-powered applications produced favourable results. This successful simulation shows that the proposed CMOS charge pump design is feasible and implementable in real-world scenarios involving self-powered devices.

In summary, this study introduces a CMOS charge pump topology that successfully sustains a constant 1V output voltage over a broad temperature range. Self-powered devices benefit from improved stability and resistance to temperature variations because to the inclusion of a closed-loop control circuit. Additionally, the effective boosting of low input voltages to more stable outputs is demonstrated by the successful integration of a MOSFET-based DC-to-DC converter within the charge pump mechanism.

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