INVESTIGATION OF A 3NM STRAINED FIN FIELD-EFFECT TRANSISTOR (FINFET)

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ABSTRACT

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Fin Field-Effect Transistor (FinFET) device is qualified for its low-power operation capability at which the performance can be improved with further scaling. However, critical scaling towards 10nm of FinFET leads to a series of issues such as drain-induced barrier lowering (DIBL), threshold voltage roll-off, hot carrier effects, reverse leakage current rise which affecting the functionality of the device. Shrinking of MOSFET transistor size is no longer sufficient to boost integrated circuit performance for higher generation of technology. To address this issue, the design of 3nm strained FinFET using strained SiGe wafer is proposed. In this project. 3nm FinFET is implemented using GMSH software and 3D-DDCC software. Simulation is performed using 3D-DDCC simulator to investigate the respective performance as compared with conventional Si FinFET. Both designs conform with the standard characteristics of an operational FinFET. By analysing both the output and transfer characteristic of both FinFET design, the drive current of strained FinFET is proven to be higher than

conventional FinFET which indicating higher performance. Besides, the current leakage of SiGe FinFET is identified to be higher than Si FinFET by 17.19% due to enhanced electron mobility. Even so, the leakage current is found to be low in 0.075 μA which causes negligible effect in power consumption and temperature dissipation. Further study can be done to investigate the possibility of leakage current reduction using triangular shaped FinFET, GAAFET structure and high-k dielectric material for the benefit of variety of people.

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APPROVAL SHEET

This thesis/dissertation entitled "INVESTIGATION OF 3NM STRAINED FIN FIELD-EFFECT TRANSISTOR (FINFET)" was prepared by TAN PEI XIN and submitted as partial fulfilment of the requirements for the degree of Master of Engineering (Electronic Engineering) at Universiti Tunku Abdul Rahman.

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SUBMISSION OF THESIS/ DISSERTATION

It is hereby certified that TAN PEI XIN (21AGM06713) has completed this thesis entitled "Investigation of 3nm Strained Fin Field-Effect Transistor (FinFET)" under the supervision of Dr Yeap Kim Ho from the Department of Engineering, Faculty of Engineering and Green Technology.

I understand that the University will upload softcopy of my thesis in pdf format into UTAR Institutional Repository, which may be made accessible to UTAR community and public.

Yours truly,

____

Tan Pei Xin

DECLARATION

I TAN PEI XIN hereby declare that the thesis/dissertation is based on my original work except for quotations and citations which have been duly acknowledged. I also declare that it has not been previously or concurrently submitted for any other degree at UTAR or other institutions.

Tan Pei Xin

Date: 18 August 2023

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LIST OF ABBREVIATION

3D-DDCC	Three-dimensional Drift-diffusion Charge Control
AMD	Advanced Micro Devices
BJT	Bipolar Junction Transistor
DIBL	Drain-Induced Barrier Lowering
FET	Field-Effect Transistor
FinFET	Fin Field-Effect Transistor
Ge	Germanium
GMSH	Graphic Mesh
Intel	Integrated Electronics
IBM	International Business Machines
I-V	Current-Voltage
MIT	Massachusetts Institute of Technology
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NMOS	N-channel Metal-Oxide-Semiconductor
PMOS	P-channel Metal-Oxide-Semiconductor
Si	Silicon
USA	United States of America

CHAPTER 1

INTRODUCTION

1.1 Background of Study

The world is in the midst of forth industrial revolution, Industry 4.0 which Internet of things (IoT) is gradually adopted in robotics and machines that revolutionize the engineering field. IoT enables the connection of human with the object to improve lifestyles through real-time data collection and processing using the device that have been augmented with intelligence. In that sense, IoE devices require fast decision making capability, low heat dissipation and close proximity to the human body (Ghoneim et al., 2016). Hence, this gives rise to the demands of high performance, flexibility and low power consumption devices. Moreover, ultra-low power (ULP) digital integrated circuit (DIC) applications are ceaselessly in need for high speed and multi-threshold voltage devices (Dubey & Kondekar, 2016). In this context, FinFET device is qualified for low-power operation. Further scaling can also be done through it nonplanar 3D architecture, to cope with Moore's law (Medina-Bailon et al., 2018).

However, mobility degradation occurs due to the effect of the larger vertical electric field, has becomes one of the main obstacles in nano scale transistors. Reduced MOS transistor size is no longer adequate to boost integrated circuit performance for higher generation of technology. The scaling challenges of recent MOSFET

technologies necessitate the use of new materials and technological advancements. Among them, strain technique is one of the promising techniques for FinFETs with different high k/metal gates and piezo materials.

In the middle of the 1980s, it was initially shown that transistors fabricated with strained silicon had higher switching speeds due to improved electron mobility and velocity. Although the effects of strain were not fully investigated, the strain was once again revitalized in the early 1990s at Massachusetts Institute of Technology (MIT), USA on biaxial and process-induced strain. In 1992, the first strained n-channel Silicon MOSFET created was proven to exhibit a 70% higher effective mobility than conventional MOSFET. Strain silicon technology for MOS transistor started to be commercially adopted in 90 nm technology node by major semiconductor companies like Integrated Electronics (Intel), Advanced Micro Devices (AMD) and International Business Machines (IBM) (Roy & Singh, 2010).

There are lots of studies been done by previous researches on strained technology for FinFET which including three-layer SiGe strain relaxed buffer (Zhao et al., 2019), 7nm FinFET with Extreme Ultraviolet Lithography (EUV) and Dual Strained High Mobility Channels (Xie et al., 2017), strained silicon on two-stage operational transconductance amplifiers (Ribeiro et al., 2022) and so on. However, the research on strained FinFET beyond 5nm technology nodes is still limited. Thus, it is interesting to investigate the advantages of 3nm Strained FinFET as compared with conventional FinFET in this project.

1.2 Problem Statements

Since the introduction of planar CMOS technology at the 20nm, multi-gate fully depleted device topologies have been developed to continue device scaling in order to achieve higher performance at lower supply voltages for 14nm (Nanda & Dhar, 2021) ,10nm (Medina-Bailon et al., 2018), 7nm (Xie et al., 2017) (Dash et al., 2018) and 5nm nodes (Moroz et al., 2016) based on strained engineering. However, transistor is prone to short-channel effects (SCEs) when the dimensions decrease(Jena et al., 2020). SCEs happen when the channel length is equivalent to the source and drain junction's depletion-layer widths. The closer distance between the drain and the source diminishes ability of the gate electrode to control the flow of current in the channel region. This leads to a series of issues such as velocity saturation, polysilicon gate depletion effect, mobility reduction, drain-induced barrier lowering (DIBL), threshold voltage roll-off, hot carrier effects, reverse leakage current rise, etc.

Besides, critical dimensions have been scaled aggressively that four or more masks are required for an optical solution to define a single critical layer, which is cost concern and may resulted in significant defectivity. There are other challenges related to lithography which including mask alignment, tolerances associated with double patterning as well as performance and reliability concerns associated with aging. These issues continued to worsen with every scaling step. Nevertheless, the various effects described significantly downgrade the performance of transistor at process. Dimension scaling is not a solution in the future anymore which gives rise to the introduction of strain technology to increase the performance of FinFET at 3nm scale.

1.3 Aim and Objectives

The objectives of the research are as follows:

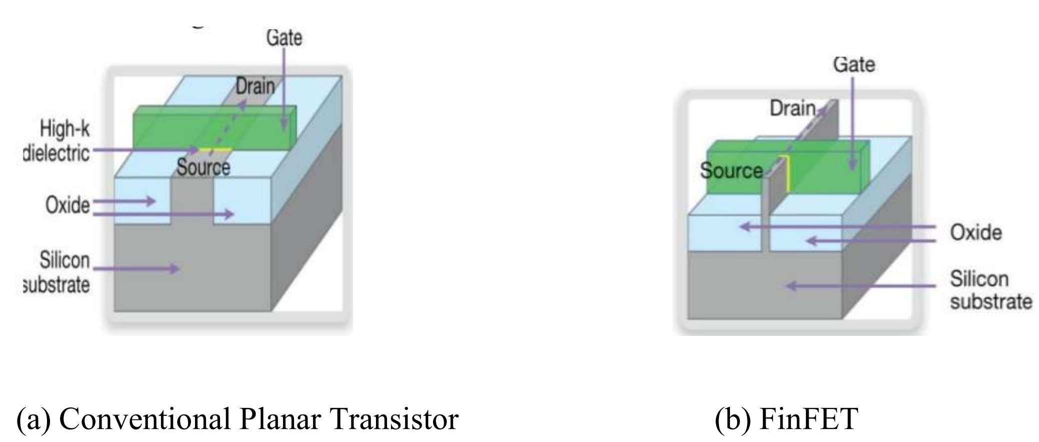
1. To develop a 3nm Strained FinFET using GMSH software.
2. To simulate the current-voltage characteristic curve (I-V curve) of 3nm Strained FinFET using 3D-DDCC software.
3. To analyze the performance of 3nm Strained FinFET as compared with conventional FinFET.

CHAPTER 2

LITERATURE REVIEW

2.1 FinFET

FinFET, which is also called as a Fin Field-Effect Transistor is a multi-gate device, MOSFET invented by Professor Hu Zhenming of University California, Berkeley. The invention allows transistors to be scaled down to the nanoscale region. FinFET is constructed on a silicon substrate by placing the gate on multiple sides of the channel (fin), which makes it differs from planar transistor as displayed in Figure 2.1.



(a) Conventional Planar Transistor (b) FinFET

Figure 2.1: Structure of conventional planar transistors and FinFET (Pavan Kumar & Lakshmi Chetana, 2019)

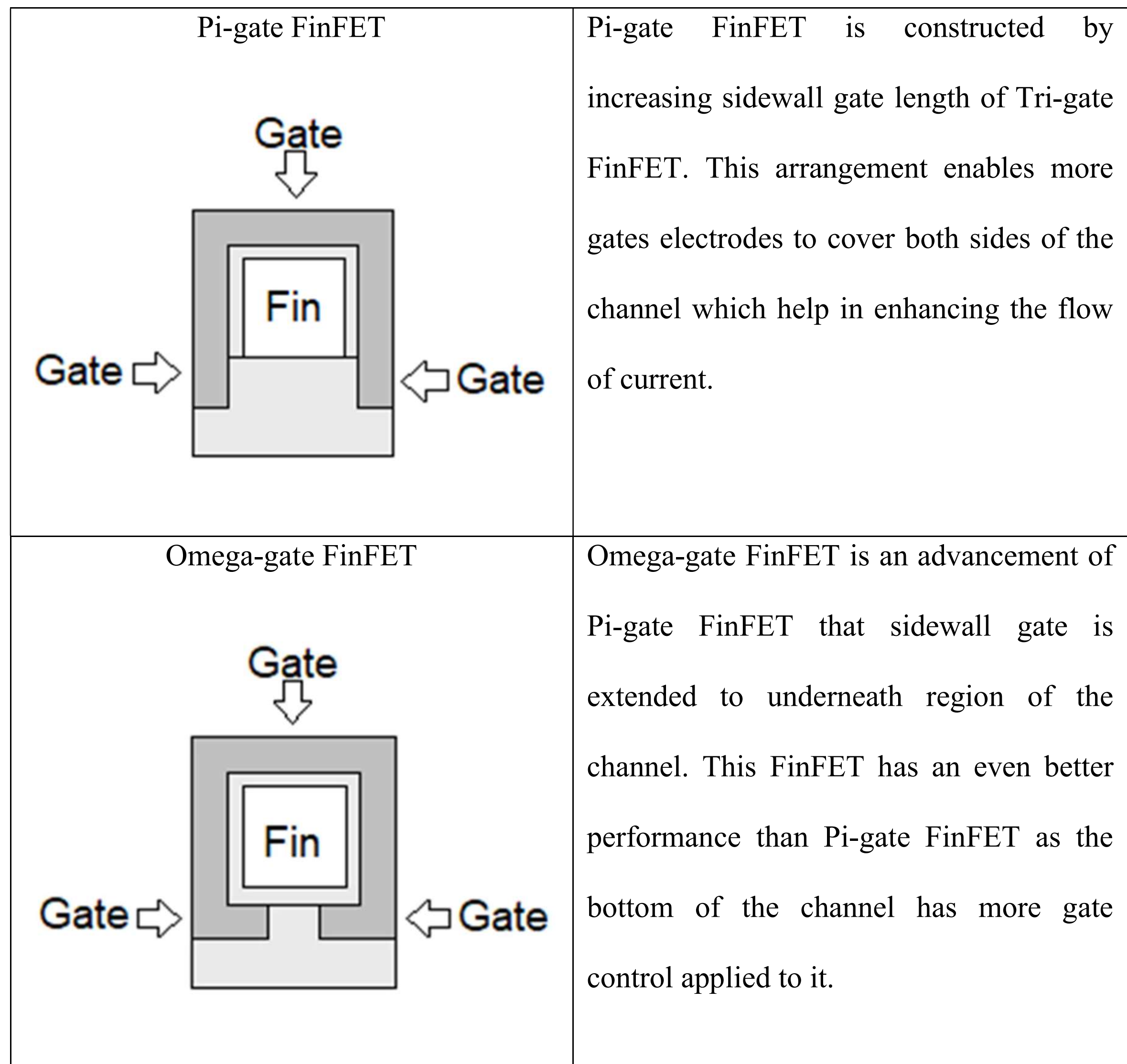
The gate structure that wraps around the channel provides a fully depleted operation for chips to operate at lower power consumption. It is called as FinFET due to its source/drain region are put on the silicon surface, which looks like the back fin of a fish. The 3-D fin-shaped structure helps improving the gate's control over the channel by increasing the area of the gate surrounding the channel. In addition, drive current and current leakage can be enhanced significantly due to the presence of gate electrodes on each side of the fin. This greatly shorten the gate length of the transistor and making channel doping optional. As a result, the effect of dopant-induced variation can be diminished. Low channel doping also allows better mobility of the carriers inside the channel. This enables FinFET to operate in lower threshold voltage. Hence, better performance and low power dissipation FET can be obtained through the fin structure.

The advent of the 3D transistor technology has introduced a various type of FinFET transistor such as Double-gate FinFET, Tri-gate FinFET, Pi-gate FinFET and Omega-gate FinFET as shown in Table 2.1. Each type of the transistor is named according to the way the gate electrode wraps around the channel regions of the transistor. Among them, tri-gate FinFET is proven to have better performance than Double-gate FinFET due to the presence of third gate that inhibit the electric field. This provides a better gate control on the current flow along the channel region which solves the problem of the current leakage effectively. At the same times, the power consumption of the device will be lowered down which is beneficial for low power device. Both Pi-gate and Omega-gate FinFET structure has better current flow control capability than tri-gate FinFET with increased complexity of fabrication process.

Therefore, tri-gate FinFET is chosen to be investigated as the intent of the project is to analyze effect of strain technology on 3nm FinFET.

Table 2.1: Types of FinFET Configurations

Types of Configurations	**Description**
Double-gate FinFET (DG-FinFET) Gate Hard mask Drain Source	Double-gate FinFET or DG-FinFET has a hard mask on top of the silicon 'fin', which is a dielectric layer that impede the electric field. This structure helps improving the performance by preventing the formation of the parasitic inversion layer. The gate electrodes are exerted on the channel from both sides of the fin to control the flow of the current.
Tri-gate FinFET Gate Gate Fin Gate	Differ from DG-FinFET, the gate electrodes of Tri-gate FinFET are exerted on three sides of the fin which are top and sides of the channel region. The third gate provides a better gate control on the current flow along the channel region which resolves current leakage problem of DG-FinFET.



Pi-gate FinFET	Pi-gate FinFET is constructed by increasing sidewall gate length of Tri-gate FinFET. This arrangement enables more gates electrodes to cover both sides of the channel which help in enhancing the flow of current.
Omega-gate FinFET	Omega-gate FinFET is an advancement of Pi-gate FinFET that sidewall gate is extended to underneath region of the channel. This FinFET has an even better performance than Pi-gate FinFET as the bottom of the channel has more gate control applied to it.

2.2 Strained FinFET

Strain engineering refers to the mechanically stretching or compressing material for the purpose of improving its properties (Tsutsui et al., 2019). It has been used in FinFET to enhance the carriers transport through the changes of band structure and mobility enhancement. Strained silicon is obtained when silicon layer is placed over

silicon–germanium (SiGe) substrate. Silicon atoms are stretched beyond their normal interatomic distance which decreases the atomic forces that obstruct electrons' ability to travel freely across transistors. These electrons can move 70% faster allowing strained silicon transistors to switch 35% faster (Ribeiro). Epitaxial growth of stained Si is an important part of FET channel and source-drain formation. Hence, the heart of strain engineering technology will be the ability to control the structural quality to create epitaxial layers that free of defects. This is crucial to prevent issues such as device reliability degradation, strain relaxation and anomalous dopant redistribution. (Hashemi et al., 2015).

An example of strained silicon used in FinFET is SiGe. In order to create compressive strain in the silicon channel, SiGe mixture comprises of 20% germanium and 80% silicon is used. A layer of SiGe is initially grown during epitaxial growth by introducing a few Ge atoms into wafer's crystalline surface. In the view of fact that Ge has a larger lattice constant (5.65 Å) than Si (5.4Å), larger crystal structure is grown as shown in Figure 2.2.

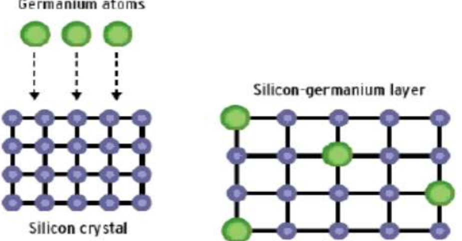


Figure 2.2: Strained SiGe structure

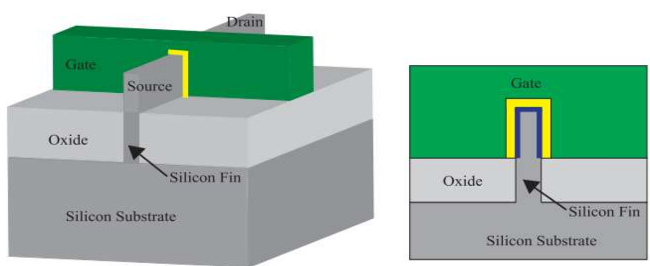
2.3 Working Principle of FinFET

FinFET is a four terminals device with drain (D), source(S), gate (G) and body (B) terminals as shown in Figure 2.3. It shares similar functions as MOSFET where the conductivity of the device is determined by input voltage. This makes it better as compared with bipolar junction transistor (BJT) since no input current is required to control the load current. There are two types of FinFET which are NMOS for negative channel and PMOS for positive channel.

For a negatively doped drain and source (i.e., a NMOS transistor), when a positive potential is applied onto the gate, it repels the positive charges (holes) of the P-substrate and the negative carriers are attracted from the substrate to form a channel inversion between the source and drain terminals underneath the insulator material. To operate this device, a potential must be applied to the gate and drain terminals. The potential applied onto the gate terminal, V_G must be larger than the threshold voltage, V_{TH}. If $V_G < V_{TH}$, no channel will be formed between the source and drain terminals and no current can flow from the source to the drain terminal. The device is said to be in the 'OFF' state. Besides, for a constant gate potential, the potential difference between the gate and insulator interface decreases when approaching to the drain terminal as the drain voltage applied is higher than the source voltage. A phenomenon known as 'Pinched off' may occurred when $V_G – V_D \leq V_{TH}$. As a result of pinch-off, the channel stops before it is connected to the drain. However, the transistor still conducts because the electrons are attracted to the drain terminal by the depletion region. For positively doped drain and source terminals (i.e. a PMOS transistor), the operating principle shared

similar concept except for negatively gate potential is applied. The negative charges (electrons) of the P-substrate are repelled and positive carriers (holes) are attracted to form the inversion channel connecting the drain and source terminals.

FinFET functions differently with operating region. In cut off region, there is no current flows through it and the device is in OFF state. In contrary, constant currents flow from drain to source without considering the enhancement in the voltage, enable the device to turn on. Hence, FinFET can functions as a switch in these two operating regions. Besides, it can be used as an amplifier in linear/ohmic region. With the increment in the voltage across the drain to source path, current across the drain to source terminal is improved which perform amplifier functionality. An ideal transistor allows the current flows as much as possible when it is in the 'ON' state and almost zero current flows in its 'OFF' state. Switching between the 'ON' and 'OFF' state must be as fast as possible in order to improve the performance of the device.



(a) 3D structure (b) Cross-sectional view

Figure 2.3: 3D structure and Cross-sectional view of FinFET(Yanambaka et al., 2017)

2.3 Comparison of Strained FinFET and conventional FinFET

The comparison of Strained FinFET and conventional FinFET is tabulated in Table 2.2. As the fin height can be increased in order to increase the transistor density on the wafer, it becomes possible for the technology to shrink towards 3 nm. When a thin layer of silicon is being stretched, electrons drop to a lower energy level, so that it can achieve a comparable level of conductance at lower power. This results in higher transconductance as compared to conventional FinFET. When Ge is added into Si to form SiGe, electron mobility is also enhanced which leads to more current can flow along the channel with the same value of input voltage applied. As a result, strained FinFET is able to operate at a lower voltage. The operation speed of strained FinFET is also faster than conventional FinFET transistor due to its greater switching speed between ON/OFF state. The dynamic power consumption is much lower as the parasitic capacitance is lower.

Table 2.2: Comparison of Strained FinFET and Conventional FinFET

Parameters	Strained FinFET	Conventional FinFET
Features sizes	Smaller	Larger
Operation speed	Faster	Slower
Dynamic power consumption	Lower	Higher
Rate of current flows	Higher	Lower
Trans-conductance	Higher	Lower
Operating voltage	Lower	Higher

2.4 Fabrication of tri-gate FinFET device

Both conventional FinFET and strained FinFET share similar device fabrication steps in manufacturing transistor devices, except for the material used in source and drain. Silicon On Insulator (SOI) fabrication technology is used in for Tri-gate FinFET in this project to improve the performance through the reduction of parasitic capacitance of FinFET. This can be achieved when an insulator layer is placed in between silicon substrate as shown in Figure 2.4.

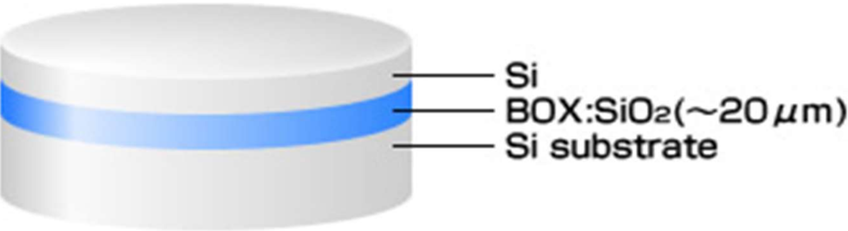


Figure 2.4: Structure of SOI wafer

The first step in FinFET fabrication process is wafer preparation. For conventional FinFET, Si wafer is being used while strained FinFET is using SiGe wafer. Different wafer cleaning process is necessary to remove particles and contaminations on the surface such as photoresist remains, debris and so on. Next, heating process is done to remove moisture absorbed on wafer surface to prepare for clean and dry surface essential for the adhesion of photo resist.

Then, a positive photoresist layer is coated onto the surface of the Si wafer and a hard mask is covered on top of the desired area of the photoresist to prevent it from UV

exposure. There are two types of photoresists which are positive and negative photoresists. A negative photoresist is initially soluble and sensitive to sunlight. After being exposed to UV light, the area coated with photoresist become insoluble and harden. On the contrary, a positive photoresist has the characteristics opposite to the negative photoresist (Nader Shehata et al., 2015). In the fabrication process of the transistor, positive photoresist are more popularly used compared to the negative photoresist due to its higher photolithographic resolution.

After the UV exposure to positive photoresist, the exposed photoresist area becomes soluble and easily removed by the etching process using chemical solvent. Then, the surface of SOI-layer that is not covered by the photoresist is removed by the etching process with the use of another chemical. A layer of gate oxide is deposited on top of the fin via thermal oxidation to isolate the gate electrode from the channel (Philipp, 2017). Besides that, a poly-silicon gate electrode is deposited on top of the 'fin' forming the gate that wraps around the channel. Application of photoresist, UV light exposure and etching process are repeated until desired tri-gate FINFET structure is obtained. Finally, the fabrication process ends with the doping of the source and drain regions.

CHAPTER 3

METHODOLOGY

3.1 Project Implementation Flow

The implementation flow of the project is shown in Figure 3.1. Research and literature review are done for 3n Strained FinFET. The structure and working principle of strained FinFET is studied and fully understand to get a general concept prior to implementing. Next, research is done for GMSH and 3D DDCC software as well to be acquainted with the software's interface and features that going to be used in the project. After that, the implementation process begins by developing 3nm FinFET using GMSH software. Then, mesh file generated is loaded to 3D-DDCC software to determine if the structure achieves 3nm specification. Else, the FinFET structure is altered until getting expected output. After that, parameters used for both Si FinFET and Strained (SiGe) FinFET are determined and configured in the setting for simulation purpose. If simulation process is failing, parameter setting need to be revisit until desired output is obtained. After simulation is completed, output I-V curve of 3nm FinFET and Strained FinFET are generated. The output I-V curves are observed and analyzed to study the benefits of strained FinFET as compared with conventional FinFET which is the main concern of the research.

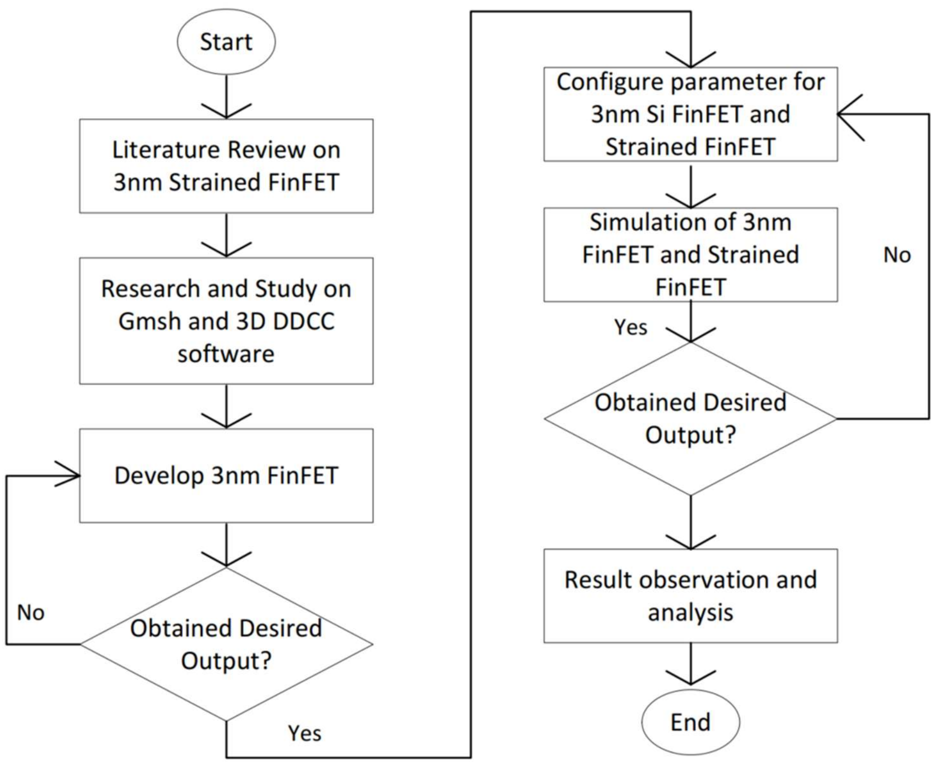


Figure 3.1: Project Implementation Flow

3.2 FinFET implementation Flow

3.2.1 GMSH software

3nm FinFET in this project is constructed by using GMSH software, which is an 3D finite element mesh generator built-in with CAD engine and post-processing facilities. It is developed by Jean-Francois Remacle and Christophe Geuzaine in 2003 with the aim of providing a fast, light and user-friendly meshing tool with parametric

input and advanced visualization capabilities. GMSH comes with 4 modules for geometry description, meshing, solving and post-processing. It enables geometry to be described interactively with the use of the graphical user interface (GUI), or in ASCII text files using a built-in scripting language or Gmsh Application Programming Interface (API). ASCII text file makes it possible to model repetitive structures and automate all treatments using user-defined macros, conditionals commands, loops, loops etc. For more complex geometry that cannot be achieved using built-in scripting language, users are free to choose from Python, C++, C or Julia API with the downside of having an extra interpreter to compile the code. The interface of the GMSH software is shown in Figure 3.2 below. In this project, scripting language is chosen to construct 3nm Strained FinFET due to its ability to assign the size more accurately.

3

Figure 3.2: Interface of GMSH Software

3.2.2 Design Rule of FinFET model

There is design rule of FinFET design that need to be followed during FinFET construction in order to obtain FinFET design with expected functionality. FinFET design proposed in this project is made up of Fin (drain, source, and channel), gate, oxide layer and substrates layers. It is crucial to configure the ratio of fin width, W_{FIN} and the channel length, L_g to be lower than (1:2) (Wu, 2010) as shown in Table 3.1. By doing so, the short channel effect is well suppressed and the subs-threshold swing is basically the theoretical best case.

Table 3.1: Design Rule of the FinFET Structure

Regions	Ratio
Channel length	$L_g = \alpha\ nm$
Fin Width	$W_{FIN} = \frac{\alpha}{2}\ nm$

3.2.3 Construction of 3nm Strained FinFET

FinFET structure construction is started by setting the location of the points along X-axis, Y-axis and Z-axis. Then, those points are joined together to form the surface as shown in Figure 3.3 Each surface needs to be allocated correctly to generate desired FinFET structure. After that, 3-D structure is constructed by assigning volumes

to the structure with no overlapping to ensure successful simulation. Figure 3.4 and 3.5 illustrate the 3nm FinFET structure after surface and volume assigned to it.

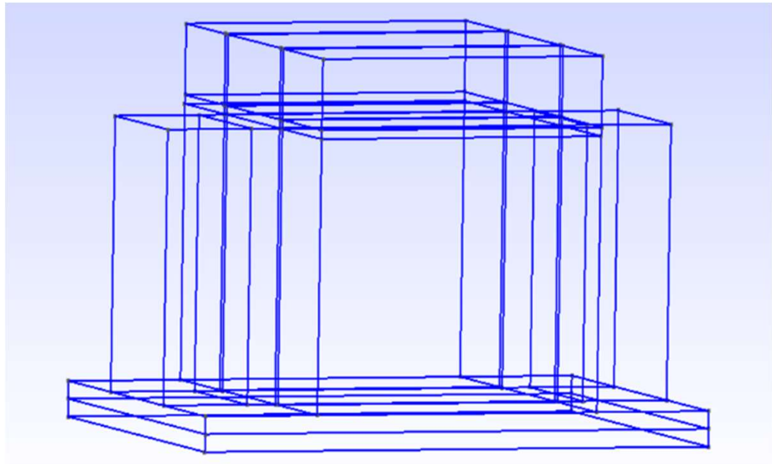


Figure 3.3: 3nm FinFET structure with Points and Lines assigned

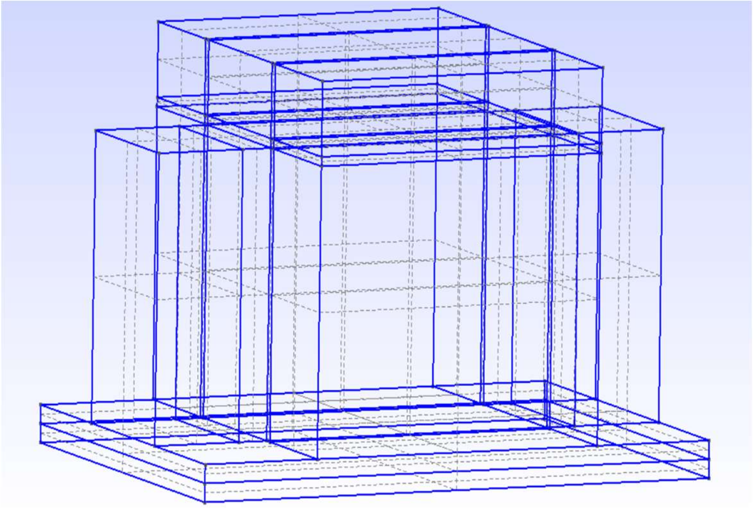


Figure 3.4: 3nm FinFET structure with Surface assigned

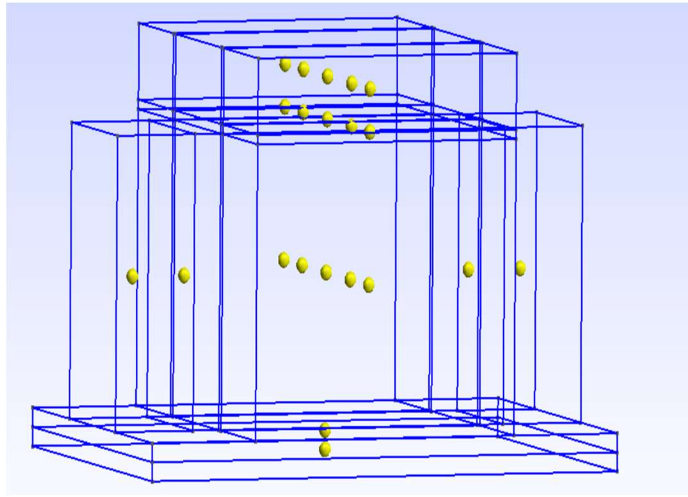


Figure 3.5: 3nm FinFET structure with Volumn assigned

3.2.4 Meshing Module

Meshing process is done by using mesh module of GMSH software to mesh the structure in 2D and 3D structure. Prior to the process, the lines and surfaces of gate region, channel region and oxide layer region have to be correctly assigned to transfinite algorithm. Else, undesired output will be obtained. The structure constructed is successfully meshed into 2D and 3D as shown in Figure 3.6. As the last step of the FinFET structure construction, the basic model FinFET construction is saved as geo.file format by default. Since 3D-DDCC software only able to read the file in .msh format, 3D model constructed in GMSH is required to save in .msh format.

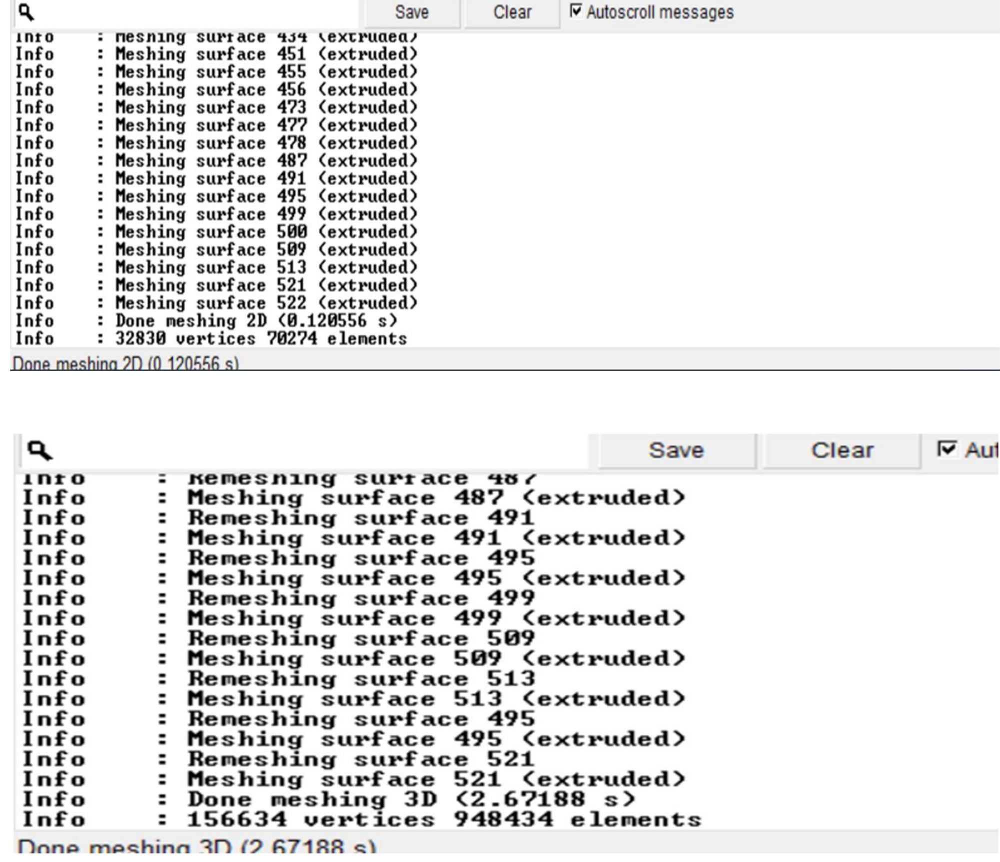


Figure 3.6: Successful meshing of 2D and 3D structure

3.3 FinFET Simulation Flow

3.3.1 3D-DDCC software

Three-dimensional Drift-diffusion Charge Control solver or 3D-DDCC is a 3D finite element-based Poisson and drift-diffusion solver developed by Dr. Yuh-Renn Wu. This solver is able to solve various problems which including Gaussian shape tail state models, thermal and light extraction. trap problem, and field dependent mobility.

Besides, 3D localization landscape model introduced into the program recently enable it to compute the effective quantum potential very effectively. In this project, 3D-DDCC software is used to perform the simulation of the FINFET structure constructed. Figure 3.7 below shows the display of 3D-DDCC software. There are several important steps must be known in using the 3D-DDCC software such as mesh setting, material range setting, basic parameters setting and panel setting which will be discussed in later section.

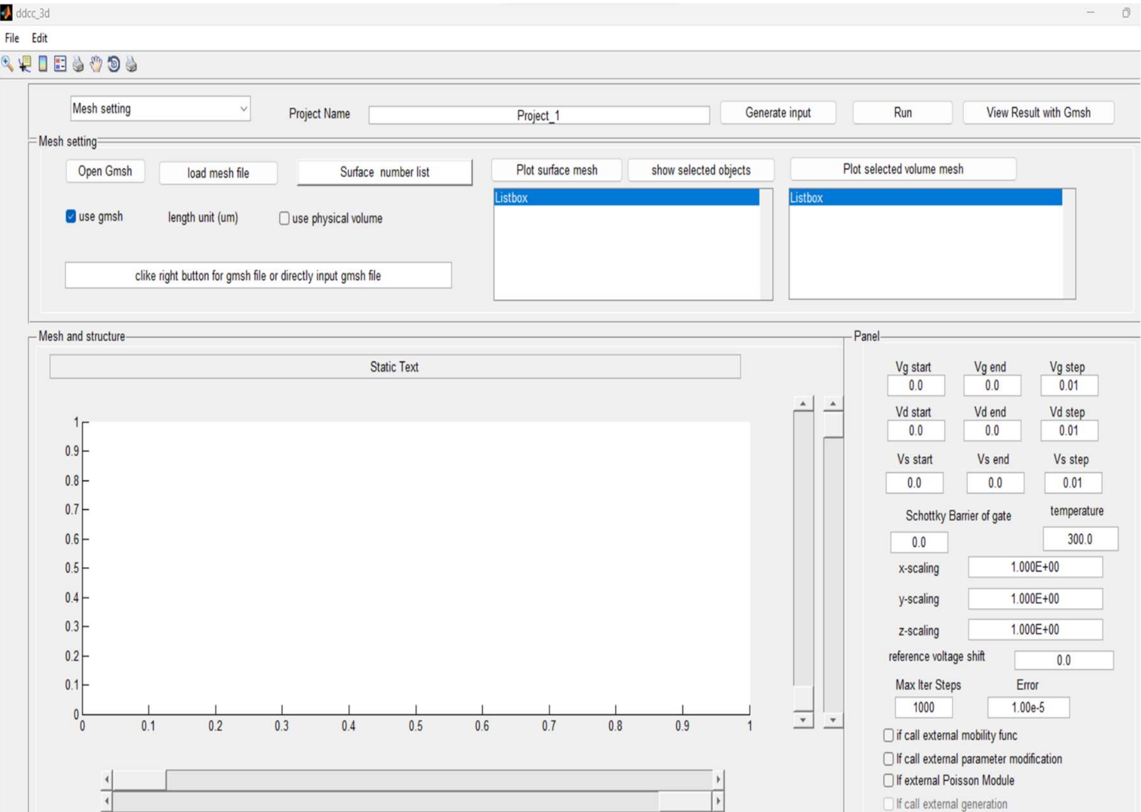


Figure 3.7: Interface of 3D DDCC software

3.3.2 Mesh Setting

Figure 3.8 illustrates the mesh format file generated in gmsh software is read in 3D-DDCC software. Physical volume option is checked to simplify the number of the surface and volume used for the convenience of reading.

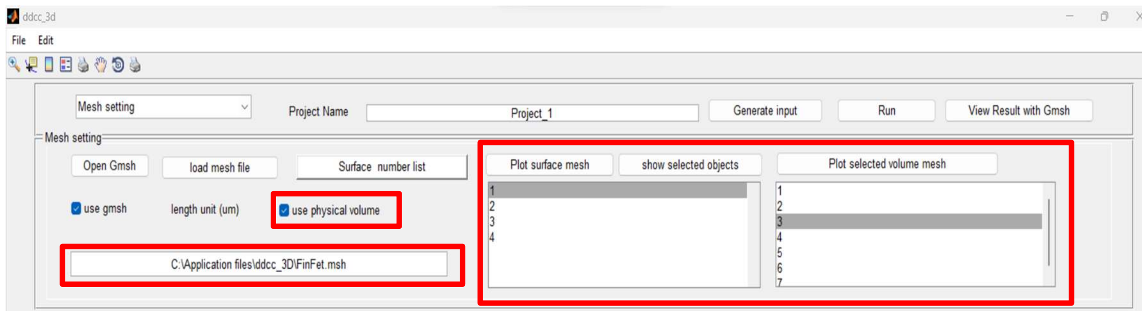


Figure 3.8: Mesh Setting

3.3.3 Material Range Setting

Material range setting are set as shown in Figure 3.9. GMSH range is set to 7 to indicate the number of volumes constructed for the FinFET structure for Source, Drain, Channel, Gate, Oxide Layer, Oxide Film and Substrate Layer. Each of the volume number is automatically assigned to their respective region number following the structure in the GMSH software. Next, GMSH boundary is configured to be 3 to represent the number of surfaces that will be used for the simulation process. At the same time, surface numbers are assigned manually to their respective surface contact defined as drain, source and drain. This step is important as drain, source or gate is determined by the surface contact instead of their volume region.

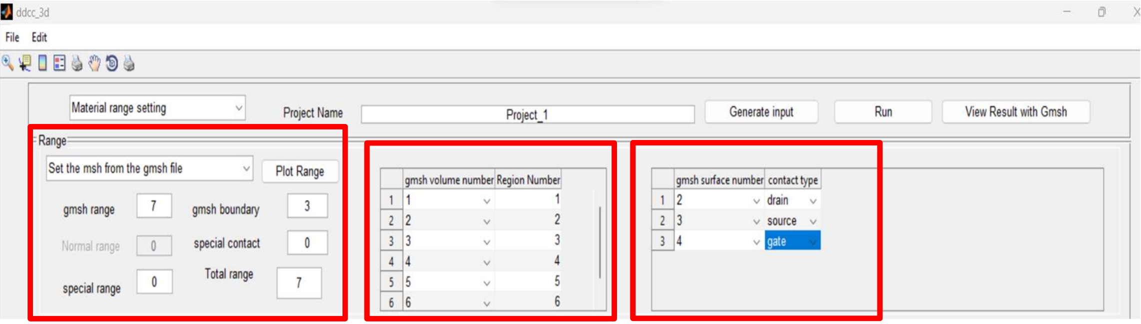


Figure 3.9: Material Range Setting

3.3.4 Basic Parameter

After the material range setting is done, parameters of the FINFET structure are assigned as shown in Figure 3.2. The number of regions in the FINFET structure are determined according to the number of volumes clarified in the previous step. Then, the materials used in each of the volume of the FINFET structure are decided and their respective activation energy value, dopant density and also the substrate layer are determined. Both volumes for source and drain must be heavily doped for the contact purpose. After that, other parameters can be generated automatically by clicking on the 'generate parameters' button as displayed in Figure 3.10. This function will auto assign the other parameters value such as band gap energy, electron mobility and etc.

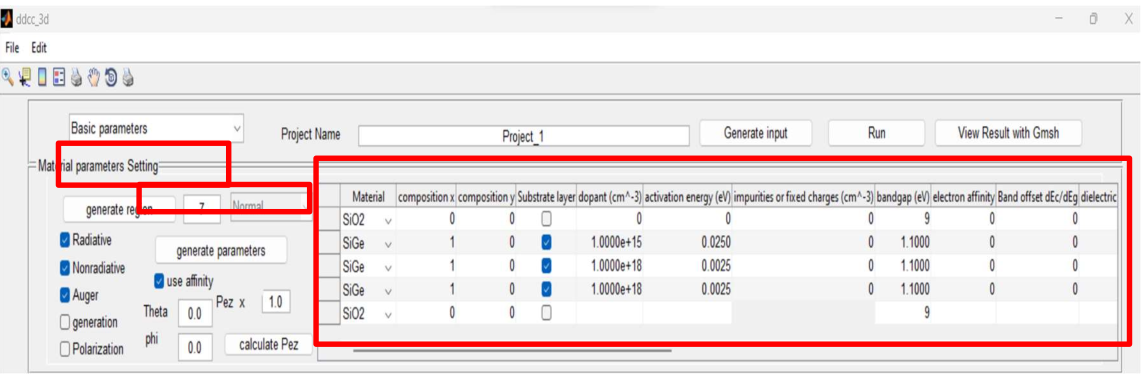


Figure 3.10: Basic Parameter Setting

Table 3.1: Parameter of 3nm FinFET constrained

Surface	Parameter	
	Si	SiGe
Drain	Material: Silicon Dopant density: $1.0 \times 10^{18}\ cm^{-3}$ Activation energy: 0.025 eV Length: 1 nm Thickness: 3 nm	Material: Silicon Germanium Dopant density: $1.0 \times 10^{18}\ cm^{-3}$ Activation energy: 0.050 eV Length: 1 nm Thickness: 3 nm
Source	Material: Silicon Dopant density: $1.0 \times 10^{18}\ cm^{-3}$ Activation energy: 0.025 eV Length: 1 nm Thickness: 3 nm	Material: Silicon Germanium Dopant density: $1.0 \times 10^{18}\ cm^{-3}$ Activation energy: 0.050 eV Length: 1 nm Thickness: 3 nm

Substrate	Material: Silicon Dopant density: 1.0 × 10^{15} cm^{-3} Activation energy: 0.025 eV Length: 6 nm Thickness: 1 nm	Material: Silicon Dopant density: 1.0 × 10^{15} cm^{-3} Activation energy: 0.025 eV Length: 6 nm Thickness: 1 nm
Gate	Material: Silicon Dioxide Dopant density: 0 cm^{-3} Activation energy: 0 eV Gate length: 3 nm	Material: Silicon Dioxide Dopant density: 0 cm^{-3} Activation energy: 0 eV Gate length: 3 nm
Channel	Material: Silicon Dopant density: 1.0 × 10^{18} cm^{-3} Activation energy: 0.025 eV Length:4 nm Thickness: 1 nm	Material: Silicon Germanium Dopant density: 1.0 × 10^{18} cm^{-3} Activation energy: 0.050 eV Length: 4 nm Thickness: 1 nm

3.3.5 Panel

Prior to simulation run, start, end and step voltages need to be configured appropriately. Similar goes to the values of the Schottky barrier, temperature and xyz-scaling as shown in Figure 3.11. Lastly, the project is saved and simulation run is initiated. Simulation run result can be observed in Figure 3.12 below.

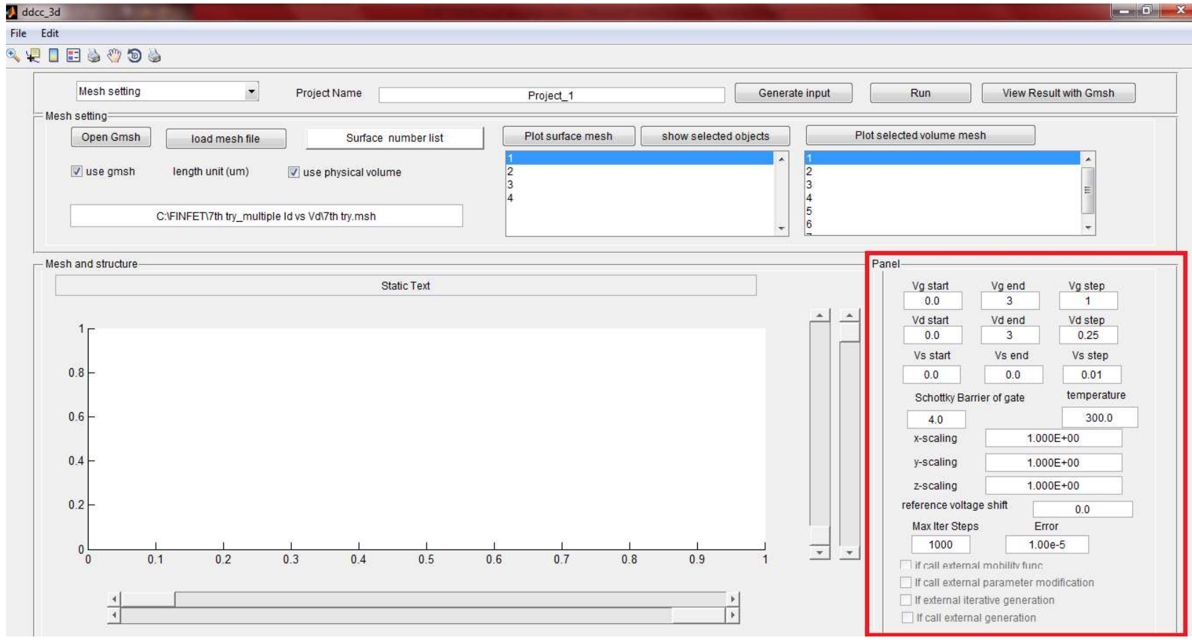


Figure 3.11: Panel Section Parameter Setting

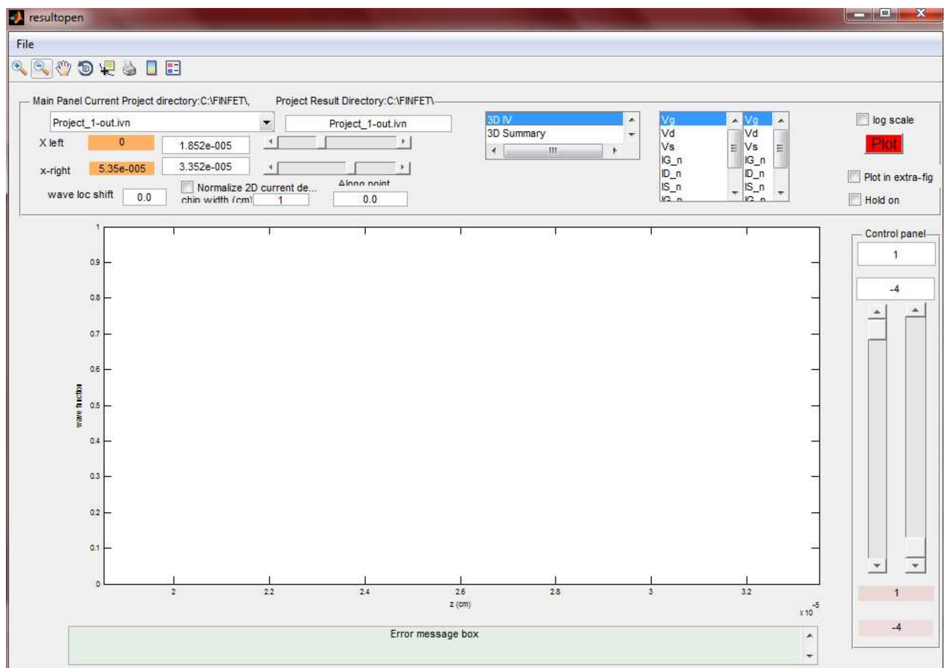


Figure 3.12: Result Observation Platform

CHAPTER 4

RESULT AND DISCUSSION

4.1 Successful Implementation of 3nm Strained FinFET in GMSH and 3D-DDCC

3nm strained FinFET was successfully constructed using GMSH software. The Top View, Front View, Side View of 3nm FinFET in GMSH upon successful meshing process are displayed in Figure 4.1, 4.2 and 4.3. By referring to Overall view of 3nm FinFET in Figure 4.4, it is clearly shown that the FinFET is constructed with Drain, Source, Channel, Gates, Oxide Layer, Oxide Fiim and Substrate Layer assigned. Besides, FinFET structure was implemented in SOI Technology as there was an oxide film in between Si substrate and Silicon layer. This structure decreased the respective parasitic capacitance of FinFET that contributing to enhanced performance. However, the output obtained in GMSH was not enough to illustrate the gate length of 3nm FinFET visually. This can be verified by observing the cross-sectional view of 3nm FinFET after the mesh file was loaded in 3D-DDCC software as displayed in Figure 4.6 and 4.7. Both figures shows that the FinFET design implemented having 3nm gate length, while the length of source and drain are 1nm each. Besides, the design fulfilled design rule that the fin width have to be equal to half of the value of channel length(2nm), which was proven in the top view as illustrated in Figure 4.5.

GMSH

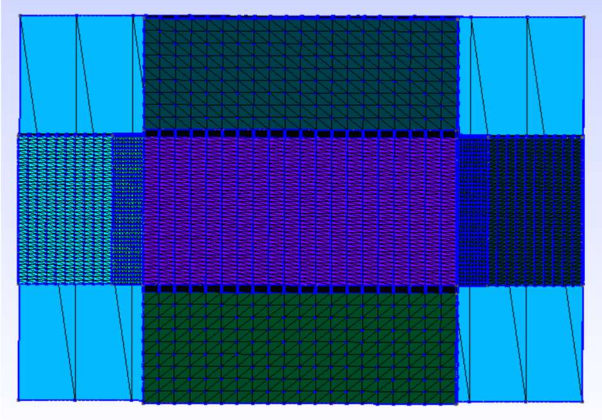


Figure 4.1: Top view of 3nm FinFET after meshing

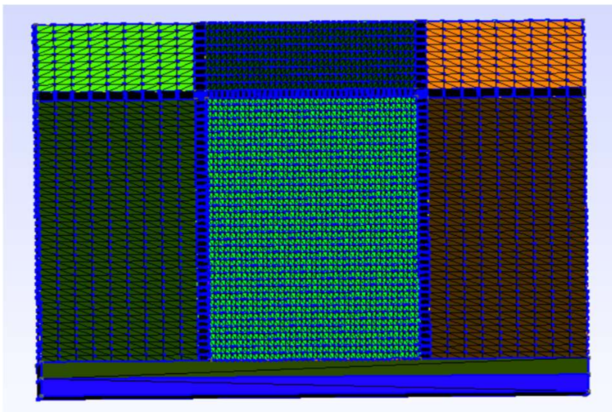


Figure 4.2: Front view of of 3nm FinFET after meshing

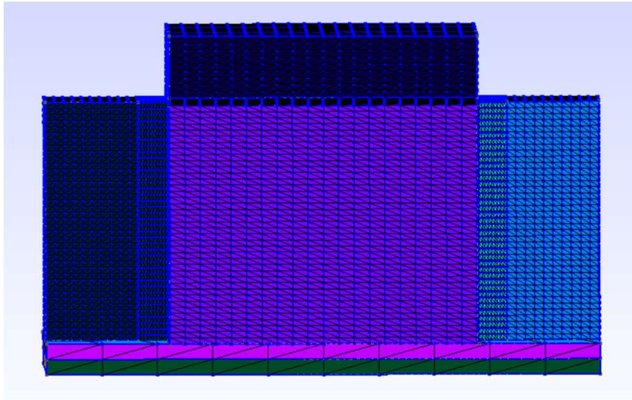


Figure 4.3: Side view of of 3nm FinFET after meshing

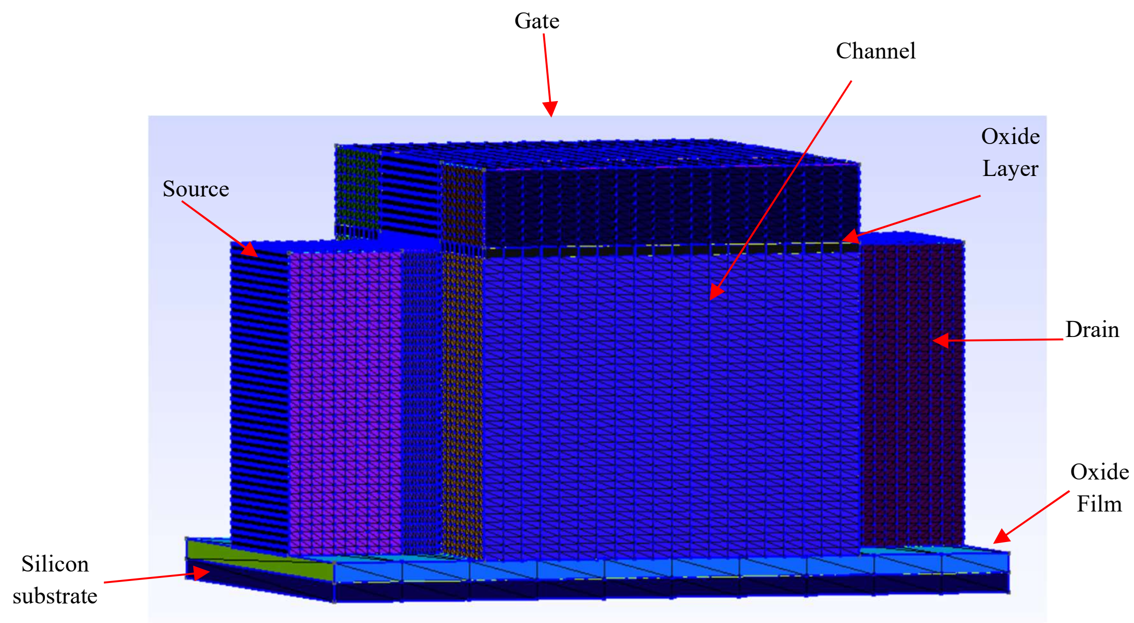


Figure 4.4: Overall View of 3nm FinFET after meshing

3D-DDCC

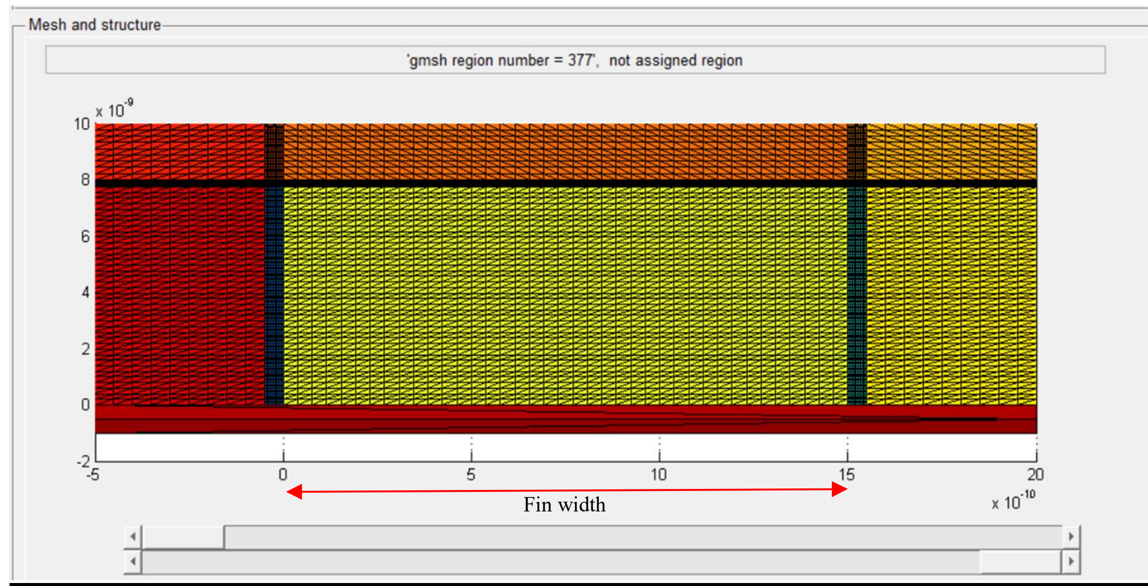


Figure 4.5: Front View of 3nm FinFET in 3D-DDCC software

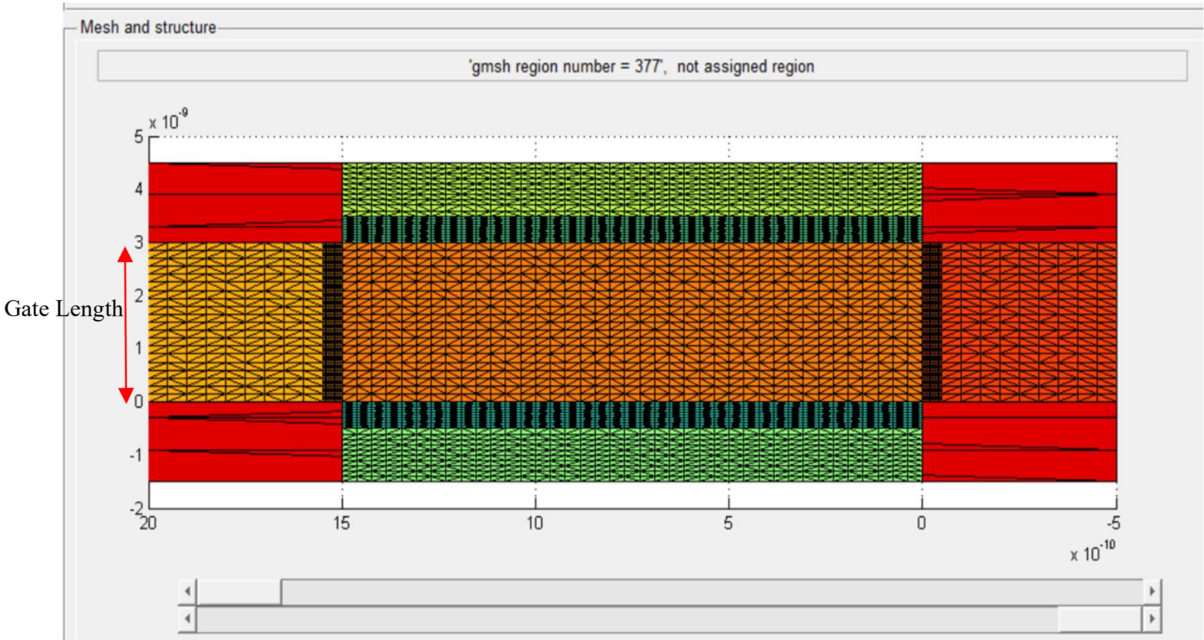


Figure 4.6: Top View of 3nm FinFET in 3D-DDCC software

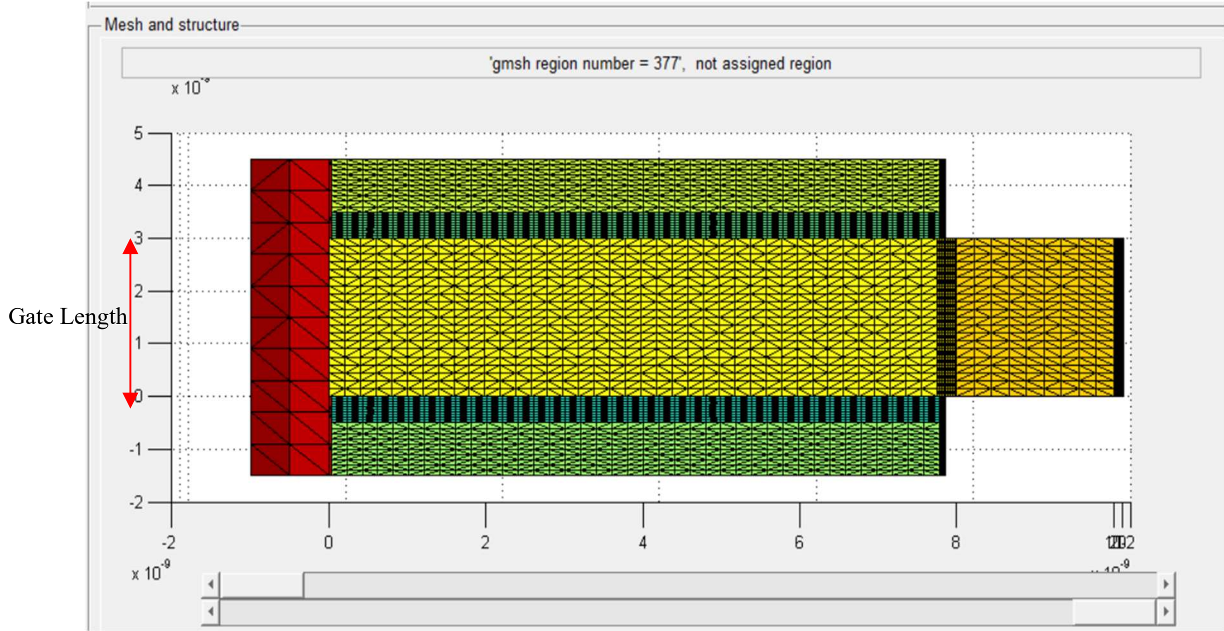


Figure 4.7: Side View of 3nm FinFET in 3D-DDCC software

4.2 Simulation of current-voltage characteristic

In order to study the performance of 3nm strained FinFET designed, two aspects need to be analyzed which are output and transfer characteristic. For output characteristic, 'I_D against V_D' graphs were plotted to investigate the relation between output drain voltage and drain current of FinFET. While transfer characteristic was analyzed by observing 'I_D against V_G' graph for the relation between gate voltage and drain current. Comparison was done between conventional FinFET and strained FinFET to determine the design with better performance.

4.2.1 Output Characteristic IV curve of Si based FinFET

Figures 4.8 to 4.11 show the Drain Current, I_D against Gate Voltage, V_G electrical characteristic curves of 3 nm Si FinFET. The saturation point at different values of gate voltage are observed and tabulated in Table 4.1.

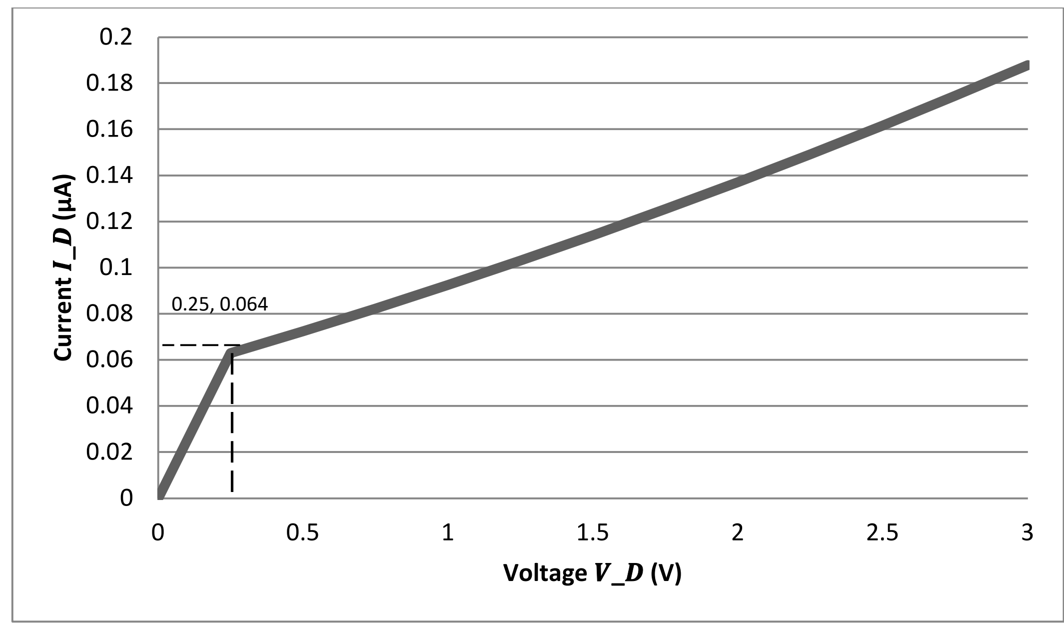


Figure 4.8: Si FinFET Drain Current, ID_n against Drain Voltage, V_D graph with Gate Voltage, V_G = 0 V

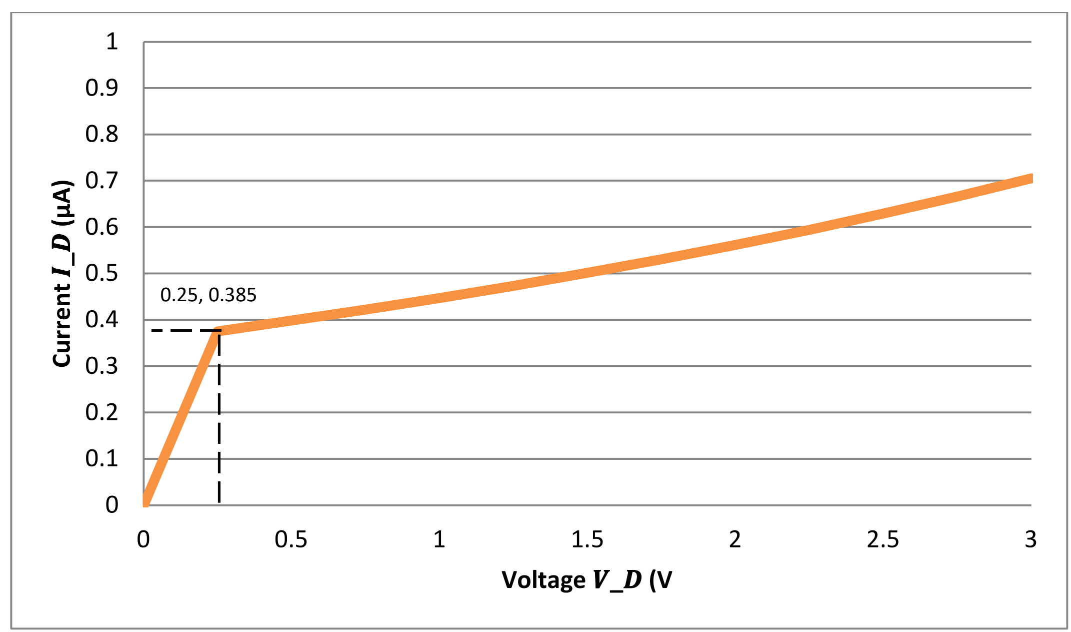


Figure 4.9: Si FinFET Drain Current, ID_n against Drain Voltage, V_D graph with Gate Voltage, V_G = 1 V

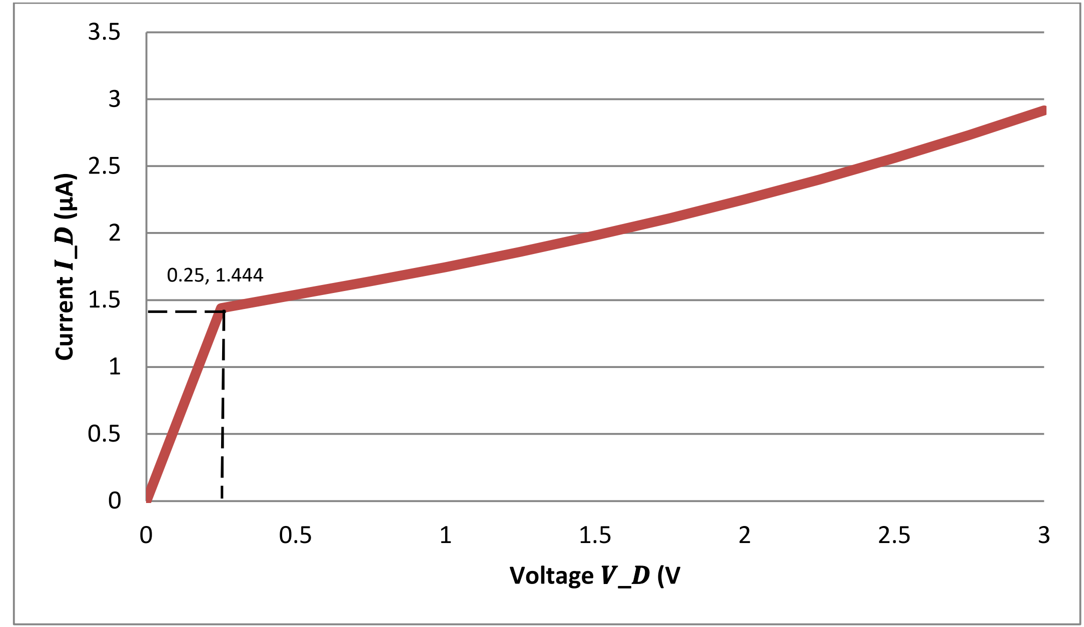


Figure 4.10: Si FinFET Drain Current, ID_n against Drain Voltage, V_D graph with Gate Voltage, V_G = 2 V

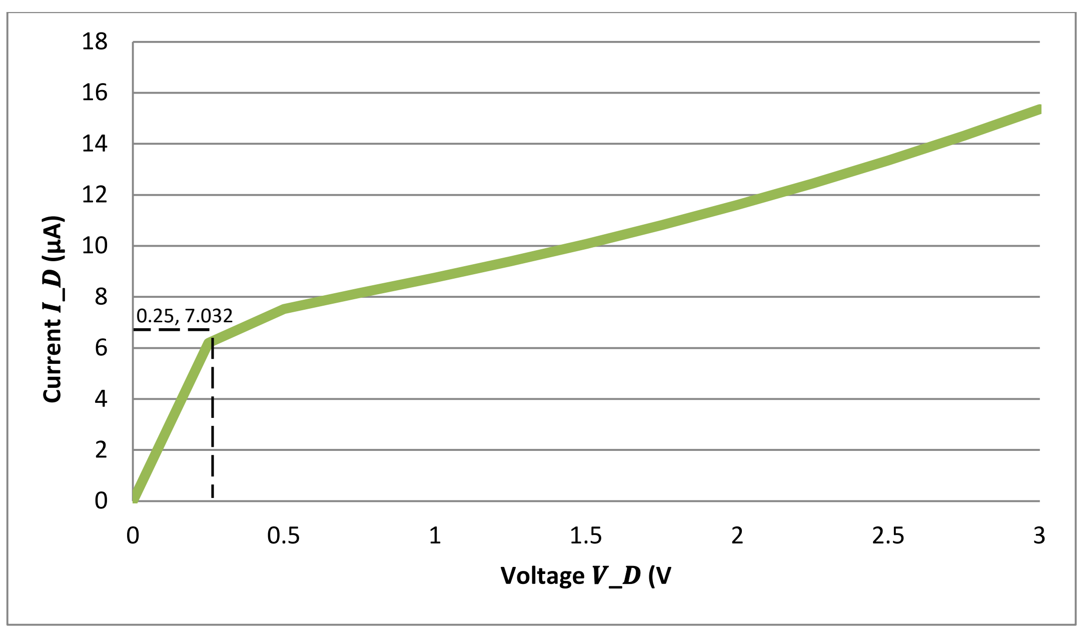


Figure 4.11: Si FinFET Drain Current, ID_n against Drain Voltage, V_D graph with Gate Voltage, V_G = 3 V

Table 4.1: Saturation Points of Si FinFET at Different Value of Gate Voltages

Gate voltage, V_G (V)	Saturated current, $I_{D,SAT}$ (μA)	Saturated voltage, $V_{D,SAT}$ (V)
0	0.064	0.25
1	0.385	0.25
2	1.444	0.25
3	7.032	0.25

4.2.2 Output Characteristic IV curve of SiGe based FinFET

The Drain Current, I_D against Gate Voltage, V_G electrical characteristic curves of 3 nm SiGe FinFET are plotted using the 3D-DDCC simulator as shown in Figures 4.12 to 4.15. The output characteristics at different values of gate voltage are observed and tabulated in Table 4.2.

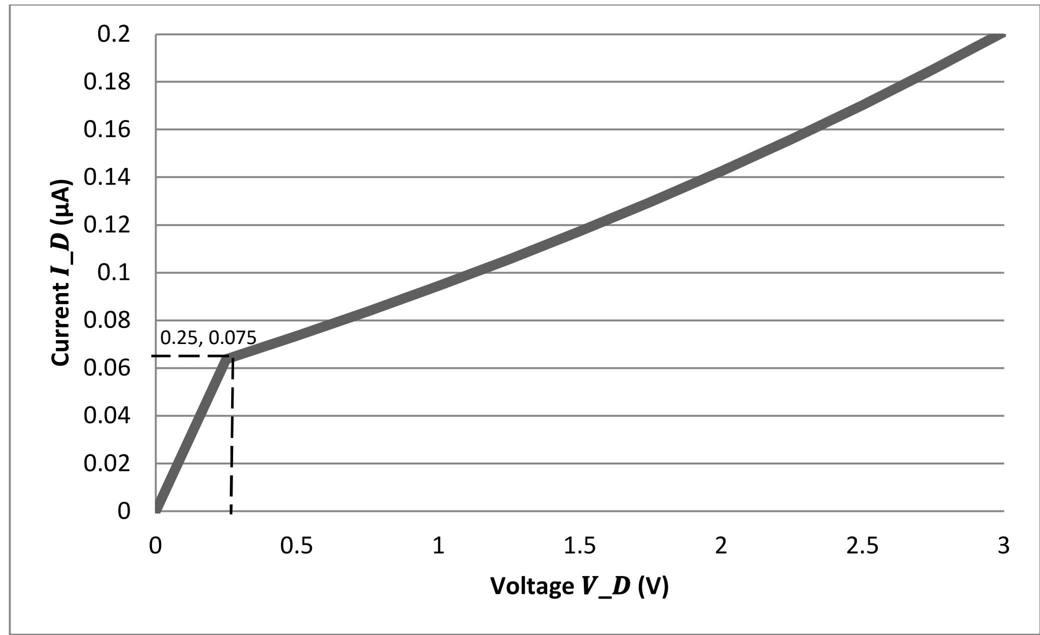


Figure 4.12: SiGe FinFET Drain Current, IDn against Drain Voltage, VD graph with Gate Voltage, VG = 0 V

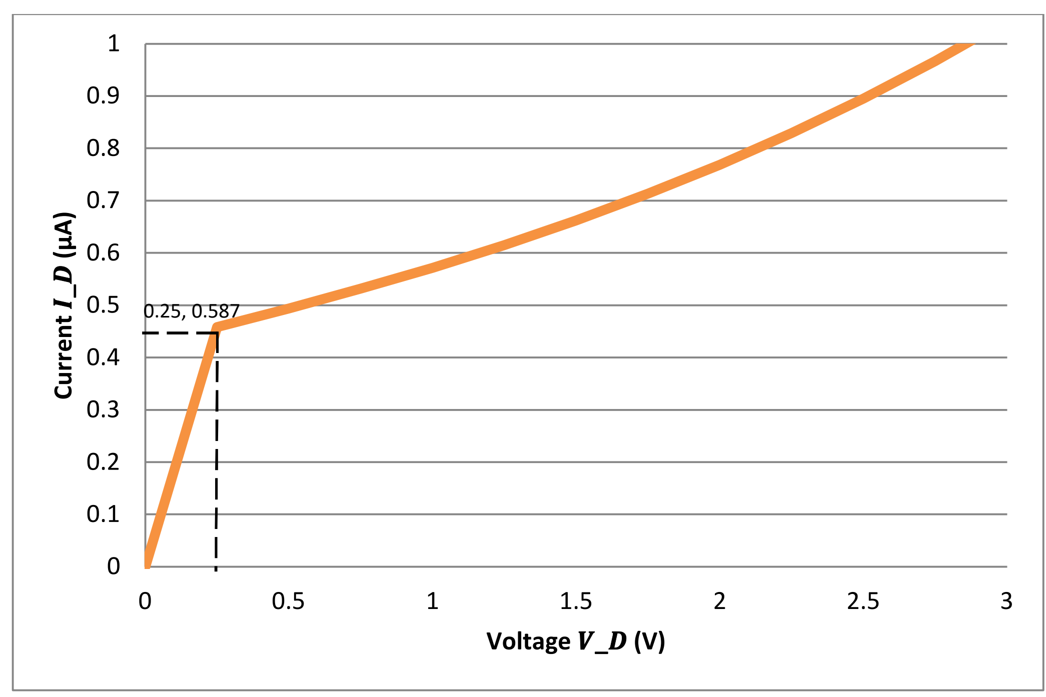


Figure 4.13: SiGe FinFET Drain Current, IDn against Drain Voltage, VD graph with Gate Voltage, VG = 1 V

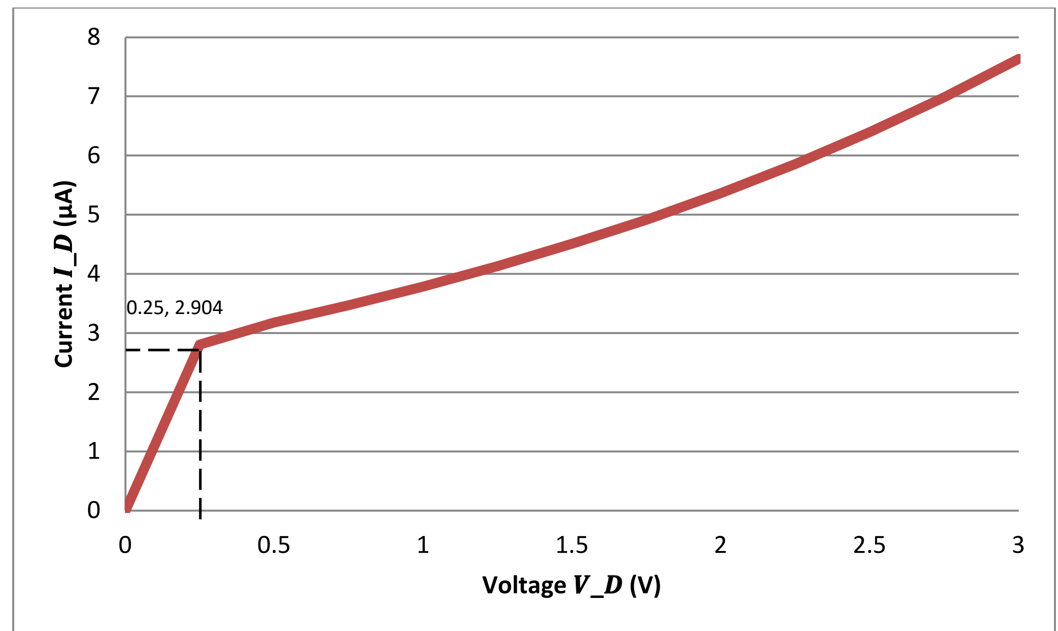


Figure 4.14: SiGe FinFET Drain Current, IDn against Drain Voltage, VD graph with Gate Voltage, VG = 2 V

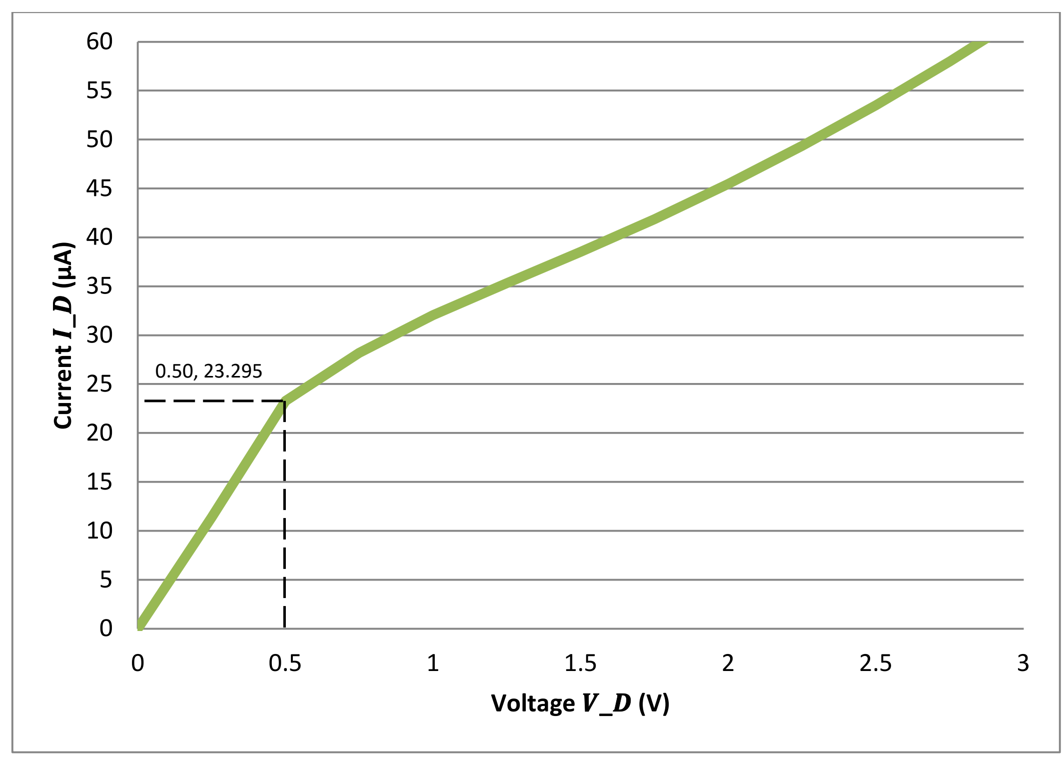


Figure 4.15: SiGe FinFET Drain Current, IDn against Drain Voltage, VD graph with Gate Voltage, VG = 3 V

Table 4.2: Saturation Points of SiGe FinFET at Different Value of Gate Voltages

Gate voltage, V_G (V)	Saturated current, $I_{D,SAT}$ (µA)	Saturated voltage, $V_{D,SAT}$ (V)
0	0.075	0.25
1	0.587	0.25
2	2.904	0.25
3	23.295	0.50

4.2.3 Discussion on both the Output Characteristic IV curve of FinFET

The output characteristic curves of both conventional 3nm Si FinFET and 3nm strained SiGe FinFET obtained from simulation are proven to exhibit correct characteristics of FinFET. By observing the graphs from Figure 4.7 to 4.14, the curves were divided into 2 regions which are linear (triode) region and saturation region. Linear region is determined when the drain voltage, V_D is lower than saturated voltage, $V_{D, SAT}$. In the contrary, saturation region falls in the region when the drain voltage, V_D is greater than saturated voltage, $V_{D, SAT}$.

At the origin of the curve, the drain voltage and drain current had the value equal to zero indicating that the potential of drain was same with the potential of the source at this point. With a fixed value of gate voltage was being applied, output drain current started to increase with drain voltage, V_D in linear region. This condition continued until it reached saturation point. At saturation point, any increase in drain voltage, V_D will only cause minimal increment in drain current, I_D. During this stage, the channel was pinched off and FinFET operated in the saturation region.

Moreover, it is found that the output drain current, I_D increased when the gate voltage increased. Gate voltage applied helped to attract the electrons in the substrate layer to form an inversion layer between the drain and source regions which known as channel. This allowed electrons to flow across the channel. When the gate voltage was increased, more electrons were attracted from the substrate layer to the surface underneath the oxide layer due to the potential difference. The larger electric field

generated increased the channel width. As a result, the output current flew across the channel more easily. This applied the same to both Si and SiGe FinFET.

By observing the value of saturation point at $V_G = 0$ as tabulated in Table 4.1 and 4.2, it is discovered that SiGe FinFET saturated at approximately 0.25 V and 0.064 μA while Si FinFET saturated at approximately 0.25 V and 0.075 μA. This violated the theory that there should be no any current flow in the transistor when the gate voltage was lower than the threshold voltage. The occurrence of the subs-threshold was due to short-channel effect. When the size of the FinFET was shrinking towards 20nm, the gate started to lose its control on the channel region due to the depletion region of the drain exerts under the gate and extended towards the source region. As a result, there were some currents flowing across the channel before the gate voltage overcome the threshold voltage. The current leakage of SiGe FinFET is identified to be higher than Si FinFET by 17.19% due to enhanced electron mobility. Nonetheless, the current leakage occurred at an extremely low value measured in micro ampere, μA which was almost no current flows for both Si and SiGe FinFET. This kind of current leakage will not cause any significant side-effects such as power consumption and temperature dissipation to the devices.

By comparing the value of saturation point between Si FinFET and Strained SiGe FinFET as tabulated in the Table 4.1 and Table 4.2, SiGe FinFET was observed to have larger saturation current and voltage as compared to Si FinFET. Taking the output saturation point at $V_G = 3V$ to be analyzed, the saturation point of Si FinFET was (0.25V, 7.032 μA) while the saturation point of SiGe FinFET was (0.50V, 23.295 μA). This is

because silicon atoms were stretched beyond their normal interatomic distance when germanium atoms were added into it. The reduction of atomic forces that obstruct electrons' ability to travel freely across transistors enable SiGe to has greater electron mobility than Si. Hence, it can be concluded that output current of SiGe based FinFET is higher due to greater electrical conduction.

4.2.4 Transfer Characteristic IV curve of Si based FinFET

Figures 4.16 to 4.21 show the particular transfer characteristics of the 3 nm Si based FinFET with various value of V_D in order to determine the threshold voltage of the FinFET designed.

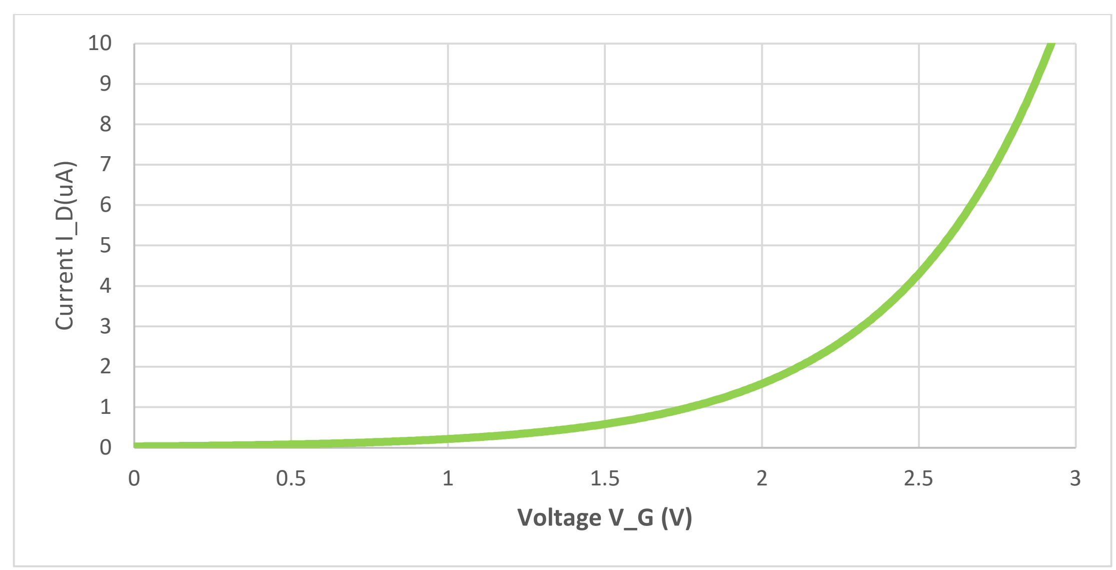


Figure 4.16: Si FinFET Drain Current, ID_n against Gate Voltage, V_G graph with Drain Voltage, V_D = 1 V

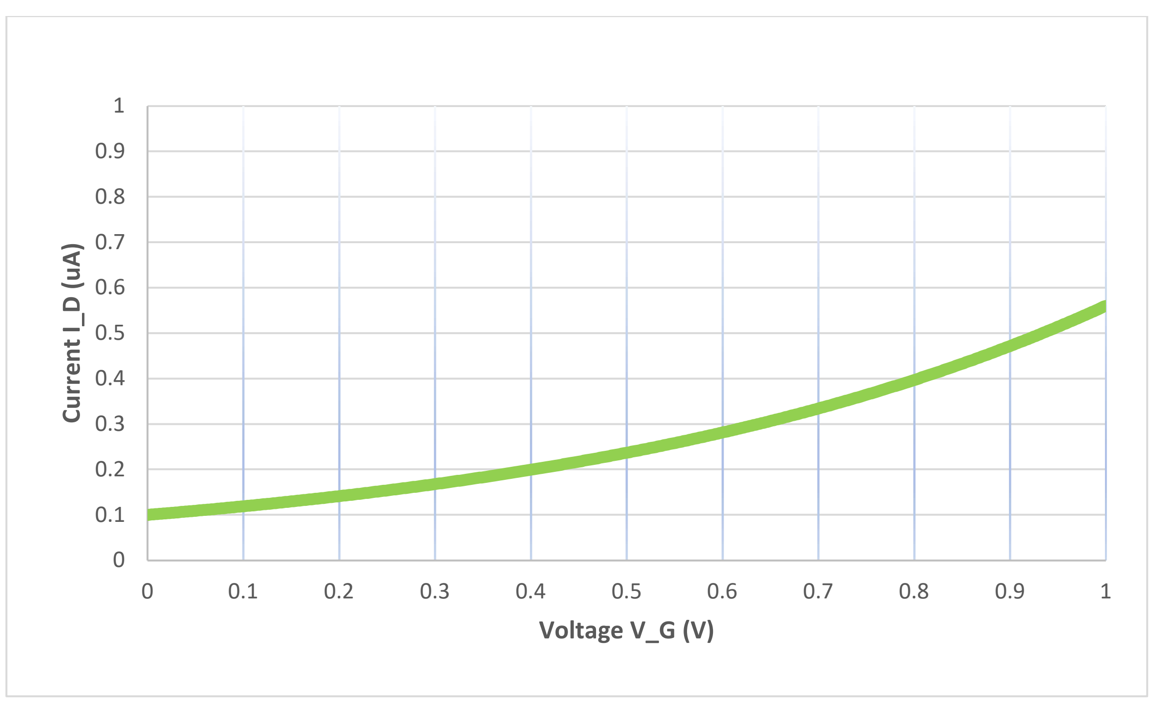


Figure 4.17: Si FinFET Zoomed In version of Drain Current, ID_n against Gate Voltage, V_G graph with Drain Voltage, V_D = 1 V

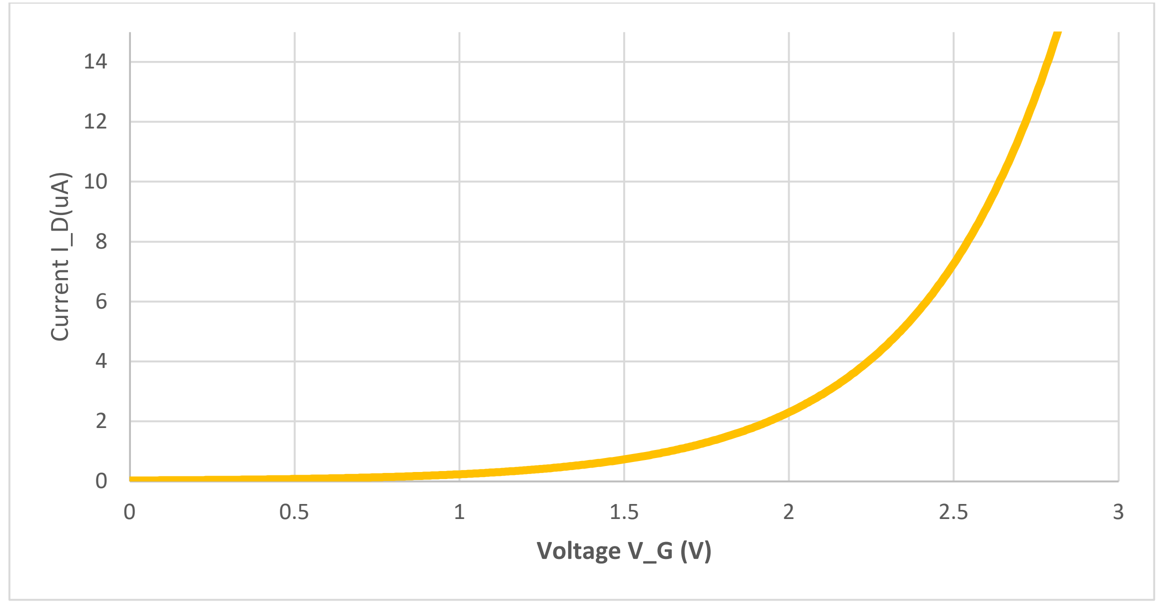


Figure 4.18: Si FinFET Drain Current, ID_n against Gate Voltage, V_G graph with Drain Voltage, V_D = 2 V

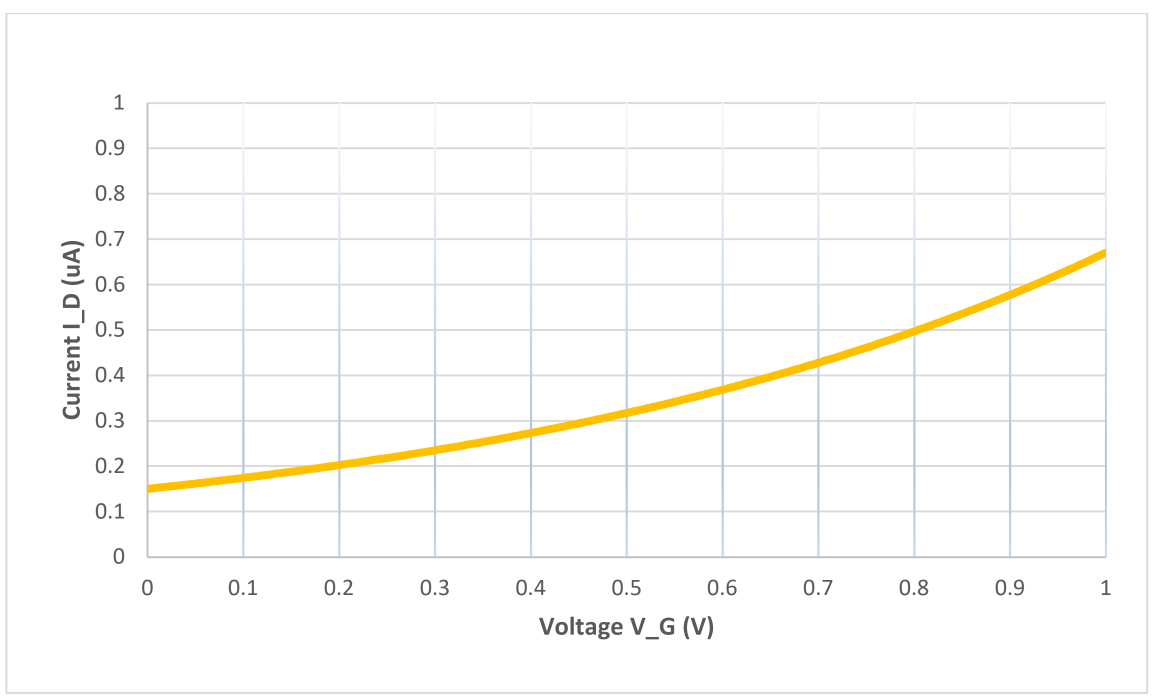


Figure 4.19: Si FinFET Zoomed In version of Drain Current, ID_n against Gate Voltage, V_G graph with Drain Voltage, V_D = 2 V

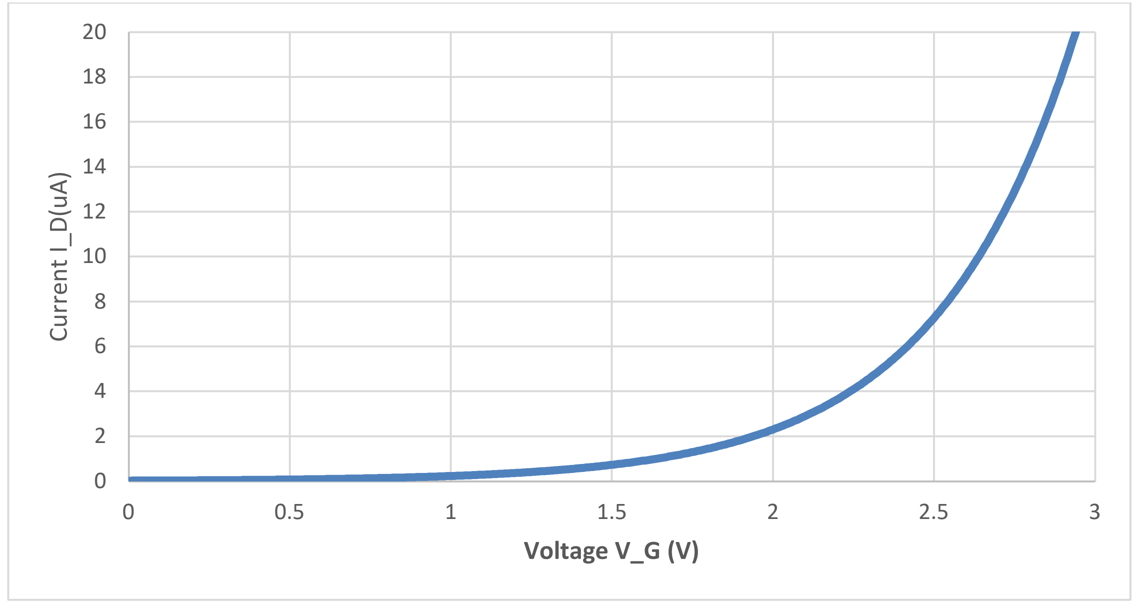


Figure 4.20: Si FinFET Drain Current, ID_n against Gate Voltage, V_G graph with Drain Voltage, V_D = 3 V

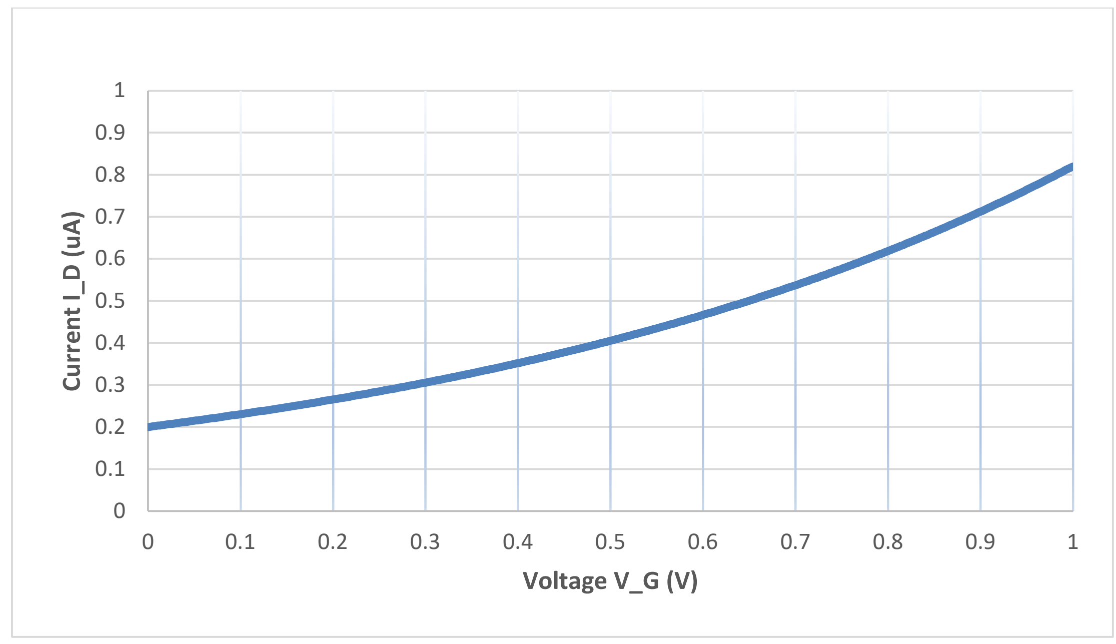


Figure 4.21: Si FinFET Zoomed In version of Drain Current, ID_n against Gate Voltage, V_G graph with Drain Voltage, V_D = 3 V

4.2.5 Transfer Characteristic IV curve of SiGe based FinFET

Figures 4.22 to 4.27 show the particular transfer characteristics of the 3 nm SiGe based FinFET with various value of V_D in order to determine the threshold voltage of the FinFET designed.

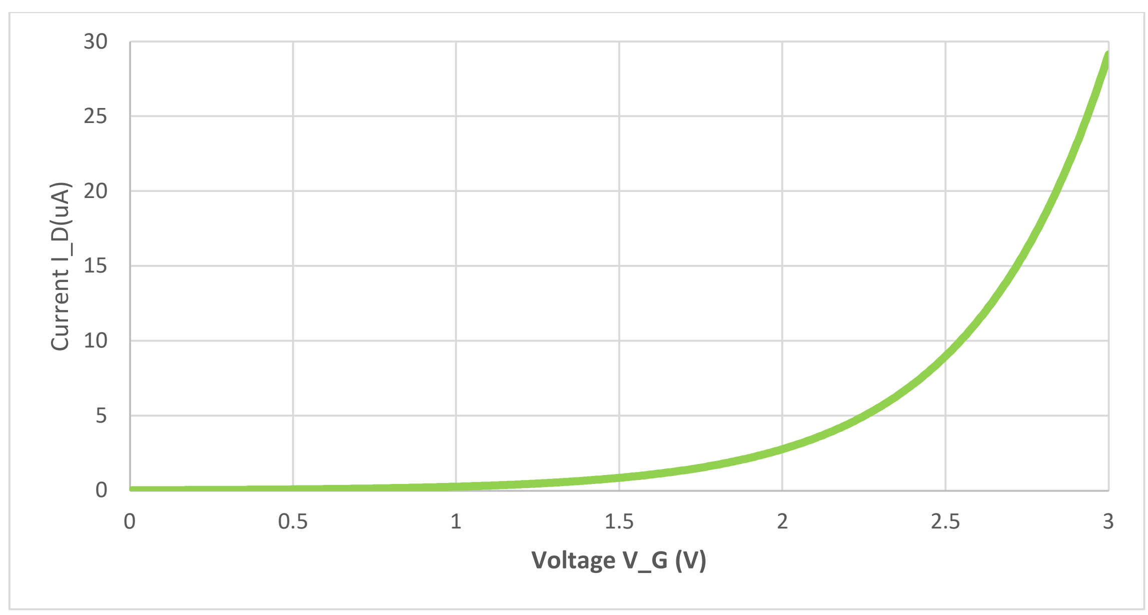


Figure 4.22: SiGe FinFET Drain Current, ID_n against Gate Voltage, V_G graph with Drain Voltage, V_D = 1 V

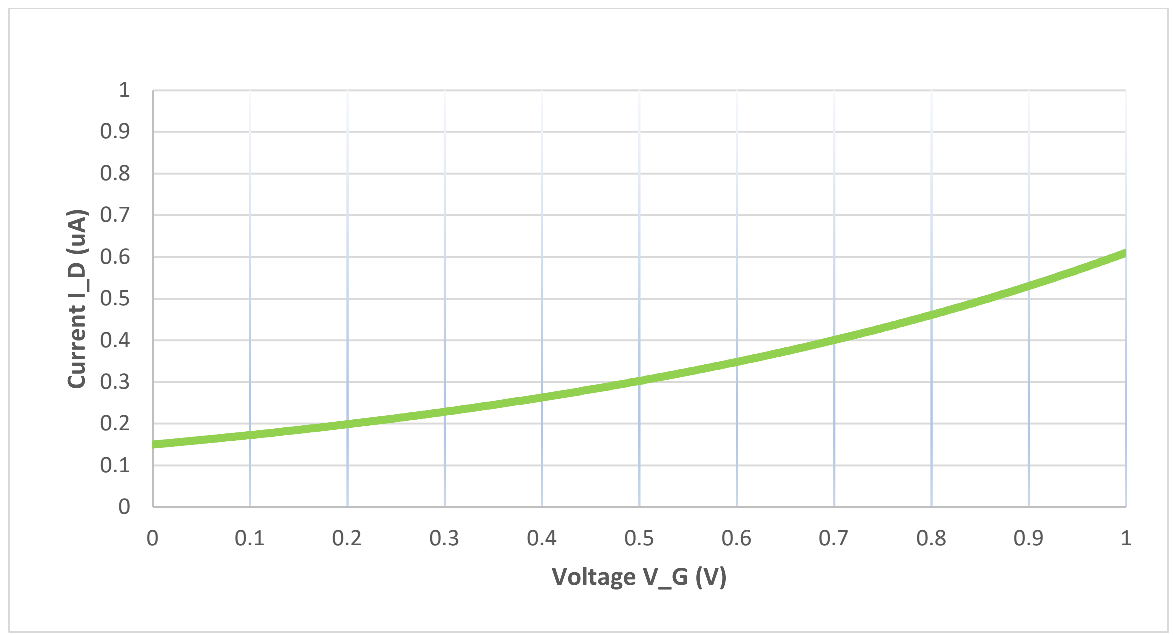


Figure 4.23: SiGe FinFET Zoomed In version of Drain Current, ID_n against Gate Voltage, V_G graph with Drain Voltage, V_D = 1 V

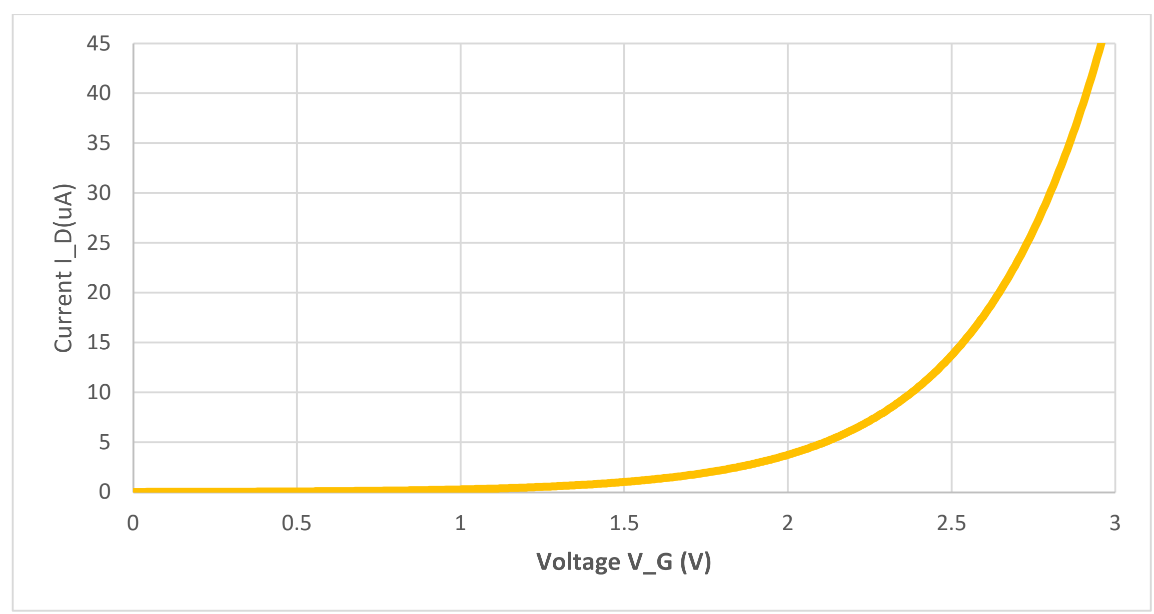


Figure 4.24: SiGe FinFET Drain Current, ID_n against Gate Voltage, V_G graph with Drain Voltage, V_D = 2 V

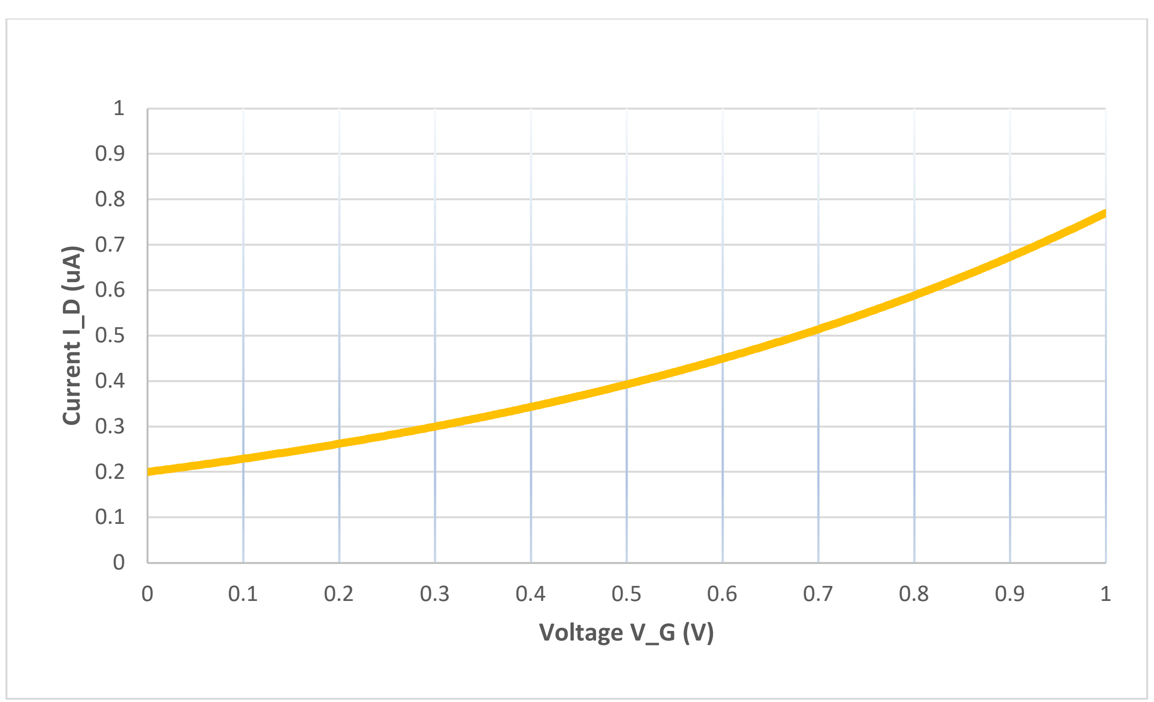


Figure 4.25: SiGe FinFET Zoomed In version of Drain Current, ID_n against Gate Voltage, V_G graph with Drain Voltage, V_D = 2 V

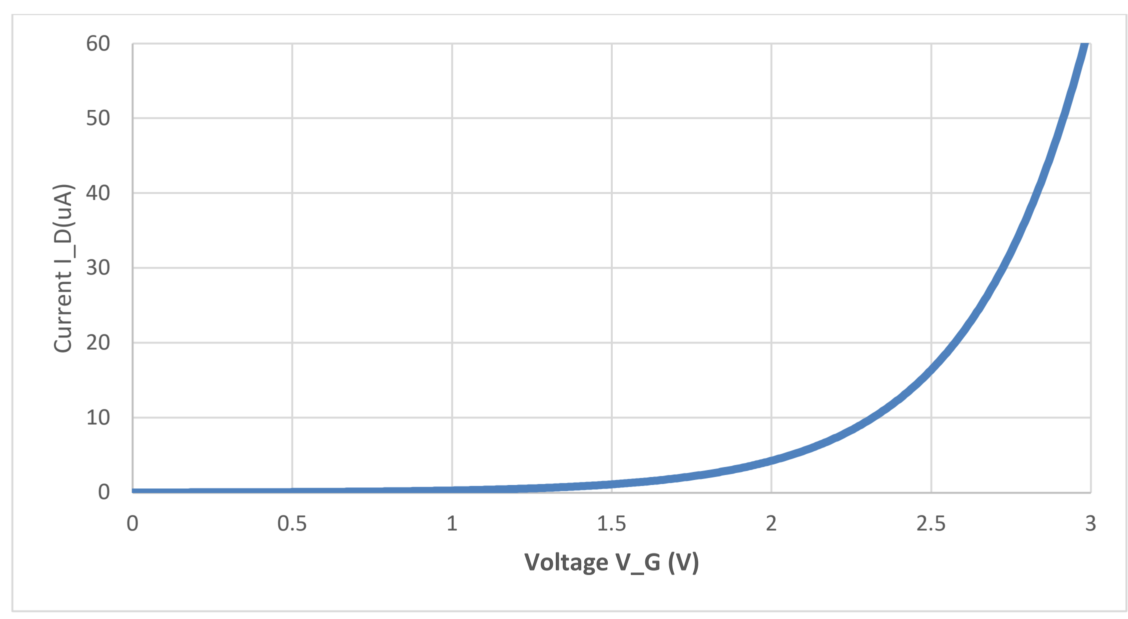


Figure 4.26: SiGe FinFET Zoomed In version of Drain Current, ID_n against Gate Voltage, V_G graph with Drain Voltage, V_D = 3 V

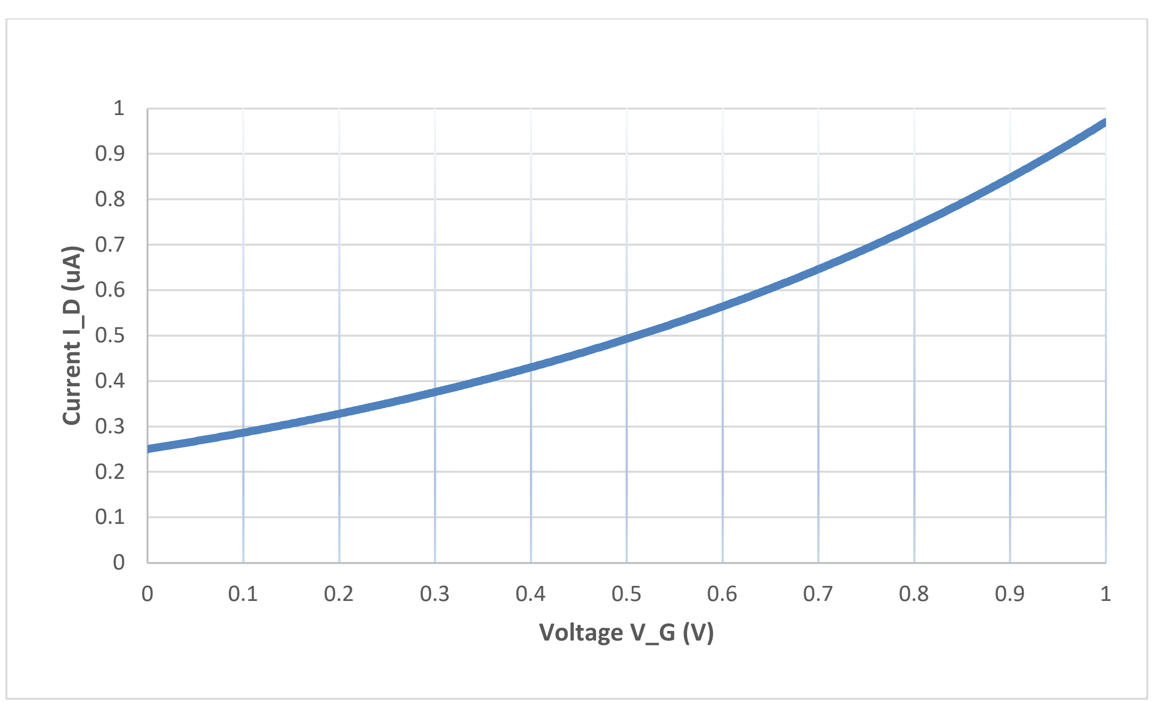


Figure 4.27: SiGe FinFET Zoomed In version of Drain Current, ID_n against Gate Voltage, V_G graph with Drain Voltage, V_D = 3 V

4.2.6 Discussion on both the Transfer Characteristic IV curve of FinFET

Figure 4.16 to 4.27 show the variation of the 3 nm Si and SiGe FinFETs' drain current, I_D as a function of gate voltage, V_G and their respective zoomed in waveform in order to determine their start off point. From the observation on the figures above, the threshold voltage, V_T of both FinFETs are identified to be 1 V which means the FinFET is in the 'ON' state only when the gate voltage applied is above this threshold level. This behavior agrees with the ideal transfer characteristic of the FinFET transistor.

By observing the zoomed in version of drain current. I_D against drain voltage, V_D curves of Si FinFET in Figures 4.16, 4.18 and 4.20, drain current, I_D are found to consist of some current when gate voltage, V_G = 0 V. When drain voltage, V_D increased from 1V to 3 V, drain current, I_D is equaled to 0.1 μA, 0.15 μA and 0.20 μA respectively. In shorts, it can be concluded that the greater the drain voltage is applied, the higher the value of the drain current exists on the 0 V of gate voltage. This condition applies the same to SiGe based FinFET with more current exist as shown in Figures 4.22, 4.24 and 4.26. The phenomenon is caused by Drain induced barrier lowering (DIBL) effect. Upon the application of a high drain voltage, more holes were generated near the drain due to influence of the drain electric field. This led to greater capability of drain in attracting the electrons across the channel region from the source. The gate became more positive bias which lowered down the threshold voltage. As a result, ability of the gate in attracting the electrons in the substrate layer was enhanced. The depletion region started to extend into the gate region resulted in easier formation of inversion layer. (Rahim, 2012). Hence, the flowing of the current along the channel is improved.

CHAPTER 5

CONCLUSIONS AND RECOMMENDATIONS

5.1 Conclusion

In conclusion, all the objectives of this research have been achieved. The fundamental of FinFET and strained technology are studied and understood to get general concept prior to the construction of FinFET. 3nm strained FINFET is implemented using GMSH software with successful meshing of the design into 2D and 3D structure.

Simulation of the FinFET is carried out by using 3D-DDCC software. The parameter used for strained SiGe FinFET and conventional Si FinFET are identified and constrained in the simulator to analyze the respective device characteristic. Both FinFET designs implemented conform with the FinFET I-V characteristic. As discussed in the chapter 4, the performance of the SiGe FinFET is proven to produce higher output current as compared to Si FinFET. This is due to SiGe has better electrical conduction when Ge atom is added into Si. Moreover, there is negligible current leakage problem due to the effect of high electric fields at the source and drain regions when channel length decreases. Therefore, 3 nm SiGe FinFET could be a recommended candidate for electronic device with the requirements of high switching speed and low current leakage. In conclusion, it was evident that the objectives of this project had been achieved. Further study can be done to reduce the effect of leakage current which will be discuss in next section.

5.2 Future Recommendations

For future improvement of the research, it is recommended to always follow the design rules that the width of the fin width must be at least the half of the channel length. Besides, oxide layer of the model cannot be too thick. Else, the FinFET design implemented will not obey the standard characteristic of MOSFET. Moreover, different transfinite algorithm must be assigned correctly to each surfaces of the model accordingly, which is not an easy job as there were large amount of surfaces in the FinFET model. Hence, it is suggested to writing the script with comment append to ease the debug process. For any doubt in determining the transfinite algorithm to be used as well as parameter for the material range setting, the example given by the founder of both GMSH and 3D-DDCC software will be the best reference to troubleshoot the errors.

Although the leakage current of strain FinFET is found to be low, further study can be done to reduce the short-channel effect. This can be achieved by using high-permittivity (high-k) dielectric for gate oxides(H.Moriya, 2017). For instances, HfO_2, ZrO_2, and TiO_2 are suitable candidates to be used. Moreover, strained technology on triangular fin shape devices is worth to be studied. The lightly doped fins of triangular fin shape structure are more susceptible for short channel effects with significant improvement in driving current as compared to rectangular shape FinFET (Shashank et, 2016). Moreover, strained technology can be adopted in gate-all-around FET (GAAFET) design, which is believed to produce higher drive current and low leakage current through the stacking of nanosheets(Mukhesh,2022).

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APPENDICES

Appendices A- Scripting Code of 3nm Strained FinFET model

```
lc = 0.0002;
nm=1.0e-10 ;
finwidth=10;
siliconthick=5;
height3=finwidth+siliconthick; // 15
Nwire=40;
Noxide=10;

//FIN AND OXIDE LAYER
Point(1) = {0, 0, 0, lc};
Point(2) = {15*nm, 0, 0, lc} ;
Point(3) = {15*nm, 77.5*nm, 0, lc} ;
Point(4) = {0, 77.5*nm, 0, lc} ;
Point(5) = {-0.5*nm, 0, 0, lc} ;
Point(6) = {-0.5*nm, 77.5*nm, 0, lc} ;
Point(7) = {-0.5*nm, 80*nm, 0, lc} ;
Point(8) = {0*nm, 80*nm, 0, lc} ;
Point(9) = {15*nm, 80*nm, 0, lc} ;
Point(10) = {15.5*nm, 80*nm, 0, lc} ;
Point(11) = {15.5*nm, 77.5*nm, 0, lc} ;
Point(12) = {15.5*nm, 0*nm, 0, lc} ;

//GATE
Point(13) = {20*nm, 0*nm, 0, lc} ;
Point(14) = {20*nm, 100*nm, 0, lc} ;
Point(15) = {-5*nm, 100*nm, 0, lc} ;
Point(16) = {-5*nm, 0*nm, 0, lc} ;
Point(23) = {-0.5*nm, 100*nm,0, lc};
```

```
Point(24) = {15.5*nm, 100*nm, 0, lc};
Point(25) = {20*nm, 80*nm, 0, lc};
Point(26) = {-5*nm, 80*nm, 0, lc};
Point(27) = {20*nm, 77.5*nm, 0, lc};
Point(28) = {-5*nm, 77.5*nm, 0, lc};
Point(29) = {15*nm,100*nm, 0, lc};
Point(30) = {0*nm, 100*nm, 0, lc};

//OXIDE FILM
Point(17) = {20*nm, 0*nm, -height3*nm, lc} ;
Point(18) = {-5*nm, 0*nm, -height3*nm, lc} ;
Point(19) = {20*nm, -5*nm, -height3*nm, lc} ;
Point(20) = {-5*nm, -5*nm, -height3*nm, lc} ;

//SUBSTRATE
Point(21) = {20*nm, -10*nm, -height3*nm, lc} ;
Point(22) = {-5*nm, -10*nm, -height3*nm, lc} ;


//FIN AND OXIDE LAYER
Line(1) = {1, 4};
Line(2) = {4, 3};
Line(3) = {3, 2};
Line(4) = {2, 1};
Line(5) = {1, 5};
Line(6) = {5, 6};
Line(7) = {6, 4};
Line(8) = {6, 7};
Line(9) = {7, 8};
Line(10) = {8, 4};
Line(11) = {8, 9};
```

```
Line(12) = {9, 3};
Line(13) = {9, 10};
Line(14) = {10, 11};
Line(15) = {11, 3};
Line(16) = {11, 12};
Line(17) = {12, 2};

//GATE
Line(18) = {5, 16};
Line(19) = {28, 26};
Line(40) = {28, 16};
Line(42) = {28, 6};
Line(20) = {15, 26};
Line(21) = {15, 23};
Line(22) = {7, 23};
Line(23) = {7, 26};
Line(24) = {24, 29};
Line(38) = {29, 30};
Line(39) = {30, 23};
Line(44) = {9, 29};
Line(45) = {8, 30};
Line(25) = {12, 13};
Line(26) = {13, 27};
Line(41) = {25, 27};
Line(43) = {11, 27};
Line(27) = {14, 25};
Line(28) = {14, 24};
Line(29) = {10, 24};
Line(30) = {10, 25};

//OXIDE FILM & SUBSTRATE
```

```
Line(31) = {17, 18};
Line(32) = {18, 20};
Line(33) = {17, 19};
Line(34) = {19, 20};
Line(35) = {19, 21};
Line(36) = {20, 22};
Line(37) = {21, 22};

Transfinite Line{1,6,2,3,4,11,16,26,38,40}=Nwire;
Transfinite
Line{5,7,9,8,10,12,13,14,15,17,41,42,43,44,45,18,19,20,21,22,23,24,25,27,28,29,30,39}
=Noxide;


//FIN AND OXIDE LAYER
Line Loop(18) = {2, 3, 4, 1};
Plane Surface(1) = {18};
//+
Line Loop(20) = {1, -7, -6, -5};
Plane Surface(2) = {20};
//+
Line Loop(22) = {10, -7, 8, 9};
Plane Surface(3) = {22};
//+
Line Loop(24) = {11, 12, -2, -10};
Plane Surface(4) = {24};
//+
Line Loop(26) = {13, 14, 15, -12};
Plane Surface(5) = {26};
//+
Line Loop(28) = {16, 17, -3, -15};
```

```
Plane Surface(6) = {28};

//GATE
Line Loop(44) = {16, 25, 26, -43};
Plane Surface(14) = {44};
//+
Line Loop(46) = {14, 43, -41, -30};
Plane Surface(15) = {46};
//+
Line Loop(48) = {27, -30, 29, -28};
Plane Surface(16) = {48};
//+
Line Loop(50) = {13, 29, 24, -44};
Plane Surface(17) = {50};
//+
Line Loop(52) = {38, -45, 11, 44};
Plane Surface(18) = {52};
//+
Line Loop(54) = {45, 39, -22, 9};
Plane Surface(19) = {54};
//+
Line Loop(56) = {21, -22, 23, -20};
Plane Surface(20) = {56};
//+
Line Loop(58) = {8, 23, -19, 42};
Plane Surface(21) = {58};
//+
Line Loop(60) = {6, -42, 40, -18};
Plane Surface(22) = {60};

//OXIDE FILM & SUBSTRATE
```

```
Line Loop(40) = {31, 32, -34, -33};
Plane Surface(12) = {40};
//+
Line Loop(42) = {37, -36, -34, 35};
Plane Surface(13) = {42};

Transfinite Surface{1,2,3,4,5,6,12,13,14,15,16,17,18,19,20,21,22};



Extrude {0, 0, 30*nm} {
   Surface{1,2,3,4,5,6}; Layers{20};          // CHANNEL & OXIDE LAYER
 }
Extrude {0, 0, -5*nm} {
   Surface{1}; Layers{10};                    // CHANNEL
 }
Extrude {0, 0, 5*nm} {
   Surface{82}; Layers{10};                   // CHANNEL
 }
Extrude {0, 0, -10*nm} {
   Surface{214}; Layers{10};                  // SOURCE
 }
Extrude {0, 0, 10*nm} {
   Surface{236}; Layers{10};                  // DRAIN
 }
Extrude {0, 0, 30*nm} {
   Surface{14,15,16,17,18,19,20,21,22}; Layers{20};        // GATE
 }
Extrude {0, 0, 60*nm} {
   Surface{12,13}; Layers{10};                // OXIDE FILM & SUSBTRATE
 }
```

```
Physical Surface(1) = {179,161,157,135,125,121,99};                 //OXIDE LAYER
Physical Surface(2) = {267,279,271};                                //DRAIN
Physical Surface(3) = {257,245,249};                                //SOURCE
Physical Surface(4) = {297,319,333,345,363,377,403,421,433,451,473};   //GATE


Physical Volume(1) = {2,3,4,5,6};                                   //OXIDE LAYER
Physical Volume(2) = {1,8,7};                                       //CHANNEL
Physical Volume(3) = {10};                                          //DRAIN
Physical Volume(4) = {9};                                           //SOURCE
Physical Volume(5) = {11,12,13,14,15,16,17,18,19};                  //GATE
Physical Volume(6) = {20};                                          //OXIDE FILM
Physical Volume(7) = {21};                                          //SUBSTRATE


Coherence;
```