WIDE-SUPPLY INTEGRATION CMOS DC-DC CONVERTER FOR ENERGY HARVESTING APPLICATIONS

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AUGUST 2023

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By

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ABSTRACT

WIDE-SUPPLY INTEGRATION CMOS DC-DC CONVERTER FOR ENERGY HARSVESTING APPLICATIONS

Nur Allisa Sabrina

This study describes the design, analysis, and simulation of a Wide-Supply Integrated CMOS DC-DC Converter in the goal of creating energy-efficient technology for energy harvesting applications. Cross couple charge pump is utilized in this design to to meet the special requirements of energy harvesting systems by effectively capturing and converting captured energy into suitable voltage levels. Furthermore, this paper proposed DC-DC converter that improve the existence charge pump like Dickson Charge Pump (DCP) by adding Pulse Frequency Modulation (PFM) to enhance the performance and generate a high voltage output with a variety of supply voltages. By accomplishing its goals, this study advances energy-efficient technologies and has great potential for integrated circuit systems and a variety of energy harvesting projects.

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LIST OF ABBREVIATIONS

SoCs	System on Chips
IoT	Internet-of-Things
WSNs	Wireless Sensor Networks
EH	Energy Harvesting
PV	Photovoltaic
DC	Direct Current
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
SC	Switching Capacitor
L	Inductor
DCP	Dickson Charge Pump
CP`	Charge Pump
LDO	Linear Dropout
C_P	Pumping Capacitance
C_L	Load Capacitor
V_{DD}	Power Supply
I_L	Load Current
PFM	Pulse Frequency Modulation
NMOS	N-type Metal-Oxide-Semiconductor
PMOS	P-type Metal-Oxide-Semiconductor
CMOS	Complementary Metal-Oxide-Semiconductor
IC	Integrated Circuit
PCB	Printed Circuit Board
CTS	Charge Transfer Switch

LVCP	Low-Voltage Charge Pump
HVCP	High-Voltage Charge Pump
PCE	Power Conversion Efficiency
DBB	Dynamic Body Biasing
VCE	Voltage Conversion Efficiency
TEG	Thermaoelectric Generator
mV	mili Volt
u	micro
m	meter/mili
pF	pico Farad
MHz	Mega Hertz
dBmW	Decibels miliwatt
K	Kilo
VBC	Voltage Boost Converter
SD	Sub-Driver
MD	Main-Driver
VIN	Input Supply
mA	mili Ampere
Nm	nanometer
Vth	Treshold Voltage
Vdc	Direct Current Voltage
Vref	Reference Voltage

CHAPTER 1

INTRODUCTION

1.0 Introduction

As process technology progresses, portable devices become more and more popular. System on Chips (SoCs) with a smaller form factor, less energy consumption, a lower price, and lower conservation are becoming increasingly important for Internet-of-Things (IoT) systems. IoT is widely used because it can cooperate and exchange information without a lot of direct human interaction. It more closely resembles an extensive network of intelligent gadgets that can communicate with one another online. As an example, Wireless Sensor Networks (WSNs) are networks of small, self-powered gadgets called sensor nodes that collaborate to gather and send data from the environment. Due to their capacity to track and collect data from various physical, environmental, or industrial contexts, these networks have grown significantly in relevance and appeal. These sensor nodes are often employed in a variety of settings, including industrial automation, healthcare, and environmental monitoring. On the other hand, most of WSNs available today still rely on batteries to supply the required power for their functioning [1]. In addition to lowering power consumption, energy harvesting (EH) has been recommended as a potential alternative, particularly for IoT, to enhance lifelong, decrease maintenance, and cut costs. [2] [3]

Energy harvesters provide voltage by converting the available energy from outside sources into electrical energy. As an example, external sources of energy are electromagnetic, mechanical, thermal, and solar energy. Following that, this electrical energy is gathered, controlled, or transformed to meet the needs of the devices being powered or the energy storage system being charged. The harvester' output voltages, however, are insufficient to fully charge the battery for example, the output voltage of a single photovoltaic (PV) cell at its highest power point is around 0.5 to 0.6V, but the voltage required to perform charging is greater than 4V. Hence, it is important to use a power management circuit with voltage boost converter such as charge pump [4].

Charge pump circuits or also known as Charge Transfer Switch or DC-DC converter which are high-voltage generators that generate voltage above the typical supply voltage. The charge pump circuit has evolved into an important circuit technique in low supply-voltage systems, in addition to various conventional usage in memory design. Electrostatic aerators, analogue switches in switched-capacitor devices, and nonvolatile memory all require high voltage to work properly [5]. When a system requires more than one dc supply voltage, a switch-mode dc-dc converter, also known as a simple charge-pump circuit, is typically utilized. It is built with capacitors and switches. The switches in discrete designs are normally diodes, although IC variations can also employ MOSFETs. The two primary subcategories of DC-DC converters are buck converters and boost converters. Buck converters are used frequently in many SoCs to reduce the voltage supplied to them. Boost converters, on the

other hand, are used to enhance the input voltage. Several boost converter designs are described, including L-based [3], [6], cross-coupled switching capacitor (SC) [7], and Dickson charge pump (DCP). It is feasible to utilize both switching capacitor (SC) and linear dropout regulator (LDO) on one chip and have it work correctly. Nonetheless, for energy harvesting based systems, a cascade technique with an enhancement stage that raises voltage and a buck stage for controlling it is required. This cascade leads to a greater area and worse efficiency [6].

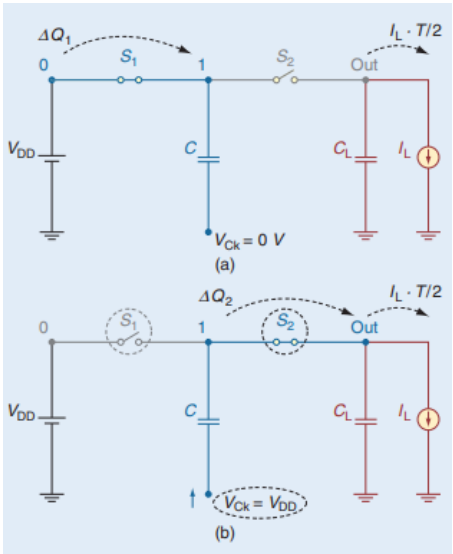

Figure 1. One Stage Charge Pump [1]; (a) first phase (b) second phase

An ideal charge pump as shown in figure 1 indicates that one stage charge pump which consists of two switches, pumping capacitance C_P, load capacitor C_L, power supply (V_{DD}) and load current (I_L) . The charge pump will be driven by two phase of clock that have same amplitude with the power supply V_{DD}.

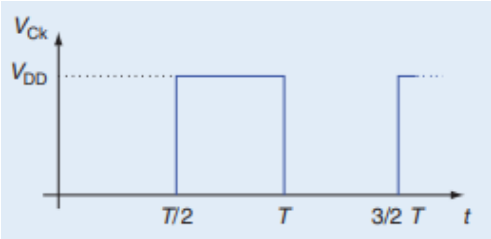

Figure 2. Clock signal, V_{CK} of the Charge Pump [1]

During phase 1 which from 0 to T/2 as shown in figure 2, S2 is open while S1 is close. Hence C_P is being charged as it connected to V_{DD}. Therefore, the V_{CK} is equal to V_{DD}. Then, during second phase which is T/2 to T, the switches change state, S1 is open and S2 is close. The clock signal has set to V_{DD}, hence the C_P will transfer charge to C_L and I_L which can cause the voltage across to C_L increase. Clock signal is an external signal that control the timing of the switching operations within the circuit. By transferring the charge from C_P to I_L, the output voltage will be increasing follow as equation 1 stated below [8].

$$V_{\text{Out}}|_{\text{Steady State}} = 2V_{\text{DD}} - \frac{I_L \cdot T}{C}. \qquad (1)$$

The number of steps in an ideal charge pump can effect the output voltage, as shown by the equation below, where N is the number of stages and VDD is the voltage from the supply, as shown in equation (2). The output voltage corresponds to the number of steps, as shown. As a result, as the number of stages expands. this affects the output voltage because it is directly linked to the supply voltage.

$$V_{OUT} = N * V_{DD} \quad (2)$$

However, there is a trade-off between the number of stages and other design factors including space , current usage, and power consumption. It's crucial to remember that the charge pump circuit's unique architecture might have an impact on the correlation between the number of stages and the output voltage. The Dickson Charge Pump, Bootstrap Charge Pump, Double Charge Pumps, Series-Parallel Charge Pumps, and Charge Pumps with Adaptive Number of Stages are a few examples of different topologies. Each has unique properties, benefits, and drawbacks.

In some application, there required different voltages for each component. Therefore, Pulse Frequency Modulation (PFM) is needed to adjust switching frequency of the charge pump based on the load demand in order to boost voltage regulation. This method can be applied to a wide range of applications to optimize energy consumption and improve overall efficiency in various electronic systems and devices. Basically PFM is used to regulate the frequency to match the output voltage same as desired value.

This study develops a wide-supply integrated CMOS employing the cross coupling DC-DC converter technology and pulse frequency modulation (PFM) to increase output voltage. However, the high performance NMOS and PMOS transistors utilized in DC-DC converters use a 130nm CMOS semiconductor manufacturing technology. The most recent technology in Cadence Software employed for simulation in this project is integrated circuits

(ICs) with feature sizes of about 130 nm.Cadence software is used to simulate the DC-DC converter and analyse the input and output voltage in order to achieve the project's aim, which is to increase the output voltage from low input voltage. PFM is employed to control the frequency in order to provide consistent output voltage with a wide variety of input voltages. In this case, the input voltage is tuned between 0.35V and 0.75V to produce an output value of about 1V

1. 1 **Problem Statement**

Since the inductance value is directly correlated with the number of turns, and more turns need more space, small PCB sizes are in great demand nowadays but are not suited for inductors since they take up a lot of board area. Besides that, numerous ICs nowadays need a variety of voltages as it contains multiple components with different voltage requirements. For example, in one IC contains analog and digital components which they have different operations. Analog components require higher supply voltage compare to digital components for a better performance. However, by taking account design constraints and power consumption, DC-DC converter with pulse frequency modulation can be utilized to regulate the output voltage and follow the supply voltage for each of the components. This approach can maintain the power efficiency and minimize additional external components. Moreover, Dickson Charge pump has some drawback in term of the voltage conversion. This is because the charge pump in Dickson method are directly connect to the supply voltage. Hence the the output can only double the input voltage. Since this project is for energy harvesting application which using low input supply and generate high voltage output. this method is not suitable. Additionally, Dickson CP features threshold losses and voltage drops. The voltage drop in Dickson CP is caused by a resistance that is present when the transistor is turned on, even if it is very tiny. However, it will become larger if there are additional stages. The threshold voltage is no different. This may reduce efficiency and have an impact on voltage output. Furthermore, DCP function in an open loop manner without feedback to precisely tune the output voltage.

Compared to more complex topologies with feedback loops, DCP techniques may lead to less accurate voltage control.

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1.3 OBJECTIVES

i. Design a DC-DC converter using suitable topology for energy harvesting application.

ii. Investigate the key issues in the existing charge pump and propose solutions.

iii. Develop a wide-supply integrated CMOS using DC-DC converter.

iv. Simulate and verify the operation of the DC-DC converter.

CHAPTER 2

LITERATURE REVIEW

2.1 Charge Pump Topology

Dickson invented the Dickson topology [7] in 1976. As illustrated below, it consists of NMOS transistors, capacitors, two clock phases, a supply voltage, and an output voltage. But at each level, the NMOS turns on in turn. The threshold voltage decreases in accordance with each level. Moreover, the bulk terminals of the NMOS are often connected to the ground by the Dickson charge pump. The more stages a Dickson charge pump has, the greater body effect-induced threshold voltage drop is produced. In the end, this resulted in a loss in pumping efficiency [5]-[3],[9]-[13].

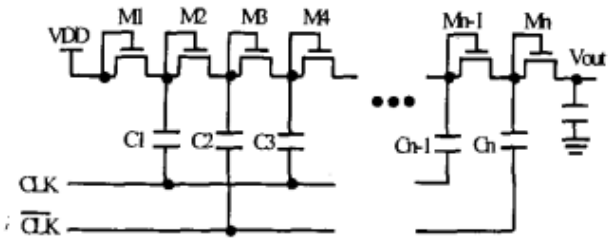


Figure 3 Dickson Charge Pump schematic design [7]

Thus, a charge transfer switch (CTS) and floating well can be utilized to reduce the PMOS gate voltage and improve the transmission voltage in the diode-connecting channel in order to prevent threshold voltage reductions and body effects [5] [9]. The floating well may keep the voltage between the source and the body constant. On the other hand, when the two pumping branches in

the cross coupled CP method work in simultaneously the diode loss across stages is minimized, and the output voltage ripple is reduced. Similarly, when the number of stages rises in a DCP design, dynamic body biasing as well as other approaches may be used to assure dependability [12]. As seen in the cross coupled CTS circuit below, the inverter's gate is connected to the preceding pumping capacitance on a similar branch. The NMOS transistor's source terminal is also connected to the pumping capacitance of a prior stage on a separate branch. There is no need to wait for the capacitance of the subsequent stage to have a higher voltage in order to regulate the CTS PMOS gate at the moment of transition when the variance among VA2 and VA3 exceeds VTP since AN3 and AP3 are close in time. Capacitance charging time may be reduced as a result [9].

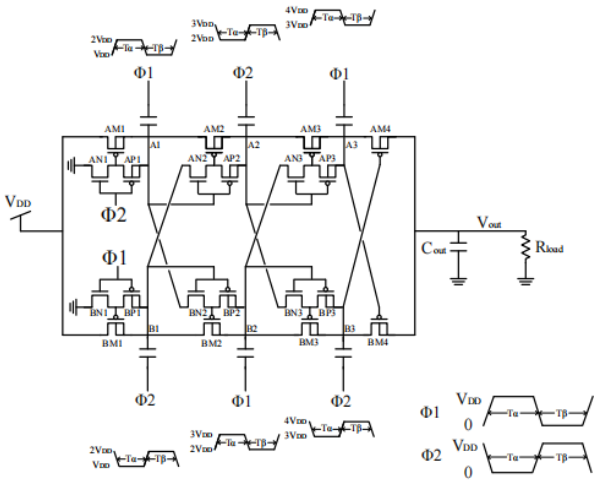
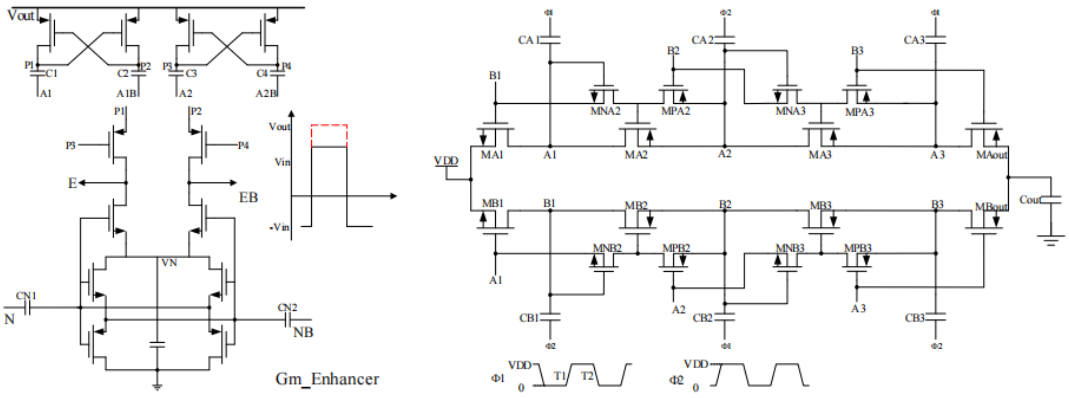


Figure 4. Cross Coupled CTS circuit [9]

Nevertheless, in low voltage charge pump (LVCP), conductance enhancement technology may be used to activate the CTS and threshold reduction technology to raise the power conversion efficiency (PCE). By

combining DBB and Gm enhancement methods, it may be possible to push the MOSFET threshold voltage over the low input voltage [2]. The DC-DC converter circuit has evolved into a crucial circuit approach in low-supply-voltage systems, in addition to several conventional uses in storage design. Electrostatic aerators, analogue switches in switched-capacitor devices, and nonvolatile memory all require high voltage to function. A Low Input Voltage CP for EH was created by Yi Li, Sheng Ming, and Quanzhen Duan. It consists of two parts: startup, which employs a Low Input Voltage Charge Pump (LVCP), and boost, which uses a High Input Voltage Charge Pump (HVCP). According to figure 5(a) below, the LVCP in this architecture is made up of two CP, a clock generator and a Gm Enhancer.Moreover, Dynamic Body Bias (DBB) was implemented to boost Power Conversion Efficiency (PCE). A complementary branch system is employed in the HVCP circuit, as shown in figure 5(b), which helps to eliminate output voltage ripples. This system is referring to the CTS charge pump technology.



(a) LVCP circuit (b) HVCP circuit

Figure 5 . Detailed Schematic of LVCP and HVCP circuit [2]

Kuo-Hsing Cheng, Chung-Yu Chang, and Chia-Hung Wei proposed a CMOS CP for sub-2.0V operation utilizing floating well and CTS, both of which successfully reduced the PMOS gate voltage while improving the transmitted voltage in the diode-connecting channel. These methods can help to lessen both the body effect and the threshold voltage drop [5]. As a result, the circuit below may provide a similar amount of current flowing out and capacitance while increasing the voltage.

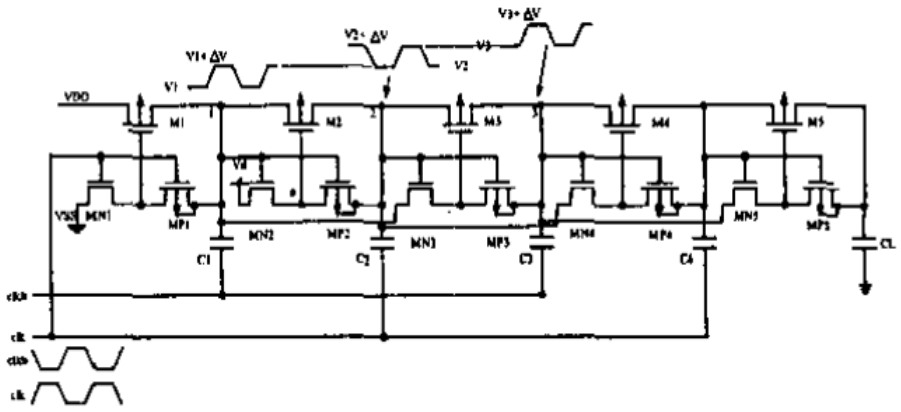


Figure 6 CMOS Charge Pump in sub-2.0V operation [5]

According to the Andrea Ballo, Alfio, and Gaetani publications on evaluating of CP topology for Power Management of IoT Nodes [10], the application, CMOS technology, and design requirements determine the choice of a certain topology among those given in the preceding section. This study demonstrates that cross-coupled topology offers the lowest supply voltage while also having the lowest voltage conversion efficiency (VCE). Moreover, because they enable a lower input voltage, body and gate control systems may be a good alternative for low-supply-voltage systems such as TEG energy recovery. Clock-boosted flash memory could be beneficial if the primary

function of internal DC-DC converters is to create a variety of voltage levels with quick settling periods. According to the comparison in this research, the boostrap and cross coupled charge pump topologies are the most commonly utilized to create high voltage from low input voltage. If low-threshold devices are available, they can be used for this purpose; however, because of their large leakage current, it is vital to consider the possible power efficiency loss. The usage of common threshold devices in the subthreshold region, on the other hand, results in a diminished capacity to transmit charge. Higher efficiency can be obtained in this situation by taking advantage of a wide area of active devices.

Ref.	[2]	[3]	[12]	[13]	[14]	[15]	[17]	[18]	[20]	[58] [a]		[23]
Topology	Cross-coupled/ composite	Cross-coupled	Bootstrap	Dickson-with DGB	Cross-coupled with BGB	Cross-coupled DBB	Bootstrap	Bootstrap	Bootstrap	Adiabatic		Adaptive
No. Of Stages	6 pararallel 24	3	10	4	6	3	3	5	1	3	7	10
Aux. Circuit	Start-up circuit	Clock booster 3x	Clock booster 2x	Dynamic G control	Backward G Biasing	Dynamic B control	-	Split-merge four-branches	-	Low-threshold diode in every CTS		-
Technology (nm)	130	65	65	65	180	130	130	130	180	130		65
Min. Supply (mV)	70	150	100	550	320	150	270	500	390	125		120
Clock Frequency (MHz)	0.040	15.2	10	1.8	0.45	0.25	0.8	2.5	23	0.360		1
Total Pumping Cap. (pF)	46.08	22.5	1001	160	288	36,000 [b]	150	310	500	96	224	286
Load Cap. (pF)	10,000 [b]	30	100	400	50.7	10,000 [b]	500	800	4000 [b]	100		-
Load Current at Peak η (μA)	12	1.74	0.76	10	-	21	5	30	620	0.1		3.9
Max Output Power (μW)	15	1.5	6.6	4.7	-	10.5	7	75	620	0.061	0.035	3
Peak VCE (%)	50	80	76	96	89	86	65	93	93	70	80	58
Peak η (%)	58	38.8	33	66	-	34 [c]	58	78.6 [c]	76	59	62	38.8
Area (mm^2)	0.6	0.032	1.32	0.17	0.14 mm^2	0.066 [b]	0.42	0.98	0.48	0.15	0.1	0.78

Figure 7. Comparison of different charge pumps. [10]

A innovative CMOS CP module with an integrated two-phase clock generator has been created for energy-harvesting step-up converters by Huan Peng, Nghia Tang, Youngoo, and Deukhyoun [13] as shown in figure 8. The goal of the charge pump is composed of two branches of charge transfer switches that include both NMOS and PMOS. These devices help in the transfer of charge from one capacitor to another. Using NMOS and PMOS devices enhances charge flow control and reduces the potential of reverse charge sharing. When combined with a corrected two-branch structure, it may

entirely switch on and off the CTS with a low voltage supply. Backward control boosts internal voltages to increase clock amplitude, significantly reducing switching loss and the reverse charge-sharing event. This system can run on a small power supply by using sub threshold operation and a body bias approach. However, this purposed design is made up of six stages, each having a 24 pF pumping capacitor. With a 320 mV input, the charge pump's observed output voltage may grow from 0 to 2.04 V in 0.1 milliseconds.

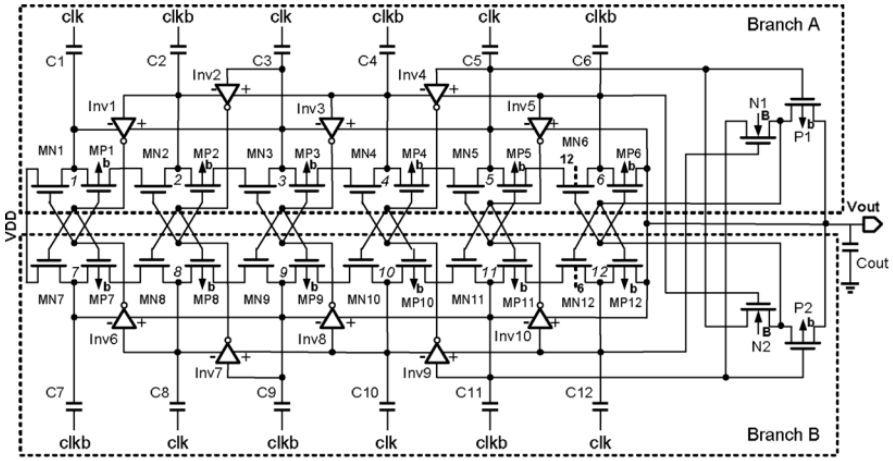


Figure 8 CP With Body Bias and Backward Control Circuit [13]

Kwangrok You, Hyungchul Kim, Minsun Kin, and Youngoo Yang presented in their work 900MHz CMOS RF-to-DC Converter Energy Harvesting with a Cross-Coupled Charge Pump, which involves of a cross coupled rectifier and a cross coupled charge pump. For their demonstrated design in this study, they employed a 0.13um CMOS technology. The charge pump may operate on an independent clock with a operating frequency of 25 MHz and a switch capacitor of 4 pF. Under these conditions, the charge pump shown a great performance of around 74% with RF power input of -6 dBm, input frequency of 900 MHz, load of 100K, and output voltage of 2.05 V. The

cross coupled circuit arrangement reduces the voltage drop and reverse leakage current of the transistor [14].

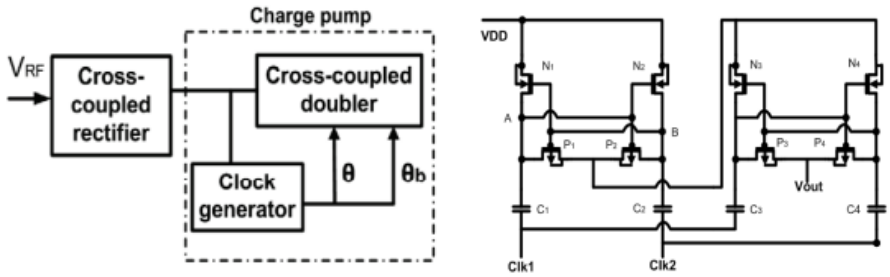


Figure 9 (a)Block Diagram of RF to DC Converter (b) Cross coupled doubler circuit [14]

Yuto Tsuji, Tetsuya Hirose, and Toshihiro Ozaki describe a voltage boost converter (VBC) with minimal leakage drive for low-voltage energy harvesting, which includes three tiers of charge pumps with minimal leakage drivers, a ring oscillator, and a four-phase clock oscillator. A cross coupling charge pump design is used in the charge pump circuit. The driver involves of four sub-driver (SD) and main-driver (MD) pairs, each of which is assigned to producing four switching voltages, VGN1, VGN2, VGP1 and VGP2. The results of this study produced an output voltage that was four times larger than the input voltage VIN. The low-leakage driver controls the CPs so that they run with a small leakage current. The load current is unaffected by the amplitude of the control signal 2VIN. The proposed VBC transformed 0.6 V input to 2.38 V output and 0.1 V input to 0.362 V output when the load current was zero, according to simulation results. For a 0.6V input supply and a 1mA current draw, the highest efficiency was 70.3% [16].

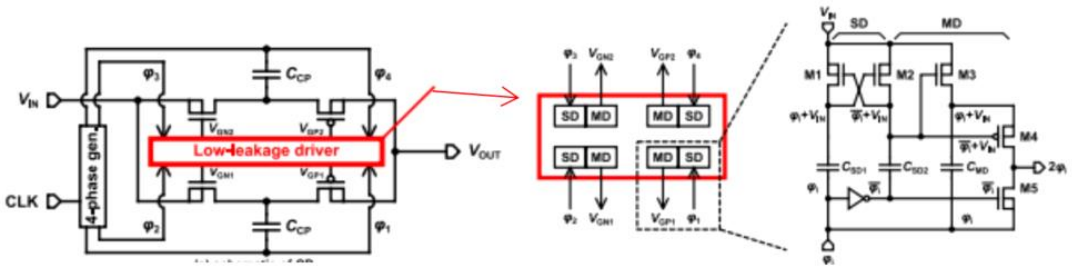
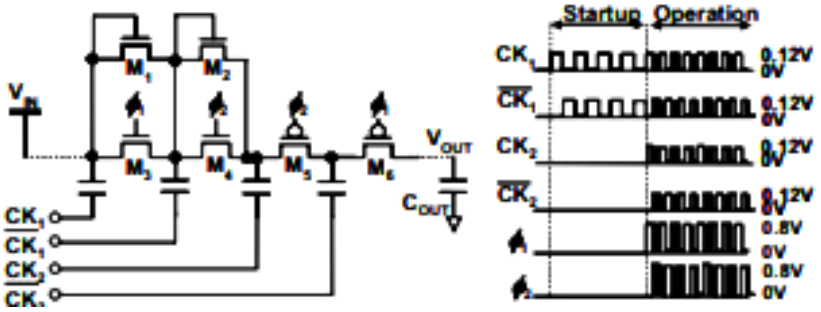
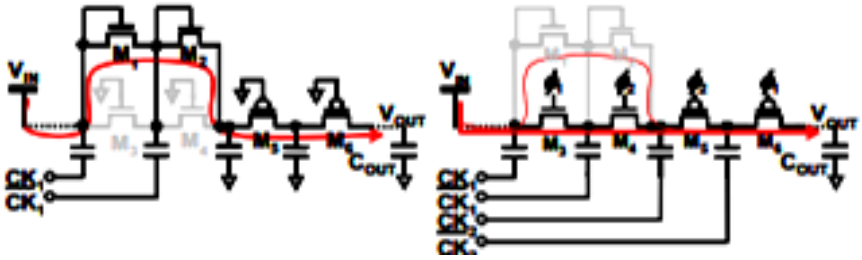


Figure 10. Schematic of the proposed Charge Pump [16]

Po-Hung Chen, Koichi Ishida, and Xin Zhang developed a 120mV Input, Fully Integrated Dual-Mode Charge Pump in 65nm CMOS for a Thermoelectric Energy Harvester with an output voltage conversion efficiency of 38.8%. The proposed design can be observed in the figure below. NMOS transistors with the model numbers M3 and M4 make up the first half stages of the CMOS charge pump, while PMOS transistors with the model numbers M5 and M6 make up the back half stages. This method indicates that each transistor achieves the entire overdrive voltage when the gate terminals are controlled by high voltage clocks. Despite the fact that transistors M1 and M2 continue to operate, the majority of current flows via the CMOS switches M3 and M4 because their on-resistance is substantially lower than that of the diode-connected MOSFETs M1 and M2. As the result, the CMOS charge pump increases the performance of conversion, whereas the Dickson charge pump provides a low voltage start. With a 320 mV input, the suggested charge pump's observed output voltage may rise from zero voltage to 2.04 V in 0.1 milliseconds [18].



(a) Schematic of whole Charge Pump *(b) Operations sequences of the proposed dual-model CP*



(c) Startup mode *(d) Operation mode*

Figure 11. Proposed Design in fully integrated dual-mode charge pump [18]

According to A. Ballo, A. D. Grasso, G. Palumbo and G. Giustolisi paper on Optimized Charge Pump with Clock Booster for Reduce Rise Time or Silicon Area, they have enhance Dickson Charge Pump (DCP) topology by adding clock booster in their proposed design as shown in figure 12. In contrasts to a standard Dickson charge pump, this design allows for an improvement in rise time while maintaining the same area occupancy or, whereas, an area decreased for a similar rise time. According to their simulation results, the suggested approach is helpful when the number of stages is big enough and the value of the load capacitor is smaller than the whole pumping capacitance. Furthermore, the rising time and size savings can be

higher as 60% at the tradeoff of power consumption and minor circuit complexity due to the need of a clock booster [19].

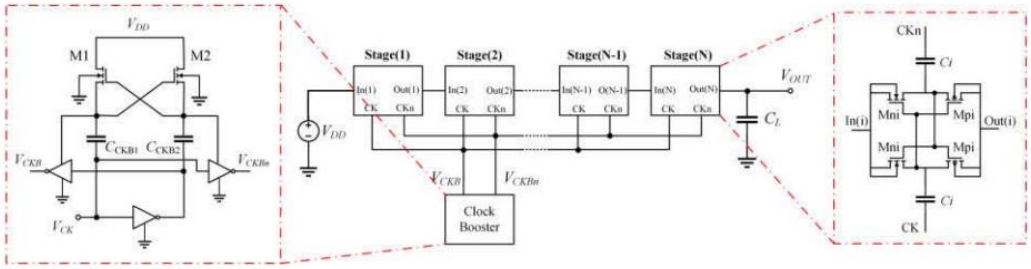


Figure 12. Schematic of the Charge Pump with Clock Booster [19]

David Matousek, Jiri Hospodka and Ondrej Subrt have done two simulations to determine the size of and their impacts to efficiency and output voltage as describes in figure 13. The cell is made up of five transistors M1, M2, M3, M4, M5 and a pumping capacitor. This block is controlled by clock signals. Transistors M1, M3, M5 are closed during the first phase when CLK1 and CLK2 is equal to VDD. As a result, the transfer capacitor CT is biased to the supply voltage VDD. While transistors M2 and M4 are closed during the second phase CLK1 and CLK2 is equal to GND. As a result, transistor M2 keep bias transistor M5 unconnected. Transistor M4 links the transfer capacitor CT between the cell's input and output. As a result, the input voltage is raised by the voltage of the transfer capacitor from the the biased phase. All transistors are opened in the final phase where the CLK1 is equal to GND while CLK2 is equal to VDD. At the beginning of the simulations, the efficiency rises with rising load current and falling clock frequency. Conversely, when the load current decreases and the clock frequency rises, the output voltage rises. The effectiveness of the provided charge pump's optimization depends on the results of the second phase of the simulations.

With MOSFETs of the original sizes and a load of 1 M, the efficiency and output voltage are, respectively, 33.43% and 4.008 V. The efficiency may be improved by roughly 10% using the transistor sizing approach [20].

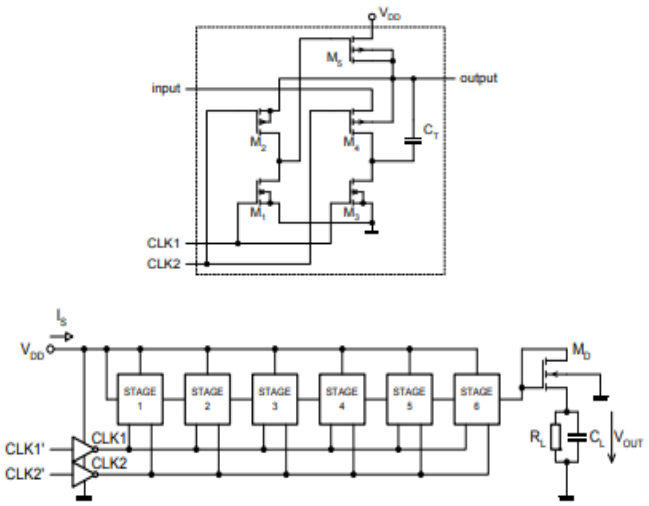


Figure 13 (a) One stage of Charge Pump (b) Schematic Diagram of Proposed Design [20]

A High-Performance Charge Pump Topology for Very Low Voltage Applications was proposed by A.Ballo, A.D. Grasso, and G. Palumbo [21]. They created and tested a four-stage and a six-stage Charge Pump to demonstrate the advantages of using STMicroelectronis' 65nm triple well CMOS technology. Each CTS is made up of an NMOS and a PMOS transistor linked in series with each other, as seen in the red outlined box. Every transistor connects its bulk terminal to the terminal designating the source during the conduction phase. Although less effectively owing to body impact, it operates in a similar manner as biasing the NMOS bulk to ground. The NMOS gate voltage is connected to node V3, whereas the PMOS gate voltage is driven by voltage V1. Except for the final stage, where a different MOSFET with a lower capacitance MB and CB is used for booting the gate voltage of the

NMOS in an effort to remain the same operation as the other CTSs, and the first stage, in which the gate voltage of the PMOS is linked to the negated clock signal, this configuration continues to be repeated through the charge pump. Despite a little drop in VCE at voltages around the MOS threshold voltage owing to reverse losses, the proposed Charge Pumps have an extensive driving range, energy efficiency, and performance. It also performs effectively at an extremely low input voltage. Hence, the proposed solution seems to be especially well suited for uses needing very low input voltages.

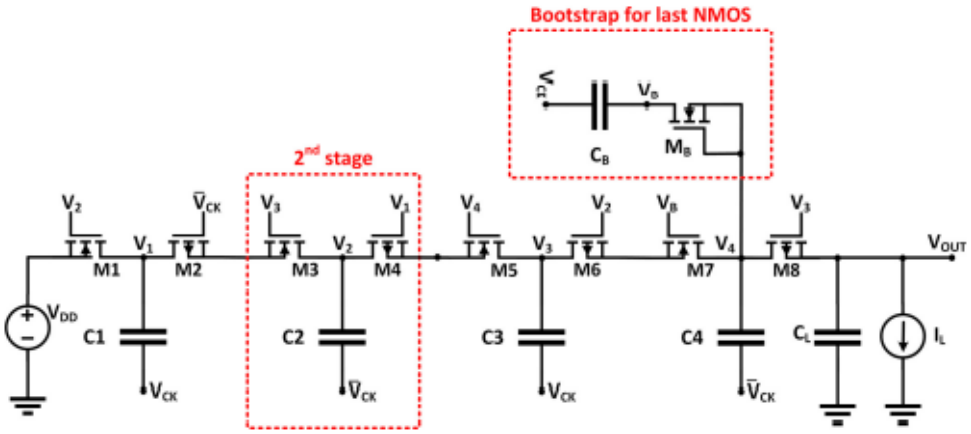


Figure 14. Schematic the proposed Charge Pump [21]

Kishore Kumar, Gabriel Chong, Harikrishan and Yazed has created a review paper on Low-Voltage Capacitive-Based Step-Up DC-DC Converters for RF Energy Harvesting System. All of the charge-pump approaches as shown in figure 15 in this paper are found to be appropriate for RFEH systems, where two or more of these techniques can be used to increase Power Conversion Effeciency (PCE) and startup performance across the board. Maximizing the PCE of charge pump is the primary design goal. The Rload, N-stage, and Cpump are the primary factors that have an impact on PCE. To achieve the intended specification, there must be trade-offs between variables

like start-up time, Voutcp, and area. For example, increasing the size of a charge-pump transistor increases gate capacitance, which impacts switch loss. Furthermore, decreasing the size of the transistor improves conduction loss, reducing switching losses, which results in the overall PCE of the RFEH system. This leads to an optimal transistor size for minimal losses and the largest PCE of the charge pump, resulting in a higher power efficiency [22].

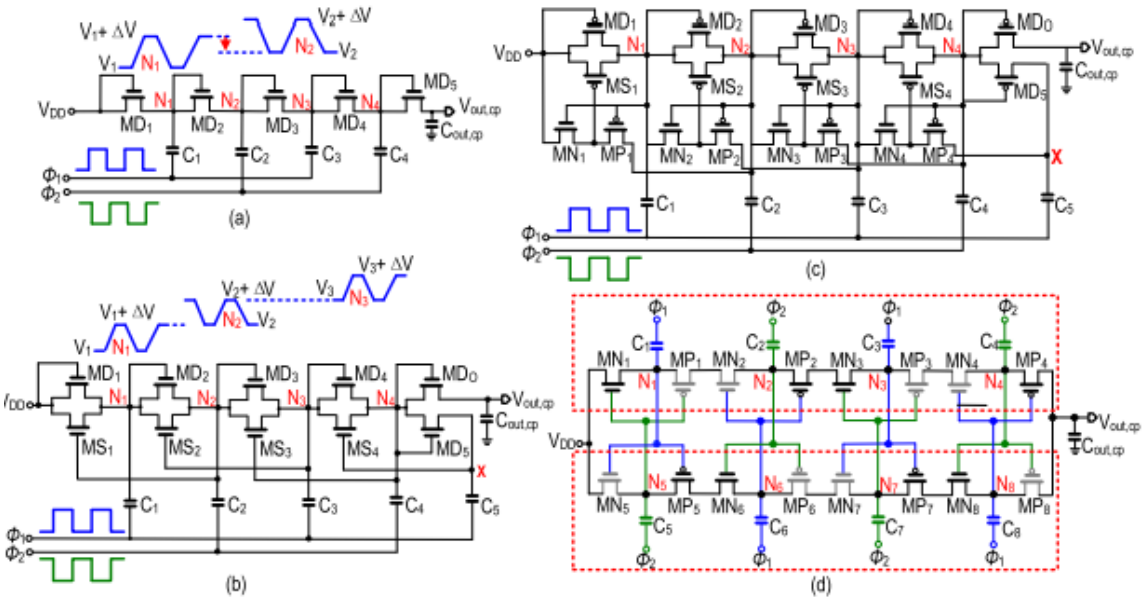


Figure 15. Charge Pump Method (a) Conventional. (b) Charge transfer switch:Type-I (c) Charge transfer switch: Type-II . (d) Two-branch latch charge-pump

Moreover, in a study paper A Charge Pump Based Power Management Unit With 66%-Efficiency in 65 nm CMOS by Abdulqader Mahmoud, Mohammad Alhawari, Baker Mohammad, Hani Saleh and Mohammed Ismail has proposed a cross coupled charge pump that has improvise from Dickson Charge Pump to increase and control a low input voltage as shown in in figure 10. In order to dramatically minimize the losses seen in typical DCP switches, an alternative switching mechanism is described. Silicon measurement results in 65 nm CMOS technology demonstrate a maximum efficiency of 66% at

input voltage of 0.7 V and output power of 27W using a four-stage charge pump. The system can operate at a maximum operating frequency of 1.8MHz and is capable of handling load currents ranging from 0.1 A to 34 A. The proposed architecture may be employed in energy harvesting applications and supports an input voltage range of 0.55 to 0.7 V [26].

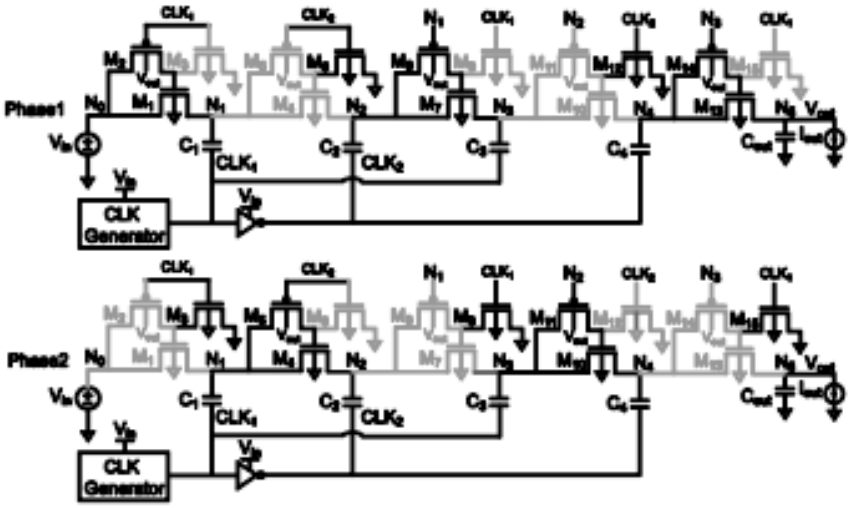


Figure 16. Cross coupled charge pump [26]

Table 1 below shows the different of CMOS technology, the supply voltage, generated voltage, the value of the pumping capacitor and load capacitor as well as the frequency used in 9 papers that used CP to produce high voltage from the lower supply voltage. Based on the comparison table, A Charge Pump Based Power Management Unit with 66% Efficiecny in 65nm CMOS by Abdulqader Mahmoud, Mohammad Alhawari, Baker Mohammad, Hani Saleh and Mohammed Ismail has a great charge pump as it can pump up to 3V with lowest supply voltage in between 0.55V to 0.7V which can be used in energy harvesting application. This paper is used cross coupled topology to boost up the output voltage with bigger load capacitor which is 400pF.

Table 1 : Comparison of existing papers

	[5]	[3]	[9]	[11]	[13]	[16]	[18]	[21]	[26]
CMOS tech	**250nm**	**65nm**	**180nm**	**350nm**	**180nm**	**65nm**	**65nm**	**65nm**	**65nm**
Supply Voltage (V)	**<2**	**0.55-0.7**	**1-1.2**	**0.9-2**	**0.32-0.44**	**0.1-0.6**	**0.12**	**0.4**	**0.55-0.7**
Output Voltage (V)	**8.2 @Vin = 0.9**	**2 @Vin =0.6**	**3.58 @Vin=1.2**	**~3 @Vin=0.9**	**~2 @Vin = 0.32**	**2.38 @Vin= 0.6**	**0.77**	**~1**	**1.1-3.4**
Pumping Capacitor (F)	**10p**	**40p**	**20p**	**3p**	**24p**	**50p**	**28.6p**	**20p**	**40p**
Load Cap (F)	**20p**		**10p**		**50.7**	**100p**		**160p**	**400p**
Frequency (MHz)	**50**	**0.5-1.8**	**10**	**50**	**0.45**		**1**	**25**	**0.5-1.8**

2.2 Pulse Frequency Modulation (PFM)

Based on the An Accurate, Low-Voltage, CMOS Switching Power Supply with Adaptive On-Time Pulse-Frequency Modulation (PFM) Control by Biranchinath Sahu and Gabriel, the proposed design is using PFM buck as shown in figure 17 which to step down the DC-DC converter with on-time scheme that generates a 27mV output ripple voltage from 1.4V to 4.2V input supply. Although the purpose of the circuit is to step down the voltage, however, the purpose of PFM in this proposed design is same as in this project which is to controls the low peak of the output ripple and sets the high peak. On the other hands, when the feedback sense voltage, which is obtained from the output voltage using a feedback resistor divider, falls below the reference value, the output of the comparator switches from low to high. This occurrence causes the complementary output of the SR latch to transition from high to low accordingly, therefore turning on the power PMOS transistor, causing the output ripple to rise as shown in figure 18.

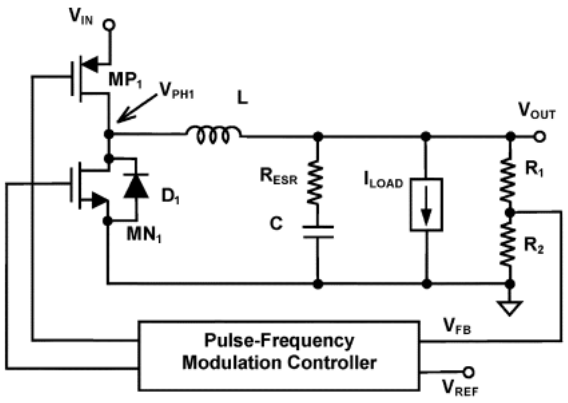


Figure 17. Schematic of a synchronous buck converter with PFM control [23].

The range of input supply is equivalent with battery compatible range. With minimal circuit complexity added, this design may achieve 2% to 10% greater power efficiency than conventional fixed on time design, which is crucial under light-loading circumstances when idle current is a key factor in determining efficiency and battery-life performance. Hence, the result in this proposed design, the output voltage dropped to their reference voltage which set to 0.5V when they supplied the input voltage from 1.4V to 4.2V [23].

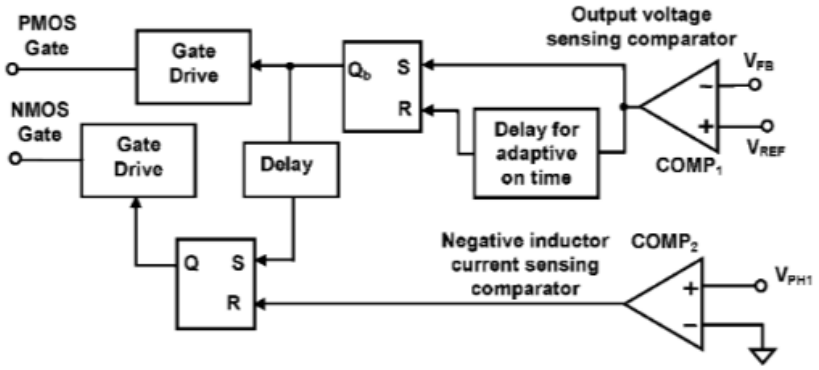


Figure 18. Adaptive on-time PFM controller circuit [23]

The paper A High-Voltage Generation Charge-Pump IC with Input Voltage Modulated Regulation for Neural Implant Devices by Alfian Abdi, Hyung Seok Kim, and Hyok-Kyu Cha details an intensive voltage development charge pump integrated circuit IC with an unique control mechanism for brain stimulation purposes. An input voltage modulated regulation with a low drop-out regulator at the feedback path's input is utilized instead of the typically used pulse frequency modulation technique with a changing clock frequency to sustain the charge pump voltage output with varied current load ranging from 10 A to 1 mA.

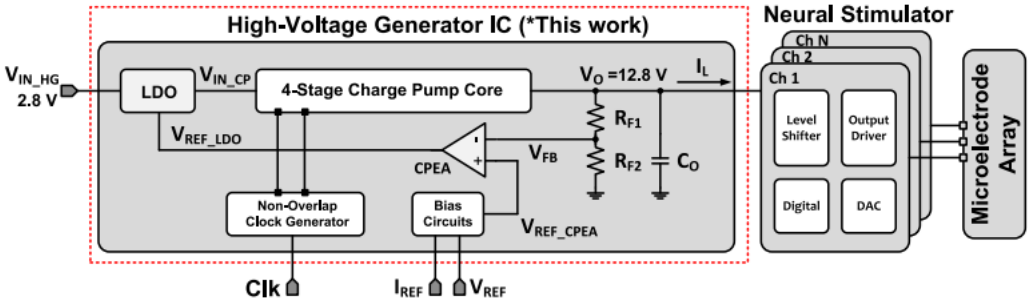


Figure 19 Architecture of the proposed high voltage generator IC [25]

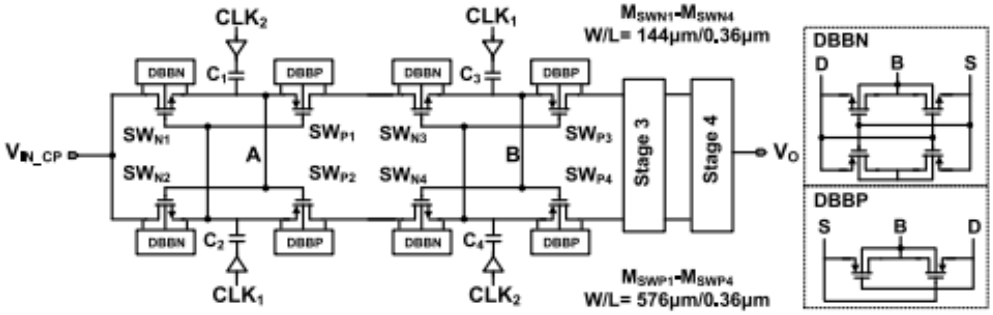


Figure 20. Proposed Charge Pump [25]

Based in the proposed design, the first two phases on the left demonstrate how the charge pump core works. CLK1 is high when CLK2 is high. Node A in the first stage will be high at this moment, whereas node B in the second stage will be low. SWN2, SWP1, SWN3, and SWP4 will be turned on, while SWN1, SWP2, SWN4, and SWP3 will be turned off. The input will charge the pumping capacitor C2, while the charge in capacitor C1 will discharge to charge capacitor C3. CLK2 is low during the following clock phase, whereas CLK1 is up. Node A is currently low whereas node B is high. A capacitor-less low-dropout (LDO) design is used because its output voltage can be changed faster than a capacitor of low-dropout (LDO) configuration. It is placed at the input of the charge pump. This is necessary to ensure that the

entire HV generating circuit works properly during load transients. The main problem in the LDO design is stability at low load and loop gain. An error amplifier (EA), a buffer, a limiter, a power transistor (MP), and feedback resistors RL1 and RL2 comprise the LDO as describe in figure 21. It also adjusts the gate voltage of the MP to regulate its voltage drop through the limiter circuit. The limiter circuit is implemented with a comparator and analog multiplexers to limit the current through MP, particularly when the charge pump starts up to charge the pumping capacitors. [25]

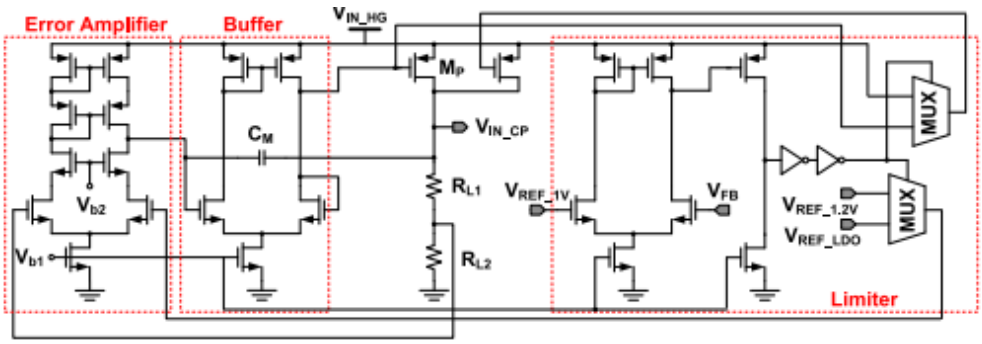


Figure 21 LDO regulator [25]

Charge Pump Based Power Management Unit with 66% Efficiecny in 65nm CMOS by Abdulqader Mahmoud, Mohammad Alhawari, Baker Mohammad, Hani Saleh and Mohammed Ismail described in this study uses an improved stage-switch Dickson charge pump (DCP) to boost and control a low input voltage. In order to dramatically minimize the losses seen in typical DCP switches, an alternative switching mechanism is described. The design proposed uses frequency and stage modulation as shown in figure 22.

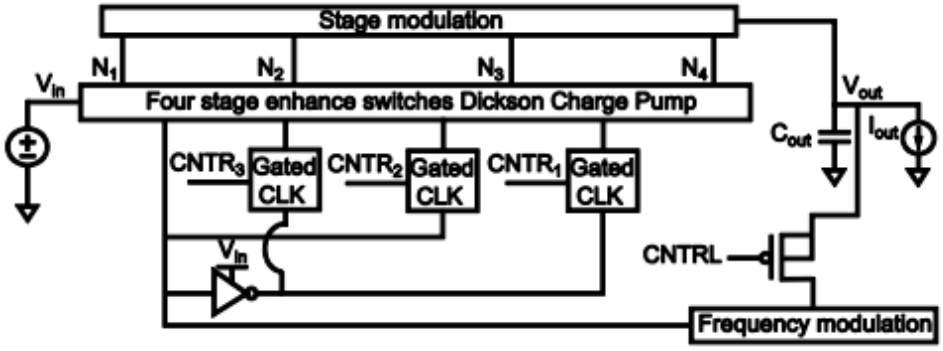


Figure 22. Charge Pump with Power Management Unit

Based on this paper, cross coupled charge pump is being utilized to boost up the output voltage. It consists of load capacitor, four stages of charge pump, clock generator from the PFM, input and output voltages as shown in figure 23. The input voltage charges C1 during phase 1. C2 also charges C3, and C4 charges Cout. Cout finally drives the load. C1 charges C2, and C3 charges C4 in phase 2. The load continues to consume power from Cout. CLK1 is used to operate the gates of M2 and M3. To turn off M8,11,14, the gate control is obtained from the previous step. Using M7 as an example, in phase 2, M9 sends 0 to M7's gate. Furthermore, VsM8 = 1.2V and VgM8 = 1.2V. As a consequence, VgsM8 = 0 V, and M8 is turned off. During phase 1, however, VsM8 = 1.8V and VgM8 = 0.6V. So VgsM8 = 1.2 V, and M8 is turned on. As a result, M7 operates as a diode-connected transistor, with the transistor's drain and gate terminals connected. This configuration acts like a diode, allowing electricity to flow in one direction while blocking it in the other.

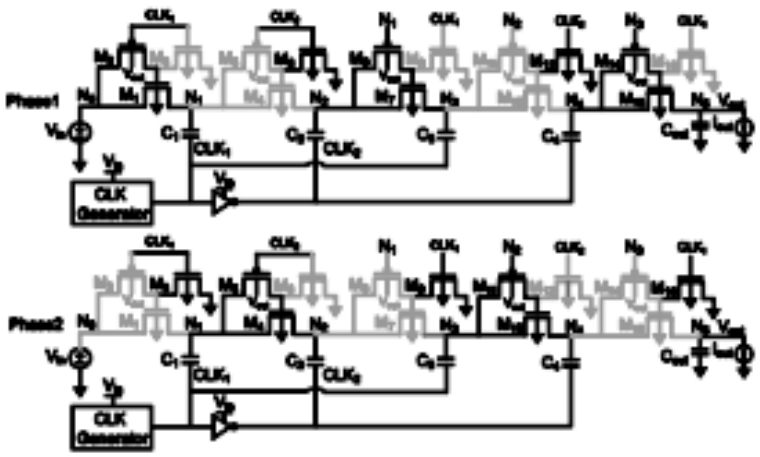


Figure 23. Flow of the Charge Pump [26]

The frequency modulation tunes the voltage level and controls the output voltage based on a predetermined reference voltage, while the stage modulation offers various gain levels. In this paper, they are using pulse frequency modulation that consists of ring oscillator, level shifter and comparator, 2:1 muiltplexers and nand gate as shown in figure 24.

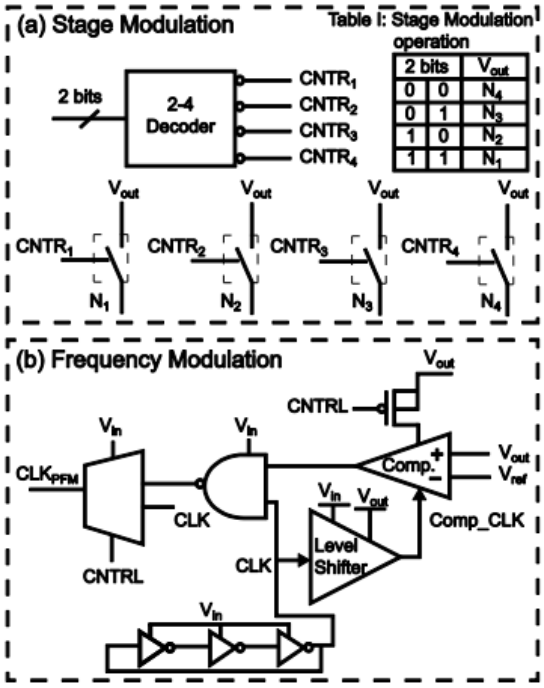


Figure 24 Stage and Frequency Modulation [26]

Stage modulation is a method that uses an active low decoder which the input in selected by external digital bits and switches to link each stage to the output. The CNTRL signal is used by the multiplexer to decide whether the ring oscillator for without regulation or output of the NAND if need regulation as sources of clock for the charge pump [26]. This paper has same configuration as in A Gain-Controlled, Low-Leakage Dickson Charge Pump for Energy Harvesting Applications studied by same authors. [28]

CHAPTER 3

METHODOLOGY

3.1 Flowchart

Figure 25 illustrate the flow chart to develop a wide supply Integration CMOS DC-DC converter for energy harvesting application. Cadence Virtuoso software has been used throughout this project for simulations and schematic design.

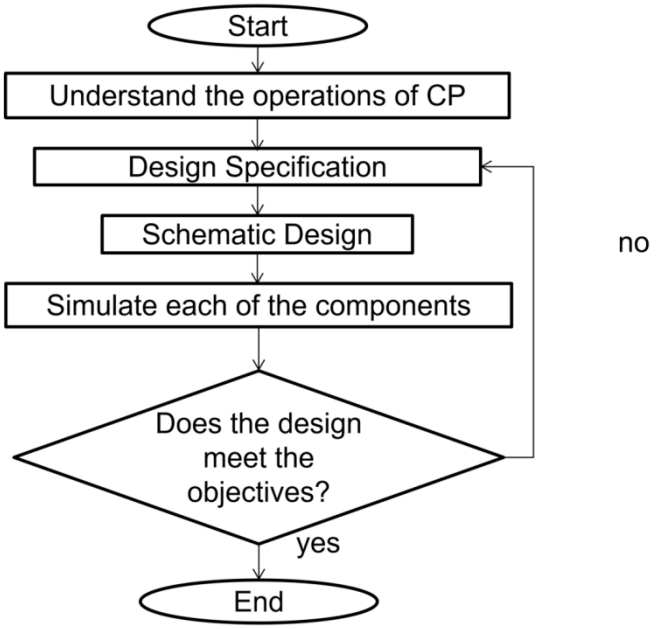


Figure 25. Flow Chart of Wide Supply Integration CMOS DC-DC Converter for Energy Harvesting Applications

First step before start this project is to understand the basic charge pump and the existence charge pump for example Dickson Charge Pump. Hence, create a schematic design for Dickson Charge Pump to understand the principle of DC-DC converter where the output voltage is double from the input voltage. Furthermore, by testing the basic operations of charge pump, can

understand more what parameters that will effect the output voltage. For example, by increasing the stage of the charge pump can increase the output voltage. However, the threshold voltage will be increases for this case.

Next is design specification where to determine which topology of charge pump will be used to generate a stable output voltage which approximately 1V . In this project, cross couple charge pump is chosen to boost up output voltage as it has high efficiency as the voltage drop is reducing during charge transfer switches which can lessen the power loss as well as reducing the switching losses during in and off states. Besides that, cross couple can enhance stability as this design can minimize the reverse leakage currents. This effect can cause inefficiencies and affect the stability of the voltage boost process.

Once cross couple charge pump is decided to use in this project, schematic design need to be done to determine the specification for the design such as the size of the transistors, the number of stages for the charge pump, the value of pumping capacitors and the frequency will be used in this project. Next, in order to achieve our objectives which is to generate a stable output from varies supply voltage, Pulse Frequency Modulation is needed to regulate the frequency and adjust the output voltage accordingly to approximately 1V.

Moreover, simulations are required to determine each of the components used are behaviour correctly as expected before integrate with the whole design. For example, creating a test bench for charge pump to simulate and obtain result to check whether the circuit able to boost up the supply voltage or not. Not just that, component used inside PFM also need to be simulated such as inverter, nand gate and latched comparator to ensure the result as same as expected.

Lastly, once the PFM and Charge Pump has been integrated and simulated, need to check whether the output voltage is able to sustain around 1V even though the supply voltage change from 0.35 to 0.75V. If the result are not as expected, need to check the design and adjust until can achieve our objectives,

Using 180nm CMOS technology, Dickson charge pump is used to understand the basic working of charge pump by simulating it using Cadence Virtuoso software. The five-stage charge pump shown below uses high-performance PMOS and a metal-insulator-metal capacitor. Cadence software will be used to analyze the design for DC characteristics. The goal of checking the DC characteristic is to verify that the circuit is receiving current and voltage. As shown in the given figure, each net has a voltage of 500 mV, 400 mV, 300 mV, 200 mV, and 100 mV, respectively, with a supply voltage of 500 mV.

3.2 Testing Basic Charge Pump (DCP)

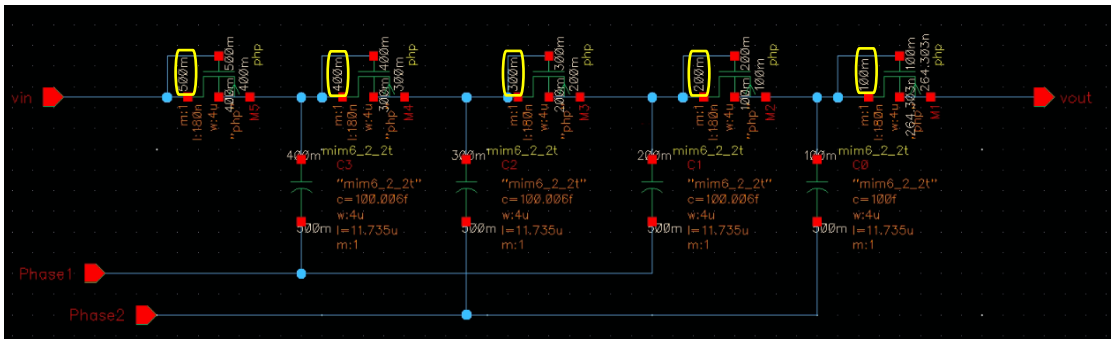


Figure 26. Dickson Charge Pump circuit

Next, Vdc is sweep for 0-1V, as a result, when the Vdc is high, the current at the Vin will be high as well. However, the output voltage, Vout is stable and remain 0V due to not operating as it need clock to operate. This is because, during DC, the capacitors act as open circuit. Hence, if looking at the Vth at M5 as shown in figure 15, the Vth = -436.617mV. Therefore, it requires 5*Vth = 2.18V for the transistor to operate. Since the Vdc is about 0-1V, thus, the Vout is remain 0V.

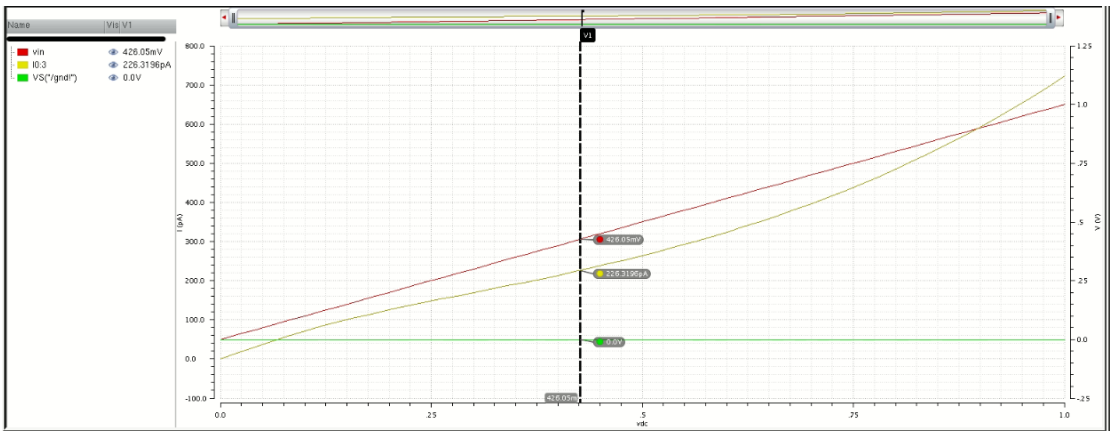


Figure 27. Graph for DC characteristic for Vdc from 0 to 1V

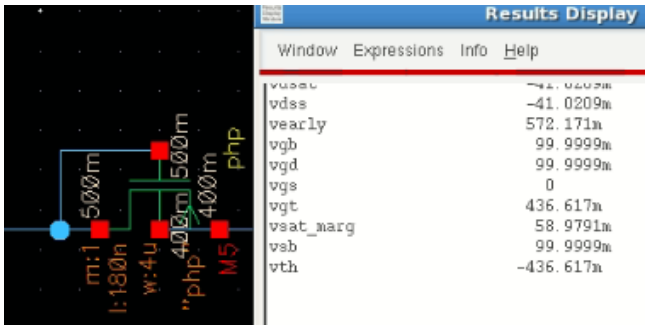


Figure 28 Vth value for M5 Transistor

When change sweep for Vdc from 0V to 3V, as shown in figure below, the voltage increase from uV to mV after 2.5V . While, when increase the sweep value to 5V, the output voltage become linear as shown in figure 30.

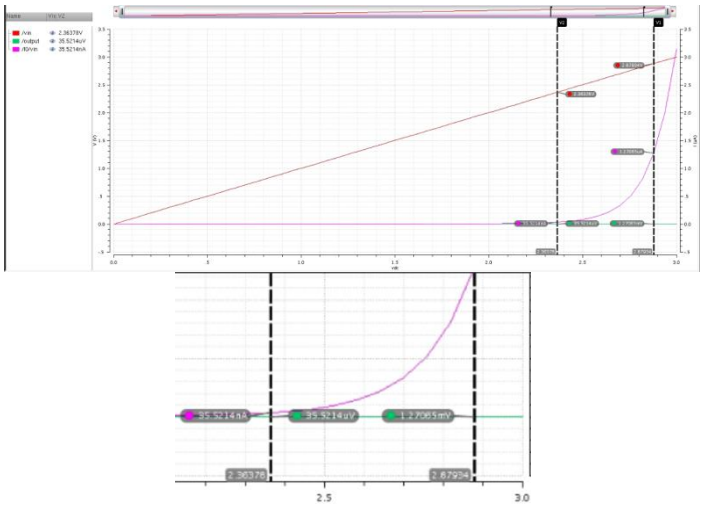


Figure 29 : Graph for DC Characteristic (Vdc 0-3V)

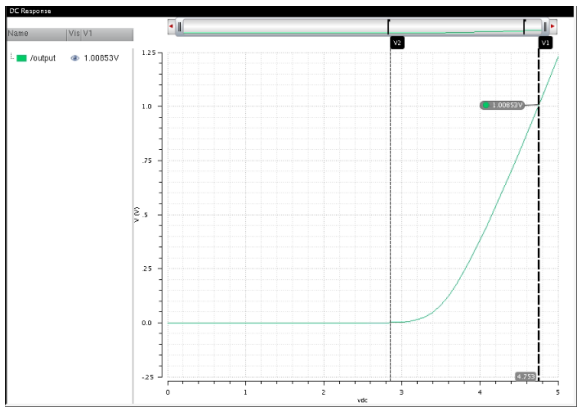


Figure 30 :Graph for DC Characteristic (Vdc 0-5V)

Figure 32 illustrates the graph where the transistor is turn on faster at 2V when load resistor RL is change from 1K ohm to 1 M ohms.

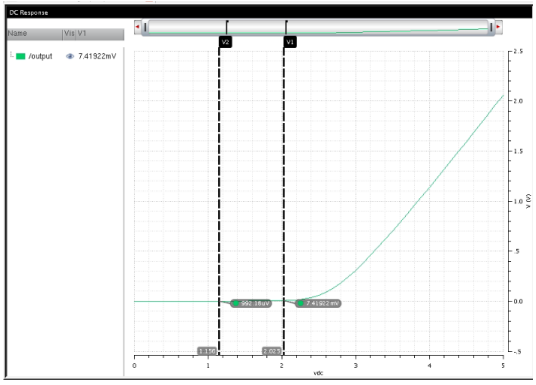


Figure 31. Graph when R_L = 1M ohms

Next, after voltage, the current will be tested by plotting the current in and current out. As shown in graph below, current out is opposite from current in as the current out is in negative value. This proves that the currents are flowing from input to output. Hence the DC characteristic are successfully tested and the circuit is works.

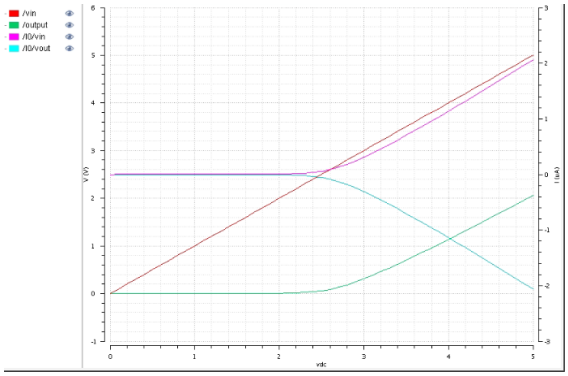


Figure 32. Graph for DC characteristic

On the other hand, PMOS transistor is change to NMOS transistor to test for clock. When the parameters below are configure, the output voltage seems like it pumping down the voltage as the value for output voltage is below than input voltage.

Freq =1Mhz, RL=1M ohm, CL=10pF, W/L = 1u/180n

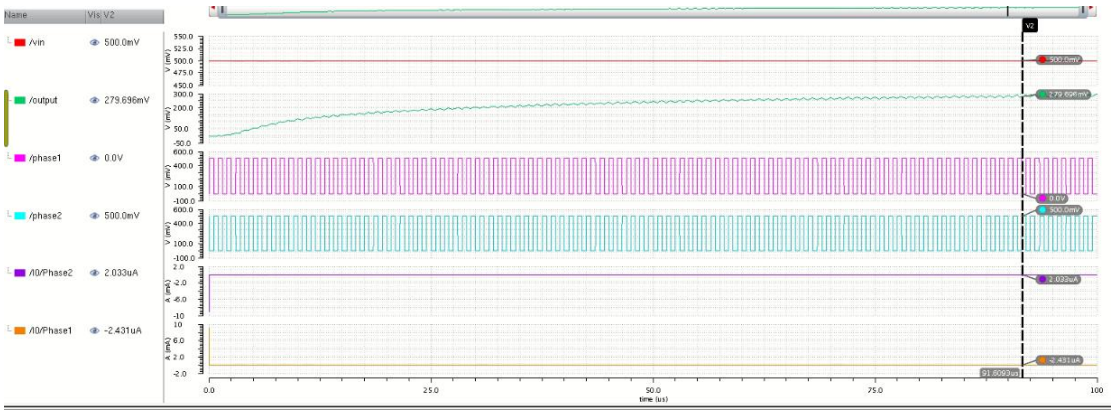


Figure 33. Simulation result Vin =500mV

In addition, the transistor size is increased to 3u/180nm in order to determine whether the output voltage would change as the voltage is pushed down. However the outcomes remain unchanged and the output voltage continues to drop.

Next approach is increase the number of stages from 5 to 9 stages. However, the results turns out as in figure below where the output voltage is too much drop due to many stages.

Freq =500KHz, RL=1M ohm, CL=10pF, W/L = 3u/180n

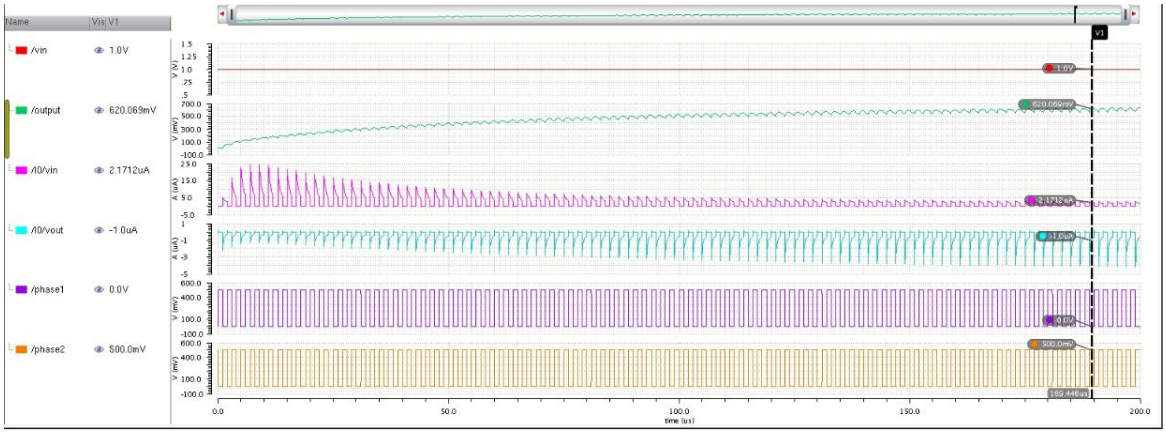


Figure 34 Simulation result Vin=1V

Moreover, since the design keep on pumping down the output voltage,the next approach is connect the bulk of the transistor to the ground as shown in schematic design in figure 35 and set the parameter as below. The output voltage is pumping up where the supply voltage is 1V and the output voltage is 1.433V however, it is not achieve our goals which to supply around 0.5V-0.9V and the output voltage will be approximately 1V.

RL=1M ohm CL=50pF, freq =10MHz

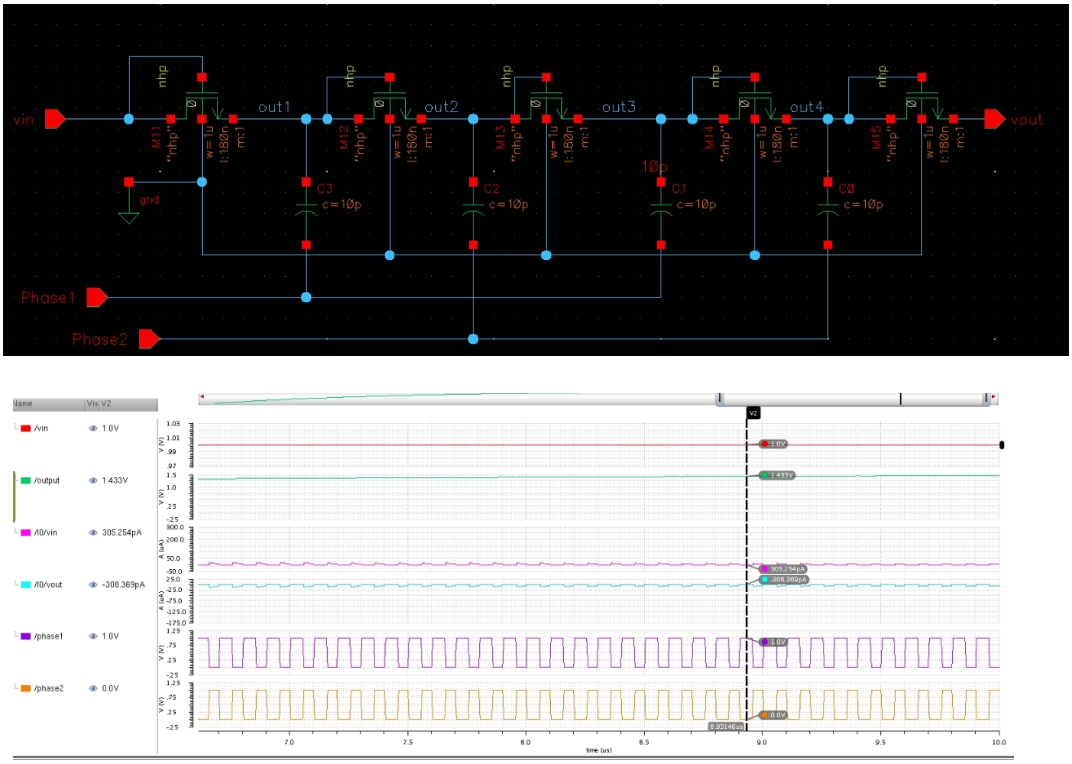


Figure 35. Schematic and simulation result for Vin =1V

As a result of the output voltage being increased by the following approach. The next step is to create an output voltage Vout of around 1V using various supply voltages. This implies that even if the source voltage may change, the output voltage will always be around 1V. The load resistor RL should be adjusted according to the supply voltage, and the remaining parameters should remain constant until the required output voltage is reached.

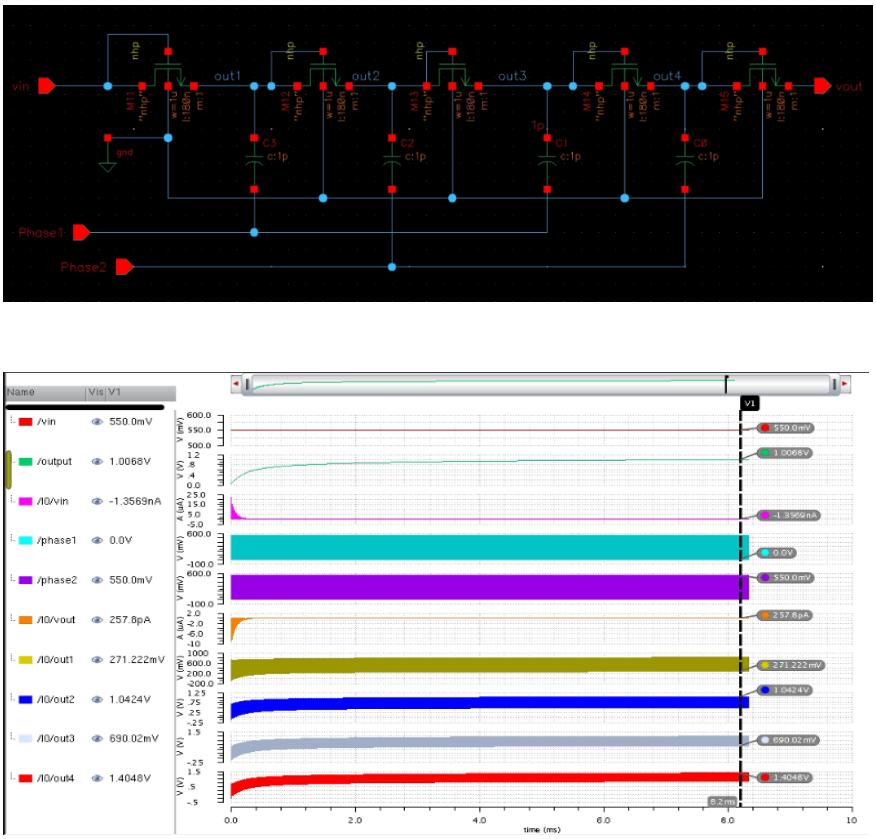


Figure 36 Simulation Result of DCP

The result shows that the load resistor can affect the output voltage. The lowest the supply voltage, the higher the load resistor required. However, it only can supply at least 550mV in order to get ~1V output voltage.

Table 2 Parameters for Proposed Design I

Vin (V)	**RL(ohm)**	**CL (pF)**	**FREQ (Hz)**	**CP (pF)**	**Vout (V)**
550m	5G	50	600K	1	1.0
650m	58M	50	600K	1	1.0
750m	12M	50	600K	1	0.99
850m	7M	50	600K	1	1.02

950m	5M	50	600K	1	1.05

3.3 PROPOSED DESIGN (Part I)

The block diagram shown below is the first proposed design where the charge pump is directly connected to supply voltage. Hence, the output voltage is only depend on the input voltage. This method is an open loop circuit as it do not have any feedback circuit that can feedback the output to get the desired result. Since this circuit do not have any feedback circuit, hence it wont regulate the output voltage to get as expected result which is around 1 V.

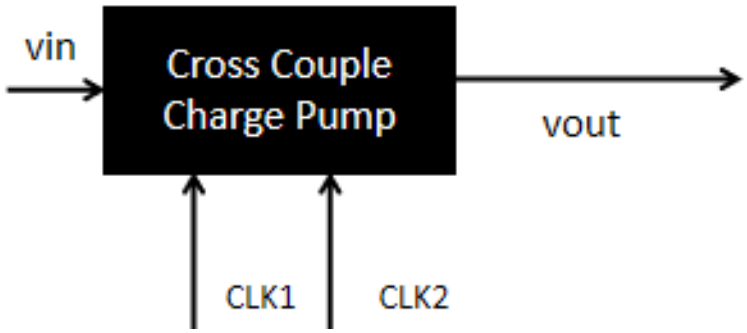


Figure 37. Block Diagram of Charge Pump without PFM

Nevertheless, since the bulk terminals of the NMOS transistor are linked to ground, a downside of the Dickson Charge Pump is that it can cause a reduction in the threshold voltage and body effect, which can reduce the pumping efficiency. The proposed design that will be used in this project is shown below. This proposed design is consists of the 5 stages of charge pump, two source clocks, one supply voltage and output voltage. As can be seen, both high performance NMOS and PMOS transistors and capacitor have been

utilized in this design. The architecture is essentially the same as the Dickson Charge Pump, but it has been improved by the addition of a floating well and cross couple technique.

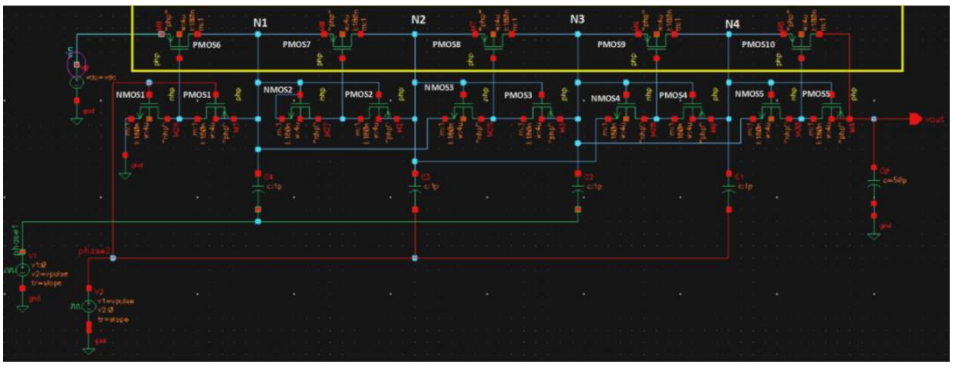


Figure 38. Proposed Design I

Based on figure above, the highlighted yellow is the floating well which using PMOS transistor. The floating well has the ability to maintain a constant voltage between the source and the body. It may lessen the body's impact. The parasitic capacitance of this circuit are reduced, and the design and implementation of this method in a traditional CMOS n-well process are both simple. Moreover, it resolves the body effect issue and boosts output voltage gains.

The charge transfer switches utilized in this circuit have the ability to be totally switched on and off as requested. The charge transfer switches technique is shown in figure above by the pair of MOS transistors NMOS and PMOS. The following explanation explains how the dynamically regulated charge transfer switches work. When clock phase 1 is high, clock phase 2 will be low, hence NMOS1 will be charged by couple effect of C4. Next, when the

voltage at N1 is greater than its threshold voltage Vth, NMOS2 will be turned on. Thus, NMOS2 will transfer lower voltage to PMOS7 for it to turn on. After that, voltage at N2 become lower due to couple effect of C4 and when the voltage at N3 is bigger than its Vth, N2 will turn on the PMOS3. on the other hand, PMOS3 will transfer high voltage to PMOS8. however, PMOS8 will turn off due to gate-to-source voltage is zero which can avoid reverse current transmit by PMOS8. Next, for the clock phase 2, when the clock phase is high, it will cause the clock phase1 become lower hence, PMOS7 OFF and PMOS8 will turn on and the same case happen as in clock phase 1 for following transistor.

Because of this suggested design, the charge transfer switches and floating well may be employed to efficiently reduce the PMOS gate voltage while increasing the transmission voltage in the diode-connecting channel. These methods can lessen the body effect and the threshold voltage drop. As a result, the improved charge pump circuit may totally transfer voltage levels. The result are shown in appendices where the frequency are keep changing with input supply around 0.35V to 0.75V in order to get output voltage approximately 1V.

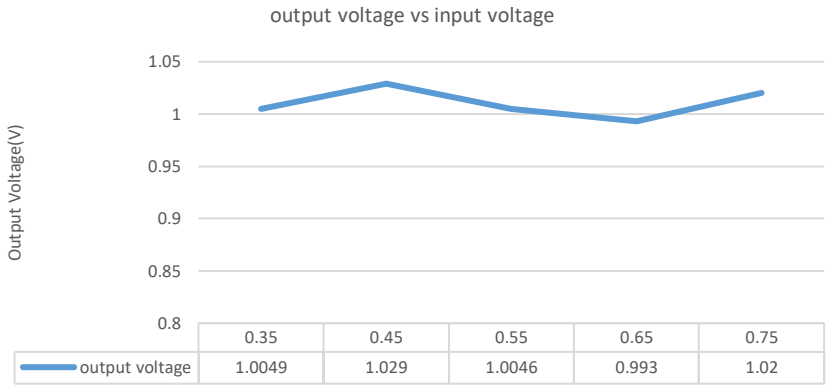
3.4 RESULTS AND DISCUSSIONS

In this simulation, the charge capacitor (CP), load capacitor (CL), size of the transistor for PMOS and NMOS are all same which are 50p, 1p, 4u/180n respectively. However, the supply voltage and frequency are varies in order to get approximately 1V output voltage. Table below is the result of the simulation, where the higher the supply voltage, the bigger the clock frequency.

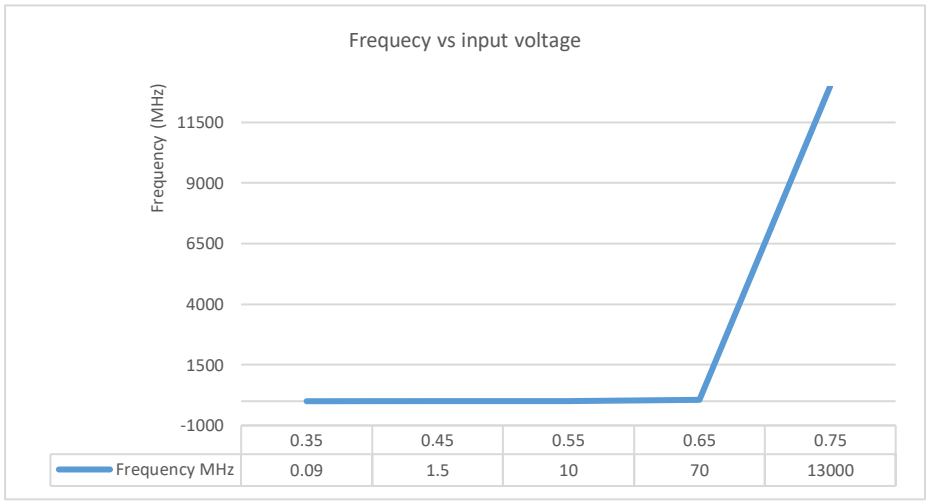
Table 3 Parameters of Charge Pump without PFM

Vin(mV)	Frequency (Hz)	Vout (V)	CL(F)	CP(F)	W/L (m)
350	90K	1.0049	50p	1p	4u/180n
450	1.5M	1.029	50p	1p	4u/180n
550	10M	1.0046	50p	1p	4u/180n
650	70M	0.993	50p	1p	4u/180n
750	13G	1.02	50p	1p	4u/180n

As shown in figure 39a, the result of the output voltage when the frequency is keep changing as shown in figure 39b in order to get approximately 1V while other parameters are constant. It shows that high frequency are required to pump the small input voltage in order to boost up the output voltage. This is because when the frequency is increases, the load current will decrease, hence the output voltage will be increase.



(a)



(b)

Figure 39. (a) output voltage vs input voltage (b) Frequency vs input voltage

3.5 PROPOSED DESIGN (Part II)

Additionally, to further accomplish our main goal for this project, which is to create a wide supply integrated CMOS employing a DC-DC converter, pulse frequency modulation (PFM) is also implemented. The primary function of PFM is to maintain the charge pump's output voltage at the correct reference voltage. The PFM control method is a technology often used in DC-DC converters to accomplish voltage management while boosting power efficiency. Below is shown the block diagram of the whole architecture in this project. Previously, the output of the charge pump is directly connect to the input supply and the clock source is coming from the external source. However, in this proposed design, the clock source of the charge pump is generated by the Pulse Frequency Modulation. The output voltage of the charge pump will be compared with reference voltage (Vref) which set to 1V. When the PFM detect there is mismatch in between output voltage and also reference voltage, the PFM will regulate the frequency and ensure that the output voltage will get approximately 1V.

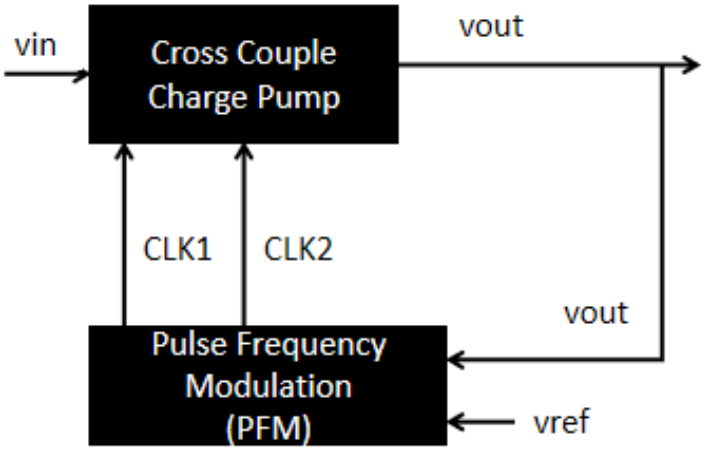


Figure 40. High Level of Proposed Design II

Figure 41 shows the details of the PFM where it consists of latch comparator, NAND gate, and ring oscillator. The purpose of comparator is to compare the reference voltage and output voltage and the output of the comparator will go to NAND gate. On the other hands, the purpose of ring oscillator is to generate clock. Hence, NAND gate will regulate these two clocks to generate a clock that will be a source clock for the charge pump. Ring oscillator is consists of three inverter that will continuously produce a clock.

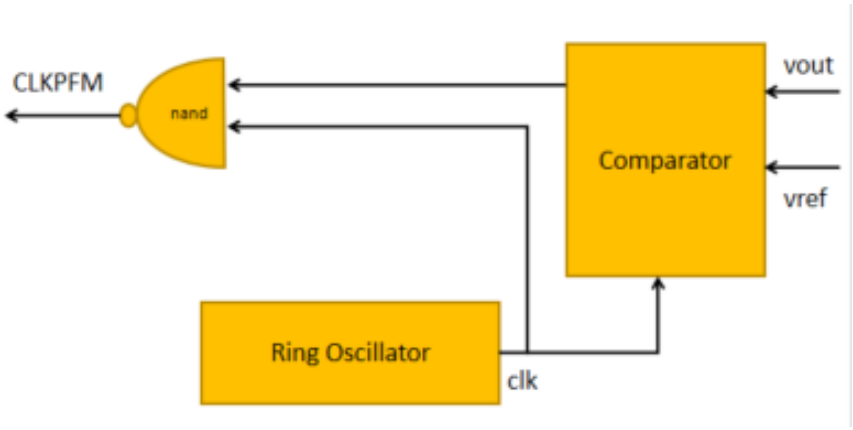


Figure 41. The Architecture of PFM

The charge pump method is remain as in previous proposed design where it used cross couple topology. The reason of using cross couple charge pump is because cross couple charge pump has greater voltage conversion efficiency compared to the existence charge pump which is Dickson Charge pump. This is because the arrangement in cross couple topology improves the efficiency by lowering the voltage drop along the switches during the transferring charges cycles as well as reducing switching losses. Not just that, cross couple also able boost up the voltage output more effectively rather than Dickson Charge pump as in Dickson charge pump topology, the output voltage along the load capacitor will have voltage drops due to the switch resistance

and threshold voltage. Even though the value is small, but it can get bigger when the stages of the charge pump increases. While in cross couple operations, the voltage drop are diminished which can boost up input voltage more accurate. Furthermore, by using cross couple charge pump, it can reduce the reverse leakage currents which can cause inefficiencies and affect the voltage boost process.

3.6 RESULT AND DISCUSSIONS

Cross couple charge pump has been simulated by creating a test bench as shown in figure below. It is made up of five stages of charge pump, two clock sources, capacitor pumping, input and output voltages. C4 and C2 are connected to clock 1 while C1 and C3 are connected to clock 2. Bulk terminals for all NMOS in between NMOS and PMOS are connected to ground while PMOS are connected to VOUT. Bulk of NMOS is connected to ground to ensure that the threshold voltage of the NMOS transistor is properly defined. Hence, it can operate effectively as switches when the Vgs is greater than Vth. As a result, it may help to reduce the sub-threshold leakage current and enhance the performance. While for PMOS, the bulk terminals are connected to output voltage for charge storage purpose. This allow it to store and release charge during voltage transfer cycles to boost up the supply voltage.

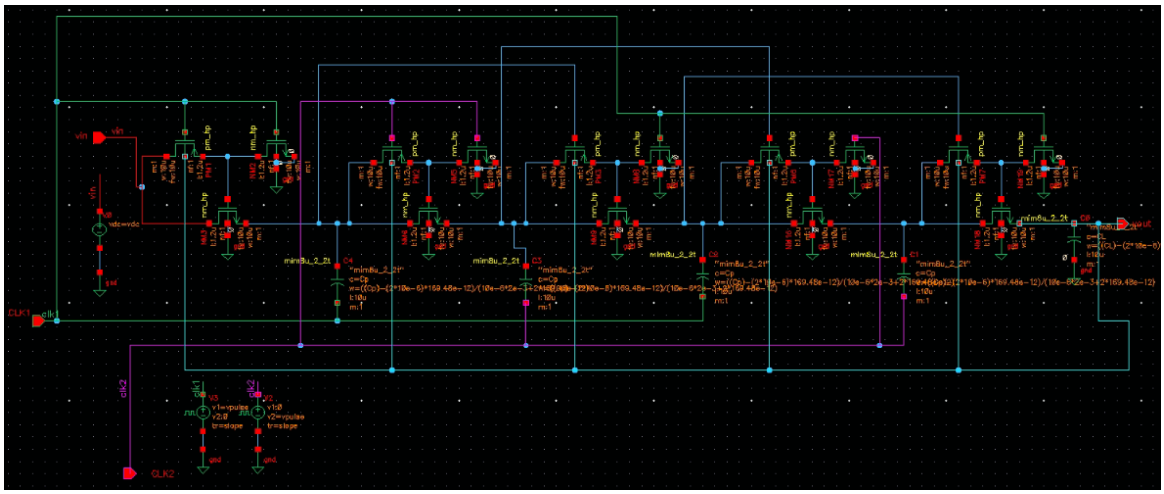


Figure 42. Test Bench of Cross Couple Charge Pump

As shown in figure 42, the input voltage charges capacitor C1, capacitor C2 charges capacitor C3, and capacitor C4 charges the output capacitor (Cout) during phase 1 of the proposed charge pump arrangement. The output voltage from Cout drives the load. Transistor M8 is switched on during this period, whereas transistor M7 functions as a diode-connected transistor where the gate and drain terminals of the transistor are shorted together, and the source terminal is connected to the drain terminal. This effect allows the transistor to conduct current in only one direction, similar to a diode, allowing the charge transfer between the stage capacitors while minimizing leakage effects. In phase 2, capacitor C1 charges capacitor C2, and capacitor C3 charges capacitor C4. Cout continues to supply current to the load. The parameters are set as shown below. The purpose of testing the charge pump is to determine that this circuit are able to boost up the supply voltage. Thus, when the supply voltage is set to 550mV the voltage output can reach 1.3V with 250KHz frequency as describes in figure 44.

	Name	
1	Cp	50p
2	delay	1n
3	slope	5n
4	vdc	550m
5	frequency	250K
6	vpulse	vdc
7	period	1/frequency
8	duty_cycle	period/2
9	stop_time	period*1000

Figure 43. Parameters of Proposed Charge Pump

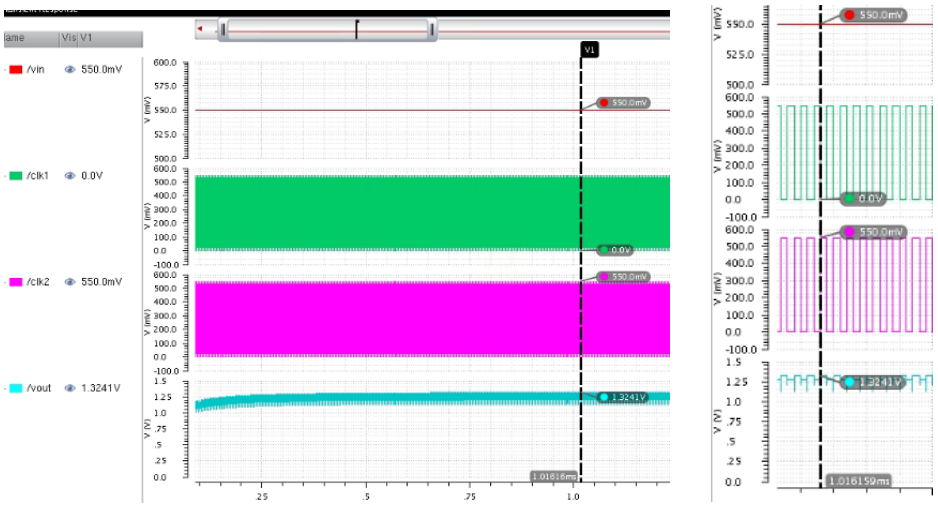


Figure 44. Simulation Result when Vin = 550mV

Next, when the voltage supply change to 450mV , the charge pump able to boost up until 1V of output voltage as shown in figure below. The parameter are remain unchanged. The graph shows that when the input voltage is increase, the output voltage will be increase as well. Since the clock of the charge pump is coming from the clock source, the result are not stable as it operates in open loop. This is because the charge pump does not have any feedback that can regulate the output voltage approximately 1V.

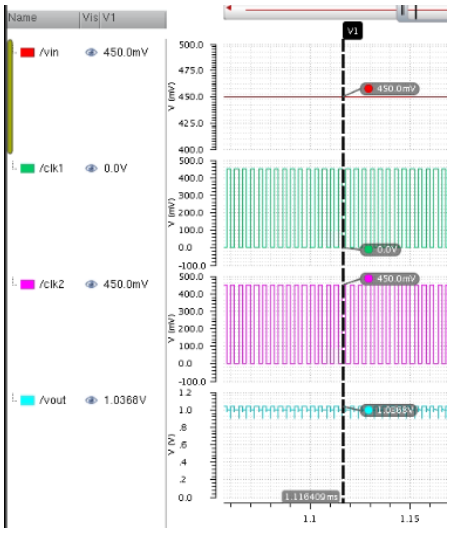


Figure 45. Simulation Result when Vin =450m

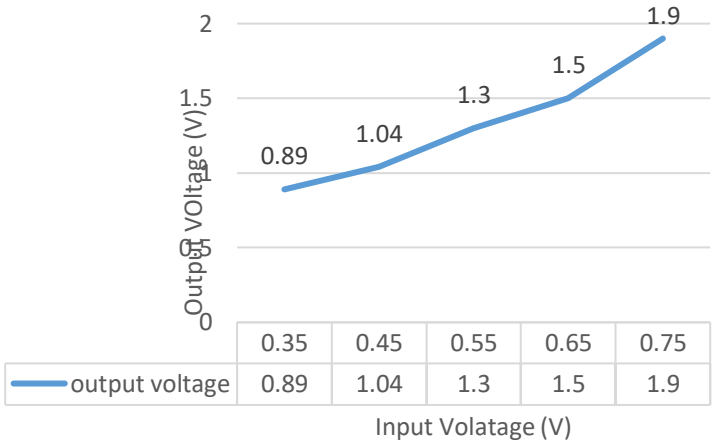


Figure 46 Graph of Input Voltage vs Output Voltage

Next, Pulse Frequency Modulation in this proposed design is made of latched comparator, nand gate and ring oscillator. In order to build the PFM, each of the components need to be simulated to ensure the behaviour of each components are correct. The purpose of PFM is to generate a regulate clock that responsible to source clock for the charge pump.

Figure 47 describe the test bench of the PFM that has been simulated in this project. As can be seen, vref is reference voltage that always set to 1V. while vout_CP is output voltage that has been generated from the charge pump. Ring oscillator will keep producing clock for comparator and nand gate. Hence, the output voltage of the charge pump will be compared with vref. It the value is not match, the PFM will start regulate the clock to generate a new vout that approximately vref which is 1V. Nand gate is responsible to regulate the clock from the ring oscillator and the output from the comparator. Therefore, the result from the nand gate will go to the charge pump.

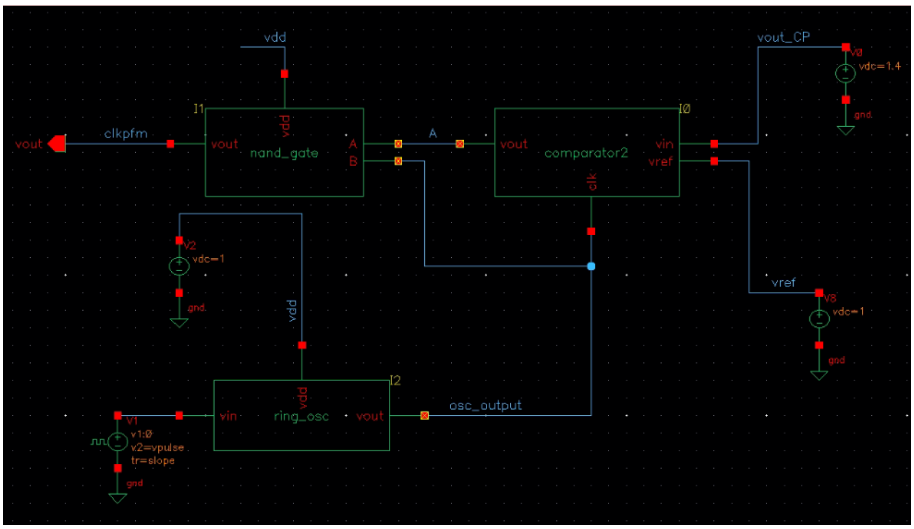


Figure 47. Test Bench of PFM [26]

The PFM used in this proposed design is based on the paper "A Charge Pump Based Power Management Unit with 66% Efficiency in 65nm CMOS". However, they paper is used 2:1 multiplexer to give an option to the desgn to choose whether to use non regulation or regulation clock. But in this project, the clock will always regulate depend on the output voltage.

Inside the PFM, latched comparator has been utilized to compare the result from the charge pump and the reference voltage that set to 1V. Test Bench of latched comparator design has illustrated in figure 48 is referring to this paper Design of a Strong-Arm Dynamic-Latch based comparator with high speed, low power and low offset for SAR-ADC [27] where the proposed latched comparator are able to operate with lower offset voltage and reduce dynamic offset. By lowering the offset voltage, it can reduce the difference between switching threshold. This is vital for precise comparison, particularly in applications requiring accuracy. Dynamic offset, commonly referred to as input-referred noise or flicker noise, is the fluctuation in offset voltage caused

by shifting input circumstances or other external variables. Reduced dynamic offset makes the comparator's response more consistent and stable under shifting situations. This stability is critical in applications that demand consistent performance under varying conditions, ensuring that the comparator's performance stays predictable and accurate.

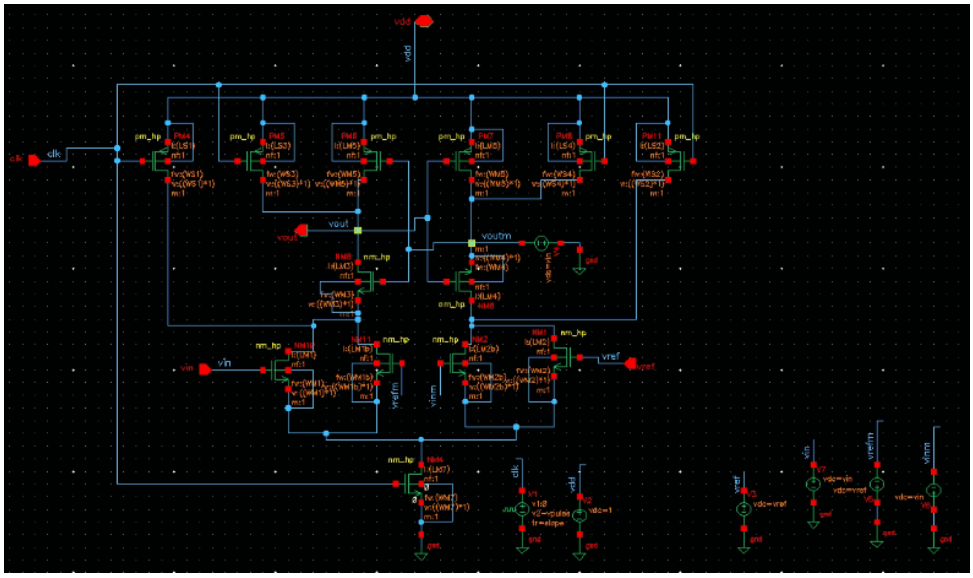


Figure 48. Test Bench of Latched Comparator [27]

Figure 49 is the result simulation of the latched comparator where the vref is set to 1V and let say the output voltage of the charge pump (vin) is 500mV , therefore, when the comparator compared the Vin and Vref, the Vout will generate the voltage that same as reference voltage which is approximately 1V when it detect mismatch between vin and vref. Based on the simulation result, it shows that the comparator design is behaving as expected with the all parameters stated.

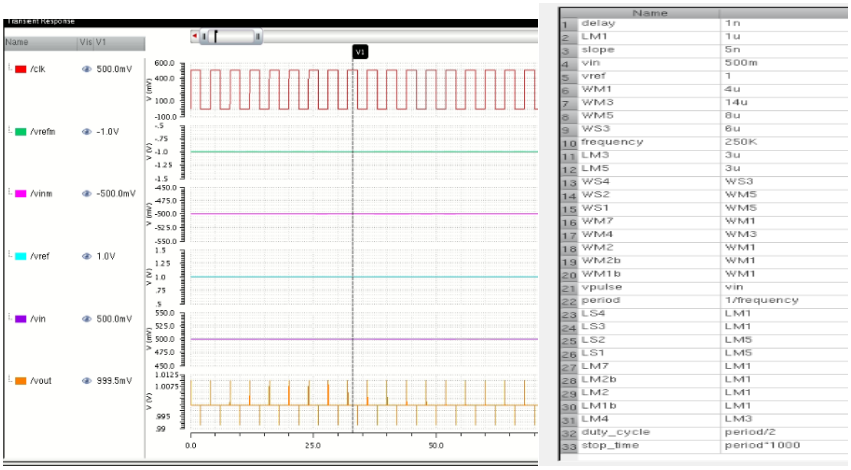


Figure 49. Simulation of Comparator and the parameters

Next, is to simulate NAND gate by creating a test bench as shown in figure 50. Table below is illustrates the truth table of NAND gate. Nand gate is made of two PMOS that connected in parallel while two NMOS transistor are connected in series.

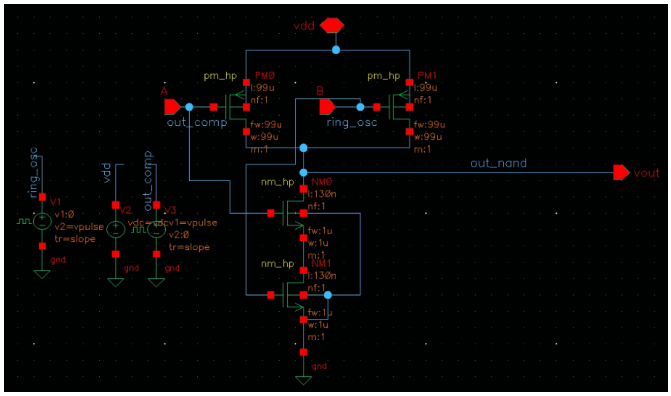


Figure 50. Schematic Design of NAND gate

Table 4. Truth Table NAND gate

A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

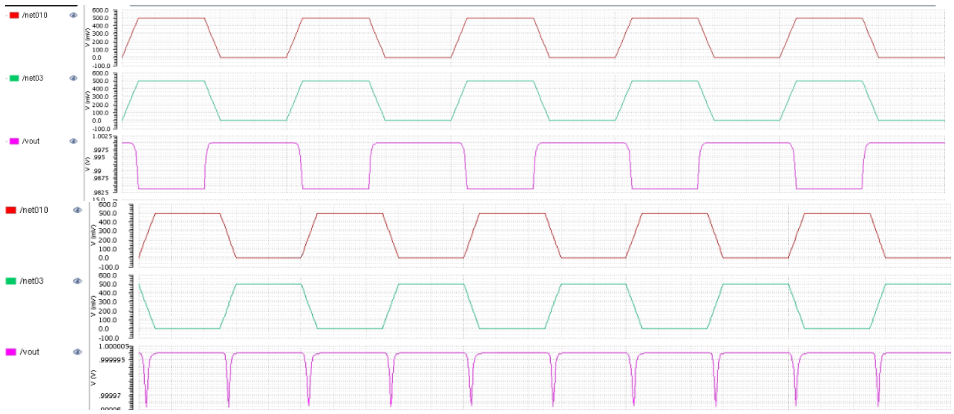


Figure 51. Simulation of NAD gate

As shown in the simulation result, the NAND gate is behaving as expected where when the input A is 0 and input B is 0, the output will be 1. Same goes to when the input A and input B is not same either A is 0 and B is 1 or vice versa. The output will remain as 1. However, when the input A and B is 1, the output will be 0.

Moreover, ring oscillator is made of three inverters as shown in figure below. Before simulating the ring oscillator, inverter are required to test to ensure the output is inverting the input.

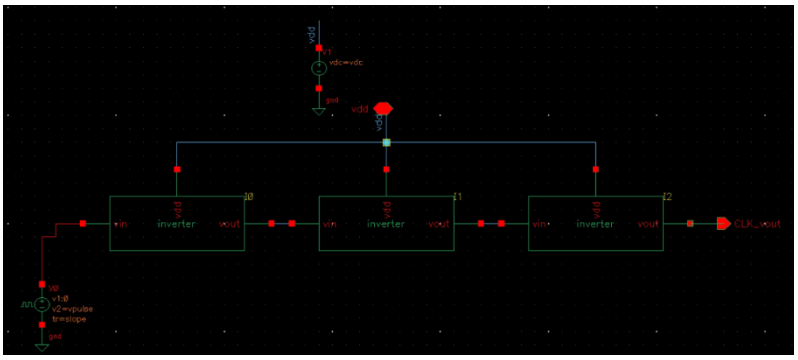
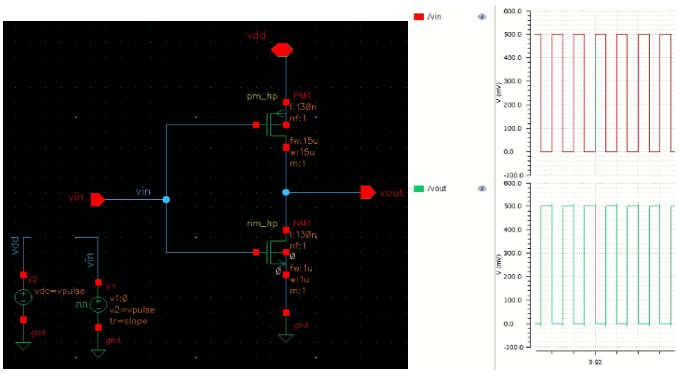


Figure 52. Test Bench of Ring Oscillator

Figure 53 illustrates the test bench of inverter. Schematic design of inverter is very simple as it only consists of one PMOS and NMOS where the PMOS need to connected on top while NMOS is connected to ground. Based on the simulation result, the inverter is generated a correct output where they are inverting each other.



(a) Test Bench of Inverter *(b) Simulation of inverter*

Figure 53. Inverter (a) Test Bench (b) Simulation Result

Since the inverter is behaving as expected, therefore simulating the test bench of ring oscillator can be done as shown in figure 54. Based on the result, it shows that the vout which is the output of the ring oscillator is inverting the input signal. Thus, it proves that the ring oscillator is behaving as expected.

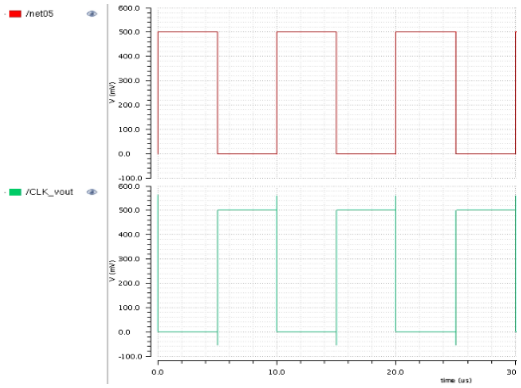


Figure 54. Simulation Result of Ring Oscillator

Since all the components inside the Pulse Frequency Modulation are behaving as expected. Simulating the test bench of PFM in figure 47 can be continued. The result below showing the output of PFM. As mentioned before, the PFM are responsible as a clock source to charge pump. Hence the output of PFM which is clkpfm should in clock waveform as shown in figure 55. in summarize, when the vref and vout_CP is compared using comparator, it will generate output A, for this case A is approximately 1V . Next, the output A will be fetch by NAND gate same goes to the output ring oscillator where the clock from ring oscillator and the output from the comparator will be input for NAND gate to regulate the clock and produce clkpfm.

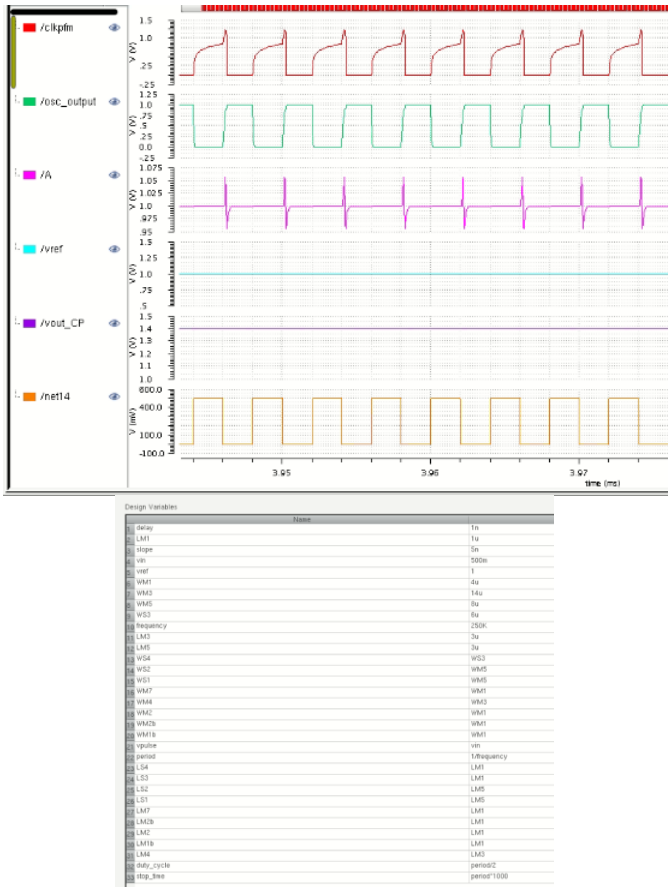


Figure 55. Simulation of PFM and The Parameters Used

The next step is to integrate the charge pump design with the PFM design. Note that all the design are being tested with fixed parameters as shown in figure 55. Figure 56 describes the test bench for whole charge pump where it consists of load capacitor, inverter, pulse frequency modulation (PFM) and cross couple charge pump. As mentioned before, the clk pfm will be a source clock for the charge pump. However, the clk 1 is directly connected to the charge pump while the clk2 is inverted of the clock generated by the PFM. Therefore, the inverter is used to invert the clock generated by PFM. Pulse Frequency Modulation (PFM) control scheme affects the output voltage of the charge pump by regulating the switching frequency of the charge pump's internal MOSFET switches. The PFM control scheme enables the charge pump

to adjust its output voltage dynamically, responding to load conditions and maintaining the desired voltage level efficiently. By having the PFM, this design are operates in close loop manner where it give feedback in order to achieve voltage regulation while minimizing power consumption.

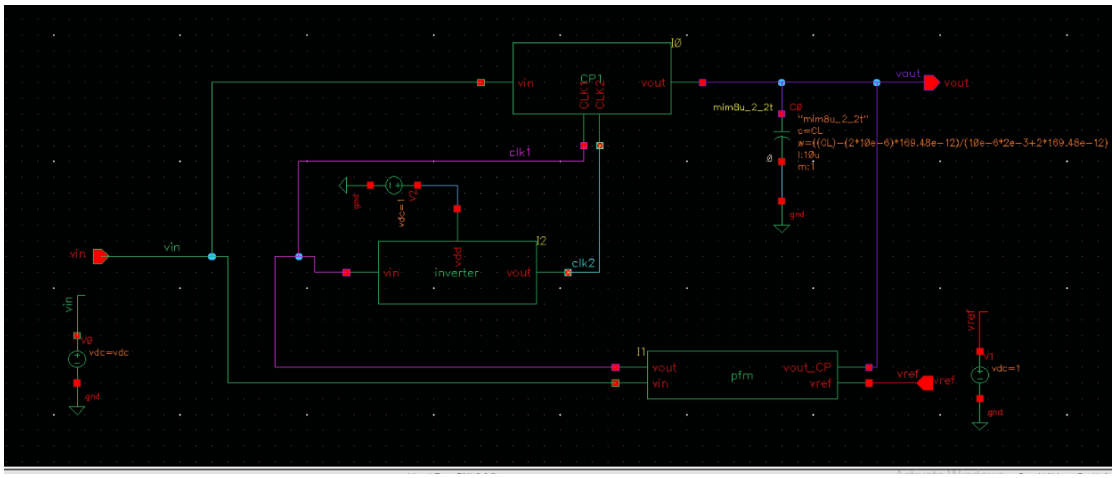


Figure 56. Test Bench of Proposed Design

The simulation result of whole design shown in figure below, as can be seen the when the input supply is 550mV, 650mV and 750mV, the output voltage able to pump up approximately 1V which same as reference voltage. All the parameters are remain same while the input supply will keep changing to test whether the output voltage able to generate a stable around 1V.

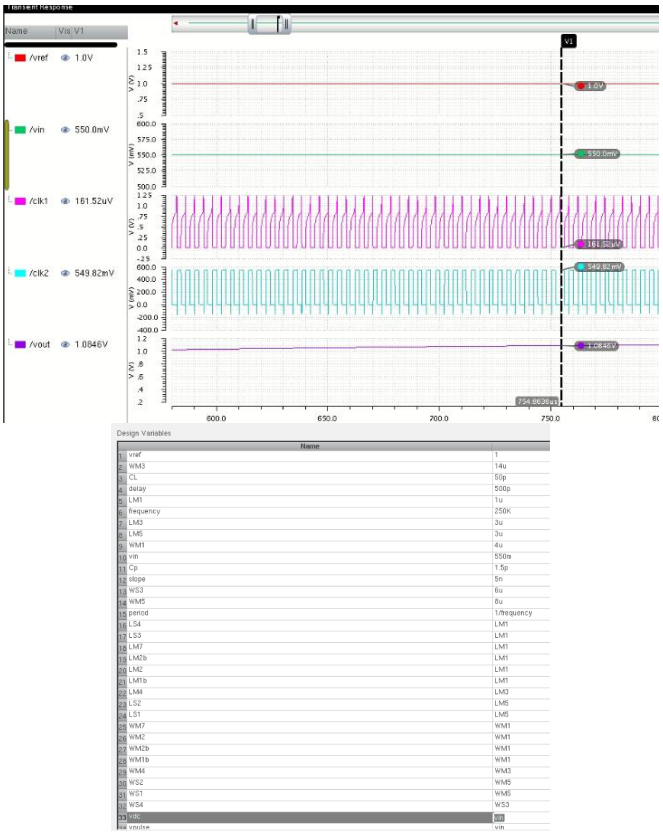


Figure 57. Simulation of proposed design and parameters, Vin =550mV

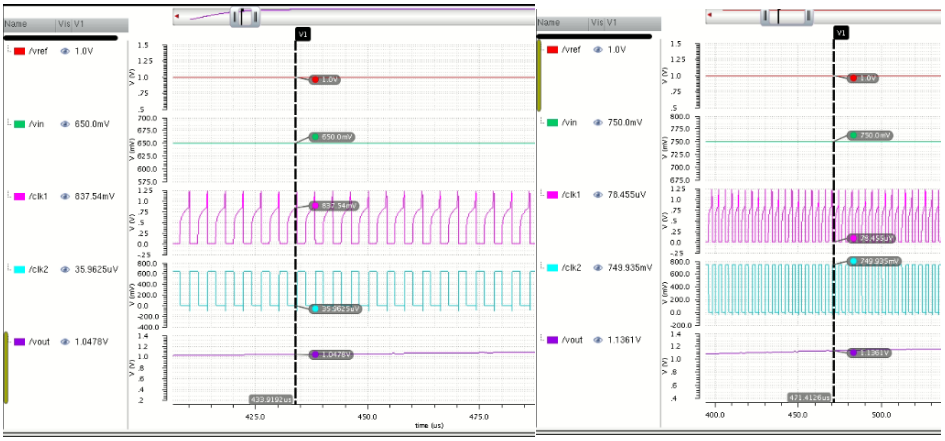


Figure 58. Simulation of proposed design when Vin = 650mV and 750mV

Graph below illustrates the output voltage of the proposed design when the input supply are varies. It shows that the proposed design able to stable the output voltage by having a close loop manner using Pulse Frequency modulation (PFM).

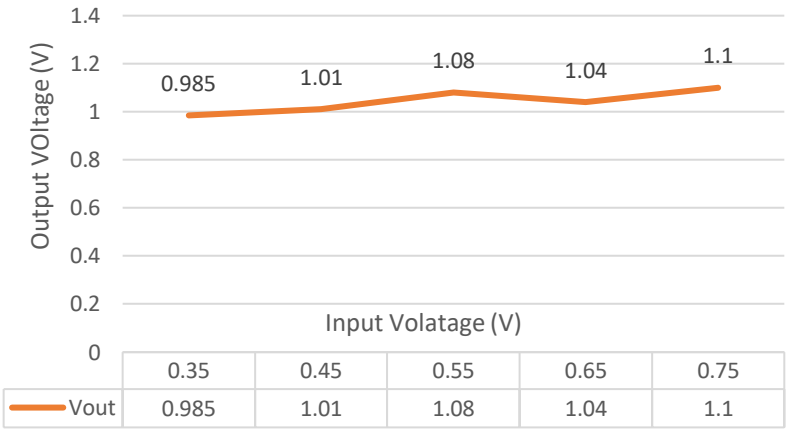
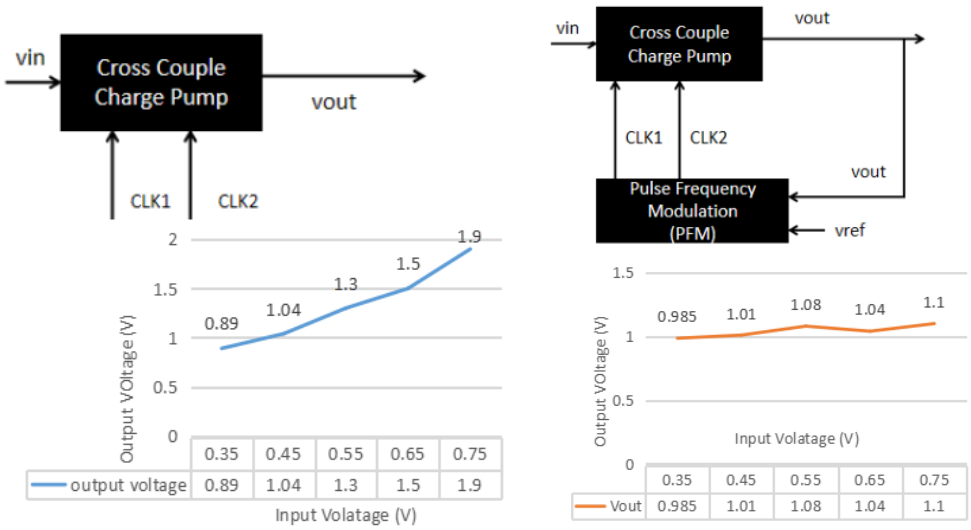


Figure 59. Graph of Simulation For Proposed Design II



(a)Charge Pump Without PFM *(b) Charge Pump with PFM*

Figure 60. Comparison of with and without PFM

Figure 60 shows the comparison of cross coupled charge pump with and without pulse frequency modulation. Charge pump that operates without PFM is known as open loop operations as there is no feedback given. This is because the clock source of the charge pump is coming from the external sources and the output of the charge pump is directly depend on the input supply. Without using PFM, the output voltage is not stable and need to tuned some parameters in order to get a stable output from a low input supply.

For the second proposed design as describes in figure 60(b) which using PFM to regulate the frequency in order to achieve our main objectives of this project which is to develop a wide-supply integrated CMOS using DC-DC converter. By using PFM, this proposed design is operates in close loop manners as there is a feedback given in order to get the desired output. Besides that, the PFM is will generate a clock source that will use by the charge pump. From the graph, it shows that the output of the charge pump are more stable

when using PFM as it can control scheme affects the output voltage of the charge pump by regulating the switching frequency of the charge pump's internal MOSFET switches. Even though it is not accurate 1V but our main objective is approximately 1V. Hence, +- 5% of output volateg 1.08V are acceptable. The range of 1.08V is because the median input voltage id 550mV. Therefore, the reading will be taken in between for 350mV, 450mV, 550mV, 650mV and 750mV.

Table 5. The parameters used in proposed design.

Variable	Value
Vin (V)	0.35/0.45/0.55/0.65/0.75
Vref (V)	1
Frequency (Hz)	250K
Period (s)	1/frequency
Duty cycle (s)	Period/2
Cp	1.5pF
CL	50pF
W/L(m)	10u/1.2u

Table 6. Parameters used for Comparator

Variable	Value (m)
LM1/LM2/LM1b/LM2b/LS4/LS3/LM7	1u
LM3/LM5/LM4/LS2/LS1	3u
WM1/WM7/WM2/WM2b/WM1b	4u
WM5/WS2/WS1	8u
WS3/WS4	6u

Table 5 and table 6 shows the parameter used in the whole design and the for comparator purposed. The frequency used in this design are fixed 250KHz which source to the ring oscillator for it to generate a continuous clock. Capacitor pumping and load capacitor also remain constant which are 1.5pF and 50pF respectively. However, the supply voltage will be varied to tabulate data in between 0.35V to 0.75V. The size of the transistor used in comparator is follows as in [27].

CONCLUSION

In conclusion, wide-supply integration CMOS dc-dc converter for energy harvesting application has been develop, designed and simulated using 130nm CMOS technology and proved by Cadence Virtuoso software. The data have been tabulated in the result and discussion section. Based on the result, this proposed design is able to develop a DC-DC converter for energy harvesting as the input supply is very low around 0.35V to 0.75V which suitable for energy harvesting application. Cross coupled charge pump has been chosen to meet the requirement of energy harvesting which may transform the harvested energy to the desired voltage levels. By using cross coupled topology, it proves that can enhance the existence charge pump which is Dickson Charge Pump (DCP). by comparing DCP and the proposed design, the DCP need at least 550mV in order to get output voltage approximately 1V however in cross couple charge, it able to boost up the lower input voltage 350mV to 0.98V output voltage. Next, this proposed design able to support a wide supply and get a stable output voltage +- 5% of 1.08V by using Pulse Frequency Modulation (PFM). The using of PFM with the proposed design helps to dynamically adjusts the frequency of the ring oscillator to regulate the output voltage based on the load and input voltage conditions. All of these objectives has been simulate and recorded using Cadence Virtuoso software. However, this proposed design can be more accurate by using noise or error architectures to ensure that the output of each components are accurate to produce an efficient result.

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