# FRONT END DESIGN (LOGIC SYNTHESIS) OF RISC-V PROCESSOR USING DESIGN COMPILER

**KOAY YENN NEE**

**A project report submitted in partial fulfilment of the**

**requirements for the award of Master of Engineering (Electronic Systems)**

**(Structure C)**

**Faculty of Engineering and Green Technology (FEGT)**

**Universiti Tunku Abdul Rahman**

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# DECLARATION

I hereby declare that this project report is based on my original work except for citations and quotations which have been duly acknowledged. I also declare that it has not been previously and concurrently submitted for any other degree or award at UTAR or other institutions.

Signature : 

Name : KOAY YENN NEE

IC No. : 970529-07-5190

Date : 10-AUGUST-2023

**APPROVAL FOR SUBMISSION**

I certify that this project report entitled **"FRONT END DESIGN (LOGIC SYNTHESIS) OF RISC-V PROCESSOR USING DESIGN COMPILER"** was prepared by **KOAY YENN NEE** as met the required standard for submission in partial fulfilment of the requirements for the award of Master of Engineering (Electronic Systems) (Structure C) at Universiti Tunku Abdul Rahman.

Approved by,

Signature : 

Supervisor : Ir. Dr. Loh Siu Hong

Date : 10 August 2023

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# ABSTRACT

Modern microprocessors depend on Design Compiler's logic synthesis of RISC-V processor Front-Ends. This study examines the synthesis process for a 14nm, 32nm, or 90nm RISC-V processor at clock periods from 0 to 5 nanoseconds. The analysis begins with design constraints, including clock frequency, area limits, and timing requirements for each technological node. The Design Compiler tool converts the Register Transfer Level (RTL) description of the RISC-V processor into a gate-level netlist. The design's applicability to 14nm, 32nm, and 90nm process nodes is assessed during synthesis by linking technology libraries. After synthesizing designs, performance indicators like timing closure, clock period needs, and slack margins across technology nodes are analysed. To understand the processor's power consumption, power analysis is done at different clock intervals. To optimize designs at each technological node, processor area consumption is analysed. The research examines 14nm, 32nm, and 90nm front-end design performances using clock durations from 0 to 5 nanoseconds. These different manufacturing technologies and operating circumstances provide vital insights about the processor's performance, power efficiency, and space usage. With this knowledge, designers can choose technology, clock frequency, and architectural changes to suit future computing system demands. This research helps designers construct high-performance, energy-efficient, area-optimized RISC-V processors that are adaptable to different technology nodes and clock periods. The study advances front-end design in microprocessor development, enabling the design of cutting-edge processors that excel across varied technology landscapes and operating scenarios.

# TABLE OF CONTENTS

# LIST OF TABLES

# LIST OF FIGURES

# LIST OF SYMBOLS / ABBREVIATIONS

# LIST OF APPENDICES

# CHAPTER 1

# INTRODUCTION

## 1.1 Background

The desire for faster computers fuelled the microprocessor revolution over the last several decades, and substantial study has been undertaken to determine the capabilities of computer applications in a variety of disciplines. For example, computer applications in automobiles, cell phones, and the human genome project are not commercially viable until the computer technology revolution occurs. The fast growth of computer industry will make augmented reality, self-driving cars, and phones as thin as a sheet of paper possible in the future.

Computer architecture, which includes instruction set architecture, microarchitecture, and logic design, is necessary to create a computer system. It is necessary for a consumer electronic computational device to have a highly efficient system with low cost and power consumption, as well as excellent energy efficiency and security [1].

Computer architectures are classified into two broad categories: Complex Instruction Set Computing (CISC) and Reduced Instruction Set Computing (RISC) (RISC). CISC and RISC architectures each have their own set of advantages and limitations, and the architecture chosen is determined by the design's intended use. As a result of its compatibility with direct native hardware implementation rather than simulations, RISC-V is a widely recognized Instruction Set Architecture (ISA). It also provides support for substantial instruction set expansions, which may be implemented by specialised variants [2].

Instruction Set Architecture (ISA), commonly known as computer architecture, plays a critical role in computer design by serving as the interface between software and hardware [3]. Intel, AMD, and ARM all have their own ISA designs, which are either CISC or RISC architectures. However, the most widely

used commercial ISAs are proprietary, and other firms will be required to pay significant licencing costs to utilise the ISA designs. This results in increased research expenditures for hardware designers and precludes academics from utilising any ISA in hardware or software creation.

At the University of California, Berkeley, the RISC-V project began in 2010 with the goal of developing an academically useful open-source licence ISA [4]. RISC-V is a RISC architecture that was derived from the original RISC architectures. It was intended to facilitate tiny, rapid, and low-power implementation in the actual world. It quickly gained popularity among the community and attracted the attention of industry participants. Additionally, the open nature of RISC-V fosters academic study by allowing for the publication, reuse, and modification of its design.

Exploring system-level factors to optimise run-time performance in the front-end flow is a well-researched topic in the literature. However, the majority of solutions in the literature are imperfect and frequently rely on a complicated set of factors that can be reduced.

Due to this flexibility, an open instruction set architecture dubbed RISC-V has recently changed system design. As a result of the impetus generated by RISC-V adoption, there is a rising need for RISC-V system design and prototyping. While various attempts have been made to design and create efficient single-core RISC-V compute systems [5]. There is a rising demand for frameworks that facilitate the investigation of RISC-V-based SoCs in order to allow system designers to create efficient platforms for next-generation computing systems.

## 1.2 Problem Statement

In many embedded systems such as mobile smart phones, portable gaming gadgets, and mobile computers, System-on-Chip (SoC) has become a practical solution in numerous application areas such as cryptography, image processing system, and digital signal processing. SoC is bringing their complex algorithm that requires a lot of computation into hardware, which is implemented as an Application Specific Instruction Set Processor (ASISP) as a co-processor or, more precisely, as a

hardware accelerator for a processor core, which is faster than software on the same platform.

RISC-V, being the group responsible for providing open-source, open-license ISA to the public, has established a strong presence in the industry. Apart from the person or academic researcher developing their ideas, several firms, including Qualcomm, Samsung, Alibaba, and Nvidia, use RISC-V in their processors. With the rapid expansion of the RISC-V contributor community, the ISA's success is simply a matter of time. Although the RISC-V community is expanding rapidly, only few processor designs based on this ISA have been released due to the ISA's brief development history. However, with the community's continued support, the RISC-V software ecosystem and toolchains have grown over the years. Regrettably, most of the RISC-based CPU development is still centred on the ARM and MIPS architectures.

This research aims to improve the timing of RISC-V as well as its total power consumption through the application of a vast array of technology libraries. In order to gain a faster performance from the hardware, it is necessary to test with various technology. Within the scope of this inquiry, a Front-End Design (Logic Synthesis) of RISC-V Processor Using Design Compiler is proposed.

## 1.3 Objective

1. To study the principle of the RISC-V architecture.
2. To implement the RISC-V processor with the aid of EDA tools – Design Compiler.
3. To perform logic synthesis by optimised the timing of RICS-V processor before Place and Route with variant of technology libraries.

# CHAPTER 2

# LITERATURE REVIEW

## 2.1 RISC-V

### 2.1.1 Principle and Architecture

The abbreviation RISC means for Reduced Instruction Set Computer, and it is a form of microprocessor architecture that employs a compact, basic, and highly efficient set of instructions.

Along with its flexibility, a new open instruction-set architecture known as RISC-V has completely transformed the elements of system design. RISC-V-based system design and prototyping are becoming increasingly popular as a result of the momentum generated by the adoption of the architecture [6]. The RISC processor requires new instructions, all of which are the same length, most of which are executed in one machine clock cycle, the control unit is hardwired, and it has a large number of registers and limited address modes [3].

### 2.1.2 Previous Work of the RISC-V

According to the report [7], a heterogeneous processor that is based on an open source 64-bit core of the RISC-V architecture, as well as a reconfigurable neural network accelerator, is being developed. The authors explore the characteristics of the implementation of a binary matrix neural network on FPGA and its combination with the RISC-V RV64GC core in tasks of cognitive robotics and industrial production, with the goal of increasing safety in the interaction between a robot and a person. The FPGA's restricted resources were the most significant problems encountered over the course of the project. If a 115k logic gate microcircuit was used, just 11% of the resources are left available, which removes any need for intricacy in the neuroaccelerator architectural design.

Modern machine learning (ML) applications, such as deep neural networks, and video processing are becoming more dependent on real-time processing of pictures and videos. Having a more efficient and compressed floating point arithmetic may considerably improve the performance of such applications by optimising memory consumption and information transmission. Therefore, a RISC-V processor is suggested by the authors [8] to operate image processing. The authors accomplished significantly more than 60 frames processed per second in both the 16-bit and 8-bit positive cases with the aid of the RISC-V processor. Implementing positive arithmetic in the vector environment in order to completely transition to positive arithmetic in all DNN operations, allowing future researchers to take full advantage of data compression to 16 or 8 bits, will be the focus of future development.

### 2.1.3 Advantages of RISC-V

The research agrees that RISC-V has certain distinct benefits over standard ISAs. According to some of RISC-designers, V's the objective was to build an ISA that was equally suited to basic and large applications and could be readily upgraded and branched by the community [9]. Branching an open-source piece of software refers to the process by which an engineer adds or removes sections of the source code to make the programme better fit their requirements.

The fact that RISC-V is open-source software was cited as a distinguishing benefit by authors in the literature [9]–[11]. In fact, part of the examined literature documents RISC-V branches and how they optimise it for a single, unique intended purpose [10]–[12].

Based on the conference paper [10], the researchers looked at RISC-V branches that include special instructions for use in cryptography and machine learning. Branch of RISC-V exhibited up to nine times the performance of a baseline RISC-V processor in cryptography and machine learning applications in testing of more than 60 CPU implementations. In one example, the researchers discovered that a cryptographic RISC-V branch completed an encryption operation 9.3 times quicker

than a standard RISC-V processor. It did this with a small increase in resource overhead and just a 4% increase in cycle time.

## 2.2 System-On-Chip (SoC)

### 2.2.1 Definition

A 'system' is comprised of a CPU, memory, and peripherals. A bespoke or conventional microprocessor, or a specialised media processor for sound, modem, or video applications, might be used as the processor. There may be numerous processors as well as additional bus cycle generators such as DMA controllers. DMA controllers can be arbitrarily complicated, and they are only separated from processors by the absence or presence of instruction fetching. Processors communicate with one another using a number of techniques, including shared memory and message-passing hardware entities such as specialised channels and mailboxes [13]. There are two majors process in constructing a complete SoC, which is front-end and back-end process.

### 2.2.2 Front-End

Front-end of the VLSI is needed a high-level requirement, such as function, throughput, and power consumption, must be specified in the design. Design capture is the act of transferring a design from the marketing person's thoughts, the back of an envelope, or a word processor document into machine-readable form.

To find an implementation with appropriate power and load balance, architectural exploration will test various combinations of processors, memory, and bus topologies. A flexibly timed high-level model is sufficient to compute an architecture's performance. The logic synthesis process will transform behavioural RTL to structural RTL.

There are some steps are required during the front-end design [13]:

1. Specification:

   This is the first step in the design process in which we determine the major system parameters that must be specified.

2. High level Design:

   At this stage, several features of the design architecture are determined. At this time, details regarding the various functional blocks, as well as the interface communication protocols between them, are being established.

3. Low Level Design:

   The microarchitecture phase is also known as low level design. During this phase, lower-level design specifics for each functional block implementation are defined. Modules, state machines, counters, MUXes, decoders, internal registers, and other details can be incorporated.

4. RTL coding:

   At the RTL coding process, the micro design is specified in a Hardware Description Language, such as Verilog/VHDL, using synthesizable constructs of the language. The use of synthesizable structures allows the RTL model to be fed into a synthesis tool, which will eventually transform the design to real gate level implementation.

5. Functional Verification:

   The act of assessing the functional features of a design by producing multiple input stimuli and testing for accurate design implementation behaviour is known as functional verification.

6. Logic Synthesis:

   It aids in the translation of RTL to structural RTL. Logic Synthesis assists in solving existing design issues by optimising time, area, power, and testing all at the same time. It provides a predictable flow, resulting in a shorter time to results and a pre-implementation area estimate. As a result, the designer can anticipate and estimate the space and duration during the pre-layout process.

### 2.2.3 Logic Synthesis

Logic synthesis converts a high-level digital circuit description, usually in an HDL, into a hardware-implementable representation. Logic synthesis optimises area, power, and time while maintaining functionality.

In logic synthesis, flip-flops, logic gates, and arithmetic operators are identified from the input HDL description. These building blocks are mapped to a library of standard cells, pre-designed and pre-verified logic gates that may be effectively implemented in hardware. Timing and power consumption limitations guide mapping.

Logic synthesis optimises circuit size, power, and timing after mapping basic building blocks to standard cells. Combining algorithms at different abstraction levels usually does this. Retiming and pipelining can optimise circuit timing. Boolean logic optimisation and technology mapping can reduce circuit area and power.

After optimisation, logic synthesis generates a netlist for physical design. The netlist shows how standard cells are connected and whether buffers or multiplexers are needed to meet design limitations. Physical design tools build a silicon-fabricable circuit architecture from the netlist.

In conclusion, logic synthesis helps digital circuit designers turn high-level specifications into optimal lower-level representations that may be implemented in hardware. Logic synthesis uses computational techniques and design limitations to optimise performance, area, and power while maintaining circuit functioning.

### 2.2.4 Previous Work about SoC

This paper [14] provides a brief summary of existing System on Chip applications in IoT and the medical arena, as well as their methodology. A thorough examination of essential system characteristics including as power, throughput, and latency provides an in-depth understanding of the architectures of HNoCs and ECG-based identification systems. This article also gives an overview of current advancements

in Heterogeneous Network-on-Chip Simulator interconnects, data collecting, and patient analysis approaches. Biometric solutions are the ideal fit for all health applications based on the Internet of Things. The study shows framework-based SoCs, IoT cloud-based patient data storage, and a basic machine learning tool to discover patients from their obtained data, which aids in remote diagnosis and treatment.

To mitigate the effects of unpredictable timing and to apply the dynamic voltage and frequency scaling (DVFS) scheme for overall power reduction, high performance, and complex system-on-chip (SoC) designs necessitate a throughput and reliable timing monitor. The researchers [15] describes a multi-stage timing monitor that combines three timing-monitoring stages to provide high timing resolution and a wide timing range at the same time. Furthermore, because the suggested timing monitor is immune to pro. The suggested architecture offers minimal PVT sensitivity and good stability in complicated SoCs with varied operating conditions. This timing monitor not only decreases the impact of uncertain timing on the system but also increases the efficiency and accuracy of DVFS operation in high performance and complicated SoC designs. Power–voltage–temperature (PVT) change, it gives more stable time-monitoring data.

As a proof-of-concept, researchers offer a model for the logic synthesis of sequential logic circuits and confirm that we can handle multiple types of sequential logic circuits. In specifically, the researchers successfully manufactured parallel counters ranging from 4-bits to 32-bits and analysed the clock rates of their respective architectural designs. Moreover, certain components of a 16-bit MIPS CPU can be synthesised. This inquiry reduces the number of buffers required for pipeline stage balancing [16]. A unique technique based on the co-optimization of standard cell designs and synthesis algorithms to efficiently tune synthesised circuits in order to extract more performance from any given design [17].

## 2.3 Process Node / Technology

SAED_EDK14_FINFET[18], SAED_EDK32/28_CORE[19] and SAED_EDK90_CORE[20] are three different semiconductor technologies/ process

node, each with its unique features and characteristics. Both technologies is widely used in education purposes that invented by *The Synosys,Inc*[21]. Students may apply a complete design flow and master today's complex design criteria, such as those for low power, when combined with the latest Synopsys EDA tools. Each library has digital and I/O standard cell libraries, memory, phase-locked loops, technology kits, and example designs [21].

### 2.3.1 SAED_EDK14_FINFET

SAED_EDK14_FINFET[18] is a 14nm FinFET technology, which refers to the size of the smallest feature that can be manufactured on the semiconductor wafer. FinFETs are a type of transistor that uses a fin-like structure to increase the transistor's performance and reduce power consumption. This technology is commonly used in high-performance processors and SoCs. Hence, it is employs a full 14nm high-performance FinFET SRAM design (1kB) based on a "realistic industrial strength" circuit design [22][23]. It is also used to study on high speed sense amplifier and improve the overshoots in voltage regulators by *Synopsys Armenia Educational Department*[24], [25].

### 2.3.2 SAED_EDK32/28_CORE

On the other hand, SAED_EDK32/28_CORE[19] is a 32/28nm planar CMOS technology. Planar CMOS refers to a type of transistor that uses a flat structure rather than a fin-like structure. This technology is commonly used in low-power applications[26], [27], such as mobile devices and IoT devices. IoT devices are often produced in large volumes and with tight cost constraints, SAED_EDK32/28_CORE may be a more attractive option for IoT device manufacturers. An efficient architectural design using SAED 32nm technology is the near-memory CMOS VLSI bit-sliced 2D architecture for Sobel edge detection for IoT image applications [28].

### 2.3.3 SAED_EDK90_CORE

The SAED_EDK90_CORE[20] Digital Standard encompasses a comprehensive collection of cell libraries, each containing several unique cells along with their corresponding technical specifications. The library is exempt from intellectual property limitations. The aforementioned component is a constituent element of the SAED_EDK90 Educational Design Kit (EDK). The SAED_EDK90, often known as the EDK, is designed to be utilized for educational purposes with the specific goal of training individuals to become highly skilled specialists in the field of microelectronics. This technology is typically employed in low-power applications[29]–[31], such as AMBA and Internet of Things (IoT) devices. IoT devices are frequently manufactured in large quantities and under stringent cost constraints.

### 2.3.4 Similarities between SAED_EDK14_FINFET, SAED_EDK32/28_CORE and SAED_EDK90_CORE

The SAED_EDK14_FINFET, SAED_EDK32/28_CORE, and SAED_EDK90_CORE are semiconductor devices that employ complementary metal-oxide-semiconductor (CMOS) technology. These devices have gained significant popularity and are extensively utilized across many applications.

a) CMOS Technology

   Both SAED_EDK14_FINFET and SAED_EDK32/28_CORE employ CMOS technology, a type of semiconductor technology that utilizes p-type and n-type transistors for the creation of logic gates and memory cells. The utilization of CMOS technology is prevalent in contemporary electronic devices owing to its notable attributes such as low power consumption, exceptional performance, and high integration density. In a similar vein, SAED_EDK90_CORE also leverages CMOS technology, so allowing it to capitalize on the corresponding benefits, such as enhanced power efficiency and increased integrated density.

b) Wide Range of Applications

SAED_EDK14_FINFET, SAED_EDK32/28_CORE and SAED_EDK90_CORE exhibit extensive utilization across several domains, including high-performance central processing units (CPUs), mobile devices, Internet of Things (IoT) devices, and other electronic systems. These technologies offer a range of performance and cost options, rendering them suitable for diverse applications. The adaptability of the three process nodes enables its deployment in diverse electronic systems, hence offering solutions for a broad spectrum of applications.

c) Advanced Manufacturing Processes

Both SAED_EDK14_FINFET and SAED_EDK32/28_CORE is based on innovative manufacturing procedures that employ sophisticated techniques to produce smaller and more complex semiconductor devices. These procedures include numerous steps, including lithography, etching, deposition, and doping, to produce the complex structures necessary for contemporary electronic devices. Similarly, the SAED_EDK90_CORE has been developed with sophisticated manufacturing techniques in order to attain enhanced levels of integration and performance, all the while preserving the advantageous characteristics of CMOS technology.

In summary, it can be observed that SAED_EDK14_FINFET, SAED_EDK32/28_CORE, and SAED_EDK90_CORE exhibit the shared characteristic of employing complementary metal-oxide-semiconductor (CMOS) technology and finding application in many domains. Moreover, all of these entities leverage improved manufacturing techniques to fabricate intricate semiconductor components for contemporary electronic systems.

### 2.3.5 Differences between SAED_EDK14_FINFET, SAED_EDK32/28_CORE and SAED_EDK90_CORE

a. Size

The primary difference between SAED_EDK90_CORE and SAED_EDK14_FINFET / SAED_EDK32/28_CORE lies in their size and technology node. SAED_EDK90_CORE is designed for the 90nm technology node, while SAED_EDK14_FINFET is for the 14nm FinFET node and SAED_EDK32/28_CORE is for the 32/28nm planar CMOS node. This means that SAED_EDK90_CORE has larger transistor sizes compared to the other two technologies, resulting in a lower integration density and potentially lower performance.

b. Transistor Structure

Structure of Transistors: A further distinction between SAED_EDK14_FINFET and SAED_EDK32/28_CORE is the structure of the transistors they employ. SAED_EDK14_FINFET employs FinFETs, a type of transistor with a fin-like structure that increases performance and decreases power consumption. SAED_EDK32/28_CORE and SAEED_EDK90_CORE employs planar CMOS transistors, which are characterised by a flat structure. FinFETs are regarded as superior to planar CMOS transistors in terms of performance and power consumption, but they are more costly to produce.

c. Performance

Performance is an additional distinction between SAED_EDK14_FINFET, SAED_EDK32/28_CORE and SAED_EDK90_CORE. SAED_EDK90_CORE may offer a different level of performance compared to SAED_EDK14_FINFET and SAED_EDK32/28_CORE. Due to its larger technology node, SAED_EDK90_CORE might have slower clock rates and potentially higher power consumption. SAED_EDK14_FINFET often

provides superior performance to SAED_EDK32/28_CORE, as seen by its faster clock rates, greater power efficiency, and enhanced performance in high-temperature conditions. However, SAED_EDK14_FINFET is more expensive to produce, making it less cost-effective for various applications.

d. Cost

In regard to cost, SAED_EDK90_CORE may possess a comparative advantage over SAED_EDK14_FINFET due to the utilization of a less sophisticated and potentially more economically viable fabrication technique. The cost of manufacturing semiconductor devices at the 90nm node may be comparatively lower when compared to the 14nm FinFET or 32/28nm nodes. Hence, it may be argued that SAED_EDK90_CORE presents a viable alternative in terms of cost-effectiveness for specific applications that do not necessitate the state-of-the-art capabilities offered by smaller technology nodes.

### 2.3.6 Summary of SAED_EDK14_FINFET, SAED_EDK32/28_CORE and SAED_EDK90_COREE

In general, FinFET technology offers better performance and lower power consumption than planar CMOS technology, but it is also more expensive to manufacture. Therefore, FinFET technology is typically used in high-performance applications that require the best possible performance, while planar CMOS technology is used in low-power applications where cost is a more significant concern. Table 2-1 is the summary table of both technologies finding.

Table 2-1 Summary of SAED_EDK14_FINFET, SAED_EDK32/28_CORE and SAED_EDK90_CORE

| | **SAED_EDK14_FINFET** | **SAED_EDK32/28_CORE** | **SAED_EDK90_CORE** |
|---|---|---|---|
| Manufacturing Process | FinFET (Fin Field Effect Transistor) | Tri-gate FinFET | Planar CMOS |
| Node | 14 nm | 32/28 nm | 90 nm |
| Performance | High performance and energy efficiency | High performance and energy efficiency | Performance suitable for various applications |
| Power Consumption | Low power consumption | Low power consumption | Low power consumption |
| Area Density | Higher area density | Lower area density | Moderate area density |
| Process Complexity | More complex manufacturing process | Less complex manufacturing process | Moderate complexity manufacturing process |
| Compatibility | Compatible with a variety of applications | Compatible with a variety of applications | Compatible with a variety of applications |
| Cost | More expensive than SAED_EDK32/28_CORE | Less expensive than SAED_EDK14_FINFET | Moderate cost |

In summary, SAED_EDK14_FINFET, SAED_EDK32/28_CORE and SAED_DK90_COR are three different semiconductor technologies with different performance, power consumption, and cost characteristics. The choice of technology

depends on the specific application and the trade-offs between performance, power consumption, and cost that are most important for that application.

## 2.4 Conclusion

It has been demonstrated that RISC-V processors based SoC are equivalent to commercial processors on the market in terms of the performance and efficiency that they give. The openness of the RISC-V instruction set architecture provides benefits to the industry not just from a financial standpoint (it is free and open-source), but it also encourages better innovation through free-market competition. In the end, the cost of processors will be reduced, making them more accessible for a wider range of applications, such as Internet of Things devices. As a result, RISC-V as an open-source instruction set architecture (ISA), will usher in a new era in the computing industry. SAED_EDK14_FINFET, SAED_EDK32/28_CORE and SAED_EDK90_CORE are semiconductor technologies with different performance, power consumption, and cost. The application and its performance, power consumption, and cost trade-offs determine the technology.

# CHAPTER 3

# METHODOLOGY AND WORK PLAN

## 3.1 Methodology Flow

There are three technology libraries will be tested compared in this project: SAED_EDK14_FINFET, SAED_EDK32/28_CORE and SAED_EDK90_CORE. Therefore, the following steps will be repeated against the technologies.

This project is divided into five stages:

1. Library Definition – The initial phase of synthesis is to map the design to a target library. This entails selecting a library of target technology that contains the set of cells and their related attributes, such as delay, power, and area.
2. Analysis - This process involves analysing the HDL code to determine its structure, design hierarchy, and other design restrictions. Timing constraints, power restrictions, and space constraints are examples of design constraints.
3. Optimization - During the optimisation process, the HDL code is transformed into an optimised gate-level netlist. Several optimisation techniques, including logic restructuring, constant propagation, and register balancing, are utilised to achieve this.
4. Technology Mapping - The optimised netlist is mapped to the target technology library at this stage. Choosing the optimal implementation for each logic element in the design based on its functionality and limitations is part of the technology mapping procedure.
5. Verification - Once the netlist has been constructed, its functionality and temporal limitations are validated using a logic simulator. The outcomes are examined, and any errors or infractions are rectified.

The flowchart is shown in Figure 3-1 which based on the front-end design flow in the section 2.2.2 above.

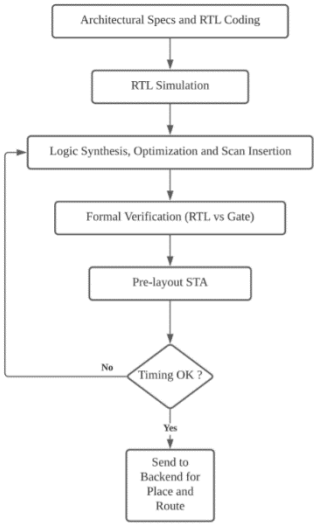


Figure 3-1 Flowchart of the Front-End

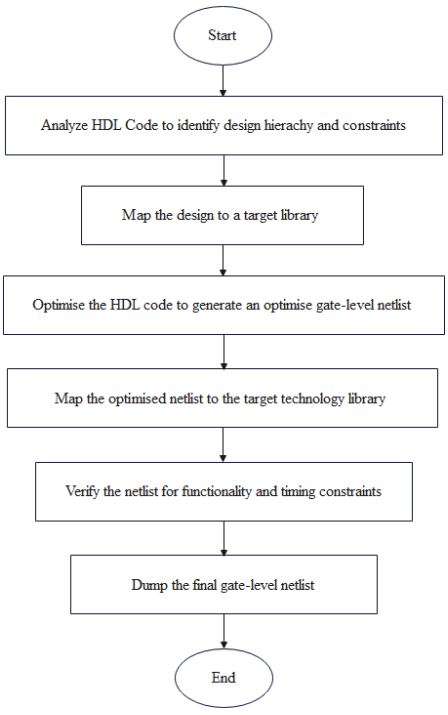


Figure 3-2 Flowchart of the Logic Synthesis

Figure 3-2 Flowchart of the Logic Synthesis is the details flowchart based on the 3.1 Methodology Flow.

## 3.2 Tools and Implementation

There is one and only tool is needed in this project, which is design compiler from Synopsys and used for synthesised purposes.

### 3.2.1 Design Compiler EDA Tool

Design Compiler (DC) is used for logic synthesis, which is the process of translating a hardware description language like as Verilog or VHDL design description into an optimal gate-level netlist mapped to a specific logic library. When the synthesised design meets functionality, timing, power consumption, and other design goals, and when it can be handed to the IC compiler tool for physical implementation.

Designs are logical circuit descriptions. Multiple design formats, including VHDL and Verilog HDL, are utilised to describe designs. To show logic-level designs, sets of Boolean equations are used. In order to illustrate gate-level designs, such as netlists, interconnected cells are utilised.

Designs can exist and be assembled separately, or they can be incorporated as sub designs within larger designs. Designs that are flat or hierarchical are preferred:

1. Designs that are entirely horizontal

   There are no sub designs and only one structural level in flat designs. They do not contain any cells from the library.

2. Organizations based on hierarchy.

   As sub designs, one or more designs are contained within a hierarchical design. Each sub design may contain further sub designs, resulting in a multi-layered design hierarchy. The parent design is the one in which the sub designs reside.

The components of a design are an instance, a net, a port, and a pin. It is capable of containing sub-designs and library cells. The design that is currently being developed is referred to as the current design. The bulk of commands are design-specific, which means they function within the context of the current design.

### 3.2.2 Implementations

This section will detail the intricacies of the Logic Synthesis process using Design Compiler, illuminating the meticulous steps involved in transforming a high-level hardware description in Verilog or VHDL into a gate-level netlist, ready for physical design and eventual manufacturing. There are three ways to execute in Design Compiler:

a. Interactive Command Entry in Design Compiler Shell:
   When working with Design Compiler, source the commands interactively, line-by-line, into the design compiler shell to execute various operations and configurations.

b. Comprehensive Source Script for All Steps:
   Construct a script that encompasses all the necessary stages, including constraint definition, reading the Verilog code, and linking the library. This one-time source script automates the entire procedure, streamlining your productivity for greater effectiveness.

c. User-Friendly Design Vision Graphic User Interface (GUI):
   The Design Vision Graphic User Interface (GUI) features an intuitive menu that was created with the user in mind. The user interface is effortless to navigate, making the instrument simple to use even for those unfamiliar with its features and capabilities.

In this undertaking, the design flow included both interactive command entry within the Design Compiler shell and the user-friendly Graphical User Interface

(GUI) of Design Vision. Throughout the process, the interactive commands were used to execute numerous operations and configurations in the Design Compiler shell. In addition, the Design Vision GUI enabled simple navigation and interaction with the tool's functionalities, making for a seamless and intuitive experience. As a result of utilizing these interactive methods, all commands were eventually consolidated into a comprehensive source script, thereby automating the entire procedure for increased efficiency.

#### 3.2.2.1 Execution Flow

##### 3.2.2.1.1 Environment Definition

To begin this voyage, the Design Compiler must first dexterously the “environment”. In the context of using Design Compiler, the term "environment" refers to a set of libraries and configurations necessary for the synthesis process. The key components of this environment include the target libraries, synthetic libraries, and link-libraries. The target libraries encompass the cell library specific to the design's target technology. These libraries contain pre-characterized standard cells, essential for building the gate-level representation of the design.

On the other hand, synthetic libraries, such as Design Ware libraries, consist of a collection of pre-optimized and pre-characterized intellectual property (IP) blocks provided by semiconductor IP vendors. These synthetic libraries serve as a valuable resource for efficiently incorporating complex functional elements into the design. Lastly, the link-libraries serve the purpose of linking against external libraries or modules, ensuring seamless integration of additional functionalities or custom components during the synthesis process. By meticulously setting up this environment and leveraging these libraries, Design Compiler enables a smooth and effective synthesis flow, culminating in a gate-level netlist ready for subsequent physical design steps.

The Table 3-1 shows the Environment File that setup with different technology libraires. Using a common .synopsys_dc.setup file becomes impractical when each technology library has distinct locations, databases, and tech files, as it

cannot accommodate the specific configurations required for each technology. In such cases, the .synopsys_dc.setup file must be customized and tailored to each design or process node target. This customization ensures that the appropriate technology libraries and associated files are linked during the synthesis process, allowing Design Compiler to make precise timing, area, and power estimates based on the specific process technology.

Table 3-1 Table of The Environment File for Three Differences Technology Libraries

| Technology (nm) | Environment File |
|---|---|
| 14 | puts "RM-info: Running script [info script]\n"<br><br>## Point to the new 14nm SAED libs<br><br>set DESIGN_REF_PATH "../SAED14_EDK"<br><br>set DESIGN_REF_TECH_PATH "${DESIGN_REF_PATH}/tech"<br><br>##########################################################################################<br># Hierarchical Flow Design Variables<br>##########################################################################################<br><br>set HIERARCHICAL_DESIGNS "" ;# List of hierarchical block design names "DesignA DesignB" ...<br>set HIERARCHICAL_CELLS "" ;# List of hierarchical block cell instance names "u_DesignA u_DesignB" ...<br><br>##########################################################################################<br># Library Setup Variables<br>##########################################################################################<br><br>set LINK_LIBRARY_FILES "* \<br>${DESIGN_REF_PATH}/lib/stdcell_rvt/db_nldm/saed14rvt_ss0p72v125c.db \<br>${DESIGN_REF_PATH}/lib/stdcell_rvt/db_nldm/saed14rvt_ss0p6v125c.db \<br>${DESIGN_REF_PATH}/lib/stdcell_rvt/db_nldm/saed14rvt_dlvl_ss0p72v125c_i0p72v.db \<br>${DESIGN_REF_PATH}/lib/stdcell_rvt/db_nldm/saed14rvt_dlvl_ss0p6v125c_i0p6v.db \<br>${DESIGN_REF_PATH}/lib/stdcell_rvt/db_nldm/saed14rvt_ulvl_ss0p72v125c_i0p72v.db \<br>${DESIGN_REF_PATH}/lib/stdcell_rvt/db_nldm/saed14rvt_ulvl_ss0p6v125c_i0p6v.db \<br>${DESIGN_REF_PATH}/lib/sram_lp/logic_synth/singlelp/saed14sram_ss0p72v125c_i0p72v.db \<br>${DESIGN_REF_PATH}/lib/sram_lp/logic_synth/singlelp/saed14sram_tt0p8v25c_i0p8v.db"<br><br>set TARGET_LIBRARY_FILES "\<br>${DESIGN_REF_PATH}/lib/stdcell_rvt/db_nldm/saed14rvt_ss0p72v125c.db \<br>${DESIGN_REF_PATH}/lib/stdcell_rvt/db_nldm/saed14rvt_ss0p6v125c.db \<br>${DESIGN_REF_PATH}/lib/stdcell_rvt/db_nldm/saed14rvt_dlvl_ss0p72v125c_i0p72v.db \<br>${DESIGN_REF_PATH}/lib/stdcell_rvt/db_nldm/saed14rvt_dlvl_ss0p6v125c_i0p6v.db \<br>${DESIGN_REF_PATH}/lib/stdcell_rvt/db_nldm/saed14rvt_ulvl_ss0p72v125c_i0p72v.db \<br>${DESIGN_REF_PATH}/lib/stdcell_rvt/db_nldm/saed14rvt_ulvl_ss0p6v125c_i0p6v.db \<br>${DESIGN_REF_PATH}/lib/sram_lp/logic_synth/singlelp/saed14sram_ss0p72v125c_i0p72v.db \<br>${DESIGN_REF_PATH}/lib/sram_lp/logic_synth/singlelp/saed14sram_tt0p8v25c_i0p8v.db"<br><br>set NDM_REFERENCE_LIB_DIRS " \<br>${DESIGN_REF_PATH}/lib/stdcell_rvt/ndm/saed14rvt_frame_only.ndm \<br>${DESIGN_REF_PATH}/lib/stdcell_hvt/ndm/saed14hvt_frame_only.ndm \<br>${DESIGN_REF_PATH}/lib/stdcell_lvt/ndm/saed14lvt_frame_only.ndm \<br>${DESIGN_REF_PATH}/lib/sram_lp/ndm/saed14_sram_lp_lrw_frame_only.ndm \<br>${DESIGN_REF_PATH}/lib/io_std/ndm/saed14io_wb_frame_only.ndm \<br>"<br><br>set NDM_REFERENCE_LIB_DIRS_CLG " \<br>${DESIGN_REF_PATH}/lib/stdcell_rvt/ndm/saed14rvt_frame_only.ndm \<br>${DESIGN_REF_PATH}/lib/sram_lp/ndm/saed14_sram_lp_lrw_frame_only.ndm \<br>"<br>set_app_var target_library $TARGET_LIBRARY_FILES<br>set_app_var synthetic_library dw_foundation.sldb<br>set_app_var link_library "* $target_library $synthetic_library"<br>define_design_lib default -path ./work<br>set MW_REFERENCE_CONTROL_FILE "" ;# Reference Control file to define the MW ref libs<br><br>set TECH_FILE "${DESIGN_REF_PATH}/tech/milkyway/saed14nm_lp9m_mw.tf" ;# Milkyway technology file<br>set MAP_FILE "${DESIGN_REF_PATH}/tech/star_rc/saed14nm_tf_itf_tluplus.map" ;# Mapping file for TLUplus<br>set TLUPLUS_MAX_FILE "${DESIGN_REF_PATH}/tech/star_rc/max/saed14nm_lp9m_Cmax.tluplus" ;# Max TLUplus file<br>set TLUPLUS_MIN_FILE "${DESIGN_REF_PATH}/tech/star_rc/min/saed14nm_lp9m_Cmin.tluplus" ;# Min TLUplus file<br>set GDS_MAP_FILE "${DESIGN_REF_PATH}/tech/milkyway/saed14nm_lp9m_gdsout_mw.map"<br>set STD_CELL_GDS "${DESIGN_REF_PATH}/lib/stdcell_rvt/gds/saed14rvt.gds"<br>set SRAMLP_SINGLELP_GDS "${DESIGN_REF_PATH}/lib/sram_lp/gds/singlelp.gds" |

32

```
set LIB_ROOT ../saed32nm/lib

set LVT_LIB " \
       saed32lvt_ss0p95v125c.db \
       "

set LVT_LIB_SEARCH_PATH "$LIB_ROOT/stdcell_lvt/db_nldm"

set search_path "$search_path \
                 $LVT_LIB_SEARCH_PATH"

set_app_var target_library $LVT_LIB
set_app_var synthetic_library dw_foundation.sldb
set_app_var link_library "* $target_library $synthetic_library"
define_design_lib default -path ./work

set mw_design_library MW_BC
set mw_reference_library "$LIB_ROOT/stdcell_lvt/milkyway/saed32nm_lvt_1p9m"

set TECH_FILE "$LIB_ROOT/tech/milkyway/saed32nm_1p9m_mw.tf"
set MAP_FILE "$LIB_ROOT/tech/star_rc/saed32nm_tf_itf_tluplus.map"
set TLUPLUS_MAX_FILE "$LIB_ROOT/tech/star_rc/saed32nm_1p9m_Cmax.tluplus"
set TLUPLUS_MIN_FILE "$LIB_ROOT/tech/star_rc/saed32nm_1p9m_Cmin.tluplus"

set MW_POWER_NET        "VDD"
set MW_POWER_PORT       "VDD"
set MW_GROUND_NET       "VSS"
set MW_GROUND_PORT      "VSS"
set MIN_ROUTING_LAYER   "M1"
set MAX_ROUTING_LAYER   "M6"

if { [shell_is_in_topographical_mode] || ($::synopsys_program_name=="icc_shell") } {
    if {![file isdirectory $mw_design_library ]} {
      create_mw_lib   -technology $TECH_FILE \
                      -mw_reference_library $mw_reference_library \
                      $mw_design_library
    } else {
      set_mw_lib_reference $mw_design_library \
        -mw_reference_library $mw_reference_library
    }

    open_mw_lib     $mw_design_library
       set_tlu_plus_files -max_tluplus $TLUPLUS_MAX_FILE \
                      -min_tluplus $TLUPLUS_MIN_FILE \
                      -tech2itf_map $MAP_FILE
}
```

90

```
# - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
#  Library Setup
# - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -

set search_path "$search_path ../ref/db ./unmapped ./scripts ./rtl ./.solutions"

set synthetic_library dw_foundation.sldb
set target_library   "sc_max.db"
set link_library     "* $target_library $synthetic_library"


echo "\n\nSettings:"
echo "search_path:       $search_path"
echo "link_library:      $link_library"
echo "target_library:    $target_library"
```

#### 3.2.2.1.2 Verilog Elaboration

To begin this voyage, the Design Compiler must first dexterously read the Verilog design and decipher the Register Transfer Level (RTL) description of the hardware's behaviour. This sophisticated parsing of the Verilog code enables the tool to build an internal representation of the design, laying the groundwork for subsequent transformations. Hence the common command is used for three different technology process. The Figure 3-3 shows the command that used to read the Verilog file for RISC-V, and it's common as it has no different Verilog code are specified on different technology libraries by the Front-End designer.

```
read_file -format sverilog {/home/user/Jenny/fe/code/adder.sv /home/user/Jenny/fe/code/alu.sv /
home/user/Jenny/fe/code/aludec.sv /home/user/Jenny/fe/code/c_ID_IEx.sv /home/user/Jenny/fe/code/
c_IEx_IM.sv /home/user/Jenny/fe/code/c_IM_IW.sv /home/user/Jenny/fe/code/controller.sv /home/user/
Jenny/fe/code/datapath.sv /home/user/Jenny/fe/code/dmem.sv /home/user/Jenny/fe/code/extend.sv /
home/user/Jenny/fe/code/flopenr.sv /home/user/Jenny/fe/code/flopr.sv /home/user/Jenny/fe/code/
hazardunit.sv /home/user/Jenny/fe/code/ID_IEx.sv /home/user/Jenny/fe/code/IEx_IMem.sv /home/user/
Jenny/fe/code/IF_ID.sv /home/user/Jenny/fe/code/imem.sv /home/user/Jenny/fe/code/IMem_IW.sv /home/
user/Jenny/fe/code/maindec.sv /home/user/Jenny/fe/code/mux2.sv /home/user/Jenny/fe/code/mux3.sv /
home/user/Jenny/fe/code/mux4.sv /home/user/Jenny/fe/code/regfile.sv /home/user/Jenny/fe/code/
riscv_pip_27.sv /home/user/Jenny/fe/code/riscv_pip_27_test.sv /home/user/Jenny/fe/code/
testbench.sv /home/user/Jenny/fe/code/testbenchimem.sv /home/user/Jenny/fe/code/top.sv /home/user/
Jenny/fe/code/topimem.sv}
current_design riscv_pip_27
link
check_design
```

Figure 3-3 Command to read the Verilog file.

#### 3.2.2.1.3 Design Constraint Specification

Specification of design constraints is essential for designs because it ensures that the design fulfils the desired requirements. Constraints can be used to specify the design's timing, area, power consumption, and functionality.

Listed below are a few of the reasons that design constraint specification is crucial:

1. To ensure that the design satisfies the intended specifications: Use constraints to specify the design's timing, area, power, and functionality. This ensures that the design meets the intended specifications and is capable of meeting the end-user's needs.

2. To enhance the design's quality: Constraints can enhance the design's quality by guaranteeing that it is optimally optimized. This can result in a speedier, smaller, and more power-efficient design.
3. To save money and time: Constraints can help save time and money by eliminating the need to re-synthesize the design multiple times. This is due to the fact that constraints can be used to guide the synthesis process and ensure that the design initially fulfils the desired requirements.

The provided constraint file contains various settings that direct the Design Compiler tool during the synthesis process to accomplish particular design objectives and meet timing requirements. Let's examine each setting in detail to determine its function in the Table 3-2.

Table 3-2 Table of the Design Constraint File

| Command | Purpose |
|---|---|
| reset_design | This command resets the current design, ensuring a clean slate before applying the constraints. |
| create_clock -period N [get_ports clk] | This command creates a clock with a period of N units for the port named clk. Which the N is defined with different period clock of time in nanoseconds (ns) SI unit, to get the best performance based on each technology libraries. |
| set_clock_uncertainty -setup 0.1 [get_clocks clk] | This line sets the clock uncertainty for setup timing checks to 0.1 units for the clock clk. The setup uncertainty defines the maximum expected variation in clock arrival time at the flip-flops. |
| set_clock_transition -max 0.05 | This command sets the maximum clock |

| | |
|---|---|
| [get_clocks clk] | transition time to 0.05 units for the clock clk. It represents the maximum expected rise or fall time of the clock signal. |
| set_input_delay -clock clk -max 0.2 [get_ports reset] | This line sets the maximum input delay for the port named reset with respect to the clock clk. It defines the maximum allowed delay for the reset signal to be propagated and captured correctly. |
| set_input_delay -clock clk -max 0.1 [get_ports {InstrF[*] ReadDataM[*]}] | This command sets the maximum input delay for multiple ports that match the patterns InstrF[*] and ReadDataM[*] with respect to the clock clk. It specifies the maximum allowed delay for these input signals to be captured correctly. |
| remove_input_delay [get_ports clk] | This command removes any input delay constraints applied to the clk port. It indicates that the tool should not consider any specific input delay constraints for the clock signal. |
| remove_driving_cell [get_ports clk] | This command removes the driving cell (source) associated with the clk port. It is typically used when the clock is an external signal and not generated within the design. |
| set_output_delay -clock clk -max 0.2 [all_outputs] | This line sets the maximum output delay for all output ports with respect to the clock clk. It specifies the maximum allowed delay for output signals to meet timing requirements. |

| | |
|---|---|
| set_load -max 0.5 [all_outputs] | This command sets the maximum load capacitance to 0.5 units for all output ports. It represents the maximum capacitive load the output can drive while meeting timing constraints. |
| set_max_area 500 | This command sets the maximum allowable chip area to 500 units. It limits the physical area of the synthesized design. |
| set_max_fanout 5 [get_ports -filter direction=~in] | This line sets the maximum fanout (number of gates driven by a single output) to 5 for all output ports (excluding input ports). It controls the load imposed on the output and helps to balance signal strengths. |
| set_max_transition 10 [get_ports -filter direction=~in] | This command sets the maximum allowed output transition time to 10 units for all output ports (excluding input ports). It controls the speed of signal transitions at the outputs. |

These constraint parameters play a critical role in directing the synthesis tool to optimize the design for performance, power, and area while meeting timing requirements. By accurately defining these constraints, designers can create a well-optimized and dependable digital integrated circuit design.

#### 3.2.2.1.4 Compilation, Analysation and Output Generation

After the finalization of the design constraint specifications, the compilation process can be initiated. Once the compilation process is finished, the analysis by utilizing the reports created for timing, area, and power will be proceed. The assessments are

performed on a range of technological processes and varying clock periods, enabling us to evaluate the performance of the design across a variety of scenarios. The reports offer useful insights pertaining to timing violations, area utilization, and power consumption. These insights allow designer to optimize the design and make well-informed selections for various target technologies and clock frequencies. Hence, four commands are needed to be executed as shown in Figure 3-4.

```
compile
report_timing
report_area
report_power
```

Figure 3-4 Commands for Compilation and Analysation

After analysis, the synthesis tool creates an output file with the synthesis findings. This gate-level netlist defines the RISC-V processor's implementation, structure, connection, and timing. The output file is the link between the synthesis tool and the Place and Route (P&R) Designer, and the output file is generated by using the command shows in Figure 3-5 Command for Output File Generation. It allows the P&R Designer to plan and route gates, registers, and interconnections by seamlessly transferring critical design data. The P&R step maps the design into the target chip's physical resources, considering location, routing, power distribution, and signal integrity. Synthesis and P&R work together to fulfil timing, power, area, and signal delay requirements while addressing physical design problems.

The output file handoff signals the transition from logical representation to silicon realization of the RISC-V processor, a major design flow milestone. The output file gives the P&R Designer critical information and preserves logical intent acquired during synthesis. It streamlines design flow by connecting logical synthesis and physical implementation. The seamless output file generation and handoff result in a durable and efficient microprocessor design that excels in modern computing systems.

```
write_file -hierarchy -format ddc -output design_riscv.ddc
```

Figure 3-5 Command for Output File Generation

## 3.3 Conclusion

To summarise, each project has its own set of techniques and approaches for completing it efficiently. To eliminate project constraints, project restrictions and solutions must be offered before the project begins. In this chapter, there are choices for completing the entire project and collecting data as part of the overall strategy. These stages can now be carried out when the hardware and applications have been chosen.

# CHAPTER 4

# RESULTS AND DISCUSSIONS

## 4.1 Introduction

This chapter focuses on presenting the results obtained from the project titled Front End Design (Logic Synthesis) Of RISC-V Processor Using Design Compiler in which various process nodes were utilised to evaluate the performance of the technology. Throughout this study, the initiative investigated how different process nodes affected the system's timing, energy consumption, and physical footprint.

## 4.2 Result and Discussion

### 4.2.1 Generated Cell

The interpretation of the Design Compiler's schematic is a critical step in comprehending the logic structure and relationships between distinct modules in the synthesised design. The schematic depicts the links and layouts of the Verilog files in their compiled version and serves as a graphical representation of the synthesised circuit. The schematic analysis entails a methodical technique to determining the hierarchical organisation of modules, identifying important functional blocks, tracing signal routes, and grasping each module's input and output ports. Furthermore, the analysis includes checking clock and reset connections, identifying logic cells and primitives used in the design, and detecting optimisation techniques and special cells included during the synthesis process. The accuracy of the synthesis technique in translating RTL descriptions into gate-level representations is ensured by cross-referencing the schematic with the original Verilog files. The insights provided through this extensive interpretation contribute greatly to comprehending the

complexities of the synthesised design and enable effective debugging and troubleshooting when necessary.

The schematic with its module hierarchy is represents the synthesised circuit graphically, capturing the links and layouts of the Verilog files in their built form. It provides useful information on the design's structural composition, functional organisation, and signal flow. It permits methodical investigation of the design's architecture due to its hierarchical representation. It also acts as a reference for verification, allowing for comparison with the original Verilog files to assure synthesis accuracy. Overall, the schematic is an essential tool for interpreting the design's intricate relationships and evaluating its integrity.

#### 4.2.1.1 RISC-V

To facilitate its primary functions, the RISC-V module is built with four inputs and four outputs and shown in Figure 4-1. These inputs and outputs are critical to the module's operation.


Figure 4-1 The Schematic of TOP hierarchy of RISCV_PIP_27

A. Inputs:
    a. clk (Clock): The clock input acts as a fundamental timing signal that synchronises the RISC-V module's operations. It regulates the timing of instruction fetching, decoding, and execution, ensuring that each action is carried out at the appropriate clock cycle.

b. reset (Reset): The reset input is a control signal that resets the RISC-V module to its starting state. When asserted, the module is forced to begin executing instructions at a certain address, usually the reset address, resetting all internal registers and state items to their default settings.
c. instrF (Instruction Fetch): The instruction to be fetched from the instruction memory is carried by the instructionF input. It functions as the processor's instruction fetch stage, when the next instruction to be executed is retrieved.
d. ReadDataM (Read Data Memory): The ReadDataM input is used to read data from a data memory. It is used in memory read operations to fetch data from the memory location given in the instruction.

B. Outputs:

a. memwriteM (Memory Write): A control signal that specifies whether or not the module should perform a memory write operation. When asserted, it indicates that data must be written into the specified memory address.
b. The PCF output represents the value of the Programme Counter, which holds the memory address of the next instruction to be fetched from the instruction memory. It is an important component of the processor's instruction fetch stage.
c. WriteDataM (Write Data Memory): The data that needs to be written into the data memory is contained in the WriteDataM output. It is used for memory write operations, which store data in the memory location provided by the instruction.
d. ALUResultM (ALU Result): The ALUResultM output represents the outcome of the Arithmetic Logic Unit's (ALU) arithmetic and logical operations. It contains the results of ALU operations, which can be used in the RISC-V module for data manipulation and processing.

These inputs and outputs are critical to the RISC-V module's overall functionality. The inputs supply critical information and control signals for instruction retrieval, decoding, data manipulation, and memory operations. The outputs, on the other hand, communicate results and control signals that influence the module's following operations and interactions with memory and other external components. The RISC-V module can successfully execute instructions, modify data, and perform other computing tasks by carefully regulating these inputs and outputs.

The RISC-V module is organised hierarchically, with three primary components: the Controller, Datapath, and Hazard Unit as shown in Figure 4-2. Each component is critical to the operation of the RISC-V processor.

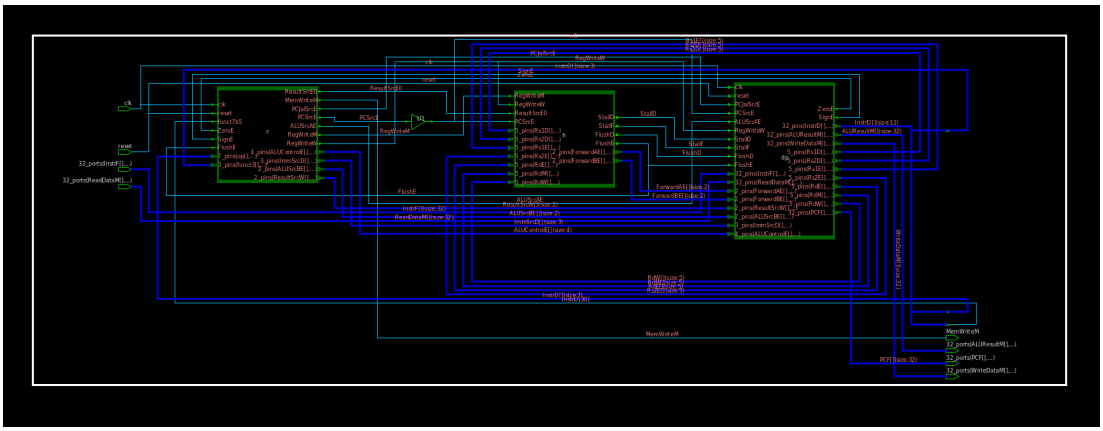

Figure 4-2 The Schematic Low Hierarchy of RISCV_PIP_27

#### 4.2.1.2 Controller

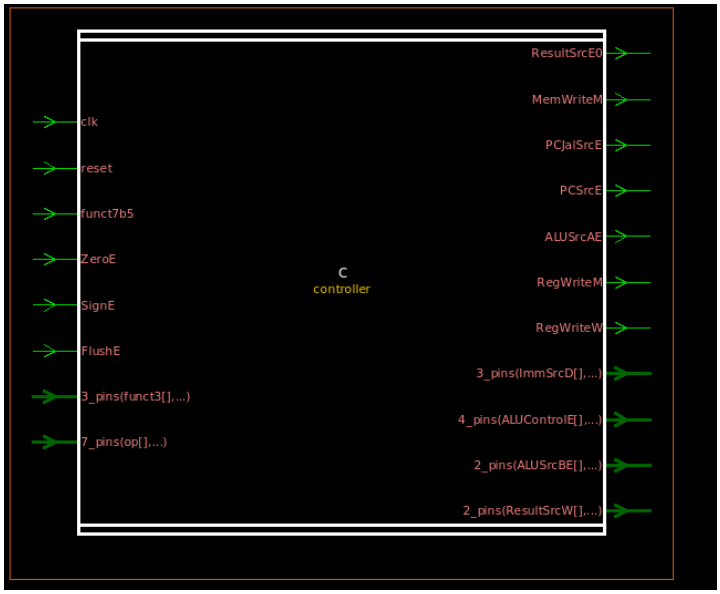


Figure 4-3 Schematic of Controller

The Controller shown in the Figure 4-5 is in charge of arranging instruction execution in the RISC-V processor. It receives instruction inputs, decodes them, and creates control signals that allow the Datapath and other functional units to work together. The Controller directs the flow of data between registers and the ALU (Arithmetic Logic Unit), ensuring that the right sequence of micro-operations is executed.

#### 4.2.1.2.1 Datapath

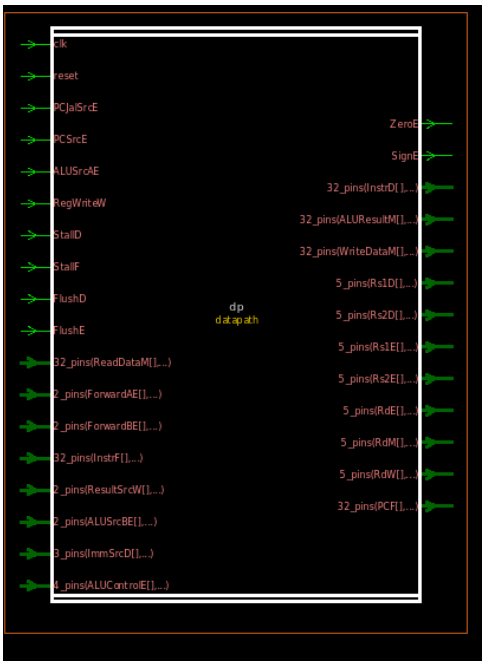


Figure 4-4 Schematic of Datapath

The Datapath is the RISC-V processor's computational core. The schematic is shown in the Figure 4-3. It is made up of several functional units, including registers, ALU, data memory, and instruction memory. The Datapath handles arithmetic and logic operations, as well as data transport and storage. It executes instructions and manipulates data based on control signals supplied by the Controller.

#### 4.2.1.2.2 Hazard Unit

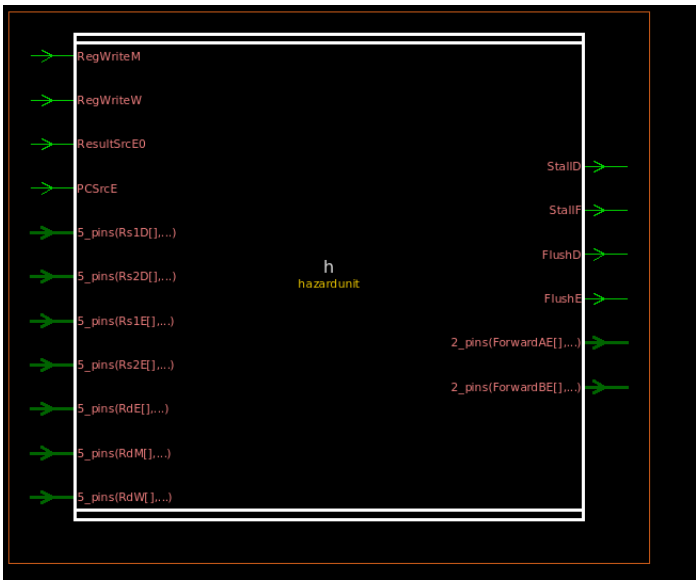


Figure 4-5 Schematic of Hazard Unit

The Hazard Unit as shown in Figure 4-4 is a vital component in the RISC-V pipeline that addresses data and control dangers. It recognises and resolves any conflicts that may develop when instructions in the pipeline rely on the outcomes of other instructions. The Hazard Unit guarantees that data dependencies and control flow are handled correctly, avoiding inaccurate outcomes or unnecessarily delaying the pipeline.

Overall, the hierarchical organisation of the RISC-V module, which includes the Controller, Datapath, and Hazard Unit, promotes efficient instruction execution and data manipulation. The RISC-V processor can perform a wide range of operations by coordinating the activities of these components, making it a powerful and adaptable architecture for varied computing tasks. The Hazard Unit guarantees that the pipeline runs smoothly by resolving any conflicts, which improves the module's overall performance and dependability.

### 4.2.2 Performance Analysis

#### 4.2.2.1 Process Node 90nm

Table 4-1 Table of Performance, Power, and Area Analysis of RISC-V Processor at Various Clock Periods in 90nm Technology

| Period (ns) | Technology | 90 |
|---|---|---|
| 0.5 | report_timing | -4.68 |
| 0.5 | report_timing min | 0.29 |
| 0.5 | report_power | 3.0227E+04 |
| 0.5 | report_area | 23563.92918 |
| 1 | report_timing | -4.16 |
| 1 | report_timing min | 0.29 |
| 1 | report_power | 1.3000E+04 |
| 1 | report_area | 22363.31949 |
| 1.5 | report_timing | -3.66 |
| 1.5 | report_timing min | 0.29 |
| 1.5 | report_power | 1.0283E+04 |
| 1.5 | report_area | 23679.1278 |
| 2 | report_timing | -2.9 |
| 2 | report_timing min | 0.29 |
| 2 | report_power | 6.7481E+03 |
| 2 | report_area | 22263.97921 |
| 3 | report_timing | -1.73 |
| 3 | report_timing min | 0.29 |
| 3 | report_power | 4.8458E+03 |
| 3 | report_area | 23277.42745 |
| 4 | report_timing | -0.88 |

| | | |
|---|---|---|
| 4 | report_timing min | 0.29 |
| 4 | report_power | 3.6970E+03 |
| 4 | report_area | 23559.508 |
| 5 | report_timing | 0 |
| 5 | report_timing min | 0.29 |
| 5 | report_power | 2.5300E+03 |
| 5 | report_area | 22263.97921 |
| 5.5 | report_timing | 0 |
| 5.5 | report_timing min | 0.29 |
| 5.5 | report_power | 2.1917E+03 |
| 5.5 | report_area | 22534.38625 |

The timing characteristics in System on Chip design are significant aspects that have a direct influence on the overall performance of integrated circuits. The timing delay refers to the duration required for signals to propagate over the essential channels within the architecture. The provided data examines the performance of the design throughout various clock cycles for a 90nm technology node as shown in the Table 4-1.

During a time, interval of 0.5 ns, the design exhibits a maximum timing delay of -4.68 ns and a HOLD time of 0.29 ns. This observation suggests that the design possesses a critical path with a signal propagation time of 4.68 ns, rendering it the circuit's most sluggish way. In contrast, the most expeditious route requires a mere 0.29 ns. The substantial disparity seen between the maximum and HOLD times implies the potential existence of obstacles in achieving rigorous timing specifications within the design.

As the duration of the period increases to 1 ns, there is an observed enhancement in the performance of the design. This improvement is evident through a decrease in the maximum timing delay of -4.16 ns, while the HOLD time remains constant at 0.29 ns. This enhancement suggests that the critical path of the design has

been reduced, leading to a decrease in signal propagation time and ultimately resulting in improved operational speed. Furthermore, there is a decrease in power usage to 13000.00 uW, and the design's size experiences a little reduction to 22363.32 units. The aforementioned reductions in power and space have advantageous implications for enhancing energy efficiency and perhaps reducing production costs.

In continuation of the observed pattern, it is noted that at a period of 1.5 ns, the maximum timing delay of the design exhibits a further enhancement of -3.66 ns, whilst the HOLD time stays unaltered at 0.29 ns. This observation illustrates a consistent improvement in performance as the duration of time grows. Additionally, there is a decrease in power usage to 10283.4 microwatts, while the area experiences an increase to 23679.13 units. These modifications demonstrate a favourable balance between power and area in order to enhance overall performance.

At a period of 2 ns, the design exhibits an enhanced maximum timing delay of -2.90 ns, while the HOLD time remains constant at 0.29 ns. This observation highlights the enhanced performance of the design as the period is extended. The power usage exhibits a further decline to 6748.10 microwatts, while the area experiences a little reduction to 22263.98units. The enhancements in power and area dimensions play a significant role in the overall efficiency advancements of the system.

When the period of the design is increased to 3 ns, the maximum timing delay is enhanced to -1.73 ns, while the HOLD time remains unchanged at 0.29 ns. This data demonstrates a consistent pattern of enhanced performance as the duration of time increases. The power consumption exhibits a drop to a value of 4845.80 microwatts, while the area experiences a minor increase to 23277.43 units. The aforementioned measurements demonstrate a positive equilibrium between performance and power efficiency.

At a period of 4 ns, the design exhibits a noteworthy enhancement in its maximum timing delay, decreasing to -0.88 ns, while the HOLD time remains at 0.29 ns. This finding suggests a significant improvement in performance when compared to previous time periods. The power usage exhibits a further decline to 3697.00 microwatts, but the area experiences an increase to 23559.507996 units. These

modifications indicate a compromise between the size of the system and its performance in order to enhance power efficiency.

At a period of 5 ns, the design exhibits a remarkable maximum timing delay of 0 ns, while the HOLD time remains at 0.29 ns. This suggests that the design has reached a significant level of progress in terms of achieving its scheduling criteria. In addition, there is a decrease in power consumption to 2530.00 microwatts, and a little decrease in area to 22263.979205 units. The current design is currently functioning at a period that is close to optimal in terms of both performance and power efficiency.

Ultimately, when the period of 5.5 ns is achieved, the design reaches a critical juncture where the greatest timing delay is reduced to 0 ns. This signifies that all paths within the design successfully satisfy the timing constraints. This indicates that the design has achieved stability and is capable of functioning during this time frame. Furthermore, there is a decrease in power consumption to a value of 2.1917 milliwatts, while the area experiences a decrease to 22534.39 units. The aforementioned results suggest that the design has achieved a state of stability in its operation, demonstrating commendable levels of power and area efficiency.

In summary, it can be observed that an increase in the period results in higher maximum timing delays and decreased power consumption in the design. From the observation, 5ns clock period is the best performance for 90nm. Consequently, this leads to improved performance and energy efficiency. The observed variations in the area of the design may be contingent upon the distinct properties of the circuit and technology employed. In general, the SoC designer is required to meticulously evaluate these trade-offs and make a judicious choice of a suitable timeframe in order to attain the desired equilibrium among performance, power consumption, and area limitations, all in accordance with the individual design prerequisites.

#### 4.2.2.2 Process Node 32nm

Table 4-2 Table of Performance, Power, and Area Analysis of RISC-V Processor at Various Clock Periods in 32nm Technology

| Period (ns) | Technology | 32 |
|---|---|---|
| 0.5 | report_timing | -1.32 |

| | | |
|---|---|---|
| 0.5 | report_timing min | 0.11 |
| 0.5 | report_power | 3.0994E+04 |
| 0.5 | report_area | 34190.42804 |
| 1 | report_timing | -0.79 |
| 1 | report_timing min | 0.11 |
| 1 | report_power | 2.0303E+04 |
| 1 | report_area | 30745.17014 |
| 1.5 | report_timing | -0.25 |
| 1.5 | report_timing min | 0.11 |
| 1.5 | report_power | 1.6898E+04 |
| 1.5 | report_area | 31938.08717 |
| 2 | report_timing | 0 |
| 2 | report_timing min | 0.12 |
| 2 | report_power | 1.4906E+04 |
| 2 | report_area | 29973.71781 |
| 3 | report_timing | 0.51 |
| 3 | report_timing min | 0.12 |
| 3 | report_power | 1.3171E+04 |
| 3 | report_area | 29607.29301 |
| 4 | report_timing | 1.25 |
| 4 | report_timing min | 0.12 |
| 4 | report_power | 1.2326E+04 |
| 4 | report_area | 29606.02097 |
| 5 | report_timing | 1.77 |
| 5 | report_timing min | 0.12 |
| 5 | report_power | 1.1805E+04 |

| | | |
|---|---|---|
| 5 | report_area | 29594.20744 |
| 5.5 | report_timing | 2 |
| 5.5 | report_timing min | 0.12 |
| 5.5 | report_power | 1.1640E+04 |
| 5.5 | report_area | 29589.93577 |

Table 4-2 shows the performance, power, and area analysis of RISC-V processor at various clock periods in 90nm Technology. At a time interval of 0.5 ns, the design exhibits a maximum timing delay of -1.32 ns, while the HOLD time is 0.11 ns. The disparity between the highest and HOLD times serves as an indicator of the design's diversity in propagation time across various pathways. Higher positive numbers are indicative of probable violations in timing limitations. The power usage during this specific period is recorded as 30,994 uW (microWatts), while the design occupies an area of 34190.42804 units.

With a period of 1 ns, the maximum timing delay is enhanced to -0.79 ns, while the HOLD time remains unchanged at 0.11 ns. This observed enhancement demonstrates superior performance in comparison to the preceding time frame. The power usage is observed to decrease to 20,303 uW, while the area experiences a reduction to 30,745.17014 units. The aforementioned decreases in power and area dimensions have a positive impact on energy efficiency and have the ability to reduce production costs.

With a period of 1.5 ns, there is an improvement in the maximum timing delay, which is now -0.25 ns, while the HOLD time remains unchanged at 0.11 ns. This observation suggests a positive correlation between the duration of time and the rate of performance improvement. The power consumption exhibits a drop to a value of 16,898 uW, while the area experiences a minor increase to 31938.09 units. These modifications indicate a harmonious equilibrium between performance and power efficiency.

When the period is set to 2 ns, the maximum timing delay reaches 0 ns, indicating that all paths within the design satisfy the timing criteria. This indicates that the design exhibits stability and is capable of functioning during this particular

time frame. The power consumption exhibits a decrease to a value of 14,906 microWatts, while the area experiences a reduction to 29973.72 units. The aforementioned numbers indicate a state of operational stability characterised by enhanced power and area efficiency.

When the period is set to 3 ns, the maximum timing delay experiences a rise to 0.51 ns, whilst the HOLD time remains constant at 0.12 ns. This suggests that there may be some minor deviations from the specified temporal limits in the design. The power consumption exhibits a drop to a value of 13,171 microWatts, while the area experiences a minor increase to a magnitude of 29,607.29 units. The enhancements in power and area efficiency remain apparent.

When the period is set to 4 ns, the maximum timing delay experiences an increase to 1.25 ns, while the HOLD time remains at 0.12 ns. The aforementioned observation suggests a notable deviation from the temporal limitation, which has a discernible impact on the overall efficacy of the design. The power usage exhibits a decrease to a value of 12326 micro-watts, while the area remains nearly constant at 29606.02 units. The enhancements in power and area efficiency persist.

At a period of 5 ns, the maximum timing delay experiences a further increase to 1.77 ns, whilst the smallest timing delay remains at 0.12 ns. The breach of the timing limitation exacerbates during this particular period. The power usage exhibits a drop to a value of 11,850 microWatts, while the area experiences a minor increase to 29594.21 units. Although there have been advancements in power efficiency, the design's performance is being adversely affected by timing violations.

When the period is reduced to 5.5 ns, the maximum timing delay is enhanced to 2 ns, while the HOLD time remained as 0.12ns. The power consumption exhibits a decrease to a value of 11640.00 microWatts, while the area experiences a reduction to 29589.94 units. Notwithstanding the enhanced power efficiency, the presence of significant timing violations renders this timeframe unfeasible for achieving steady operation.

In summary, 2ns of clock period for 32nm is the best performance. In general, while doing a comprehensive analysis of the data on a process-by-process basis, it becomes apparent that a rise in the time period results in a deterioration of the maximum timing delay, hence resulting in violations of timing constraints. Although

there is a general decrease in power consumption and variations in the area, these enhancements in power and area efficiency are insufficient to offset the significant time violations. The selection of a suitable period by the designer necessitates a meticulous consideration of the trade-off between performance and time requirements, all the while taking into account the limitations imposed by power and space limits. Ensuring the stability, dependability, and overall efficiency of the design is of utmost importance in VLSI-based systems.

#### 4.2.2.3 Process Node 14nm

Table 4-3 Table of Performance, Power, and Area Analysis of RISC-V Processor at Various Clock Periods in 14nm Technology

| Period (ns) | Technology | 14 |
|---|---|---|
| 0.5 | report_timing | -0.29 |
| 0.5 | report_timing min | 0.03 |
| 0.5 | report_power | 2.2004E+03 |
| 0.5 | report_area | 9059.954187 |
| 1 | report_timing | 0 |
| 1 | report_timing min | 0.03 |
| 1 | report_power | 1.0880E+03 |
| 1 | report_area | 8731.444541 |
| 1.5 | report_timing | 0.35 |
| 1.5 | report_timing min | 0.03 |
| 1.5 | report_power | 7.1462E+02 |
| 1.5 | report_area | 8892.319228 |
| 2 | report_timing | 0.6 |
| 2 | report_timing min | 0.03 |
| 2 | report_power | 5.4206E+02 |

| | | |
|---|---|---|
| 2 | report_area | 8890.311888 |
| 3 | report_timing | 1.1 |
| 3 | report_timing min | 0.03 |
| 3 | report_power | 3.6883E+02 |
| 3 | report_area | 8893.861697 |
| 4 | report_timing | 1.6 |
| 4 | report_timing min | 0.03 |
| 4 | report_power | 2.8275E+02 |
| 4 | report_area | 8893.116994 |
| 5 | report_timing | 2.1 |
| 5 | report_timing min | 0.03 |
| 5 | report_power | 2.3035E+02 |
| 5 | report_area | 8895.177195 |
| 5.5 | report_timing | 2.35 |
| 5.5 | report_timing min | 0.03 |
| 5.5 | report_power | 2.1116E+02 |
| 5.5 | report_area | 8895.426001 |

The performance, power, and area analysis of RISC-V processor at various clock periods in 90nm Technology are tabulated in Table 4-3. With a time period of 0.5 ns and a technology node of 14 nanometres, the design demonstrates a negative report timing of -0.29 ns, signifying its compliance with the timing specifications. The minimal report timing, denoted as rt-min, is measured at 0.03 ns, indicating a limited timing margin. The power usage is measured to be 2,200.4 microWatts (uW), while the area is determined to be 9059.954187 square units.

When the period is reduced to 1 ns, the report timing is observed to be 0 ns, suggesting that the design satisfies its timing criteria with more ease compared to a

period of 0.5 ns. The power consumption exhibits a decrease to a value of 1,088 uW, while the area experiences a reduction to 8,731.444541 square units.

With a period of 1.5 ns, the timeliness of the report is enhanced to 0.35 ns, resulting in a drop in power consumption to 714.6184 uW. The area experiences a marginal increase to 8892.319228 square units. The design exhibits superior performance and enhanced energy economy throughout this time.

When the period is reduced to 2 ns, the report timing demonstrates an improvement of 0.6 ns, while the power consumption reduces to a value of 542.0613 uW. The area has a minimal variation and is measured at 8890.311888 square units. As the duration extends, the design consistently exhibits enhanced performance and improved energy economy.

When the period is reduced to 3 ns, the report timing experiences an increase to 1.1 ns. This suggests that the design continues to satisfy its timing requirements, but with a greater margin for timing. The power consumption exhibits a drop to a value of 368.8288 microWatts, while the area experiences a tiny increase to 8893.861697 square units.

At a period of 4 ns, the report timing exhibits a notable increase to 1.6 ns, indicating a subsequent augmentation in the timing margin. The power consumption exhibits a decline to a value of 282.7517 microWatts, while the area, remains relatively constant at approximately 8893.116994 square units.

When the period is reduced to 5 ns, the report timing experiences a rise to 2.1 ns, but the power consumption undergoes a decrease to 230.3470 uW. The area occupying experiences a marginal growth to a value of 8895.177195 square units. The design consistently fulfills its timing requirements, although with a wider timing margin, and exhibits commendable power economy.

At a period of 5.5 ns, the timing for the report experiences a further increase to 2.35 ns, while the power consumption demonstrates a notable increase to 8895.426001 microWatts. The area exhibits a significant drop to a value of 211.1597 square units. Although the design is now satisfying its timing requirements, the timing margin has become significantly large, and the power consumption has noticeably increased. These observations suggest that the current state of the design may not be suitable for steady operation.

In summary, the analysis of the Table 4-3 provides insights into the performance, power efficiency, and area attributes of the VLSI design implemented using a 14 nm technology node over various clock periods. The best performance of 14nm is during 1ns clock period. As the duration of the period rises, the design exhibits enhanced timing performance and energy economy, thereby illustrating the inherent trade-offs between performance and power consumption. Nevertheless, it is imperative to meticulously choose a suitable timeframe that aligns with particular criteria in order to achieve optimal equilibrium between performance, power efficiency, and area utilization in Very Large-Scale Integration (VLSI) designs.

#### 4.2.2.4 Comparison of RISC-V Module between Process Node 90nm, 32nm and 14nm

Table 4-4 Table of combination of the three process nodes with varies period.

| Period (ns) | Technology | 14 | 32 | 90 |
|---|---|---|---|---|
| 0.5 | report_timing | -0.29 | -1.32 | -4.68 |
| | report_timing min | 0.03 | 0.11 | 0.29 |
| | report_power | 2.2004E+03 | 3.0994E+04 | 3.0227E+04 |
| | report_area | 9059.954187 | 34190.42804 | 23563.92918 |
| 1 | report_timing | 0 | -0.79 | -4.16 |
| | report_timing min | 0.03 | 0.11 | 0.29 |
| | report_power | 1.0880E+03 | 2.0303E+04 | 1.3000E+04 |
| | report_area | 8731.444541 | 30745.17014 | 22363.31949 |
| 1.5 | report_timing | 0.35 | -0.25 | -3.66 |
| | report_timing min | 0.03 | 0.11 | 0.29 |

| | | | | |
|---|---|---|---|---|
| | report_power | 7.1462E+02 | 1.6898E+04 | 1.0283E+04 |
| | report_area | 8892.319228 | 31938.08717 | 23679.1278 |
| 2 | report_timing | 0.6 | 0 | -4.63 |
| | report_timing min | 0.03 | 0.12 | 0.29 |
| | report_power | 5.4206E+02 | 1.4906E+04 | 6.7481E+03 |
| | report_area | 8890.311888 | 29973.71781 | 22263.97921 |
| 3 | report_timing | 1.1 | 0.51 | -1.73 |
| | report_timing min | 0.03 | 0.12 | 0.29 |
| | report_power | 3.6883E+02 | 1.3171E+04 | 4.8458E+03 |
| | report_area | 8893.861697 | 29607.29301 | 23277.42745 |
| 4 | report_timing | 1.6 | 1.25 | -0.88 |
| | report_timing min | 0.03 | 0.12 | 0.29 |
| | report_power | 2.8275E+02 | 1.2326E+04 | 3.6970E+03 |
| | report_area | 8893.116994 | 29606.02097 | 23559.508 |
| 5 | report_timing | 2.1 | 1.77 | 0 |
| | report_timing min | 0.03 | 0.12 | 0.29 |
| | report_power | 2.3035E+02 | 1.1805E+04 | 2.5300E+03 |
| | report_area | 8895.177195 | 29594.20744 | 22263.97921 |
| 5.5 | report_timing | 2.35 | 2 | 0 |
| | report_timing min | 0.03 | 0.12 | 0.29 |
| | report_power | 2.1116E+02 | 1.1640E+04 | 2.1917E+03 |

| | | | | |
|---|---|---|---|---|
| | report_area | 8895.426001 | 29589.93577 | 22534.38625 |

Table 4-5 Table of Area for three process nodes with varies period.

| Period(ns) | 90nm | 32nm | 14nm |
|---|---|---|---|
| 0.5 | 23563.92918 | 34190.42804 | 9059.954187 |
| 1 | 22363.31949 | 30745.17014 | 8731.444541 |
| 1.5 | 23679.1278 | 31938.08717 | 8892.319228 |
| 2 | 22263.97921 | 29973.71781 | 8890.311888 |
| 3 | 23277.42745 | 29607.29301 | 8893.861697 |
| 4 | 23559.508 | 29606.02097 | 8893.116994 |
| 5 | 22263.97921 | 29594.20744 | 8895.177195 |
| 5.5 | 22534.38625 | 29589.93577 | 8895.426001 |

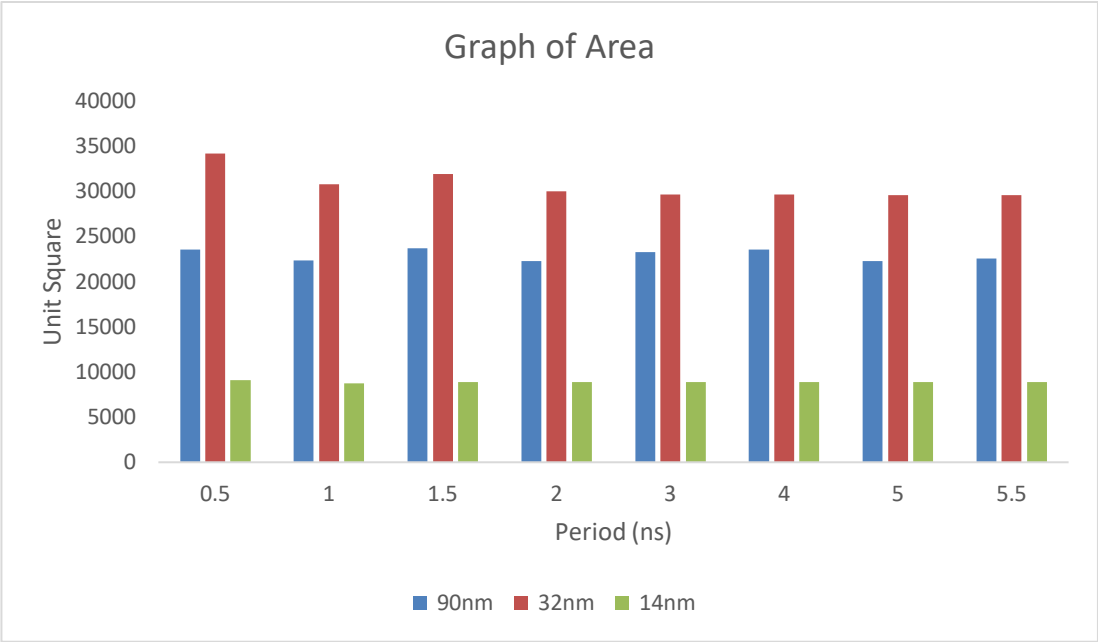


Figure 4-6 The graph of the Area for three process nodes with varies period.

In this analysis, a comparative examination of the table provided in Table 4-5 and Figure 4-6, which displays diverse VLSI designs implemented using multiple technology nodes, namely 90 nm, 32 nm, and 14 nm, across various clock periods. The table presents the quantitative values denoting the area, measured in square units, that is occupied by each design throughout each clock period. In this study, we want to examine the patterns and consequences of the allocation of space in relation to three distinct technology nodes.

During a time interval of 0.5 nanoseconds, it is observed that the design utilizing the largest technology node (90 nm) exhibits the most substantial spatial occupation, measuring 23563.92918 square units. Subsequently, the design employing the 32 nm node occupies a higher area of 34190.42804 square units, while the design employing the smallest technology node (14 nm) demonstrates the least spatial occupation, measuring 9059.954187 square units.

The observed pattern persists across all time intervals, wherein designs including larger technology nodes consistently exhibit greater spatial occupation compared to those with smaller nodes.

In the 90 nm technology node, it is seen that the area exhibits fluctuations in response to changes in the period, suggesting that the design's resource consumption is subject to variation at different clock frequencies. The observed variance can be attributed to the distinct layout requirements and design limitations that were present throughout each respective period.

In the context of the 32 nm technology node, there is a discernible pattern of diminishing area as the period increases. This observation implies that as clock frequencies increase, the architecture gets more compact and efficient. The observed decline in area suggests the possibility of implementing design optimizations in order to enhance the utilization of available space.

In the context of the 14 nm technology node, it is observed that the area exhibits a declining pattern as the periods increase, mirroring the behaviour observed in the 32 nm node. The design that employs the smallest technological node constantly exhibits superior characteristics in terms of compactness in layout and efficient utilization of room.

The utilization of area in designs employing smaller technological nodes, specifically those with 32 nm and 14 nm, constantly exhibits greater efficiency when compared to designs employing the 90 nm node. This discovery is consistent with the benefits associated with lower technology nodes in relation to transistor scaling and resource density.

The 32 nm and 14 nm designs exhibit a decline in area as the period increases, suggesting the possibility of additional area optimization at higher clock frequencies. Further investigation could be conducted into advanced architectural and layout optimizations in order to attain enhanced levels of consistent and predictable area use. The design utilizing the 32 nm technology node demonstrates greater space demands in comparison to the other designs. Nevertheless, the increased size of this particular region may necessitate a compromise in terms of enhanced speed or usefulness in certain applications. In summary, while 90nm technology is expected to occupy more space in theory, practical data analysis shows that 32nm technology utilizes the largest area. This is due to the tool's preference for larger cells to achieve desired timing performance. The relationship between timing, area, and power remains a key consideration in SoC designs, where optimizing design choices and striking the right balance is essential to achieve an efficient RISC-V processor design.

In summary, the examination of space use in VLSI designs across various technology nodes and clock periods underscores the influence of technology scaling on chip area. In general, the utilization of smaller technological nodes tends to yield designs that are more compact and efficient in terms of area utilization. Conversely, the adoption of larger nodes may necessitate greater area allocations. Based on the available data, it can be inferred that the design with the smallest technological node (14 nm) consistently exhibits superior area usage efficiency throughout various clock periods. However, it is crucial to thoroughly evaluate the selection of the technological node and prioritize area optimization, taking into account the precise demands of the application. The utilization of advanced design approaches and layout techniques has the potential to significantly augment area efficiency, hence facilitating the development of more potent and compact Very Large-Scale Integration (VLSI) systems in the forthcoming years.

Table 4-6 Table of Power for three process nodes with varies period.

| Period(ns) | 90nm | 32nm | 14nm |
|---|---|---|---|
| 0.5 | 30227.3 | 30994 | 2200.4 |
| 1 | 13000 | 20303 | 1088 |
| 1.5 | 10283.4 | 16898 | 714.6184 |
| 2 | 6748.1 | 14906 | 542.0613 |
| 3 | 4845.8 | 13171 | 368.8288 |
| 4 | 3697 | 12326 | 282.7517 |
| 5 | 2530 | 11805 | 230.347 |
| 5.5 | 2191.7 | 11640 | 211.1597 |

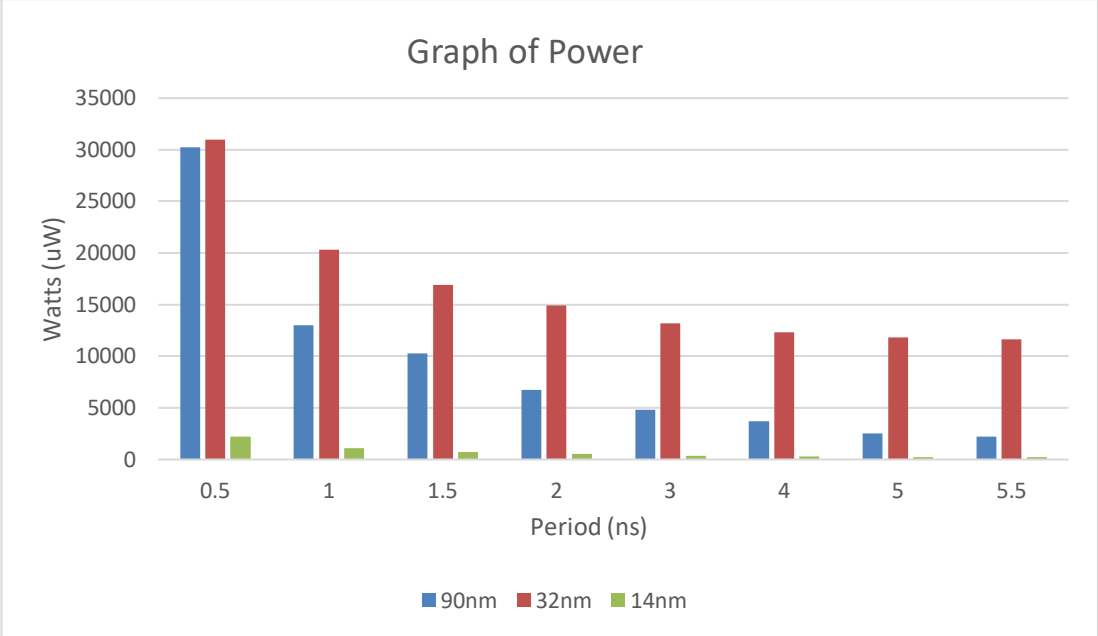


Figure 4-7 The graph of the Power for three process nodes with varies period.

The given table shows in Table 4-6 and Figure 4-7 compares three distinct VLSI designs with differing technology nodes (90 nm, 32 nm, and 14 nm) at varying clock frequencies. In microwatts (uW), the data in the table represents the power consumption of each design during each clock period. The energy efficiency and performance characteristics of these designs can be better comprehended by analysing the power consumption trends for each technology node.

The significant impact of the technology node on power consumption is one of the important observations. In general, the VLSI design utilizing the largest technology node of 90 nm has the medium power consumption across all clock periods, while the design which having the maximum power consumption is utilizing the 32 nm node. In contrast, the design with the tiniest technology node of 14 nm exhibits the lowest power consumption across all clock periods. This trend is consistent with the well-known benefits of shrinking technology nodes, such as reduced leakage current and enhanced transistor performance, which result in decreased power dissipation.

The data also reveal a significant decrease in power consumption as the clock period increases. This pattern is observable across all three technological nodes. As the clock period increases, the quantity of processing and computation performed per clock cycle decreases, resulting in a decrease in dynamic power consumption. Higher clock frequencies (shorter periods) are associated with increased power dissipation, whereas lower clock frequencies (longer periods) promote energy efficiency.

The data on power consumption highlights the trade-offs that designers must consider when selecting a technology node for a VLSI layout. Larger technology nodes, such as 90 nm, may offer improved functionality and performance, but at the expense of increased power consumption. Smaller technology nodes, such as 14 nm, enable designs that are suitable for applications with stringent energy constraints, such as mobile devices and battery-powered electronics.

According to the data, all three designs may have room for power optimization. While the 14 nm design already consumes the least amount of energy, the 90 nm and 32 nm designs could benefit from power optimization techniques. Strategies for power optimization may include architectural optimizations, voltage

scaling, clock gating, and more efficient resource utilization. These methods could help improve energy efficiency without sacrificing performance.

As technology continues to advance, compact technology nodes and novel power optimization techniques will likely play a crucial role in VLSI design. The relentless pursuit of smaller transistors and advanced fabrication techniques bears the promise of reduced power consumption and enhanced performance. Emerging technologies, such as low-power design methodologies, heterogeneous computing, and specialized hardware accelerators, provide intriguing opportunities for increasing the power efficiency of VLSI designs.

In conclusion, the power consumption analysis of VLSI designs with various technology nodes and clock periods demonstrates the significant effect of technology scaling on power efficiency. Smaller technology nodes reduce power consumption, making them optimal for energy-sensitive applications. When selecting a technology node for a VLSI design, it is essential to carefully balance performance requirements and power constraints, as illustrated by the power consumption trends. With continued research and innovation, the future of VLSI design holds great promise for attaining greater levels of energy efficiency and performance, revolutionizing the landscape of electronic devices and systems even further.

Table 4-7 Table of Timing (SETUP) for three process nodes with varies period.

| Period(ns) | 90nm | 32nm | 14nm |
|---|---|---|---|
| 0.5 | -4.68 | -1.32 | -0.29 |
| 1 | -4.16 | -0.79 | 0 |
| 1.5 | -3.66 | -0.25 | 0.35 |
| 2 | -2.90 | 0 | 0.6 |
| 3 | -1.73 | 0.51 | 1.1 |
| 4 | -0.88 | 1.25 | 1.6 |

| | | | |
|---|---|---|---|
| 5 | 0 | 1.77 | 2.1 |
| 5.5 | 0 | 2 | 2.35 |

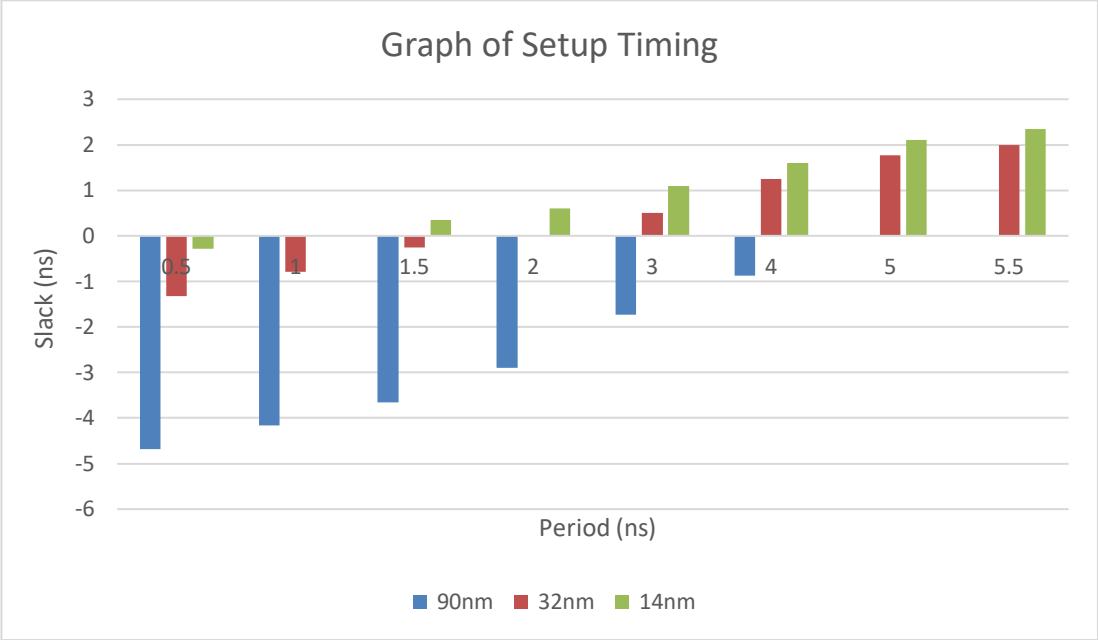


Figure 4-8 The graph of Timing (SETUP) for three process nodes with varies period.

The given Table 4-7 and Figure 4-8 compares three distinct VLSI designs with differing technology nodes (90 nm, 32 nm, and 14 nm) at varying clock frequencies and shows the trend. In nanoseconds (ns), the data in the table represents the timing latencies of each design at each clock period. The performance characteristics and timing constraints of these designs can be better understood by analysing the timing data for each technology node.

The data elucidates the significant impact of the technology node on the timing performance of VLSI designs. As the technology node shrinks from 90 nm to 14 nm, timing delays resolve and become increasingly negative. This trend indicates that designs with smaller technology nodes have quicker signal propagation and fewer delays, which contribute to enhanced performance.

At a period of 0.5 ns, both 90 nm and 32 nm technology node designs exhibit negative timing delays, indicating that they satisfy their timing requirements. However, the design utilizing the 14 nm technology node exhibits a marginally

positive timing delay (0.29 ns), indicating that it may not satisfy the timing constraints at this time.

As the clock period increases, the timing latencies of all three designs improve. For the 14 nm design, the negative timing delays (indicating compliance with timing constraints) become more pronounced. The 14 nm design obtains negative timing delays at 1 ns and beyond, indicating its stability and ability to meet timing requirements at those periods.

The data emphasizes the significance of selecting a suitable clock period for a VLSI design. Shorter clock periods (e.g., 0.5 ns) enable quicker data processing, but may result in more difficult timing constraints and potential design complexity. Alternatively, extended clock periods (e.g., 5 ns) provide more relaxed timing requirements, potentially simplifying the design at the expense of slower data processing rates.

For optimal design solutions, designers must carefully balance performance requirements and timing constraints. Techniques for timing optimization, such as pipelining, retiming, and clock skew adjustments, can be used to assure stable and efficient operation across multiple clock periods. As technology nodes continue to reduce and clock frequencies increase, timing becomes an essential component of VLSI design. Advanced technologies make achieving precise timing closure and maintaining stability in all operating conditions more difficult.

To overcome these obstacles, designers will require sophisticated EDA tools, static timing analysis, and timing-driven layout methodologies. In addition, advancements in clock distribution and synchronization techniques will be essential for ensuring timing performance reliability in complex VLSI designs.

In conclusion, the timing data analysis of VLSI designs with various technology nodes and clock periods demonstrates the significance of technology scaling in timing performance. Smaller technological nodes result in quicker signal propagation and reduced timing delays, thereby enhancing overall performance. When choosing a technology node and clock period, however, designers must weigh the trade-offs between performance, timing constraints, and design complexity. Timing optimization and closure will continue to be essential aspects of VLSI design as technology advances. To meet the timing challenges presented by shrinking

technology nodes and higher clock frequencies, continued research and innovation in design methodologies and EDA tools will be necessary. To deliver cutting-edge VLSI designs that fuel the next generation of electronic devices and systems, it will be essential to strike a balance between performance, power efficiency, and timing requirements.

## 4.3 Conclusion

The comparison and analysis of the three tables containing VLSI designs with distinct technology nodes (90 nm, 32 nm, and 14 nm) and varying clock periods yields a number of noteworthy conclusions. Smaller technology nodes, such as 32 nm and 14 nm, consistently exhibit superior power efficiency and area utilization compared to designs utilizing a larger technology node, such as 90 nm. The 14 nm design with 1ns clock period exhibits the most effective area utilization, demonstrating the advantages of decreasing technology nodes for achieving compact layouts. Choosing a technology node requires careful consideration of the trade-offs between performance, power consumption, and area utilization. Smaller technology nodes also improve timing performance, necessitating precise timing optimization across all clock periods. Future advances in technology scaling, power optimization, and timing closure will continue to be the primary focus of VLSI design, creating opportunities for the development of more potent and energy-efficient electronic devices and systems. In order to obtain optimal VLSI design solutions, the choice of technology node should ultimately align with the specific requirements of the application.

# CHAPTER 5

# CONCLUSIONS AND RECOMMENDATIONS

## 5.1 Conclusions

The exhaustive analysis of the three tables comparing VLSI designs with varying technology nodes (90 nm, 32 nm, and 14 nm) at various clock periods has yielded valuable insights regarding their performance, power efficiency, and area utilization. The design and efficacy of System-on-Chip (SoC) and VLSI circuits are directly influenced by the relationship between these three fundamental factors: time, power, and area.

The timing performance of a VLSI design is the time required for signals to propagate through the circuit's critical channels. Due to shorter gate lengths and reduced parasitic effects, smaller technology nodes, such as 32 nm and 14 nm, provide faster switching velocities by nature. This results in enhanced timing performance, as demonstrated by the negative timing latencies observed in Table 4-7 especially on 32nm and 90nm technology nodes, indicating that these designs meet or exceed their timing requirements. In contrast, the design in with 90nm technology process nodes, exhibits slightly larger positive timing delays, which may indicate that it is more difficult to meet timing constraints during specific clock periods. As the size of technology nodes decreases, achieving timing closure becomes more difficult, necessitating advanced timing optimization techniques to resolve violations and ensure stable operation.

Modern SoC and VLSI design must take power consumption into account, particularly for battery-powered devices and power-constrained systems. In general, smaller technology nodes consume less energy, as evidenced by the progressively lower power values in Table 4-6 with 14nm and 32nm technology nodes. The larger 90 nm technology node utilizes the most energy during all clock periods. This improvement in power efficiency is attributable to reduced gate capacitances and leakage currents, which result in energy savings during switching operations. Future

power optimization research may concentrate on voltage scaling, clock gating, and low-power design methodologies in order to increase the power efficiency of VLSI devices.

The area occupied by a VLSI design has a significant effect on the size, cost, and manufacturability of the device. Smaller technology nodes permit greater transistor densities, resulting in more compact and resource-effective layouts. As seen in Table 4-5, designs with reduced technology nodes exhibit superior area utilization, demonstrating the advantages of scaling down technology nodes. The largest 90 nm technology node, consistently occupies the most area, underscoring the trade-off between performance and area requirements. Future research in VLSI design could concentrate on area reduction strategies, advanced place-and-route algorithms, and architectural optimizations to achieve even greater area utilization efficiency and uniformity.

In SoC and VLSI design, the relationship between time, power, and area is intricate and interdependent. Due to faster switching velocities and lower energy consumption per operation, smaller technology nodes contribute to enhanced timing performance and power efficiency. Nevertheless, these advantages may be accompanied by increased design complexity and the possibility of timing constraint violations. When selecting the appropriate technology node for a specific application, designers must carefully consider the trade-offs between performance, power consumption, and area utilization. These factors must be optimized in order to achieve a well-balanced design that meets the intended performance requirements, minimizes power consumption, and maximizes the available chip area.

In conclusion, the analysis of the supplied tables highlights the substantial effect of scaling technology has on the relationship between time, power, and area in SoC and VLSI circuits. Smaller technology nodes provide enhanced timing performance, power efficiency, and area utilization, making them an attractive option for high-performance and power-constrained applications. As technology progresses, designers must continue to innovate and explore advanced design methodologies and optimization techniques to unleash the full potential of smaller technology nodes while addressing the design challenges they may present. The constant evolution of SoC and VLSI design will propel advancements in numerous industries and influence the future of electronic devices and systems.

## 5.2 Recommendations for future work

A further topic that merits investigation is dynamic frequency scaling, a technique that involves the dynamic adjustment of the clock frequency in accordance with the workload and performance demands of the system. The implementation of dynamic frequency scaling algorithms has the potential to achieve power savings during periods of reduced computing demand, while also ensuring optimal performance during peak workloads.

In addition, it is imperative to address clock domain crossover (CDC) analysis and synchronisation in multi-clock domain architectures in order to uphold data integrity and prevent the occurrence of metastability concerns. Conducting research in this particular field has the potential to yield significant contributions to the approaches employed by the Centres for Disease Control and Prevention (CDC), thereby enhancing the strength and dependability of intricate designs.

In addition to traditional design techniques, the emergence of new technologies offers promising prospects for breakthroughs in Very Large-Scale Integration (VLSI). The investigation of neuromorphic computing, quantum computing, and photonic computing has the potential to expand the possibilities of integrated circuits, enabling them to achieve higher performance levels while consuming less energy.

In addition, the use of machine learning algorithms into Very Large-Scale Integration (VLSI) design has the potential to enhance and optimise diverse design procedures, leading to the development of chip designs that are characterised by improved efficiency and reliability. Machine learning methodologies can be utilised to perform several tasks, including timing analysis, power optimisation, layout generation, and problem identification. These applications contribute to the improvement of design productivity and accuracy.

With the rising complexity of VLSI designs, ensuring security and dependability has emerged as a critical priority. The pursuit of research in hardware security mechanisms, fault tolerance, and resilience against hardware attacks is of utmost importance in order to protect sensitive data and maintain continuous operation of vital systems.

In conclusion, the outcome analysis presents a thorough examination of the intricacies and difficulties encountered in Very Large-Scale Integration (VLSI) design. Potential areas for future improvement and research include the development of more sophisticated timing optimisation methods, the use of power-efficient techniques, the utilisation of strategies to reduce area requirements, the exploration of dynamic frequency scaling approaches, the investigation of upcoming technologies, the integration of machine learning methodologies, and a heightened focus on ensuring security and dependability. By focusing on these specific domains, the field of VLSI design can persistently advance, hence expanding the limits of performance, efficiency, and functionality in contemporary integrated circuits. Consequently, this progress will drive the future technological advancements.

# REFERENCES


[1] A. Bindal, *Fundamentals of Computer Architecture and Design*. 2017.

[2] F. Merchant, D. Sisejkovic, L. M. Reimann, K. Yasotharan, T. Grass, and R. Leupers, "ANDROMEDA: An FPGA Based RISC-V MPSoC Exploration Framework," *Proc. IEEE Int. Conf. VLSI Des.*, vol. 2021-Febru, pp. 270–275, 2021, doi: 10.1109/VLSID51830.2021.00051.

[3] R. Kwan, *Computer systems*, vol. 50, no. 11. 2012.

[4] A. S. Waterman, "Design of the RISC-V Instruction Set Architecture," p. 67, 2016, [Online]. Available: https://escholarship.org/uc/item/98384265.

[5] A. Kamaleldin, M. Ali, P. Amini Rad, M. Gottschalk, and D. Gohringer, "Modular memory system for risc-v based mpsocs on xilinx fpgas," *Proc. - 2019 IEEE 13th Int. Symp. Embed. Multicore/Many-Core Syst. MCSoC 2019*, pp. 68–73, 2019, doi: 10.1109/MCSoC.2019.00017.

[6] A. Waterman and D. A. Patterson, "The RISC-V Instruction Set Manual Volume II : Privileged Architecture Version 1 . 9 . 1," vol. II, 2016.

[7] A. Zelensky, A. Alepko, V. Dubovskov, and V. Kuptsov, "Heterogeneous neuromorphic processor based on RISC-V tasks," no. September 2020, 2021, doi: 10.1117/12.2574470.

[8] M. Cococcioni, F. Rossi, E. Ruffaldi, and S. Saponara, "Faster deep neural network image processing by using vectorized posit operations on a RISC-V processor," vol. 1173604, no. April, 2021, doi: 10.1117/12.2586565.

[9] E. Alon, K. Asanović, J. Bachrach, B. Nikolić, and R. Isa, "Invited : Open-Source EDA Tools and IP , A View from the Trenches," pp. 10–12, doi: 10.1145/3316781.3323481.

[10] G. Liu, J. Primmer, and Z. Zhang, "Rapid Generation of High-Quality RISC-V Processors from Functional Instruction Set Specifications," pp. 1–6, 2019.

[11] S. Di Mascio, A. Menicucci, and E. Gill, "Leveraging the Openness and Modularity of RISC-V in Space," vol. 16, no. 11, pp. 454–472, 2019, doi: 10.2514/1.I010735.

[12] L. Morais, V. Silva, A. Goldman, M. Frank, and G. Araujo, "Adding Tightly-Integrated Task Scheduling Acceleration to a RISC-V Multi-core Processor," 2019, doi: 3352460.3358271.

[13] D. J. Greaves, "System on Chip Design and Modelling," no. C, 2011.

[14] A. Ishtiaq, M. U. Khan, S. Z. Ali, and K. Habib, "A Review of System on Chip ( SOC ) Applications in Internet of Things ( IOT ) and A Review of System on Chip ( SOC ) Applications in Internet of Things ( IOT ) and Medical," no. September, 2021.

[15] D. Sheng, H. R. Lin, and L. Tai, "Low-process–voltage–temperature-sensitivity multi-stage timing monitor for system-on-chip applications," *Electron.*, vol. 10, no. 13, 2021, doi: 10.3390/electronics10131587.

[16] R. Saito, C. L. Ayala, O. Chen, T. Tanaka, T. Tamura, and N. Yoshikawa,

"Logic synthesis of sequential logic circuits for adiabatic quantum-flux-parametron logic," *IEEE Trans. Appl. Supercond.*, vol. 31, no. 5, 2021, doi: 10.1109/TASC.2021.3061636.

[17] A. Datta *et al.*, "Design-synthesis co-optimisation using skewed and tapered gates," *Proc. 2016 Des. Autom. Test Eur. Conf. Exhib. DATE 2016*, pp. 1144–1147, 2016, doi: 10.3850/9783981537079_0310.

[18] I. Synopsys, "SAED 14nm FinFET Generic Liraries," 2020.

[19] I. Synopsys, "SAED_32/28nm Digital Standard Cell Library," *SYNOPSYS Armen. Educ. Dep. Rev.*, 2012, [Online]. Available: https://www.synopsys.com/academic-research/university.html.

[20] S. E. D. K. Core, "SAED_EDK90_CORE-90nm Digital Standard Cell Library Digital Standard Cell Library SAED_EDK90_CORE DATABOOK Revision : 1.4 Technology : SAED90nm Process : SAED90nm 1P9M 1.2v / 2.5v SAED_EDK90_CORE-90nm Digital Standard Cell Library," pp. 1–100, 2008, Accessed: Jul. 30, 2023. [Online]. Available: http://web.engr.oregonstate.edu/~traylor/ece474/reading/SAED_Cell_Lib_Rev1_4_20_1.pdf.

[21] "University Software Program | SARA." https://www.synopsys.com/academic-research/university.html (accessed Mar. 25, 2023).

[22] D. Kraak *et al.*, "Degradation analysis of high performance 14nm finfet SRAM," *Proc. 2018 Des. Autom. Test Eur. Conf. Exhib. DATE 2018*, vol. 2018-Janua, pp. 201–206, 2018, doi: 10.23919/DATE.2018.8342003.

[23] R. Hajare and C. Lakhminarayana, "Design and Evaluation of FinFET based SRAM Cells at 22nm and 14nm Node Technologies," *Int. J. Comput. Appl.*, vol. 171, no. 6, pp. 26–31, 2017, doi: 10.5120/ijca2017915005.

[24] V. S. Melikyan *et al.*, "The Overshoot Reducing Method in Voltage Regulators in SAED 14nm FinFet Technology," *2019 IEEE 39th Int. Conf. Electron. Nanotechnology, ELNANO 2019 - Proc.*, pp. 106–109, 2019, doi: 10.1109/ELNANO.2019.8783708.

[25] V. Melikyan, S. Harutyunyan, A. Khachatryan, and H. Harutyunyan, "A Novel Voltage Mode High Speed Sense Amplifier," *2019 IEEE 39th Int. Conf. Electron. Nanotechnology, ELNANO 2019 - Proc.*, pp. 120–123, 2019, doi: 10.1109/ELNANO.2019.8783427.

[26] B. V. P. V. Kumar, N. S. M. Sharma, K. L. Kishore, and N. Goel, "Leakage power recovery in spare cells by using state dependent leakage tables from library models," *Asia Pacific Conf. Postgrad. Res. Microelectron. Electron.*, no. December, pp. 19–24, 2012, doi: 10.1109/PrimeAsia.2012.6458620.

[27] V. S. Melikyan *et al.*, "Low Power, Low Offset, Area Efficient Comparator Design in Nanoscale CMOS Technology," *Proc. 2018 IEEE East-West Des. Test Symp. EWDTS 2018*, 2018, doi: 10.1109/EWDTS.2018.8524737.

[28] R. Joshi, M. A. Zaman, and S. Katkoori, "Novel Bit-Sliced Near-Memory Computing Based VLSI Architecture for Fast Sobel Edge Detection in IoT Edge Devices," *Proc. - 2020 6th IEEE Int. Symp. Smart Electron. Syst. iSES 2020*, pp. 291–296, 2020, doi: 10.1109/iSES50453.2020.00071.

[29] S. A. D. V. Jacinto *et al.*, “Development of Low Power Full-Custom 1 Kb 8T Synchronous SRAM for Wireless Sensor Network in 90nm CMOS Process Technology,” in *IEEE Region 10 Annual International Conference, Proceedings/TENCON*, 2019, vol. 2018-Octob, pp. 2366–2371, doi: 10.1109/TENCON.2018.8650402.

[30] D. S. Arellano *et al.*, “Design of an Advanced Microcontroller Bus Architecture for Wireless Sensor Network in 90nm Process Technology,” in *IEEE Region 10 Annual International Conference, Proceedings/TENCON*, 2019, vol. 2018-Octob, pp. 2352–2356, doi: 10.1109/TENCON.2018.8650335.

[31] A. L. L. Avelino *et al.*, “Development of a Self-Correcting CMOS-Based Clock Generator for Wireless Sensor Network in 90nm Process Technology,” in *IEEE Region 10 Annual International Conference, Proceedings/TENCON*, 2019, vol. 2018-Octob, pp. 2340–2345, doi: 10.1109/TENCON.2018.8650425.

# APPENDICES

## APPENDIX A: The Report Area of Technology 14nm with varies clock period.

```
Filename : ra_0.5.rpt


****************************************
Report : area
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 02:27:22 2023
****************************************

Library(s) Used:

    saed14rvt_ss0p72v125c(File:
/home/user/Jenny/SAED14_EDK/lib/stdcell_rvt/db_nldm/saed14rvt_ss0p72v125c.
db)

Number of ports:                         3242
Number of nets:                         10812
Number of cells:                         7718
Number of combinational cells:           6172
Number of sequential cells:              1517
Number of macros/black boxes:               0
Number of buf/inv:                       1363
Number of references:                       4

Combinational area:              1941.256773
Buf/Inv area:                     292.240799
Noncombinational area:           1583.481600
Macro/Black Box area:               0.000000
Net Interconnect area:           5535.215813

Total cell area:                 3524.738374
Total area:                      9059.954187
1
Filename : ra_1.5.rpt

Filename : ra_1.rpt


****************************************
Report : area
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 02:28:43 2023
****************************************

Library(s) Used:

    saed14rvt_ss0p72v125c(File:
/home/user/Jenny/SAED14_EDK/lib/stdcell_rvt/db_nldm/saed14rvt_ss0p72v125c.
db)

Number of ports:                         3242
Number of nets:                         10223
```

```
Number of cells:                         7135
Number of combinational cells:           5589
Number of sequential cells:              1517
Number of macros/black boxes:               0
Number of buf/inv:                       1080
Number of references:                       4

Combinational area:                1755.709182
Buf/Inv area:                       226.084801
Noncombinational area:             1576.377601
Macro/Black Box area:                 0.000000
Net Interconnect area:             5399.357758

Total cell area:                   3332.086783
Total area:                        8731.444541
1
Filename : ra_2.rpt


****************************************
Report : area
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 02:29:32 2023
****************************************

Library(s) Used:

    saed14rvt_ss0p72v125c(File:
/home/user/Jenny/SAED14_EDK/lib/stdcell_rvt/db_nldm/saed14rvt_ss0p72v125c.
db)

Number of ports:                         3242
Number of nets:                          9969
Number of cells:                         6881
Number of combinational cells:           5335
Number of sequential cells:              1517
Number of macros/black boxes:               0
Number of buf/inv:                       1020
Number of references:                       4

Combinational area:                1684.003185
Buf/Inv area:                       214.096801
Noncombinational area:             1523.230808
Macro/Black Box area:                 0.000000
Net Interconnect area:             5683.077895

Total cell area:                   3207.233993
Total area:                        8890.311888
1
Filename : ra_3.rpt


****************************************
```

```
Report : area
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 02:30:25 2023
****************************************

Library(s) Used:

    saed14rvt_ss0p72v125c(File:
/home/user/Jenny/SAED14_EDK/lib/stdcell_rvt/db_nldm/saed14rvt_ss0p72v125c.
db)

Number of ports:                         3242
Number of nets:                          9962
Number of cells:                         6874
Number of combinational cells:           5328
Number of sequential cells:              1517
Number of macros/black boxes:               0
Number of buf/inv:                       1019
Number of references:                       4

Combinational area:              1682.804385
Buf/Inv area:                     214.185601
Noncombinational area:           1523.230808
Macro/Black Box area:               0.000000
Net Interconnect area:           5687.826504

Total cell area:                 3206.035193
Total area:                      8893.861697
1
Filename : ra_4.rpt


****************************************
Report : area
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 02:31:20 2023
****************************************

Library(s) Used:

    saed14rvt_ss0p72v125c(File:
/home/user/Jenny/SAED14_EDK/lib/stdcell_rvt/db_nldm/saed14rvt_ss0p72v125c.
db)

Number of ports:                         3242
Number of nets:                          9962
Number of cells:                         6874
Number of combinational cells:           5328
Number of sequential cells:              1517
Number of macros/black boxes:               0
Number of buf/inv:                       1016
Number of references:                       4
```

```
Combinational area:               1683.381585
Buf/Inv area:                      213.386401
Noncombinational area:            1523.230808
Macro/Black Box area:                0.000000
Net Interconnect area:            5686.504601

Total cell area:                  3206.612393
Total area:                       8893.116994
1
Filename : ra_5.5.rpt


****************************************
Report : area
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 02:33:01 2023
****************************************

Library(s) Used:

    saed14rvt_ss0p72v125c(File:
/home/user/Jenny/SAED14_EDK/lib/stdcell_rvt/db_nldm/saed14rvt_ss0p72v125c.
db)

Number of ports:                        3242
Number of nets:                         9964
Number of cells:                        6876
Number of combinational cells:          5330
Number of sequential cells:             1517
Number of macros/black boxes:              0
Number of buf/inv:                      1015
Number of references:                      4

Combinational area:               1683.248385
Buf/Inv area:                      213.120001
Noncombinational area:            1523.230808
Macro/Black Box area:                0.000000
Net Interconnect area:            5688.946807

Total cell area:                  3206.479194
Total area:                       8895.426001
1
Filename : ra_5.rpt


****************************************
Report : area
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 02:32:16 2023
****************************************
```

```
Library(s) Used:

    saed14rvt_ss0p72v125c(File:
/home/user/Jenny/SAED14_EDK/lib/stdcell_rvt/db_nldm/saed14rvt_ss0p72v125c.
db)

Number of ports:                         3242
Number of nets:                          9966
Number of cells:                         6878
Number of combinational cells:           5332
Number of sequential cells:              1517
Number of macros/black boxes:               0
Number of buf/inv:                       1017
Number of references:                       4

Combinational area:              1682.804385
Buf/Inv area:                     213.475201
Noncombinational area:           1523.230808
Macro/Black Box area:               0.000000
Net Interconnect area:           5689.142001

Total cell area:                 3206.035193
Total area:                      8895.177195
1
```

APPENDIX B: The Report Power of Technology 14nm with varies clock period.

```
Filename : rp_0.5.rpt

Loading db file
'/home/user/Jenny/SAED14_EDK/lib/stdcell_rvt/db_nldm/saed14rvt_ss0p72v125
c.db'
Information: Propagating switching activity (low effort zero delay
simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
        -analysis_effort low
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 02:27:27 2023
****************************************


Library(s) Used:

    saed14rvt_ss0p72v125c (File:
/home/user/Jenny/SAED14_EDK/lib/stdcell_rvt/db_nldm/saed14rvt_ss0p72v125c
.db)


Operating Conditions: ss0p72v125c   Library: saed14rvt_ss0p72v125c
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
riscv_pip_27           8000              saed14rvt_ss0p72v125c


Global Operating Voltage = 0.72
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   1.9954 mW   (92%)
  Net Switching Power  = 181.1789 uW    (8%)
                         ---------
Total Dynamic Power    =   2.1766 mW  (100%)

Cell Leakage Power     =  23.7972 uW


                 Internal         Switching           Leakage
Total
```

```
Power Group      Power            Power               Power
Power   (   %    )  Attrs
--------------------------------------------------------------------------
-------------------------
io_pad             0.0000            0.0000            0.0000
0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000
0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000
0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000
0.0000  (   0.00%)
register       1.9041e+03           24.1175        1.3195e+07
1.9414e+03  (  88.23%)
sequential         0.0000            0.0000            0.0000
0.0000  (   0.00%)
combinational     91.3756          157.0616        1.0602e+07
259.0396  (  11.77%)
--------------------------------------------------------------------------
-------------------------
Total          1.9954e+03 uW       181.1791 uW     2.3797e+07 pW
2.2004e+03 uW
1
Filename : rp_1.5.rpt

Information: Propagating switching activity (low effort zero delay
simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
        -analysis_effort low
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 02:38:07 2023
****************************************


Library(s) Used:

    saed14rvt_ss0p72v125c (File:
/home/user/Jenny/SAED14_EDK/lib/stdcell_rvt/db_nldm/saed14rvt_ss0p72v125c
.db)


Operating Conditions: ss0p72v125c   Library: saed14rvt_ss0p72v125c
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
riscv_pip_27           8000              saed14rvt_ss0p72v125c
```

```
Global Operating Voltage = 0.72
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  = 627.5790 uW   (91%)
  Net Switching Power  =  64.7680 uW    (9%)
                         ---------
Total Dynamic Power    = 692.3470 uW  (100%)

Cell Leakage Power     =  22.2714 uW


                 Internal         Switching           Leakage
Total
Power Group      Power            Power               Power
Power   (   %    )  Attrs
--------------------------------------------------------------------------------
-------------------------
io_pad             0.0000            0.0000            0.0000
0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000
0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000
0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000
0.0000  (   0.00%)
register         603.8760            8.8840        1.1710e+07
624.4703  (  87.39%)
sequential         0.0000            0.0000            0.0000
0.0000  (   0.00%)
combinational     23.7028           55.8841        1.0561e+07
90.1481  (  12.61%)
--------------------------------------------------------------------------------
-------------------------
Total            627.5789 uW        64.7681 uW     2.2271e+07 pW
714.6184 uW
1
Filename : rp_1.rpt

Loading db file
'/home/user/Jenny/SAED14_EDK/lib/stdcell_rvt/db_nldm/saed14rvt_ss0p72v125
c.db'
Information: Propagating switching activity (low effort zero delay
simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
```

```
        -analysis_effort low
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 02:28:47 2023
****************************************


Library(s) Used:

    saed14rvt_ss0p72v125c (File:
/home/user/Jenny/SAED14_EDK/lib/stdcell_rvt/db_nldm/saed14rvt_ss0p72v125c
.db)


Operating Conditions: ss0p72v125c   Library: saed14rvt_ss0p72v125c
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
riscv_pip_27          8000               saed14rvt_ss0p72v125c


Global Operating Voltage = 0.72
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  = 970.8690 uW   (91%)
  Net Switching Power  =  93.7321 uW    (9%)
                         ---------
Total Dynamic Power    =   1.0646 mW  (100%)

Cell Leakage Power     =  23.3604 uW


                 Internal         Switching           Leakage
Total
Power Group      Power            Power               Power
Power   (   %    )  Attrs
--------------------------------------------------------------------------------
------------------------
io_pad             0.0000            0.0000            0.0000
0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000
0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000
0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000
0.0000  (   0.00%)
```

```
register          931.8571           12.3901        1.3406e+07
957.6543  (  88.02%)
sequential         0.0000            0.0000             0.0000
0.0000  (   0.00%)
combinational     39.0114           81.3421        9.9543e+06
130.3080  (  11.98%)
--------------------------------------------------------------------------------
-------------------------
Total             970.8685 uW        93.7321 uW     2.3360e+07 pW
1.0880e+03 uW
1
Filename : rp_2.rpt

Loading db file
'/home/user/Jenny/SAED14_EDK/lib/stdcell_rvt/db_nldm/saed14rvt_ss0p72v125
c.db'
Information: Propagating switching activity (low effort zero delay
simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
        -analysis_effort low
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 02:29:37 2023
****************************************


Library(s) Used:

    saed14rvt_ss0p72v125c (File:
/home/user/Jenny/SAED14_EDK/lib/stdcell_rvt/db_nldm/saed14rvt_ss0p72v125c
.db)


Operating Conditions: ss0p72v125c   Library: saed14rvt_ss0p72v125c
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
riscv_pip_27           8000              saed14rvt_ss0p72v125c


Global Operating Voltage = 0.72
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW
```

```
  Cell Internal Power  = 470.5101 uW   (91%)
  Net Switching Power  =  49.2487 uW    (9%)
                         ---------
Total Dynamic Power    = 519.7589 uW  (100%)

Cell Leakage Power     =  22.3027 uW


                 Internal         Switching           Leakage
Total
Power Group      Power            Power               Power
Power   (   %    )  Attrs
--------------------------------------------------------------------------------
------------------------
io_pad             0.0000            0.0000            0.0000
0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000
0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000
0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000
0.0000  (   0.00%)
register         452.4743            6.7131        1.1710e+07
470.8975  (  86.87%)
sequential         0.0000            0.0000            0.0000
0.0000  (   0.00%)
combinational     18.0362           42.5356        1.0592e+07
71.1639  (  13.13%)
--------------------------------------------------------------------------------
------------------------
Total            470.5105 uW        49.2487 uW     2.2303e+07 pW
542.0613 uW
1
Filename : rp_3.rpt

Loading db file
'/home/user/Jenny/SAED14_EDK/lib/stdcell_rvt/db_nldm/saed14rvt_ss0p72v125
c.db'
Information: Propagating switching activity (low effort zero delay
simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
        -analysis_effort low
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 02:30:29 2023
****************************************


Library(s) Used:
```

```
    saed14rvt_ss0p72v125c (File:
/home/user/Jenny/SAED14_EDK/lib/stdcell_rvt/db_nldm/saed14rvt_ss0p72v125c
.db)


Operating Conditions: ss0p72v125c   Library: saed14rvt_ss0p72v125c
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
riscv_pip_27           8000              saed14rvt_ss0p72v125c


Global Operating Voltage = 0.72
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  = 313.9536 uW   (91%)
  Net Switching Power  =  32.5522 uW    (9%)
                         ---------
Total Dynamic Power    = 346.5058 uW  (100%)

Cell Leakage Power     =  22.3230 uW


                 Internal         Switching           Leakage
Total
Power Group      Power            Power               Power
Power   (   %    )  Attrs
--------------------------------------------------------------------------
------------------------
io_pad             0.0000            0.0000            0.0000
0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000
0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000
0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000
0.0000  (   0.00%)
register         301.8224            4.4517        1.1711e+07
317.9851  (  86.21%)
sequential         0.0000            0.0000            0.0000
0.0000  (   0.00%)
combinational     12.1313           28.1005        1.0612e+07
50.8437  (  13.79%)
--------------------------------------------------------------------------
------------------------
Total            313.9537 uW        32.5522 uW     2.2323e+07 pW
368.8288 uW
```

```
1
Filename : rp_4.rpt

Information: Propagating switching activity (low effort zero delay
simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
        -analysis_effort low
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 02:31:21 2023
****************************************


Library(s) Used:

    saed14rvt_ss0p72v125c (File:
/home/user/Jenny/SAED14_EDK/lib/stdcell_rvt/db_nldm/saed14rvt_ss0p72v125c
.db)


Operating Conditions: ss0p72v125c   Library: saed14rvt_ss0p72v125c
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
riscv_pip_27           8000              saed14rvt_ss0p72v125c


Global Operating Voltage = 0.72
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  = 236.0241 uW   (91%)
  Net Switching Power  =  24.3803 uW    (9%)
                         ---------
Total Dynamic Power    = 260.4044 uW  (100%)

Cell Leakage Power     =  22.3474 uW


                 Internal         Switching           Leakage
Total
Power Group      Power            Power               Power
Power   (   %    )  Attrs
```

```
--------------------------------------------------------------------------------
-------------------------
io_pad              0.0000            0.0000            0.0000
0.0000  (   0.00%)
memory              0.0000            0.0000            0.0000
0.0000  (   0.00%)
black_box           0.0000            0.0000            0.0000
0.0000  (   0.00%)
clock_network       0.0000            0.0000            0.0000
0.0000  (   0.00%)
register          226.7911            3.3470        1.1708e+07
241.8457  (  85.53%)
sequential          0.0000            0.0000            0.0000
0.0000  (   0.00%)
combinational       9.2330           21.0333        1.0640e+07
40.9060  (  14.47%)
--------------------------------------------------------------------------------
-------------------------
Total             236.0241 uW        24.3803 uW     2.2347e+07 pW
282.7517 uW
1
Filename : rp_5.5.rpt

Information: Propagating switching activity (low effort zero delay
simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
        -analysis_effort low
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 02:33:02 2023
****************************************


Library(s) Used:

    saed14rvt_ss0p72v125c (File:
/home/user/Jenny/SAED14_EDK/lib/stdcell_rvt/db_nldm/saed14rvt_ss0p72v125c
.db)


Operating Conditions: ss0p72v125c   Library: saed14rvt_ss0p72v125c
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
riscv_pip_27           8000              saed14rvt_ss0p72v125c


Global Operating Voltage = 0.72
Power-specific unit information :
```

```
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  = 170.9889 uW   (91%)
  Net Switching Power  =  17.8666 uW    (9%)
                         ---------
Total Dynamic Power    = 188.8556 uW  (100%)

Cell Leakage Power     =  22.3041 uW


                 Internal         Switching           Leakage
Total
Power Group      Power            Power               Power
Power   (   %    )  Attrs
--------------------------------------------------------------------------
-------------------------
io_pad             0.0000            0.0000            0.0000
0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000
0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000
0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000
0.0000  (   0.00%)
register         164.4627            2.4496        1.1714e+07
178.6260  (  84.59%)
sequential         0.0000            0.0000            0.0000
0.0000  (   0.00%)
combinational      6.5262           15.4171        1.0590e+07
32.5337  (  15.41%)
--------------------------------------------------------------------------
-------------------------
Total            170.9889 uW        17.8666 uW     2.2304e+07 pW
211.1597 uW
1
Filename : rp_5.rpt

Information: Propagating switching activity (low effort zero delay
simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
        -analysis_effort low
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 02:32:17 2023
****************************************
```

```
Library(s) Used:

    saed14rvt_ss0p72v125c (File:
/home/user/Jenny/SAED14_EDK/lib/stdcell_rvt/db_nldm/saed14rvt_ss0p72v125c
.db)


Operating Conditions: ss0p72v125c   Library: saed14rvt_ss0p72v125c
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
riscv_pip_27           8000              saed14rvt_ss0p72v125c


Global Operating Voltage = 0.72
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  = 188.4996 uW   (91%)
  Net Switching Power  =  19.5412 uW    (9%)
                         ---------
Total Dynamic Power    = 208.0408 uW  (100%)

Cell Leakage Power     =  22.3062 uW


                 Internal         Switching           Leakage
Total
Power Group      Power            Power               Power
Power   (   %    )  Attrs
--------------------------------------------------------------------------
------------------------
io_pad             0.0000            0.0000            0.0000
0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000
0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000
0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000
0.0000  (   0.00%)
register         181.3693            2.6661        1.1708e+07
195.7435  (  84.98%)
sequential         0.0000            0.0000            0.0000
0.0000  (   0.00%)
combinational      7.1303           16.8751        1.0598e+07
34.6036  (  15.02%)
```

```
-------------------------------------------------------------------------
------------------------
Total            188.4996 uW        19.5412 uW     2.2306e+07 pW
230.3470 uW
1
```

APPENDIX C: The Report Timing of Technology 14nm with varies clock period.

```
Filename : rt_0.5.rpt

Information: Updating design information... (UID-85)
Warning: Design 'riscv_pip_27' contains 1 high-fanout nets. A fanout
number of 1000 will be used for delay calculations involving these nets.
(TIM-134)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 02:27:22 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: ss0p72v125c   Library: saed14rvt_ss0p72v125c
Wire Load Model Mode: top

  Startpoint: dp/pipreg1/Rs2E_reg[4]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: dp/pipreg1/ImmExtE_reg[1]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       8000                  saed14rvt_ss0p72v125c

  Point                                                          Incr       Path
  ---------------------------------------------------------------------------
---
  clock clk (rise edge)                                          0.00       0.00
  clock network delay (ideal)                                    0.00       0.00
  dp/pipreg1/Rs2E_reg[4]/CK (SAEDRVT14_FDPRB_V3_2)               0.00 #     0.00
r
  dp/pipreg1/Rs2E_reg[4]/Q (SAEDRVT14_FDPRB_V3_2)                0.05       0.05
r
  dp/pipreg1/Rs2E[4] (ID_IEx)                                    0.00       0.05
r
  dp/Rs2E[4] (datapath)                                          0.00       0.05
r
  h/Rs2E[4] (hazardunit)                                         0.00       0.05
r
  h/U11/X (SAEDRVT14_EO2_1)                                      0.03       0.07
f
  h/U35/X (SAEDRVT14_NR2_MM_0P5)                                 0.01       0.09
r
  h/U17/X (SAEDRVT14_AN4_2)                                      0.03       0.12
r
```

```
  h/U24/X (SAEDRVT14_NR2_MM_1)                              0.02       0.14
f
  h/ForwardBE[0] (hazardunit)                               0.00       0.14
f
  dp/ForwardBE[0] (datapath)                                0.00       0.14
f
  dp/forwardMuxB/s[0] (mux3_3)                              0.00       0.14
f
  dp/forwardMuxB/U21/X (SAEDRVT14_BUF_PS_1P5)               0.02       0.16
f
  dp/forwardMuxB/U104/X (SAEDRVT14_OAI22_0P5)               0.01       0.17
r
  dp/forwardMuxB/U1/X (SAEDRVT14_AO2BB2_2)                  0.02       0.19
f
  dp/forwardMuxB/y[0] (mux3_3)                              0.00       0.19
f
  dp/srcbmux/d0[0] (mux3_2)                                 0.00       0.19
f
  dp/srcbmux/U86/X (SAEDRVT14_AN2_MM_1)                     0.01       0.21
f
  dp/srcbmux/U7/X (SAEDRVT14_OR2_1)                         0.02       0.22
f
  dp/srcbmux/y[0] (mux3_2)                                  0.00       0.22
f
  dp/alu/SrcB[0] (alu)                                      0.00       0.22
f
  dp/alu/U48/X (SAEDRVT14_EO2_V1_0P75)                      0.03       0.25
f
  dp/alu/add_1_root_add_17_2/B[0] (alu_DW01_add_5)          0.00       0.25
f
  dp/alu/add_1_root_add_17_2/U375/X (SAEDRVT14_INV_S_0P5)
                                                            0.01       0.27
r
  dp/alu/add_1_root_add_17_2/U668/X (SAEDRVT14_OAI21_0P5)
                                                            0.02       0.28
f
  dp/alu/add_1_root_add_17_2/U373/X (SAEDRVT14_AOI21_0P5)
                                                            0.02       0.30
r
  dp/alu/add_1_root_add_17_2/U623/X (SAEDRVT14_OAI21_0P5)
                                                            0.02       0.32
f
  dp/alu/add_1_root_add_17_2/U352/X (SAEDRVT14_AOI21_0P75)
                                                            0.02       0.33
r
  dp/alu/add_1_root_add_17_2/U673/X (SAEDRVT14_OAI21_0P5)
                                                            0.02       0.35
f
  dp/alu/add_1_root_add_17_2/U535/X (SAEDRVT14_INV_S_0P5)
                                                            0.01       0.36
r
  dp/alu/add_1_root_add_17_2/U602/X (SAEDRVT14_OAI21_0P5)
                                                            0.02       0.38
f
```

```
  dp/alu/add_1_root_add_17_2/U533/X (SAEDRVT14_EN2_0P5)
                                                          0.02       0.40
f
  dp/alu/add_1_root_add_17_2/SUM[11] (alu_DW01_add_5)     0.00       0.40
f
  dp/alu/U488/X (SAEDRVT14_AN2_0P5)                       0.01       0.42
f
  dp/alu/U194/X (SAEDRVT14_OR4_1)                         0.02       0.44
f
  dp/alu/U208/X (SAEDRVT14_OR4_1)                         0.03       0.47
f
  dp/alu/U374/X (SAEDRVT14_OR4_2)                         0.03       0.50
f
  dp/alu/U344/X (SAEDRVT14_OR4_2)                         0.03       0.53
f
  dp/alu/U948/X (SAEDRVT14_NR4_0P75)                      0.03       0.55
r
  dp/alu/Zero (alu)                                       0.00       0.55
r
  dp/ZeroE (datapath)                                     0.00       0.55
r
  c/ZeroE (controller)                                    0.00       0.55
r
  c/U2/X (SAEDRVT14_OAI22_0P5)                            0.02       0.57
f
  c/U4/X (SAEDRVT14_OR2_1)                                0.02       0.59
f
  c/PCSrcE (controller)                                   0.00       0.59
f
  h/PCSrcE (hazardunit)                                   0.00       0.59
f
  h/U8/X (SAEDRVT14_OR2_1)                                0.02       0.61
f
  h/FlushE (hazardunit)                                   0.00       0.61
f
  dp/FlushE (datapath)                                    0.00       0.61
f
  dp/pipreg1/clear (ID_IEx)                               0.00       0.61
f
  dp/pipreg1/U161/X (SAEDRVT14_INV_S_0P5)                 0.01       0.63
r
  dp/pipreg1/U152/X (SAEDRVT14_BUF_PS_1P5)                0.02       0.64
r
  dp/pipreg1/U155/X (SAEDRVT14_BUF_PS_1P5)                0.02       0.66
r
  dp/pipreg1/U90/X (SAEDRVT14_AN2B_PMM_2)                 0.02       0.68
r
  dp/pipreg1/ImmExtE_reg[1]/D (SAEDRVT14_FDPRB_V3_2)      0.01       0.69
r
  data arrival time                                                  0.69

  clock clk (rise edge)                                   0.50       0.50
  clock network delay (ideal)                             0.00       0.50
  clock uncertainty                                      -0.10       0.40
```

```
  dp/pipreg1/ImmExtE_reg[1]/CK (SAEDRVT14_FDPRB_V3_2)      0.00       0.40
r
  library setup time                                       0.00       0.40
  data required time                                                  0.40
  ---------------------------------------------------------------------------
---
  data required time                                                  0.40
  data arrival time                                                  -0.69
  ---------------------------------------------------------------------------
---
  slack (VIOLATED)                                                   -0.29


1
Filename : rt_1.5.rpt

Filename : rt_1.rpt

Information: Updating design information... (UID-85)
Warning: Design 'riscv_pip_27' contains 1 high-fanout nets. A fanout
number of 1000 will be used for delay calculations involving these nets.
(TIM-134)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 02:28:43 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: ss0p72v125c   Library: saed14rvt_ss0p72v125c
Wire Load Model Mode: top

  Startpoint: dp/pipreg1/Rs2E_reg[4]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: dp/pipreg1/ImmExtE_reg[28]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       8000                  saed14rvt_ss0p72v125c

  Point                                                    Incr       Path
  ---------------------------------------------------------------------------
---
  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
```

```
  dp/pipreg1/Rs2E_reg[4]/CK (SAEDRVT14_FDPRB_V3_2)        0.00 #     0.00
r
  dp/pipreg1/Rs2E_reg[4]/Q (SAEDRVT14_FDPRB_V3_2)         0.05       0.05
r
  dp/pipreg1/Rs2E[4] (ID_IEx)                             0.00       0.05
r
  dp/Rs2E[4] (datapath)                                   0.00       0.05
r
  h/Rs2E[4] (hazardunit)                                  0.00       0.05
r
  h/U66/X (SAEDRVT14_OR2_MM_1)                            0.02       0.06
r
  h/U50/X (SAEDRVT14_OR4_1)                               0.02       0.09
r
  h/U52/X (SAEDRVT14_INV_S_0P5)                           0.01       0.10
f
  h/U46/X (SAEDRVT14_OR4_1)                               0.03       0.12
f
  h/U17/X (SAEDRVT14_OR4_1)                               0.03       0.16
f
  h/U3/X (SAEDRVT14_INV_S_1)                              0.02       0.17
r
  h/ForwardBE[1] (hazardunit)                             0.00       0.17
r
  dp/ForwardBE[1] (datapath)                              0.00       0.17
r
  dp/forwardMuxB/s[1] (mux3_3)                            0.00       0.17
r
  dp/forwardMuxB/U43/X (SAEDRVT14_NR2_MM_0P5)             0.02       0.20
f
  dp/forwardMuxB/U6/X (SAEDRVT14_BUF_ECO_1)               0.03       0.23
f
  dp/forwardMuxB/U27/X (SAEDRVT14_AO222_1)                0.05       0.27
f
  dp/forwardMuxB/y[0] (mux3_3)                            0.00       0.27
f
  dp/srcbmux/d0[0] (mux3_2)                               0.00       0.27
f
  dp/srcbmux/U15/X (SAEDRVT14_AO222_1)                    0.04       0.32
f
  dp/srcbmux/y[0] (mux3_2)                                0.00       0.32
f
  dp/alu/SrcB[0] (alu)                                    0.00       0.32
f
  dp/alu/U411/X (SAEDRVT14_EO2_V1_0P75)                   0.04       0.36
f
  dp/alu/add_1_root_add_17_2/B[0] (alu_DW01_add_5)        0.00       0.36
f
  dp/alu/add_1_root_add_17_2/U622/X (SAEDRVT14_INV_S_0P5)
                                                          0.02       0.37
r
  dp/alu/add_1_root_add_17_2/U663/X (SAEDRVT14_OAI21_0P5)
                                                          0.02       0.39
f
```

```
  dp/alu/add_1_root_add_17_2/U655/X (SAEDRVT14_AOI21_0P5)
                                                          0.02       0.41
r
  dp/alu/add_1_root_add_17_2/U666/X (SAEDRVT14_OAI21_0P5)
                                                          0.02       0.43
f
  dp/alu/add_1_root_add_17_2/U667/X (SAEDRVT14_AOI21_0P5)
                                                          0.02       0.45
r
  dp/alu/add_1_root_add_17_2/U599/X (SAEDRVT14_OAI21_0P5)
                                                          0.02       0.47
f
  dp/alu/add_1_root_add_17_2/U631/X (SAEDRVT14_AOI21_0P5)
                                                          0.03       0.50
r
  dp/alu/add_1_root_add_17_2/U627/X (SAEDRVT14_OAI21_0P5)
                                                          0.02       0.52
f
  dp/alu/add_1_root_add_17_2/U501/X (SAEDRVT14_EN2_1)     0.03       0.55
f
  dp/alu/add_1_root_add_17_2/SUM[18] (alu_DW01_add_5)     0.00       0.55
f
  dp/alu/U220/X (SAEDRVT14_AO221_0P5)                     0.03       0.58
f
  dp/alu/U506/X (SAEDRVT14_OR4_1)                         0.03       0.61
f
  dp/alu/U478/X (SAEDRVT14_OR2_0P75)                      0.02       0.63
f
  dp/alu/U560/X (SAEDRVT14_NR4_0P75)                      0.02       0.66
r
  dp/alu/U245/X (SAEDRVT14_AN4_1)                         0.02       0.68
r
  dp/alu/U3/X (SAEDRVT14_AN4_1)                           0.03       0.71
r
  dp/alu/Zero (alu)                                       0.00       0.71
r
  dp/ZeroE (datapath)                                     0.00       0.71
r
  c/ZeroE (controller)                                    0.00       0.71
r
  c/U8/X (SAEDRVT14_EO2_1)                                0.02       0.73
r
  c/U7/X (SAEDRVT14_OAI22_0P5)                            0.02       0.75
f
  c/U1/X (SAEDRVT14_AO21_1)                               0.03       0.78
f
  c/PCSrcE (controller)                                   0.00       0.78
f
  h/PCSrcE (hazardunit)                                   0.00       0.78
f
  h/U37/X (SAEDRVT14_OR2_1)                               0.02       0.80
f
  h/FlushE (hazardunit)                                   0.00       0.80
f
```

```
  dp/FlushE (datapath)                                    0.00       0.80
f
  dp/pipreg1/clear (ID_IEx)                               0.00       0.80
f
  dp/pipreg1/U4/X (SAEDRVT14_INV_S_0P75)                  0.02       0.82
r
  dp/pipreg1/U12/X (SAEDRVT14_BUF_ECO_1)                  0.03       0.85
r
  dp/pipreg1/U117/X (SAEDRVT14_BUF_ECO_1)                 0.02       0.87
r
  dp/pipreg1/U42/X (SAEDRVT14_AN2_MM_0P5)                 0.02       0.89
r
  dp/pipreg1/ImmExtE_reg[28]/D (SAEDRVT14_FDPRB_V3_2)     0.01       0.90
r
  data arrival time                                                  0.90

  clock clk (rise edge)                                   1.00       1.00
  clock network delay (ideal)                             0.00       1.00
  clock uncertainty                                      -0.10       0.90
  dp/pipreg1/ImmExtE_reg[28]/CK (SAEDRVT14_FDPRB_V3_2)
                                                          0.00       0.90
r
  library setup time                                      0.00       0.90
  data required time                                                 0.90
  ------------------------------------------------------------------------
---
  data required time                                                 0.90
  data arrival time                                                 -0.90
  ------------------------------------------------------------------------
---
  slack (MET)                                                        0.00


1
Filename : rt_2.rpt

Information: Updating design information... (UID-85)
Warning: Design 'riscv_pip_27' contains 1 high-fanout nets. A fanout
number of 1000 will be used for delay calculations involving these nets.
(TIM-134)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 02:29:32 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: ss0p72v125c   Library: saed14rvt_ss0p72v125c
```

```
Wire Load Model Mode: top

  Startpoint: c/c_pipreg2/ResultSrcW_reg[1]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: dp/rf/rf_reg[31][1]
            (falling edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       8000                  saed14rvt_ss0p72v125c

  Point                                                          Incr       Path
  ---------------------------------------------------------------------------
---
  clock clk (rise edge)                                          0.00       0.00
  clock network delay (ideal)                                    0.00       0.00
  c/c_pipreg2/ResultSrcW_reg[1]/CK (SAEDRVT14_FDPRBQ_V2LP_1)
                                                                 0.00 #     0.00
r
  c/c_pipreg2/ResultSrcW_reg[1]/Q (SAEDRVT14_FDPRBQ_V2LP_1)
                                                                 0.05       0.05
r
  c/c_pipreg2/ResultSrcW[1] (c_IM_IW)                            0.00       0.05
r
  c/ResultSrcW[1] (controller)                                   0.00       0.05
r
  dp/ResultSrcW[1] (datapath)                                    0.00       0.05
r
  dp/resultmux/s[1] (mux3_1)                                     0.00       0.05
r
  dp/resultmux/U42/X (SAEDRVT14_BUF_ECO_1)                       0.03       0.08
r
  dp/resultmux/U43/X (SAEDRVT14_NR2_MM_1)                        0.03       0.11
f
  dp/resultmux/U1/X (SAEDRVT14_BUF_ECO_1)                        0.03       0.14
f
  dp/resultmux/U9/X (SAEDRVT14_AO222_1)                          0.06       0.19
f
  dp/resultmux/y[1] (mux3_1)                                     0.00       0.19
f
  dp/rf/wd3[1] (regfile)                                         0.00       0.19
f
  dp/rf/U3/X (SAEDRVT14_INV_S_1)                                 0.02       0.21
r
  dp/rf/U109/X (SAEDRVT14_BUF_ECO_1)                             0.03       0.25
r
  dp/rf/U548/X (SAEDRVT14_OAI22_1)                               0.04       0.29
f
  dp/rf/rf_reg[31][1]/D (SAEDRVT14_FDN_V2_1)                     0.01       0.29
f
  data arrival time                                                         0.29
```

```
  clock clk (fall edge)                                   1.00       1.00
  clock network delay (ideal)                             0.00       1.00
  clock uncertainty                                      -0.10       0.90
  dp/rf/rf_reg[31][1]/CK (SAEDRVT14_FDN_V2_1)             0.00       0.90
f
  library setup time                                     -0.01       0.89
  data required time                                                 0.89
  ---------------------------------------------------------------------------
---
  data required time                                                 0.89
  data arrival time                                                 -0.29
  ---------------------------------------------------------------------------
---
  slack (MET)                                                        0.60


1
Filename : rt_3.rpt

Information: Updating design information... (UID-85)
Warning: Design 'riscv_pip_27' contains 1 high-fanout nets. A fanout
number of 1000 will be used for delay calculations involving these nets.
(TIM-134)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 02:30:25 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: ss0p72v125c   Library: saed14rvt_ss0p72v125c
Wire Load Model Mode: top

  Startpoint: c/c_pipreg2/ResultSrcW_reg[1]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: dp/rf/rf_reg[31][1]
            (falling edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       8000                  saed14rvt_ss0p72v125c

  Point                                                   Incr       Path
  ---------------------------------------------------------------------------
---
  clock clk (rise edge)                                   0.00       0.00
```

```
  clock network delay (ideal)                              0.00       0.00
  c/c_pipreg2/ResultSrcW_reg[1]/CK (SAEDRVT14_FDPRBQ_V2LP_1)
                                                           0.00 #     0.00
r
  c/c_pipreg2/ResultSrcW_reg[1]/Q (SAEDRVT14_FDPRBQ_V2LP_1)
                                                           0.05       0.05
r
  c/c_pipreg2/ResultSrcW[1] (c_IM_IW)                      0.00       0.05
r
  c/ResultSrcW[1] (controller)                             0.00       0.05
r
  dp/ResultSrcW[1] (datapath)                              0.00       0.05
r
  dp/resultmux/s[1] (mux3_1)                               0.00       0.05
r
  dp/resultmux/U42/X (SAEDRVT14_BUF_ECO_1)                 0.03       0.08
r
  dp/resultmux/U43/X (SAEDRVT14_NR2_MM_1)                  0.03       0.11
f
  dp/resultmux/U1/X (SAEDRVT14_BUF_ECO_1)                  0.03       0.14
f
  dp/resultmux/U9/X (SAEDRVT14_AO222_1)                    0.06       0.19
f
  dp/resultmux/y[1] (mux3_1)                               0.00       0.19
f
  dp/rf/wd3[1] (regfile)                                   0.00       0.19
f
  dp/rf/U3/X (SAEDRVT14_INV_S_1)                           0.02       0.21
r
  dp/rf/U109/X (SAEDRVT14_BUF_ECO_1)                       0.03       0.25
r
  dp/rf/U610/X (SAEDRVT14_OAI22_1)                         0.04       0.29
f
  dp/rf/rf_reg[31][1]/D (SAEDRVT14_FDN_V2_1)               0.01       0.29
f
  data arrival time                                                   0.29

  clock clk (fall edge)                                    1.50       1.50
  clock network delay (ideal)                              0.00       1.50
  clock uncertainty                                       -0.10       1.40
  dp/rf/rf_reg[31][1]/CK (SAEDRVT14_FDN_V2_1)              0.00       1.40
f
  library setup time                                      -0.01       1.39
  data required time                                                  1.39
  ---------------------------------------------------------------------------
---
  data required time                                                  1.39
  data arrival time                                                  -0.29
  ---------------------------------------------------------------------------
---
  slack (MET)                                                         1.10


1
```

```
Filename : rt_4.rpt

Information: Updating design information... (UID-85)
Warning: Design 'riscv_pip_27' contains 1 high-fanout nets. A fanout
number of 1000 will be used for delay calculations involving these nets.
(TIM-134)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 02:31:20 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: ss0p72v125c   Library: saed14rvt_ss0p72v125c
Wire Load Model Mode: top

  Startpoint: c/c_pipreg2/ResultSrcW_reg[1]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: dp/rf/rf_reg[31][1]
            (falling edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       8000                  saed14rvt_ss0p72v125c

  Point                                                         Incr       Path
  --------------------------------------------------------------------------
---
  clock clk (rise edge)                                         0.00       0.00
  clock network delay (ideal)                                   0.00       0.00
  c/c_pipreg2/ResultSrcW_reg[1]/CK (SAEDRVT14_FDPRBQ_V2LP_1)
                                                                0.00 #     0.00
r
  c/c_pipreg2/ResultSrcW_reg[1]/Q (SAEDRVT14_FDPRBQ_V2LP_1)
                                                                0.05       0.05
r
  c/c_pipreg2/ResultSrcW[1] (c_IM_IW)                           0.00       0.05
r
  c/ResultSrcW[1] (controller)                                  0.00       0.05
r
  dp/ResultSrcW[1] (datapath)                                   0.00       0.05
r
  dp/resultmux/s[1] (mux3_1)                                    0.00       0.05
r
  dp/resultmux/U42/X (SAEDRVT14_BUF_ECO_1)                      0.03       0.08
r
```

```
  dp/resultmux/U43/X (SAEDRVT14_NR2_MM_1)                 0.03       0.11
f
  dp/resultmux/U1/X (SAEDRVT14_BUF_ECO_1)                 0.03       0.14
f
  dp/resultmux/U9/X (SAEDRVT14_AO222_1)                   0.06       0.19
f
  dp/resultmux/y[1] (mux3_1)                              0.00       0.19
f
  dp/rf/wd3[1] (regfile)                                  0.00       0.19
f
  dp/rf/U3/X (SAEDRVT14_INV_S_1)                          0.02       0.21
r
  dp/rf/U109/X (SAEDRVT14_BUF_ECO_1)                      0.03       0.25
r
  dp/rf/U610/X (SAEDRVT14_OAI22_1)                        0.04       0.29
f
  dp/rf/rf_reg[31][1]/D (SAEDRVT14_FDN_V2_1)              0.01       0.29
f
  data arrival time                                                  0.29

  clock clk (fall edge)                                   2.00       2.00
  clock network delay (ideal)                             0.00       2.00
  clock uncertainty                                      -0.10       1.90
  dp/rf/rf_reg[31][1]/CK (SAEDRVT14_FDN_V2_1)             0.00       1.90
f
  library setup time                                     -0.01       1.89
  data required time                                                 1.89
  ---------------------------------------------------------------------------
---
  data required time                                                 1.89
  data arrival time                                                 -0.29
  ---------------------------------------------------------------------------
---
  slack (MET)                                                        1.60


1
Filename : rt_5.5.rpt

Information: Updating design information... (UID-85)
Warning: Design 'riscv_pip_27' contains 1 high-fanout nets. A fanout
number of 1000 will be used for delay calculations involving these nets.
(TIM-134)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 02:33:01 2023
****************************************
```

```
 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: ss0p72v125c   Library: saed14rvt_ss0p72v125c
Wire Load Model Mode: top

  Startpoint: c/c_pipreg2/ResultSrcW_reg[1]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: dp/rf/rf_reg[31][1]
            (falling edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       8000                  saed14rvt_ss0p72v125c

  Point                                                          Incr       Path
  ---------------------------------------------------------------------------
---
  clock clk (rise edge)                                          0.00       0.00
  clock network delay (ideal)                                    0.00       0.00
  c/c_pipreg2/ResultSrcW_reg[1]/CK (SAEDRVT14_FDPRBQ_V2LP_1)
                                                                 0.00 #     0.00
r
  c/c_pipreg2/ResultSrcW_reg[1]/Q (SAEDRVT14_FDPRBQ_V2LP_1)
                                                                 0.05       0.05
r
  c/c_pipreg2/ResultSrcW[1] (c_IM_IW)                            0.00       0.05
r
  c/ResultSrcW[1] (controller)                                   0.00       0.05
r
  dp/ResultSrcW[1] (datapath)                                    0.00       0.05
r
  dp/resultmux/s[1] (mux3_1)                                     0.00       0.05
r
  dp/resultmux/U42/X (SAEDRVT14_BUF_ECO_1)                       0.03       0.08
r
  dp/resultmux/U43/X (SAEDRVT14_NR2_MM_1)                        0.03       0.11
f
  dp/resultmux/U1/X (SAEDRVT14_BUF_ECO_1)                        0.03       0.14
f
  dp/resultmux/U9/X (SAEDRVT14_AO222_1)                          0.06       0.19
f
  dp/resultmux/y[1] (mux3_1)                                     0.00       0.19
f
  dp/rf/wd3[1] (regfile)                                         0.00       0.19
f
  dp/rf/U3/X (SAEDRVT14_INV_S_1)                                 0.02       0.21
r
  dp/rf/U103/X (SAEDRVT14_BUF_ECO_1)                             0.03       0.25
r
  dp/rf/U608/X (SAEDRVT14_OAI22_1)                               0.04       0.29
f
```

```
  dp/rf/rf_reg[31][1]/D (SAEDRVT14_FDN_V2_1)              0.01       0.29
f
  data arrival time                                                  0.29

  clock clk (fall edge)                                   2.75       2.75
  clock network delay (ideal)                             0.00       2.75
  clock uncertainty                                      -0.10       2.65
  dp/rf/rf_reg[31][1]/CK (SAEDRVT14_FDN_V2_1)             0.00       2.65
f
  library setup time                                     -0.01       2.64
  data required time                                                 2.64
  ------------------------------------------------------------------------
---
  data required time                                                 2.64
  data arrival time                                                 -0.29
  ------------------------------------------------------------------------
---
  slack (MET)                                                        2.35


1
Filename : rt_5.rpt

Information: Updating design information... (UID-85)
Warning: Design 'riscv_pip_27' contains 1 high-fanout nets. A fanout
number of 1000 will be used for delay calculations involving these nets.
(TIM-134)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 02:32:16 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: ss0p72v125c   Library: saed14rvt_ss0p72v125c
Wire Load Model Mode: top

  Startpoint: c/c_pipreg2/ResultSrcW_reg[1]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: dp/rf/rf_reg[31][1]
            (falling edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       8000                  saed14rvt_ss0p72v125c
```

```
  Point                                                   Incr       Path
  ------------------------------------------------------------------------
---
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  c/c_pipreg2/ResultSrcW_reg[1]/CK (SAEDRVT14_FDPRBQ_V2LP_1)
                                                          0.00 #     0.00
r
  c/c_pipreg2/ResultSrcW_reg[1]/Q (SAEDRVT14_FDPRBQ_V2LP_1)
                                                          0.05       0.05
r
  c/c_pipreg2/ResultSrcW[1] (c_IM_IW)                     0.00       0.05
r
  c/ResultSrcW[1] (controller)                            0.00       0.05
r
  dp/ResultSrcW[1] (datapath)                             0.00       0.05
r
  dp/resultmux/s[1] (mux3_1)                              0.00       0.05
r
  dp/resultmux/U42/X (SAEDRVT14_BUF_ECO_1)                0.03       0.08
r
  dp/resultmux/U43/X (SAEDRVT14_NR2_MM_1)                 0.03       0.11
f
  dp/resultmux/U1/X (SAEDRVT14_BUF_ECO_1)                 0.03       0.14
f
  dp/resultmux/U9/X (SAEDRVT14_AO222_1)                   0.06       0.19
f
  dp/resultmux/y[1] (mux3_1)                              0.00       0.19
f
  dp/rf/wd3[1] (regfile)                                  0.00       0.19
f
  dp/rf/U3/X (SAEDRVT14_INV_S_1)                          0.02       0.21
r
  dp/rf/U109/X (SAEDRVT14_BUF_ECO_1)                      0.03       0.25
r
  dp/rf/U610/X (SAEDRVT14_OAI22_1)                        0.04       0.29
f
  dp/rf/rf_reg[31][1]/D (SAEDRVT14_FDN_V2_1)              0.01       0.29
f
  data arrival time                                                  0.29

  clock clk (fall edge)                                   2.50       2.50
  clock network delay (ideal)                             0.00       2.50
  clock uncertainty                                      -0.10       2.40
  dp/rf/rf_reg[31][1]/CK (SAEDRVT14_FDN_V2_1)             0.00       2.40
f
  library setup time                                     -0.01       2.39
  data required time                                                 2.39
  ------------------------------------------------------------------------
---
  data required time                                                 2.39
  data arrival time                                                 -0.29
  ------------------------------------------------------------------------
---
```

```
  slack (MET)                                                              2.10


1
Filename : rt_min_0.5.rpt


****************************************
Report : timing
         -path full
         -delay min
         -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 02:27:22 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: ss0p72v125c   Library: saed14rvt_ss0p72v125c
Wire Load Model Mode: top

  Startpoint: c/c_pipreg0/ResultSrcE_reg[1]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: c/c_pipreg1/ResultSrcM_reg[1]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       8000                  saed14rvt_ss0p72v125c

  Point                                                    Incr       Path
  ---------------------------------------------------------------------------
---
  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  c/c_pipreg0/ResultSrcE_reg[1]/CK (SAEDRVT14_FSDPRBQ_V2LP_0P5)
                                                           0.00 #     0.00
r
  c/c_pipreg0/ResultSrcE_reg[1]/Q (SAEDRVT14_FSDPRBQ_V2LP_0P5)
                                                           0.02       0.02
f
  c/c_pipreg0/ResultSrcE[1] (c_ID_IEx)                     0.00       0.02
f
  c/c_pipreg1/ResultSrcE[1] (c_IEx_IM)                     0.00       0.02
f
  c/c_pipreg1/ResultSrcM_reg[1]/D (SAEDRVT14_FDPRBQ_V2LP_1)
                                                           0.01       0.03
f
  data arrival time                                                   0.03

  clock clk (rise edge)                                    0.00       0.00
```

```
  clock network delay (ideal)                                  0.00       0.00
  c/c_pipreg1/ResultSrcM_reg[1]/CK (SAEDRVT14_FDPRBQ_V2LP_1)
                                                               0.00       0.00
r
  library hold time                                            0.00       0.00
  data required time                                                      0.00
  -------------------------------------------------------------------------
---
  data required time                                                      0.00
  data arrival time                                                      -0.03
  -------------------------------------------------------------------------
---
  slack (MET)                                                             0.03


1
Filename : rt_min_1.5.rpt

Filename : rt_min_1.rpt


****************************************
Report : timing
        -path full
        -delay min
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 02:28:43 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: ss0p72v125c   Library: saed14rvt_ss0p72v125c
Wire Load Model Mode: top

  Startpoint: c/c_pipreg0/ResultSrcE_reg[1]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: c/c_pipreg1/ResultSrcM_reg[1]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       8000                  saed14rvt_ss0p72v125c

  Point                                                        Incr       Path
  -------------------------------------------------------------------------
---
  clock clk (rise edge)                                        0.00       0.00
  clock network delay (ideal)                                  0.00       0.00
  c/c_pipreg0/ResultSrcE_reg[1]/CK (SAEDRVT14_FSDPRBQ_V2LP_0P5)
```

```
                                                          0.00 #     0.00
r
  c/c_pipreg0/ResultSrcE_reg[1]/Q (SAEDRVT14_FSDPRBQ_V2LP_0P5)
                                                          0.02       0.02
f
  c/c_pipreg0/ResultSrcE[1] (c_ID_IEx)                    0.00       0.02
f
  c/c_pipreg1/ResultSrcE[1] (c_IEx_IM)                    0.00       0.02
f
  c/c_pipreg1/ResultSrcM_reg[1]/D (SAEDRVT14_FDPRBQ_V2LP_1)
                                                          0.01       0.03
f
  data arrival time                                                  0.03

  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  c/c_pipreg1/ResultSrcM_reg[1]/CK (SAEDRVT14_FDPRBQ_V2LP_1)
                                                          0.00       0.00
r
  library hold time                                       0.00       0.00
  data required time                                                 0.00
  ------------------------------------------------------------------------
---
  data required time                                                 0.00
  data arrival time                                                 -0.03
  ------------------------------------------------------------------------
---
  slack (MET)                                                        0.03


1
Filename : rt_min_2.rpt


****************************************
Report : timing
        -path full
        -delay min
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 02:29:32 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: ss0p72v125c   Library: saed14rvt_ss0p72v125c
Wire Load Model Mode: top

  Startpoint: c/c_pipreg0/ResultSrcE_reg[1]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: c/c_pipreg1/ResultSrcM_reg[1]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
```

```
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       8000                  saed14rvt_ss0p72v125c

  Point                                                    Incr       Path
  -----------------------------------------------------------------------
---
  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  c/c_pipreg0/ResultSrcE_reg[1]/CK (SAEDRVT14_FSDPRBQ_V2LP_0P5)
                                                           0.00 #     0.00
r
  c/c_pipreg0/ResultSrcE_reg[1]/Q (SAEDRVT14_FSDPRBQ_V2LP_0P5)
                                                           0.02       0.02
f
  c/c_pipreg0/ResultSrcE[1] (c_ID_IEx)                     0.00       0.02
f
  c/c_pipreg1/ResultSrcE[1] (c_IEx_IM)                     0.00       0.02
f
  c/c_pipreg1/ResultSrcM_reg[1]/D (SAEDRVT14_FDPRBQ_V2LP_1)
                                                           0.01       0.03
f
  data arrival time                                                   0.03

  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  c/c_pipreg1/ResultSrcM_reg[1]/CK (SAEDRVT14_FDPRBQ_V2LP_1)
                                                           0.00       0.00
r
  library hold time                                        0.00       0.00
  data required time                                                  0.00
  -----------------------------------------------------------------------
---
  data required time                                                  0.00
  data arrival time                                                  -0.03
  -----------------------------------------------------------------------
---
  slack (MET)                                                         0.03


1
Filename : rt_min_3.rpt


****************************************
Report : timing
        -path full
        -delay min
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 02:30:25 2023
```

```
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: ss0p72v125c   Library: saed14rvt_ss0p72v125c
Wire Load Model Mode: top

  Startpoint: c/c_pipreg0/ResultSrcE_reg[1]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: c/c_pipreg1/ResultSrcM_reg[1]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       8000                  saed14rvt_ss0p72v125c

  Point                                                    Incr       Path
  -----------------------------------------------------------------------------
---
  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  c/c_pipreg0/ResultSrcE_reg[1]/CK (SAEDRVT14_FSDPRBQ_V2LP_0P5)
                                                           0.00 #     0.00
r
  c/c_pipreg0/ResultSrcE_reg[1]/Q (SAEDRVT14_FSDPRBQ_V2LP_0P5)
                                                           0.02       0.02
f
  c/c_pipreg0/ResultSrcE[1] (c_ID_IEx)                     0.00       0.02
f
  c/c_pipreg1/ResultSrcE[1] (c_IEx_IM)                     0.00       0.02
f
  c/c_pipreg1/ResultSrcM_reg[1]/D (SAEDRVT14_FDPRBQ_V2LP_1)
                                                           0.01       0.03
f
  data arrival time                                                   0.03

  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  c/c_pipreg1/ResultSrcM_reg[1]/CK (SAEDRVT14_FDPRBQ_V2LP_1)
                                                           0.00       0.00
r
  library hold time                                        0.00       0.00
  data required time                                                  0.00
  -----------------------------------------------------------------------------
---
  data required time                                                  0.00
  data arrival time                                                  -0.03
  -----------------------------------------------------------------------------
---
  slack (MET)                                                         0.03
```

```
1
Filename : rt_min_4.rpt


****************************************
Report : timing
        -path full
        -delay min
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 02:31:20 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: ss0p72v125c   Library: saed14rvt_ss0p72v125c
Wire Load Model Mode: top

  Startpoint: c/c_pipreg0/ResultSrcE_reg[1]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: c/c_pipreg1/ResultSrcM_reg[1]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       8000                  saed14rvt_ss0p72v125c

  Point                                                          Incr       Path
  ----------------------------------------------------------------------------
---
  clock clk (rise edge)                                          0.00       0.00
  clock network delay (ideal)                                    0.00       0.00
  c/c_pipreg0/ResultSrcE_reg[1]/CK (SAEDRVT14_FSDPRBQ_V2LP_0P5)
                                                                 0.00 #     0.00
r
  c/c_pipreg0/ResultSrcE_reg[1]/Q (SAEDRVT14_FSDPRBQ_V2LP_0P5)
                                                                 0.02       0.02
f
  c/c_pipreg0/ResultSrcE[1] (c_ID_IEx)                           0.00       0.02
f
  c/c_pipreg1/ResultSrcE[1] (c_IEx_IM)                           0.00       0.02
f
  c/c_pipreg1/ResultSrcM_reg[1]/D (SAEDRVT14_FDPRBQ_V2LP_1)
                                                                 0.01       0.03
f
  data arrival time                                                         0.03

  clock clk (rise edge)                                          0.00       0.00
  clock network delay (ideal)                                    0.00       0.00
  c/c_pipreg1/ResultSrcM_reg[1]/CK (SAEDRVT14_FDPRBQ_V2LP_1)
```

```
                                                                0.00       0.00
r
  library hold time                                             0.00       0.00
  data required time                                                       0.00
  -------------------------------------------------------------------------
---
  data required time                                                       0.00
  data arrival time                                                       -0.03
  -------------------------------------------------------------------------
---
  slack (MET)                                                              0.03


1
Filename : rt_min_5.5.rpt


****************************************
Report : timing
        -path full
        -delay min
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 02:33:01 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: ss0p72v125c   Library: saed14rvt_ss0p72v125c
Wire Load Model Mode: top

  Startpoint: c/c_pipreg0/ResultSrcE_reg[1]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: c/c_pipreg1/ResultSrcM_reg[1]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       8000                  saed14rvt_ss0p72v125c

  Point                                                    Incr       Path
  -------------------------------------------------------------------------
---
  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  c/c_pipreg0/ResultSrcE_reg[1]/CK (SAEDRVT14_FSDPRBQ_V2LP_0P5)
                                                           0.00 #     0.00
r
  c/c_pipreg0/ResultSrcE_reg[1]/Q (SAEDRVT14_FSDPRBQ_V2LP_0P5)
                                                           0.02       0.02
f
```

```
  c/c_pipreg0/ResultSrcE[1] (c_ID_IEx)                    0.00       0.02
f
  c/c_pipreg1/ResultSrcE[1] (c_IEx_IM)                    0.00       0.02
f
  c/c_pipreg1/ResultSrcM_reg[1]/D (SAEDRVT14_FDPRBQ_V2LP_1)
                                                          0.01       0.03
f
  data arrival time                                                  0.03

  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  c/c_pipreg1/ResultSrcM_reg[1]/CK (SAEDRVT14_FDPRBQ_V2LP_1)
                                                          0.00       0.00
r
  library hold time                                       0.00       0.00
  data required time                                                 0.00
  ------------------------------------------------------------------------
---
  data required time                                                 0.00
  data arrival time                                                 -0.03
  ------------------------------------------------------------------------
---
  slack (MET)                                                        0.03


1
Filename : rt_min_5.rpt


****************************************
Report : timing
        -path full
        -delay min
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 02:32:16 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: ss0p72v125c   Library: saed14rvt_ss0p72v125c
Wire Load Model Mode: top

  Startpoint: c/c_pipreg0/ResultSrcE_reg[1]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: c/c_pipreg1/ResultSrcM_reg[1]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       8000                  saed14rvt_ss0p72v125c
```

```
  Point                                                   Incr       Path
  ------------------------------------------------------------------------
---
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  c/c_pipreg0/ResultSrcE_reg[1]/CK (SAEDRVT14_FSDPRBQ_V2LP_0P5)
                                                          0.00 #     0.00
r
  c/c_pipreg0/ResultSrcE_reg[1]/Q (SAEDRVT14_FSDPRBQ_V2LP_0P5)
                                                          0.02       0.02
f
  c/c_pipreg0/ResultSrcE[1] (c_ID_IEx)                    0.00       0.02
f
  c/c_pipreg1/ResultSrcE[1] (c_IEx_IM)                    0.00       0.02
f
  c/c_pipreg1/ResultSrcM_reg[1]/D (SAEDRVT14_FDPRBQ_V2LP_1)
                                                          0.01       0.03
f
  data arrival time                                                  0.03

  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  c/c_pipreg1/ResultSrcM_reg[1]/CK (SAEDRVT14_FDPRBQ_V2LP_1)
                                                          0.00       0.00
r
  library hold time                                       0.00       0.00
  data required time                                                 0.00
  ------------------------------------------------------------------------
---
  data required time                                                 0.00
  data arrival time                                                 -0.03
  ------------------------------------------------------------------------
---
  slack (MET)                                                        0.03


1
```

APPENDIX D: The Report Area of Technology 32nm with varies clock period.

```
Filename : ra_0.5.rpt


****************************************
Report : area
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:32:23 2023
****************************************

Library(s) Used:

    saed32lvt_ss0p95v125c (File:
/home/user/Jenny/saed32nm/lib/stdcell_lvt/db_nldm/saed32lvt_ss0p95v125c.d
b)

Number of ports:                         3242
Number of nets:                         12066
Number of cells:                         8981
Number of combinational cells:           7397
Number of sequential cells:              1549
Number of macros/black boxes:               0
Number of buf/inv:                       1012
Number of references:                       3

Combinational area:              16325.448331
Buf/Inv area:                     1770.367148
Noncombinational area:           10503.771807
Macro/Black Box area:                0.000000
Net Interconnect area:            7361.207902

Total cell area:                 26829.220138
Total area:                      34190.428040
1
Filename : ra_1.5.rpt


****************************************
Report : area
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 03:10:14 2023
****************************************

Library(s) Used:

    saed32lvt_ss0p95v125c (File:
/home/user/Jenny/saed32nm/lib/stdcell_lvt/db_nldm/saed32lvt_ss0p95v125c.d
b)

Number of ports:                         3242
Number of nets:                         10433
Number of cells:                         7343
Number of combinational cells:           5759
```

```
Number of sequential cells:              1549
Number of macros/black boxes:               0
Number of buf/inv:                       1030
Number of references:                       3

Combinational area:             14120.748964
Buf/Inv area:                    1943.693331
Noncombinational area:          10504.280095
Macro/Black Box area:               0.000000
Net Interconnect area:           7313.058111

Total cell area:                24625.029058
Total area:                     31938.087169
1
Filename : ra_1.rpt


****************************************
Report : area
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:35:04 2023
****************************************

Library(s) Used:

    saed32lvt_ss0p95v125c (File:
/home/user/Jenny/saed32nm/lib/stdcell_lvt/db_nldm/saed32lvt_ss0p95v125c.d
b)

Number of ports:                         3242
Number of nets:                         11173
Number of cells:                         7094
Number of combinational cells:           5542
Number of sequential cells:              1517
Number of macros/black boxes:               0
Number of buf/inv:                        986
Number of references:                       3

Combinational area:             14153.533695
Buf/Inv area:                    1793.240105
Noncombinational area:          10291.307416
Macro/Black Box area:               0.000000
Net Interconnect area:           6300.329033

Total cell area:                24444.841111
Total area:                     30745.170144
1
Filename : ra_2.rpt


****************************************
Report : area
Design : riscv_pip_27
```

```
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:36:56 2023
****************************************

Library(s) Used:

    saed32lvt_ss0p95v125c (File:
/home/user/Jenny/saed32nm/lib/stdcell_lvt/db_nldm/saed32lvt_ss0p95v125c.d
b)

Number of ports:                         3242
Number of nets:                         11014
Number of cells:                         6937
Number of combinational cells:           5385
Number of sequential cells:              1517
Number of macros/black boxes:               0
Number of buf/inv:                        957
Number of references:                       3

Combinational area:              12830.714045
Buf/Inv area:                     1515.460706
Noncombinational area:           10290.799128
Macro/Black Box area:                0.000000
Net Interconnect area:            6852.204638

Total cell area:                 23121.513173
Total area:                      29973.717811
1
Filename : ra_3.rpt


****************************************
Report : area
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:37:48 2023
****************************************

Library(s) Used:

    saed32lvt_ss0p95v125c (File:
/home/user/Jenny/saed32nm/lib/stdcell_lvt/db_nldm/saed32lvt_ss0p95v125c.d
b)

Number of ports:                         3242
Number of nets:                         10864
Number of cells:                         6787
Number of combinational cells:           5235
Number of sequential cells:              1517
Number of macros/black boxes:               0
Number of buf/inv:                        908
Number of references:                       3

Combinational area:              12591.056237
```

```
Buf/Inv area:                    1439.979939
Noncombinational area:          10290.799128
Macro/Black Box area:               0.000000
Net Interconnect area:           6725.437641

Total cell area:                22881.855365
Total area:                     29607.293006
1
Filename : ra_4.rpt


****************************************
Report : area
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:38:41 2023
****************************************

Library(s) Used:

    saed32lvt_ss0p95v125c (File:
/home/user/Jenny/saed32nm/lib/stdcell_lvt/db_nldm/saed32lvt_ss0p95v125c.d
b)

Number of ports:                        3242
Number of nets:                        10877
Number of cells:                        6800
Number of combinational cells:          5248
Number of sequential cells:             1517
Number of macros/black boxes:              0
Number of buf/inv:                       909
Number of references:                      3

Combinational area:             12582.923626
Buf/Inv area:                    1430.068324
Noncombinational area:          10290.799128
Macro/Black Box area:               0.000000
Net Interconnect area:           6732.298216

Total cell area:                22873.722754
Total area:                     29606.020969
1
Filename : ra_5.5.rpt


****************************************
Report : area
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:40:27 2023
****************************************

Library(s) Used:
```

```
    saed32lvt_ss0p95v125c (File:
/home/user/Jenny/saed32nm/lib/stdcell_lvt/db_nldm/saed32lvt_ss0p95v125c.d
b)

Number of ports:                         3242
Number of nets:                         10880
Number of cells:                         6803
Number of combinational cells:           5251
Number of sequential cells:              1517
Number of macros/black boxes:               0
Number of buf/inv:                        910
Number of references:                       3

Combinational area:              12567.929131
Buf/Inv area:                     1432.863908
Noncombinational area:           10290.799128
Macro/Black Box area:                0.000000
Net Interconnect area:            6731.207507

Total cell area:                 22858.728259
Total area:                      29589.935766
1
Filename : ra_5.rpt


****************************************
Report : area
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:39:35 2023
****************************************

Library(s) Used:

    saed32lvt_ss0p95v125c (File:
/home/user/Jenny/saed32nm/lib/stdcell_lvt/db_nldm/saed32lvt_ss0p95v125c.d
b)

Number of ports:                         3242
Number of nets:                         10860
Number of cells:                         6783
Number of combinational cells:           5231
Number of sequential cells:              1517
Number of macros/black boxes:               0
Number of buf/inv:                        899
Number of references:                       3

Combinational area:              12575.807598
Buf/Inv area:                     1425.493731
Noncombinational area:           10290.799128
Macro/Black Box area:                0.000000
Net Interconnect area:            6727.600710

Total cell area:                 22866.606726
```

```
Total area:                    29594.207436
1
```

APPENDIX E: The Report Power of Technology 32nm with varies clock period.

```
Filename : rp_0.5.rpt

Loading db file
'/home/user/Jenny/saed32nm/lib/stdcell_lvt/db_nldm/saed32lvt_ss0p95v125c.
db'
Information: Propagating switching activity (low effort zero delay
simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
        -analysis_effort low
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:32:26 2023
****************************************


Library(s) Used:

    saed32lvt_ss0p95v125c (File:
/home/user/Jenny/saed32nm/lib/stdcell_lvt/db_nldm/saed32lvt_ss0p95v125c.d
b)


Operating Conditions: ss0p95v125c   Library: saed32lvt_ss0p95v125c
Wire Load Model Mode: enclosed

Design        Wire Load Model            Library
------------------------------------------------
riscv_pip_27           35000             saed32lvt_ss0p95v125c
controller             8000              saed32lvt_ss0p95v125c
hazardunit             8000              saed32lvt_ss0p95v125c
datapath               35000             saed32lvt_ss0p95v125c
maindec                ForQA             saed32lvt_ss0p95v125c
aludec                 ForQA             saed32lvt_ss0p95v125c
c_ID_IEx               ForQA             saed32lvt_ss0p95v125c
c_IEx_IM               ForQA             saed32lvt_ss0p95v125c
c_IM_IW                ForQA             saed32lvt_ss0p95v125c
mux2_0                 ForQA             saed32lvt_ss0p95v125c
flopenr                8000              saed32lvt_ss0p95v125c
adder_0                8000              saed32lvt_ss0p95v125c
IF_ID                  8000              saed32lvt_ss0p95v125c
regfile                35000             saed32lvt_ss0p95v125c
extend                 ForQA             saed32lvt_ss0p95v125c
ID_IEx                 8000              saed32lvt_ss0p95v125c
mux3_0                 ForQA             saed32lvt_ss0p95v125c
alu                    8000              saed32lvt_ss0p95v125c
IEx_IMem               8000              saed32lvt_ss0p95v125c
IMem_IW                8000              saed32lvt_ss0p95v125c
adder_1                8000              saed32lvt_ss0p95v125c
mux2_1                 ForQA             saed32lvt_ss0p95v125c
mux2_2                 ForQA             saed32lvt_ss0p95v125c
```

```
mux3_1                ForQA             saed32lvt_ss0p95v125c
mux3_2                ForQA             saed32lvt_ss0p95v125c
mux3_3                ForQA             saed32lvt_ss0p95v125c
adder_1_DW01_add_3    8000              saed32lvt_ss0p95v125c
adder_0_DW01_add_1    8000              saed32lvt_ss0p95v125c
alu_DW01_add_6        8000              saed32lvt_ss0p95v125c
alu_DW_cmp_6          8000              saed32lvt_ss0p95v125c


Global Operating Voltage = 0.95
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =  20.4086 mW   (97%)
  Net Switching Power  = 612.2123 uW    (3%)
                         ---------
Total Dynamic Power    =  21.0208 mW  (100%)

Cell Leakage Power     =   9.9728 mW


                 Internal         Switching           Leakage
Total
Power Group      Power            Power               Power
Power   (   %    )  Attrs
--------------------------------------------------------------------------------
-------------------------
io_pad             0.0000            0.0000            0.0000
0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000
0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000
0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000
0.0000  (   0.00%)
register       1.9303e+04           76.7453        5.9498e+09
2.5330e+04  (  81.73%)
sequential         0.0000            0.0000            0.0000
0.0000  (   0.00%)
combinational  1.1052e+03          535.4655        4.0230e+09
5.6637e+03  (  18.27%)
--------------------------------------------------------------------------------
-------------------------
Total          2.0409e+04 uW       612.2108 uW     9.9728e+09 pW
3.0994e+04 uW
1
Filename : rp_1.5.rpt
```

```
Loading db file
'/home/user/Jenny/saed32nm/lib/stdcell_lvt/db_nldm/saed32lvt_ss0p95v125c.
db'
Information: Propagating switching activity (low effort zero delay
simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
        -analysis_effort low
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 03:10:15 2023
****************************************


Library(s) Used:

    saed32lvt_ss0p95v125c (File:
/home/user/Jenny/saed32nm/lib/stdcell_lvt/db_nldm/saed32lvt_ss0p95v125c.d
b)


Operating Conditions: ss0p95v125c   Library: saed32lvt_ss0p95v125c
Wire Load Model Mode: enclosed

Design        Wire Load Model            Library
------------------------------------------------
riscv_pip_27           35000             saed32lvt_ss0p95v125c
controller             8000              saed32lvt_ss0p95v125c
hazardunit             8000              saed32lvt_ss0p95v125c
datapath               35000             saed32lvt_ss0p95v125c
maindec                ForQA             saed32lvt_ss0p95v125c
aludec                 ForQA             saed32lvt_ss0p95v125c
c_ID_IEx               ForQA             saed32lvt_ss0p95v125c
c_IEx_IM               ForQA             saed32lvt_ss0p95v125c
c_IM_IW                ForQA             saed32lvt_ss0p95v125c
mux2_0                 ForQA             saed32lvt_ss0p95v125c
flopenr                8000              saed32lvt_ss0p95v125c
adder_0                8000              saed32lvt_ss0p95v125c
IF_ID                  8000              saed32lvt_ss0p95v125c
regfile                16000             saed32lvt_ss0p95v125c
extend                 ForQA             saed32lvt_ss0p95v125c
ID_IEx                 8000              saed32lvt_ss0p95v125c
mux3_0                 ForQA             saed32lvt_ss0p95v125c
alu                    8000              saed32lvt_ss0p95v125c
IEx_IMem               8000              saed32lvt_ss0p95v125c
IMem_IW                8000              saed32lvt_ss0p95v125c
adder_1                8000              saed32lvt_ss0p95v125c
mux2_1                 ForQA             saed32lvt_ss0p95v125c
mux2_2                 ForQA             saed32lvt_ss0p95v125c
mux3_1                 ForQA             saed32lvt_ss0p95v125c
mux3_2                 ForQA             saed32lvt_ss0p95v125c
```

```
mux3_3                  ForQA             saed32lvt_ss0p95v125c
alu_DW_cmp_2            8000              saed32lvt_ss0p95v125c
adder_1_DW01_add_3      8000              saed32lvt_ss0p95v125c
adder_0_DW01_add_1      8000              saed32lvt_ss0p95v125c
alu_DW01_add_6          8000              saed32lvt_ss0p95v125c


Global Operating Voltage = 0.95
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   6.8475 mW   (97%)
  Net Switching Power  = 222.1905 uW    (3%)
                         ---------
Total Dynamic Power    =   7.0697 mW  (100%)

Cell Leakage Power     =   9.8288 mW


                 Internal         Switching           Leakage
Total
Power Group      Power            Power               Power
Power   (   %    )  Attrs
--------------------------------------------------------------------------------
-------------------------
io_pad             0.0000            0.0000            0.0000
0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000
0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000
0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000
0.0000  (   0.00%)
register        6.4207e+03           25.4827        5.9475e+09
1.2394e+04  (  73.34%)
sequential         0.0000            0.0000            0.0000
0.0000  (   0.00%)
combinational    426.7951          196.7075        3.8813e+09
4.5048e+03  (  26.66%)
--------------------------------------------------------------------------------
-------------------------
Total          6.8475e+03 uW       222.1903 uW     9.8288e+09 pW
1.6898e+04 uW
1
Filename : rp_1.rpt

Loading db file
'/home/user/Jenny/saed32nm/lib/stdcell_lvt/db_nldm/saed32lvt_ss0p95v125c.
db'
```

```
Information: Propagating switching activity (low effort zero delay
simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
        -analysis_effort low
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:35:08 2023
****************************************


Library(s) Used:

    saed32lvt_ss0p95v125c (File:
/home/user/Jenny/saed32nm/lib/stdcell_lvt/db_nldm/saed32lvt_ss0p95v125c.d
b)


Operating Conditions: ss0p95v125c   Library: saed32lvt_ss0p95v125c
Wire Load Model Mode: enclosed

Design         Wire Load Model            Library
------------------------------------------------
riscv_pip_27           35000              saed32lvt_ss0p95v125c
controller             8000               saed32lvt_ss0p95v125c
hazardunit             ForQA              saed32lvt_ss0p95v125c
datapath               35000              saed32lvt_ss0p95v125c
maindec                ForQA              saed32lvt_ss0p95v125c
aludec                 ForQA              saed32lvt_ss0p95v125c
c_ID_IEx               ForQA              saed32lvt_ss0p95v125c
c_IEx_IM               ForQA              saed32lvt_ss0p95v125c
c_IM_IW                ForQA              saed32lvt_ss0p95v125c
mux2_0                 ForQA              saed32lvt_ss0p95v125c
mux2_2                 ForQA              saed32lvt_ss0p95v125c
flopenr                8000               saed32lvt_ss0p95v125c
adder_0                8000               saed32lvt_ss0p95v125c
IF_ID                  8000               saed32lvt_ss0p95v125c
regfile                16000              saed32lvt_ss0p95v125c
extend                 ForQA              saed32lvt_ss0p95v125c
ID_IEx                 8000               saed32lvt_ss0p95v125c
mux3_0                 ForQA              saed32lvt_ss0p95v125c
mux2_1                 ForQA              saed32lvt_ss0p95v125c
mux3_3                 ForQA              saed32lvt_ss0p95v125c
mux3_2                 ForQA              saed32lvt_ss0p95v125c
adder_1                8000               saed32lvt_ss0p95v125c
alu                    8000               saed32lvt_ss0p95v125c
IEx_IMem               8000               saed32lvt_ss0p95v125c
IMem_IW                8000               saed32lvt_ss0p95v125c
mux3_1                 ForQA              saed32lvt_ss0p95v125c
adder_0_DW01_add_1     8000               saed32lvt_ss0p95v125c
adder_1_DW01_add_3     8000               saed32lvt_ss0p95v125c
```

```
alu_DW_cmp_6           8000              saed32lvt_ss0p95v125c
alu_DW01_add_6         8000              saed32lvt_ss0p95v125c


Global Operating Voltage = 0.95
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   9.9675 mW   (97%)
  Net Switching Power  = 289.1320 uW    (3%)
                         ---------
Total Dynamic Power    =  10.2566 mW  (100%)

Cell Leakage Power     =  10.0462 mW


                 Internal         Switching           Leakage
Total
Power Group      Power            Power               Power
Power   (   %    )  Attrs
--------------------------------------------------------------------------------
-------------------------
io_pad             0.0000            0.0000            0.0000
0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000
0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000
0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000
0.0000  (   0.00%)
register       9.4464e+03           36.8471        5.8197e+09
1.5303e+04  (  75.37%)
sequential         0.0000            0.0000            0.0000
0.0000  (   0.00%)
combinational    521.0922          252.2871        4.2264e+09
4.9998e+03  (  24.63%)
--------------------------------------------------------------------------------
-------------------------
Total          9.9675e+03 uW       289.1342 uW     1.0046e+10 pW
2.0303e+04 uW
1
Filename : rp_2.rpt

Loading db file
'/home/user/Jenny/saed32nm/lib/stdcell_lvt/db_nldm/saed32lvt_ss0p95v125c.
db'
Information: Propagating switching activity (low effort zero delay
simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
```

```
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
        -analysis_effort low
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:36:59 2023
****************************************


Library(s) Used:

    saed32lvt_ss0p95v125c (File:
/home/user/Jenny/saed32nm/lib/stdcell_lvt/db_nldm/saed32lvt_ss0p95v125c.d
b)


Operating Conditions: ss0p95v125c   Library: saed32lvt_ss0p95v125c
Wire Load Model Mode: enclosed

Design         Wire Load Model            Library
------------------------------------------------
riscv_pip_27           35000              saed32lvt_ss0p95v125c
controller             8000               saed32lvt_ss0p95v125c
hazardunit             ForQA              saed32lvt_ss0p95v125c
datapath               35000              saed32lvt_ss0p95v125c
maindec                ForQA              saed32lvt_ss0p95v125c
aludec                 ForQA              saed32lvt_ss0p95v125c
c_ID_IEx               ForQA              saed32lvt_ss0p95v125c
c_IEx_IM               ForQA              saed32lvt_ss0p95v125c
c_IM_IW                ForQA              saed32lvt_ss0p95v125c
mux2_0                 ForQA              saed32lvt_ss0p95v125c
mux2_2                 ForQA              saed32lvt_ss0p95v125c
flopenr                8000               saed32lvt_ss0p95v125c
adder_0                8000               saed32lvt_ss0p95v125c
IF_ID                  8000               saed32lvt_ss0p95v125c
regfile                16000              saed32lvt_ss0p95v125c
extend                 ForQA              saed32lvt_ss0p95v125c
ID_IEx                 8000               saed32lvt_ss0p95v125c
mux3_0                 ForQA              saed32lvt_ss0p95v125c
mux2_1                 ForQA              saed32lvt_ss0p95v125c
mux3_3                 ForQA              saed32lvt_ss0p95v125c
mux3_2                 ForQA              saed32lvt_ss0p95v125c
adder_1                8000               saed32lvt_ss0p95v125c
alu                    8000               saed32lvt_ss0p95v125c
IEx_IMem               8000               saed32lvt_ss0p95v125c
IMem_IW                8000               saed32lvt_ss0p95v125c
mux3_1                 ForQA              saed32lvt_ss0p95v125c
adder_0_DW01_add_1     8000               saed32lvt_ss0p95v125c
adder_1_DW01_add_3     8000               saed32lvt_ss0p95v125c
alu_DW_cmp_6           8000               saed32lvt_ss0p95v125c
alu_DW01_add_6         8000               saed32lvt_ss0p95v125c
```

```
Global Operating Voltage = 0.95
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   4.9425 mW   (97%)
  Net Switching Power  = 141.6218 uW    (3%)
                         ---------
Total Dynamic Power    =   5.0842 mW  (100%)

Cell Leakage Power     =   9.8222 mW


                 Internal         Switching           Leakage
Total
Power Group      Power            Power               Power
Power   (   %    )  Attrs
--------------------------------------------------------------------------------
------------------------
io_pad             0.0000            0.0000            0.0000
0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000
0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000
0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000
0.0000  (   0.00%)
register       4.7237e+03           19.0937        5.8186e+09
1.0561e+04  (  70.85%)
sequential         0.0000            0.0000            0.0000
0.0000  (   0.00%)
combinational    218.8839          122.5281        4.0036e+09
4.3451e+03  (  29.15%)
--------------------------------------------------------------------------------
------------------------
Total          4.9425e+03 uW       141.6217 uW     9.8222e+09 pW
1.4906e+04 uW
1
Filename : rp_3.rpt

Loading db file
'/home/user/Jenny/saed32nm/lib/stdcell_lvt/db_nldm/saed32lvt_ss0p95v125c.
db'
Information: Propagating switching activity (low effort zero delay
simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
```

```
Report : power
        -analysis_effort low
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:37:52 2023
****************************************


Library(s) Used:

    saed32lvt_ss0p95v125c (File:
/home/user/Jenny/saed32nm/lib/stdcell_lvt/db_nldm/saed32lvt_ss0p95v125c.d
b)


Operating Conditions: ss0p95v125c   Library: saed32lvt_ss0p95v125c
Wire Load Model Mode: enclosed

Design        Wire Load Model            Library
------------------------------------------------
riscv_pip_27           35000             saed32lvt_ss0p95v125c
controller             8000              saed32lvt_ss0p95v125c
hazardunit             ForQA             saed32lvt_ss0p95v125c
datapath               35000             saed32lvt_ss0p95v125c
maindec                ForQA             saed32lvt_ss0p95v125c
aludec                 ForQA             saed32lvt_ss0p95v125c
c_ID_IEx               ForQA             saed32lvt_ss0p95v125c
c_IEx_IM               ForQA             saed32lvt_ss0p95v125c
c_IM_IW                ForQA             saed32lvt_ss0p95v125c
mux2_0                 ForQA             saed32lvt_ss0p95v125c
mux2_2                 ForQA             saed32lvt_ss0p95v125c
flopenr                8000              saed32lvt_ss0p95v125c
adder_0                8000              saed32lvt_ss0p95v125c
IF_ID                  8000              saed32lvt_ss0p95v125c
regfile                16000             saed32lvt_ss0p95v125c
extend                 ForQA             saed32lvt_ss0p95v125c
ID_IEx                 8000              saed32lvt_ss0p95v125c
mux3_0                 ForQA             saed32lvt_ss0p95v125c
mux2_1                 ForQA             saed32lvt_ss0p95v125c
mux3_3                 ForQA             saed32lvt_ss0p95v125c
mux3_2                 ForQA             saed32lvt_ss0p95v125c
adder_1                8000              saed32lvt_ss0p95v125c
alu                    8000              saed32lvt_ss0p95v125c
IEx_IMem               8000              saed32lvt_ss0p95v125c
IMem_IW                8000              saed32lvt_ss0p95v125c
mux3_1                 ForQA             saed32lvt_ss0p95v125c
adder_0_DW01_add_1     8000              saed32lvt_ss0p95v125c
adder_1_DW01_add_3     8000              saed32lvt_ss0p95v125c
alu_DW_cmp_6           8000              saed32lvt_ss0p95v125c
alu_DW01_add_6         8000              saed32lvt_ss0p95v125c


Global Operating Voltage = 0.95
Power-specific unit information :
```

```
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   3.2823 mW   (97%)
  Net Switching Power  =  95.6952 uW    (3%)
                         ---------
Total Dynamic Power    =   3.3780 mW  (100%)

Cell Leakage Power     =   9.7931 mW


                 Internal         Switching           Leakage
Total
Power Group      Power            Power               Power
Power   (   %    )  Attrs
--------------------------------------------------------------------------
------------------------
io_pad             0.0000            0.0000            0.0000
0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000
0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000
0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000
0.0000  (   0.00%)
register       3.1454e+03           12.8262        5.8163e+09
8.9744e+03  (  68.14%)
sequential         0.0000            0.0000            0.0000
0.0000  (   0.00%)
combinational    136.9621           82.8691        3.9768e+09
4.1966e+03  (  31.86%)
--------------------------------------------------------------------------
------------------------
Total          3.2823e+03 uW        95.6953 uW     9.7931e+09 pW
1.3171e+04 uW
1
Filename : rp_4.rpt

Loading db file
'/home/user/Jenny/saed32nm/lib/stdcell_lvt/db_nldm/saed32lvt_ss0p95v125c.
db'
Information: Propagating switching activity (low effort zero delay
simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
        -analysis_effort low
Design : riscv_pip_27
```

```
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:38:45 2023
****************************************


Library(s) Used:

    saed32lvt_ss0p95v125c (File:
/home/user/Jenny/saed32nm/lib/stdcell_lvt/db_nldm/saed32lvt_ss0p95v125c.d
b)


Operating Conditions: ss0p95v125c   Library: saed32lvt_ss0p95v125c
Wire Load Model Mode: enclosed

Design         Wire Load Model            Library
------------------------------------------------
riscv_pip_27           35000              saed32lvt_ss0p95v125c
controller             8000               saed32lvt_ss0p95v125c
hazardunit             ForQA              saed32lvt_ss0p95v125c
datapath               35000              saed32lvt_ss0p95v125c
maindec                ForQA              saed32lvt_ss0p95v125c
aludec                 ForQA              saed32lvt_ss0p95v125c
c_ID_IEx               ForQA              saed32lvt_ss0p95v125c
c_IEx_IM               ForQA              saed32lvt_ss0p95v125c
c_IM_IW                ForQA              saed32lvt_ss0p95v125c
mux2_0                 ForQA              saed32lvt_ss0p95v125c
mux2_2                 ForQA              saed32lvt_ss0p95v125c
flopenr                8000               saed32lvt_ss0p95v125c
adder_0                8000               saed32lvt_ss0p95v125c
IF_ID                  8000               saed32lvt_ss0p95v125c
regfile                16000              saed32lvt_ss0p95v125c
extend                 ForQA              saed32lvt_ss0p95v125c
ID_IEx                 8000               saed32lvt_ss0p95v125c
mux3_0                 ForQA              saed32lvt_ss0p95v125c
mux2_1                 ForQA              saed32lvt_ss0p95v125c
mux3_3                 ForQA              saed32lvt_ss0p95v125c
mux3_2                 ForQA              saed32lvt_ss0p95v125c
adder_1                8000               saed32lvt_ss0p95v125c
alu                    8000               saed32lvt_ss0p95v125c
IEx_IMem               8000               saed32lvt_ss0p95v125c
IMem_IW                8000               saed32lvt_ss0p95v125c
mux3_1                 ForQA              saed32lvt_ss0p95v125c
adder_0_DW01_add_1     8000               saed32lvt_ss0p95v125c
adder_1_DW01_add_3     8000               saed32lvt_ss0p95v125c
alu_DW_cmp_6           8000               saed32lvt_ss0p95v125c
alu_DW01_add_6         8000               saed32lvt_ss0p95v125c


Global Operating Voltage = 0.95
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
```

```
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   2.4606 mW   (97%)
  Net Switching Power  =  70.7064 uW    (3%)
                         ---------
Total Dynamic Power    =   2.5313 mW  (100%)

Cell Leakage Power     =   9.7944 mW


                 Internal         Switching           Leakage
Total
Power Group      Power            Power               Power
Power   (   %    )  Attrs
--------------------------------------------------------------------------------
------------------------
io_pad             0.0000            0.0000            0.0000
0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000
0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000
0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000
0.0000  (   0.00%)
register       2.3591e+03            9.6296        5.8163e+09
8.1850e+03  (  66.41%)
sequential         0.0000            0.0000            0.0000
0.0000  (   0.00%)
combinational    101.5376           61.0768        3.9782e+09
4.1408e+03  (  33.59%)
--------------------------------------------------------------------------------
------------------------
Total          2.4606e+03 uW        70.7064 uW     9.7944e+09 pW
1.2326e+04 uW
1
Filename : rp_5.5.rpt

Information: Propagating switching activity (low effort zero delay
simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
        -analysis_effort low
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:40:28 2023
****************************************


Library(s) Used:
```

```
    saed32lvt_ss0p95v125c (File:
/home/user/Jenny/saed32nm/lib/stdcell_lvt/db_nldm/saed32lvt_ss0p95v125c.d
b)


Operating Conditions: ss0p95v125c   Library: saed32lvt_ss0p95v125c
Wire Load Model Mode: enclosed

Design        Wire Load Model            Library
------------------------------------------------
riscv_pip_27          35000              saed32lvt_ss0p95v125c
controller            8000               saed32lvt_ss0p95v125c
hazardunit            ForQA              saed32lvt_ss0p95v125c
datapath              35000              saed32lvt_ss0p95v125c
maindec               ForQA              saed32lvt_ss0p95v125c
aludec                ForQA              saed32lvt_ss0p95v125c
c_ID_IEx              ForQA              saed32lvt_ss0p95v125c
c_IEx_IM              ForQA              saed32lvt_ss0p95v125c
c_IM_IW               ForQA              saed32lvt_ss0p95v125c
mux2_0                ForQA              saed32lvt_ss0p95v125c
mux2_2                ForQA              saed32lvt_ss0p95v125c
flopenr               8000               saed32lvt_ss0p95v125c
adder_0               8000               saed32lvt_ss0p95v125c
IF_ID                 8000               saed32lvt_ss0p95v125c
regfile               16000              saed32lvt_ss0p95v125c
extend                ForQA              saed32lvt_ss0p95v125c
ID_IEx                8000               saed32lvt_ss0p95v125c
mux3_0                ForQA              saed32lvt_ss0p95v125c
mux2_1                ForQA              saed32lvt_ss0p95v125c
mux3_3                ForQA              saed32lvt_ss0p95v125c
mux3_2                ForQA              saed32lvt_ss0p95v125c
adder_1               8000               saed32lvt_ss0p95v125c
alu                   8000               saed32lvt_ss0p95v125c
IEx_IMem              8000               saed32lvt_ss0p95v125c
IMem_IW               8000               saed32lvt_ss0p95v125c
mux3_1                ForQA              saed32lvt_ss0p95v125c
adder_0_DW01_add_1    8000               saed32lvt_ss0p95v125c
adder_1_DW01_add_3    8000               saed32lvt_ss0p95v125c
alu_DW_cmp_6          8000               saed32lvt_ss0p95v125c
alu_DW01_add_6        8000               saed32lvt_ss0p95v125c


Global Operating Voltage = 0.95
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   1.7897 mW   (97%)
  Net Switching Power  =  51.4605 uW    (3%)
```

```
                          ---------
Total Dynamic Power    =   1.8411 mW  (100%)

Cell Leakage Power     =   9.7984 mW


                 Internal         Switching           Leakage
Total
Power Group      Power            Power               Power
Power   (   %    )  Attrs
--------------------------------------------------------------------------
-------------------------
io_pad             0.0000            0.0000            0.0000
0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000
0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000
0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000
0.0000  (   0.00%)
register       1.7157e+03            7.0035        5.8163e+09
7.5390e+03  (  64.77%)
sequential         0.0000            0.0000            0.0000
0.0000  (   0.00%)
combinational     73.9731           44.4570        3.9822e+09
4.1006e+03  (  35.23%)
--------------------------------------------------------------------------
-------------------------
Total          1.7897e+03 uW        51.4606 uW     9.7984e+09 pW
1.1640e+04 uW
1
Filename : rp_5.rpt

Information: Propagating switching activity (low effort zero delay
simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
        -analysis_effort low
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:39:37 2023
****************************************


Library(s) Used:

    saed32lvt_ss0p95v125c (File:
/home/user/Jenny/saed32nm/lib/stdcell_lvt/db_nldm/saed32lvt_ss0p95v125c.d
b)
```

```
Operating Conditions: ss0p95v125c   Library: saed32lvt_ss0p95v125c
Wire Load Model Mode: enclosed

Design        Wire Load Model            Library
------------------------------------------------
riscv_pip_27           35000             saed32lvt_ss0p95v125c
controller             8000              saed32lvt_ss0p95v125c
hazardunit             ForQA             saed32lvt_ss0p95v125c
datapath               35000             saed32lvt_ss0p95v125c
maindec                ForQA             saed32lvt_ss0p95v125c
aludec                 ForQA             saed32lvt_ss0p95v125c
c_ID_IEx               ForQA             saed32lvt_ss0p95v125c
c_IEx_IM               ForQA             saed32lvt_ss0p95v125c
c_IM_IW                ForQA             saed32lvt_ss0p95v125c
mux2_0                 ForQA             saed32lvt_ss0p95v125c
mux2_2                 ForQA             saed32lvt_ss0p95v125c
flopenr                8000              saed32lvt_ss0p95v125c
adder_0                8000              saed32lvt_ss0p95v125c
IF_ID                  8000              saed32lvt_ss0p95v125c
regfile                16000             saed32lvt_ss0p95v125c
extend                 ForQA             saed32lvt_ss0p95v125c
ID_IEx                 8000              saed32lvt_ss0p95v125c
mux3_0                 ForQA             saed32lvt_ss0p95v125c
mux2_1                 ForQA             saed32lvt_ss0p95v125c
mux3_3                 ForQA             saed32lvt_ss0p95v125c
mux3_2                 ForQA             saed32lvt_ss0p95v125c
adder_1                8000              saed32lvt_ss0p95v125c
alu                    8000              saed32lvt_ss0p95v125c
IEx_IMem               8000              saed32lvt_ss0p95v125c
IMem_IW                8000              saed32lvt_ss0p95v125c
mux3_1                 ForQA             saed32lvt_ss0p95v125c
adder_0_DW01_add_1     8000              saed32lvt_ss0p95v125c
adder_1_DW01_add_3     8000              saed32lvt_ss0p95v125c
alu_DW_cmp_6           8000              saed32lvt_ss0p95v125c
alu_DW01_add_6         8000              saed32lvt_ss0p95v125c


Global Operating Voltage = 0.95
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   1.9682 mW   (97%)
  Net Switching Power  =  57.0302 uW    (3%)
                         ---------
Total Dynamic Power    =   2.0252 mW  (100%)

Cell Leakage Power     =   9.7803 mW
```

```
                 Internal         Switching           Leakage
Total
Power Group      Power            Power               Power
Power    (   %    )  Attrs
--------------------------------------------------------------------------------
------------------------
io_pad             0.0000           0.0000            0.0000
0.0000   (   0.00%)
memory             0.0000           0.0000            0.0000
0.0000   (   0.00%)
black_box          0.0000           0.0000            0.0000
0.0000   (   0.00%)
clock_network      0.0000           0.0000            0.0000
0.0000   (   0.00%)
register       1.8872e+03           7.6989        5.8163e+09
7.7112e+03   (  65.32%)
sequential         0.0000           0.0000            0.0000
0.0000   (   0.00%)
combinational     80.9905          49.3314        3.9640e+09
4.0943e+03   (  34.68%)
--------------------------------------------------------------------------------
------------------------
Total          1.9682e+03 uW       57.0303 uW     9.7803e+09 pW
1.1805e+04 uW
1
```

APPENDIX F: The Report Timing of Technology 32nm with varies clock period.

```
Filename : rt_0.5.rpt

Information: Updating design information... (UID-85)
Warning: Design 'riscv_pip_27' contains 1 high-fanout nets. A fanout
number of 1000 will be used for delay calculations involving these nets.
(TIM-134)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:32:23 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: ss0p95v125c   Library: saed32lvt_ss0p95v125c
Wire Load Model Mode: enclosed

  Startpoint: dp/pipreg2/RdM_reg[3]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: dp/IF/q_reg[12]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 saed32lvt_ss0p95v125c
  IEx_IMem           8000                  saed32lvt_ss0p95v125c
  hazardunit         8000                  saed32lvt_ss0p95v125c
  mux3_3             ForQA                 saed32lvt_ss0p95v125c
  datapath           35000                 saed32lvt_ss0p95v125c
  alu                8000                  saed32lvt_ss0p95v125c
  alu_DW01_add_6     8000                  saed32lvt_ss0p95v125c
  controller         8000                  saed32lvt_ss0p95v125c
  mux2_2             ForQA                 saed32lvt_ss0p95v125c
  flopenr            8000                  saed32lvt_ss0p95v125c

  Point                                                   Incr       Path
  --------------------------------------------------------------------------
---
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  dp/pipreg2/RdM_reg[3]/CLK (DFFARX2_LVT)                 0.00 #     0.00
r
  dp/pipreg2/RdM_reg[3]/QN (DFFARX2_LVT)                  0.11       0.11
r
  dp/pipreg2/U4/Y (INVX4_LVT)                             0.01       0.12
f
```

```
  dp/pipreg2/RdM[3] (IEx_IMem)                          0.00       0.12
f
  dp/RdM[3] (datapath)                                  0.00       0.12
f
  h/RdM[3] (hazardunit)                                 0.00       0.12
f
  h/U5/Y (INVX4_LVT)                                    0.01       0.13
r
  h/U12/Y (XNOR2X2_LVT)                                 0.06       0.20
f
  h/U3/Y (AND4X1_LVT)                                   0.07       0.26
f
  h/U43/Y (NAND2X0_LVT)                                 0.03       0.30
r
  h/U78/Y (NAND4X0_LVT)                                 0.03       0.33
f
  h/U65/Y (NOR2X2_LVT)                                  0.07       0.40
r
  h/ForwardBE[0] (hazardunit)                           0.00       0.40
r
  dp/ForwardBE[0] (datapath)                            0.00       0.40
r
  dp/forwardMuxB/s[0] (mux3_3)                          0.00       0.40
r
  dp/forwardMuxB/U44/Y (NAND2X4_LVT)                    0.06       0.46
f
  dp/forwardMuxB/U15/Y (INVX8_LVT)                      0.02       0.48
r
  dp/forwardMuxB/U87/Y (AO222X1_LVT)                    0.10       0.58
r
  dp/forwardMuxB/y[17] (mux3_3)                         0.00       0.58
r
  dp/srcbmux/d0[17] (mux3_2)                            0.00       0.58
r
  dp/srcbmux/U9/Y (AO222X2_LVT)                         0.09       0.67
r
  dp/srcbmux/y[17] (mux3_2)                             0.00       0.67
r
  dp/alu/SrcB[17] (alu)                                 0.00       0.67
r
  dp/alu/U285/Y (XOR2X2_LVT)                            0.07       0.75
f
  dp/alu/add_1_root_add_17_2/B[17] (alu_DW01_add_6)     0.00       0.75
f
  dp/alu/add_1_root_add_17_2/U362/Y (NOR2X1_LVT)        0.05       0.80
r
  dp/alu/add_1_root_add_17_2/U171/Y (NOR2X0_LVT)        0.05       0.85
f
  dp/alu/add_1_root_add_17_2/U170/Y (AOI21X1_LVT)       0.07       0.92
r
  dp/alu/add_1_root_add_17_2/U363/Y (OAI21X2_LVT)       0.06       0.98
f
  dp/alu/add_1_root_add_17_2/U375/Y (AOI21X1_LVT)       0.06       1.04
r
```

```
  dp/alu/add_1_root_add_17_2/U433/Y (OA21X1_LVT)          0.05       1.09
r
  dp/alu/add_1_root_add_17_2/U434/Y (XOR2X2_LVT)          0.06       1.15
f
  dp/alu/add_1_root_add_17_2/SUM[19] (alu_DW01_add_6)     0.00       1.15
f
  dp/alu/U523/Y (NAND2X0_LVT)                             0.03       1.18
r
  dp/alu/U174/Y (NAND2X0_LVT)                             0.04       1.22
f
  dp/alu/U785/Y (NOR4X1_LVT)                              0.09       1.31
r
  dp/alu/U176/Y (AND2X1_LVT)                              0.03       1.34
r
  dp/alu/U177/Y (AND3X1_LVT)                              0.04       1.39
r
  dp/alu/Zero (alu)                                       0.00       1.39
r
  dp/ZeroE (datapath)                                     0.00       1.39
r
  c/ZeroE (controller)                                    0.00       1.39
r
  c/U12/Y (NAND3X0_LVT)                                   0.03       1.42
f
  c/U5/Y (NAND2X0_LVT)                                    0.04       1.45
r
  c/U3/Y (OR2X2_LVT)                                      0.05       1.50
r
  c/PCSrcE (controller)                                   0.00       1.50
r
  dp/PCSrcE (datapath)                                    0.00       1.50
r
  dp/pcmux/s (mux2_2)                                     0.00       1.50
r
  dp/pcmux/U1/Y (NBUFFX4_LVT)                             0.06       1.56
r
  dp/pcmux/U16/Y (MUX21X1_LVT)                            0.07       1.63
f
  dp/pcmux/y[12] (mux2_2)                                 0.00       1.63
f
  dp/IF/d[12] (flopenr)                                   0.00       1.63
f
  dp/IF/U21/Y (MUX21X1_LVT)                               0.06       1.69
f
  dp/IF/q_reg[12]/D (DFFARX1_LVT)                         0.00       1.69
f
  data arrival time                                                  1.69

  clock clk (rise edge)                                   0.50       0.50
  clock network delay (ideal)                             0.00       0.50
  clock uncertainty                                      -0.10       0.40
  dp/IF/q_reg[12]/CLK (DFFARX1_LVT)                       0.00       0.40
r
  library setup time                                     -0.03       0.37
```

```
  data required time                                                 0.37
  -----------------------------------------------------------------------
---
  data required time                                                 0.37
  data arrival time                                                 -1.69
  -----------------------------------------------------------------------
---
  slack (VIOLATED)                                                  -1.32


1
Filename : rt_1.5.rpt

Information: Updating design information... (UID-85)
Warning: Design 'riscv_pip_27' contains 1 high-fanout nets. A fanout
number of 1000 will be used for delay calculations involving these nets.
(TIM-134)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 03:10:14 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: ss0p95v125c   Library: saed32lvt_ss0p95v125c
Wire Load Model Mode: enclosed

  Startpoint: dp/pipreg2/RdM_reg[2]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: dp/pipreg0/PCD_reg[26]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 saed32lvt_ss0p95v125c
  IEx_IMem           8000                  saed32lvt_ss0p95v125c
  hazardunit         8000                  saed32lvt_ss0p95v125c
  mux3_3             ForQA                 saed32lvt_ss0p95v125c
  datapath           35000                 saed32lvt_ss0p95v125c
  alu                8000                  saed32lvt_ss0p95v125c
  alu_DW01_add_6     8000                  saed32lvt_ss0p95v125c
  controller         8000                  saed32lvt_ss0p95v125c
  IF_ID              8000                  saed32lvt_ss0p95v125c

  Point                                                   Incr       Path
```

```
  ------------------------------------------------------------------------
---
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  dp/pipreg2/RdM_reg[2]/CLK (DFFARX2_LVT)                 0.00 #     0.00
r
  dp/pipreg2/RdM_reg[2]/QN (DFFARX2_LVT)                  0.10       0.10
r
  dp/pipreg2/U7/Y (INVX2_LVT)                             0.01       0.12
f
  dp/pipreg2/RdM[2] (IEx_IMem)                            0.00       0.12
f
  dp/RdM[2] (datapath)                                    0.00       0.12
f
  h/RdM[2] (hazardunit)                                   0.00       0.12
f
  h/U45/Y (NAND2X0_LVT)                                   0.03       0.15
r
  h/U46/Y (NAND2X0_LVT)                                   0.02       0.17
f
  h/U88/Y (AND4X1_LVT)                                    0.07       0.24
f
  h/U16/Y (NAND3X0_LVT)                                   0.03       0.27
r
  h/U33/Y (NAND3X0_LVT)                                   0.03       0.30
f
  h/U22/Y (OR2X2_LVT)                                     0.05       0.35
f
  h/U23/Y (INVX4_LVT)                                     0.02       0.37
r
  h/ForwardBE[0] (hazardunit)                             0.00       0.37
r
  dp/ForwardBE[0] (datapath)                              0.00       0.37
r
  dp/forwardMuxB/s[0] (mux3_3)                            0.00       0.37
r
  dp/forwardMuxB/U19/Y (NAND2X4_LVT)                      0.06       0.43
f
  dp/forwardMuxB/U5/Y (INVX4_LVT)                         0.02       0.45
r
  dp/forwardMuxB/U52/Y (AO222X1_LVT)                      0.10       0.55
r
  dp/forwardMuxB/y[9] (mux3_3)                            0.00       0.55
r
  dp/srcbmux/d0[9] (mux3_2)                               0.00       0.55
r
  dp/srcbmux/U17/Y (AO222X1_LVT)                          0.09       0.64
r
  dp/srcbmux/y[9] (mux3_2)                                0.00       0.64
r
  dp/alu/SrcB[9] (alu)                                    0.00       0.64
r
  dp/alu/U395/Y (XOR2X2_LVT)                              0.07       0.72
f
```

```
  dp/alu/add_1_root_add_17_2/B[9] (alu_DW01_add_6)        0.00       0.72
f
  dp/alu/add_1_root_add_17_2/U266/Y (NOR2X0_LVT)          0.05       0.77
r
  dp/alu/add_1_root_add_17_2/U262/Y (NOR2X0_LVT)          0.05       0.82
f
  dp/alu/add_1_root_add_17_2/U432/Y (AOI21X1_LVT)         0.07       0.89
r
  dp/alu/add_1_root_add_17_2/U413/Y (OA21X1_LVT)          0.05       0.94
r
  dp/alu/add_1_root_add_17_2/U366/Y (INVX2_LVT)           0.01       0.95
f
  dp/alu/add_1_root_add_17_2/U379/Y (NAND2X0_LVT)         0.03       0.98
r
  dp/alu/add_1_root_add_17_2/U380/Y (AND2X1_LVT)          0.04       1.02
r
  dp/alu/add_1_root_add_17_2/U491/Y (OA21X1_LVT)          0.05       1.06
r
  dp/alu/add_1_root_add_17_2/U490/Y (XOR2X2_LVT)          0.07       1.13
f
  dp/alu/add_1_root_add_17_2/SUM[20] (alu_DW01_add_6)     0.00       1.13
f
  dp/alu/U868/Y (INVX1_LVT)                               0.02       1.15
r
  dp/alu/U870/Y (OA22X1_LVT)                              0.05       1.20
r
  dp/alu/U872/Y (NAND4X0_LVT)                             0.04       1.24
f
  dp/alu/U374/Y (AOI221X1_LVT)                            0.06       1.30
r
  dp/alu/U372/Y (AND3X1_LVT)                              0.04       1.34
r
  dp/alu/Zero (alu)                                       0.00       1.34
r
  dp/ZeroE (datapath)                                     0.00       1.34
r
  c/ZeroE (controller)                                    0.00       1.34
r
  c/U2/Y (INVX0_LVT)                                      0.01       1.35
f
  c/U7/Y (AND2X1_LVT)                                     0.03       1.39
f
  c/U4/Y (OR2X2_LVT)                                      0.05       1.44
f
  c/PCSrcE (controller)                                   0.00       1.44
f
  h/PCSrcE (hazardunit)                                   0.00       1.44
f
  h/U10/Y (NBUFFX2_LVT)                                   0.04       1.48
f
  h/FlushD (hazardunit)                                   0.00       1.48
f
  dp/FlushD (datapath)                                    0.00       1.48
f
```

```
  dp/pipreg0/clear (IF_ID)                                0.00       1.48
f
  dp/pipreg0/U7/Y (OR2X2_LVT)                             0.05       1.53
f
  dp/pipreg0/U9/Y (INVX8_LVT)                             0.03       1.56
r
  dp/pipreg0/U80/Y (AO22X1_LVT)                           0.06       1.61
r
  dp/pipreg0/PCD_reg[26]/D (DFFARX1_LVT)                  0.00       1.61
r
  data arrival time                                                  1.61

  clock clk (rise edge)                                   1.50       1.50
  clock network delay (ideal)                             0.00       1.50
  clock uncertainty                                      -0.10       1.40
  dp/pipreg0/PCD_reg[26]/CLK (DFFARX1_LVT)                0.00       1.40
r
  library setup time                                     -0.04       1.36
  data required time                                                 1.36
  ------------------------------------------------------------------------
---
  data required time                                                 1.36
  data arrival time                                                 -1.61
  ------------------------------------------------------------------------
---
  slack (VIOLATED)                                                  -0.25


1
Filename : rt_1.rpt

Information: Updating design information... (UID-85)
Warning: Design 'riscv_pip_27' contains 1 high-fanout nets. A fanout
number of 1000 will be used for delay calculations involving these nets.
(TIM-134)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:35:04 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: ss0p95v125c   Library: saed32lvt_ss0p95v125c
Wire Load Model Mode: enclosed

  Startpoint: dp/pipreg1/Rs2E_reg[4]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: dp/pipreg0/InstrD_reg[14]
```

```
          (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 saed32lvt_ss0p95v125c
  ID_IEx             8000                  saed32lvt_ss0p95v125c
  hazardunit         ForQA                 saed32lvt_ss0p95v125c
  mux3_3             ForQA                 saed32lvt_ss0p95v125c
  datapath           35000                 saed32lvt_ss0p95v125c
  alu                8000                  saed32lvt_ss0p95v125c
  alu_DW01_add_6     8000                  saed32lvt_ss0p95v125c
  controller         8000                  saed32lvt_ss0p95v125c
  IF_ID              8000                  saed32lvt_ss0p95v125c

  Point                                                    Incr       Path
  ------------------------------------------------------------------------
---
  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  dp/pipreg1/Rs2E_reg[4]/CLK (DFFARX1_LVT)                 0.00 #     0.00
r
  dp/pipreg1/Rs2E_reg[4]/QN (DFFARX1_LVT)                  0.10       0.10
r
  dp/pipreg1/U16/Y (INVX2_LVT)                             0.02       0.12
f
  dp/pipreg1/Rs2E[4] (ID_IEx)                              0.00       0.12
f
  dp/Rs2E[4] (datapath)                                    0.00       0.12
f
  h/Rs2E[4] (hazardunit)                                   0.00       0.12
f
  h/U19/Y (INVX2_LVT)                                      0.02       0.14
r
  h/U58/Y (AND2X1_LVT)                                     0.04       0.17
r
  h/U59/Y (NAND4X0_LVT)                                    0.03       0.21
f
  h/U60/Y (NAND4X0_LVT)                                    0.05       0.25
r
  h/U61/Y (NOR3X0_LVT)                                     0.07       0.32
f
  h/U63/Y (NOR3X0_LVT)                                     0.06       0.38
r
  h/ForwardBE[0] (hazardunit)                              0.00       0.38
r
  dp/ForwardBE[0] (datapath)                               0.00       0.38
r
  dp/forwardMuxB/s[0] (mux3_3)                             0.00       0.38
r
  dp/forwardMuxB/U26/Y (INVX1_LVT)                         0.02       0.40
f
```

```
  dp/forwardMuxB/U34/Y (NAND2X4_LVT)                      0.07       0.47
r
  dp/forwardMuxB/U7/Y (INVX4_LVT)                         0.02       0.49
f
  dp/forwardMuxB/U19/Y (NAND2X0_LVT)                      0.03       0.52
r
  dp/forwardMuxB/U21/Y (NAND3X0_LVT)                      0.04       0.56
f
  dp/forwardMuxB/y[1] (mux3_3)                            0.00       0.56
f
  dp/srcbmux/d0[1] (mux3_2)                               0.00       0.56
f
  dp/srcbmux/U28/Y (AO222X2_LVT)                          0.06       0.62
f
  dp/srcbmux/y[1] (mux3_2)                                0.00       0.62
f
  dp/alu/SrcB[1] (alu)                                    0.00       0.62
f
  dp/alu/U147/Y (XOR2X2_LVT)                              0.08       0.70
r
  dp/alu/add_1_root_add_17_2/B[1] (alu_DW01_add_6)        0.00       0.70
r
  dp/alu/add_1_root_add_17_2/U526/Y (AND2X1_LVT)          0.03       0.73
r
  dp/alu/add_1_root_add_17_2/U331/Y (AOI21X1_LVT)         0.06       0.79
f
  dp/alu/add_1_root_add_17_2/U329/Y (OAI21X2_LVT)         0.07       0.86
r
  dp/alu/add_1_root_add_17_2/U360/Y (AO21X2_LVT)          0.07       0.93
r
  dp/alu/add_1_root_add_17_2/U394/Y (XNOR2X2_LVT)         0.07       1.00
r
  dp/alu/add_1_root_add_17_2/SUM[6] (alu_DW01_add_6)      0.00       1.00
r
  dp/alu/U642/Y (AO22X1_LVT)                              0.06       1.06
r
  dp/alu/U167/Y (AOI221X1_LVT)                            0.07       1.12
f
  dp/alu/U35/Y (AND3X1_LVT)                               0.04       1.17
f
  dp/alu/U888/Y (AND4X1_LVT)                              0.06       1.23
f
  dp/alu/U889/Y (NAND4X0_LVT)                             0.03       1.26
r
  dp/alu/U890/Y (NOR4X1_LVT)                              0.07       1.33
f
  dp/alu/U891/Y (NAND4X0_LVT)                             0.03       1.36
r
  dp/alu/U266/Y (INVX1_LVT)                               0.02       1.38
f
  dp/alu/Zero (alu)                                       0.00       1.38
f
  dp/ZeroE (datapath)                                     0.00       1.38
f
```

```
  c/ZeroE (controller)                                    0.00       1.38
f
  c/U14/Y (NAND2X0_LVT)                                   0.03       1.41
r
  c/U13/Y (NAND2X0_LVT)                                   0.02       1.43
f
  c/U12/Y (OR2X2_LVT)                                     0.05       1.48
f
  c/PCSrcE (controller)                                   0.00       1.48
f
  h/PCSrcE (hazardunit)                                   0.00       1.48
f
  h/FlushD (hazardunit)                                   0.00       1.48
f
  dp/FlushD (datapath)                                    0.00       1.48
f
  dp/pipreg0/clear (IF_ID)                                0.00       1.48
f
  dp/pipreg0/U4/Y (INVX1_LVT)                             0.04       1.52
r
  dp/pipreg0/U2/Y (AND2X4_LVT)                            0.07       1.59
r
  dp/pipreg0/U106/Y (AO22X1_LVT)                          0.06       1.65
r
  dp/pipreg0/InstrD_reg[14]/D (DFFARX1_LVT)               0.00       1.65
r
  data arrival time                                                  1.65

  clock clk (rise edge)                                   1.00       1.00
  clock network delay (ideal)                             0.00       1.00
  clock uncertainty                                      -0.10       0.90
  dp/pipreg0/InstrD_reg[14]/CLK (DFFARX1_LVT)             0.00       0.90
r
  library setup time                                     -0.04       0.86
  data required time                                                 0.86
  ---------------------------------------------------------------------------
---
  data required time                                                 0.86
  data arrival time                                                 -1.65
  ---------------------------------------------------------------------------
---
  slack (VIOLATED)                                                  -0.79


1
Filename : rt_2.rpt

Information: Updating design information... (UID-85)
Warning: Design 'riscv_pip_27' contains 1 high-fanout nets. A fanout
number of 1000 will be used for delay calculations involving these nets.
(TIM-134)

****************************************
Report : timing
```

```
        -path full
        -delay max
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:36:56 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: ss0p95v125c   Library: saed32lvt_ss0p95v125c
Wire Load Model Mode: enclosed

  Startpoint: dp/pipreg1/Rs1E_reg[2]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: dp/pipreg1/Rs2E_reg[0]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 saed32lvt_ss0p95v125c
  hazardunit         ForQA                 saed32lvt_ss0p95v125c
  mux3_0             ForQA                 saed32lvt_ss0p95v125c
  datapath           35000                 saed32lvt_ss0p95v125c
  alu_DW01_add_6     8000                  saed32lvt_ss0p95v125c
  alu                8000                  saed32lvt_ss0p95v125c
  controller         8000                  saed32lvt_ss0p95v125c
  ID_IEx             8000                  saed32lvt_ss0p95v125c

  Point                                                   Incr       Path
  --------------------------------------------------------------------------
---
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  dp/pipreg1/Rs1E_reg[2]/CLK (DFFARX1_LVT)                0.00 #     0.00
r
  dp/pipreg1/Rs1E_reg[2]/Q (DFFARX1_LVT)                  0.14       0.14
f
  dp/pipreg1/Rs1E[2] (ID_IEx)                             0.00       0.14
f
  dp/Rs1E[2] (datapath)                                   0.00       0.14
f
  h/Rs1E[2] (hazardunit)                                  0.00       0.14
f
  h/U70/Y (INVX1_LVT)                                     0.02       0.16
r
  h/U20/Y (NAND3X0_LVT)                                   0.04       0.19
f
  h/U19/Y (OR3X1_LVT)                                     0.05       0.24
f
  h/U72/Y (AND2X1_LVT)                                    0.04       0.28
f
```

```
  h/U32/Y (NAND3X0_LVT)                                0.03       0.31
r
  h/U31/Y (NOR3X0_LVT)                                 0.07       0.39
f
  h/U73/Y (NOR4X1_LVT)                                 0.08       0.47
r
  h/ForwardAE[0] (hazardunit)                          0.00       0.47
r
  dp/ForwardAE[0] (datapath)                           0.00       0.47
r
  dp/forwardMuxA/s[0] (mux3_0)                         0.00       0.47
r
  dp/forwardMuxA/U2/Y (AND2X2_LVT)                     0.06       0.52
r
  dp/forwardMuxA/U6/Y (NBUFFX2_LVT)                    0.06       0.58
r
  dp/forwardMuxA/U32/Y (AO222X1_LVT)                   0.10       0.68
r
  dp/forwardMuxA/y[19] (mux3_0)                        0.00       0.68
r
  dp/srcamux/d0[19] (mux2_1)                           0.00       0.68
r
  dp/srcamux/U23/Y (AO22X1_LVT)                        0.07       0.76
r
  dp/srcamux/y[19] (mux2_1)                            0.00       0.76
r
  dp/alu/SrcA[19] (alu)                                0.00       0.76
r
  dp/alu/add_1_root_add_17_2/A[19] (alu_DW01_add_6)    0.00       0.76
r
  dp/alu/add_1_root_add_17_2/U410/Y (NOR2X1_LVT)       0.07       0.82
f
  dp/alu/add_1_root_add_17_2/U434/Y (OAI21X2_LVT)      0.08       0.90
r
  dp/alu/add_1_root_add_17_2/U449/Y (AND2X1_LVT)       0.04       0.94
r
  dp/alu/add_1_root_add_17_2/U448/Y (NOR2X0_LVT)       0.05       0.99
f
  dp/alu/add_1_root_add_17_2/U396/Y (OAI21X2_LVT)      0.08       1.07
r
  dp/alu/add_1_root_add_17_2/U393/Y (AOI21X1_LVT)      0.06       1.14
f
  dp/alu/add_1_root_add_17_2/U473/Y (OA21X1_LVT)       0.04       1.18
f
  dp/alu/add_1_root_add_17_2/U401/Y (INVX1_LVT)        0.02       1.20
r
  dp/alu/add_1_root_add_17_2/U399/Y (NAND2X0_LVT)      0.02       1.21
f
  dp/alu/add_1_root_add_17_2/U400/Y (NAND2X0_LVT)      0.03       1.25
r
  dp/alu/add_1_root_add_17_2/SUM[28] (alu_DW01_add_6)  0.00       1.25
r
  dp/alu/U469/Y (AO22X1_LVT)                           0.06       1.30
r
```

```
  dp/alu/U167/Y (AOI221X1_LVT)                          0.07       1.37
f
  dp/alu/U54/Y (AND2X1_LVT)                             0.04       1.41
f
  dp/alu/U753/Y (NAND4X0_LVT)                           0.03       1.44
r
  dp/alu/U757/Y (NOR4X1_LVT)                            0.08       1.51
f
  dp/alu/U777/Y (AND2X1_LVT)                            0.04       1.55
f
  dp/alu/Zero (alu)                                     0.00       1.55
f
  dp/ZeroE (datapath)                                   0.00       1.55
f
  c/ZeroE (controller)                                  0.00       1.55
f
  c/U11/Y (NAND3X0_LVT)                                 0.03       1.58
r
  c/U4/Y (NAND4X0_LVT)                                  0.06       1.64
f
  c/PCSrcE (controller)                                 0.00       1.64
f
  h/PCSrcE (hazardunit)                                 0.00       1.64
f
  h/U13/Y (INVX1_LVT)                                   0.04       1.68
r
  h/U57/Y (NAND2X0_LVT)                                 0.03       1.71
f
  h/FlushE (hazardunit)                                 0.00       1.71
f
  dp/FlushE (datapath)                                  0.00       1.71
f
  dp/pipreg1/clear (ID_IEx)                             0.00       1.71
f
  dp/pipreg1/U8/Y (NBUFFX2_LVT)                         0.05       1.76
f
  dp/pipreg1/U25/Y (INVX2_LVT)                          0.03       1.78
r
  dp/pipreg1/U22/Y (NBUFFX2_LVT)                        0.05       1.83
r
  dp/pipreg1/U97/Y (AND2X1_LVT)                         0.04       1.86
r
  dp/pipreg1/Rs2E_reg[0]/D (DFFARX1_LVT)                0.00       1.86
r
  data arrival time                                                1.86

  clock clk (rise edge)                                 2.00       2.00
  clock network delay (ideal)                           0.00       2.00
  clock uncertainty                                    -0.10       1.90
  dp/pipreg1/Rs2E_reg[0]/CLK (DFFARX1_LVT)              0.00       1.90
r
  library setup time                                   -0.03       1.87
  data required time                                               1.87
```

```
  ------------------------------------------------------------------------
---
  data required time                                                  1.87
  data arrival time                                                  -1.86
  ------------------------------------------------------------------------
---
  slack (MET)                                                         0.00


1
Filename : rt_3.rpt

Information: Updating design information... (UID-85)
Warning: Design 'riscv_pip_27' contains 1 high-fanout nets. A fanout
number of 1000 will be used for delay calculations involving these nets.
(TIM-134)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:37:48 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: ss0p95v125c   Library: saed32lvt_ss0p95v125c
Wire Load Model Mode: enclosed

  Startpoint: dp/pipreg1/Rs2E_reg[3]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: dp/IF/q_reg[5]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 saed32lvt_ss0p95v125c
  hazardunit         ForQA                 saed32lvt_ss0p95v125c
  mux3_3             ForQA                 saed32lvt_ss0p95v125c
  datapath           35000                 saed32lvt_ss0p95v125c
  alu                8000                  saed32lvt_ss0p95v125c
  alu_DW01_add_6     8000                  saed32lvt_ss0p95v125c
  controller         8000                  saed32lvt_ss0p95v125c
  mux2_2             ForQA                 saed32lvt_ss0p95v125c
  flopenr            8000                  saed32lvt_ss0p95v125c

  Point                                                   Incr       Path
  ------------------------------------------------------------------------
---
```

```
  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  dp/pipreg1/Rs2E_reg[3]/CLK (DFFARX1_LVT)                 0.00 #     0.00
r
  dp/pipreg1/Rs2E_reg[3]/Q (DFFARX1_LVT)                   0.13       0.13
f
  dp/pipreg1/Rs2E[3] (ID_IEx)                              0.00       0.13
f
  dp/Rs2E[3] (datapath)                                    0.00       0.13
f
  h/Rs2E[3] (hazardunit)                                   0.00       0.13
f
  h/U40/Y (OR3X1_LVT)                                      0.06       0.19
f
  h/U39/Y (OR3X1_LVT)                                      0.05       0.24
f
  h/U38/Y (AND4X1_LVT)                                     0.07       0.31
f
  h/U37/Y (AND4X1_LVT)                                     0.09       0.41
f
  h/U3/Y (NOR4X1_LVT)                                      0.09       0.49
r
  h/ForwardBE[0] (hazardunit)                              0.00       0.49
r
  dp/ForwardBE[0] (datapath)                               0.00       0.49
r
  dp/forwardMuxB/s[0] (mux3_3)                             0.00       0.49
r
  dp/forwardMuxB/U35/Y (AND2X1_LVT)                        0.06       0.55
r
  dp/forwardMuxB/U36/Y (NBUFFX2_LVT)                       0.06       0.61
r
  dp/forwardMuxB/U11/Y (AO222X1_LVT)                       0.10       0.72
r
  dp/forwardMuxB/y[2] (mux3_3)                             0.00       0.72
r
  dp/srcbmux/d0[2] (mux3_2)                                0.00       0.72
r
  dp/srcbmux/U1/Y (AO222X2_LVT)                            0.13       0.85
r
  dp/srcbmux/y[2] (mux3_2)                                 0.00       0.85
r
  dp/alu/SrcB[2] (alu)                                     0.00       0.85
r
  dp/alu/U137/Y (INVX2_LVT)                                0.05       0.90
f
  dp/alu/U77/Y (XNOR2X1_LVT)                               0.09       0.99
r
  dp/alu/add_1_root_add_17_2/B[2] (alu_DW01_add_6)         0.00       0.99
r
  dp/alu/add_1_root_add_17_2/U376/Y (OR2X1_LVT)            0.04       1.04
r
  dp/alu/add_1_root_add_17_2/U556/Y (INVX1_LVT)            0.01       1.05
f
```

```
  dp/alu/add_1_root_add_17_2/U413/Y (OA21X1_LVT)          0.04       1.09
f
  dp/alu/add_1_root_add_17_2/U430/Y (OAI21X1_LVT)         0.07       1.17
r
  dp/alu/add_1_root_add_17_2/U373/Y (AO21X1_LVT)          0.05       1.22
r
  dp/alu/add_1_root_add_17_2/U432/Y (AO21X1_LVT)          0.06       1.28
r
  dp/alu/add_1_root_add_17_2/U388/Y (AOI21X1_LVT)         0.07       1.35
f
  dp/alu/add_1_root_add_17_2/U518/Y (OA21X1_LVT)          0.05       1.40
f
  dp/alu/add_1_root_add_17_2/U548/Y (XOR2X1_LVT)          0.08       1.48
r
  dp/alu/add_1_root_add_17_2/SUM[31] (alu_DW01_add_6)     0.00       1.48
r
  dp/alu/U203/Y (OA221X1_LVT)                             0.06       1.54
r
  dp/alu/U202/Y (NAND3X0_LVT)                             0.03       1.57
f
  dp/alu/U201/Y (OA221X1_LVT)                             0.06       1.64
f
  dp/alu/U196/Y (NAND4X0_LVT)                             0.05       1.69
r
  dp/alu/U123/Y (OR4X1_LVT)                               0.08       1.77
r
  dp/alu/U6/Y (NOR4X1_LVT)                                0.08       1.85
f
  dp/alu/U195/Y (AND2X1_LVT)                              0.04       1.89
f
  dp/alu/Zero (alu)                                       0.00       1.89
f
  dp/ZeroE (datapath)                                     0.00       1.89
f
  c/ZeroE (controller)                                    0.00       1.89
f
  c/U4/Y (XOR2X1_LVT)                                     0.08       1.97
r
  c/U6/Y (AO22X1_LVT)                                     0.04       2.02
r
  c/U5/Y (AO21X1_LVT)                                     0.06       2.08
r
  c/PCSrcE (controller)                                   0.00       2.08
r
  dp/PCSrcE (datapath)                                    0.00       2.08
r
  dp/pcmux/s (mux2_2)                                     0.00       2.08
r
  dp/pcmux/U34/Y (INVX1_LVT)                              0.05       2.13
f
  dp/pcmux/U1/Y (INVX1_LVT)                               0.07       2.19
r
  dp/pcmux/U37/Y (INVX0_LVT)                              0.07       2.27
f
```

```
  dp/pcmux/U6/Y (AO22X1_LVT)                              0.06       2.33
f
  dp/pcmux/y[5] (mux2_2)                                  0.00       2.33
f
  dp/IF/d[5] (flopenr)                                    0.00       2.33
f
  dp/IF/U6/Y (AO22X1_LVT)                                 0.04       2.36
f
  dp/IF/q_reg[5]/D (DFFARX1_LVT)                          0.00       2.36
f
  data arrival time                                                  2.36

  clock clk (rise edge)                                   3.00       3.00
  clock network delay (ideal)                             0.00       3.00
  clock uncertainty                                      -0.10       2.90
  dp/IF/q_reg[5]/CLK (DFFARX1_LVT)                        0.00       2.90
r
  library setup time                                     -0.03       2.87
  data required time                                                 2.87
  --------------------------------------------------------------------------
---
  data required time                                                 2.87
  data arrival time                                                 -2.36
  --------------------------------------------------------------------------
---
  slack (MET)                                                        0.51


1
Filename : rt_4.rpt

Information: Updating design information... (UID-85)
Warning: Design 'riscv_pip_27' contains 1 high-fanout nets. A fanout
number of 1000 will be used for delay calculations involving these nets.
(TIM-134)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:38:41 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: ss0p95v125c   Library: saed32lvt_ss0p95v125c
Wire Load Model Mode: enclosed

  Startpoint: c/c_pipreg2/ResultSrcW_reg[1]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: dp/rf/rf_reg[10][7]
```

```
          (falling edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 saed32lvt_ss0p95v125c
  mux3_1             ForQA                 saed32lvt_ss0p95v125c
  datapath           35000                 saed32lvt_ss0p95v125c
  regfile            16000                 saed32lvt_ss0p95v125c

  Point                                                   Incr       Path
  ------------------------------------------------------------------------
---
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  c/c_pipreg2/ResultSrcW_reg[1]/CLK (DFFARX1_LVT)         0.00 #     0.00
r
  c/c_pipreg2/ResultSrcW_reg[1]/Q (DFFARX1_LVT)           0.14       0.14
r
  c/c_pipreg2/ResultSrcW[1] (c_IM_IW)                     0.00       0.14
r
  c/ResultSrcW[1] (controller)                            0.00       0.14
r
  dp/ResultSrcW[1] (datapath)                             0.00       0.14
r
  dp/resultmux/s[1] (mux3_1)                              0.00       0.14
r
  dp/resultmux/U1/Y (INVX1_LVT)                           0.03       0.17
f
  dp/resultmux/U41/Y (INVX2_LVT)                          0.05       0.23
r
  dp/resultmux/U34/Y (NOR2X0_LVT)                         0.09       0.32
f
  dp/resultmux/U38/Y (NBUFFX2_LVT)                        0.08       0.40
f
  dp/resultmux/U4/Y (AO222X1_LVT)                         0.10       0.49
f
  dp/resultmux/y[7] (mux3_1)                              0.00       0.49
f
  dp/rf/wd3[7] (regfile)                                  0.00       0.49
f
  dp/rf/U330/Y (NBUFFX2_LVT)                              0.06       0.55
f
  dp/rf/U2884/Y (AO22X1_LVT)                              0.06       0.61
f
  dp/rf/rf_reg[10][7]/D (DFFNX1_LVT)                      0.00       0.61
f
  data arrival time                                                  0.61

  clock clk (fall edge)                                   2.00       2.00
  clock network delay (ideal)                             0.00       2.00
  clock uncertainty                                      -0.10       1.90
```

```
  dp/rf/rf_reg[10][7]/CLK (DFFNX1_LVT)                    0.00       1.90
f
  library setup time                                     -0.04       1.86
  data required time                                                 1.86
  ------------------------------------------------------------------------
---
  data required time                                                 1.86
  data arrival time                                                 -0.61
  ------------------------------------------------------------------------
---
  slack (MET)                                                        1.25


1
Filename : rt_5.5.rpt

Information: Updating design information... (UID-85)
Warning: Design 'riscv_pip_27' contains 1 high-fanout nets. A fanout
number of 1000 will be used for delay calculations involving these nets.
(TIM-134)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:40:27 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: ss0p95v125c   Library: saed32lvt_ss0p95v125c
Wire Load Model Mode: enclosed

  Startpoint: c/c_pipreg2/ResultSrcW_reg[1]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: dp/rf/rf_reg[14][28]
            (falling edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 saed32lvt_ss0p95v125c
  mux3_1             ForQA                 saed32lvt_ss0p95v125c
  datapath           35000                 saed32lvt_ss0p95v125c
  regfile            16000                 saed32lvt_ss0p95v125c

  Point                                                   Incr       Path
  ------------------------------------------------------------------------
---
  clock clk (rise edge)                                   0.00       0.00
```

```
  clock network delay (ideal)                              0.00       0.00
  c/c_pipreg2/ResultSrcW_reg[1]/CLK (DFFARX1_LVT)          0.00 #     0.00
r
  c/c_pipreg2/ResultSrcW_reg[1]/Q (DFFARX1_LVT)            0.14       0.14
r
  c/c_pipreg2/ResultSrcW[1] (c_IM_IW)                      0.00       0.14
r
  c/ResultSrcW[1] (controller)                             0.00       0.14
r
  dp/ResultSrcW[1] (datapath)                              0.00       0.14
r
  dp/resultmux/s[1] (mux3_1)                               0.00       0.14
r
  dp/resultmux/U1/Y (INVX1_LVT)                            0.03       0.17
f
  dp/resultmux/U41/Y (INVX2_LVT)                           0.05       0.23
r
  dp/resultmux/U34/Y (NOR2X0_LVT)                          0.09       0.32
f
  dp/resultmux/U37/Y (NBUFFX2_LVT)                         0.08       0.40
f
  dp/resultmux/U13/Y (AO222X1_LVT)                         0.10       0.49
f
  dp/resultmux/y[28] (mux3_1)                              0.00       0.49
f
  dp/rf/wd3[28] (regfile)                                  0.00       0.49
f
  dp/rf/U319/Y (NBUFFX2_LVT)                               0.06       0.55
f
  dp/rf/U2731/Y (AO22X1_LVT)                               0.06       0.61
f
  dp/rf/rf_reg[14][28]/D (DFFNX1_LVT)                      0.00       0.61
f
  data arrival time                                                   0.61

  clock clk (fall edge)                                    2.75       2.75
  clock network delay (ideal)                              0.00       2.75
  clock uncertainty                                       -0.10       2.65
  dp/rf/rf_reg[14][28]/CLK (DFFNX1_LVT)                    0.00       2.65
f
  library setup time                                      -0.04       2.61
  data required time                                                  2.61
  ------------------------------------------------------------------------
---
  data required time                                                  2.61
  data arrival time                                                  -0.61
  ------------------------------------------------------------------------
---
  slack (MET)                                                         2.00


1
Filename : rt_5.rpt
```

```
Information: Updating design information... (UID-85)
Warning: Design 'riscv_pip_27' contains 1 high-fanout nets. A fanout
number of 1000 will be used for delay calculations involving these nets.
(TIM-134)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:39:35 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: ss0p95v125c   Library: saed32lvt_ss0p95v125c
Wire Load Model Mode: enclosed

  Startpoint: c/c_pipreg2/ResultSrcW_reg[1]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: dp/rf/rf_reg[31][1]
            (falling edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 saed32lvt_ss0p95v125c
  mux3_1             ForQA                 saed32lvt_ss0p95v125c
  datapath           35000                 saed32lvt_ss0p95v125c
  regfile            16000                 saed32lvt_ss0p95v125c

  Point                                                   Incr       Path
  ------------------------------------------------------------------------
---
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  c/c_pipreg2/ResultSrcW_reg[1]/CLK (DFFARX1_LVT)         0.00 #     0.00
r
  c/c_pipreg2/ResultSrcW_reg[1]/Q (DFFARX1_LVT)           0.14       0.14
r
  c/c_pipreg2/ResultSrcW[1] (c_IM_IW)                     0.00       0.14
r
  c/ResultSrcW[1] (controller)                            0.00       0.14
r
  dp/ResultSrcW[1] (datapath)                             0.00       0.14
r
  dp/resultmux/s[1] (mux3_1)                              0.00       0.14
r
  dp/resultmux/U1/Y (INVX1_LVT)                           0.03       0.17
f
```

```
  dp/resultmux/U41/Y (INVX2_LVT)                          0.05       0.23
r
  dp/resultmux/U34/Y (NOR2X0_LVT)                         0.09       0.32
f
  dp/resultmux/U39/Y (NBUFFX2_LVT)                        0.08       0.40
f
  dp/resultmux/U22/Y (AO222X1_LVT)                        0.09       0.49
f
  dp/resultmux/y[1] (mux3_1)                              0.00       0.49
f
  dp/rf/wd3[1] (regfile)                                  0.00       0.49
f
  dp/rf/U392/Y (NBUFFX2_LVT)                              0.06       0.54
f
  dp/rf/U3226/Y (AO22X1_LVT)                              0.04       0.59
f
  dp/rf/rf_reg[31][1]/D (DFFNX1_LVT)                      0.00       0.59
f
  data arrival time                                                  0.59

  clock clk (fall edge)                                   2.50       2.50
  clock network delay (ideal)                             0.00       2.50
  clock uncertainty                                      -0.10       2.40
  dp/rf/rf_reg[31][1]/CLK (DFFNX1_LVT)                    0.00       2.40
f
  library setup time                                     -0.04       2.36
  data required time                                                 2.36
  ---------------------------------------------------------------------------
---
  data required time                                                 2.36
  data arrival time                                                 -0.59
  ---------------------------------------------------------------------------
---
  slack (MET)                                                        1.77


1
Filename : rt_min_0.5.rpt


****************************************
Report : timing
        -path full
        -delay min
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:32:23 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: ss0p95v125c   Library: saed32lvt_ss0p95v125c
Wire Load Model Mode: enclosed
```

```
  Startpoint: dp/pipreg2/RdM_reg[0]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: dp/pipreg3/RdW_reg[0]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 saed32lvt_ss0p95v125c
  IEx_IMem           8000                  saed32lvt_ss0p95v125c

  Point                                                    Incr       Path
  -----------------------------------------------------------------------
---
  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  dp/pipreg2/RdM_reg[0]/CLK (DFFARX1_LVT)                  0.00 #     0.00
r
  dp/pipreg2/RdM_reg[0]/QN (DFFARX1_LVT)                   0.07       0.07
f
  dp/pipreg2/U6/Y (INVX2_LVT)                              0.02       0.09
r
  dp/pipreg2/RdM[0] (IEx_IMem)                             0.00       0.09
r
  dp/pipreg3/RdM[0] (IMem_IW)                              0.00       0.09
r
  dp/pipreg3/RdW_reg[0]/D (DFFARX1_LVT)                    0.00       0.09
r
  data arrival time                                                   0.09

  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  dp/pipreg3/RdW_reg[0]/CLK (DFFARX1_LVT)                  0.00       0.00
r
  library hold time                                       -0.02      -0.02
  data required time                                                 -0.02
  -----------------------------------------------------------------------
---
  data required time                                                 -0.02
  data arrival time                                                  -0.09
  -----------------------------------------------------------------------
---
  slack (MET)                                                         0.11


1
Filename : rt_min_1.5.rpt


****************************************
Report : timing
        -path full
```

```
        -delay min
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 03:10:14 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: ss0p95v125c   Library: saed32lvt_ss0p95v125c
Wire Load Model Mode: enclosed

  Startpoint: dp/pipreg2/RdM_reg[3]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: dp/pipreg3/RdW_reg[3]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 saed32lvt_ss0p95v125c
  IEx_IMem           8000                  saed32lvt_ss0p95v125c

  Point                                                   Incr       Path
  ------------------------------------------------------------------------
---
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  dp/pipreg2/RdM_reg[3]/CLK (DFFARX1_LVT)                 0.00 #     0.00
r
  dp/pipreg2/RdM_reg[3]/QN (DFFARX1_LVT)                  0.07       0.07
f
  dp/pipreg2/U4/Y (INVX1_LVT)                             0.02       0.09
r
  dp/pipreg2/RdM[3] (IEx_IMem)                            0.00       0.09
r
  dp/pipreg3/RdM[3] (IMem_IW)                             0.00       0.09
r
  dp/pipreg3/RdW_reg[3]/D (DFFARX1_LVT)                   0.00       0.09
r
  data arrival time                                                  0.09

  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  dp/pipreg3/RdW_reg[3]/CLK (DFFARX1_LVT)                 0.00       0.00
r
  library hold time                                      -0.02      -0.02
  data required time                                                -0.02
  ------------------------------------------------------------------------
---
  data required time                                                -0.02
  data arrival time                                                 -0.09
```

```
  ------------------------------------------------------------------------
---
  slack (MET)                                                       0.11


1
Filename : rt_min_1.rpt


****************************************
Report : timing
        -path full
        -delay min
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:35:04 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: ss0p95v125c   Library: saed32lvt_ss0p95v125c
Wire Load Model Mode: enclosed

  Startpoint: dp/pipreg2/RdM_reg[4]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: dp/pipreg3/RdW_reg[4]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 saed32lvt_ss0p95v125c
  IEx_IMem           8000                  saed32lvt_ss0p95v125c

  Point                                                    Incr       Path
  ------------------------------------------------------------------------
---
  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  dp/pipreg2/RdM_reg[4]/CLK (DFFARX1_LVT)                  0.00 #     0.00
r
  dp/pipreg2/RdM_reg[4]/QN (DFFARX1_LVT)                   0.07       0.07
f
  dp/pipreg2/U4/Y (INVX2_LVT)                              0.02       0.09
r
  dp/pipreg2/RdM[4] (IEx_IMem)                             0.00       0.09
r
  dp/pipreg3/RdM[4] (IMem_IW)                              0.00       0.09
r
  dp/pipreg3/RdW_reg[4]/D (DFFARX1_LVT)                    0.00       0.09
r
  data arrival time                                                   0.09
```

```
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  dp/pipreg3/RdW_reg[4]/CLK (DFFARX1_LVT)                 0.00       0.00
r
  library hold time                                      -0.02      -0.02
  data required time                                                -0.02
  ------------------------------------------------------------------------
---
  data required time                                                -0.02
  data arrival time                                                 -0.09
  ------------------------------------------------------------------------
---
  slack (MET)                                                        0.11


1
Filename : rt_min_2.rpt


****************************************
Report : timing
        -path full
        -delay min
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:36:56 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: ss0p95v125c   Library: saed32lvt_ss0p95v125c
Wire Load Model Mode: enclosed

  Startpoint: c/c_pipreg0/MemWriteE_reg
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: c/c_pipreg1/MemWriteM_reg
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 saed32lvt_ss0p95v125c
  controller         8000                  saed32lvt_ss0p95v125c

  Point                                                   Incr       Path
  ------------------------------------------------------------------------
---
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  c/c_pipreg0/MemWriteE_reg/CLK (DFFARX1_LVT)             0.00 #     0.00
r
```

```
  c/c_pipreg0/MemWriteE_reg/Q (DFFARX1_LVT)               0.11       0.11
f
  c/c_pipreg0/MemWriteE (c_ID_IEx)                        0.00       0.11
f
  c/c_pipreg1/MemWriteE (c_IEx_IM)                        0.00       0.11
f
  c/c_pipreg1/MemWriteM_reg/D (DFFARX1_LVT)               0.00       0.11
f
  data arrival time                                                  0.11

  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  c/c_pipreg1/MemWriteM_reg/CLK (DFFARX1_LVT)             0.00       0.00
r
  library hold time                                      -0.01      -0.01
  data required time                                                -0.01
  ------------------------------------------------------------------------
---
  data required time                                                -0.01
  data arrival time                                                 -0.11
  ------------------------------------------------------------------------
---
  slack (MET)                                                        0.12


1
Filename : rt_min_3.rpt


****************************************
Report : timing
        -path full
        -delay min
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:37:48 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: ss0p95v125c   Library: saed32lvt_ss0p95v125c
Wire Load Model Mode: enclosed

  Startpoint: c/c_pipreg0/MemWriteE_reg
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: c/c_pipreg1/MemWriteM_reg
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 saed32lvt_ss0p95v125c
```

```
  controller         8000                  saed32lvt_ss0p95v125c

  Point                                                    Incr       Path
  ---------------------------------------------------------------------------
---
  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  c/c_pipreg0/MemWriteE_reg/CLK (DFFARX1_LVT)              0.00 #     0.00
r
  c/c_pipreg0/MemWriteE_reg/Q (DFFARX1_LVT)                0.11       0.11
f
  c/c_pipreg0/MemWriteE (c_ID_IEx)                         0.00       0.11
f
  c/c_pipreg1/MemWriteE (c_IEx_IM)                         0.00       0.11
f
  c/c_pipreg1/MemWriteM_reg/D (DFFARX1_LVT)                0.00       0.11
f
  data arrival time                                                   0.11

  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  c/c_pipreg1/MemWriteM_reg/CLK (DFFARX1_LVT)              0.00       0.00
r
  library hold time                                       -0.01      -0.01
  data required time                                                 -0.01
  ---------------------------------------------------------------------------
---
  data required time                                                 -0.01
  data arrival time                                                  -0.11
  ---------------------------------------------------------------------------
---
  slack (MET)                                                         0.12


1
Filename : rt_min_4.rpt


****************************************
Report : timing
        -path full
        -delay min
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:38:41 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: ss0p95v125c   Library: saed32lvt_ss0p95v125c
Wire Load Model Mode: enclosed

  Startpoint: c/c_pipreg0/MemWriteE_reg
```

```
            (rising edge-triggered flip-flop clocked by clk)
  Endpoint: c/c_pipreg1/MemWriteM_reg
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 saed32lvt_ss0p95v125c
  controller         8000                  saed32lvt_ss0p95v125c

  Point                                                    Incr       Path
  -----------------------------------------------------------------------
---
  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  c/c_pipreg0/MemWriteE_reg/CLK (DFFARX1_LVT)              0.00 #     0.00
r
  c/c_pipreg0/MemWriteE_reg/Q (DFFARX1_LVT)                0.11       0.11
f
  c/c_pipreg0/MemWriteE (c_ID_IEx)                         0.00       0.11
f
  c/c_pipreg1/MemWriteE (c_IEx_IM)                         0.00       0.11
f
  c/c_pipreg1/MemWriteM_reg/D (DFFARX1_LVT)                0.00       0.11
f
  data arrival time                                                   0.11

  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  c/c_pipreg1/MemWriteM_reg/CLK (DFFARX1_LVT)              0.00       0.00
r
  library hold time                                       -0.01      -0.01
  data required time                                                 -0.01
  -----------------------------------------------------------------------
---
  data required time                                                 -0.01
  data arrival time                                                  -0.11
  -----------------------------------------------------------------------
---
  slack (MET)                                                         0.12


1
Filename : rt_min_5.5.rpt


****************************************
Report : timing
        -path full
        -delay min
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
```

```
Date   : Fri Jul 28 22:40:27 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: ss0p95v125c   Library: saed32lvt_ss0p95v125c
Wire Load Model Mode: enclosed

  Startpoint: c/c_pipreg0/MemWriteE_reg
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: c/c_pipreg1/MemWriteM_reg
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 saed32lvt_ss0p95v125c
  controller         8000                  saed32lvt_ss0p95v125c

  Point                                                    Incr       Path
  -----------------------------------------------------------------------------
---
  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  c/c_pipreg0/MemWriteE_reg/CLK (DFFARX1_LVT)              0.00 #     0.00
r
  c/c_pipreg0/MemWriteE_reg/Q (DFFARX1_LVT)                0.11       0.11
f
  c/c_pipreg0/MemWriteE (c_ID_IEx)                         0.00       0.11
f
  c/c_pipreg1/MemWriteE (c_IEx_IM)                         0.00       0.11
f
  c/c_pipreg1/MemWriteM_reg/D (DFFARX1_LVT)                0.00       0.11
f
  data arrival time                                                   0.11

  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  c/c_pipreg1/MemWriteM_reg/CLK (DFFARX1_LVT)              0.00       0.00
r
  library hold time                                       -0.01      -0.01
  data required time                                                 -0.01
  -----------------------------------------------------------------------------
---
  data required time                                                 -0.01
  data arrival time                                                  -0.11
  -----------------------------------------------------------------------------
---
  slack (MET)                                                         0.12


1
Filename : rt_min_5.rpt
```

```
****************************************
Report : timing
        -path full
        -delay min
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:39:35 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: ss0p95v125c   Library: saed32lvt_ss0p95v125c
Wire Load Model Mode: enclosed

  Startpoint: c/c_pipreg0/MemWriteE_reg
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: c/c_pipreg1/MemWriteM_reg
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 saed32lvt_ss0p95v125c
  controller         8000                  saed32lvt_ss0p95v125c

  Point                                                   Incr       Path
  ------------------------------------------------------------------------
---
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  c/c_pipreg0/MemWriteE_reg/CLK (DFFARX1_LVT)             0.00 #     0.00
r
  c/c_pipreg0/MemWriteE_reg/Q (DFFARX1_LVT)               0.11       0.11
f
  c/c_pipreg0/MemWriteE (c_ID_IEx)                        0.00       0.11
f
  c/c_pipreg1/MemWriteE (c_IEx_IM)                        0.00       0.11
f
  c/c_pipreg1/MemWriteM_reg/D (DFFARX1_LVT)               0.00       0.11
f
  data arrival time                                                  0.11

  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  c/c_pipreg1/MemWriteM_reg/CLK (DFFARX1_LVT)             0.00       0.00
r
  library hold time                                      -0.01      -0.01
  data required time                                                -0.01
  ------------------------------------------------------------------------
---
```

```
  data required time                                                -0.01
  data arrival time                                                 -0.11
  ------------------------------------------------------------------------
---
  slack (MET)                                                        0.12


1
```

APPENDIX G: The Report Area of Technology 90nm with varies clock period.

```
Filename : ra_0.5.rpt


****************************************
Report : area
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:53:45 2023
****************************************

Library(s) Used:

    cb13fs120_tsmc_max (File: /home/user/Jenny/ref/db/sc_max.db)

Number of ports:                         3242
Number of nets:                         10379
Number of cells:                         7291
Number of combinational cells:           5707
Number of sequential cells:              1549
Number of macros/black boxes:               0
Number of buf/inv:                       1287
Number of references:                       4

Combinational area:              10917.750000
Buf/Inv area:                     1806.500000
Noncombinational area:            8986.000000
Macro/Black Box area:                0.000000
Net Interconnect area:            3660.179177

Total cell area:                 19903.750000
Total area:                      23563.929177
1
Filename : ra_1.5.rpt


****************************************
Report : area
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 03:09:14 2023
****************************************

Library(s) Used:

    cb13fs120_tsmc_max (File: /home/user/Jenny/ref/db/sc_max.db)

Number of ports:                         3242
Number of nets:                         10537
Number of cells:                         7448
Number of combinational cells:           5864
Number of sequential cells:              1549
Number of macros/black boxes:               0
Number of buf/inv:                       1235
Number of references:                       4
```

```
Combinational area:              11118.500000
Buf/Inv area:                     1692.500000
Noncombinational area:            8867.500000
Macro/Black Box area:                0.000000
Net Interconnect area:            3693.127798

Total cell area:                 19986.000000
Total area:                      23679.127798
1
Filename : ra_1.rpt


****************************************
Report : area
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:55:06 2023
****************************************

Library(s) Used:

    cb13fs120_tsmc_max (File: /home/user/Jenny/ref/db/sc_max.db)

Number of ports:                         3242
Number of nets:                         10790
Number of cells:                         6807
Number of combinational cells:           5255
Number of sequential cells:              1517
Number of macros/black boxes:               0
Number of buf/inv:                       1079
Number of references:                       5

Combinational area:              10072.250000
Buf/Inv area:                     1411.250000
Noncombinational area:            8801.750000
Macro/Black Box area:                0.000000
Net Interconnect area:            3489.319491

Total cell area:                 18874.000000
Total area:                      22363.319491
1
Filename : ra_2.rpt


****************************************
Report : area
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:57:16 2023
****************************************

Library(s) Used:
```

```
    cb13fs120_tsmc_max (File: /home/user/Jenny/ref/db/sc_max.db)

Number of ports:                         3242
Number of nets:                         11232
Number of cells:                         7246
Number of combinational cells:           5694
Number of sequential cells:              1517
Number of macros/black boxes:               0
Number of buf/inv:                       1159
Number of references:                       4

Combinational area:              10661.250000
Buf/Inv area:                     1670.000000
Noncombinational area:            8821.500000
Macro/Black Box area:                0.000000
Net Interconnect area:            3538.449072

Total cell area:                 19482.750000
Total area:                      23021.199072
1
Filename : ra_3.rpt


****************************************
Report : area
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 23:00:13 2023
****************************************

Library(s) Used:

    cb13fs120_tsmc_max (File: /home/user/Jenny/ref/db/sc_max.db)

Number of ports:                         3242
Number of nets:                         11338
Number of cells:                         7348
Number of combinational cells:           5796
Number of sequential cells:              1517
Number of macros/black boxes:               0
Number of buf/inv:                       1200
Number of references:                       4

Combinational area:              10816.500000
Buf/Inv area:                     1768.500000
Noncombinational area:            8912.250000
Macro/Black Box area:                0.000000
Net Interconnect area:            3548.677454

Total cell area:                 19728.750000
Total area:                      23277.427454
1
Filename : ra_4.rpt
```

```
****************************************
Report : area
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 23:02:17 2023
****************************************

Library(s) Used:

    cb13fs120_tsmc_max (File: /home/user/Jenny/ref/db/sc_max.db)

Number of ports:                         3242
Number of nets:                         11423
Number of cells:                         7440
Number of combinational cells:           5888
Number of sequential cells:              1517
Number of macros/black boxes:               0
Number of buf/inv:                       1251
Number of references:                       4

Combinational area:              11173.000000
Buf/Inv area:                     1729.750000
Noncombinational area:            8609.250000
Macro/Black Box area:                0.000000
Net Interconnect area:            3777.257996

Total cell area:                 19782.250000
Total area:                      23559.507996
1
Filename : ra_5.5.rpt


****************************************
Report : area
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 23:05:16 2023
****************************************

Library(s) Used:

    cb13fs120_tsmc_max (File: /home/user/Jenny/ref/db/sc_max.db)

Number of ports:                         3242
Number of nets:                         10833
Number of cells:                         6850
Number of combinational cells:           5298
Number of sequential cells:              1517
Number of macros/black boxes:               0
Number of buf/inv:                        979
Number of references:                       4

Combinational area:              10021.500000
```

```
Buf/Inv area:                     1048.500000
Noncombinational area:            8508.250000
Macro/Black Box area:                0.000000
Net Interconnect area:            3734.229205

Total cell area:                 18529.750000
Total area:                      22263.979205
1
Filename : ra_5.rpt


****************************************
Report : area
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 23:04:14 2023
****************************************

Library(s) Used:

    cb13fs120_tsmc_max (File: /home/user/Jenny/ref/db/sc_max.db)

Number of ports:                        3242
Number of nets:                        11090
Number of cells:                        7101
Number of combinational cells:          5549
Number of sequential cells:             1517
Number of macros/black boxes:              0
Number of buf/inv:                      1112
Number of references:                      4

Combinational area:              10441.000000
Buf/Inv area:                     1342.750000
Noncombinational area:            8517.500000
Macro/Black Box area:                0.000000
Net Interconnect area:            3743.803217

Total cell area:                 18958.500000
Total area:                      22702.303217
1
```

APPENDIX H: The Report Power of Technology 90nm with varies clock period.

```
Filename : rp_0.5.rpt

Loading db file '/home/user/Jenny/ref/db/sc_max.db'
Information: Propagating switching activity (low effort zero delay
simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
        -analysis_effort low
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:53:46 2023
****************************************


Library(s) Used:

    cb13fs120_tsmc_max (File: /home/user/Jenny/ref/db/sc_max.db)


Operating Conditions: cb13fs120_tsmc_max   Library: cb13fs120_tsmc_max
Wire Load Model Mode: enclosed

Design        Wire Load Model            Library
------------------------------------------------
riscv_pip_27           35000             cb13fs120_tsmc_max
controller             8000              cb13fs120_tsmc_max
hazardunit             ForQA             cb13fs120_tsmc_max
datapath               35000             cb13fs120_tsmc_max
maindec                ForQA             cb13fs120_tsmc_max
aludec                 ForQA             cb13fs120_tsmc_max
c_ID_IEx               ForQA             cb13fs120_tsmc_max
c_IEx_IM               ForQA             cb13fs120_tsmc_max
c_IM_IW                ForQA             cb13fs120_tsmc_max
mux2_0                 ForQA             cb13fs120_tsmc_max
flopenr                8000              cb13fs120_tsmc_max
adder_0                8000              cb13fs120_tsmc_max
IF_ID                  8000              cb13fs120_tsmc_max
regfile                16000             cb13fs120_tsmc_max
extend                 ForQA             cb13fs120_tsmc_max
ID_IEx                 8000              cb13fs120_tsmc_max
mux3_0                 ForQA             cb13fs120_tsmc_max
alu                    8000              cb13fs120_tsmc_max
IEx_IMem               8000              cb13fs120_tsmc_max
IMem_IW                8000              cb13fs120_tsmc_max
adder_1                8000              cb13fs120_tsmc_max
mux2_1                 ForQA             cb13fs120_tsmc_max
mux2_2                 ForQA             cb13fs120_tsmc_max
mux3_1                 ForQA             cb13fs120_tsmc_max
mux3_2                 ForQA             cb13fs120_tsmc_max
mux3_3                 ForQA             cb13fs120_tsmc_max
adder_1_DW01_add_1     8000              cb13fs120_tsmc_max
```

```
alu_DW_cmp_2           ForQA             cb13fs120_tsmc_max
adder_0_DW01_add_1     8000              cb13fs120_tsmc_max
alu_DW01_add_5         8000              cb13fs120_tsmc_max


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =  17.0344 mW   (57%)
  Net Switching Power  =  13.0696 mW   (43%)
                          ---------
Total Dynamic Power    =  30.1040 mW  (100%)

Cell Leakage Power     = 123.3114 uW


                 Internal         Switching           Leakage
Total
Power Group      Power            Power               Power
Power   (   %    )  Attrs
--------------------------------------------------------------------------------
-------------------------
io_pad             0.0000            0.0000            0.0000
0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000
0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000
0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000
0.0000  (   0.00%)
register           2.7900            4.3642        6.0849e+07
7.2150  (  23.87%)
sequential         0.0000            0.0000            0.0000
0.0000  (   0.00%)
combinational     14.2444            8.7054        6.2463e+07
23.0123  (  76.13%)
--------------------------------------------------------------------------------
-------------------------
Total             17.0344 mW        13.0696 mW     1.2331e+08 pW
30.2273 mW
1
Filename : rp_1.5.rpt

Loading db file '/home/user/Jenny/ref/db/sc_max.db'
Information: Propagating switching activity (low effort zero delay
simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)
```

```
****************************************
Report : power
         -analysis_effort low
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 03:09:22 2023
****************************************


Library(s) Used:

    cb13fs120_tsmc_max (File: /home/user/Jenny/ref/db/sc_max.db)


Operating Conditions: cb13fs120_tsmc_max   Library: cb13fs120_tsmc_max
Wire Load Model Mode: enclosed

Design        Wire Load Model            Library
------------------------------------------------
riscv_pip_27           35000             cb13fs120_tsmc_max
controller             8000              cb13fs120_tsmc_max
hazardunit             ForQA             cb13fs120_tsmc_max
datapath               35000             cb13fs120_tsmc_max
maindec                ForQA             cb13fs120_tsmc_max
aludec                 ForQA             cb13fs120_tsmc_max
c_ID_IEx               ForQA             cb13fs120_tsmc_max
c_IEx_IM               ForQA             cb13fs120_tsmc_max
c_IM_IW                ForQA             cb13fs120_tsmc_max
mux2_0                 ForQA             cb13fs120_tsmc_max
flopenr                8000              cb13fs120_tsmc_max
adder_0                8000              cb13fs120_tsmc_max
IF_ID                  8000              cb13fs120_tsmc_max
regfile                16000             cb13fs120_tsmc_max
extend                 ForQA             cb13fs120_tsmc_max
ID_IEx                 8000              cb13fs120_tsmc_max
mux3_0                 ForQA             cb13fs120_tsmc_max
alu                    8000              cb13fs120_tsmc_max
IEx_IMem               8000              cb13fs120_tsmc_max
IMem_IW                8000              cb13fs120_tsmc_max
adder_1                8000              cb13fs120_tsmc_max
mux2_1                 ForQA             cb13fs120_tsmc_max
mux2_2                 ForQA             cb13fs120_tsmc_max
mux3_1                 ForQA             cb13fs120_tsmc_max
mux3_2                 ForQA             cb13fs120_tsmc_max
mux3_3                 ForQA             cb13fs120_tsmc_max
adder_1_DW01_add_1     8000              cb13fs120_tsmc_max
alu_DW_cmp_2           ForQA             cb13fs120_tsmc_max
adder_0_DW01_add_1     8000              cb13fs120_tsmc_max
alu_DW01_add_5         8000              cb13fs120_tsmc_max


Global Operating Voltage = 1.08
Power-specific unit information :
```

```
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   5.8092 mW   (57%)
  Net Switching Power  =   4.3523 mW   (43%)
                         ---------
Total Dynamic Power    =  10.1615 mW  (100%)

Cell Leakage Power     = 121.8909 uW


                 Internal         Switching           Leakage
Total
Power Group      Power            Power               Power
Power   (   %    )  Attrs
--------------------------------------------------------------------------
-------------------------
io_pad             0.0000            0.0000            0.0000
0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000
0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000
0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000
0.0000  (   0.00%)
register           1.0446            1.8238        6.0680e+07
2.9290  (  28.48%)
sequential         0.0000            0.0000            0.0000
0.0000  (   0.00%)
combinational      4.7646            2.5286        6.1211e+07
7.3544  (  71.52%)
--------------------------------------------------------------------------
-------------------------
Total              5.8092 mW         4.3523 mW     1.2189e+08 pW
10.2834 mW
1
Filename : rp_1.rpt

Loading db file '/home/user/Jenny/ref/db/sc_max.db'
Information: Propagating switching activity (low effort zero delay
simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
        -analysis_effort low
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:55:08 2023
```

```
****************************************


Library(s) Used:

    cb13fs120_tsmc_max (File: /home/user/Jenny/ref/db/sc_max.db)


Operating Conditions: cb13fs120_tsmc_max   Library: cb13fs120_tsmc_max
Wire Load Model Mode: enclosed

Design         Wire Load Model            Library
------------------------------------------------
riscv_pip_27           35000              cb13fs120_tsmc_max
controller             ForQA              cb13fs120_tsmc_max
hazardunit             ForQA              cb13fs120_tsmc_max
datapath               35000              cb13fs120_tsmc_max
maindec                ForQA              cb13fs120_tsmc_max
aludec                 ForQA              cb13fs120_tsmc_max
c_ID_IEx               ForQA              cb13fs120_tsmc_max
c_IEx_IM               ForQA              cb13fs120_tsmc_max
c_IM_IW                ForQA              cb13fs120_tsmc_max
mux2_0                 ForQA              cb13fs120_tsmc_max
mux2_2                 ForQA              cb13fs120_tsmc_max
flopenr                8000               cb13fs120_tsmc_max
adder_0                8000               cb13fs120_tsmc_max
IF_ID                  8000               cb13fs120_tsmc_max
regfile                16000              cb13fs120_tsmc_max
extend                 ForQA              cb13fs120_tsmc_max
ID_IEx                 8000               cb13fs120_tsmc_max
mux3_0                 ForQA              cb13fs120_tsmc_max
mux2_1                 ForQA              cb13fs120_tsmc_max
mux3_3                 ForQA              cb13fs120_tsmc_max
mux3_2                 ForQA              cb13fs120_tsmc_max
adder_1                8000               cb13fs120_tsmc_max
alu                    8000               cb13fs120_tsmc_max
IEx_IMem               8000               cb13fs120_tsmc_max
IMem_IW                8000               cb13fs120_tsmc_max
mux3_1                 ForQA              cb13fs120_tsmc_max
adder_0_DW01_add_1     8000               cb13fs120_tsmc_max
adder_1_DW01_add_1     8000               cb13fs120_tsmc_max
alu_DW_cmp_2           ForQA              cb13fs120_tsmc_max
alu_DW01_add_5         8000               cb13fs120_tsmc_max


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW
```

```
  Cell Internal Power  =   7.2749 mW   (56%)
  Net Switching Power  =   5.6082 mW   (44%)
                         ---------
Total Dynamic Power    =  12.8831 mW  (100%)

Cell Leakage Power     = 116.8382 uW


                 Internal         Switching           Leakage
Total
Power Group      Power            Power               Power
Power   (   %    )  Attrs
--------------------------------------------------------------------------------
------------------------
io_pad             0.0000            0.0000            0.0000
0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000
0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000
0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000
0.0000  (   0.00%)
register           1.4370            2.2048        5.9482e+07
3.7013  (  28.47%)
sequential         0.0000            0.0000            0.0000
0.0000  (   0.00%)
combinational      5.8380            3.4034        5.7356e+07
9.2987  (  71.53%)
--------------------------------------------------------------------------------
------------------------
Total              7.2749 mW         5.6082 mW     1.1684e+08 pW
13.0000 mW
1
Filename : rp_2.rpt

Loading db file '/home/user/Jenny/ref/db/sc_max.db'
Information: Propagating switching activity (low effort zero delay
simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
        -analysis_effort low
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:57:18 2023
****************************************


Library(s) Used:

    cb13fs120_tsmc_max (File: /home/user/Jenny/ref/db/sc_max.db)
```

```
Operating Conditions: cb13fs120_tsmc_max   Library: cb13fs120_tsmc_max
Wire Load Model Mode: enclosed

Design        Wire Load Model            Library
------------------------------------------------
riscv_pip_27          35000              cb13fs120_tsmc_max
controller            ForQA              cb13fs120_tsmc_max
hazardunit            ForQA              cb13fs120_tsmc_max
datapath              35000              cb13fs120_tsmc_max
maindec               ForQA              cb13fs120_tsmc_max
aludec                ForQA              cb13fs120_tsmc_max
c_ID_IEx              ForQA              cb13fs120_tsmc_max
c_IEx_IM              ForQA              cb13fs120_tsmc_max
c_IM_IW               ForQA              cb13fs120_tsmc_max
mux2_0                ForQA              cb13fs120_tsmc_max
mux2_2                ForQA              cb13fs120_tsmc_max
flopenr               8000               cb13fs120_tsmc_max
adder_0               8000               cb13fs120_tsmc_max
IF_ID                 8000               cb13fs120_tsmc_max
regfile               16000              cb13fs120_tsmc_max
extend                ForQA              cb13fs120_tsmc_max
ID_IEx                8000               cb13fs120_tsmc_max
mux3_0                ForQA              cb13fs120_tsmc_max
mux2_1                ForQA              cb13fs120_tsmc_max
mux3_3                ForQA              cb13fs120_tsmc_max
mux3_2                ForQA              cb13fs120_tsmc_max
adder_1               8000               cb13fs120_tsmc_max
alu                   8000               cb13fs120_tsmc_max
IEx_IMem              8000               cb13fs120_tsmc_max
IMem_IW               8000               cb13fs120_tsmc_max
mux3_1                ForQA              cb13fs120_tsmc_max
adder_0_DW01_add_1    8000               cb13fs120_tsmc_max
adder_1_DW01_add_1    8000               cb13fs120_tsmc_max
alu_DW_cmp_2          8000               cb13fs120_tsmc_max
alu_DW01_add_5        8000               cb13fs120_tsmc_max


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   3.8082 mW   (57%)
  Net Switching Power  =   2.8193 mW   (43%)
                         ---------
Total Dynamic Power    =   6.6275 mW  (100%)

Cell Leakage Power     = 120.6279 uW
```

```
                 Internal         Switching           Leakage
Total
Power Group      Power            Power               Power
Power    (   %    )  Attrs
--------------------------------------------------------------------------------
-------------------------
io_pad             0.0000            0.0000            0.0000
0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000
0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000
0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000
0.0000  (   0.00%)
register           0.6977            1.3887        5.9725e+07
2.1460  (  31.80%)
sequential         0.0000            0.0000            0.0000
0.0000  (   0.00%)
combinational      3.1106            1.4306        6.0902e+07
4.6021  (  68.20%)
--------------------------------------------------------------------------------
-------------------------
Total              3.8082 mW         2.8193 mW     1.2063e+08 pW
6.7481 mW
1
Filename : rp_3.rpt

Loading db file '/home/user/Jenny/ref/db/sc_max.db'
Information: Propagating switching activity (low effort zero delay
simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
        -analysis_effort low
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 23:00:14 2023
****************************************


Library(s) Used:

    cb13fs120_tsmc_max (File: /home/user/Jenny/ref/db/sc_max.db)


Operating Conditions: cb13fs120_tsmc_max   Library: cb13fs120_tsmc_max
Wire Load Model Mode: enclosed

Design        Wire Load Model            Library
------------------------------------------------
riscv_pip_27           35000             cb13fs120_tsmc_max
```

```
controller              ForQA             cb13fs120_tsmc_max
hazardunit              ForQA             cb13fs120_tsmc_max
datapath                35000             cb13fs120_tsmc_max
maindec                 ForQA             cb13fs120_tsmc_max
aludec                  ForQA             cb13fs120_tsmc_max
c_ID_IEx                ForQA             cb13fs120_tsmc_max
c_IEx_IM                ForQA             cb13fs120_tsmc_max
c_IM_IW                 ForQA             cb13fs120_tsmc_max
mux2_0                  ForQA             cb13fs120_tsmc_max
mux2_2                  ForQA             cb13fs120_tsmc_max
flopenr                 8000              cb13fs120_tsmc_max
adder_0                 8000              cb13fs120_tsmc_max
IF_ID                   8000              cb13fs120_tsmc_max
regfile                 16000             cb13fs120_tsmc_max
extend                  ForQA             cb13fs120_tsmc_max
ID_IEx                  8000              cb13fs120_tsmc_max
mux3_0                  ForQA             cb13fs120_tsmc_max
mux2_1                  ForQA             cb13fs120_tsmc_max
mux3_3                  ForQA             cb13fs120_tsmc_max
mux3_2                  ForQA             cb13fs120_tsmc_max
adder_1                 8000              cb13fs120_tsmc_max
alu                     8000              cb13fs120_tsmc_max
IEx_IMem                8000              cb13fs120_tsmc_max
IMem_IW                 8000              cb13fs120_tsmc_max
mux3_1                  ForQA             cb13fs120_tsmc_max
adder_0_DW01_add_1      8000              cb13fs120_tsmc_max
adder_1_DW01_add_1      8000              cb13fs120_tsmc_max
alu_DW_cmp_2            ForQA             cb13fs120_tsmc_max
alu_DW01_add_5          8000              cb13fs120_tsmc_max


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   2.7706 mW   (59%)
  Net Switching Power  =   1.9521 mW   (41%)
                         ---------
Total Dynamic Power    =   4.7227 mW  (100%)

Cell Leakage Power     = 123.1326 uW


                 Internal         Switching           Leakage
Total
Power Group      Power            Power               Power
Power   (   %    )  Attrs
--------------------------------------------------------------------------
------------------------
```

```
io_pad              0.0000            0.0000            0.0000
0.0000  (   0.00%)
memory              0.0000            0.0000            0.0000
0.0000  (   0.00%)
black_box           0.0000            0.0000            0.0000
0.0000  (   0.00%)
clock_network       0.0000            0.0000            0.0000
0.0000  (   0.00%)
register            0.5633            0.9576        6.0759e+07
1.5816  (  32.64%)
sequential          0.0000            0.0000            0.0000
0.0000  (   0.00%)
combinational       2.2073            0.9945        6.2373e+07
3.2642  (  67.36%)
--------------------------------------------------------------------------------
-------------------------
Total               2.7706 mW         1.9521 mW     1.2313e+08 pW
4.8458 mW
1
Filename : rp_4.rpt

Loading db file '/home/user/Jenny/ref/db/sc_max.db'
Information: Propagating switching activity (low effort zero delay
simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
        -analysis_effort low
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 23:02:19 2023
****************************************


Library(s) Used:

    cb13fs120_tsmc_max (File: /home/user/Jenny/ref/db/sc_max.db)


Operating Conditions: cb13fs120_tsmc_max   Library: cb13fs120_tsmc_max
Wire Load Model Mode: enclosed

Design        Wire Load Model            Library
------------------------------------------------
riscv_pip_27           35000             cb13fs120_tsmc_max
controller             ForQA             cb13fs120_tsmc_max
hazardunit             ForQA             cb13fs120_tsmc_max
datapath               35000             cb13fs120_tsmc_max
maindec                ForQA             cb13fs120_tsmc_max
aludec                 ForQA             cb13fs120_tsmc_max
c_ID_IEx               ForQA             cb13fs120_tsmc_max
c_IEx_IM               ForQA             cb13fs120_tsmc_max
```

```
c_IM_IW                 ForQA             cb13fs120_tsmc_max
mux2_0                  ForQA             cb13fs120_tsmc_max
mux2_2                  ForQA             cb13fs120_tsmc_max
flopenr                 8000              cb13fs120_tsmc_max
adder_0                 8000              cb13fs120_tsmc_max
IF_ID                   8000              cb13fs120_tsmc_max
regfile                 16000             cb13fs120_tsmc_max
extend                  ForQA             cb13fs120_tsmc_max
ID_IEx                  8000              cb13fs120_tsmc_max
mux3_0                  ForQA             cb13fs120_tsmc_max
mux2_1                  ForQA             cb13fs120_tsmc_max
mux3_3                  ForQA             cb13fs120_tsmc_max
mux3_2                  ForQA             cb13fs120_tsmc_max
adder_1                 8000              cb13fs120_tsmc_max
alu                     8000              cb13fs120_tsmc_max
IEx_IMem                8000              cb13fs120_tsmc_max
IMem_IW                 8000              cb13fs120_tsmc_max
mux3_1                  ForQA             cb13fs120_tsmc_max
adder_0_DW01_add_1      8000              cb13fs120_tsmc_max
adder_1_DW01_add_1      8000              cb13fs120_tsmc_max
alu_DW_cmp_2            ForQA             cb13fs120_tsmc_max
alu_DW01_add_5          8000              cb13fs120_tsmc_max


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   2.0675 mW   (58%)
  Net Switching Power  =   1.5092 mW   (42%)
                         ---------
Total Dynamic Power    =   3.5767 mW  (100%)

Cell Leakage Power     = 120.3582 uW


                 Internal         Switching           Leakage
Total
Power Group      Power            Power               Power
Power   (   %    )  Attrs
--------------------------------------------------------------------------------
-------------------------
io_pad             0.0000            0.0000            0.0000
0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000
0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000
0.0000  (   0.00%)
```

```
clock_network      0.0000            0.0000            0.0000
0.0000  (   0.00%)
register           0.3962            0.7439        5.9059e+07
1.1991  (  32.43%)
sequential         0.0000            0.0000            0.0000
0.0000  (   0.00%)
combinational      1.6713            0.7653        6.1299e+07
2.4979  (  67.57%)
--------------------------------------------------------------------------------
-------------------------
Total              2.0675 mW         1.5092 mW     1.2036e+08 pW
3.6970 mW
1
Filename : rp_5.5.rpt

Information: Propagating switching activity (low effort zero delay
simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
        -analysis_effort low
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 23:05:16 2023
****************************************


Library(s) Used:

    cb13fs120_tsmc_max (File: /home/user/Jenny/ref/db/sc_max.db)


Operating Conditions: cb13fs120_tsmc_max   Library: cb13fs120_tsmc_max
Wire Load Model Mode: enclosed

Design         Wire Load Model            Library
------------------------------------------------
riscv_pip_27           35000              cb13fs120_tsmc_max
controller             ForQA              cb13fs120_tsmc_max
hazardunit             ForQA              cb13fs120_tsmc_max
datapath               35000              cb13fs120_tsmc_max
maindec                ForQA              cb13fs120_tsmc_max
aludec                 ForQA              cb13fs120_tsmc_max
c_ID_IEx               ForQA              cb13fs120_tsmc_max
c_IEx_IM               ForQA              cb13fs120_tsmc_max
c_IM_IW                ForQA              cb13fs120_tsmc_max
mux2_0                 ForQA              cb13fs120_tsmc_max
mux2_2                 ForQA              cb13fs120_tsmc_max
flopenr                8000               cb13fs120_tsmc_max
adder_0                8000               cb13fs120_tsmc_max
IF_ID                  8000               cb13fs120_tsmc_max
regfile                16000              cb13fs120_tsmc_max
```

```
extend                  ForQA             cb13fs120_tsmc_max
ID_IEx                  8000              cb13fs120_tsmc_max
mux3_0                  ForQA             cb13fs120_tsmc_max
mux2_1                  ForQA             cb13fs120_tsmc_max
mux3_3                  ForQA             cb13fs120_tsmc_max
mux3_2                  ForQA             cb13fs120_tsmc_max
adder_1                 8000              cb13fs120_tsmc_max
alu                     8000              cb13fs120_tsmc_max
IEx_IMem                8000              cb13fs120_tsmc_max
IMem_IW                 8000              cb13fs120_tsmc_max
mux3_1                  ForQA             cb13fs120_tsmc_max
adder_0_DW01_add_1      8000              cb13fs120_tsmc_max
adder_1_DW01_add_1      8000              cb13fs120_tsmc_max
alu_DW01_add_5          8000              cb13fs120_tsmc_max
alu_DW_cmp_3            ForQA             cb13fs120_tsmc_max


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   1.0685 mW   (51%)
  Net Switching Power  =   1.0157 mW   (49%)
                         ---------
Total Dynamic Power    =   2.0842 mW  (100%)

Cell Leakage Power     = 107.4436 uW


                 Internal         Switching           Leakage
Total
Power Group      Power            Power               Power
Power   (   %    )  Attrs
--------------------------------------------------------------------------------
-------------------------
io_pad             0.0000            0.0000            0.0000
0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000
0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000
0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000
0.0000  (   0.00%)
register           0.2413            0.5235        5.7923e+07
0.8228  (  37.54%)
sequential         0.0000            0.0000            0.0000
0.0000  (   0.00%)
combinational      0.8272            0.4922        4.9521e+07
1.3689  (  62.46%)
```

```
------------------------------------------------------------------------
-------------------------
Total              1.0685 mW         1.0157 mW     1.0744e+08 pW
2.1917 mW
1
Filename : rp_5.rpt

Loading db file '/home/user/Jenny/ref/db/sc_max.db'
Information: Propagating switching activity (low effort zero delay
simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
        -analysis_effort low
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 23:04:15 2023
****************************************


Library(s) Used:

    cb13fs120_tsmc_max (File: /home/user/Jenny/ref/db/sc_max.db)


Operating Conditions: cb13fs120_tsmc_max   Library: cb13fs120_tsmc_max
Wire Load Model Mode: enclosed

Design        Wire Load Model            Library
------------------------------------------------
riscv_pip_27           35000             cb13fs120_tsmc_max
controller             ForQA             cb13fs120_tsmc_max
hazardunit             ForQA             cb13fs120_tsmc_max
datapath               35000             cb13fs120_tsmc_max
maindec                ForQA             cb13fs120_tsmc_max
aludec                 ForQA             cb13fs120_tsmc_max
c_ID_IEx               ForQA             cb13fs120_tsmc_max
c_IEx_IM               ForQA             cb13fs120_tsmc_max
c_IM_IW                ForQA             cb13fs120_tsmc_max
mux2_0                 ForQA             cb13fs120_tsmc_max
mux2_2                 ForQA             cb13fs120_tsmc_max
flopenr                8000              cb13fs120_tsmc_max
adder_0                8000              cb13fs120_tsmc_max
IF_ID                  8000              cb13fs120_tsmc_max
regfile                16000             cb13fs120_tsmc_max
extend                 ForQA             cb13fs120_tsmc_max
ID_IEx                 8000              cb13fs120_tsmc_max
mux3_0                 ForQA             cb13fs120_tsmc_max
mux2_1                 ForQA             cb13fs120_tsmc_max
mux3_3                 ForQA             cb13fs120_tsmc_max
mux3_2                 ForQA             cb13fs120_tsmc_max
adder_1                8000              cb13fs120_tsmc_max
```

```
alu                     8000              cb13fs120_tsmc_max
IEx_IMem                8000              cb13fs120_tsmc_max
IMem_IW                 8000              cb13fs120_tsmc_max
mux3_1                  ForQA             cb13fs120_tsmc_max
adder_0_DW01_add_1      8000              cb13fs120_tsmc_max
adder_1_DW01_add_1      8000              cb13fs120_tsmc_max
alu_DW01_add_5          8000              cb13fs120_tsmc_max
alu_DW_cmp_3            8000              cb13fs120_tsmc_max


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   1.2848 mW   (53%)
  Net Switching Power  =   1.1381 mW   (47%)
                         ---------
Total Dynamic Power    =   2.4229 mW  (100%)

Cell Leakage Power     = 111.0986 uW


                 Internal         Switching           Leakage
Total
Power Group      Power            Power               Power
Power   (   %    )  Attrs
---------------------------------------------------------------------------
-------------------------
io_pad             0.0000            0.0000            0.0000
0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000
0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000
0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000
0.0000  (   0.00%)
register           0.2708            0.5758        5.8029e+07
0.9047  (  35.70%)
sequential         0.0000            0.0000            0.0000
0.0000  (   0.00%)
combinational      1.0140            0.5622        5.3070e+07
1.6293  (  64.30%)
---------------------------------------------------------------------------
-------------------------
Total              1.2848 mW         1.1381 mW     1.1110e+08 pW
2.5340 mW
1
```

APPENDIX I: The Report Timing of Technology 90nm with varies clock period.

```
Filename : rt_0.5.rpt

Information: Updating design information... (UID-85)
Warning: Design 'riscv_pip_27' contains 1 high-fanout nets. A fanout
number of 1000 will be used for delay calculations involving these nets.
(TIM-134)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:53:45 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: cb13fs120_tsmc_max   Library: cb13fs120_tsmc_max
Wire Load Model Mode: enclosed

  Startpoint: dp/pipreg1/Rs1E_reg[1]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: dp/IF/q_reg[0]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 cb13fs120_tsmc_max
  hazardunit         ForQA                 cb13fs120_tsmc_max
  mux3_0             ForQA                 cb13fs120_tsmc_max
  datapath           35000                 cb13fs120_tsmc_max
  alu                8000                  cb13fs120_tsmc_max
  controller         8000                  cb13fs120_tsmc_max
  mux2_2             ForQA                 cb13fs120_tsmc_max

  Point                                    Incr       Path
  ----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  dp/pipreg1/Rs1E_reg[1]/CP (dfcrq2)       0.00 #     0.00 r
  dp/pipreg1/Rs1E_reg[1]/Q (dfcrq2)        0.35       0.35 f
  dp/pipreg1/Rs1E[1] (ID_IEx)              0.00       0.35 f
  dp/Rs1E[1] (datapath)                    0.00       0.35 f
  h/Rs1E[1] (hazardunit)                   0.00       0.35 f
  h/U78/ZN (nr03d0)                        0.11       0.46 r
  h/U15/Z (an03d1)                         0.18       0.64 r
  h/U79/ZN (nr02d0)                        0.08       0.71 f
  h/U16/Z (an04d2)                         0.16       0.87 f
  h/U22/ZN (nd02d2)                        0.05       0.92 r
  h/U21/ZN (nd02d2)                        0.05       0.97 f
```

```
h/U30/ZN (nr03d0)                          0.12       1.10 r
h/ForwardAE[0] (hazardunit)                0.00       1.10 r
dp/ForwardAE[0] (datapath)                 0.00       1.10 r
dp/forwardMuxA/s[0] (mux3_0)               0.00       1.10 r
dp/forwardMuxA/U15/ZN (inv0d1)             0.12       1.22 f
dp/forwardMuxA/U14/ZN (nd02d2)             0.10       1.32 r
dp/forwardMuxA/U10/ZN (invbd2)             0.12       1.43 f
dp/forwardMuxA/U55/Z (aor222d1)            0.35       1.78 f
dp/forwardMuxA/y[31] (mux3_0)              0.00       1.78 f
dp/srcamux/d0[31] (mux2_1)                 0.00       1.78 f
dp/srcamux/U2/Z (mx02d2)                   0.21       1.99 f
dp/srcamux/y[31] (mux2_1)                  0.00       1.99 f
dp/alu/SrcA[31] (alu)                      0.00       1.99 f
dp/alu/U249/Z (bufbd7)                     0.13       2.12 f
dp/alu/U14/ZN (inv0d4)                     0.05       2.17 r
dp/alu/U484/ZN (oai2222d2)                 0.41       2.58 f
dp/alu/U777/ZN (oai2222d1)                 0.31       2.89 r
dp/alu/U266/Z (aor222d1)                   0.19       3.08 r
dp/alu/U219/ZN (nr03d0)                    0.08       3.16 f
dp/alu/U945/Z (aor221d1)                   0.25       3.41 f
dp/alu/U117/Z (aor311d2)                   0.26       3.67 f
dp/alu/U50/ZN (invbd2)                     0.03       3.70 r
dp/alu/U950/ZN (nd04d0)                    0.14       3.84 f
dp/alu/U951/ZN (nr03d0)                    0.14       3.98 r
dp/alu/U153/Z (an03d2)                     0.18       4.15 r
dp/alu/Zero (alu)                          0.00       4.15 r
dp/ZeroE (datapath)                        0.00       4.15 r
c/ZeroE (controller)                       0.00       4.15 r
c/U9/ZN (nr02d0)                           0.08       4.23 f
c/U17/ZN (nr02d0)                          0.09       4.32 r
c/U18/ZN (nd02d2)                          0.08       4.41 f
c/PCSrcE (controller)                      0.00       4.41 f
dp/PCSrcE (datapath)                       0.00       4.41 f
dp/U12/Z (bufbd3)                          0.13       4.54 f
dp/pcmux/s (mux2_2)                        0.00       4.54 f
dp/pcmux/U2/Z (buffd7)                     0.14       4.68 f
dp/pcmux/U34/Z (mx02d1)                    0.21       4.90 r
dp/pcmux/y[0] (mux2_2)                     0.00       4.90 r
dp/IF/d[0] (flopenr)                       0.00       4.90 r
dp/IF/q_reg[0]/D (decrq4)                  0.00       4.90 r
data arrival time                                     4.90

clock clk (rise edge)                      0.50       0.50
clock network delay (ideal)                0.00       0.50
clock uncertainty                         -0.10       0.40
dp/IF/q_reg[0]/CP (decrq4)                 0.00       0.40 r
library setup time                        -0.18       0.22
data required time                                    0.22
-----------------------------------------------------------
data required time                                    0.22
data arrival time                                    -4.90
-----------------------------------------------------------
slack (VIOLATED)                                     -4.68
```

```
1
Filename : rt_1.5.rpt

Information: Updating design information... (UID-85)
Warning: Design 'riscv_pip_27' contains 1 high-fanout nets. A fanout
number of 1000 will be used for delay calculations involving these nets.
(TIM-134)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 03:09:14 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: cb13fs120_tsmc_max   Library: cb13fs120_tsmc_max
Wire Load Model Mode: enclosed

  Startpoint: dp/pipreg1/Rs2E_reg[1]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: dp/IF/q_reg[0]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 cb13fs120_tsmc_max
  hazardunit         ForQA                 cb13fs120_tsmc_max
  mux3_3             ForQA                 cb13fs120_tsmc_max
  datapath           35000                 cb13fs120_tsmc_max
  alu                8000                  cb13fs120_tsmc_max
  controller         8000                  cb13fs120_tsmc_max
  mux2_2             ForQA                 cb13fs120_tsmc_max

  Point                                    Incr       Path
  ----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  dp/pipreg1/Rs2E_reg[1]/CP (dfcrq2)       0.00 #     0.00 r
  dp/pipreg1/Rs2E_reg[1]/Q (dfcrq2)        0.31       0.31 r
  dp/pipreg1/Rs2E[1] (ID_IEx)              0.00       0.31 r
  dp/Rs2E[1] (datapath)                    0.00       0.31 r
  h/Rs2E[1] (hazardunit)                   0.00       0.31 r
  h/U71/ZN (nr02d0)                        0.09       0.41 f
  h/U10/Z (an04d2)                         0.16       0.57 f
  h/U79/ZN (nr04d0)                        0.16       0.73 r
  h/U80/ZN (nd04d0)                        0.13       0.86 f
```

```
h/U44/Z (an12d2)                          0.22       1.08 r
h/ForwardBE[0] (hazardunit)               0.00       1.08 r
dp/ForwardBE[0] (datapath)                0.00       1.08 r
dp/forwardMuxB/s[0] (mux3_3)              0.00       1.08 r
dp/forwardMuxB/U13/ZN (invbd7)            0.06       1.13 f
dp/forwardMuxB/U70/ZN (nd02d2)            0.07       1.21 r
dp/forwardMuxB/U19/ZN (invbd7)            0.06       1.27 f
dp/forwardMuxB/U76/Z (aor222d1)           0.34       1.61 f
dp/forwardMuxB/y[14] (mux3_3)             0.00       1.61 f
dp/srcbmux/d0[14] (mux3_2)                0.00       1.61 f
dp/srcbmux/U97/Z (aor222d2)               0.39       1.99 f
dp/srcbmux/y[14] (mux3_2)                 0.00       1.99 f
dp/alu/SrcB[14] (alu)                     0.00       1.99 f
dp/alu/U734/ZN (nr04d0)                   0.11       2.10 r
dp/alu/U735/ZN (nd04d0)                   0.15       2.25 f
dp/alu/U445/ZN (nr03d0)                   0.14       2.39 r
dp/alu/U419/Z (an03d2)                    0.21       2.59 r
dp/alu/U107/Z (an12d2)                    0.16       2.75 r
dp/alu/U278/ZN (nd02d2)                   0.08       2.83 f
dp/alu/U669/ZN (aoi221d1)                 0.31       3.15 r
dp/alu/U609/Z (aoim22d2)                  0.21       3.35 f
dp/alu/U104/ZN (nd02d2)                   0.04       3.39 r
dp/alu/U908/ZN (nr04d0)                   0.12       3.51 f
dp/alu/U597/ZN (nd03d0)                   0.11       3.62 r
dp/alu/U963/ZN (nr04d0)                   0.13       3.75 f
dp/alu/U995/Z (an04d1)                    0.16       3.90 f
dp/alu/U1001/ZN (nd04d0)                  0.08       3.99 r
dp/alu/U632/ZN (nr02d0)                   0.12       4.10 f
dp/alu/Zero (alu)                         0.00       4.10 f
dp/ZeroE (datapath)                       0.00       4.10 f
c/ZeroE (controller)                      0.00       4.10 f
c/U7/ZN (nr02d0)                          0.08       4.18 r
c/U15/ZN (nr02d0)                         0.11       4.29 f
c/U16/ZN (nd02d2)                         0.08       4.37 r
c/PCSrcE (controller)                     0.00       4.37 r
dp/PCSrcE (datapath)                      0.00       4.37 r
dp/U16/Z (bufbd2)                         0.14       4.51 r
dp/pcmux/s (mux2_2)                       0.00       4.51 r
dp/pcmux/U1/ZN (inv0d4)                   0.08       4.59 f
dp/pcmux/U4/ZN (invbd7)                   0.06       4.66 r
dp/pcmux/U18/Z (mx02d1)                   0.22       4.87 r
dp/pcmux/y[0] (mux2_2)                    0.00       4.87 r
dp/IF/d[0] (flopenr)                      0.00       4.87 r
dp/IF/q_reg[0]/D (decrq4)                 0.00       4.87 r
data arrival time                                    4.87

clock clk (rise edge)                     1.50       1.50
clock network delay (ideal)               0.00       1.50
clock uncertainty                        -0.10       1.40
dp/IF/q_reg[0]/CP (decrq4)                0.00       1.40 r
library setup time                       -0.18       1.22
data required time                                   1.22
-----------------------------------------------------------
data required time                                   1.22
```

```
  data arrival time                                       -4.87
  ---------------------------------------------------------------
  slack (VIOLATED)                                        -3.66


1
Filename : rt_1.rpt

Information: Updating design information... (UID-85)
Warning: Design 'riscv_pip_27' contains 1 high-fanout nets. A fanout
number of 1000 will be used for delay calculations involving these nets.
(TIM-134)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:55:06 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: cb13fs120_tsmc_max   Library: cb13fs120_tsmc_max
Wire Load Model Mode: enclosed

  Startpoint: dp/pipreg1/Rs1E_reg[1]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: dp/IF/q_reg[0]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 cb13fs120_tsmc_max
  hazardunit         ForQA                 cb13fs120_tsmc_max
  mux3_0             ForQA                 cb13fs120_tsmc_max
  datapath           35000                 cb13fs120_tsmc_max
  alu                8000                  cb13fs120_tsmc_max
  controller         ForQA                 cb13fs120_tsmc_max
  mux2_2             ForQA                 cb13fs120_tsmc_max

  Point                                    Incr       Path
  ------------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  dp/pipreg1/Rs1E_reg[1]/CP (dfcrq2)       0.00 #     0.00 r
  dp/pipreg1/Rs1E_reg[1]/Q (dfcrq2)        0.35       0.35 f
  dp/pipreg1/Rs1E[1] (ID_IEx)              0.00       0.35 f
  dp/Rs1E[1] (datapath)                    0.00       0.35 f
  h/Rs1E[1] (hazardunit)                   0.00       0.35 f
```

```
h/U67/ZN (nr04d0)                          0.18       0.53 r
h/U68/ZN (nd12d1)                          0.11       0.64 f
h/U71/Z (an02d1)                           0.12       0.76 f
h/U18/ZN (nd02d1)                          0.06       0.81 r
h/U13/ZN (nr02d0)                          0.08       0.89 f
h/U27/ZN (nr03d0)                          0.13       1.02 r
h/ForwardAE[0] (hazardunit)                0.00       1.02 r
dp/ForwardAE[0] (datapath)                 0.00       1.02 r
dp/forwardMuxA/s[0] (mux3_0)               0.00       1.02 r
dp/forwardMuxA/U6/Z (or02d2)               0.23       1.25 r
dp/forwardMuxA/U5/ZN (invbd2)              0.13       1.38 f
dp/forwardMuxA/U19/Z (aor222d1)            0.35       1.73 f
dp/forwardMuxA/y[6] (mux3_0)               0.00       1.73 f
dp/srcamux/d0[6] (mux2_1)                  0.00       1.73 f
dp/srcamux/U32/Z (mx02d2)                  0.29       2.02 f
dp/srcamux/y[6] (mux2_1)                   0.00       2.02 f
dp/alu/SrcA[6] (alu)                       0.00       2.02 f
dp/alu/U19/ZN (invbd4)                     0.08       2.10 r
dp/alu/U531/ZN (oai2222d2)                 0.44       2.54 f
dp/alu/U566/ZN (oai2222d1)                 0.30       2.84 r
dp/alu/U148/ZN (nd02d2)                    0.05       2.89 f
dp/alu/U276/Z (an02d1)                     0.10       2.99 f
dp/alu/U275/ZN (aoi322d1)                  0.30       3.29 r
dp/alu/U28/ZN (inv0d1)                     0.05       3.34 f
dp/alu/U246/Z (or03d2)                     0.24       3.58 f
dp/alu/U758/ZN (nr02d0)                    0.08       3.66 r
dp/alu/U759/ZN (nd04d0)                    0.12       3.78 f
dp/alu/U817/ZN (nr04d0)                    0.11       3.89 r
dp/alu/U875/ZN (nd04d0)                    0.14       4.03 f
dp/alu/U882/ZN (nr02d0)                    0.11       4.14 r
dp/alu/Zero (alu)                          0.00       4.14 r
dp/ZeroE (datapath)                        0.00       4.14 r
c/ZeroE (controller)                       0.00       4.14 r
c/U6/ZN (nr02d0)                           0.09       4.23 f
c/U15/ZN (nr02d0)                          0.09       4.32 r
c/U16/ZN (nd02d2)                          0.08       4.40 f
c/PCSrcE (controller)                      0.00       4.40 f
dp/PCSrcE (datapath)                       0.00       4.40 f
dp/U5/Z (bufbd3)                           0.13       4.53 f
dp/pcmux/s (mux2_2)                        0.00       4.53 f
dp/pcmux/U2/ZN (inv0d4)                    0.06       4.59 r
dp/pcmux/U5/ZN (invbd7)                    0.07       4.67 f
dp/pcmux/U6/Z (mx02d1)                     0.22       4.88 r
dp/pcmux/y[0] (mux2_2)                     0.00       4.88 r
dp/IF/d[0] (flopenr)                       0.00       4.88 r
dp/IF/q_reg[0]/D (decrq4)                  0.00       4.88 r
data arrival time                                     4.88

clock clk (rise edge)                      1.00       1.00
clock network delay (ideal)                0.00       1.00
clock uncertainty                         -0.10       0.90
dp/IF/q_reg[0]/CP (decrq4)                 0.00       0.90 r
library setup time                        -0.18       0.72
data required time                                    0.72
```

```
  ------------------------------------------------------------
  data required time                                    0.72
  data arrival time                                    -4.88
  ------------------------------------------------------------
  slack (VIOLATED)                                     -4.16


1
Filename : rt_2.rpt

Information: Updating design information... (UID-85)
Warning: Design 'riscv_pip_27' contains 1 high-fanout nets. A fanout
number of 1000 will be used for delay calculations involving these nets.
(TIM-134)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:57:16 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: cb13fs120_tsmc_max   Library: cb13fs120_tsmc_max
Wire Load Model Mode: enclosed

  Startpoint: dp/pipreg1/Rs1E_reg[1]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: dp/pipreg1/PCPlus4E_reg[7]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 cb13fs120_tsmc_max
  hazardunit         ForQA                 cb13fs120_tsmc_max
  mux3_0             ForQA                 cb13fs120_tsmc_max
  datapath           35000                 cb13fs120_tsmc_max
  mux2_1             ForQA                 cb13fs120_tsmc_max
  alu                8000                  cb13fs120_tsmc_max
  alu_DW01_add_5     8000                  cb13fs120_tsmc_max
  controller         ForQA                 cb13fs120_tsmc_max
  ID_IEx             8000                  cb13fs120_tsmc_max

  Point                                                   Incr       Path
  ------------------------------------------------------------------------
---
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
```

```
  dp/pipreg1/Rs1E_reg[1]/CP (dfcrq2)                      0.00 #     0.00
r
  dp/pipreg1/Rs1E_reg[1]/Q (dfcrq2)                       0.33       0.33
f
  dp/pipreg1/Rs1E[1] (ID_IEx)                             0.00       0.33
f
  dp/Rs1E[1] (datapath)                                   0.00       0.33
f
  h/Rs1E[1] (hazardunit)                                  0.00       0.33
f
  h/U84/ZN (nr03d0)                                       0.11       0.44
r
  h/U4/Z (an03d2)                                         0.17       0.61
r
  h/U85/ZN (nr02d0)                                       0.07       0.68
f
  h/U11/Z (an04d2)                                        0.17       0.85
f
  h/U30/ZN (nd02d2)                                       0.05       0.91
r
  h/U31/ZN (nd02d2)                                       0.05       0.95
f
  h/U64/ZN (nr04d4)                                       0.28       1.23
r
  h/ForwardAE[0] (hazardunit)                             0.00       1.23
r
  dp/ForwardAE[0] (datapath)                              0.00       1.23
r
  dp/forwardMuxA/s[0] (mux3_0)                            0.00       1.23
r
  dp/forwardMuxA/U36/ZN (invbd2)                          0.06       1.30
f
  dp/forwardMuxA/U61/ZN (nd02d0)                          0.06       1.36
r
  dp/forwardMuxA/U82/ZN (nd03d0)                          0.11       1.48
f
  dp/forwardMuxA/U60/ZN (nd02d1)                          0.08       1.55
r
  dp/forwardMuxA/y[0] (mux3_0)                            0.00       1.55
r
  dp/srcamux/d0[0] (mux2_1)                               0.00       1.55
r
  dp/srcamux/U28/ZN (nd02d2)                              0.06       1.62
f
  dp/srcamux/U29/ZN (nd02d2)                              0.06       1.67
r
  dp/srcamux/y[0] (mux2_1)                                0.00       1.67
r
  dp/alu/SrcA[0] (alu)                                    0.00       1.67
r
  dp/alu/U140/Z (buffd7)                                  0.13       1.80
r
  dp/alu/add_1_root_add_17_2/A[0] (alu_DW01_add_5)        0.00       1.80
r
```

```
  dp/alu/add_1_root_add_17_2/U538/ZN (nd12d1)              0.11       1.91
r
  dp/alu/add_1_root_add_17_2/U675/ZN (aoi21d4)             0.22       2.13
f
  dp/alu/add_1_root_add_17_2/U442/ZN (nd12d1)              0.12       2.26
f
  dp/alu/add_1_root_add_17_2/U695/ZN (nd02d2)              0.07       2.32
r
  dp/alu/add_1_root_add_17_2/U647/ZN (nd02d2)              0.08       2.40
f
  dp/alu/add_1_root_add_17_2/U385/ZN (nd02d2)              0.05       2.46
r
  dp/alu/add_1_root_add_17_2/U625/ZN (nd02d2)              0.07       2.53
f
  dp/alu/add_1_root_add_17_2/U696/Z (an02d2)               0.13       2.66
f
  dp/alu/add_1_root_add_17_2/U589/Z (ora21d1)              0.15       2.81
f
  dp/alu/add_1_root_add_17_2/U582/ZN (nd02d1)              0.06       2.87
r
  dp/alu/add_1_root_add_17_2/U583/ZN (nd02d2)              0.05       2.92
f
  dp/alu/add_1_root_add_17_2/SUM[12] (alu_DW01_add_5)      0.00       2.92
f
  dp/alu/U523/ZN (oaim211d2)                               0.29       3.21
f
  dp/alu/U1041/ZN (nr02d0)                                 0.06       3.27
r
  dp/alu/U1042/ZN (nd04d0)                                 0.13       3.40
f
  dp/alu/U1070/ZN (nr02d0)                                 0.08       3.48
r
  dp/alu/U1090/ZN (nd04d0)                                 0.13       3.61
f
  dp/alu/U1093/ZN (nr02d0)                                 0.08       3.70
r
  dp/alu/U323/Z (an04d2)                                   0.19       3.89
r
  dp/alu/Zero (alu)                                        0.00       3.89
r
  dp/ZeroE (datapath)                                      0.00       3.89
r
  c/ZeroE (controller)                                     0.00       3.89
r
  c/U6/ZN (nr02d0)                                         0.07       3.97
f
  c/U19/ZN (nr02d0)                                        0.09       4.06
r
  c/U1/ZN (nd02d2)                                         0.09       4.15
f
  c/PCSrcE (controller)                                    0.00       4.15
f
  h/PCSrcE (hazardunit)                                    0.00       4.15
f
```

```
  h/U20/ZN (invbd2)                                       0.06       4.20
r
  h/U66/ZN (nd02d2)                                       0.08       4.28
f
  h/FlushE (hazardunit)                                   0.00       4.28
f
  dp/FlushE (datapath)                                    0.00       4.28
f
  dp/pipreg1/clear (ID_IEx)                               0.00       4.28
f
  dp/pipreg1/U10/ZN (invbd4)                              0.05       4.34
r
  dp/pipreg1/U20/Z (buffd7)                               0.13       4.47
r
  dp/pipreg1/U6/Z (buffd7)                                0.13       4.60
r
  dp/pipreg1/U41/Z (an02d1)                               0.11       4.71
r
  dp/pipreg1/PCPlus4E_reg[7]/D (dfcrq1)                   0.00       4.71
r
  data arrival time                                                  4.71

  clock clk (rise edge)                                   2.00       2.00
  clock network delay (ideal)                             0.00       2.00
  clock uncertainty                                      -0.10       1.90
  dp/pipreg1/PCPlus4E_reg[7]/CP (dfcrq1)                  0.00       1.90
r
  library setup time                                     -0.09       1.81
  data required time                                                 1.81
  ------------------------------------------------------------------------
---
  data required time                                                 1.81
  data arrival time                                                 -4.71
  ------------------------------------------------------------------------
---
  slack (VIOLATED)                                                  -2.90


1
Filename : rt_3.rpt

Information: Updating design information... (UID-85)
Warning: Design 'riscv_pip_27' contains 1 high-fanout nets. A fanout
number of 1000 will be used for delay calculations involving these nets.
(TIM-134)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 23:00:13 2023
```

```
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: cb13fs120_tsmc_max   Library: cb13fs120_tsmc_max
Wire Load Model Mode: enclosed

  Startpoint: dp/pipreg1/Rs2E_reg[1]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: dp/pipreg1/PCE_reg[20]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 cb13fs120_tsmc_max
  hazardunit         ForQA                 cb13fs120_tsmc_max
  mux3_3             ForQA                 cb13fs120_tsmc_max
  datapath           35000                 cb13fs120_tsmc_max
  mux3_2             ForQA                 cb13fs120_tsmc_max
  alu                8000                  cb13fs120_tsmc_max
  alu_DW01_add_5     8000                  cb13fs120_tsmc_max
  controller         ForQA                 cb13fs120_tsmc_max
  ID_IEx             8000                  cb13fs120_tsmc_max

  Point                                                   Incr       Path
  ------------------------------------------------------------------------
---
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  dp/pipreg1/Rs2E_reg[1]/CP (dfcrq2)                      0.00 #     0.00
r
  dp/pipreg1/Rs2E_reg[1]/Q (dfcrq2)                       0.33       0.33
r
  dp/pipreg1/Rs2E[1] (ID_IEx)                             0.00       0.33
r
  dp/Rs2E[1] (datapath)                                   0.00       0.33
r
  h/Rs2E[1] (hazardunit)                                  0.00       0.33
r
  h/U107/ZN (nr03d0)                                      0.15       0.47
f
  h/U34/ZN (nd02d1)                                       0.07       0.55
r
  h/U108/Z (an02d1)                                       0.10       0.65
r
  h/U88/ZN (nd03d0)                                       0.10       0.75
f
  h/U99/ZN (nr03d0)                                       0.15       0.90
r
  h/U97/ZN (invbd2)                                       0.10       1.00
f
```

```
  h/U98/ZN (invbd7)                                       0.05       1.06
r
  h/ForwardBE[0] (hazardunit)                             0.00       1.06
r
  dp/ForwardBE[0] (datapath)                              0.00       1.06
r
  dp/forwardMuxB/s[0] (mux3_3)                            0.00       1.06
r
  dp/forwardMuxB/U14/ZN (invbd7)                          0.05       1.11
f
  dp/forwardMuxB/U74/ZN (nd02d2)                          0.07       1.17
r
  dp/forwardMuxB/U47/ZN (invbd7)                          0.07       1.24
f
  dp/forwardMuxB/U2/Z (aor222d2)                          0.35       1.59
f
  dp/forwardMuxB/y[27] (mux3_3)                           0.00       1.59
f
  dp/srcbmux/d0[27] (mux3_2)                              0.00       1.59
f
  dp/srcbmux/U82/ZN (nd02d1)                              0.05       1.64
r
  dp/srcbmux/U55/ZN (nd03d0)                              0.10       1.74
f
  dp/srcbmux/y[27] (mux3_2)                               0.00       1.74
f
  dp/alu/SrcB[27] (alu)                                   0.00       1.74
f
  dp/alu/U407/Z (bufbd2)                                  0.13       1.86
f
  dp/alu/U724/Z (xr02d2)                                  0.27       2.13
f
  dp/alu/add_1_root_add_17_2/B[27] (alu_DW01_add_5)       0.00       2.13
f
  dp/alu/add_1_root_add_17_2/U827/ZN (nr02d0)             0.07       2.20
r
  dp/alu/add_1_root_add_17_2/U541/Z (an12d2)              0.19       2.39
f
  dp/alu/add_1_root_add_17_2/U501/ZN (nd02d2)             0.07       2.46
r
  dp/alu/add_1_root_add_17_2/U705/ZN (nd02d2)             0.06       2.52
f
  dp/alu/add_1_root_add_17_2/U374/Z (an12d2)              0.11       2.63
f
  dp/alu/add_1_root_add_17_2/U679/ZN (nr02d0)             0.05       2.68
r
  dp/alu/add_1_root_add_17_2/U707/ZN (oaim21d2)           0.18       2.87
f
  dp/alu/add_1_root_add_17_2/U581/Z (or02d1)              0.12       2.98
f
  dp/alu/add_1_root_add_17_2/U432/ZN (nd02d1)             0.06       3.04
r
  dp/alu/add_1_root_add_17_2/U395/ZN (nd02d2)             0.08       3.12
f
```

```
  dp/alu/add_1_root_add_17_2/SUM[31] (alu_DW01_add_5)      0.00       3.12
f
  dp/alu/U801/Z (or04d1)                                   0.22       3.34
f
  dp/alu/U769/ZN (nd12d1)                                  0.05       3.39
r
  dp/alu/U529/ZN (nd04d0)                                  0.12       3.50
f
  dp/alu/U760/ZN (nr03d0)                                  0.16       3.66
r
  dp/alu/Zero (alu)                                        0.00       3.66
r
  dp/ZeroE (datapath)                                      0.00       3.66
r
  c/ZeroE (controller)                                     0.00       3.66
r
  c/U5/ZN (nr02d0)                                         0.11       3.77
f
  c/U11/ZN (nr02d0)                                        0.09       3.86
r
  c/U1/ZN (nd02d2)                                         0.08       3.94
f
  c/PCSrcE (controller)                                    0.00       3.94
f
  h/PCSrcE (hazardunit)                                    0.00       3.94
f
  h/U22/ZN (inv0d2)                                        0.05       3.99
r
  h/U102/ZN (nd02d2)                                       0.08       4.07
f
  h/FlushE (hazardunit)                                    0.00       4.07
f
  dp/FlushE (datapath)                                     0.00       4.07
f
  dp/pipreg1/clear (ID_IEx)                                0.00       4.07
f
  dp/pipreg1/U32/ZN (invbd4)                               0.04       4.11
r
  dp/pipreg1/U25/Z (bufbd4)                                0.16       4.27
r
  dp/pipreg1/U55/Z (buffd7)                                0.15       4.42
r
  dp/pipreg1/U153/Z (an02d1)                               0.12       4.54
r
  dp/pipreg1/PCE_reg[20]/D (dfcrq4)                        0.00       4.54
r
  data arrival time                                                   4.54

  clock clk (rise edge)                                    3.00       3.00
  clock network delay (ideal)                              0.00       3.00
  clock uncertainty                                       -0.10       2.90
  dp/pipreg1/PCE_reg[20]/CP (dfcrq4)                       0.00       2.90
r
  library setup time                                      -0.09       2.81
```

```
  data required time                                                 2.81
  ------------------------------------------------------------------------
---
  data required time                                                 2.81
  data arrival time                                                 -4.54
  ------------------------------------------------------------------------
---
  slack (VIOLATED)                                                  -1.73


1
Filename : rt_4.rpt

Information: Updating design information... (UID-85)
Warning: Design 'riscv_pip_27' contains 1 high-fanout nets. A fanout
number of 1000 will be used for delay calculations involving these nets.
(TIM-134)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 23:02:17 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: cb13fs120_tsmc_max   Library: cb13fs120_tsmc_max
Wire Load Model Mode: enclosed

  Startpoint: dp/pipreg1/Rs2E_reg[2]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: dp/IF/q_reg[1]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 cb13fs120_tsmc_max
  hazardunit         ForQA                 cb13fs120_tsmc_max
  mux3_3             ForQA                 cb13fs120_tsmc_max
  datapath           35000                 cb13fs120_tsmc_max
  alu                8000                  cb13fs120_tsmc_max
  alu_DW01_add_5     8000                  cb13fs120_tsmc_max
  controller         ForQA                 cb13fs120_tsmc_max
  mux2_2             ForQA                 cb13fs120_tsmc_max

  Point                                                   Incr       Path
  ------------------------------------------------------------------------
---
```

```
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  dp/pipreg1/Rs2E_reg[2]/CP (dfcrq2)                      0.00 #     0.00
r
  dp/pipreg1/Rs2E_reg[2]/Q (dfcrq2)                       0.34       0.34
f
  dp/pipreg1/Rs2E[2] (ID_IEx)                             0.00       0.34
f
  dp/Rs2E[2] (datapath)                                   0.00       0.34
f
  h/Rs2E[2] (hazardunit)                                  0.00       0.34
f
  h/U67/ZN (invbd2)                                       0.04       0.38
r
  h/U82/Z (xr02d1)                                        0.23       0.61
r
  h/U31/ZN (invbd2)                                       0.04       0.65
f
  h/U83/ZN (nr04d0)                                       0.09       0.74
r
  h/U89/ZN (nr04d0)                                       0.12       0.86
f
  h/ForwardBE[0] (hazardunit)                             0.00       0.86
f
  dp/ForwardBE[0] (datapath)                              0.00       0.86
f
  dp/forwardMuxB/s[0] (mux3_3)                            0.00       0.86
f
  dp/forwardMuxB/U35/Z (buffd3)                           0.17       1.04
f
  dp/forwardMuxB/U108/ZN (invbd7)                         0.04       1.08
r
  dp/forwardMuxB/U121/ZN (nd02d2)                         0.07       1.15
f
  dp/forwardMuxB/U7/ZN (inv0d2)                           0.04       1.18
r
  dp/forwardMuxB/U26/ZN (nd02d2)                          0.05       1.23
f
  dp/forwardMuxB/U22/ZN (nd02d2)                          0.04       1.28
r
  dp/forwardMuxB/U24/ZN (invbd2)                          0.04       1.32
f
  dp/forwardMuxB/U23/ZN (nd02d2)                          0.04       1.36
r
  dp/forwardMuxB/y[0] (mux3_3)                            0.00       1.36
r
  dp/srcbmux/d0[0] (mux3_2)                               0.00       1.36
r
  dp/srcbmux/U109/Z (aoim22d1)                            0.19       1.55
r
  dp/srcbmux/y[0] (mux3_2)                                0.00       1.55
r
  dp/alu/SrcB[0] (alu)                                    0.00       1.55
r
```

```
  dp/alu/U666/ZN (invbd2)                                 0.08       1.63
f
  dp/alu/U226/ZN (invbd7)                                 0.05       1.68
r
  dp/alu/U354/ZN (xn02d1)                                 0.20       1.88
r
  dp/alu/add_1_root_add_17_2/B[0] (alu_DW01_add_5)        0.00       1.88
r
  dp/alu/add_1_root_add_17_2/U488/ZN (aoi21d4)            0.23       2.11
f
  dp/alu/add_1_root_add_17_2/U411/Z (or02d2)              0.14       2.24
f
  dp/alu/add_1_root_add_17_2/U498/ZN (nd02d2)             0.05       2.29
r
  dp/alu/add_1_root_add_17_2/U583/ZN (nd12d1)             0.08       2.37
f
  dp/alu/add_1_root_add_17_2/U575/ZN (nd02d2)             0.07       2.44
r
  dp/alu/add_1_root_add_17_2/U609/ZN (invbd2)             0.05       2.50
f
  dp/alu/add_1_root_add_17_2/U535/ZN (nd02d2)             0.04       2.54
r
  dp/alu/add_1_root_add_17_2/U601/ZN (nd02d2)             0.05       2.59
f
  dp/alu/add_1_root_add_17_2/SUM[3] (alu_DW01_add_5)      0.00       2.59
f
  dp/alu/U574/ZN (aoi2222d2)                              0.23       2.82
r
  dp/alu/U560/ZN (aon211d1)                               0.23       3.04
f
  dp/alu/U1047/ZN (nr04d0)                                0.16       3.20
r
  dp/alu/U1049/ZN (nd03d0)                                0.12       3.32
f
  dp/alu/U1055/ZN (nr04d0)                                0.11       3.43
r
  dp/alu/U1056/ZN (nd04d0)                                0.16       3.58
f
  dp/alu/U1061/ZN (nr04d0)                                0.22       3.81
r
  dp/alu/Zero (alu)                                       0.00       3.81
r
  dp/ZeroE (datapath)                                     0.00       3.81
r
  c/ZeroE (controller)                                    0.00       3.81
r
  c/U9/ZN (nr02d0)                                        0.12       3.92
f
  c/U10/ZN (nr02d0)                                       0.09       4.02
r
  c/U18/ZN (nd02d2)                                       0.08       4.10
f
  c/PCSrcE (controller)                                   0.00       4.10
f
```

```
  dp/PCSrcE (datapath)                                    0.00       4.10
f
  dp/U3/Z (bufbd2)                                        0.14       4.24
f
  dp/pcmux/s (mux2_2)                                     0.00       4.24
f
  dp/pcmux/U2/Z (bufbd7)                                  0.15       4.38
f
  dp/pcmux/U4/Z (mx02d1)                                  0.22       4.60
r
  dp/pcmux/y[1] (mux2_2)                                  0.00       4.60
r
  dp/IF/d[1] (flopenr)                                    0.00       4.60
r
  dp/IF/q_reg[1]/D (decrq4)                               0.00       4.60
r
  data arrival time                                                  4.60

  clock clk (rise edge)                                   4.00       4.00
  clock network delay (ideal)                             0.00       4.00
  clock uncertainty                                      -0.10       3.90
  dp/IF/q_reg[1]/CP (decrq4)                              0.00       3.90
r
  library setup time                                     -0.18       3.72
  data required time                                                 3.72
  ------------------------------------------------------------------------
---
  data required time                                                 3.72
  data arrival time                                                 -4.60
  ------------------------------------------------------------------------
---
  slack (VIOLATED)                                                  -0.88


1
Filename : rt_5.5.rpt

Information: Updating design information... (UID-85)
Warning: Design 'riscv_pip_27' contains 1 high-fanout nets. A fanout
number of 1000 will be used for delay calculations involving these nets.
(TIM-134)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 23:05:16 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.
```

```
Operating Conditions: cb13fs120_tsmc_max   Library: cb13fs120_tsmc_max
Wire Load Model Mode: enclosed

  Startpoint: dp/pipreg1/Rs2E_reg[0]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: dp/IF/q_reg[0]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 cb13fs120_tsmc_max
  hazardunit         ForQA                 cb13fs120_tsmc_max
  mux3_3             ForQA                 cb13fs120_tsmc_max
  datapath           35000                 cb13fs120_tsmc_max
  mux3_2             ForQA                 cb13fs120_tsmc_max
  alu                8000                  cb13fs120_tsmc_max
  controller         ForQA                 cb13fs120_tsmc_max
  mux2_2             ForQA                 cb13fs120_tsmc_max

  Point                                    Incr       Path
  ------------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  dp/pipreg1/Rs2E_reg[0]/CP (dfcrq2)       0.00 #     0.00 r
  dp/pipreg1/Rs2E_reg[0]/Q (dfcrq2)        0.35       0.35 f
  dp/pipreg1/Rs2E[0] (ID_IEx)              0.00       0.35 f
  dp/Rs2E[0] (datapath)                    0.00       0.35 f
  h/Rs2E[0] (hazardunit)                   0.00       0.35 f
  h/U30/ZN (xn02d1)                        0.25       0.60 f
  h/U20/Z (an04d2)                         0.15       0.75 f
  h/U23/ZN (nd02d2)                        0.05       0.80 r
  h/U18/ZN (invbd2)                        0.04       0.84 f
  h/U16/ZN (nr04d4)                        0.27       1.11 r
  h/ForwardBE[0] (hazardunit)              0.00       1.11 r
  dp/ForwardBE[0] (datapath)               0.00       1.11 r
  dp/forwardMuxB/s[0] (mux3_3)             0.00       1.11 r
  dp/forwardMuxB/U59/ZN (nd02d1)           0.06       1.17 f
  dp/forwardMuxB/U8/Z (buffd4)             0.17       1.34 f
  dp/forwardMuxB/U22/ZN (invbda)           0.06       1.40 r
  dp/forwardMuxB/U3/ZN (nd02d2)            0.05       1.46 f
  dp/forwardMuxB/U45/ZN (nd03d0)           0.11       1.57 r
  dp/forwardMuxB/y[9] (mux3_3)             0.00       1.57 r
  dp/srcbmux/d0[9] (mux3_2)                0.00       1.57 r
  dp/srcbmux/U74/Z (aor221d1)              0.17       1.74 r
  dp/srcbmux/U42/Z (an02d2)                0.18       1.92 r
  dp/srcbmux/y[9] (mux3_2)                 0.00       1.92 r
  dp/alu/SrcB[9] (alu)                     0.00       1.92 r
  dp/alu/U214/Z (or03d1)                   0.17       2.08 r
  dp/alu/U365/ZN (nr02d0)                  0.10       2.18 f
  dp/alu/U334/ZN (nd02d1)                  0.07       2.26 r
  dp/alu/U212/ZN (inv0d2)                  0.05       2.31 f
  dp/alu/U397/ZN (nd02d2)                  0.06       2.37 r
```

```
  dp/alu/U49/ZN (invbd2)                   0.05       2.42 f
  dp/alu/U13/Z (an02d4)                    0.17       2.59 f
  dp/alu/U496/ZN (nd02d2)                  0.07       2.66 r
  dp/alu/U7/ZN (invbd4)                    0.07       2.73 f
  dp/alu/U6/ZN (nd02d1)                    0.10       2.83 r
  dp/alu/U629/ZN (oai322d1)                0.59       3.42 f
  dp/alu/U270/Z (aor211d1)                 0.21       3.63 f
  dp/alu/U850/ZN (nr04d0)                  0.14       3.77 r
  dp/alu/U852/ZN (nd04d0)                  0.14       3.92 f
  dp/alu/U853/ZN (nr03d0)                  0.14       4.05 r
  dp/alu/U863/ZN (nd04d0)                  0.15       4.20 f
  dp/alu/U864/ZN (nr02d0)                  0.12       4.32 r
  dp/alu/Zero (alu)                        0.00       4.32 r
  dp/ZeroE (datapath)                      0.00       4.32 r
  c/ZeroE (controller)                     0.00       4.32 r
  c/U13/ZN (nd03d0)                        0.10       4.42 f
  c/U14/ZN (nd03d0)                        0.11       4.53 r
  c/U15/ZN (nd12d1)                        0.10       4.63 f
  c/U16/ZN (nd02d2)                        0.09       4.73 r
  c/PCSrcE (controller)                    0.00       4.73 r
  dp/PCSrcE (datapath)                     0.00       4.73 r
  dp/U3/Z (buffd7)                         0.12       4.84 r
  dp/pcmux/s (mux2_2)                      0.00       4.84 r
  dp/pcmux/U2/Z (buffd7)                   0.15       4.99 r
  dp/pcmux/U33/Z (mx02d1)                  0.23       5.22 r
  dp/pcmux/y[0] (mux2_2)                   0.00       5.22 r
  dp/IF/d[0] (flopenr)                     0.00       5.22 r
  dp/IF/q_reg[0]/D (decrq4)                0.00       5.22 r
  data arrival time                                   5.22

  clock clk (rise edge)                    5.50       5.50
  clock network delay (ideal)              0.00       5.50
  clock uncertainty                       -0.10       5.40
  dp/IF/q_reg[0]/CP (decrq4)               0.00       5.40 r
  library setup time                      -0.18       5.22
  data required time                                  5.22
  ----------------------------------------------------------
  data required time                                  5.22
  data arrival time                                  -5.22
  ----------------------------------------------------------
  slack (MET)                                         0.00


1
Filename : rt_5.rpt

Information: Updating design information... (UID-85)
Warning: Design 'riscv_pip_27' contains 1 high-fanout nets. A fanout
number of 1000 will be used for delay calculations involving these nets.
(TIM-134)

****************************************
Report : timing
        -path full
```

```
        -delay max
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 23:04:13 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: cb13fs120_tsmc_max   Library: cb13fs120_tsmc_max
Wire Load Model Mode: enclosed

  Startpoint: dp/pipreg1/PCE_reg[27]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: dp/pipreg0/PCD_reg[22]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 cb13fs120_tsmc_max
  datapath           35000                 cb13fs120_tsmc_max
  adder_1_DW01_add_1 8000                  cb13fs120_tsmc_max
  mux3_2             ForQA                 cb13fs120_tsmc_max
  alu                8000                  cb13fs120_tsmc_max
  controller         ForQA                 cb13fs120_tsmc_max
  IF_ID              8000                  cb13fs120_tsmc_max

  Point                                                        Incr       Path
  ------------------------------------------------------------------------------
---
  clock clk (rise edge)                                        0.00       0.00
  clock network delay (ideal)                                  0.00       0.00
  dp/pipreg1/PCE_reg[27]/CP (dfcrq1)                           0.00 #     0.00
r
  dp/pipreg1/PCE_reg[27]/Q (dfcrq1)                            0.37       0.37
f
  dp/pipreg1/PCE[27] (ID_IEx)                                  0.00       0.37
f
  dp/pcaddbranch/a[27] (adder_1)                               0.00       0.37
f
  dp/pcaddbranch/add_2/A[27] (adder_1_DW01_add_1)              0.00       0.37
f
  dp/pcaddbranch/add_2/U367/ZN (nd02d1)                        0.10       0.47
r
  dp/pcaddbranch/add_2/U59/ZN (oai21d1)                        0.23       0.70
f
  dp/pcaddbranch/add_2/U527/ZN (aoi21d4)                       0.22       0.92
r
  dp/pcaddbranch/add_2/U43/ZN (oai21d1)                        0.20       1.12
f
  dp/pcaddbranch/add_2/U368/Z (aor21d2)                        0.17       1.29
f
```

```
  dp/pcaddbranch/add_2/U580/ZN (nr02d0)                    0.08       1.37
r
  dp/pcaddbranch/add_2/U585/ZN (nd02d1)                    0.09       1.45
f
  dp/pcaddbranch/add_2/U495/ZN (nd02d2)                    0.07       1.52
r
  dp/pcaddbranch/add_2/SUM[29] (adder_1_DW01_add_1)        0.00       1.52
r
  dp/pcaddbranch/y[29] (adder_1)                           0.00       1.52
r
  dp/srcbmux/d2[29] (mux3_2)                               0.00       1.52
r
  dp/srcbmux/U43/ZN (nd02d2)                               0.05       1.57
f
  dp/srcbmux/U7/ZN (nd03d4)                                0.24       1.81
r
  dp/srcbmux/y[29] (mux3_2)                                0.00       1.81
r
  dp/alu/SrcB[29] (alu)                                    0.00       1.81
r
  dp/alu/U553/ZN (invbd2)                                  0.04       1.84
f
  dp/alu/U322/ZN (nd04d0)                                  0.08       1.93
r
  dp/alu/U728/ZN (nr04d0)                                  0.13       2.06
f
  dp/alu/U32/Z (an04d2)                                    0.19       2.25
f
  dp/alu/U49/Z (an02d2)                                    0.13       2.38
f
  dp/alu/U48/ZN (nd02d2)                                   0.08       2.47
r
  dp/alu/U34/ZN (invbd7)                                   0.08       2.54
f
  dp/alu/U23/ZN (nd02d2)                                   0.04       2.59
r
  dp/alu/U467/ZN (oai322d1)                                0.62       3.21
f
  dp/alu/U580/Z (aor211d1)                                 0.20       3.41
f
  dp/alu/U924/ZN (nr02d0)                                  0.06       3.48
r
  dp/alu/U611/ZN (nd03d0)                                  0.10       3.58
f
  dp/alu/U642/ZN (nr03d0)                                  0.09       3.67
r
  dp/alu/U982/ZN (nd04d0)                                  0.13       3.80
f
  dp/alu/U989/ZN (nr03d0)                                  0.18       3.98
r
  dp/alu/Zero (alu)                                        0.00       3.98
r
  dp/ZeroE (datapath)                                      0.00       3.98
r
```

```
  c/ZeroE (controller)                                    0.00       3.98
r
  c/U10/ZN (nd02d1)                                       0.11       4.09
f
  c/U4/ZN (nd02d2)                                        0.05       4.14
r
  c/U5/ZN (invbd2)                                        0.04       4.18
f
  c/U13/ZN (nd02d2)                                       0.07       4.25
r
  c/PCSrcE (controller)                                   0.00       4.25
r
  h/PCSrcE (hazardunit)                                   0.00       4.25
r
  h/FlushD (hazardunit)                                   0.00       4.25
r
  dp/FlushD (datapath)                                    0.00       4.25
r
  dp/pipreg0/clear (IF_ID)                                0.00       4.25
r
  dp/pipreg0/U18/Z (or02d2)                               0.18       4.42
r
  dp/pipreg0/U8/Z (buffd7)                                0.15       4.58
r
  dp/pipreg0/U14/ZN (invbd7)                              0.07       4.65
f
  dp/pipreg0/U81/Z (aor22d1)                              0.18       4.83
f
  dp/pipreg0/PCD_reg[22]/D (dfcrq4)                       0.00       4.83
f
  data arrival time                                                  4.83

  clock clk (rise edge)                                   5.00       5.00
  clock network delay (ideal)                             0.00       5.00
  clock uncertainty                                      -0.10       4.90
  dp/pipreg0/PCD_reg[22]/CP (dfcrq4)                      0.00       4.90
r
  library setup time                                     -0.07       4.83
  data required time                                                 4.83
  ------------------------------------------------------------------------
---
  data required time                                                 4.83
  data arrival time                                                 -4.83
  ------------------------------------------------------------------------
---
  slack (MET)                                                        0.00


1
Filename : rt_min_0.5.rpt


****************************************
Report : timing
```

```
        -path full
        -delay min
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:53:45 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: cb13fs120_tsmc_max   Library: cb13fs120_tsmc_max
Wire Load Model Mode: enclosed

  Startpoint: c/c_pipreg1/ResultSrcM_reg[0]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: c/c_pipreg2/ResultSrcW_reg[0]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 cb13fs120_tsmc_max
  controller         8000                  cb13fs120_tsmc_max

  Point                                                    Incr       Path
  ---------------------------------------------------------------------------
---
  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  c/c_pipreg1/ResultSrcM_reg[0]/CP (dfcrq1)                0.00 #     0.00
r
  c/c_pipreg1/ResultSrcM_reg[0]/Q (dfcrq1)                 0.29       0.29
f
  c/c_pipreg1/ResultSrcM[0] (c_IEx_IM)                     0.00       0.29
f
  c/c_pipreg2/ResultSrcM[0] (c_IM_IW)                      0.00       0.29
f
  c/c_pipreg2/ResultSrcW_reg[0]/D (dfcrq2)                 0.00       0.29
f
  data arrival time                                                   0.29

  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  c/c_pipreg2/ResultSrcW_reg[0]/CP (dfcrq2)                0.00       0.00
r
  library hold time                                        0.00       0.00
  data required time                                                  0.00
  ---------------------------------------------------------------------------
---
  data required time                                                  0.00
  data arrival time                                                  -0.29
  ---------------------------------------------------------------------------
---
```

```
  slack (MET)                                                              0.29


1
Filename : rt_min_1.5.rpt


****************************************
Report : timing
        -path full
        -delay min
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Sun Jul 30 03:09:14 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: cb13fs120_tsmc_max   Library: cb13fs120_tsmc_max
Wire Load Model Mode: enclosed

  Startpoint: c/c_pipreg1/ResultSrcM_reg[0]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: c/c_pipreg2/ResultSrcW_reg[0]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 cb13fs120_tsmc_max
  controller         8000                  cb13fs120_tsmc_max

  Point                                                    Incr       Path
  ------------------------------------------------------------------------
---
  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  c/c_pipreg1/ResultSrcM_reg[0]/CP (dfcrq1)                0.00 #     0.00
r
  c/c_pipreg1/ResultSrcM_reg[0]/Q (dfcrq1)                 0.29       0.29
f
  c/c_pipreg1/ResultSrcM[0] (c_IEx_IM)                     0.00       0.29
f
  c/c_pipreg2/ResultSrcM[0] (c_IM_IW)                      0.00       0.29
f
  c/c_pipreg2/ResultSrcW_reg[0]/D (dfcrq2)                 0.00       0.29
f
  data arrival time                                                   0.29

  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
```

```
  c/c_pipreg2/ResultSrcW_reg[0]/CP (dfcrq2)               0.00       0.00
r
  library hold time                                       0.00       0.00
  data required time                                                 0.00
  ---------------------------------------------------------------------------
---
  data required time                                                 0.00
  data arrival time                                                 -0.29
  ---------------------------------------------------------------------------
---
  slack (MET)                                                        0.29


1
Filename : rt_min_1.rpt


****************************************
Report : timing
        -path full
        -delay min
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:55:06 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: cb13fs120_tsmc_max   Library: cb13fs120_tsmc_max
Wire Load Model Mode: enclosed

  Startpoint: c/c_pipreg1/ResultSrcM_reg[0]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: c/c_pipreg2/ResultSrcW_reg[0]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 cb13fs120_tsmc_max
  controller         ForQA                 cb13fs120_tsmc_max

  Point                                                   Incr       Path
  ---------------------------------------------------------------------------
---
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  c/c_pipreg1/ResultSrcM_reg[0]/CP (dfcrq1)               0.00 #     0.00
r
  c/c_pipreg1/ResultSrcM_reg[0]/Q (dfcrq1)                0.29       0.29
f
```

```
  c/c_pipreg1/ResultSrcM[0] (c_IEx_IM)                    0.00       0.29
f
  c/c_pipreg2/ResultSrcM[0] (c_IM_IW)                     0.00       0.29
f
  c/c_pipreg2/ResultSrcW_reg[0]/D (dfcrq2)                0.00       0.29
f
  data arrival time                                                  0.29

  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  c/c_pipreg2/ResultSrcW_reg[0]/CP (dfcrq2)               0.00       0.00
r
  library hold time                                       0.00       0.00
  data required time                                                 0.00
  ------------------------------------------------------------------------
---
  data required time                                                 0.00
  data arrival time                                                 -0.29
  ------------------------------------------------------------------------
---
  slack (MET)                                                        0.29


1
Filename : rt_min_2.rpt


****************************************
Report : timing
        -path full
        -delay min
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 22:57:16 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: cb13fs120_tsmc_max   Library: cb13fs120_tsmc_max
Wire Load Model Mode: enclosed

  Startpoint: c/c_pipreg1/ResultSrcM_reg[1]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: c/c_pipreg2/ResultSrcW_reg[1]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 cb13fs120_tsmc_max
  controller         ForQA                 cb13fs120_tsmc_max
```

```
  Point                                                   Incr       Path
  ------------------------------------------------------------------------
---
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  c/c_pipreg1/ResultSrcM_reg[1]/CP (dfcrq1)               0.00 #     0.00
r
  c/c_pipreg1/ResultSrcM_reg[1]/Q (dfcrq1)                0.29       0.29
f
  c/c_pipreg1/ResultSrcM[1] (c_IEx_IM)                    0.00       0.29
f
  c/c_pipreg2/ResultSrcM[1] (c_IM_IW)                     0.00       0.29
f
  c/c_pipreg2/ResultSrcW_reg[1]/D (dfcrq2)                0.00       0.29
f
  data arrival time                                                  0.29

  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  c/c_pipreg2/ResultSrcW_reg[1]/CP (dfcrq2)               0.00       0.00
r
  library hold time                                       0.00       0.00
  data required time                                                 0.00
  ------------------------------------------------------------------------
---
  data required time                                                 0.00
  data arrival time                                                 -0.29
  ------------------------------------------------------------------------
---
  slack (MET)                                                        0.29


1
Filename : rt_min_3.rpt


****************************************
Report : timing
        -path full
        -delay min
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 23:00:13 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: cb13fs120_tsmc_max   Library: cb13fs120_tsmc_max
Wire Load Model Mode: enclosed

  Startpoint: c/c_pipreg1/ResultSrcM_reg[0]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: c/c_pipreg2/ResultSrcW_reg[0]
```

```
          (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 cb13fs120_tsmc_max
  controller         ForQA                 cb13fs120_tsmc_max

  Point                                                    Incr       Path
  -----------------------------------------------------------------------------
---
  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  c/c_pipreg1/ResultSrcM_reg[0]/CP (dfcrq1)                0.00 #     0.00
r
  c/c_pipreg1/ResultSrcM_reg[0]/Q (dfcrq1)                 0.29       0.29
f
  c/c_pipreg1/ResultSrcM[0] (c_IEx_IM)                     0.00       0.29
f
  c/c_pipreg2/ResultSrcM[0] (c_IM_IW)                      0.00       0.29
f
  c/c_pipreg2/ResultSrcW_reg[0]/D (dfcrq2)                 0.00       0.29
f
  data arrival time                                                   0.29

  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  c/c_pipreg2/ResultSrcW_reg[0]/CP (dfcrq2)                0.00       0.00
r
  library hold time                                        0.00       0.00
  data required time                                                  0.00
  -----------------------------------------------------------------------------
---
  data required time                                                  0.00
  data arrival time                                                  -0.29
  -----------------------------------------------------------------------------
---
  slack (MET)                                                         0.29


1
Filename : rt_min_4.rpt


****************************************
Report : timing
        -path full
        -delay min
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 23:02:17 2023
****************************************
```

```
 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: cb13fs120_tsmc_max   Library: cb13fs120_tsmc_max
Wire Load Model Mode: enclosed

  Startpoint: c/c_pipreg0/RegWriteE_reg
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: c/c_pipreg1/RegWriteM_reg
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 cb13fs120_tsmc_max
  controller         ForQA                 cb13fs120_tsmc_max

  Point                                                    Incr       Path
  -----------------------------------------------------------------------------
---
  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  c/c_pipreg0/RegWriteE_reg/CP (dfcrq1)                    0.00 #     0.00
r
  c/c_pipreg0/RegWriteE_reg/Q (dfcrq1)                     0.29       0.29
f
  c/c_pipreg0/RegWriteE (c_ID_IEx)                         0.00       0.29
f
  c/c_pipreg1/RegWriteE (c_IEx_IM)                         0.00       0.29
f
  c/c_pipreg1/RegWriteM_reg/D (dfcrq2)                     0.00       0.29
f
  data arrival time                                                   0.29

  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  c/c_pipreg1/RegWriteM_reg/CP (dfcrq2)                    0.00       0.00
r
  library hold time                                        0.00       0.00
  data required time                                                  0.00
  -----------------------------------------------------------------------------
---
  data required time                                                  0.00
  data arrival time                                                  -0.29
  -----------------------------------------------------------------------------
---
  slack (MET)                                                         0.29


1
Filename : rt_min_5.5.rpt
```

```
****************************************
Report : timing
        -path full
        -delay min
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 23:05:16 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: cb13fs120_tsmc_max   Library: cb13fs120_tsmc_max
Wire Load Model Mode: enclosed

  Startpoint: c/c_pipreg0/RegWriteE_reg
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: c/c_pipreg1/RegWriteM_reg
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 cb13fs120_tsmc_max
  controller         ForQA                 cb13fs120_tsmc_max

  Point                                                    Incr       Path
  ---------------------------------------------------------------------------
---
  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  c/c_pipreg0/RegWriteE_reg/CP (dfcrq1)                    0.00 #     0.00
r
  c/c_pipreg0/RegWriteE_reg/Q (dfcrq1)                     0.29       0.29
f
  c/c_pipreg0/RegWriteE (c_ID_IEx)                         0.00       0.29
f
  c/c_pipreg1/RegWriteE (c_IEx_IM)                         0.00       0.29
f
  c/c_pipreg1/RegWriteM_reg/D (dfcrq1)                     0.00       0.29
f
  data arrival time                                                   0.29

  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  c/c_pipreg1/RegWriteM_reg/CP (dfcrq1)                    0.00       0.00
r
  library hold time                                        0.00       0.00
  data required time                                                  0.00
  ---------------------------------------------------------------------------
---
  data required time                                                  0.00
  data arrival time                                                  -0.29
```

```
  ------------------------------------------------------------------------
---
  slack (MET)                                                       0.29


1
Filename : rt_min_5.rpt


****************************************
Report : timing
        -path full
        -delay min
        -max_paths 1
Design : riscv_pip_27
Version: P-2019.03-SP3
Date   : Fri Jul 28 23:04:14 2023
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: cb13fs120_tsmc_max   Library: cb13fs120_tsmc_max
Wire Load Model Mode: enclosed

  Startpoint: c/c_pipreg0/RegWriteE_reg
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: c/c_pipreg1/RegWriteM_reg
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  riscv_pip_27       35000                 cb13fs120_tsmc_max
  controller         ForQA                 cb13fs120_tsmc_max

  Point                                                    Incr       Path
  ------------------------------------------------------------------------
---
  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  c/c_pipreg0/RegWriteE_reg/CP (dfcrq1)                    0.00 #     0.00
r
  c/c_pipreg0/RegWriteE_reg/Q (dfcrq1)                     0.29       0.29
f
  c/c_pipreg0/RegWriteE (c_ID_IEx)                         0.00       0.29
f
  c/c_pipreg1/RegWriteE (c_IEx_IM)                         0.00       0.29
f
  c/c_pipreg1/RegWriteM_reg/D (dfcrq1)                     0.00       0.29
f
  data arrival time                                                   0.29

  clock clk (rise edge)                                    0.00       0.00
```

```
  clock network delay (ideal)                              0.00       0.00
  c/c_pipreg1/RegWriteM_reg/CP (dfcrq1)                    0.00       0.00
r
  library hold time                                        0.00       0.00
  data required time                                                  0.00
  ------------------------------------------------------------------------
---
  data required time                                                  0.00
  data arrival time                                                  -0.29
  ------------------------------------------------------------------------
---
  slack (MET)                                                         0.29


1
```