HIGH-EFFICIENCY, WIDE-INPUT-SUPPLY OSCILLATOR FOR
SWITCHED CAPACITOR CONVETER IN CMOS TECHNOLOGY

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By

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ABSTRACT

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In this project, a voltage-controlled ring oscillator (VCRO) cross-coupled charge pump (CCCP) is proposed. The design of the VCRO is investigated to develop a high-performance oscillator to drive a CCCP. The project is conducted via Cadence Virtuoso software and the circuit is designed using 0.18μm CMOS technology with supply voltage of 3.3V. A VCRO with high frequency ranges from 227.10Mhz to 2428.71MHz is developed. In addition, a CCCP is incorporated with the VCRO to achieve a maximum efficiency of 89.07%. The outcomes of the simulation reveal the better performance of the proposed design as compared to the previous studies in terms of oscillation frequency for VCRO and efficiency for CCCP. The proposed VCRO-CCCP can be utilized for fast charge up application such as supercapacitor-based energy storage system and stable charging for portable electronic device in particular, mobile phones.

Keywords – Switch capacitor converter, voltage-controlled ring oscillator, cross-coupled charge pump, energy harvesting, voltage doubler

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APPROVAL SHEET

This dissertation entitled "**HIGH-EFFICIENCY, WIDE-INPUT-SUPPLY OSCILLATOR FOR SWITCHED CAPACITOR CONVETER IN CMOS TECHNOLOGY**" was prepared by TAN MUN BIN and submitted as partial fulfilment of requirements for the degree of Master of Engineering in Electronic Systems at Universiti Tunku Abdul Rahman.

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_____

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DECLARATION

I <u>Tan Mun Bin</u> hereby declare that the thesis/dissertation is based on my original work except for quotations and citations which have been duly acknowledged. I also declare that it has not been previously or concurrently submitted for any other degree at UTAR or other institutions.

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(TAN MUN BIN)

Date: <u>29th July 2023</u>

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LIST OF ABBREVIATIONS

a-IGZO TFTs	Amorphous Indium-Gallium-Zinc- Oxide Thin-film transistors
n	Stage number
nMOS	N-type metal–oxide–semiconductor
pMOS	P-type metal–oxide–semiconductor
A	Anode
ADPLL	All-digital phase-locked loop
BGR	Bandgap reference
BT	Bootstrap
C	Cathod
CAGR	Compound annual growth rate
CCCP	Cross-coupled charge pump
CMOS	Complementary metal–oxide–semiconductor
CP	Charge pump
DBRO	Bootstrapped ring voltage-controlled oscillator
DC	Direct current
DGB	Dynamic gate-biasing
DVFS	Dynamic voltage frequency scaling

EDA	Electronic design automation
EH	Energy harvesting
ESOMAR	European Society for Opinion and Marketing Research
FD-SOI	Fully Depleted Silicon on Insulator technology
FOM	Figure of merit
G	Grid
HV	High-voltage
IC	Integrated circuit
IZO	Indium-zinc-oxide
LDO	Low dropout regulator
LET	Linear energy transfer
LSIs	Large scale integrated circuits
NOC	Non-overlapping clock
MOSFET	Metal-oxide-semiconductor field-effect transistor
PCE	Power conversion efficiency
PDP	Power-delay-product
RO	Ring oscillator
RVCO	Ring-voltage-controlled oscillator

SBNAND	Self-bias NAND
SCVM	Switched-capacitor voltage multiplier
SD	Skewed delay
SP	Serial parallel
SQC	Synchronous charge compensation
TFT	Thin-film transistor
ULV	Ultra-low-voltage
VCE	Voltage conversion efficiency
VCO	Voltage-controlled oscillator
VCRO	Voltage-controlled ring oscillator

CHAPTER 1

INTRODUCTION

1.1 DC-DC Converter Market and Demand

According to Future Market Insights (ESOMAR (European Society for Opinion and Marketing Research), certified market research organization and a member of Greater New York Chamber of Commerce) report in September 2022, global DC-DC (direct current) converter market demand is anticipated to be valued at US$ 10,334.6 million in 2022, and forecasted with 8.1% CAGR (compound annual growth rate) which to be valued at US$ 22,569.1 million from 2022 to 2032. DC-DC converter are extensively used for both commercial and residential applications. For instances, hybrid electrical vehicles, renewable energy sources, portable electronic devices and etc (Babaei, Abbasi and Sakhavati, 2016).

It is noteworthy that increasing use of electronic vehicles has greatly contributed to the growth of the market. Electric vehicles are gaining popularity globally owing to their better performance and zero carbon dioxide emission (Pandey et al., 2022). Indeed, rising focus on the renewable energy and environment boosts the demand for electric vehicles and hybrid vehicles globally. In recent years, developed countries are promoting battery-powered vehicles thus a regulated and steady power supply is required.

1.2 CMOS Technology

CMOS (Complementary Metal-Oxide-Semiconductor) technology is a type of semiconductor manufacturing process that is widely used to produce microchip for various electronic devices (Bhushan and Ketchen, 2011). In CMOS technology, a thin layer of silicon dioxide is used to insulate the gate of a MOSFET (Metal-oxide-semiconductor field-effect transistor) from the conducting channel, which is typically doped with p-type and n-type elements.

In CMOS circuit, both p-type and n-type MOSFETs are in a complementary manner. The most common example of the application of a CMOS is an inverter. When p-type MOSFET is used to pull the output voltage up to a high level, n-type MOSFET is used to pull the output voltage down to a low level. The operation of two MOSFETs will be reversed if the polarity of the signal is changed.

CMOS technology is known for its high level of integration, which allows for the creation of complex circuits on a single chip. It has low power consumption which makes it ideal for battery-operated devices. In addition, CMOS technology is relatively inexpensive compared to other manufacturing processes thus it's gaining popularity in electronic fields.

1.3 DC-DC Converter Types

A DC-DC converter is an electrical device that converts DC voltage from one voltage level to another. DC-DC converters are designed to operate within a broad range of voltage level for specific applications depending on the desired output voltage. There are variety of DC-DC converters available in the market

in which they could be categorized into two types which are linear voltage regulator and switching DC-DC converter (Brown et al., 2008). A linear voltage regulator will only lower or higher the voltage level from sources. It has to make sure that the output voltage is stable and consistent regardless of the type of load. The two main topologies for linear voltage regulator are shunt and series.

Enhancement has been made on ordinary DC-DC converter by adding transistors that act as switches and switching DC-DC converters are invented. They have a few advantages over linear DC-DC converter such as high efficiency, outstanding flexibility and wide range of input voltage. Most importantly, the switching operation is either fully conducting or fully blocking the current. As a result, the energy loss is minimal and usually is can achieve efficiency of 80% to 90%. Increasing the switching frequencies can further reduce the power loss. Overall, switched DC-DC converters offer a number of advantages over linear DC-DC converters. Figure 1.1 shows different types of DC-DC converters.
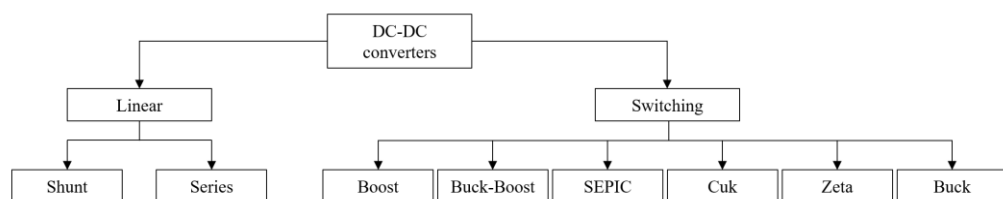
Figure 1.1: Types of DC-DC converter

1.4 Switched Capacitor Converter

A switched capacitor converter is a type of switching DC-DC conversion technology. Unlike traditional DC-DC converters, the switched capacitor converter accomplishes energy transfer and voltage conversion only using capacitors. Therefore, it can be integrated easily into a power IC (integrated

circuit) chip because it has small size and high-power density (Luo, 2013). The fundamental operation involves charge storing and discharging process of capacitors in order to achieve the desired voltage output. The speed of capacitor charging and discharging is manipulated by a control circuit such as an oscillator. Switched capacitor converters have high conversion efficiencies and hence topology using switched capacitors have aroused the interest of industry and academia in the search for high power density in power converters recently. The two most common switched capacitor voltage converters are the voltage inverter and voltage doubler as shown in Figure 1.2. This project will emphasize on voltage doubler which is also known as charge pump.
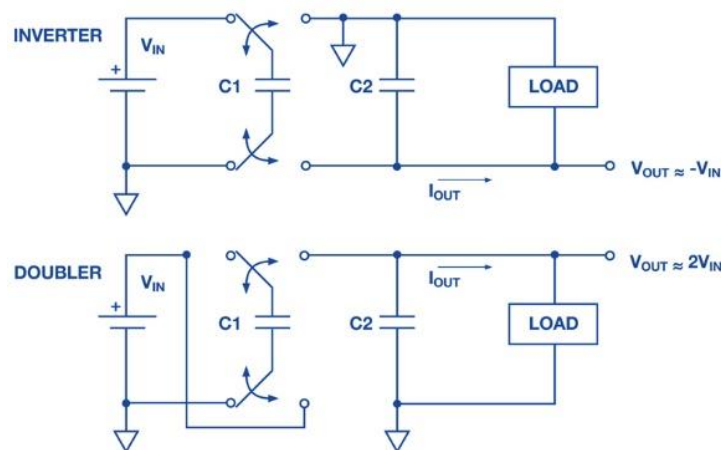
Figure 1.2: Topology of voltage inverter and voltage doubler

1.5 Cross-coupled Charge Pump

A charge pump is an electronic circuit that produces an output voltage that is double the input voltage. It is a voltage multiplier with a voltage multiplication factor equal to 2. Figure 1.3 shows the topology of Cross-Coupled Charge Pump (CCCP) with transistor as a switch (Ma and Bondade, 2012). The basic structure

of a CCCP consist of two capacitors and four switches arranged in a cross-coupled configuration. Those switches are controlled by alternating clock signals thus the capacitors will charge or discharge in a specific sequence.

The operation of CCCP is depicted in Figure 1.4 (Minami *et al.*, 2016). CLK1 and CLK2 signals function as antiphase clocks with same amplitude and frequency. When CLK1 is in LOW state and CLK2 is in HIGH state, the M1 is turned on and C_{CP1} is charged. Similarly, when CLK1 is in HIGH state and CLK2 is in LOW state, M2 is ON and C_{CP2} is charged. Two capacitors will take turn to discharge to out when M3 and M4 are turned on accordingly. By repeating this process, it is possible to calculate the output of the charge pump for N stage using the equation below:

$$V_{out} = V_{in} + N \times V_{CLK} \tag{1.1}$$

CCCP has potential for high boosting efficiency as it can operate without any loss since the charge does not flow except for the input and output terminals. Nonetheless, C_{CP1} and C_{CP2} are not only used for voltage boosting, but also for transistor gate driving. In other words, the charge is utilized to drive the MOS which may cause a decrease in the boosting efficiency.
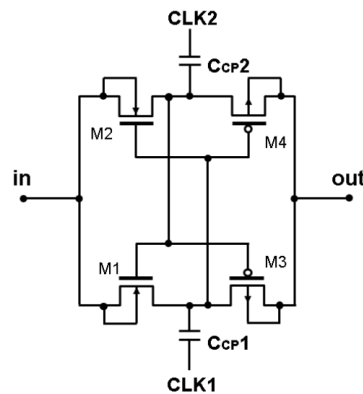
Figure 1.3: Topology of conventional CCCP
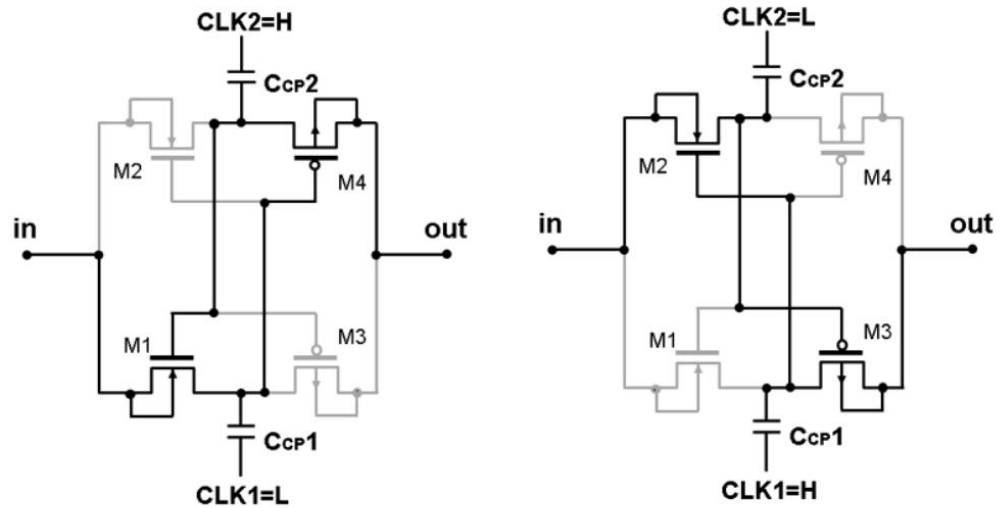
Figure 1.4: Operation of conventional CCCP

1.6 Oscillator

In order to operate the charge pump, an oscillator is required to furnish the signal that controls the switches within the charge pump. An oscillator is a circuit that produces a recurring, alternating and continuous waveform without requiring external input. Basically, oscillators convert a DC source into an alternating waveform at the desired frequency based on their specific circuit components. Oscillators can be categorized into two primary types: harmonic oscillators and relaxation oscillators (Graf, 1997).

In a harmonic oscillator, energy flows consistently from the active components to the passive components and the oscillation frequency is dictated by the feedback path. On the other hand, in a relaxation oscillator, energy is exchanged between the active and passive components and the oscillation frequency is determined by the charging and discharging time-constants within the system.

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Furthermore, harmonic oscillators yield low-distorted sine-wave outputs, whereas relaxation oscillators produce non-sinusoidal waveforms such as saw-tooth, triangular, or square shapes.

Non-Overlapping Clock (NOC) generator is a key building block of switched capacitor circuits. Standard NOC circuits use simple inverters to realize delays. For high to moderate frequencies, the number of inverters required is nominal (Mal and Todani, 2011). Ring oscillators (RO) are suitable for NOC generations due its small size, high integration, operate at low voltage, wide oscillation range (Nauneet Kumar, Bhagwat, Ramji and Bharti, 2019). A ring oscillator is a circuit consisting of an odd number of NOT gates, where the output toggles between two distinct voltage levels, representing logic 1 and logic 0. These NOT gates or inverters are connected in a series, with the output of the last inverter being fed back into the input of the first inverter as shown in Figure 1.5. Therefore, this project will emphasize on CCCP with ring oscillator.
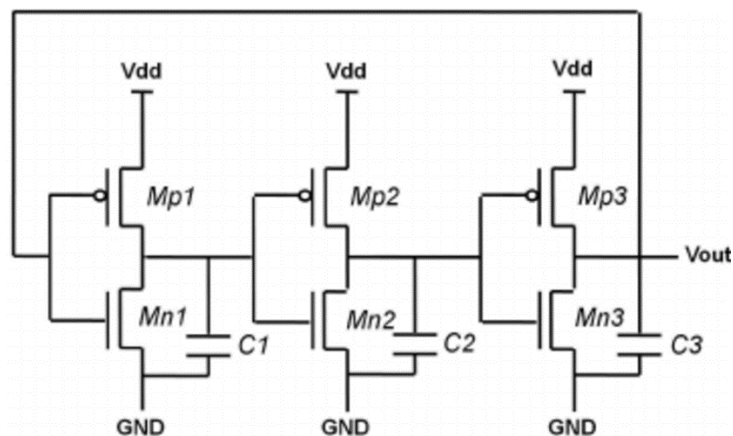
Figure 1.5: Topology of 3-stages-CMOS ring oscillator

1.7 Problem Statement

One of the main challenges with DC-DC converters is achieving high power efficiency. It could be affected by multiple factors including circuit topology, choice of components and switching frequency. For example, if the switching frequency of the oscillator is too low, the operation of the MOSFET can become slow and causing delays in the switching transition. The delay can lead to an increase in the power losses in the MOSFET, unwanted voltage spikes or overshoot. In contrast, if the switching frequency from the oscillator is too high, the MOSFET may not have enough time to toggle fully and result in significant switching losses which will contribute to the power dissipation.

Apart from switching frequency, the fast rise and fall times are crucial to minimize the operating time of MOSFET in the linear region, where it can dissipate significant power and cause heat build-up. This can be achieved by selecting a gate driver circuit with a fast rise and fall time or by using an external gate driver that can provide the necessary signal.

The duty cycle of the gate signal should be selected to ensure that the MOSFET is fully turned on and off during each switching cycle. The duty cycle can be adjusted to control the amount of power transferred to the load and to maintain stable operation of the circuit.

It is also important to ensure that the gate signal is free from noise and other unwanted signals, which can cause unintended switching and potentially damage the MOSFET or the surrounding circuitry. Therefore, proper signal conditioning and noise filtering techniques should be employed to ensure reliable and efficient operation of the MOSFET.

In this project, a high efficiency, wide-input-supply voltage-controlled ring oscillator for charge pump is proposed. The voltage-controlled ring oscillator should generate a waveform to drive the CCCP with following characteristics: minimal rise and fall time, balanced duty cycle and noise-free. The performance of proposed ring oscillator on CCCP will be investigated. On the other hand, the power efficiency of both ring oscillator and CCCP will be analysed and evaluated.

1.8 Objectives

1. To investigate and analyse oscillators and cross-coupled charge pump for wide-input supply applications

2. Design and develop oscillator for the high efficiency charge pump

3. Develop testbench to simulate and verify the performances of the proposed design

4. Improve the power efficiency of the oscillator and charge pump

CHAPTER 2

LITERATURE REVIEW

A comprehensive literature review is presented in this chapter to discuss about the researches which are relevant to cross-coupled charge pump (CCCP) and ring oscillator (RO). The performance of CCCP and RO in different applications are investigated.

A dynamic voltage frequency scaling technique (DVFS) tailored for a complementary metal-oxide-semiconductor (CMOS) differential bootstrapped ring voltage-controlled oscillator (DBRO), designed specifically for energy harvesting (EH) applications was proposed by Pakkirisami Churchill et al. (2022). The 3-stage cross-coupled charge pump within the DBRO was implemented with a split input-supply circuit, accommodating a signal with an input range of 0.15–0.5V and loads of 100 k–1 MX, incrementally varied by 100 k and 2MX respectively. By employing this technique, the DVFS-DBRO operated at an optimal frequency with reduced power consumption, significantly enhancing the power conversion efficiency (PCE) and establishing a broad energy harvesting range. Notably, the circuit achieved a PCE of 44.73% with a 0.15 V input voltage when driving a 2 MX load. Furthermore, DVFS facilitated a twofold clock boosting of the input voltage without the voltage scaling effect, leading to improved charge-pump conduction at low input voltage and allowing a gate-to-source input voltage of 0.5V. These characteristics contribute to the

robustness of the proposed technique and demonstrate its considerable potential for a wide range of energy harvesting applications.

Yong et al. (2022) proposed a 3-stage dual branch charge pump (CP) with an advanced dynamic gate-biasing technique (DGB) enabling ultra-low-voltage (0.1V) energy harvesting as shown in Figure 2.1. The combination of an advanced DGB and an NMOS-PMOS (n-type metal–oxide–semiconductor - p-type metal–oxide–semiconductor) dual-switch transistor pair reduced the forward conduction loss and the reverse current leakage loss. The proposed design achieved a PCE of 10.5% to 43.4% over the input voltage range of 40mV to 100 mV.
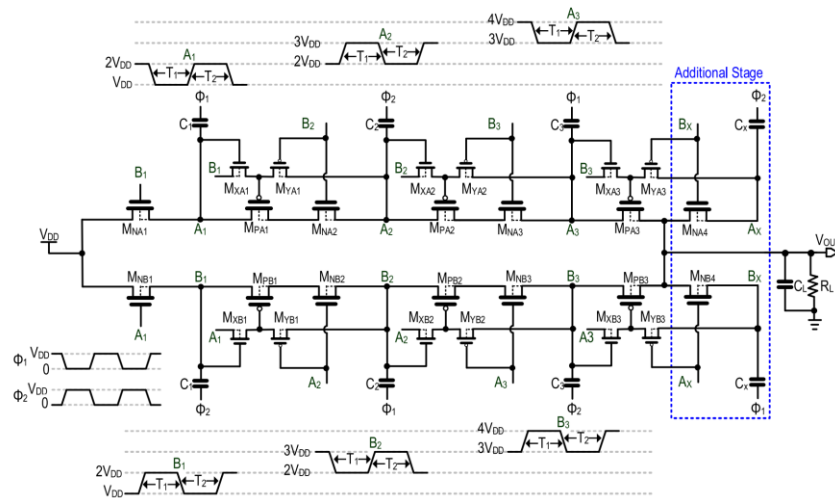
Figure 2.1: 3-stage CCCP topology with an advanced dynamic gate biasing

Sebe et al. (2021) introduced a self-bias NAND (SBNAND) gate as part of a non-overlapping clock (NOC) generator designed for highly efficient CMOS LSIs operating at extremely low voltages. The SBNAND gate was comprised of a primary NAND gate and a feedback inverter which effectively enhanced the output performance by regulating the body-bias voltages (VBS) of the main NAND gate. Experimental results from a prototype chip validated that the

proposed NOL clock generator, incorporating SBNANDs, successfully operated at an incredibly low VDD of 6mV.

Xu et al. (2020) introduced a novel approach to design high-speed ring oscillators (ROs) using n-type-only indium-zinc-oxide (IZO) thin-film transistor (TFT) technology. Their objective was to achieve higher oscillation frequencies, which they accomplished by incorporating a skewed delay (SD) scheme and bootstrap inverter into the proposed ROs. Additionally, they designed improved output buffers with enhanced driving capability. For comparison, they fabricated both the proposed seven-stage SD ROs and conventional bootstrap ROs on the same glass substrate. Notably, the SD ROs exhibited significant improvements in oscillation frequencies, with increases of over 45% and 25% for −tpd and 0 SD, respectively, across a supply voltage range of 6V to 20V. Furthermore, the measured output swings of the newly designed boost buffers showed notable enhancements of more than 50% at input frequencies higher than megahertz.

Tiwari et al. (2020) proposed a high-speed ring oscillator (RO) employing amorphous Indium-Gallium-Zinc-Oxide Thin-film transistors (a-IGZO TFTs). The innovation in the proposed RO lies in its ability to reduce the delay of a single-stage inverter by utilizing intermediate signals generated within the RO, resulting in significant speed improvement. They fabricated two conventional ROs, one with a diode-load inverter and the other with a bootstrapped pseudo-CMOS inverter, alongside the proposed RO, all at a temperature not exceeding 180°C. Experimental results revealed that the proposed RO achieved a frequency of 173.2kHz and a power-delay-product (PDP) of 0.7nJ at a supply voltage of 6V. When compared to ROs based on diode-load inverter and bootstrapped pseudo-CMOS inverter, the proposed RO exhibited impressive enhancements,

with a 155% increase in frequency and a 14% decrease in PDP, respectively. Consequently, these findings demonstrate the suitability of the proposed RO for applications in low-voltage and high-speed designs, particularly for efficient timing signal generation.

A radiation-tolerant digitally controlled complementary CMOS ring oscillator design suitable for all-digital phase-locked loop (ADPLL) implementations is proposed (Tlelo-Cuautle, Castañeda-Aviña, Trejo-Guerra and Carbajal-Gómez, 2019). The oscillator circuit is experimentally characterized using a 65-nm technology and demonstrating remarkable improvements in sensitivity reduction up to a linear energy transfer (LET) of 63.5 MeV mg−1 cm^2. It remains free from harmonic oscillation errors even under irradiation and proves resilient against a total radiation dose exceeding 1.5 Grad. Operating at the design frequency of 1.28GHz, the oscillator consumes a power of 7mW, while achieving a phase noise of −105dBc/Hz at a 1 MHz offset, corresponding to an impressive figure of merit (FOM) of 159dB.

Jiang, Yin, Mak, and Martins (2019) proposed an ultra-low-voltage 8-phase bootstrap (BT) ring-voltage-controlled oscillator (RVCO) with an impressive figure of merit, reaching up to 165.2dBc/Hz. The block diagram of the proposed BT RVCO is depicted in Figure 2.2. This RVCO took advantage of the inherent non-overlapping clocks provided by pseudo-differential BT inverters, which effectively reduced charge loss caused by asynchronous charge-pump operation and minimized phase sensitivity to transistor noise. As a result, the proposed RVCO achieved higher oscillation frequency and output swing while simultaneously reducing phase noise. Fabricated in 6-nm CMOS technology, the BT RVCO exhibited a phase noise ranging from -93.7dBc/Hz to -92.6dBc/Hz at

a 1MHz offset across frequencies of 0.4GHz to 1.6GHz. Additionally, the power

dissipation ranged from 47.4 µW to 280µW at 0.5V.
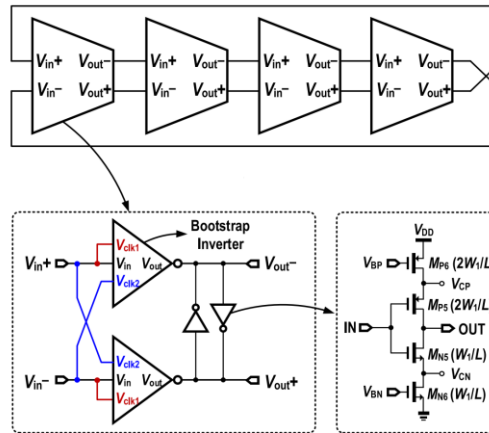
Figure 2.2: Block diagram of 8-phase BT RVCO core using non-overlapping clocks

A high efficiency fully integrated high-voltage (HV) pulse driver in standard

CMOS was proposed by Wu et al. (2019). The system design involved the

utilization of an optimized 4-stage cross-coupled switched-capacitor voltage

multiplier (SCVM) alongside an on-chip HV output driver. This combination

allowed the generation of HV pulses exceeding 10V, all powered by a standard

I/O DC voltage of 2.5V. The area efficient HV output driver stage could reach

up to 12% total active area reduction while maintaining the low static power

characteristics. A synchronous charge compensation (SQC) technique was

presented to alleviate the loading-dependent signal distortion through reducing

the HV rail voltage droop and improving the HV pulse settling time during the

driver output transitions. Fabricated in 65-nm bulk CMOS, the chip prototype

generated HV pulses from 250 kHz to 1 MHz with a 15pF load while ensuring

no device breakdown. Measurement results demonstrate a peak SCVM PCE of

50% and an overall driving efficiency of 12.25%. The chip prototype attains approximately 2 times faster output pulse transition speed compared with the state-of-the-art.

A 0.4V 65nm CMOS relaxation oscillator with bootstrapped logic gates and outputs was developed (Lei, Mak and Martins, 2018). The utilization of bootstrapped logic gates allowed for an output swing of 1.15V which effectively overcoming the challenges posed by ultra-low-voltage (ULV) digital circuits without requiring an additional voltage source. Additionally, a ULV comparator with bulk-driven inputs exhibited an 18dB gain with 3 cascaded stages. The relaxation oscillator was operating at 3.3MHz and equipped with built-in calibration. It demonstrated remarkable stability with frequency deviations of $\pm0.71\%$ and $\pm0.57\%$ against temperature (-30 to 100°C) and voltage (0.36 to 0.44V) variations respectively based on Monte-Carlo simulations (N=30). This excellent performance was attributed to the incorporation of a background delay-time cancellation scheme. The simulation results indicated a power consumption of 6.4µW, resulting in an energy efficiency of 1.9pJ per cycle.

Yoshida and Miyaji (2018) proposed a two-stage start-up CMOS gate boosting voltage doubler charge pump circuit designed for extremely low input voltages as illustrated in Figure 2.3. In this circuit, an inverter level shifter was utilized to generate a 2Vin voltage swing which was applied to the gates of the main NMOS and PMOS power transistors within the charge pump. This approach effectively reduced channel resistance. Measurement results revealed that the proposed circuit achieved a minimum input voltage of 190mV, resulting in a remarkable 181% increase in output power compared to the conventional forward-body-bias scheme at a 300mV input voltage. At an input voltage of 390mV and an output

current of 320nA, the proposed scheme demonstrated a peak efficiency of 59.2%. Due to its capabilities in operating below threshold voltage, the proposed circuit is particularly suitable as a start-up circuit in ultralow power energy harvesting power management applications.
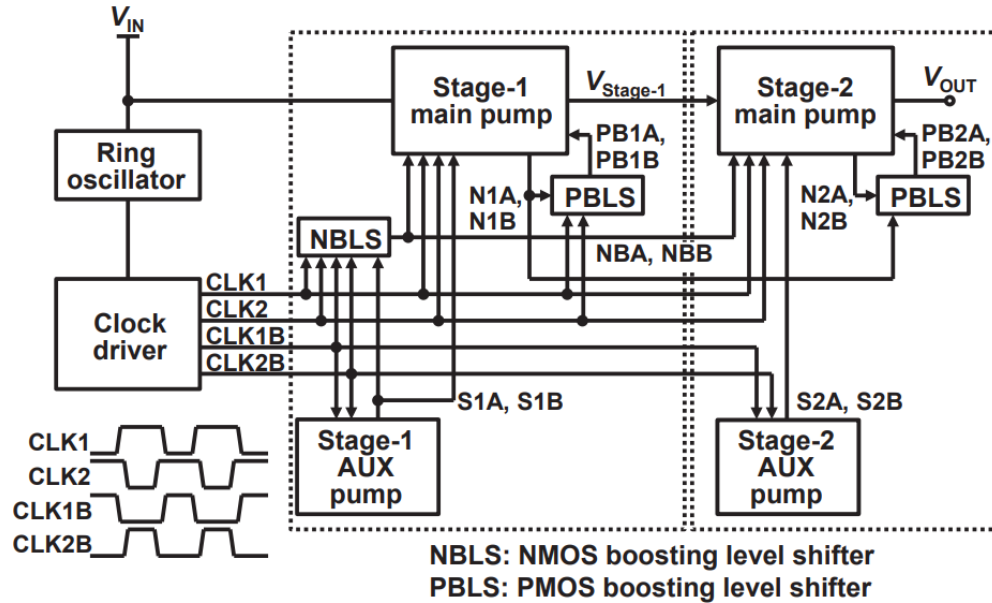
Figure 2.3: Architectural block diagram of the proposed circuit

Referring to Table 2.1, the design of a ring oscillator using CMOS technology is capable to provide oscillating signals with high frequency while consuming low power. It is suitable to be incorporated with CCCP to achieve high PCE and remarkable efficiency. Taking into account both power efficiency and manufacturing cost consideration for RO and CCCP, 180nm CMOS technology emerges as the optimal choice for this project. This technology not only offer cost advantages over the 65nm and 130nm CMOS technology, yet it also guarantees the desired performance levels for the design.

Table 2.1: Summary of review on CCCP and RO

CCCP / RO	Performance
DVFS-DBRO for 3-stasge CCCP (Pakkirisami Churchill et al., 2022)	44.73% of PCE with 0.15V input voltage when driving a 2MX load
3-stage dual branch CP with DGB on NMOS-PMOS dual-switch transistor pair (Yong et al., 2022)	PCE of 10.5% to 43.4% over the input voltage of 40mV to 100mV
SBNAND fate in NOL clock generator for extremely low-voltage CMOS LSIs (Sebe et al., 2021)	It can operate at extremely low VDD of 60mV
Highspeed RO in n-type-only IZO TFT technology (Xu et al., 2020)	Oscillation frequencies were improved by 45% and 25% within the supply ranged from 6V up to 20V
RO with a-IGZO TFTs (Tiwari et al., 2020)	Frequency was improved by 155% at a supply voltage of 6V
Radiation-tolerant digitally controlled complementary CMOS RO design for ADPLL (Tlelo-Cuautle, Castañeda-Aviña, Trejo-Guerra and Carbajal-Gómez, 2019)	The oscillator dissipates 7mW of power while achieving a phase noise of -105dBc/Hz at 1MHz offset
Ultra-low-voltage 8-phase BT RVCO (Jiang, Yin, Mak and Martins,2019)	The BT RVCO measured a phase noise of -93.7 dBc/Hz to -92.6dBc/Hz at a 1MHz offset from 0.4GHz to

	1.6GHz, while dissipating 47.4 µW to 280µW at 0.5 V
Fully integrated HV pulse driver for SCVM (Wu et al., 2019)	The SCVM has PCE of 50% and overall driving efficiency of 12.25%
CMOS relaxation oscillator with bootstrapped logic gates and outputs (Lei, Mak and Martins, 2018)	The power consumption is 6.4µW, resulting in an energy efficiency of 1.9pJ per cycle
Two-stage start-up CMOS gate boosting voltage doubler charge pump circuit (Yoshida and Miyaji, 2018)	It can achieve a maximum efficiency of 59.2% when the input voltage is 390mV and the output current is 320nA

CHAPTER 3

METHODS

3.1 Background theory

This section will briefly discuss on the history, basic structure and operation of a ring oscillator (RO). To enhance the capabilities of a conventional RO, voltage control circuitry is incorporated to create a voltage-controlled ring oscillator (VCRO).

3.1.1 History of Ring Oscillator

Ring oscillator is one of the most popular control circuits due to its compact size, broad tuning range and multiple phase outputs. The idea of using gain stages in a ring configuration dates back to the vacuum-tube era. In 1953, Gally presented a structure consists of nine triodes to form an oscillating loop as shown in Figure 3.1 (Razavi, 2019). The grid (G), cathode (C) and anode (A) are equivalent to the gate, source and drain of a metal-oxide-semiconductor field-effect transistor (MOSFET).
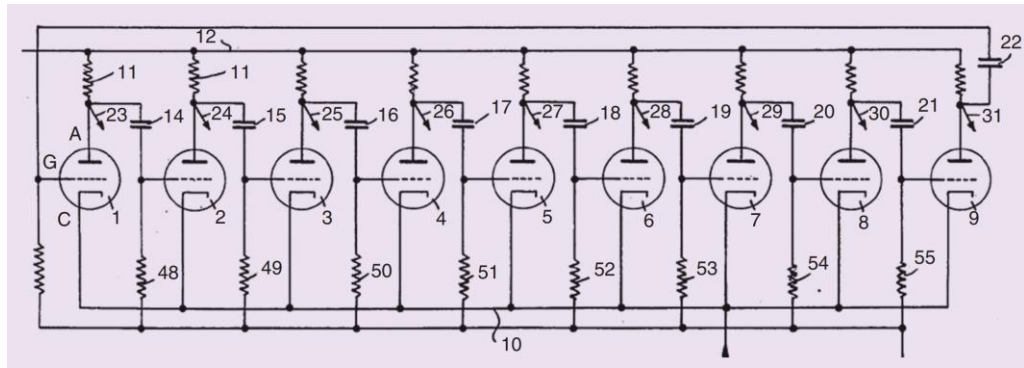
Figure 3.1: Ring oscillator described by Gallay

3.1.2 Basic Structure and Operation of Ring Oscillator

A ring oscillator consists of an odd number of inverters which connected in series with positive feedback. The output will oscillate between two voltage levels either one or zero. The inverter can be represented by NOT gate. A 3-stage ring oscillator as shown in Figure 3.2 is the most fundamental structure to make sure the oscillation and gain of the system are sufficient and Barkhausen criteria is fulfilled.

The ring oscillator operates based on the principle of logical instability. Assuming that X is high state whereas ~X is low state. It is observed that the input is inverted by the first NOT gate and the process is repeated by second and third NOT gates. As a result, the output will keep toggling between high state and low state because of the feedback connection.
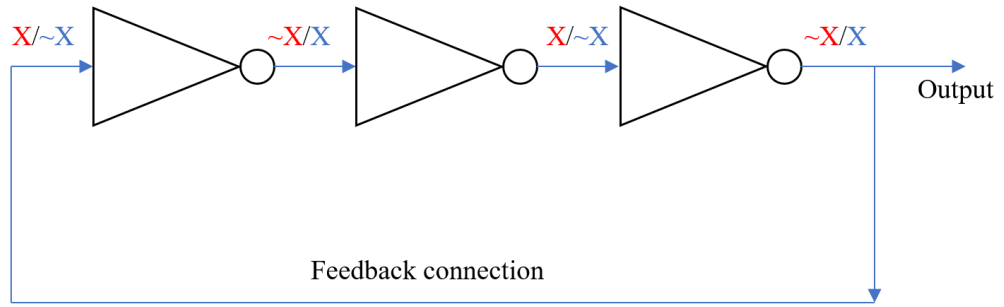
Figure 3.2: 3-stage ring oscillator

Ring oscillator could be extended to 5-stage, 7-stage and so on as long as the stage number (n) is an odd number. The number of inverter stages will affect the oscillating frequency of the output. The reason is each inverter contributes delay to input signal thus if there is an increase in the number of inverters, the oscillating frequency will be reduced.

The frequency of oscillation can be calculated using Equation (3.1):

$$f = \frac{1}{2n\tau} \qquad\qquad (3.1)$$

where τ = time delay for single inverter

n = number of inverters in the oscillator

3.1.3 Voltage-Controlled Ring Oscillator (VCRO)

By integrating voltage control circuitry into a ring oscillator, oscillation frequency could be tuned over a wide range to achieve the requirement of a specific system by adjusting the control voltage in VCRO. Equation (3.2) shows the output frequency for ideal VCRO:

$$f_{out} = f_o + KV_{ctrl} \qquad (3.2)$$

where f_o is free running frequency

K is the sensitivity of the VCRO

V_{ctrl} is the control voltage
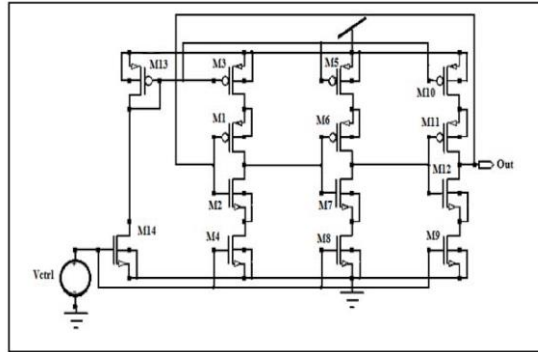
Figure 3.3: Schematic diagram of current starved ring VCO

Figure 3.3 shows the schematic diagram of an existing current starved ring voltage-controlled oscillator (VCO). Six transistors are responsible for generating the oscillating signal, while the remaining transistors function as a current source that regulating the current flow to the inverters as illustrated in Table 3.1. The amount of V_{ctrl} will determine the oscillation frequency of the VCO.

Table 3.1: Functionality of transistor in current starved ring VCO

Transistors	Functionality
M1 & M2 M6 & M7 M11 & M12	Inverters
M3, M4, M5, M8, M9, M10, M13, M14	Current source

The delay of each stage, τ is shown in the Equation (3.3):

$$\tau = \frac{V_{osc}C_G}{I_{ctrl}}$$

(3.3)

where C_G is the parasitic capacitance

V_{osc} is the oscillation amplitude

I_{ctrl} is the control current

Equation (3.3) is subsequently manipulated to derive the frequency equation for the current-starved voltage-controlled oscillator (VCO) in relation to the control current. Based on Equation (3.4), control voltage is directly proportional to oscillation frequency thus the frequency can be tuned accordingly.
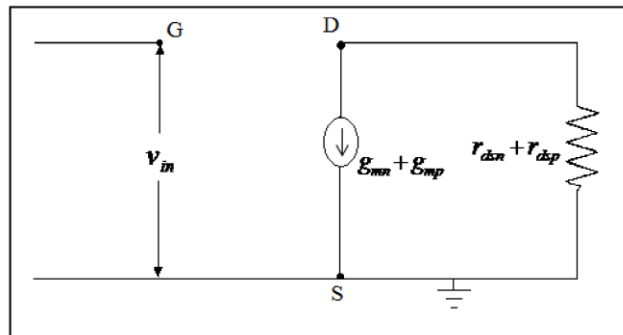
$$f_{osc} = \frac{I_{ctrl}}{2NV_{osc}C_G}$$

(3.4)

Figure 3.4: Small signal model inverter

Referring to Figure 3.4, the gain of an inverter can be expressed as Equation (3.5):

$$A = g_m r_{ds}$$

(3.5)

where g_m is the transconductance of the device

r_{ds} is the drain-source resistance

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In this project, an additional nMOS (n-type metal–oxide–semiconductor) transistor is employed and incorporated between each inverter as depicted in Figure 3.5.
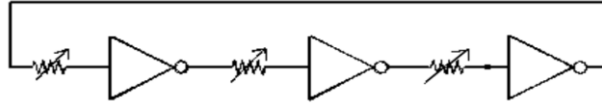
Figure 3.5: VCRO with variable resistor

As these nMOS transistor act as switches, they can be substituted with a resistance value of $1/g_m$. Assuming that both nMOS and pMOS (p-type metal–oxide–semiconductor) transistors are having the C_G which is equivalent to the g_m, the delay of each inverter stage can be determined using Equation (3.6).

$$\tau = \frac{C_G(1+G_m R_V)}{G_m} \tag{3.6}$$

The delay approximation of inverter is illustrated in Figure 3.6.

Figure 3.6: Delay approximation of inverter

Equation (3.7) is derived to relate the oscillation frequency in terms of variable resistance.

$$f_{osc} = \frac{G_m}{2NC_G(1+G_m R_V)} \tag{3.7}$$

The frequency at which the VCRO oscillates is based on the g_m, C_g and variable resistance, R_V. Both g_m and C_g are considered as device parameters and assumed to be fixed. In short, the wide frequency range of the VCRO can be manipulated by controlling the resistance.
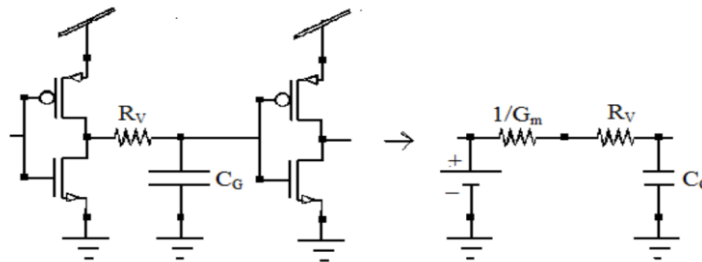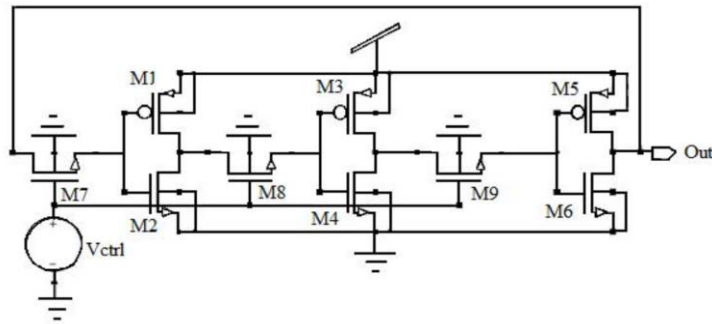

Figure 3.7: Proposed three stages VCRO

The proposed three stages VCRO is shown in the Figure 3.7. Three inverters are cascaded to form a 3-stage ring oscillator. An extra nMOS is added in between each inverter to further enhance the VCRO performance. Those nMOS are connected to control voltage source to manipulate the oscillating frequency of the circuit.

Prior to the first delay stage, transistor M7 functions as a voltage-controlled switch to control the amount of voltage to drive the gate of the inverter. M7 is biased into conduction region when V_{ctrl} is high. At this moment, the switch is closed and the resistance of the nMOS (M7) becomes significantly low. The smaller the resistance, the shorter the delay within the circuit which escalates the VCRO frequency.

On the other hand, if V_{ctrl} is low, transistor M7 enters the cut-off region, resulting in a lower output frequency. As a result, it becomes essential for the resistance to adapt based on the control voltage. The transition time (rise and fall time) of

an inverter is affected by the capacitor's charging and discharging process. Additionally, the charging and discharging current relies on the carrier mobility which is higher for nMOS transistors than pMOS transistors and this will lead to an increase in the drain current.

3.2 General Plan of The Experimental Work

This project emphasizes on the design of VCRO and cross-coupled charge pump (CCCP) via Cadence Virtuoso Software. Cadence Virtuoso is a well-known electronic design automation (EDA) software suite used by engineers to design and simulate electronic circuits. It provides Virtuoso simulation that allows designers to verify their designs and check the functionalities prior to fabrication. The implementation of the simulation work will be discussed in this section.

3.2.1 Project Flow Chart

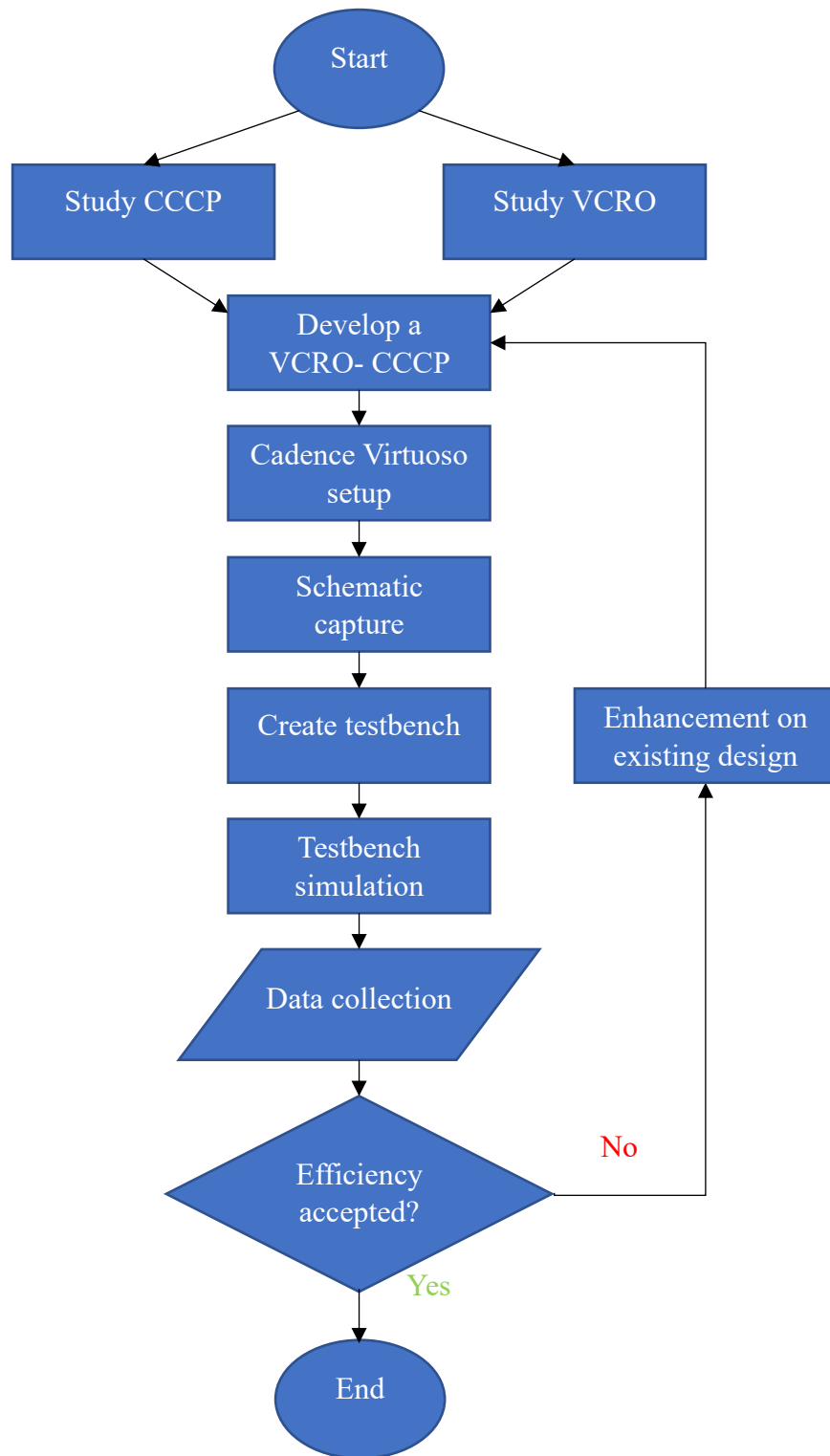The flow chart of the project development is depicted in the figure below.

Figure 3.8: Flow chart of project development

3.2.2 Schematic capture

A schematic is defined as a diagram that depicts the circuit in a simple way by using abstract and graphic symbols instead of realistic pictures. Schematic capture is the process of creating a graphical representation of electronic circuit to show comprehending and spreading information rather than doing physical operation. Hence, schematic diagram only shows the significant components of the circuit yet some details in the diagram may be exaggerated to facilitate the understanding of the system.

In schematic capture, the electronic components are represented using standardized symbols. These symbols are available in the existing libraries and can be easily accessed for schematic drawing. User can also create self-defined symbol to achieve specific requirements.

For instance, an inverter is developed using Complementary metal–oxide–semiconductor (CMOS) which consists of one nMOS and pMOS. The structure is then duplicated and cascaded to build a fundamental 3-stage RO. A RO symbol is created based on the schematic and added to the existing library.

3.2.3 Create a Testbench

Create a new schematic cell for testbench circuit. A CCCP will be developed and VCRO is imported from the library. The CCCP will be driven by the VCRO to generate output voltage. In addition, input sources and other components such as capacitor and resistor will be added to complete the circuitry for verification and testing jobs. All parameters for the testbench circuit are defined.

3.2.4 Setup Simulation Environment

Define the simulation types, such as transient analysis or DC sweep analysis. Setup the initial condition to prevent unforeseen input to be fed to the circuit which affects the functionality of the circuit. Furthermore, select the waveforms to be plotted for data interpretation and run the simulation.

3.3 VCRO-CCCP Circuit Design

To ensure the optimal performance of the VCRO-CCCP circuit, there are a few design aspects must be taken into consideration.

3.3.1 Sizing of Inverter MOSFET

The most fundamental component of a VCRO is a MOSFET. The sizes of MOSFETs have to be in correct ratio to ensure the symmetrical switching characteristics. When both nMOS and pMOS work together optimally, the rise time and fall time of the output signal should be balanced to minimize time delays and avoid signal distortions. The size ratio also affects the drive strength of the nMOS and pMOS transistors. A larger transistor size (wider channel width) generally results in higher drive current capabilities.

Moreover, the size ratio influences other important characteristics such as power consumption, power dissipation, and overall circuit speed. By selecting the appropriate size ratio, the VCRO can be optimized to meet the specific requirements of the circuit design.
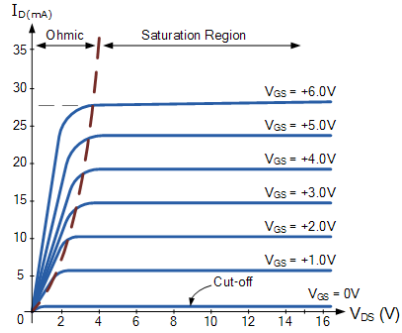
Figure 3.9: MOS transistor current response over a wide range of gate voltage

Figure 3.9 depicts the MOS transistor current response over a wide range of gate voltage. In saturation mode, the current equations of nMOS and pMOS are shown in Equation (3.8) and Equation (3.9).

$$I_{Dn} = \frac{1}{2}\mu_n C_{ox} \frac{W_n}{L_n} (V_{GS} - V_{TH})^2 \qquad (3.8)$$

$$I_{Dp} = \frac{1}{2}\mu_p C_{ox} \frac{W_p}{L_p} (V_{SG} - |V_{TH}|)^2 \qquad (3.9)$$

where μ = carrier mobility

C_{ox} = oxide capacitance per unit area

W = width of finger

L = length of finger

V_{GS} = gate-to-source voltage

V_{SG} = source-to-gate voltage

V_{TH} = threshold voltage

Assuming that C_{ox} and voltages are the same for both nMOS and pMOS, therefore I_{Dn} is equal to I_{Dp}. Equation (3.10) is then derived from Equation (3.8) and (3.9).

$$\mu_n \frac{W_n}{L_n} = \mu_p \frac{W_p}{L_p} \tag{3.10}$$

A notable distinction between pMOS and nMOS is their carrier mobility. In pMOS, the majority carriers are holes, which exhibit lower mobility than the electrons that serve as majority carriers in nMOS. As a result, pMOS generally demonstrates slower switching speed when compared to nMOS. The values of μ_n and μ_p are 1241.8cm^2/Vs and 406.9 cm^2/Vs respectively (Arora et al., 1982). The mobility of electron is approximately three times greater than that of hole. By substituting the value of carrier mobility into Equation (3.10), the size ratio of pMOS and nMOS is shown in Equation (3.11).

$$\frac{W_p}{L_p} \approx 3 \frac{W_n}{L_n} \tag{3.11}$$

3.3.2 Sizing of nMOS for Variable Resistor

The subsequent factor to be considered in the design is the size of the nMOS located between the inverters which operates as variable resistor. Referring to Equation (3.8) and Equation (3.9), it can be observed that the drive current is directly proportional to the width-to-length ratio of the transistor. As a result, adjusting either the width or the length of the nMOS transistor allows for control over the drive current. Ohm's law states that:

$$V = IR \tag{3.12}$$

where V = voltage

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I = current

R = resistance

When the control voltage is fixed at specific level, an increase in the drive current results in a decrease in resistance. Thus, by enlarging the width of the transistor fingers, the resistance of the MOS can be effectively reduced.

3.3.3 Tapering Effect

The tapered buffer structure was first proposed by Linholm (1975). The design of the tapered buffer involves a sequence of inverter stages, where the width of each MOS transistor in a stage is progressively enlarged by a constant factor which is also known as tapering factor compared to the transistors in the preceding stage. The consistent widening of the transistors sin each stage ensures a constant ratio between the output current and output capacitance. As a result, the rise time, fall time and delay time for every stage is uniform. Driving buffers have been extensively studied, and its optimum tapering factor is 2.72 (Jaeger & Linholm, 1975).

3.3.4 Body Effect

Figure 3.10 shows a nMOS transistor without and with body effect while Figure 3,11 illustrates the same transistor with body effect. Suppose V_S and V_D are equal to 0, V_G is an integer but less than threshold voltage, V_{TH}. In this situation, depletion region is formed under the gate but inversion channel does not exist.
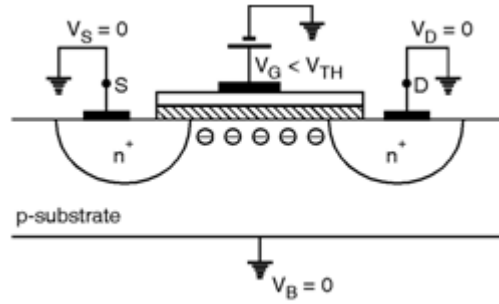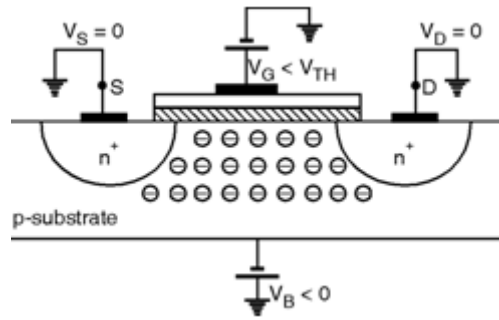
Figure 3.10: nMOS transistor without body effect

Figure 3.11: nMOS transistor with body effect

When V_B is a negative value, more holes are drawn towards the substrate connection resulting in an accumulation of large amount of negatively charged ions. Therefore, the depletion region widens as shown in Figure 3.11. Given that the threshold voltage V_{TH} is dependent on the total charge within the depletion region, a decrease in the V_B leads to an increase in the depletion charge and so the V_{TH}. This phenomenon referred to body effect.

The relation between V_{TH} and V_{SB} is depicted in the Equation (3.13). To eliminate the body effect, bulk terminal is connected to the ground resulting in the minimum threshold voltage for nMOS transistor.

$$V_{TH} = V_{TH0} + 0.5(\sqrt{2\varphi_B + V_{SB}} - \sqrt{2\varphi_B}) \qquad (3.13)$$

where φ_B = substrate doping

V_{SB} = bulk to source voltage

3.3.5 Smoothing capacitor and Buffer

A capacitor will be added at the output of VCRO to enhance the signal stability and transient response. The stored energy in capacitor is supplied to the circuit when input goes below the peak value. Consequently, the output signal is smoother.

In addition, two inverters are connected in series to serve as a buffer. While each inverter cancels out the inversion, the buffer amplifies the signal and boosts the current-carrying capacity, enabling it to drive a load effectively.

3.4 Schematic and Testbench Capture

Schematic diagrams that representing the VCRO, CCCP, and inverters have been created, along with corresponding symbols derived from the schematic as shown in Figure 3.12 to Figure 3.17. These components will be integrated into a testbench to facilitate the simulation of a VCRO-CCCP circuit as depicted in Figure 3.18. By running simulations on the testbench, the behaviour and characteristics of the VCRO-CCCP system can be assessed, enabling further analysis and optimization of its performance.
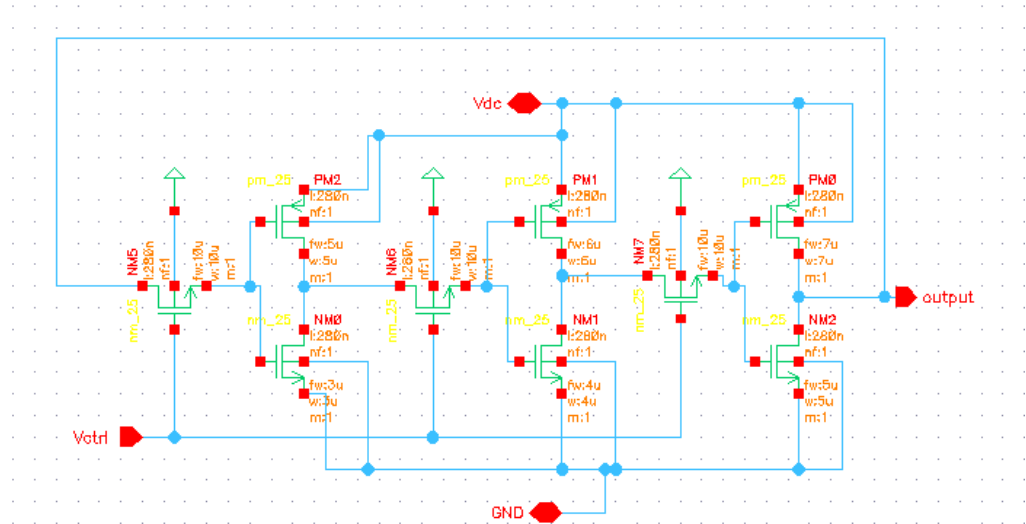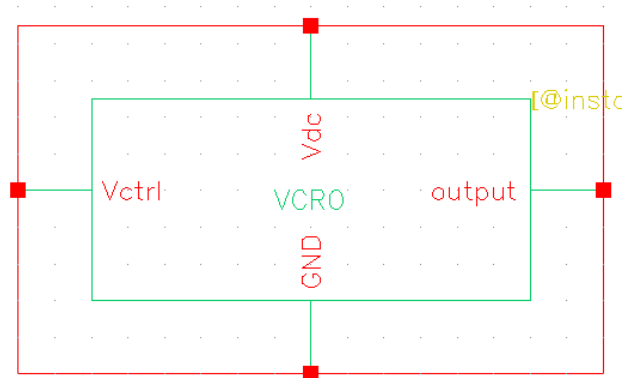
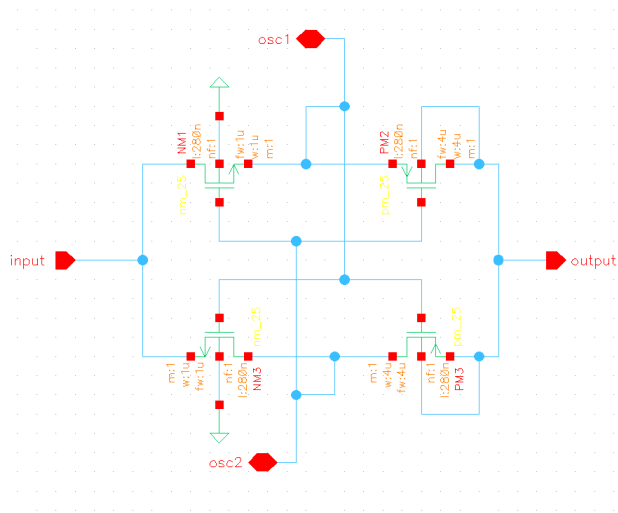**Figure 3.12: Schematic diagram of VCRO**

Figure 3.13: Symbol of VCRO

Figure 3.14: Schematic diagram of CCCP
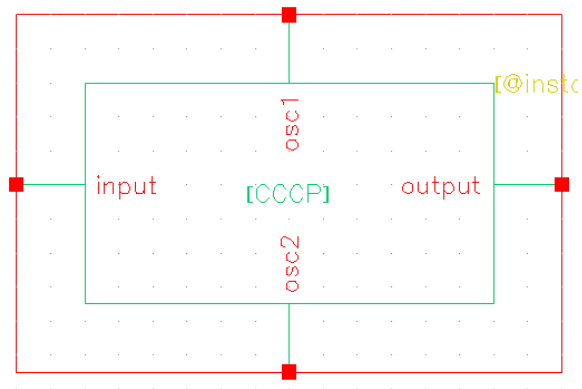
Figure 3.15: Symbol of VCRO
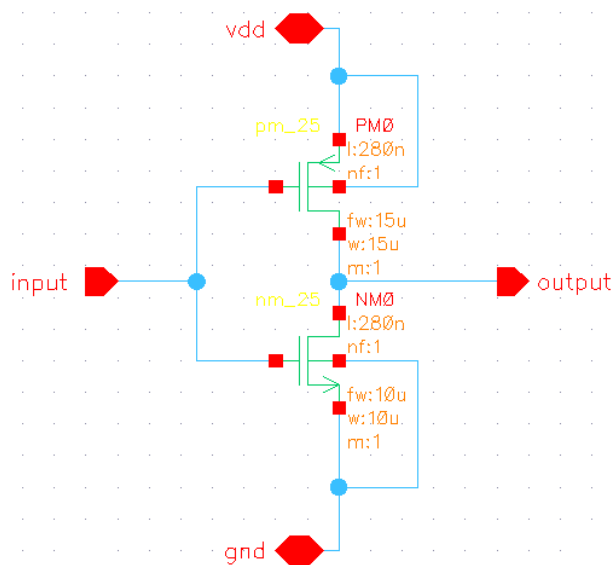
Figure 3.16: Schematic diagram of Inverter
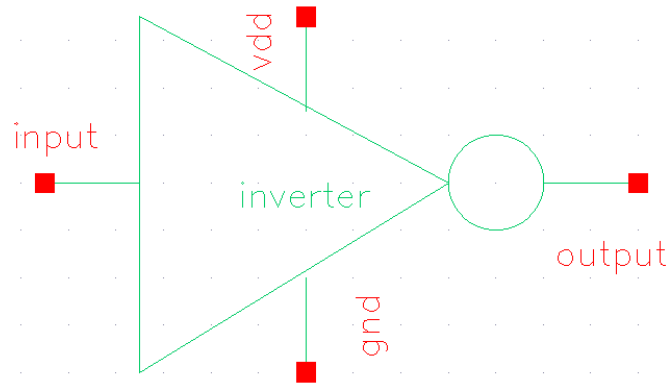
Figure 3.17: Symbol of Inverter
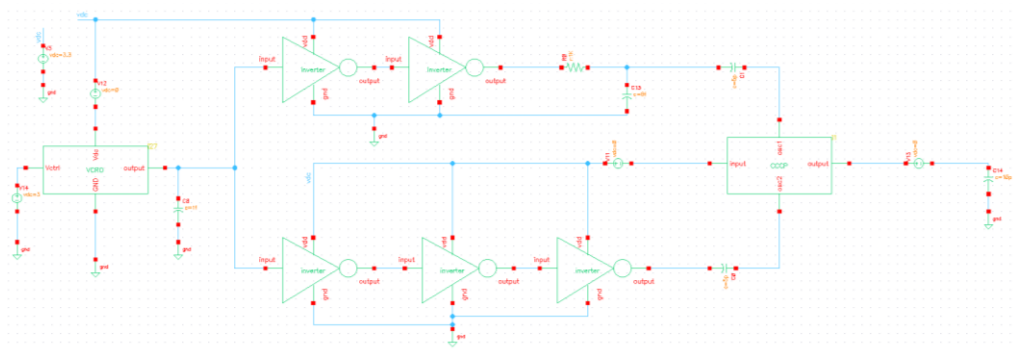
Figure 3.18: Testbench of VCRO-CCCP

3.5 Analytical Procedure

The waveform is collected from the simulation and the data is organized and evaluated based on the initial expectation. The results will be compared with previous research. Any potential issues are identified and the circuit design is optimized and refined accordingly. This process is repeated until the desired results are obtained. The performance of the VCRO is examined based on power consumption while the performance of the CCCP is evaluated based on power efficiency and voltage conversion efficiency (VCE).

3.5.1 Power Consumption of VCRO

The primary focus for the VCRO is minimizing power consumption since it utilizes power to generate signals. Equation (3.14) is used to calculate power consumption.

$$P_{consumption} = V_{in}I_{in} \tag{3.14}$$

where V_{in} is input voltage

   I_{in} is input current

3.5.2 Power efficiency of CCCP

Efficiency is a measure of how effectively a system or device converts input power to the desired output power. It is expressed as a percentage and can be calculated using Equation (3.15).

$$Efficiency\ (\%) = \frac{P_{out}}{P_{in}}\ x\ 100\% \tag{3.15}$$

where P_{out} is the output power delivered by the system

   P_{in} is the input power to the system

3.5.3 VCE of CCCP

VCE is a measure of how efficiently a voltage conversion system or device converts input voltage to output voltage. Equation (3.16) indicates the effectiveness of the conversion process and is typically expressed as a percentage.

$$VCE\ (\%) = \frac{V_{out}}{V_{ideal}}\ x\ 100\% \tag{3.16}$$

where V_{out} is the output voltage of CCCP

   V_{ideal} is the ideal output voltage of CCCP

CHAPTER 4

RESULTS

In this chapter, the data collected from the simulation was tabulated to observe the performance of both voltage-controlled ring oscillator (VCRO) and cross-coupled charge pump (CCCP). Additionally, graphs were plotted to provide visual aids to facilitate the evaluation of the performances of VCRO and CCCP.

4.1 Performance of VCRO

The main concerns for a VCRO revolve around two key factors: the frequency of the output signal and the power consumption to sustain a stable oscillation. Both of these aspects are directly influenced by the control voltage, V_{ctrl}. By adjusting the V_{ctrl}, the waveform of the output signal can be tuned to the desired shape that best suits the CCCP.

4.1.1 Effect of V_{ctrl} on Frequency and Power Consumption

In this work, a supply voltage of 3.3V was employed to operate the entire circuit. The V_{ctrl} was adjusted within a range of 1.5V to 3.3V to evaluate the performance at both minimum and maximum V_{TH} levels. The frequency of the oscillating signal produced by VCRO, as well as the power consumption, are tabulated in Table 4.1. The data are graphically represented in Figure 4.1 and Figure 4.2.

Table 4.1: Simulation results for proposed VCRO

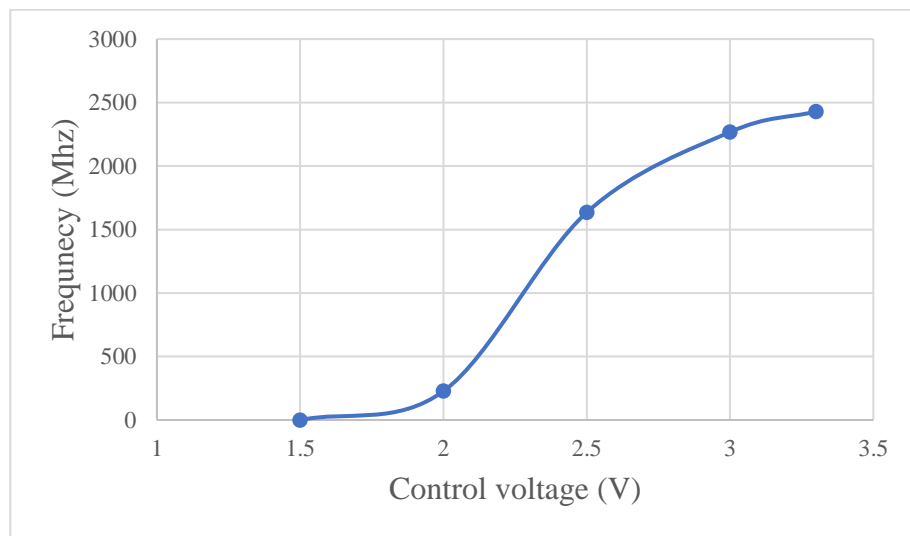| Control voltage, V_{ctrl} (V)	Frequency (MHz)	Power consumption (mW)
1.5	-	0.0004
2.0	227.10	2.87
2.5	1634.92	3.66
3.0	2267.63	6.61
3.3	2428.71	20.64

Figure 4.1: Graph of frequency versus control voltage
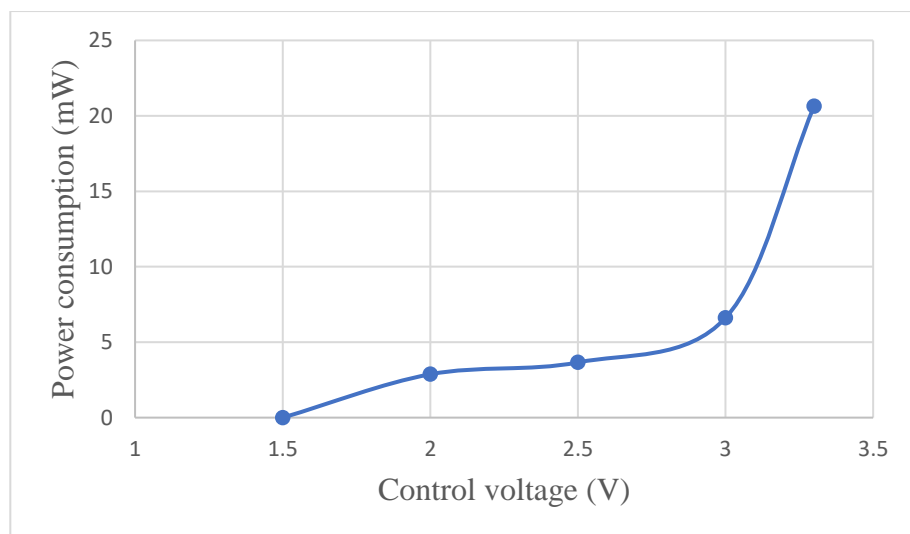

Figure 4.2: Graph of power consumption versus control voltage

According to the data presented in Table 4.1, the frequency of output signal was invalid when V_{ctrl} was set at 1.5V since it behaved like DC (direct current) signal. The output signal started to oscillate at 227.1MHz when V_{ctrl} was increased to 2V. Subsequently, the V_{ctrl} was incremented by 0.5V until it reached the maximum level of 3.3V.

It is observed that the frequency increased in correlation with V_{ctrl}, yet improvement in frequency varied across different V_{ctrl} increments. Notably, there was a remarkable surge in frequency when the V_{ctrl} was adjusted from 2V to 2.5V. As the V_{ctrl} was approaching the supply voltage, the enhancement in frequency became less significant. Ultimately, the maximum frequency achieved by the proposed VCRO for the oscillating signal was 2428.71 MHz.

On the other hand, the power consumption of the VCRO was minimal at V_{ctrl} of 1.5V. The power consumption experienced an upward trend from V_{ctrl} of 2V to 3V, with a slight decline at 3.3V.

4.1.2 Effect of V_{ctrl} on Output DC Voltage and Alternating Clock Signals

The oscillating signal was influenced by the value of V_{ctrl}. The output waveforms of the VCRO corresponding to different V_{ctrl} are illustrated in Figure 4.3 to Figure 4.7. From Figure 4.3, it could be observed that the output waveform was a DC signal. At V_{ctrl} of 2V, the output waveform transformed into a square wave. When V_{ctrl} exceeded 2.5V, the output waveform changed to a triangular wave. In Figure 4.4 and Figure 4.5, the rising and falling times of the oscillation were uneven. Specifically, the falling time was relatively longer compared to the rising

time. The output waveforms corresponding to V_{ctrl} of 3V and 3.3V were similar and demonstrated the most balanced oscillation.

Noise was detected in all the output waveforms. Interestingly, the disturbance increased as V_{ctrl} decreased, while the swing of the oscillation intensified as the V_{ctrl} rose.
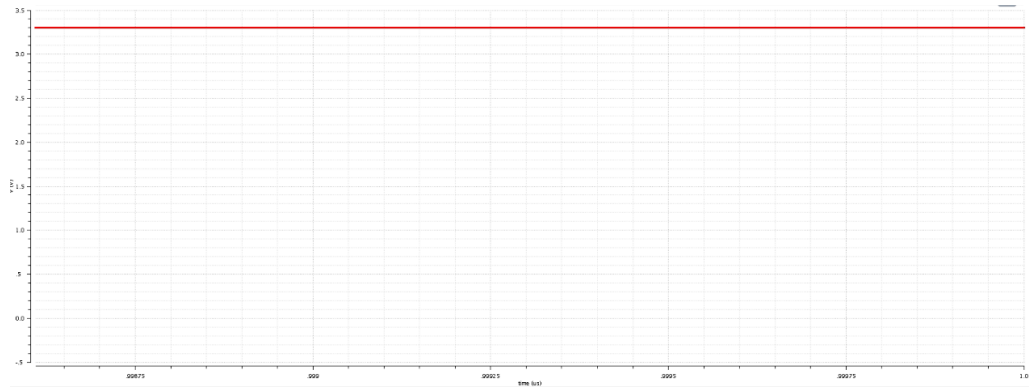
Figure 4.3: Oscillating signal when V$_{ctrl}$ = 1.5V
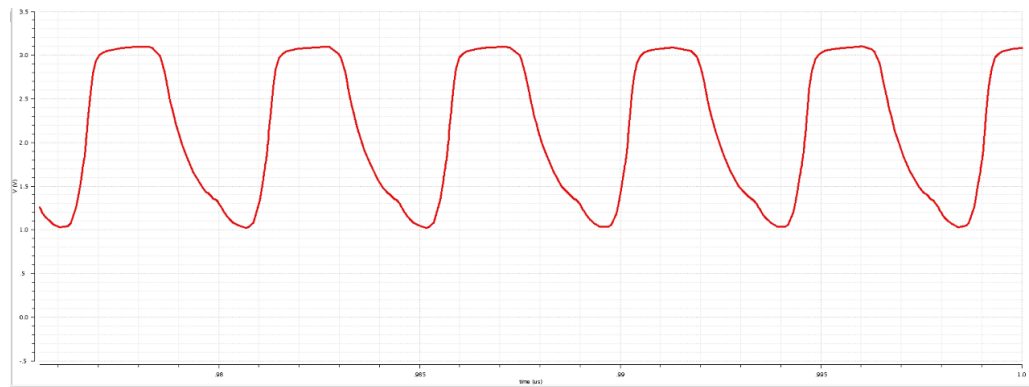
Figure 4.4: Oscillating signal when V$_{ctrl}$ = 2.0V
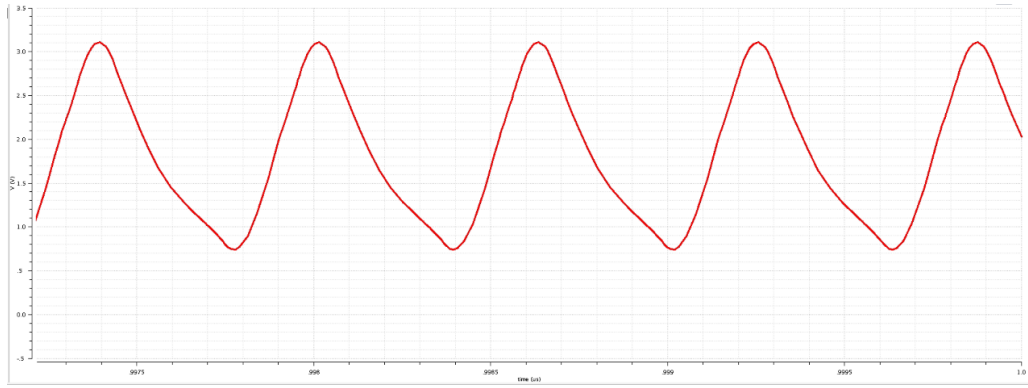
Figure 4.5: Oscillating signal when V_ctrl = 2.5V
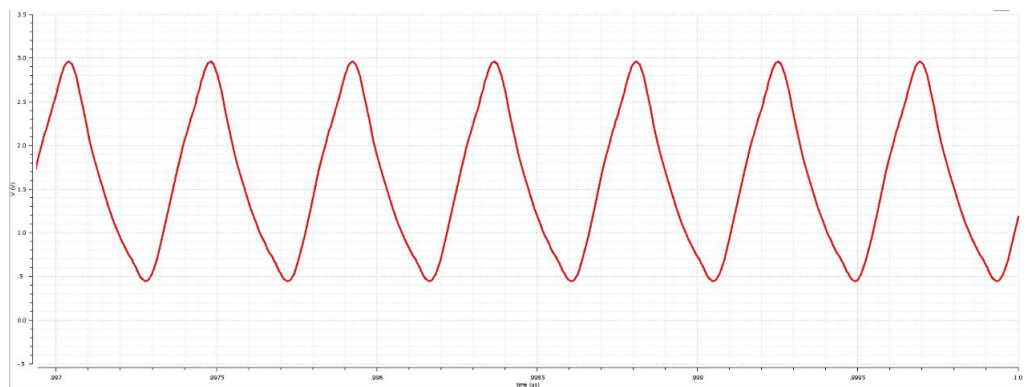
Figure 4.6: Oscillating signal when V_ctrl = 3V
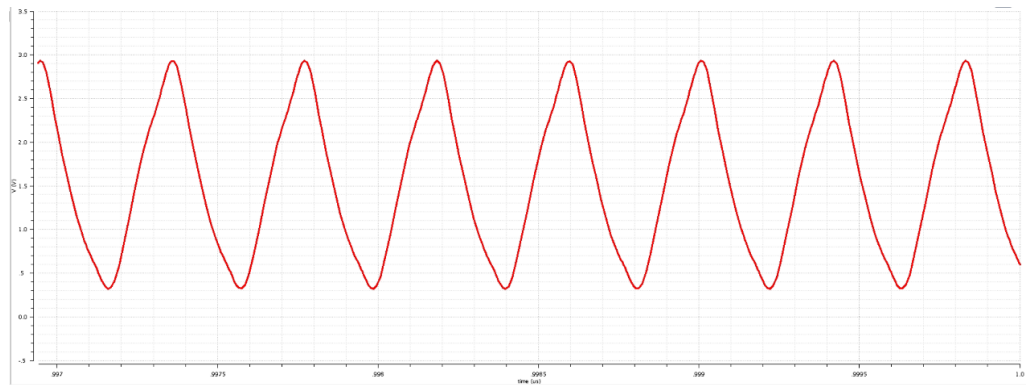
Figure 4.7: Oscillating signal when V_ctrl = 3.3V

Figure 4.8 to Figure 4.12 are the snippets of the simulation window which consist of oscillating signal from the VCRO, the input clock signal, the inverted input clock signal, and the output voltage of the CCCP (arranged from top to bottom). The clock signals were generated by buffers, which took the oscillating signal

from the VCRO as input. It is found that the buffer helped in smoothing out the signals. Subsequently, the CCCP consumed these alternating clock signals to generate the output voltage.

Since the signal did not oscillate at V_{ctrl} of 1.5V, the clock signals were in DC form as well. However, when V_{ctrl} exceeded 2V, the signals generated by the buffer became square waves, regardless of the shape of the input signal. At V_{ctrl} of 2V, the duty cycle was approximately 2:1 for the HIGH and LOW states. As the V_{ctrl} was approaching 3.3V, the duty cycle was improved, leading to more desirable clock signals.
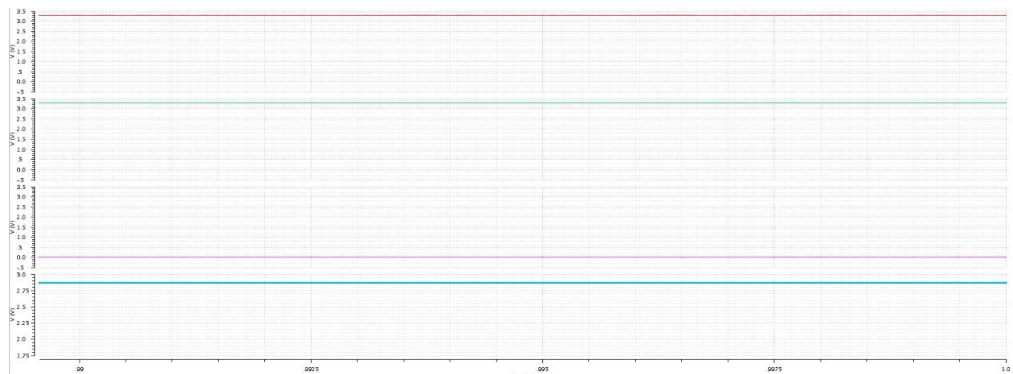
Figure 4.8: Waveforms generated when V_{ctrl} = 1.5V
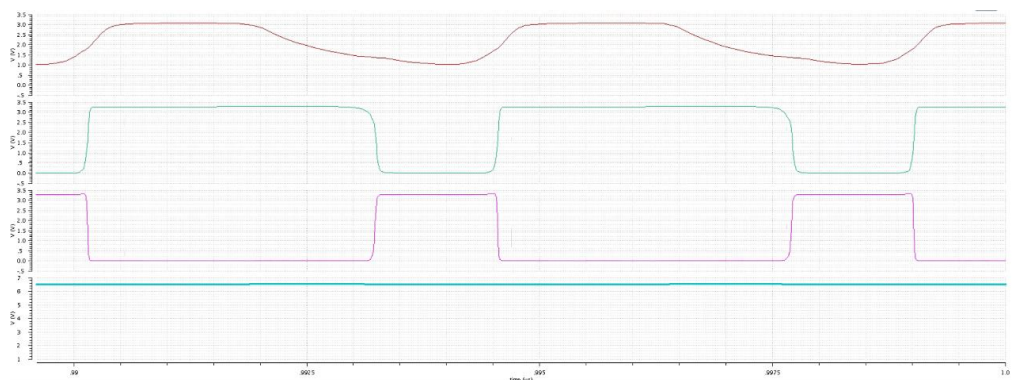
Figure 4.9: Waveforms generated when V_{ctrl} = 2.0V
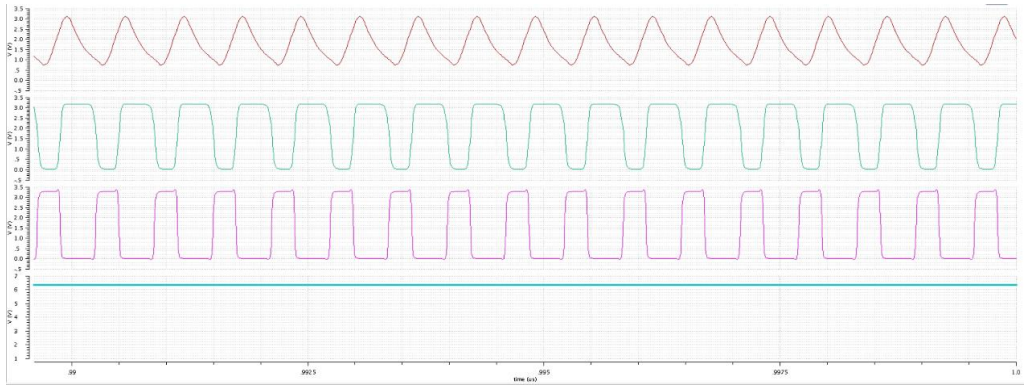
Figure 4.10: Waveforms generated when V$_{ctrl}$ = 2.5V
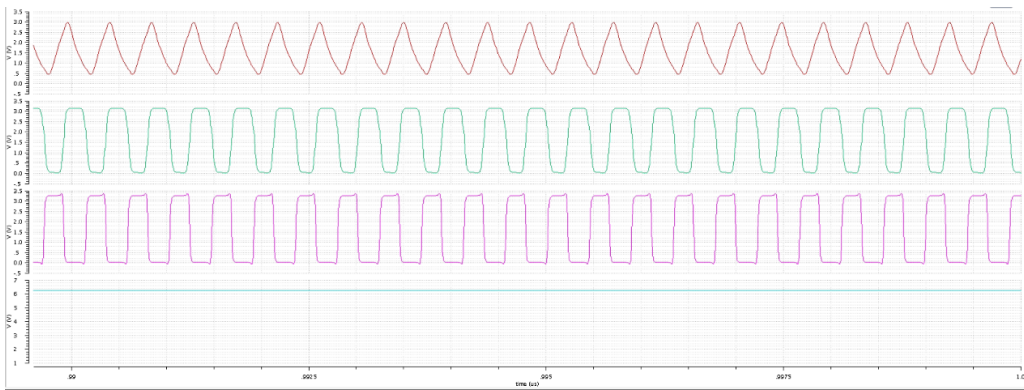
Figure 4.11: Waveforms generated when V$_{ctrl}$ = 3.0V
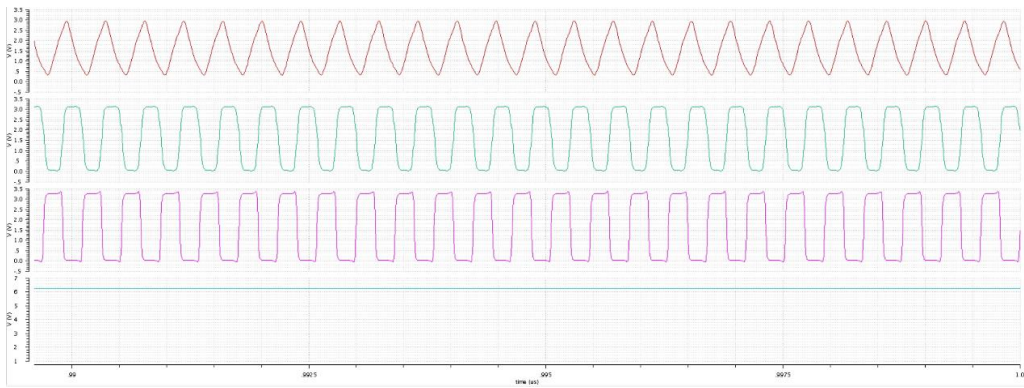
Figure 4.12: Waveforms generated when V$_{ctrl}$ = 3.3V

4.2 Performance of CCCP

The output voltage and the efficiency of the CCCP are reviewed in this section. In addition, the relationship between the charging time required for CCCP to achieve steady-state output and V_{ctrl} is investigated.

4.2.1 Output Voltage and Efficiency of CCCP

Table 4.2 shows the simulation results for CCCP including output voltage, voltage conversion efficiency (VCE) and efficiency while Figure 4.13 and Figure 4.14 depicts the performance trends of the CCCP.

Table 4.2: Simulation results for CCCP

Control Voltage, Vctrl (V)	Output voltage (V)	VCE (%)	Efficiency (%)
1.5	2.87	43.48	53.72
2.0	6.53	98.94	85.54
2.5	6.34	96.06	51.06
3.0	6.26	94.85	89.07
3.3	6.24	94.55	76.90
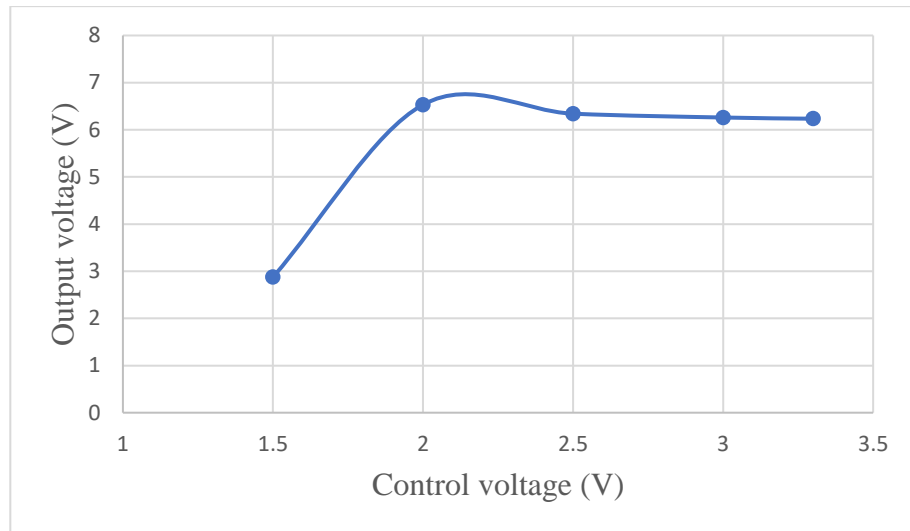
Figure 4.13: Graph of output voltage versus control voltage
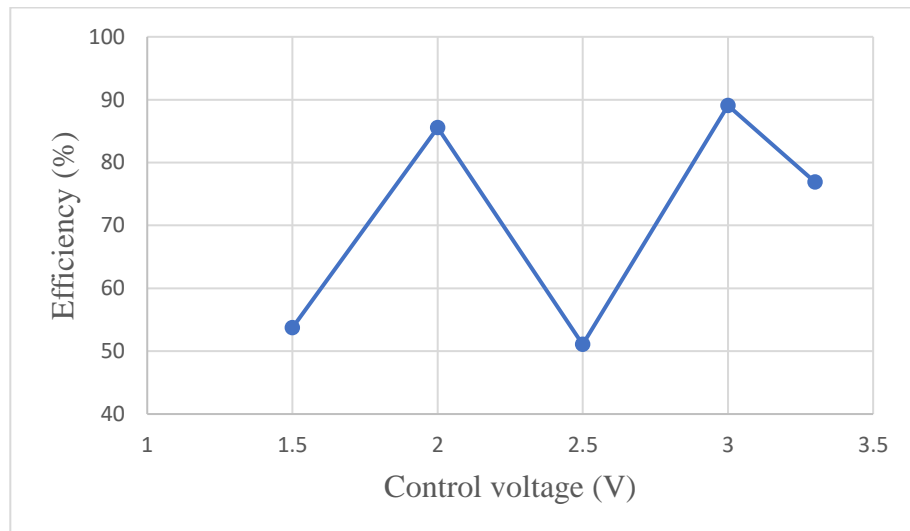
Figure 4.14: Graph of efficiency versus control voltage

At V_{ctrl} of 1.5V, the output voltage was 2.87V, which was lower than the supply voltage. As a result, the CCCP failed to fulfill its intended purpose as a voltage doubler. The maximum output voltage was achieved when V_{ctrl} was set to 2V. However, a slight decrease in the output voltage was observed as V_{ctrl} was further increased.

On the other hand, the efficiency of the CCCP was not directly proportional to the output voltage. It is observed that the efficiency varied with the increase in V_{ctrl}. When V_{ctrl} was set to 3V, the CCCP exhibited the highest efficiency, although the corresponding output voltage was 6.26V. Considering V_{ctrl} was set to a value greater than 2V, the output voltage had minor difference but the variation in the efficiency was significant.

4.2.2 Charging Response of CCCP

The CCCP was used to drive a capacitive load of 10pF. Figure 4.15 illustrates the transient response of the CCCP during the charging process until the output achieved a steady-state condition. It is found that when V_{ctrl} was set to 1.5V, the CCCP failed to meet the requirements to step up the input voltage. Impressively, V_{ctrl} of 2V resulted in the shortest charging time and highest output voltage. Yet, there was a noticeable ripple present during the steady-state period. As V_{ctrl} was increased beyond 2V, the charging process became slower and the output voltage dropped.
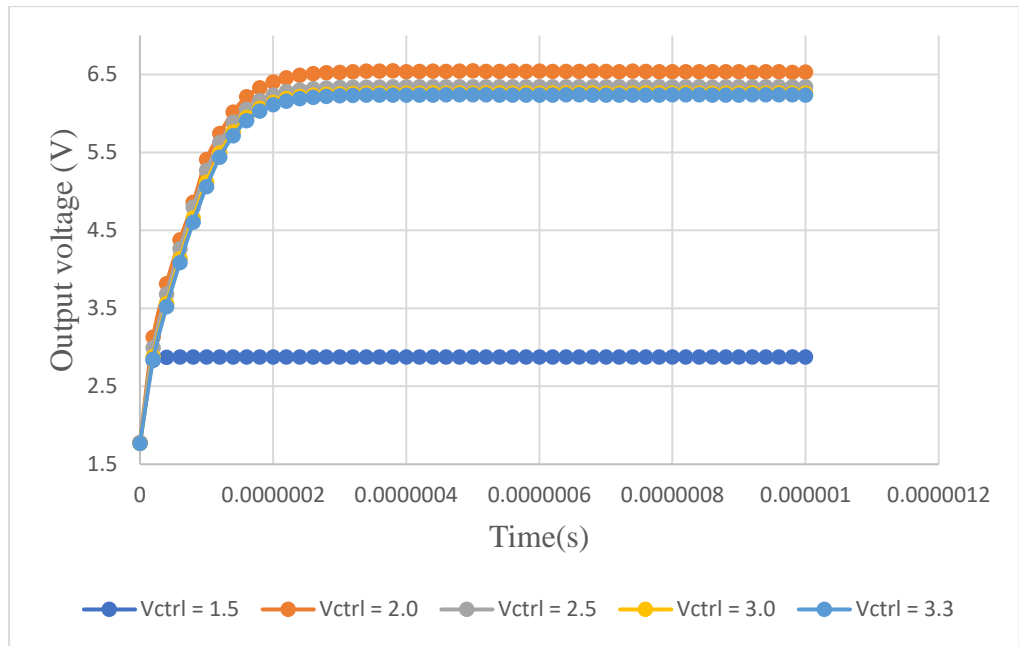
Figure 4.15: Graph of output voltage versus time

CHAPTER 5

DISCUSSION

The results obtained from the simulation in the previous chapter will be discussed in details. The performance of both voltage-controlled ring oscillator (VCRO) and cross-coupled charge pump (CCCP) are evaluated to determine the best setup for the VCRO-CCCP circuit. The application of different setup on VCRO-CCCP circuit is going to be addressed. The results in this work will be compared with the previous research to review the achievement of this work.

5.1 Performance of VCRO

The control voltage, V_{ctrl} is the key factor which affects the overall performance of VCRO. The relationship between V_{ctrl}, frequency and power consumption are investigated. In addition, the output waveform of VCRO and alternating clock signals are examined to improve the switching operation within the CCCP.

5.1.1 Effect of V_{ctrl} on Output Waveform and Alternating Clock Signals

In a VCRO circuit, the oscillation frequency is directly influenced by V_{ctrl}. V_{ctrl} has to be sufficient to adjust the biasing of the transistor within the inverter stages. Biasing refers to the DC (direct current) voltage levels applied to the transistors to establish their operating points to function properly. By modifying the biasing,

the propagation delay can be altered and this will affect the overall oscillation frequency of the VCRO.

A higher V_{ctrl} reduces the biasing resistance of the transistors, speeding up their charging and discharging processes. This shortens the propagation delay, allowing the signal to transition through the inverter stages more quickly and resulting in a higher oscillation frequency. The oscillation frequency of the VCRO is directly proportional to V_{ctrl}. Referring to Table 4.1, the simulation results align with the theory where the oscillation frequency increases with V_{ctrl}.

Theoretically, the power consumption of the VCRO circuit is primarily determined by the biasing currents and voltage levels used. Higher biasing for the transistors leads to increased power consumption due to rapid switching operations. A larger V_{ctrl} range requires more power to drive the circuitry and achieve the desired frequency tuning.

According to Table 4.1, the power consumption at Vctrl of 1.5V was negligible because the output signal from the VCRO is similar to the input supply. This indicated that 1.5V was insufficient for VCRO biasing in establishing desired operating conditions. In this case, the signal did not oscillate, resulting in minimal power consumption. The simulation results align with the expectation where higher V_{ctrl} is corresponding to higher power consumption. As the oscillation sped up, the swing of the oscillation decreased due to shorter delays. This would affect the average voltage of the oscillation signal. A smaller swing leading to a lower average voltage and increased power consumption.

The power consumption spiked up when V_{ctrl} was set to the maximum level. Biasing a transistor directly at the power supply voltage can cause gate oxide breakdown or drain-source breakdown.

Gate oxide breakdown occurs when the voltage applied between the gate and channel exceeds the breakdown voltage of the thin insulating layer (gate oxide) between them. This results in the formation of a conductive path through the oxide layer, leading to a short circuit between the gate and channel. Gate oxide breakdown can cause erratic behaviour, excessive current flow, and potential damage to the transistor.

Drain-source breakdown is associated with the breakdown of the p-n junction between the drain and source regions in Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFET). It occurs when the voltage across the drain and source exceeds a certain threshold known as the breakdown voltage. During breakdown, the p-n junction becomes highly conductive, allowing a large current to flow between the drain and source. This can result in excessive power dissipation, overheating, and permanent damage to the MOSFET.

5.1.2 Effect of V_{ctrl} on Output Waveform and Alternating Clock Signals

The bias voltage plays a crucial role in influencing the conductivity of the channel connecting the source and drain. When higher bias voltages are applied, the channel conductance increases, leading to faster charge transfer and shorter rise and fall times. Consequently, by increasing the V_{ctrl}, the output waveform of the VCRO can be enhanced. This adjustment helps in balancing out the rise time and fall time of the waveform while simultaneously reducing unwanted noise.

The bandgap reference (BGR) plays a crucial role in various applications, including analog, mixed-signal, radiofrequency and biomedical systems (Nagulapalli et al., 2021). It serves to supply biasing voltage to circuits and also provides temperature-independent voltage or current for referencing a Low Dropout Regulator (LDO). To address the mismatch issues arising from the pMOS (p-type metal–oxide–semiconductor), Nagulapalli et al. proposed a modified Meta Multiplier bias circuit. By shifting the fixed resistors to the nMOSs (n-type metal–oxide–semiconductor) drain side, threshold mismatch between the two nMOSs was minimised via the Beta Multiplier bias as shown in Figure 5.1. BGR can be implemented in the VCRO-CCCP to boost the performance of the VCRO by optimizing the biasing.
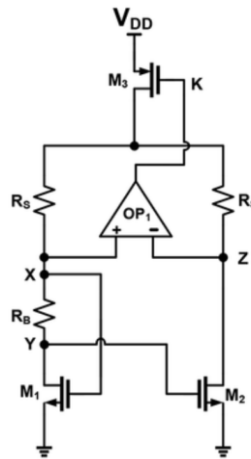
Figure 5.1: Beta Multiplier proposed by Nagulapalli et al. (2021)

On the other hand, Figure 5.2 depicts the ideal alternating clock signals for a CCCP. When the CLK signal goes LOW, the inversion of CLK must go HIGH.

During clock transitions, both n-type and p-type devices are activated simultaneously for a short duration. This creates a path for reverse charge flow from the output to the top capacitor nodes and vice versa, leading to potential

issues. Previous study has shown that the incorporation of a non-overlapping period between the main phases and the introduction of two additional phases can allow independent control of the nMOS and pMOS transistors as depicted in Figure 5.3 (Abaravicius, Cochran and Mitra, 2021). This can effectively prevent any reverse flow conditions and enhance efficiency significantly.
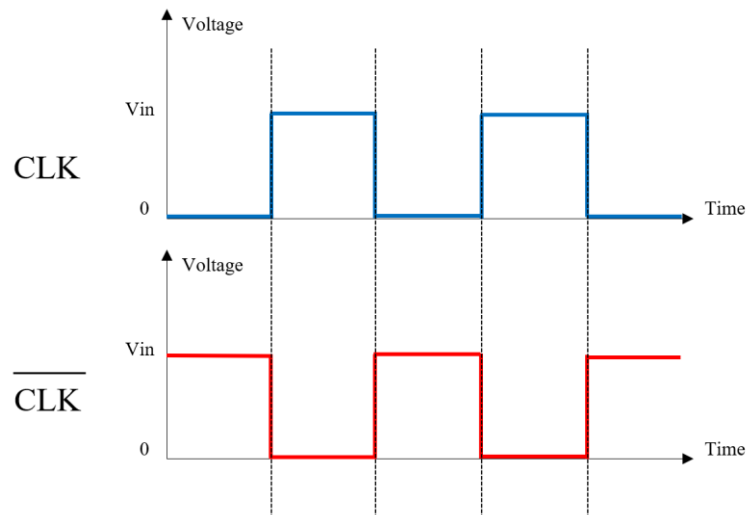
Figure 5.2: Ideal alternating clock signals
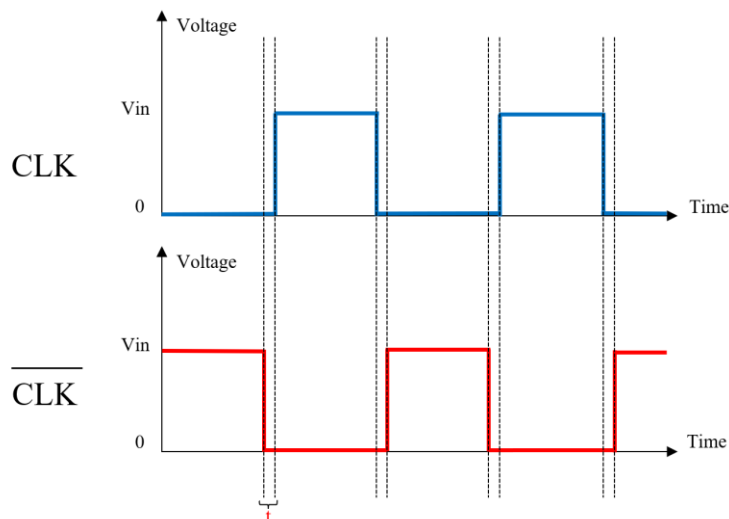
Figure 5.3: Non-overlapping alternating clock signals

5.1.3 Comparison of Proposed VCRO with Existing Work

The performance of the proposed VCRO is compared to the work conducted by Kinger et al. (2015) as illustrated in Figure 5.4 and Figure 5.5. The frequency performance of the proposed VCRO is found to lie between that of the existing VCRO and the enhanced VCRO developed by Kinger et al.
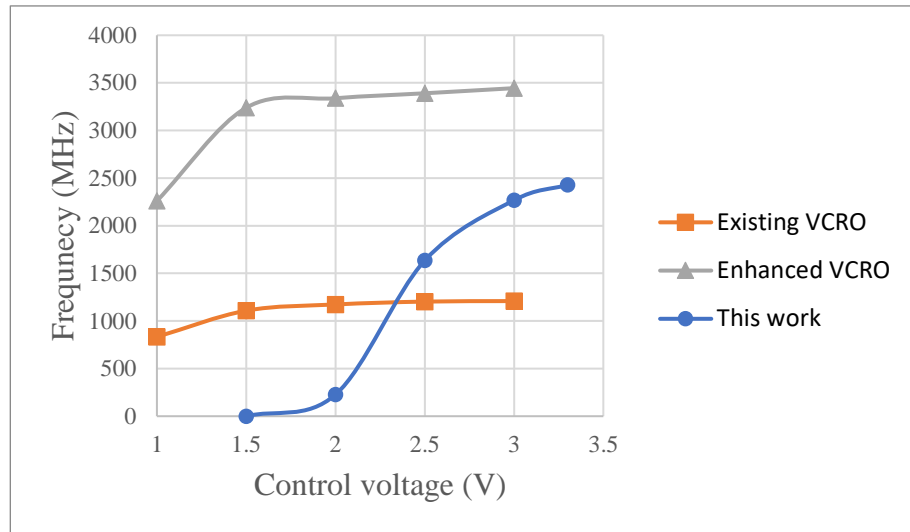
Figure 5.4: Comparison of frequency performance
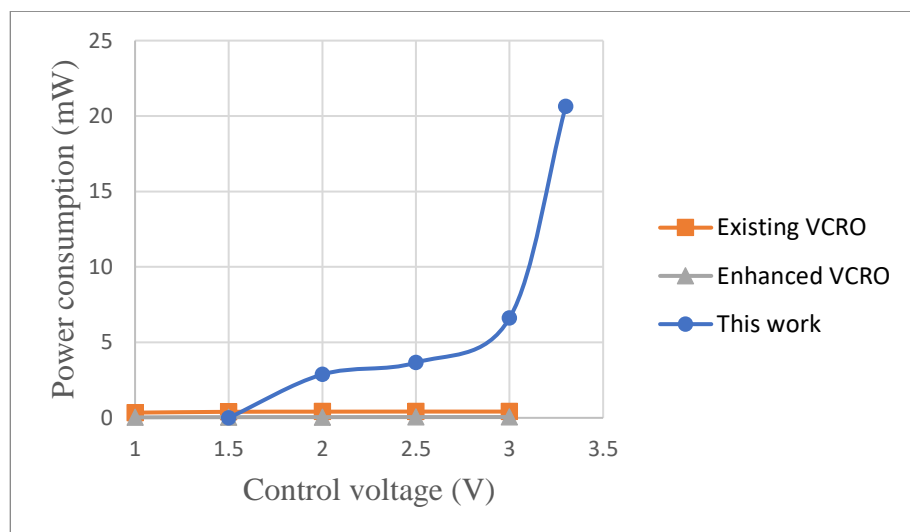
Figure 5.5: Comparison of power performance

The proposed VCRO has outperformed the existing VCRO when V_{ctrl} exceeds 2.5V. At V_{ctrl} of 3V, the frequency of proposed VCRO is twice as high as that of the existing VCRO. Nonetheless, the proposed VCRO has the highest power consumption compared to other VCRO design. VCRO by Kinger et al. and existing VCRO have consistent power consumption while the power consumption proposed VCRO varies with increasing control voltage. The reason for the higher power requirement proposed VCRO is due to 0.18μm CMOS technology whereas the previous work was using 0.13μm CMOS technology.

The most noticeable difference between 2 technologies is the feature size or critical dimensions of the transistors. In 0.18μm technology, the transistor gate length and other critical dimensions are approximately 0.18 micro-meters, whereas in 0.13μm technology, they are around 0.13 micro-meters. Smaller feature sizes allow for more transistors and increased density on a chip, leading to improved performance and reduced power consumption.

The smaller feature size of 0.13μm technology generally provides better performance compared to 0.18μm technology. Smaller transistors offer faster switching speeds and lower resistance, enabling higher operating frequencies and improved circuit performance.

Due to advancements in process technology and reduced transistor size, 0.13μm CMOS technology typically exhibits lower power consumption compared to 0.18μm CMOS technology. Smaller transistors generally have lower leakage currents, resulting in reduced power dissipation and improved energy efficiency.

As technology nodes become smaller, the cost of manufacturing tends to increase. 0.13μm technology may have higher manufacturing costs compared to 0.18μm

technology due to more advanced fabrication processes and tighter design requirements.

Even though 0.18μm CMOS technology is older and less advanced compared to 0.13μm CMOS technology, it does offer a few advantages in certain scenarios. Generally, older technology nodes tend to have lower manufacturing costs. If the production volume is not high or the application does not require the cutting-edge performance and density of 0.13μm technology, 0.18μm technology can be a more cost-effective option.

In some cases, 0.18μm CMOS technology may have better tolerance for higher voltages compared to 0.13μm technology. This can be advantageous for certain applications that require robustness against higher voltage levels.

In addition, as a more mature technology, 0.18μm CMOS has been widely used and extensively characterized. This can result in more stable and reliable manufacturing processes, as well as a larger ecosystem of available intellectual property (IP) and design tools. It may also have better yields, making it suitable for applications where reliability and predictability are crucial.

Older technology nodes like 0.18μm CMOS may still be preferred in industries where long-term availability and stability are paramount. This is particularly true for applications with longer life cycles, such as automotive, aerospace, or certain industrial applications.

5.2 Performance of CCCP

A CCCP was incorporated with the proposed VCRO to drive a capacitive load with a capacitance of 10pF. Different output voltage and efficiency are observed when V_{ctrl} was tuned from 1.5V to 3.3V. The charging response of the CCCP is examined as well.

5.2.1 Output Voltage and Efficiency of CCCP

Proper control and synchronization of the switching operation between stages are critical for maintaining high efficiency. Ensuring that the cross-coupled stages switch in a coordinated manner avoids unnecessary power dissipation and improves overall efficiency.

Leakage currents in the cross-coupled capacitors and switching devices can lead to power losses and reduced efficiency. Leakage currents can be minimized through appropriate component selection, biasing techniques, and design considerations.

When V_{ctrl} exceeded 2V, the output voltage of the CCCP was desirable. It had high voltage conversion efficiency (VCE) ranged from 94.55% to 98.94%. In other words, the CCCP is capable to charge up the capacitive load effectively and stably. However, the efficiency of CCCP is not solely dependent on output voltage. It is also affected by the clock signal waveforms therefore the efficiency fluctuates over the varied V_{ctrl}.

A V_{ctrl} of 2V exhibited high efficiency due to the lower frequency of the alternating clock signals. The switching operation of the MOSFET was at

moderate speed results in less switching losses. The alternating clock signals had imbalanced duty cycle, thus one of the cross-coupling capacitors would be stressed all the time to operate twice the period. This would affect the lifespan of the CCCP.

Furthermore, a V_{ctrl} of 3V had the highest efficiency as it had the most favourable alternating clock signals to be consumed by CCCP. The cross-coupling capacitor were working in pairs in even time frame which minimized the power loss in the CCCP.

5.2.2 Charging Response of CCCP

The CCCP demonstrated an efficiency of at least 51.06% and a VCE of 94.55% when V_{ctrl} was adjusted from 2V to 3.3V. The charging response of the CCCP is further investigated using Figure 4.15 which could be tailored to meet different design requirements.

When V_{ctrl} was set to 2.0V, the CCCP exhibited the fastest charging speed and achieved the highest output voltage. However, this advantage came at the cost of increased voltage ripple in the charging process.

Voltage ripple refers to small fluctuations of variations in the output voltage leading instability in the charged device or system. Components that rely on a stable voltage supply may be affected, causing improper functioning or even damage. If the charged device includes a battery, high voltage ripple can exert additional stress on the battery cells. This stress can impact the battery's performance, overall lifespan, and safety.

Furthermore, high voltage ripple implies a less smooth charging process, with more frequent variations in voltage levels. This can lead to energy losses and reduced overall efficiency of the charging system. The energy loss will induce heat generation within the system as well. Excessive heat can have detrimental effects on components, potentially reducing their lifespan or causing them to malfunction.

With V_{ctrl} of 3.0V, the charging speed slightly decreased compared to the 2V setting, but the output voltage remained stable and the power loss was minimal. Selecting a V_{ctrl} of 3.0V offers a trade-off between charging speed and stability, while also minimizing energy losses in the circuit.

5.2.3 Applications of Proposed VCRO-CCCP

When V_{ctrl} was set to 2V and 3.3V, the VCRO-CCCP has exceptional performance on fast charging and stable charging with minimal power loss respectively.

An electronic circuit application that requires fast charge-up is a supercapacitor-based energy storage system. Supercapacitors, also known as ultracapacitors or electrochemical capacitors, have high power density and the ability to charge and discharge rapidly. They are commonly used in applications that demand quick energy storage and release.

In certain scenarios, such as regenerative braking in electric vehicles or rapid energy bursts in renewable energy systems, the supercapacitor needs to charge up quickly to capture and store energy efficiently. The fast charge-up circuit is designed to deliver a high charging current to the supercapacitor, allowing it to

charge rapidly within a short period. The circuit may incorporate specialized charging control techniques, such as voltage and current regulation (by adjusting the V_{ctrl}), to ensure safe and efficient charging while maintaining the supercapacitor's lifespan.

By employing a fast charge-up circuit, the supercapacitor can quickly reach a desired energy storage level, enabling it to provide bursts of power when needed. This application finds utility in various fields, including hybrid and electric vehicles, renewable energy systems and power backup systems.

Alternatively, a VCRO-CCCP with stable charging is suitable for mobile phone or other portable electronic devices. These devices often rely on rechargeable lithium-ion batteries for power and efficient charging is essential to provide a reliable and long-lasting battery life. In addition, heat dissipation can be mitigated with high efficiency charging circuit and it will elongate the lifespan of the battery and the device.

5.2.4 Comparison of CCCP performance with Existing Work

A comparison of charge pump performance is shown in Table 5.1. The supply voltage and output voltage vary significantly for the different charge pumps, mainly due to the technology limitations or application requirements. The CCCP in this work showed the best performance at V_{ctrl} of 3V. Therefore, the simulation data obtained when V_{ctrl} was set to 3V is compared with the other charge pumps.

In comparison to other charge pumps, the CCCP in this work has the superior performance in the frequency. This will accelerate the switching operation of transistor within the CCCP results in rapid charging process at the output. As

different technology, topology and number of stages were being used in the previous works, the output of charge pump is evaluated based on VCE instead of the value of output voltage. It is found that the CCCP in this work and charge pump proposed by Ballo, Grasso and Palumbo (2022) have the highest VCE which is 94.85%. In other words, the output voltage is close to the ideal output voltage.

The performance of VCRO-CCCP in this work excels in multiple aspects and provides remarkably high efficiency in energy harvesting application.

Table 5.1: Comparison of charge pump performance

Reference	This work	(1)	(2)	(3)	(4)
Technology	**0.18-µm CMOS**	0.13-µm BCD	0.18µm CMOS	0.28-µm FD-SOI	0.25-µm CMOS
Topology	**Cross-coupled**	Hybrid Cross-coupled	Cross-coupled	Hybrid Cross-coupled	Dickson
Supply voltage (V)	**3.30**	3.10	1.00	0.05	2.50
Number of stages	**1**	1+4 (CC+SP)	1	1	12
Frequency (MHz)	**2267.6**	20.0/2.5	4.0	1.0	100.0
Output voltage (V)	**6.26**	26.00	1.90	0.08	28.00
VCE (%)	**94.85**	86.80	94.85	80.00	86.40
Efficiency (%)	**89.07**	42.00	91.82	38.90	23.00

(1) Abaravicius, Cochran and Mitra (2021)

(2) Ballo, Grasso and Palumbo (2022)

(3) Ballo, Grasso and Palumbo (2020)

(4) Ker and Chen (2007)

CHAPTER 6

CONCLUSIONS

The performance of voltage-controlled ring oscillator (VCRO) cross-coupled charge pump (CCCP) has been presented in this research. The control voltage of the VCRO is the key factor that affects the overall performance of the system including oscillation frequency, power consumption of VCRO, waveform of alternating clock signals, output voltage and efficiency of CCCP. The performance of the proposed VCRO-CCCP has been compared with existing work. The VCRO has outperformed the existing voltage-controlled oscillator while the CCCP is capable to generate outstanding output voltage with high efficiency. The proposed VCRO-CCCP is well-suited for the charging of portable electronic device or any system that requires fast charging.

The scope of the project is limited by technology itself and time constraint. This work could be further extended by reproducing the proposed VCRO-CCCP using 0.13μm CMOS technology. A transistor with smaller size is capable to switch at faster rate with low current leakage thus improving the oscillation frequency and reducing the power dissipation. However, it will have higher cost of manufacturing and less robustness against higher voltage levels. In addition, the performance of CCCP would be enhanced due to the exceptional alternating clock signals generated by the VCRO.

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APPENDICES

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