DESIGN OF LOW-NOISE AMPLIFIER FOR MEMS SENSORS

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A project report submitted in partial fulfilment of the requirements for the award of Bachelor of Electrical and Electronic Engineering with Honours

Lee Kong Chian Faculty of Engineering and Science
Universiti Tunku Abdul Rahman

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DECLARATION

I hereby declare that this project report is based on my original work except for citations and quotations which have been duly acknowledged. I also declare that it has not been previously and concurrently submitted for any other degree or award at UTAR or other institutions.

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ABSTRACT

This project focuses on minimizing low-frequency noise and enhancing signal integrity from a common industrial underwater pressure sensor (MS5803-14BA), whose small signal output makes it vulnerable to noise interference. In recent years, the demand for accurate and low-noise signal acquisition in MEMS-based pressure sensing applications has grown significantly. This is especially critical in underwater environments, where the design of an efficient analog front-end is essential to ensure signal integrity. To address this, the primary objective of this project is to design a low-noise, chopper-stabilized amplifier capable of interfacing with this sensor. The proposed amplifier is implemented using Generic Process Design Kit (GPDK) 90nm CMOS technology in the Cadence Virtuoso environment. Chopper modulation is employed to suppress flicker noise by modulating the low-frequency input to a higher frequency where noise is less dominant, followed by demodulation and filtering. The design process involves modelling the sensor's electrical characteristics, determining the required gain to fully utilize a 24-bit ADC, and constructing a signal chain that includes a Wheatstone bridge, NMOS chopper switches, a differential amplifier, and a low-pass filter. Transient simulation and post-layout analysis confirm the amplifier's effectiveness, achieving a gain of 20.01 dB and excellent common-mode rejection of 115.4 dB. Besides, the noise analysis shows a significant reduction in input-referred noise, from 6.33019 μV to 0.712369 μV while maintaining a low average power consumption of 17.8 μW. The output is compatible with the ADC's full dynamic range, ensuring optimal resolution. This work demonstrates a complete analog front-end solution that meets the performance requirements for high-precision MEMS pressure sensor applications. Future work may focus on integrating the digital processing blocks on-chip to streamline signal processing and minimize reliance on external components.

Keywords: Low-Noise Amplifier (LNA), Chopper Stabilization, MEMS Pressure Sensor, CMOS Circuit Design, Flicker Noise Reduction.

Subject Area: TK7800-8360 Electronics

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LIST OF SYMBOLS / ABBREVIATIONS

ΔR	Change components in resistance
R	Resistance
σ_i	Stress component
π_{11}	Longitudinal piezoresistive coefficient
π_{12}	Transverse piezoresistive coefficient
π_{44}	Shear piezoresistive coefficient
V_{Bridge_out}	Output voltage of piezoresistance bridge
V_{in}	Input signal
V_{DAC_OUT}	Output signal of DAC
N	Number of bits
LSB	Least significant bit
V_{max}	Largest measurable signal
V_{min}	Smallest measurable signal
DR	Dynamic range
G	Gain
LNA	Low-Noise Amplifier
MEMS	Micro-Electro-Mechanical Systems
ADC	Analog-to-Digital Converter
DAC	Digital-to-Analog Converter
GDPK	Generic Process Design Kit
CMOS	Complementary Metal-Oxide-Semiconductor
AOCL	Auto Offset Calibration Loop

CHAPTER 1

INTRODUCTION

1.1 General Introduction

In the fast-developing field of smart microsensors, Micro-Electro-Mechanical Systems (MEMS) are widely used to fabricate miniature sensors. This is due to its intrinsic benefits, such as high linearity, high sensitivity, low cost, small size, high reliability, and seamless integration with electronics (Kumar et al., 2019).

Among the diverse applications of MEMS, pressure sensors are particularly noteworthy, with widespread use in various industries for detecting and measuring pressure changes. In recent years, about 18% of MEMS-based sensors present in the market are pressure sensors (Kumar et al., 2019). Their ability to convert pressure variations into measurable electrical signals has revolutionized how pressure is monitored and controlled in various environments. Especially in ocean technology, receiving and processing signals in underwater detection is a crucial component. In this report, a detailed review of pressure sensors for underwater application will be discussed in Chapter 2.

MEMS pressure sensors operate on the principle of piezoresistivity, capacitive sensing, or resonant frequency, with piezoresistive sensors being among the most commonly used types. The fundamental structure of a MEMS pressure sensor typically consists of a silicon-made diaphragm, which deflects under applied pressure. As illustrated in Figure 1.1, the diaphragm is equipped with piezoresistive elements. These piezoresistors are often arranged in a Wheatstone bridge configuration, where the change in resistance is directly proportional to the strain induced by the mechanical stress on the diaphragm (Capacitive vs Piezoresistive vs Piezoelectric Pressure Sensors | The Design Engineer’s Guide | Avnet Abacus, 2015). As the pressure varies, the resulting strain in the diaphragm alters the resistance of these elements, leading to a measurable change in voltage across the bridge circuit.

Advancements in MEMS technology have enabled the integration of these sensors with complementary metal-oxide-semiconductor (CMOS)

circuitry. This enhances their performance and allows the creation of highly sensitive pressure transducers with low power consumption and high signal-to-noise ratios.

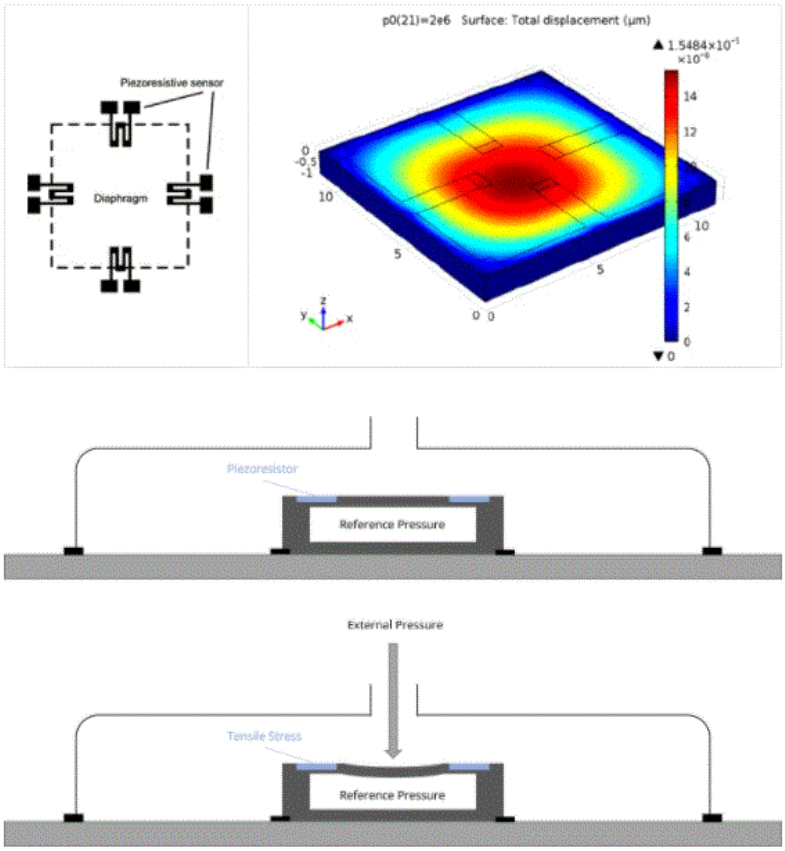

Figure 1.1: Illustration of piezoresistive sensors (MEMS Capacitive vs Piezoresistive Pressure Sensors – What are their differences? - Sens2B | Sensors Portal, 2021)

In underwater applications, the environment poses significant challenges for pressure sensors, including high pressures, temperature fluctuations, and potential interference from ambient noise. These conditions can degrade the accuracy and sensitivity of the sensors, and the collected information often contains a lot of noise (Shi et al., 2021). Moreover, signal characteristics become difficult to distinguish due to the presence of strong background noise. As a result, there is a critical need to reduce noise and improve the signal-to-noise ratio.

To increase the strength of the desired signal relative to the background noise, amplifiers are often integrated with MEMS pressure sensors.

Figure 1.2 illustrates a basic operational amplifier with two inputs: an inverting input (V_1) and a non-inverting input (V_2). The voltage difference between these inputs, known as the differential input voltage (V_{DIFF}), is amplified by the gain factor (A) of the amplifier, resulting in an output voltage (V_{OUT}) that mirrors or inverts the input polarity based on the nature of the signals.

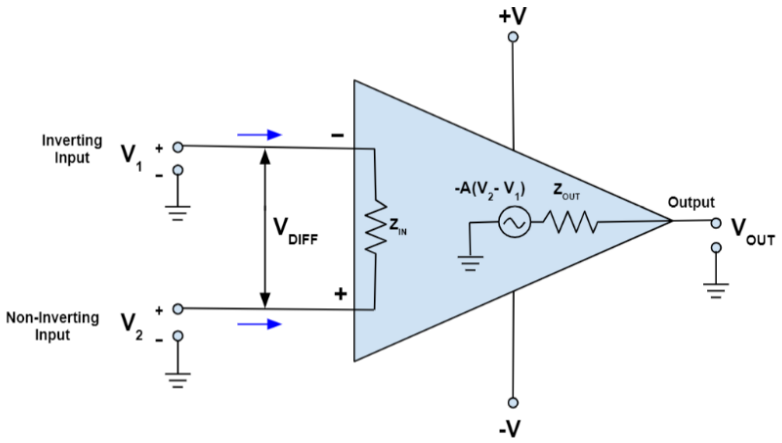

Figure 1.2: Operational Amplifier Schematic (Operational Amplifier Basics, Types, and Advantages, 2024)

Besides that, various noise reduction techniques have been developed to enhance the performance of amplifiers, particularly in improving signal integrity and sensitivity. Techniques such as chopper stabilization and auto-zeroing are commonly employed to suppress low-frequency flicker noise and other interference sources. Implementing these methods often involves trade-offs between circuit complexity, power consumption, bandwidth, and noise performance (Allstot, Li, and Shekhar, 2004). This report includes a detailed exploration of these noise mitigation strategies, which will be further discussed in Chapter 2.

Figure 1.3 shows the overview of a MEMS pressure sensing system integrated with analog signal processing and digital conversion components. The MEMS sensor chip, with its compact and sensitive design, provides the initial pressure reading, while the amplifier boosts the signal to a usable level. The subsequent analog-to-digital conversion ensures that the data can be

processed digitally, and the final output allows for real-time monitoring or further analysis. Together, these components form a robust system capable of delivering precise pressure measurements in applications where reliability and accuracy are paramount.

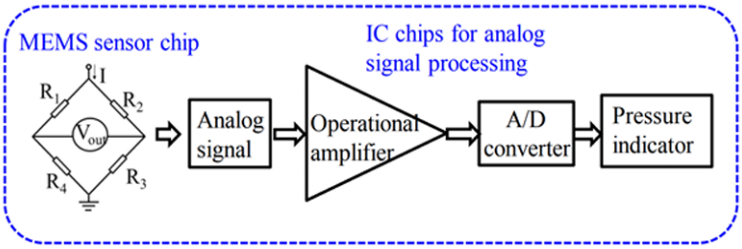

Figure 1.3: Standard MEMS pressure sensor design (Tulaev et al., 2024)

1.2 Importance of the Study

The study of MEMS pressure sensors, particularly in underwater applications, holds significant importance due to the critical role these sensors play in various industries. The ability to accurately measure and monitor pressure in challenging environments like deep-sea conditions is essential for the advancement of ocean technology, exploration, and environmental monitoring. Referring to Figure 1.4, the global market for MEMS pressure sensors is consistently growing with a compound annual growth rate of 3.8% per year to reach a value of $2.0B in 2023 (Frank, 2018). Given the steady increase in demand, there is a clear need for continued innovation and optimization of MEMS pressure sensors.

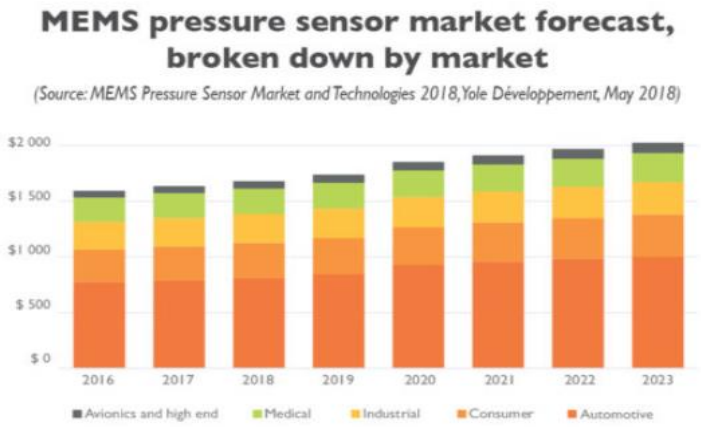

Figure 1.4: MEMS pressure sensors sales growth in 2016-2023 (Frank, 2018)

Traditional methods of underwater sensing, such as sonar and optical techniques, rely on active sensing mechanisms, which involve emitting either sound waves or light to gather information from the environment. However, these methods come with significant drawbacks that limit their efficiency and practicality, particularly in underwater environments. Sonar generates intense acoustic waves that have been shown to cause significant harm to marine life (Natarajan et al., 2014). Moreover, sonar's performance is often hindered by its relatively poor resolution, making it challenging to detect small or distant objects with high accuracy. On the other hand, optical sensing utilizes light to detect objects. While this method can be effective in clear water, its performance drastically deteriorates in clouded or turbid conditions, where suspended particles scatter and absorb light, leading to poor resolution and unreliable data (Natarajan et al., 2014).

Given these challenges, there is a critical need for the development of passive pressure sensors for underwater object detection. Unlike active sensing methods, passive pressure sensors do not emit energy into the environment; instead, they detect changes in ambient pressure caused by the presence or movement of objects. This approach is inherently more energy-efficient, reducing the strain on the limited power supplies of underwater vehicles.

Furthermore, MEMS technology offers a promising solution, with its inherent advantages of miniaturization, high sensitivity, and integration with electronic systems. However, the presence of high ambient noise and the need for precise signal processing in such environments underscore the necessity of integrating low-noise amplifiers with these sensors.

This study aims to address the challenges faced by MEMS pressure sensors in underwater applications by exploring advanced amplifier designs that can enhance signal clarity and sensor sensitivity. By improving the performance of these sensors, the research contributes to the development of more reliable and accurate measurement systems, which are vital for applications ranging from underwater exploration to industrial process control.

1.3 Problem Statement

As mentioned above, although pressure sensors provide many benefits for underwater applications, the effectiveness of MEMS pressure sensors is critically challenged by the harsh environmental conditions, such as high pressure, temperature fluctuations, and substantial ambient noise. These factors significantly degrade the accuracy and sensitivity of pressure measurements, leading to a low signal-to-noise ratio (SNR) and difficulties in detecting meaningful signals. Furthermore, these sensors are often prone to noise, making them difficult to process directly by Analog-to-Digital Converters (ADC). The challenge lies in designing a low-noise amplifier (LNA) that can effectively amplify these weak signals while minimizing noise, ensuring that the amplified signal remains within the optimal range for ADC conversion.

Although various amplifier topologies have been developed to enhance the sensitivity and reduce noise in MEMS pressure sensors, the optimal design for low-noise amplification in underwater environments remains a complex issue. This complexity arises from the need to balance linearity, input matching, and power dissipation while minimizing noise. Consequently, there is a pressing need to identify and design an amplifier that can reliably improve the SNR of MEMS pressure sensors in underwater conditions, ensuring accurate and reliable pressure measurements.

1.4 Aim and Objectives

i. Design a low-noise amplifier (LNA) tailored for MEMS pressure sensors in underwater environments.
ii. Study various types of noise reduction techniques.
iii. Study the working principle of MEMS pressure sensors for underwater applications.

1.5 Scope and Limitation of the Study

The scope of this study includes a detailed review of the existing literature on MEMS pressure sensors and their applications in underwater environments, as well as a comparative analysis of different amplifier designs based on parameters such as bandwidth, gain, and noise figure. The study will also

involve simulations using LTspice and Cadence Virtuoso to assess the performance of the amplifiers in realistic underwater scenarios. The findings are expected to contribute to the development of a more reliable and accurate MEMS pressure sensing system for underwater applications.

The initial stage of the project will involve a comprehensive analysis of past research to study existing noise reduction techniques for amplifiers. After selecting the most suitable topology, a schematic will be designed and evaluated in terms of gain, noise figure, and bandwidth. The design will then be optimized to meet the specified requirements. Finally, the amplifier will be integrated with a Wheatstone bridge in simulations to emulate its actual output performance.

The performance evaluations of the amplifiers will be primarily based on simulations and modelling due to the constraints of time and resources. As a result, the real-world applicability of the findings may require further experimental validation in actual underwater conditions. Moreover, the research is limited to the study of current and widely used amplifier topologies for MEMS pressure sensors. Emerging technologies or novel amplifier designs that have not yet been widely adopted are beyond the scope of this study.

1.6 Contribution of the Study

This study contributes to the advancement of analog front-end design for MEMS pressure sensors in underwater applications by proposing an integrated low-noise amplification solution based on chopper stabilization. One of the key contributions is the development of a systematic design methodology for implementing a low-noise amplifier (LNA) using GPDK 90nm CMOS technology within the Cadence Virtuoso environment. This includes schematic-level design, layout implementation, and post-layout verification, offering a complete design-to-simulation workflow that can be replicated or extended in future sensor interface development.

Another significant contribution is the integration of essential signal processing components such as the Wheatstone bridge, NMOS chopper switches, differential amplifier, and low-pass filter into a coherent signal chain tailored for the MS5803-14BA MEMS pressure sensor. This work also addresses the challenges of interfacing low-output sensors with high-resolution

ADCs by ensuring the amplifier design meets the required gain, bandwidth, and noise specifications.

Additionally, this project provides a reference framework for implementing noise reduction technique in low-frequency analog signal acquisition, particularly through the practical application of chopper modulation and demodulation. While simulation results confirm the effectiveness of the proposed design in reducing noise and maintaining signal fidelity, the greater value lies in demonstrating a viable, low-power, and CMOS-compatible approach to enhancing the sensitivity and accuracy of MEMS-based sensing systems.

1.7 Outline of the Report

This report is organized into five chapters, each addressing a key aspect of the study. Chapter 1 introduces the background and motivation for the research, highlighting the importance of MEMS pressure sensors in underwater applications. It outlines the problem statement, objectives, scope of the study, contribution of the study and concludes with a description of the structure of the report.

Chapter 2 presents a comprehensive literature review that covers the principles of MEMS pressure sensing, with particular emphasis on piezoresistive sensors. It also explores the biological inspiration behind passive pressure sensing and reviews previous amplifier designs and noise reduction techniques. This review forms the theoretical foundation for the amplifier design proposed in this project.

Chapter 3 describes the methodology used to design and implement the low-noise amplifier. It includes details on simulation tools, the computation of sensor and amplifier parameters, and the schematic design of individual circuit components. The chapter also explains the layout design process, verification steps such as DRC and LVS checks, and the setup for post-layout simulation.

Chapter 4 discusses the results of the simulations, including the amplifier’s transient response, noise performance, power consumption and common-mode rejection ratio. It evaluates how well the design meets the

required specifications and compares its performance to existing noise-reduction techniques discussed in the literature.

Chapter 5 concludes the report by summarizing the major findings and their implications for future research. It also offers recommendations for further improvements, such as the integration of digital processing blocks and on-chip calibration techniques to further enhance the system’s efficiency and accuracy.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

This chapter provides an overview of MEMS pressure sensors for underwater applications, with a particular focus on their integration with amplifier technologies. The review will cover several key areas, including the fundamentals of MEMS pressure sensors, the importance of amplifiers in signal processing, and techniques for improving signal quality. Additionally, this chapter reviews noise reduction techniques for the selected amplifier.

2.2 Overview of MEMS pressure sensor for underwater applications

2.2.1 Inspiration from the Blind Mexican Cave Fish

According to Natarajan et al. (2014), the lateral line system of the blind Mexican cave fish offered valuable insights into designing MEMS pressure sensors for underwater applications. The fish's lateral line system operates on passive sensing principles, detecting changes in water flow and pressure without emitting any signals. Similarly, MEMS pressure sensors for underwater applications leverage passive sensing principles. These sensors detect pressure variations without generating any external signals, making them energy-efficient and discreet.

Figure 2.1 illustrates the location of canal neuromasts within the fish’s lateral line system. This design features superficial structures for detecting water flow and fluid-filled canals for sensing pressure variations (Frank, 2018). Inspired by this biological model, MEMS pressure sensors can feature surface-mounted elements to detect rapid changes in pressure or flow and internal components to measure static pressure variations.

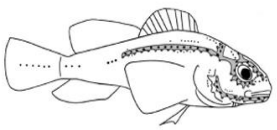

Figure 2.1: Canal neuromasts within the shaded area on the fish (Natarajan et al., 2014)

Furthermore, Nguyen et al. (2008) highlight that the flow-sensing system of fish can serve as an inspiration for developing artificial lateral lines using Micro-Electro-Mechanical Systems (MEMS) technology. To make a functional sensory system, micromachined hair cell sensors were invented that operate on the same principle as in fish. As shown in Figure 2.2, the hair cell sensor consists of two main parts, which are the hair post and the signal transducer. The hair post primarily interacts with physical signals, such as flow rate and acceleration. After interaction, the signal will be transmitted to the signal transducer, which is responsible for converting and extracting the incoming signals. The signal transducer consists of a torsional frame and two symmetrical resonators. Instead of being directly connected to the resonators, the torsional frame is coupled to the resonators via coupling combs (Yang, Hu and Wu, 2016).

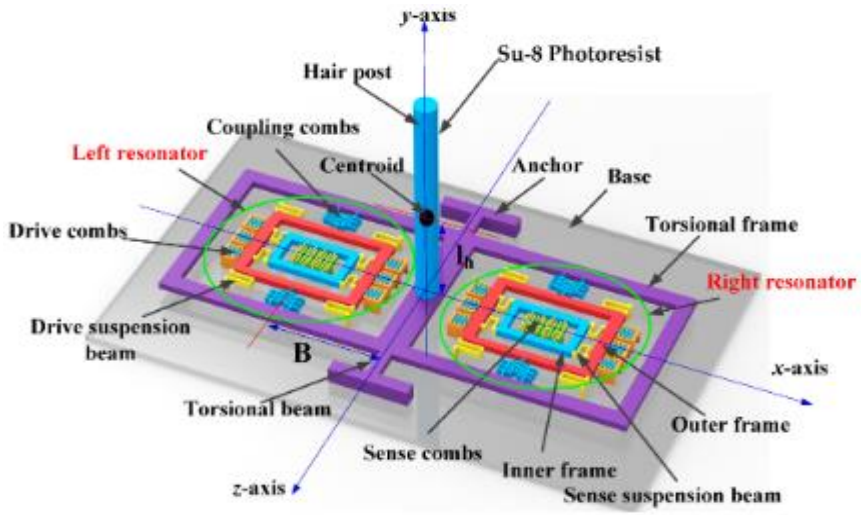

Figure 2.2: The structure of hair cell sensor (Yang, Hu and Wu, 2016)

2.2.2 Technical Analysis of MEMS Pressure Sensors

In this project, the focus will be on pressure sensors for underwater applications; therefore, gauge pressure sensors are the most suitable among others. This is because the gauge sensor would measure the difference between the sensor's internal environment and the surrounding water. This differential measurement is crucial in underwater applications, where detecting variations in ambient water pressure is vital for effective sensing and navigation. Similar to hair cell sensor, a gauge pressure sensor consists of a flexible sensing

diaphragm mounted on a base, with the base attached to the application. Referring to Figure 2.3, strain gauges are positioned on the sensing diaphragm to convert pressure changes into resistance variations in the metal piezoresistors.

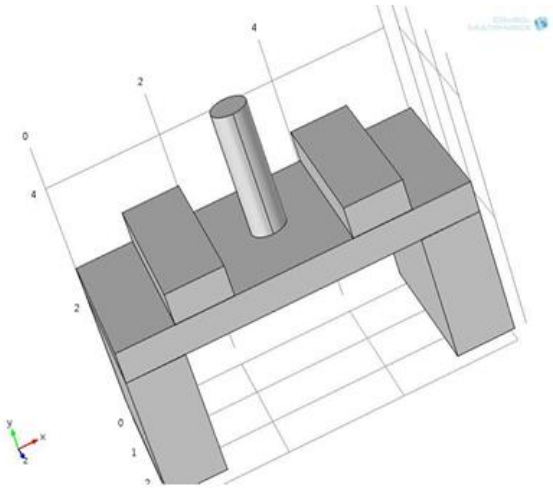

Figure 2.3: Schematic view of the gauge pressure sensor (Natarajan et al., 2014)

According to Yaul, Bulovic and Lang (2012), the gauge pressure sensors are modelled after silicon MEMS sensors, with the substrate, diaphragm, and resistive strain gauges being composed of elastomeric materials. When water flows across the sensing membrane, it creates a pressure differential between the membrane's surface and the surrounding atmosphere. As shown in Figure 2.4, this difference in pressure forces the diaphragm within the membrane to bend or deform. This is because the diaphragm is made up of elastomer, and elastomer consists of monomeric units that are naturally tangled and intertwined (Natarajan et al., 2014). When pressure is applied, these monomeric chains experience strain and start to reconfigure themselves. As the elastomer chains adjust, they contribute to the bending of the diaphragm. The degree of this bending is directly related to the amount of pressure exerted by the water flow. In other words, this bending serves as a mechanical response that can be measured and analysed to determine the pressure experienced by the membrane.

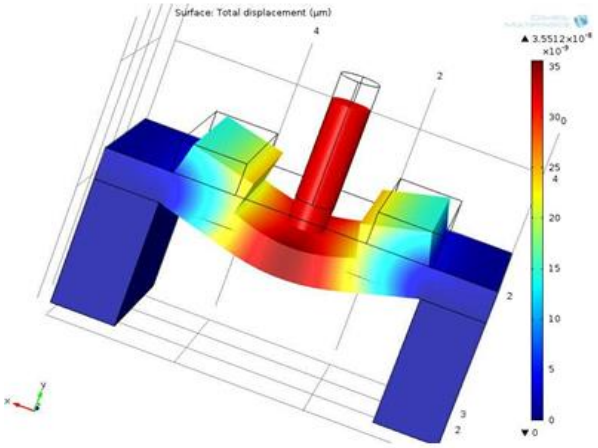

Figure 2.4: Displacement of diaphragm due to the pressure applied (Natarajan et al., 2014)

2.2.3 Analytical Solutions for MEMS Pressure Sensor

The phenomenon where a material's electrical resistance changes in response to mechanical stress is called piezoresistivity. Piezoresistivity in semiconductors is extensively utilized in various sensors, including pressure sensors. When silicon is subjected to mechanical stress, the resulting deformation alters the distribution of crystal potential. This change affects the band structure and the effective mass of both electrons and holes within the material. Consequently, the carrier mobility is modified, leading to a corresponding change in the material's electrical resistance or resistivity (Sujit, Kusuma and Hemalatha, 2017). This phenomenon is a key factor in the piezoresistive effect observed in stressed silicon.

Figure 2.5 illustrates the working principle of a piezoresistive pressure sensor. When a force is applied to the top of the diaphragm, the piezoresistors embedded within the structure experience induced stress. This stress causes their resistance to fluctuate due to the piezoresistive effect, leading to a variation in the output voltage of the Wheatstone bridge circuit. The piezoresistive effect is the underlying mechanism where the electrical resistance of the piezoresistors changes in response to the mechanical stress applied.

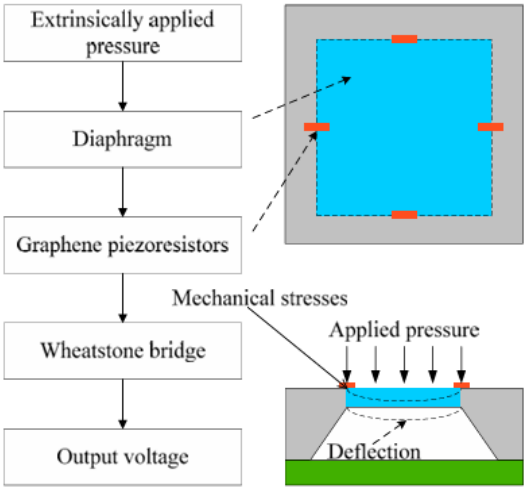

Figure 2.5: The working principle of a piezoresistive pressure sensor (Ren et al., 2022)

In a three-dimensional material like single-crystal silicon, stress and strain are not scalar quantities but are represented as tensors, which are also known as multi-dimensional arrays. Yang and Xie (2012) introduce Bond's transformation matrix, a mathematical tool used to transform these tensors from one coordinate system to another. The transformation matrix allows the derivation of piezoresistive coefficients in any arbitrary orientation of the crystal, which is essential for designing sensors that are sensitive to stress in specific directions. In this paper, the piezoresistive effect is determined using a 6 x 6 piezoresistive coefficient matrix in conjunction with the stress tensor (Sujit, Kusuma and Hemalatha, 2017). The crystallographic structure with a [1 0 0] orientation results in only three non-zero independent components (π11, π12, π44) in the piezoresistive coefficient matrix as below:

$$\begin{bmatrix} \frac{\Delta R_{11}}{R} \\ \frac{\Delta R_{22}}{R} \\ \frac{\Delta R_{33}}{R} \\ \frac{\Delta R_{23}}{R} \\ \frac{\Delta R_{31}}{R} \\ \frac{\Delta R_{12}}{R} \end{bmatrix} = \begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{bmatrix} \begin{bmatrix} \sigma_1 \\ \sigma_3 \\ \sigma_3 \\ \sigma_4 \\ \sigma_5 \\ \sigma_6 \end{bmatrix} \quad (2.1)$$

where σ_i are stress components, ΔR_{ij} are the change components in resistance, π_{11} is longitudinal piezoresistive coefficient, π_{12} is transverse piezoresistive coefficient, and π_{44} is shear piezoresistive coefficient.

Longitudinal piezoresistive coefficient, π_{11} indicates that stress along a crystal axis will cause relative changes in the resistivity or resistance components along that same axis. Transverse piezoresistive coefficient, π_{12} indicates that stress along a crystal axis will affect the relative changes in resistivity along the perpendicular crystal axis. While shear piezoresistive coefficient, π_{44} indicates that shear stress will induce relative changes in the resistivity or resistance components along the direction of the applied stress.

The simplified formula for the change in resistance of a piezoresistor can be given as follows:

$$\frac{\Delta R}{R} = \pi l \sigma l + \pi t \sigma t \tag{2.2}$$

where ΔR denotes the change in resistance resulting from applied pressure, while R represents the resistance value when no force is applied. πt and πl denotes transverse and longitudinal piezoresistive coefficients respectively, while σl and σt represent transverse and longitudinal stresses applied on the piezoresistors (Ren et al., 2022).

According to Sujit, Kusuma and Hemalatha (2017), the most common method for measuring pressure involves applying force to one side of the flexible diaphragm while a reference pressure is applied to the other. The resulting deformation of the diaphragm is then measured. Several techniques are proposed for detecting this deformation when a differential pressure is applied across the diaphragm. The majority of researchers utilize bridge connections with integrated piezoresistors, which involve placing two piezoresistors near the central zone of the membrane and the other two at the edges of the fixed diaphragm, as illustrated in Figure 2.6.

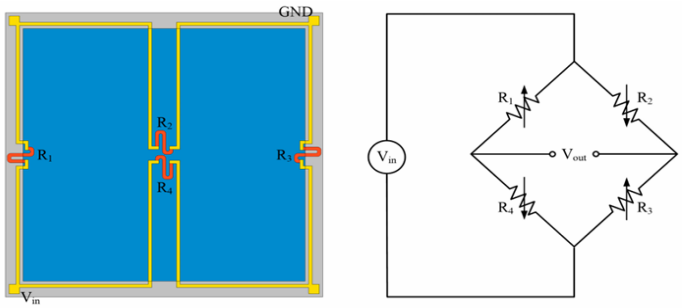

Figure 2.6: Wheatstone bridge structure and the positioning of piezoresistors (Ren et al., 2022)

As seen from Figure 2.6, four piezoresistors are arranged in a Wheatstone bridge configuration, where R_1 and R_3 represent longitudinal piezoresistors, and R_2 and R_4 represent transverse piezoresistors (Ren et al., 2022). Under zero applied pressure, the piezoresistance bridge remains in a stable state. Therefore, the voltage output of the bridge will be zero. However, when uniform pressure is applied externally, the resistance values of the piezoresistors change, causing the bridge to become unbalanced and produce an output voltage as described by the following equation:

$$V_{Bridge\ output} = \left(\frac{R_1}{R_1 + R_2} - \frac{R_4}{R_3 + R_4}\right) \times V_{DD} \tag{2.3}$$

where R_1, R_2, R_3 and R_4 are the resistances piezoresistors connected in the full bridge, V_{DD} is the input supply voltage and $V_{Bridge\ output}$ is the output voltage of the piezoresistance bridge, respectively.

2.3 Review on Low-Noise Amplifier for MEMS Pressure Sensor

2.3.1 The Importance of Integrating Amplifiers

MEMS pressure sensors produce small electrical signals in response to pressure changes. These signals are often weak and must be amplified to levels suitable for accurate processing and analysis by electronic components such as Analog-to-Digital Converters (ADCs).

According to Natarajan et al. (2014), the author analysed the change in boundary stress versus relative resistivity. As shown in Figure 2.7, when boundary stress increases, the relative resistivity also increases. It is important

to note that the magnitude of the measured signal from pressure sensors is in the micrometre range, which highlights the crucial need for high sensitivity and effective signal amplification in the sensor.

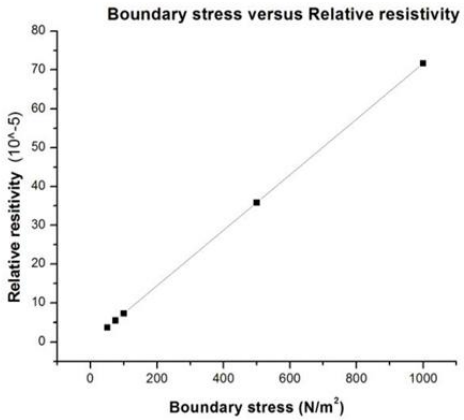

Figure 2.7: Variation of relative resistance with stress (Natarajan et al., 2014)

Therefore, a low-noise amplifier is designed to amplify the signal while adding minimal noise. This helps preserve the original signal quality and ensures that the measurement accuracy is not compromised by noise. Moreover, amplifying the signal enables the analog-to-digital converters to convert the analog signal into a digital form with higher resolution, ensuring that the full dynamic range of the ADC is utilized.

As depicted in Figure 2.8, a typical readout interface for a Wheatstone bridge-based resistive sensor includes an amplifier and subsequent processing block.

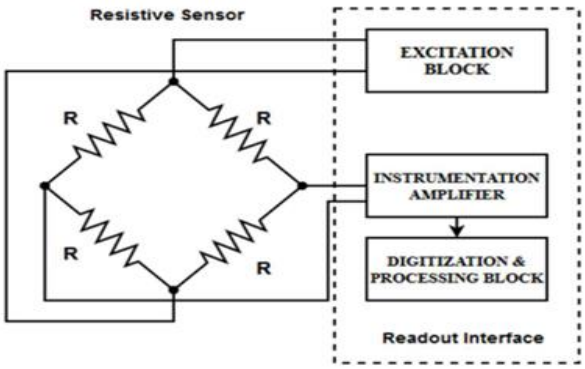

Figure 2.8: Block diagram of resistive sensor readout interface (Anupama, Roy and Padmakumar, 2023)

2.3.2 Noise Reduction Techniques for Amplifier

Ramos et al. (2012) explored the performance of conventional instrumentation amplifiers used in MEMS pressure sensor applications. The proposed design offers differential signal amplification with a high common-mode rejection ratio (CMRR), which is crucial for minimizing interference. Their study demonstrated that conventional CMOS-based amplifiers fabricated in 0.35 μm technology achieve a common-mode rejection ratio of 80 dB, and power consumption ranging from 240 μW to 870 μW, depending on the implementation. However, Ramos et al. also identified significant limitations in these amplifiers, including high input-referred noise (IRN), limited bandwidth, and increased power consumption due to the need for precisely matched resistors. These constraints have driven research toward advanced noise reduction techniques to enhance the performance of MEMS pressure sensor signal conditioning (Ramos et al., 2012).

Choi et al. (2021) proposed a fully differential amplifier with an integrated high-pass filter (HPF) design. The primary reason for implementing the high-pass filter is to reduce low-frequency noise, such as drift and interference, that can degrade the quality of the signal being amplified. In applications where the focus is on high-frequency signals, the HPF blocks unwanted low-frequency components, allowing the amplifier to amplify only the desired high-frequency signals.

Figure 2.9 shows the block diagram of the proposed amplifier design with input HPF. The amplifier uses a capacitive feedback network, which forms a high-pass transfer function. This effectively attenuates the DC offset, reducing signal distortion and preventing amplification of unwanted low-frequency components. Besides that, the high-pass filter's cutoff frequency is adjustable using a pseudo-resistor controlled by a 4-bit programmable gate voltage. This allows the filter to be fine-tuned for different conditions, ensuring optimal detection under varying signal conditions. The use of a pseudo-resistor in the high-pass filter design allows for a very high resistance value in a compact size, which is critical for implementing the high-pass filter in a small, low-power device.

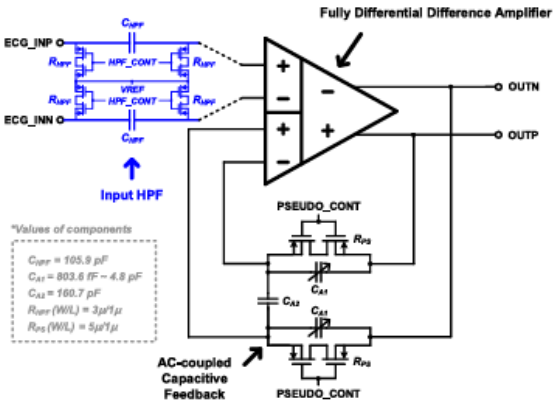

Figure 2.9: Proposed amplifier circuit with input HPF (Choi et al., 2021)

This configuration achieves an input-referred noise of 3.47 μV_{RMS} and a high CMRR of 174 dB. The detailed comparison between various proposed noise reduction techniques will be shown in Table 2.1.

Next, Yoo et al. (2022) proposed a chopper-stabilized multipath amplifier, along with an Automatic Offset Cancellation Loop (AOCL) to minimize offsets in resistive bridge sensors. The block diagram of the multipath amplifier, shown in Figure 2.10, highlights its two separate signal pathways: the high-frequency path (HFP) and the low-frequency path (LFP). The LFP is composed of five stages (G_{m21}, G_{m22}, G_{m3}, G_{m4}, and G_{m5}), while the HFP consists of two parallel stages (G_{m11} and G_{m12}) and a shared class-AB output stage (G_{m5}) with the LFP. To achieve low-noise performance at lower frequencies, the chopper technique is employed within the LFP. An AC-coupled ripple reduction loop (RRL) is implemented to mitigate the up-modulated ripple generated during chopping. For the HFP to operate efficiently, the LFP's gain is designed to be significantly higher. The LFP gain is determined by the stages G_{m21}, G_{m3}, G_{m4}, and G_{m5}, while the HFP's gain is dictated by G_{m12} and G_{m5}.

The LFP controls the low-frequency response, while the HFP governs the high-frequency band, with the RRL acting as a notch filter at the chopper frequency. Together, these paths ensure a smooth overall frequency response. To fine-tune this response, compensation capacitors (C_{m11}, C_{m12}, C_{m21}, C_{m22}, C_{m31}, C_{m32}) are added. C_{m31} and C_{m32} are specifically chosen to achieve a nearly first-order system response.

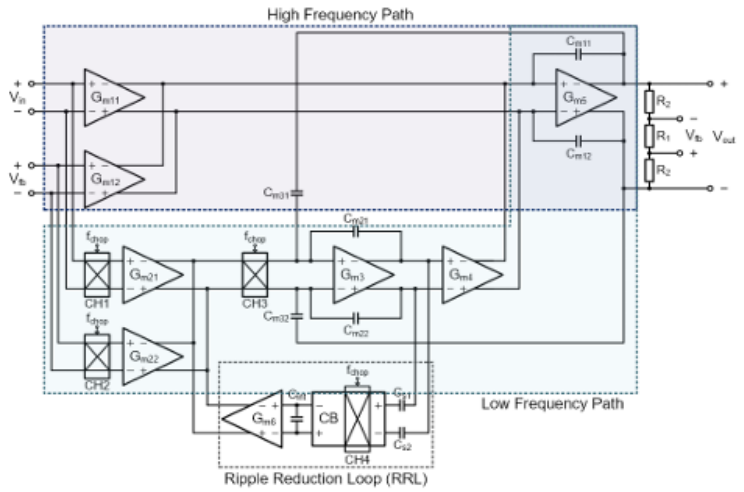

Figure 2.10: Block diagram of the multipath CFIA (Yoo et al., 2022)

The detailed operation of the RRL is as follows. The offset voltage (V_{os}) is converted to offset current (I_1) by Gm21, which is then up-modulated by the chopper CH3. The resulting square-wave ripple current (I_2) is converted into a triangular-wave voltage (V_1) by a Miller integrator, formed by G_{m3} and C_{m21}. The high-frequency components of V_1 are filtered out by AC-coupling ripple sensing capacitors (C_{s1} and C_{s2}), and the signal is demodulated back to baseband by CH4. The current buffer (CB) and C_{int} together create a low-pass filter, while the output current from G_{m6} (I_4) is fed back negatively to the summation node of the G_{m21} and G_{m22} stages, further improving performance.

In this design, the offsets in both the main high-frequency path (HFP) amplifier and the auxiliary low-frequency path (LFP) amplifier are effectively cancelled using chopper stabilization for the LFP and the Ripple Reduction Loop (RRL) for the HFP. However, offset errors in the resistive bridge sensor can still persist. To compensate for these remaining offsets, an Automatic Offset Calibration Loop (AOCL) is incorporated, as illustrated in Figure 2.11.

The AOCL consists of a comparator, a 12-bit SAR (Successive Approximation Register) logic block, and a 12-bit R-2R Digital-to-Analog Converter (DAC). This calibration loop can be activated either once during power-up, when the input is at zero, or whenever recalibration is needed. During operation, the comparator evaluates the amplified offset from the resistive bridge, and the SAR logic performs a binary-search algorithm to generate the appropriate DAC control signals. The DAC then outputs a

compensation voltage, which is fed back into the system to eliminate the offset. The resulting output voltage, incorporating the DAC's compensation, can be expressed using the equation below:

$$V_{out+} - V_{out-} = \left(1 + 2 \cdot \frac{R_2}{R_1}\right) \cdot (V_{in+} - V_{in-}) + \frac{R_2}{R_{DAC}} \cdot \left[(V_{in+} - V_{in-}) - \left(V_{DAC_{out}+} - V_{DAC_{out}-}\right)\right] \quad (2.5)$$

where R_1, R_2 are feedback resistors of amplifier, V_{in} is the input signal to the comparator, and V_{DAC_OUT} is the output signal of DAC.

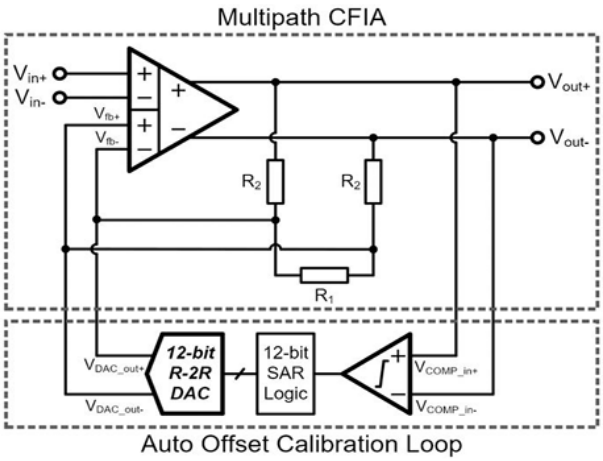

Figure 2.11: Multipath and auto offset calibration loop (AOCL) (Yoo et al., 2022)

The combination of chopper-stabilized amplification, auto-zeroing, and automatic offset calibration offers low noise, low offset, and efficient power consumption. Based on the simulations run by Yoo et al. (2022), the input-referred noise is 14.6 nV/ √ Hz, 100.7dB CMRR and 44.14dB gain.

Last but not least, chopper stabilization is a widely used technique for reducing low-frequency noise, particularly 1/f noise, and DC offset in low-noise amplifiers (Nebhen et al., 2011). This method is especially critical in MEMS-based sensor applications, where weak signals must be amplified with minimal noise interference. The fundamental principle involves modulating the input signal to a higher frequency range, amplifying it, and then demodulating it back while filtering out the unwanted low-frequency noise

components. By shifting the noise spectrum to a frequency region where thermal noise dominates, chopper amplifiers effectively eliminate the 1/f noise that typically plagues CMOS-based amplifiers (Nebhen et al., 2011).

Figure 2.12 represents a chopper amplifier architecture, illustrating key components involved in noise reduction and precision signal amplification. The first chopper shifts the input signal V_i to a higher frequency, while the amplifier block amplifies the modulated signal V_1. The second chopper converts the amplified signal back to the baseband, and finally the low-pass filter (LPF) removes the high frequency noise components.

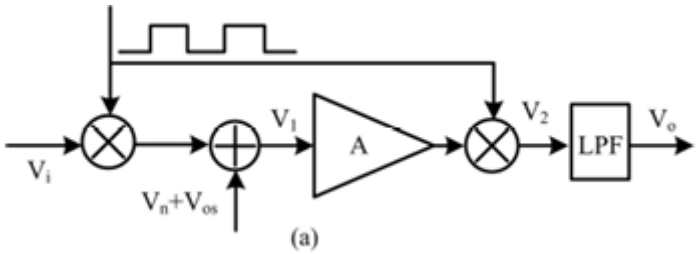

Figure 2.12: Overview of Chopper amplifier (Nebhen et al., 2011)

The chopper stabilization process consists of four main stages: modulation, amplification, demodulation, and low-pass filtering. This process is illustrated in Figure 2.13.

i. Modulation: The input signal V_i, which contains the desired signal along with 1/f noise and offset voltage V_{os}, is first modulated by a square wave signal at a frequency f_{chop}. This modulation shifts the signal spectrum to higher frequencies, away from the low-frequency noise region.

ii. Amplification: The modulated signal V_1 is then amplified using a differential amplifier. Importantly, because the low-frequency noise and offset are also modulated, they are amplified at the same higher frequency, preventing them from interfering with the baseband signal.

iii. Demodulation: After amplification, the signal is demodulated by another multiplication with the same square wave, bringing it back to its original frequency range. However, the modulated

noise and DC offset remain shifted to high frequencies, making them easy to remove.

iv. Low-Pass Filtering (LPF): The final stage involves passing the signal through a low-pass filter (LPF) to eliminate the high-frequency noise components, leaving only the clean, amplified baseband signal V_o.

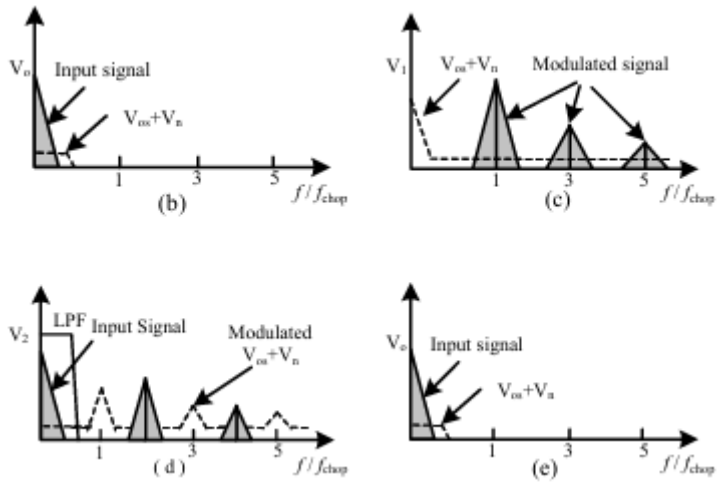

Figure 2.13: Principle of Chopper Amplifier (Yang et al., 2010)

Nebhen et al. (2011) and Yang et al. (2010) demonstrate that the implementation of chopper stabilization can effectively achieve an exceptionally low equivalent input-referred noise of just 0.194 nV/ √ Hz. This high-performance amplifier incorporates passive modulator/demodulator circuits along with a 2nd-order band-pass filter, ensuring efficient suppression of unwanted noise. Moreover, it operates with an ultra-low power consumption of only 5 μW, while delivering a 26.5 dB gain, making it highly suitable for low-power MEMS sensor applications.

In conclusion, unlike previous designs that combine auto-zeroing or other noise-cancellation add-ons such as high-pass filters and ripple reduction loops, this design focuses solely on the use of chopper stabilization. By avoiding these additional circuits, the design remains simpler, more power-efficient, and easier to implement while still achieving superior noise performance.

Table 2.1: Comparison of each noise reduction technique

Techniques	Technology	Gain	Input-referred noise (IRN)	Common mode rejection ratio (CMRR)	Power consumption	Author
Conventional	0.35 µm	7.8 dB	36 μV_{rms} (1 Hz – 4 MHz)	80 dB	240 µW	Ramos et al.
High pass filter	0.18 µm	30.35 dB	3.69 μV_{rms} (1.7 Hz to 350 Hz)	174 dB	19.4 µW	Choi et al.
Chopper-stabilized multipath and AOCL	0.18 µm	44.14 dB	14.6 nV/√Hz	100.7 dB	4.06 µW	Yoo et al.
Chopper stabilized	0.35 µm	26.5 dB	0.194 nV/√Hz	26.5 dB	5 µW	Nebhen et al.

2.3.3 Commercial MEMS Pressure Sensor and Amplifier Specification

In this project, a commercial MEMS pressure sensor, MS5803-14BA is utilized as a reference to ensure that the designed amplifier meets the system's noise and signal performance requirements.

Figure 2.14 shows the MS5803-14BA pressure sensor. It is a high-resolution MEMS pressure sensor designed for precision pressure and temperature measurements in a wide range of applications, such as water depth measurement systems, diving computers, and adventure watches. It operates over a pressure range of 0 to 14 bar and features a 24-bit ΔΣ ADC, offering highly accurate digital outputs for both pressure and temperature.

Figure 2.14: MS5803-14BA MEMS pressure sensor (TE Connectivity, 2023)

Figure 2.15 presents the technical data from the sensor's datasheet. When designing a low-noise amplifier (LNA) for this sensor, the datasheet information serves as a key reference to ensure the amplifier meets the system's noise and signal performance requirements. For example, the sensor features a 24-bit ADC, which defines the system’s noise floor. Consequently, the amplifier must be designed to maintain the high signal-to-noise ratio (SNR) provided by the sensor. With a pressure resolution of up to 0.2 mbar, the amplifier must effectively amplify small signals while minimizing noise, ensuring the amplified output is suitable for accurate digitization by the ADC.

TECHNICAL DATA

Sensor Performances (V_{DD} = 3 V)				
Pressure	**Min**	**Typ**	**Max**	**Unit**
Range	0		14	bar
ADC		24		bit
Resolution (1)		1 / 0.6 / 0.4 / 0.3 / 0.2		mbar
Accuracy 0°C to +40°C, 0 to 6 bar (2)	-20		+20	mbar
Accuracy -40°C to + 85°C 0 to 6 bar (2)	-40		+40	mbar
Response time		0.5 / 1.1 / 2.1 / 4.1 / 8.22		ms
Long term stability		-20		mbar/yr
Temperature	**Min**	**Typ**	**Max**	**Unit**
Range	-40		+85	°C
Resolution		<0.01		°C
Accuracy	-0.8		+0.8	°C
Notes: (1) Oversampling Ratio: 256 / 512 / 1024 / 2048 / 4096 (2) With autozero at one pressure point				

Figure 2.15: Technical data of MS5803-14BA (TE Connectivity, 2023)

2.4 Summary

In summary, the literature review emphasizes the significance of MEMS pressure sensors and their integration with advanced amplification technologies for underwater applications. Additionally, noise reduction techniques such as auto-zeroing and chopper stabilization were explored for their effectiveness in minimizing noise and enhancing signal quality. As shown in Table 2.1, the method proposed by Nebhen et al. (2011) demonstrated better performance in terms of input-referred noise and CMRR but sacrificed the common rejection ratio. Finally, using a commercial MEMS pressure sensor as a reference ensures that the designed amplifier meets specific performance requirements.

CHAPTER 3

METHODOLOGY AND WORK PLAN

3.1 Introduction

This chapter outlines the design of a low-noise amplifier to amplify signals from the MEMS pressure sensor. Additionally, a chopper circuit will be implemented as a noise reduction technique. In this project, simulation tools such as LTspice and Mentor Graphics EDA will be used to design and analyse the systems.

Besides that, a detailed computation will be performed to determine the amplifier's specifications, with the expected input and output clearly defined. This chapter will also cover the concept description of the proposed chopper amplifier, followed by the design procedures of each building block.

3.2 Project Work Plan

In the first stage of this project, an extensive literature review will be conducted to understand the working principles and characteristics of MEMS sensors. This will involve studying their sensitivity to noise and how low-noise amplifiers can enhance their performance. In addition, the review will focus on different noise reduction techniques, such as adding high pass filter, automatic offset cancellation loop and stabilized chopper, comparing them in terms of noise performance, common mode rejection ratio, and efficiency for MEMS applications. This stage will provide the theoretical foundation and guide the design choices for the low-noise amplifier.

The total duration of this stage is 14 weeks, starting from 20th June 2024 to 20th September 2024. Figure 3.1 shows the Gantt chart of the first stage of the project.

No.	Project Activities	Planned Completion Date	W1	W2	W3	W4	W5	W6	W7	W8	W9	W10	W11	W12	W13	W14
1.	Title registration and meet with supervisor.	2024-06-20														
2.	Doing literature research on Low Noise Amplifiers and MEMS sensor.	2024-07-26														
3.	Define project objective and problem statement	2024-07-05														
4.	Start report writing and come up with the methodology	2024-09-06														
5.	Presentation	2024-09-20														

Figure 3.1: Gantt Chart of the First Stage of the Project

In the second stage of this project, the focus shifts from theoretical exploration to practical implementation of the amplifier design. This stage involved using the Cadence Virtuoso software tools and LTspice simulator software for circuit development.

The total duration of this stage is 17 weeks, beginning on 14th February 2025 and ending on 16th May 2025. Figure 3.2 illustrates the Gantt chart of the second stage of the project.

Gantt Chart

No.	Project Activities	Planned Completion Date	W1	W2	W3	W4	W5	W6	W7	W8	W9	W10	W11	W12	W13	W14	W15	W16	W17	
1.	Prepare design tools and set up the simulation environment.	2025-02-14																		
2.	Design the chopper circuit and differential amplifier.	2025-03-14																		
3.	Design the low-pass filter for noise reduction.	2025-03-28																		
4.	Perform layout design and component placement.	2025-04-11																		
5.	Conduct DRC (Design Rule Check) and LVS (Layout vs. Schematic) verification.	2025-04-25																		
6.	Perform RC extraction and run simulations for performance validation.	2025-04-25																		
7.	Document the project, including design methodologies and results.	2025-05-02																		
8.	Presentation	2025-05-16																		

Figure 3.2: Gantt Chart of the Second Stage of the Project

The design methodology for the amplifier in this project follows a structured and iterative approach, as illustrated in Figure 3.3. The process begins with defining the sensor specifications and the required output range, which serve as the foundation for setting the amplifier's performance targets. These targets typically include gain, bandwidth, and noise level. Based on

these requirements, a suitable amplifier architecture is selected. In this case, a chopper-stabilized topology is chosen for its noise-reduction benefits.

Following architectural selection, essential design parameters such as bias current, chopper frequency, and component sizing are calculated. With these parameters, the schematic design is implemented using Cadence Virtuoso. The schematic is simulated to verify whether the design meets the targeted performance metrics such as gain, bandwidth, noise, and common-mode rejection ratio (CMRR). If the design does not meet specifications, iterative adjustments are made to the schematic or its parameters until acceptable results are achieved.

Once the schematic satisfies all performance requirements, the design is transitioned to the layout phase. After completing the layout, it undergoes two critical verification steps: Design Rule Check (DRC) and Layout Versus Schematic (LVS) check. The DRC ensures that the physical layout adheres to the manufacturing constraints provided by the semiconductor foundry. It identifies violations such as incorrect layer spacing, width violations, or improper overlaps that could compromise fabrication. The LVS check, on the other hand, compares the layout netlist to the original schematic to ensure that the circuit's connectivity and device properties are preserved. A successful LVS check confirms that the layout accurately reflects the intended circuit behavior.

If either DRC or LVS checks fail, the layout is revised and rechecked. Upon passing both checks, the design proceeds to the simulation phase, which includes both pre-layout and post-layout simulations. Before post-layout simulation, parasitic extraction is carried out to model the real-world resistances and capacitances introduced during layout, ensuring a more accurate prediction of circuit performance. The final design is only considered complete if the post-layout simulation confirms that it still meets all specifications. This comprehensive methodology ensures functional correctness, design robustness, and manufacturability, paving the way for successful chip implementation.

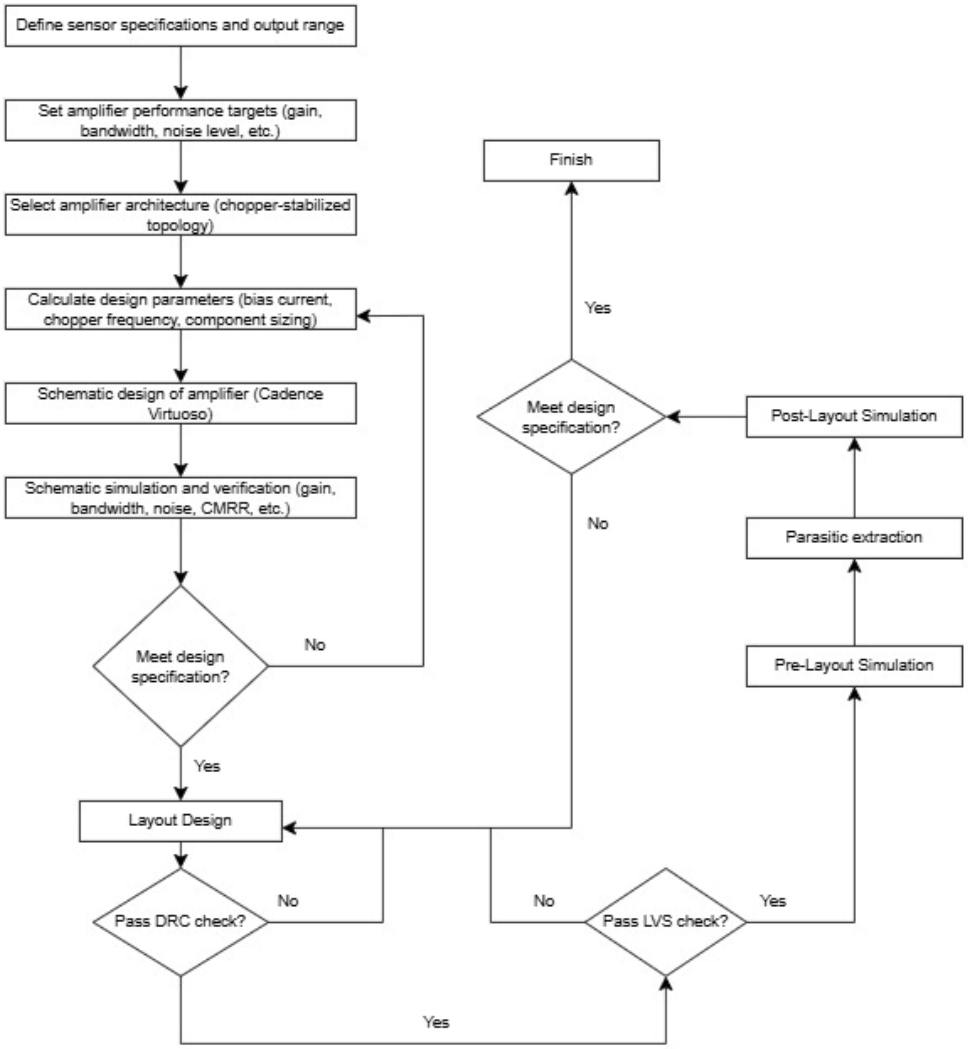

Figure 3.3: Flowchart of designing low-noise amplifier

3.3 Simulation tools

3.3.1 LTspice

LTspice is a SPICE-based simulator (Simulation Program with Integrated Circuit Emphasis). It serves as a versatile tool for both designing electronic schematics and analyzing the performance of circuits. Engineers and hobbyists can create, test, and optimize electronic designs virtually without needing to build physical prototypes. LTspice includes a highly stable and robust simulation environment, featuring a schematics editor, symbol editor, and waveform viewer for comprehensive performance evaluation.

The software provides an extensive library of both active and passive components, such as transistors, diodes, resistors, capacitors, and inductors,

making it suitable for a wide range of circuit designs. Furthermore, LTspice allows users to extract netlist information from a graphical schematic (.asc file), which is saved in a .net file format. This enables precise simulation analysis, as netlists define all the circuit connections and component parameters. With its powerful features and detailed visualization tools, LTspice stands out as essential software for simulating circuits efficiently and accurately.

Figure 3.4: Logo of LTspice

3.3.2 Cadence Virtuoso

Cadence Virtuoso is a leading electronic design automation (EDA) platform widely used in the development of integrated circuits, particularly in the areas of analog and mixed-signal design. It provides a complete suite of tools that support the entire custom IC design process, including schematic capture, circuit simulation, layout design, and verification. With its intuitive graphical interface and high-precision simulation capabilities, Virtuoso is especially well-suited for designing circuits that require careful attention to noise performance, power consumption, and layout constraints.

Furthermore, its flexibility and integration with other design tools make it a preferred choice for engineers working on sensitive analog front-end circuits and signal conditioning systems. Whether in academic research or industry applications, Cadence Virtuoso enables the creation of high-performance and reliable IC designs tailored to meet the demands of modern electronic systems.

Figure 3.5: Logo of Cadence Virtuoso

3.4 Computation of Sensor and Amplifier Parameters

Dynamic range is a measure of the ratio between the largest and smallest signals a system can accurately measure (Arar, 2018). It describes the ability of the amplifier and ADC to capture both very small and very large signals without distortion or loss of information. According to Arar (2018), the dynamic range of an ADC can be calculated as:

$$Dynamic\ range = 20\ \log_{10}\left(\frac{(2^N - 1)LSB}{LSB}\right) \approx 6.02\ \times N\ (dB) \qquad (3.1)$$

where N stands for the number of bits in the ADC, LSB stands for least significant bits.

As mentioned in the previous chapter, the commercial MEMS pressure sensor MS5803-14BA is used as a reference, which incorporates a 24-bit ADC. Based on this, the dynamic range can be calculated as 6.02 multiplied by 24, resulting in a total dynamic range of approximately 144.48 dB. Therefore, to design an amplifier that will process a signal intended for conversion into a 24-bit digital signal, a dynamic range of over 144.48 dB is required.

Next, the technical data provided in the pressure sensor's datasheet specifies a supply voltage (V_{DD}) of 3V; therefore, the sensor design in this project will also utilize a V_{DD} of 3V to ensure compatibility and optimal performance. Since the primary focus of this project is on designing the low-noise amplifier, the sensor's parameters will be based on data from previous research studies. According to Kumar et al. (2019), when there is a pressure of 1 MPa being applied to the piezoresistive bridge, the 1 kΩ n-type piezoresistors will have an enhancement of 185.2 Ω in the resistance of

longitudinal piezoresistors and a reduction of 21.64 Ω in the resistance of transverse piezoresistors. Using the bridge voltage equation from (3), the bridge output voltage can be calculated as follows:

$$V_{Bridge\_out} = \left(\frac{1185.2}{1185.2 + 978.36} - \frac{978.36}{1185.2 + 978.36}\right) \times 3 = 0.2868\ \text{V} \quad (3.2)$$

assuming 1 MPa is the maximum pressure that can be applied to the sensor, 0.286 V will be the maximum voltage applied to the amplifier.

By using all the assumptions and calculations above, the noise floor for the amplifier can be calculated as:

$$DR = 20\ \log_{10}\left(\frac{V_{max}}{V_{min}}\right) \quad (3.3)$$

where V_{max} is the largest measurable signal, V_{min} is the smallest measurable signal and DR stands for the dynamic range of the amplifier. The smallest measurable signal is typically equal to the noise level (Understanding Dynamic Range…The Numbers Game, no date). Therefore, applying all the information above, the noise level can be computed as:

$$V_{min}(Noise\ floor) = \frac{0.2868}{10^{\frac{144.48}{20}}} = 171\mu V \quad (3.4)$$

the required gain for the amplifier can be calculated as:

$$G = \frac{V_{ADC\_max}}{V_{sensor\_max}} \quad (3.5)$$

$$G = \frac{3\ V}{0.2868\ V} \quad (3.6)$$

$$G = 10.46 \quad (3.7)$$

where G is the gain of the amplifier, V_{ADC_max} is the max ADC input voltage and V_{sensor_max} is the maximum sensor's voltage output to the amplifier. So, the required gain for the amplifier would be around 10.46; this will ensure that the sensor's output signal is scaled to the ADC's full input range, allowing the ADC to make full use of its 24-bit resolution.

Besides that, the MS5803-14BA sensor offers a range of oversampling ratio (OSR) options, enabling users to optimize the trade-off between resolution, speed, and power consumption. Higher OSRs enhance the resolution of the analog-to-digital converter (ADC), but they also result in longer conversion times. For instance, the sensor's pressure conversion times can vary between 0.5 ms and 8.22 ms, depending on the chosen OSR. Consequently, the corresponding sampling frequencies range from approximately 122 Hz to 2 kHz.

In an ideal scenario, an amplifier would possess an infinite Common-Mode Rejection Ratio (CMRR), meaning it would perfectly reject all common-mode signals and only respond to differential signals. However, achieving this level of performance in practical applications is not feasible due to inherent limitations and imperfections in real-world components. Therefore, the design of the amplifier should focus on maximizing the CMRR to the highest possible extent, typically at least 90 dB or more (Maestre, 2021). This will ensure the amplifier can effectively reject common-mode noise.

Table 3.1: The required specification for amplifier

Gain	Noise-Level	CMRR	Bandwidth
10.46	<171 μV	>90 dB	122Hz - 2kHz

3.5 Overview of Proposed Chopper Amplifier Schematic Design

Figure 3.6 shows a chopper-stabilized low-noise amplification approach for MEMS sensor applications. It consists of multiple key stages: Wheatstone bridge, modulation, amplification, demodulation, and low-pass filtering, with clearly labelled pins and modules for signal flow and operation.

The input stage includes a Wheatstone bridge that generates a differential voltage signal based on the sensor's response. The differential

outputs are labelled BDNP (Bridge Differential Positive) and BDNN (Bridge Differential Negative), which serve as the input to the modulation stage.

In the modulation stage, an NMOS chopper circuit modulates the low-frequency input signal to a higher frequency, effectively reducing low-frequency noise and offset. This module has input pins INP (Input Positive) and INN (Input Negative), along with CLK and CLKB (clock signals) that control the chopping process. The modulated outputs, OUTP (Output Positive) and OUTN (Output Negative), are then fed into the amplification stage.

The amplifier stage consists of a differential amplifier, which increases the signal strength while maintaining its differential nature. The amplifier receives inputs from the previous stage and outputs an amplified differential signal to the demodulation stage.

The demodulation stage features another NMOS chopper circuit, identical to the modulation stage, which restores the signal to its original frequency while preserving the noise reduction benefits. This stage also operates with CLK and CLKB signals and provides differential outputs VOUTP (Final Output Positive) and VOUTN (Final Output Negative). Finally, the low-pass filter stage removes residual high-frequency components before delivering the clean, amplified signal to the final output. The filtering ensures the output is suitable for further signal processing in the MEMS sensor application.

This structured design effectively minimizes noise while preserving signal integrity, making it highly suitable for precision sensor interfacing.

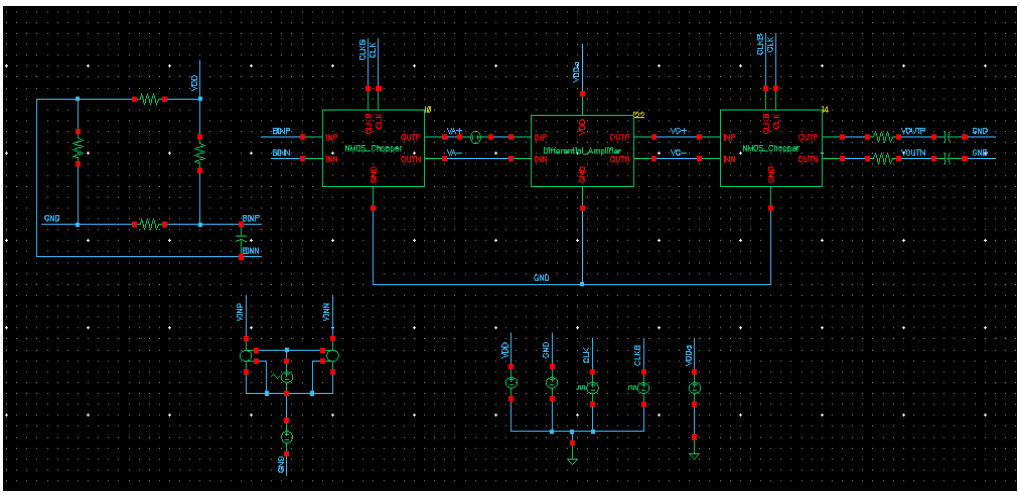

Figure 3.6: Schematic Design of Proposed Chopper Amplifier

3.6 Design Procedures of Schematic Design

3.6.1 Wheatstone Bridge

Figure 3.7 shows the schematic design of a Wheatstone bridge. The Wheatstone bridge in this design is configured to sense pressure variations using piezoresistive elements. The resistor values were carefully selected based on theoretical calculations and literature findings. According to Kumar et al. (2019), when a pressure of 1 MPa is applied to a piezoresistive bridge, the resistance of the longitudinal n-type piezoresistors increases by 185.2 Ω, while the transverse piezoresistors experience a reduction of 21.64 Ω. Based on this principle, the bridge consists of two sets of resistors: longitudinal piezoresistors with an initial resistance of approximately 1 kΩ, which increase to around 1.1852 kΩ under pressure, and transverse piezoresistors, which decrease to approximately 978.36 Ω under pressure.

The chosen resistor values ensure the simulation is similar to the real-life scenario when a 1 MPa pressure is applied to the sensor, allowing for accurate performance evaluation. Additionally, a capacitor is placed across the differential input terminals to stabilize the circuit against high-frequency noise, ensuring accurate sensor readings. The designed bridge structure is a critical component of the MEMS pressure sensing system, providing a reliable electrical representation of pressure-induced strain.

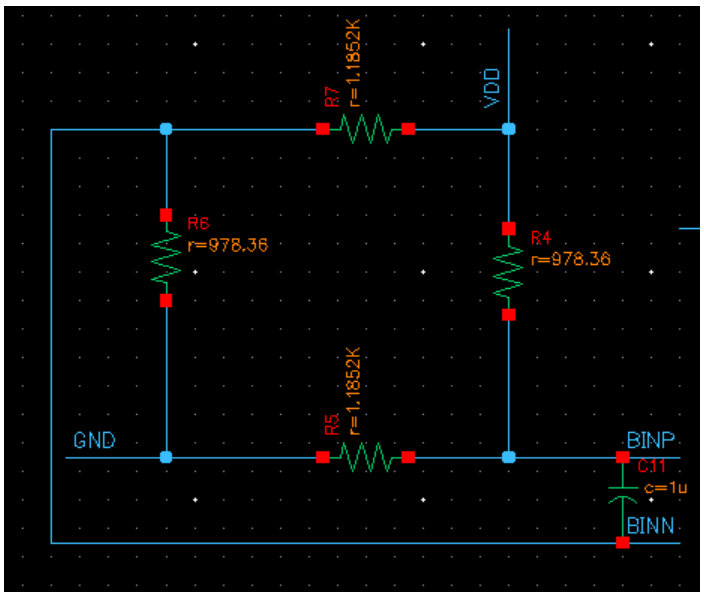

Figure 3.7: Wheatstone Bridge Schematic Design

3.6.2 NMOS-Chopper Circuit

A chopper circuit operates by periodically switching the input signal on and off at a high frequency. This modulation process shifts the signal from low-frequency baseband to a higher chopping frequency where noise effects are minimized. The demodulation stage restores the signal back to baseband after amplification or processing, effectively reducing the influence of low-frequency noise.

Figure 3.8 shows a basic chopper circuit design, it comprises NMOS switches configured in a bridge arrangement. The key components include chopping transistors (NMOS) for high-speed switching to modulate and demodulate the signal, and a clock generator that provides the chopping frequency f_{clk} to drive the NMOS switches (Sutri et al., 2015). Moreover, NMOS transistors are preferred for chopper circuits due to their superior electrical characteristics. They exhibit lower ON-resistance (R_{ON}), reducing power loss and improving efficiency. Additionally, NMOS devices offer faster switching speeds compared to PMOS counterparts, making them suitable for high-frequency applications. Their lower parasitic capacitance enhances signal integrity and reduces charge injection effects, ensuring high-fidelity signal processing (Sutri et al., 2015).

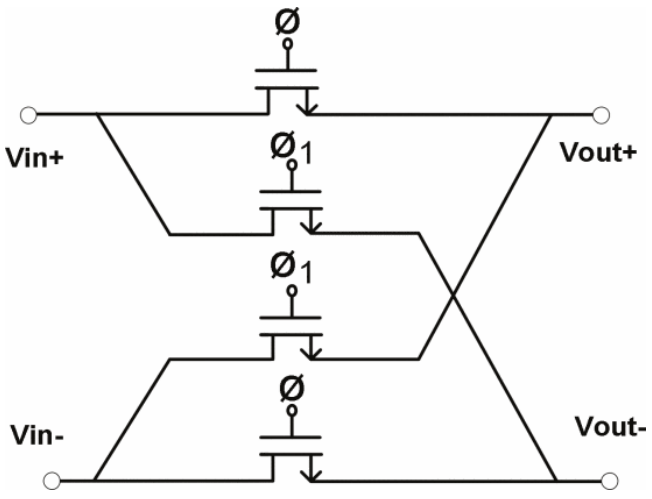

Figure 3.8: Chopper circuit (Sutri et al., 2015)

The chopper circuit is designed in a bridge arrangement as shown in Figure 3.9. It consists of NMOS transistors arranged in a cross-coupled configuration. The circuit includes differential inputs (INP and INN) and outputs (OUTP and OUTN), with clock (CLK) and complementary clock (CLKB) signals controlling the switching operation. The transistors are specified with width (w=240n or w=180n) and length (l=180n) parameters, indicating a design optimized for high-speed switching.

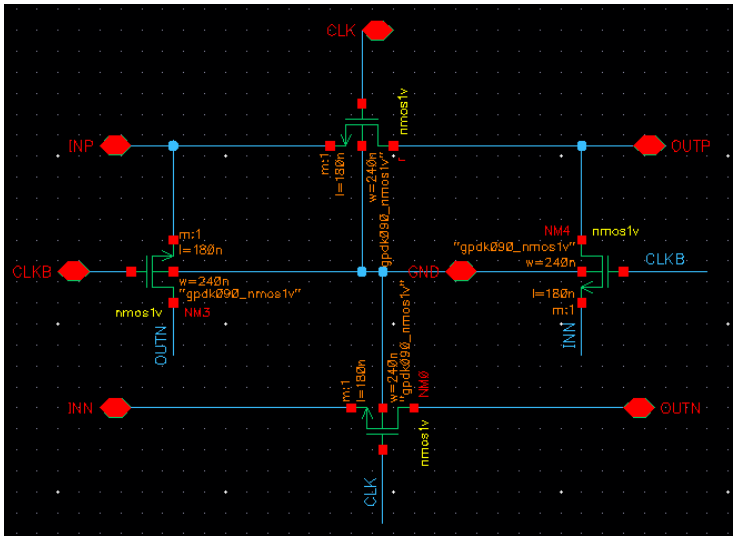

Figure 3.9: Chopper circuit schematic design

Figure 3.10 shows the properties of the voltage pulse source, which generates a clock signal with a high voltage level of 5 V and a low voltage level of 0 V. The period of the clock is determined by the inverse of the frequency (1/fclk), with a rise time and fall time of 100 picoseconds, ensuring a fast-switching transition for the circuit.

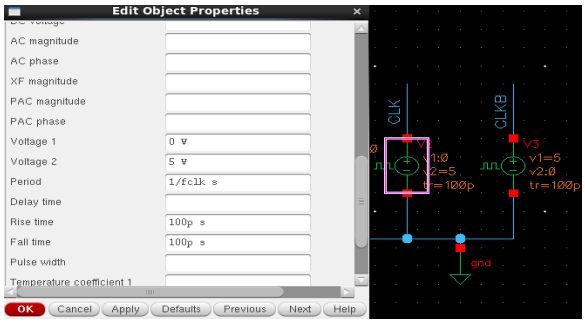

Figure 3.10: Properties for clock sources

3.6.3 Differential Amplifier

Figure 3.11 shows the schematic design for a differential amplifier. This specific design utilizes NMOS transistors and is biased with a current source to ensure proper operation. The amplifier is configured to take differential inputs (INP and INN) and produce differential outputs (OUTN and OUTP).

The core of the design consists of two NMOS transistors (NM0 and NM2), which form the differential pair. Their sources are connected together and tied to a constant current source, ensuring a stable tail current of 200 µA. The gates of NM0 and NM2 receive the differential input signals (INP and INN, respectively). Depending on the voltage difference between these two inputs, the transistors will conduct varying amounts of current, effectively steering the tail current between them.

The drain terminals of NM0 and NM2 are connected to the power supply (VDD) through resistors R8 and R1, each having a resistance of 30 kΩ. These resistors convert the drain currents into voltage signals, producing the differential output voltages at OUTN and OUTP. The high resistance values ensure a significant voltage gain for the circuit. Since the circuit is a differential amplifier, it primarily amplifies the voltage difference between the input signals while rejecting common-mode noise.

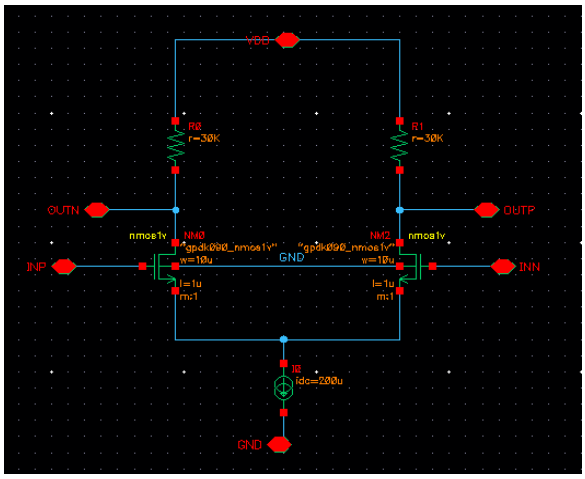

Figure 3.11: Differential Amplifier Schematic Design

3.6.4 Low Pass Filter

At the output stage, a low-pass filter is implemented to suppress high-frequency noise and recover the desired signal after chopper stabilization. Because the circuit uses chopper modulation at a frequency of 1 kHz, the cutoff frequency is designed to match the chopping frequency to ensure effective attenuation of unwanted high-frequency components while preserving the intended signal.

To achieve this, a first-order RC low-pass filter is incorporated at each output node (VOUTP and VOUTN) as shown in Figure 3.12. The filter consists of resistors R0 and R1 (each 1 kΩ) in series, followed by capacitors C0 and C1 (each 15.9 nF) to ground. The cutoff frequency of a first-order RC low-pass filter is calculated as:

$$f_c = \frac{1}{2\pi RC} \tag{3.8}$$

substituting R = 1kΩ and C = 15.9nF:

$$f_c = \frac{1}{2\pi(1 \times 10^3)(15.9 \times 10^{-9})} \tag{3.9}$$

$$f_c = 1.00\ kHz \tag{3.10}$$

this confirms that the cutoff frequency of the filter is almost exactly 1.00 kHz, ensuring optimal filtering of high-frequency chopping artifacts while preserving the intended signal integrity.

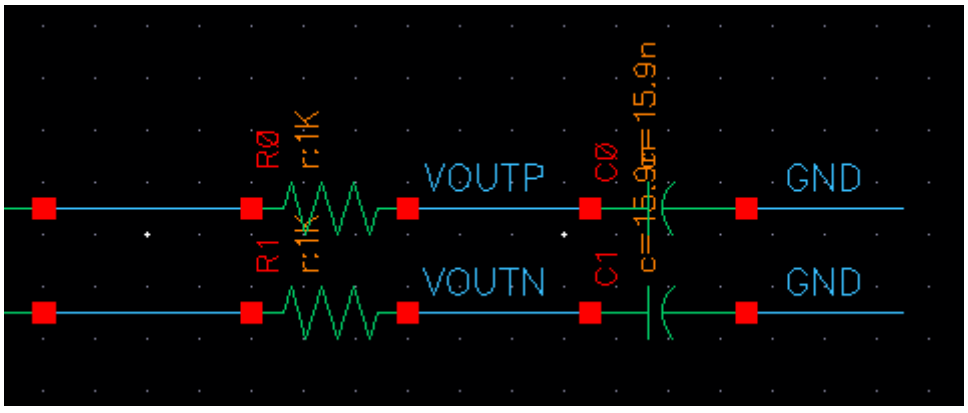

Figure 3.12: Low Pass Filter Schematic Design

3.6.5 Layout Design

In this project, the chopper amplifier layout was designed using Cadence Virtuoso, ensuring compliance with design rules while optimizing noise performance, area efficiency, and power distribution. The design focuses on proper transistor placement, routing, and parasitic reduction.

Figure 3.13 shows the complete layout design of the chopper amplifier. It consists of three primary sections: the modulation chopper, the amplification core, and the demodulation chopper. The total area of the layout, measured using the ruler provided by the design tool, is approximately 420 square micrometres. The area is carefully optimized to balance performance and manufacturability, ensuring a minimal footprint while maintaining sufficient spacing to reduce coupling effects. The centre region of the layout is dedicated to the amplification core, where matched transistors and current mirrors are placed with high precision. To the left and right, the input and output choppers are positioned, ensuring smooth signal flow from input to output. The bottom section houses the biasing network and ground, strategically placed to stabilize power supply variations.

One of the critical aspects of the layout design is transistor placement and matching. In differential amplifier structures, transistor pairs must be matched precisely to ensure consistent gain and minimal offset voltages. In this layout, common-centroid structures were employed to achieve precise matching between differential pairs.

Another key feature of the layout is the body contact strategy. Proper substrate and body connections were implemented to reduce noise coupling and prevent latch-up effects, which can degrade the amplifier’s performance. Guard rings were also included around sensitive devices to isolate them from substrate noise and ensure robust operation.

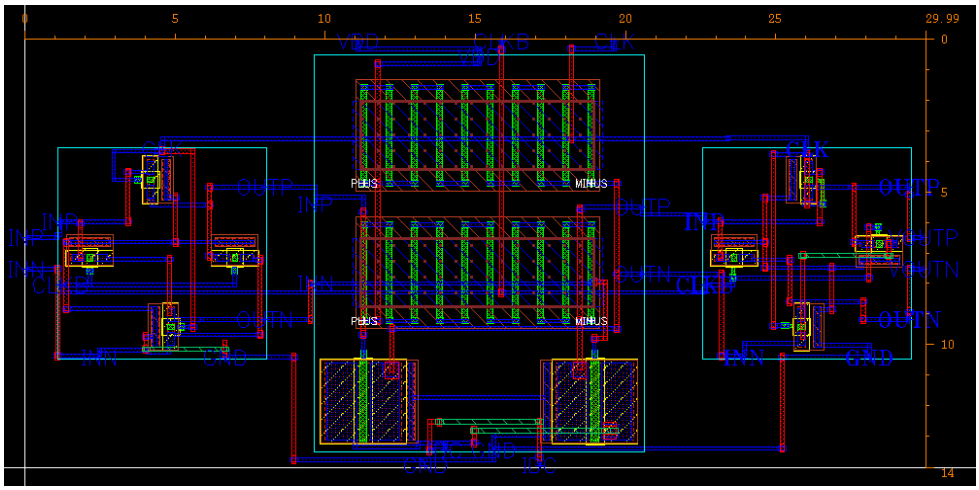

Figure 3.13: The Complete Layout Design of Chopper Amplifier

Referring to Figure 3.14 and Figure 3.15, the chopper amplifier layout successfully passed both Design Rule Check (DRC) and Layout Versus Schematic (LVS) verification. This ensures compliance with fabrication constraints and accurate representation of the circuit schematic. Design Rule Check (DRC) is used to verify whether the layout design complies with the constraints imposed by the process technology. This check is essential in the physical custom design flow to ensure that the layout meets manufacturing requirements, preventing potential chip failures. Layout Versus Schematic (LVS) is performed to compare the netlist extracted from the layout with the original schematic. The verification is considered clean if all instances, nets, and ports in the layout match those in the schematic, ensuring design accuracy before fabrication. These verifications confirm that the layout is ready for fabrication with minimal risk of errors, guaranteeing reliable performance in practical applications.

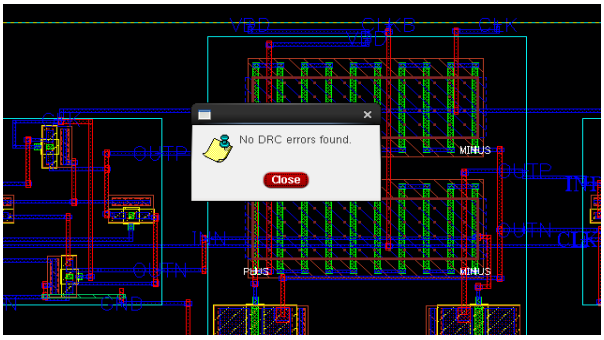

Figure 3.14: DRC Check

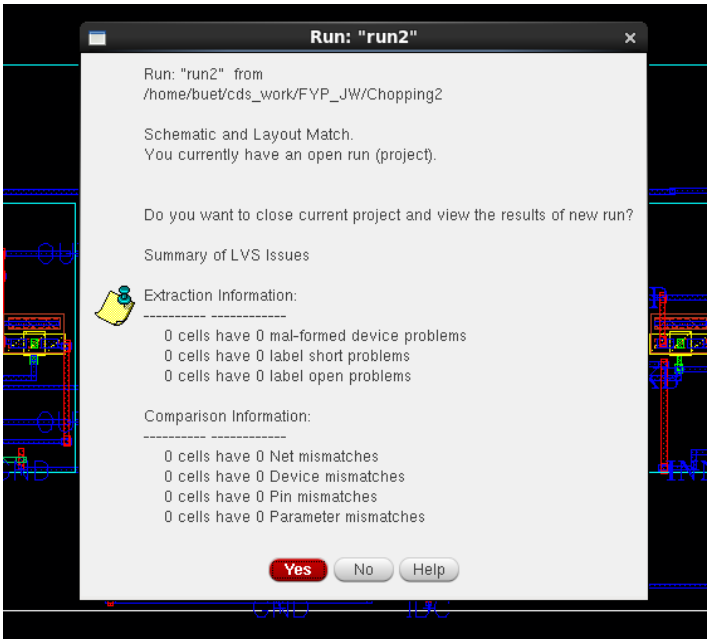

Figure 3.15: LVS Check

Figures 3.16, 3.17, and 3.18 illustrate the layout designs for each section: the modulation chopper, demodulation chopper, and differential amplifier. Each layout was carefully designed using proper routing techniques and successfully passed both Design Rule Check (DRC) and Layout Versus Schematic (LVS) verification, ensuring compliance with fabrication standards.

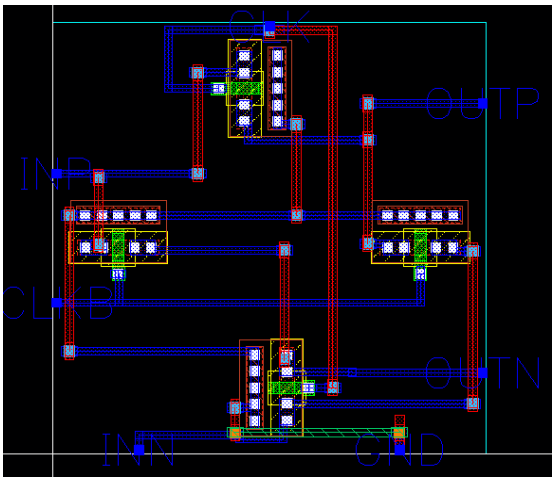

Figure 3.16: Modulation Chopper Layout Design

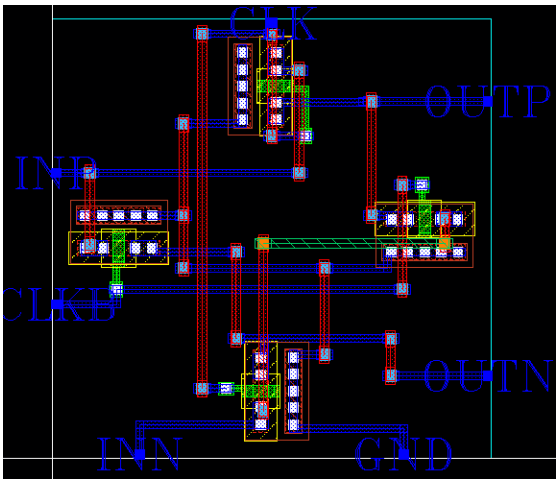

Figure 3.17: Demodulation Chopper Layout Design

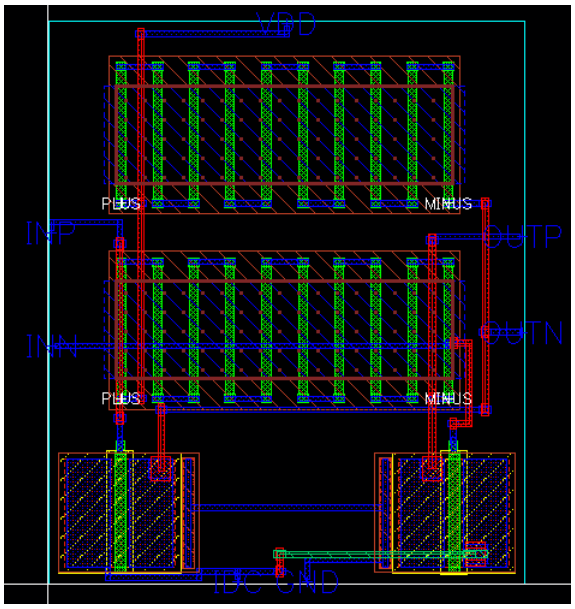

Figure 3.18: Differential Amplifier Layout Design

3.6.6 RC Extraction and Test Benches

The RC extraction and test bench setup play a crucial role in verifying the accuracy and performance of the chopper amplifier layout. Figure 3.19 presents the extraction view of the chopper amplifier, where parasitic resistance and capacitance have been included through the RC extraction process. This step ensures that real-world fabrication effects are accounted for in simulations, allowing for a more precise performance evaluation.

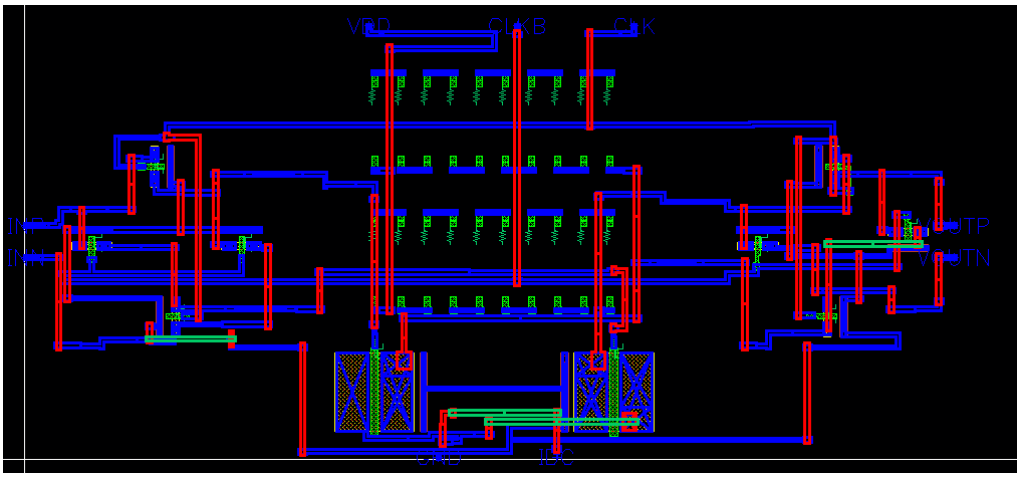

Figure 3.19: The Extraction View of Chopper Amplifier

Figure 3.20 illustrates the test bench setup used for both pre-layout and post-layout simulations. This test bench includes input signal sources, biasing circuits, and load components, replicating real-world operating conditions. By comparing the pre- and post-layout simulation results, any deviations caused by parasitic elements can be analysed and optimized before fabrication, ensuring robust circuit operation.

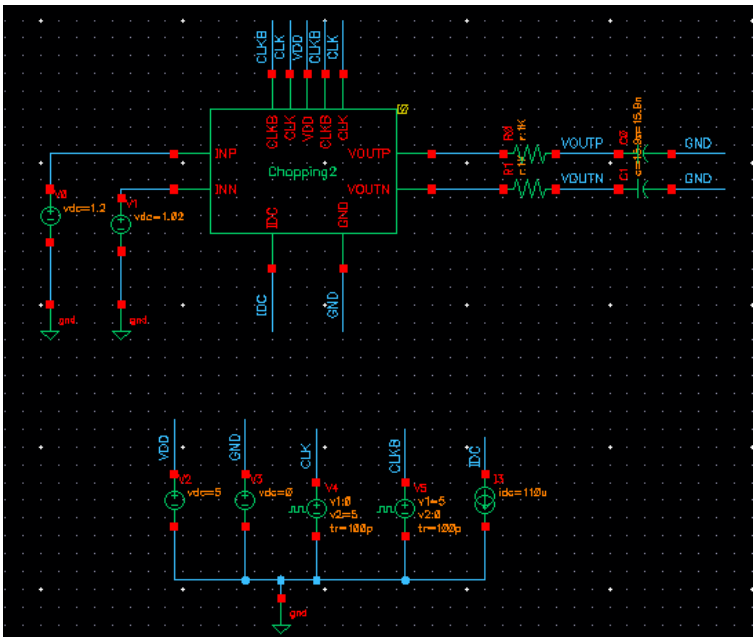

Figure 3.20: Test Bench for Pre and Post Simulation

Figure 3.21 shows the test bench that was designed to evaluate the Common-Mode Rejection Ratio (CMRR) of a differential amplifier by measuring both its open-loop and closed-loop gains. The circuit includes two differential amplifier stages, each configured to analyse the amplifier's response to different signal conditions. The top section of the schematic represents the open-loop configuration, where the differential inputs are driven by voltage sources while the output is measured without feedback. The bottom section represents the closed-loop configuration, where a feedback network is introduced to control the amplifier's gain and stability. By analysing the output voltages under these configurations, the open-loop gain (A_{OL}) and closed-loop gain (A_{CL}) can be determined. Hence, the calculation of CMRR can be done by using the formula:

$$CMRR = 20 \log \left(\frac{A_{OL}}{A_{CL}} \right) \tag{3.11}$$

The result and discussion for this CMRR calculation will be done in chapter 4.

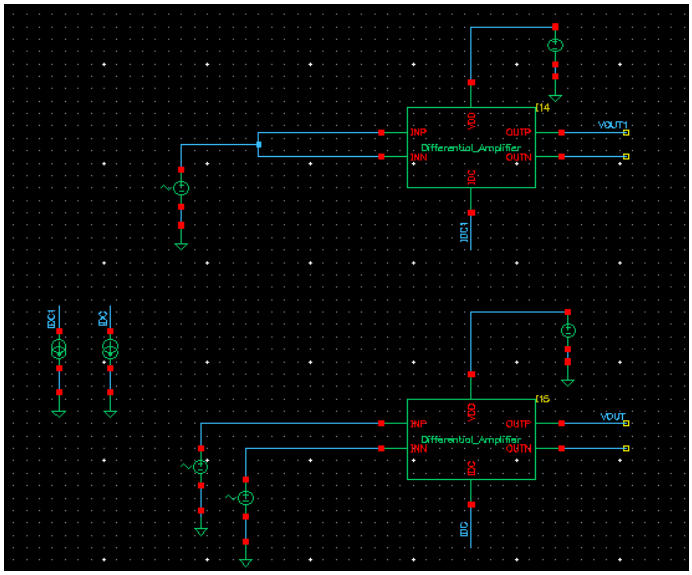

Figure 3.21: Test Bench for CMRR Calculation

3.7 Summary

In conclusion, the design is implemented using the GPDK 90nm CMOS process in Cadence Virtuoso, the design process involves the computation of sensor and amplifier parameters to determine optimal component values. This includes analysing the piezoresistive Wheatstone bridge characteristics, setting amplifier gain requirements, and selecting appropriate circuit elements to achieve the desired signal amplification with minimal noise. An overview of the proposed chopper amplifier schematic design is presented, highlighting its fundamental building blocks and operational principles. The design procedure is then detailed through a step-by-step breakdown of key subcircuits.

Besides that, the project also covers layout design, where the schematic is translated into a physical layout following the GPDK 90nm CMOS technology design rules to maintain circuit integrity and minimize parasitic effects. To ensure the accuracy of the final design, RC extraction and test bench simulations are performed, allowing the verification of circuit behaviour in a more realistic environment that includes parasitic capacitance and resistance.

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Introduction

This chapter includes a detailed evaluation of the simulation results, focusing on the noise performance of the designed low-noise amplifier, alongside the Common-Mode Rejection Ratio (CMRR) calculations. The noise analysis is crucial for understanding the effectiveness of the amplifier in suppressing unwanted signals, while the CMRR calculation provides insight into the amplifier's ability to reject common-mode noise. Additionally, the post-layout simulation results are discussed, which reflect the impact of layout parasitics on the amplifier's performance, ensuring the design's robustness in practical applications. Finally, the performance will be compared with previous noise reduction techniques proposed in past studies.

4.2 Simulation Results

The transient simulation results shown in Figure 4.1 illustrate the signal processing stages of the chopper amplifier design, demonstrating the effectiveness of the chopping modulation and demodulation technique in achieving low-noise amplification. The waveforms include the input bridge signal, clock signals, modulated signal, amplified modulated signal, and demodulated output signal.

At the first stage, the input bridge signal is observed as a low-amplitude differential voltage of approximately 180 mV. This signal represents the small voltage generated by the MEMS pressure sensor. The chopper clock signals (CLK and CLKB), shown in purple and blue, are complementary square waves oscillating between 0V and 5V. These signals control the NMOS chopper circuit, shifting the low-frequency input signal to a higher frequency, effectively minimizing low-frequency noise such as 1/f noise. Following modulation, the signal is passed through the amplifier, where the amplified modulated signal (orange waveform) reaches a peak voltage of approximately 1.805 V, indicating successful amplification. The demodulation process then shifts the amplified signal back to its original frequency domain,

producing the final output signal (VOUTP - VOUTN) with a stable amplitude of 1.802 V. This confirms that the desired gain is applied while preserving signal integrity and suppressing noise.

The gain of the chopper amplifier can be determined by calculating the ratio of the output signal amplitude to the input signal amplitude. From the simulation results, the input bridge signal amplitude is 180 mV while the output signal amplitude is around 1.802 V. Substituting the values into the voltage gain formula:

$$A_v = \frac{V_{out}}{V_{in}} \tag{4.1}$$

$$A_v = \frac{1.802\ V}{0.180\ V} \tag{4.2}$$

$$A_v \approx 10.01 \tag{4.3}$$

to get the voltage gain in decibels:

$$Gain\ (dB) = 20log_{10}(A_v) \tag{4.4}$$

$$Gain\ (dB) = 20log_{10}(10.01) \tag{4.5}$$

$$Gain\ (dB) = 20.01\ dB \tag{4.6}$$

This calculated gain of approximately 10.01 V/V or 20.01 dB confirms that the chopper amplifier effectively amplifies the input sensor signal while minimizing low-frequency noise. The achieved gain aligns with the design objectives, ensuring that the MEMS sensor output is sufficiently amplified for further signal processing.

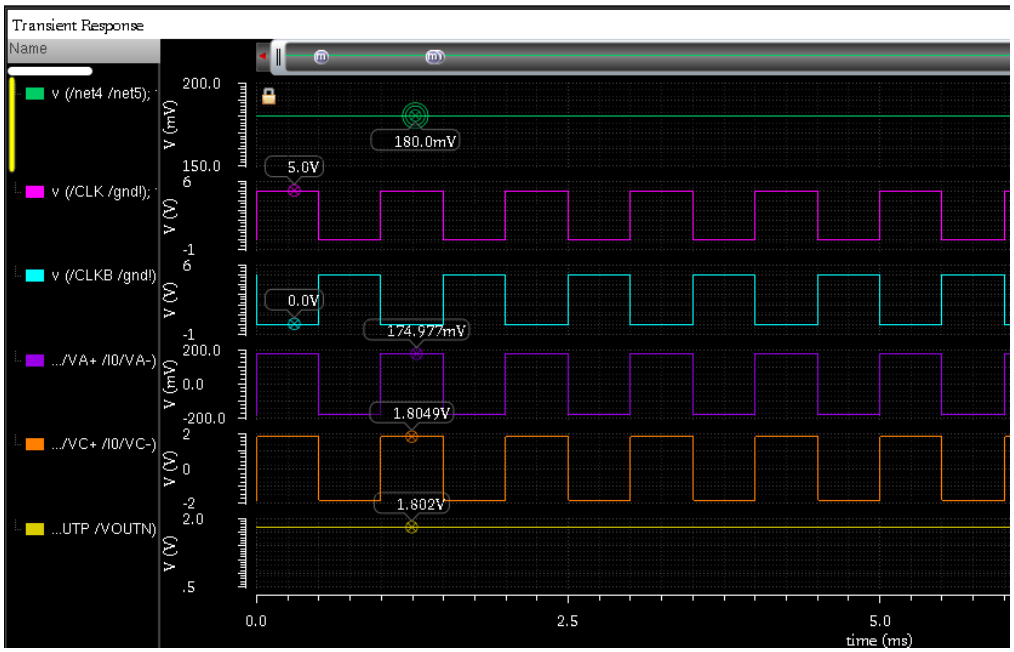

Figure 4.1: Transient Simulation Results

4.3 Noise Analysis

The noise analysis results presented in Figure 4.2 illustrate the impact of chopper modulation on the amplifier's noise performance. The upper graph represents the noise simulation performed using Cadence Virtuoso's standard noise analysis, which does not consider the effect of the chopper clock signal. In this case, the noise spectrum shows a typical 1/f (flicker) noise behaviour, where the noise level is significantly high at low frequencies and gradually decreases as frequency increases. This behaviour is the characteristic of MOSFET-based amplifiers, where low-frequency flicker noise dominates.

In contrast, the lower graph is obtained from a periodic noise (pnoise) simulation, which incorporates the effect of the chopper clock signal. Here, the noise spectrum demonstrates significant suppression of low-frequency noise, with a noticeable noise shaping effect caused by the chopper modulation. The spikes observed in the spectrum correspond to the chopper clock frequency (1 kHz) and its harmonics, indicating that the noise components have been modulated to higher frequencies, where they can be more effectively filtered out by the subsequent low-pass filter in the signal chain.

This noise reduction mechanism aligns with the primary objective of this project, which is to design a low-noise amplifier for a MEMS pressure sensor using chopper stabilization. By shifting the low-frequency noise to

higher frequencies, the chopper amplifier effectively mitigates 1/f noise, which is critical in applications requiring high precision and stability. The results confirm that the chopper modulation successfully reduces noise at low frequencies, ensuring that the amplified sensor signal remains accurate and reliable for further processing.

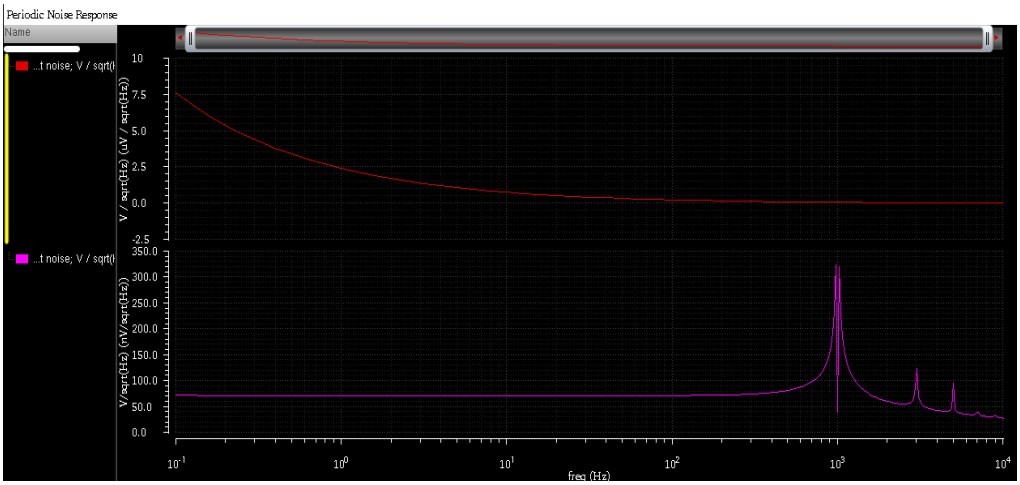

Figure 4.2: Noise Simulation Results

Furthermore, Figure 4.3 illustrates the effectiveness of the low-pass filter (LPF) in reducing high-frequency noise components in the chopper amplifier output. The upper graph represents the signal before passing through the LPF, where noticeable high-frequency fluctuations are present. These fluctuations arise due to the chopper modulation process, which shifts the low-frequency signal to higher frequencies to mitigate 1/f noise. However, this results in an output containing unwanted high-frequency components that must be filtered to obtain a clean signal.

The lower graph represents the signal after passing through the low-pass filter, which successfully attenuates the high-frequency noise while preserving the intended low-frequency signal. The result is a smoother output, with significantly reduced ripple and fluctuations, ensuring that the final signal closely represents the original sensor output without unwanted modulation artifacts.

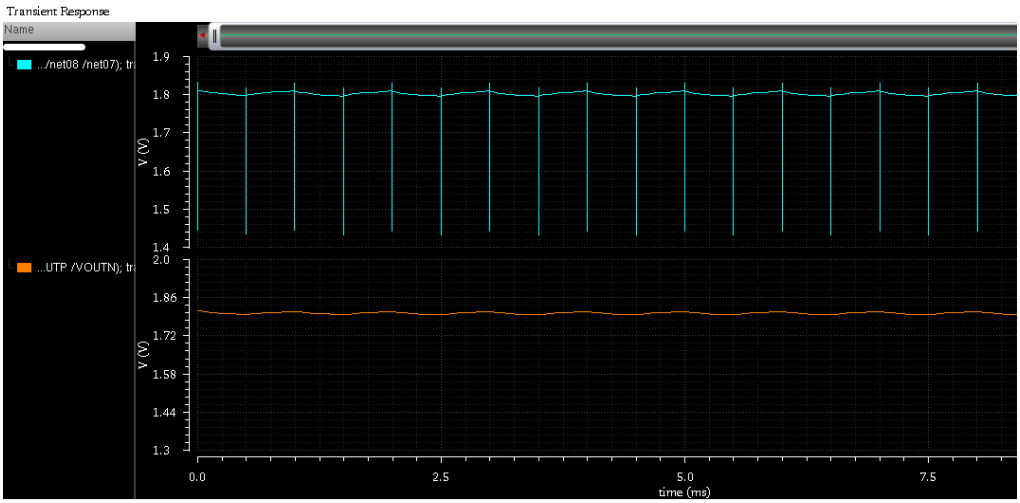

Figure 4.3: Transient Response Before and After LPF

The input-referred noise results in Figure 4.4 provide a crucial insight into the noise performance of the chopper amplifier. The first noise summary indicates a total input-referred noise of 6.33019 µV, while the second summary, which includes periodic noise analysis (pnoise), reports a lower input-referred noise of 0.712369 µV. The noise reduction improvement achieved through chopper stabilization is approximately 88.75%, this significant input-referred noise reduction highlights the effectiveness of the chopper stabilization technique in mitigating low-frequency noise.

Device	Param	Noise Contribution	% Of Total
/I22/NM2	fn	5.21748e-05	49.98
/I22/NM0	fn	5.21748e-05	49.98
/I0/NM4	id	8.5661e-07	0.01
/I0/NM3	id	8.5661e-07	0.01
/I22/NM0	id	6.78635e-07	0.01
/I22/NM2	id	6.78635e-07	0.01
/I0/NM3	fn	1.01201e-07	0.00
/I0/NM4	fn	1.01201e-07	0.00
/I4/NM3	id	8.38911e-08	0.00
/I4/NM4	id	8.38911e-08	0.00

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 7.38032e-05
Total Input Referred Noise = 6.33019e-06
The above noise summary info is for noise data

Device	Param	Noise Contribution	% Of Total
/I22/NM2	fn	5.71674e-06	48.22
/I22/NM0	fn	5.71674e-06	48.22
/I22/NM0	id	6.63946e-07	0.65
/I22/NM2	id	6.63946e-07	0.65
/I0/NM4	id	5.99219e-07	0.53
/I0/NM3	id	5.99219e-07	0.53
/I0/r	id	5.99219e-07	0.53
/I0/NM0	id	5.99219e-07	0.53
/I4/NM4	id	5.86839e-08	0.01
/I4/NM3	id	5.86839e-08	0.01

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 8.23279e-06
Total Input Referred Noise = 7.12369e-07
The above noise summary info is for pnoise data

Figure 4.4: Noise Contribution and Input Referred Noise Summary

4.4 CMRR Calculation Results

Figure 4.5 shows the calculation of the Common Mode Rejection Ratio (CMRR) using the dB20 function in Cadence Virtuoso. The formula used is:

$$CMRR = 20log_{10}\left(\frac{\frac{VOUT}{net010}}{\frac{VOUT1}{net09}}\right)$$

VOUT divided by net010 represents the open loop gain of the differential amplifier, while VOUT1 divided by net09 represents the closed loop gain. The calculation expresses CMRR in decibels (dB) to provide a logarithmic representation, which is useful for evaluating performance across a wide range of values.

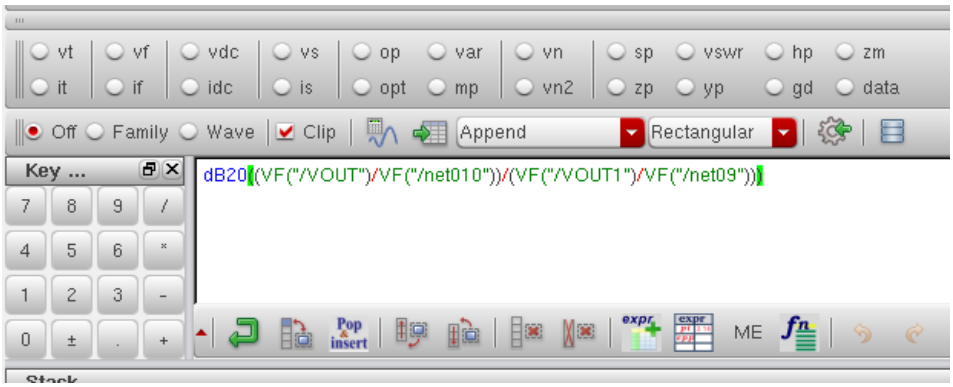

Figure 4.5: Calculation for CMRR

Figure 4.6 illustrates the Common-Mode Rejection Ratio (CMRR) of the differential amplifier across various frequencies. The CMRR remains constant at approximately 115.4 dB, indicating excellent rejection of common-mode signals. This high CMRR value ensures that the amplifier effectively suppresses noise and interference that appear equally on both inputs, which is crucial for precision signal processing applications.

dB20((VF("/VOUT")/VF("/net010"))...

	freq (Hz)	dB20((V...)) (dB)
1	100.0E-3	115.4
2	125.9E-3	115.4
3	158.5E-3	115.4
4	199.5E-3	115.4
5	251.2E-3	115.4
6	316.2E-3	115.4
7	398.1E-3	115.4
8	501.2E-3	115.4
9	631.0E-3	115.4
10	794.3E-3	115.4
11	1.000	115.4
12	1.259	115.4
13	1.585	115.4
14	1.995	115.4
15	2.512	115.4
16	3.162	115.4
17	3.981	115.4
18	5.012	115.4
19	6.310	115.4
20	7.943	115.4
21	10.00	115.4
22	12.59	115.4
23	15.85	115.4
24	19.95	115.4
25	25.12	115.4
26	31.62	115.4
27	39.81	115.4
28	50.12	115.4
29	63.10	115.4
30	79.43	115.4
31	100.0	115.4
32	125.9	115.4
33	158.5	115.4
34	199.5	115.4

Figure 4.6: Calculation Results for CMRR

4.5 Power Consumption Calculation

Figure 4.7 presented the power consumption of the designed low-noise amplifier (LNA) utilizing chopper stabilization techniques. From the waveform, it is observed that the power consumption remains consistently low throughout the operating period, with a peak value of approximately 26.95 µW. This indicates that the amplifier is highly power-efficient, aligning well with the requirements of low-power analog front-end systems. The minimal variation in power consumption also reflects stable operation, suggesting that the chopper technique effectively mitigates flicker noise without introducing significant overhead. Overall, the result demonstrates that the implemented design achieves both low-noise performance and excellent power efficiency.

To further quantify the power efficiency of the designed low-noise amplifier, the average power consumption was calculated using the built-in calculator tool in Cadence Virtuoso as shown in Figure 4.8. By applying the expression “Average”, the simulation returned a consistent average power value of 17.8 µW. This result confirms that the amplifier not only achieves a low instantaneous power peak but also maintains an impressively low average power level across the entire transient simulation.

Figure 4.7: Power Consumption Simulation Results

Figure 4.8: Average Power Calculation

4.6 Post-Layout Simulation

Figure 4.9 shows the testbench setup for the chopper amplifier, utilizing the av_extracted view in Cadence Virtuoso. This confirms that the simulation is performed at the post-layout level, incorporating parasitic effects from the layout extraction process.

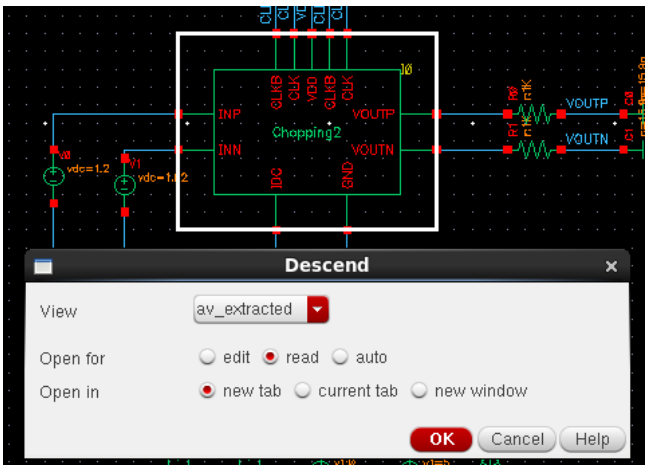

Figure 4.9: Post-Layout Simulation Setup

Figure 4.10 shows the post-layout transient responses. In comparing the pre-layout and post-layout simulation results of the chopper amplifier, it can be observed that both simulations produce consistent and stable output signals, indicating that the core amplifier design remains robust even after layout implementation. The pre-layout simulation shows an output voltage of approximately 1.802 V, while the post-layout simulation yields a very close

value of around 1.804 V. The slight deviation can be attributed to parasitic elements such as interconnect capacitances and resistances that are only present in the post-layout simulation. Additionally, both simulations demonstrate proper functionality of the chopping clock signals (CLK and CLKB), with consistent amplitude and frequency, confirming that the modulation-demodulation mechanism works as intended in both cases. This close alignment between pre-layout and post-layout results validates the design integrity and shows that the layout parasitics have minimal impact on the amplifier's overall performance.

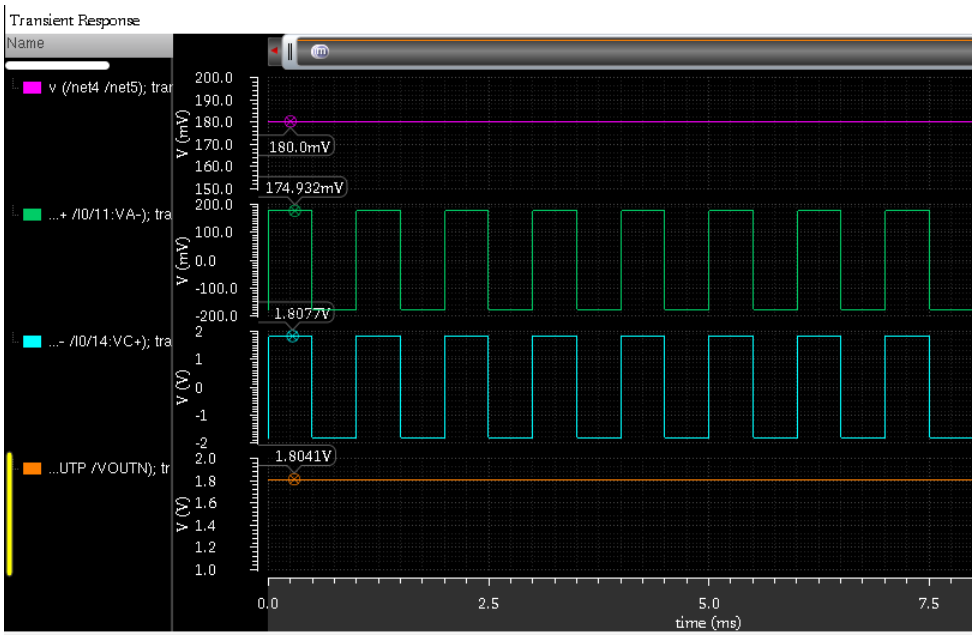

Figure 4.10: Post-Layout Simulation Results

4.7 Summary

In summary, the simulation results of the designed chopper-stabilized amplifier demonstrate its effectiveness in reducing low-frequency noise and enhancing overall performance. The amplifier achieved a gain of 10.01, which closely matches the required gain of 10.46, calculated based on the MS5803-14BA sensor's maximum output voltage of 0.2868 V and the ADC's full-scale input voltage of 3 V. The noise analysis indicates a significant improvement with the application of the chopper technique, achieving a input noise of 0.712369 µV, confirming the amplifier's suitability for low-noise applications such as MEMS pressure sensor interfacing.

Furthermore, the Common-Mode Rejection Ratio (CMRR) was calculated using Cadence Virtuoso by comparing the open-loop and closed-loop gains of the differential amplifier. The simulation yielded a CMRR of 115.4 dB, indicating excellent common-mode noise suppression. Post-layout simulation was performed using the av_extracted view to account for parasitic elements introduced during layout. The results show good agreement with the pre-layout simulation, with only minor variations in the output voltage. Additionally, the required bandwidth for the application was between 122 Hz and 2 kHz, and from the simulation results, the amplifier maintained a consistent CMRR of 115.4 dB across this frequency range. Lastly, the power consumption of this design achieved a consistent average power value of 17.8 µW. Overall, the combined analysis validates the robustness, high CMRR, low-noise performance, low power consumption and bandwidth compliance of the designed amplifier.

Compared to previous works, this design achieves a strong balance between power efficiency and noise performance. The design maintains a competitive input-referred noise of 0.712 µV and an excellent common mode rejection ratio of 115.4 dB, which is the highest among the compared works, as shown in Table 4.1. Although the power consumption are modest relative to other designs, the overall performance demonstrates an effective trade-off suited for low-power MEMS applications where noise rejection is critical.

Table 4.1: Comparison of Works

	Nebhen et al. (2011)	Choi et al. (2021)	Yoo et al. (2022)	**This work**
Techniques	Chopper stabilized	High pass filter	Multipath and AOCL	Chopper stabilized
Technology	0.35 µm	0.18 µm	0.18 µm	90 nm
Gain	26.5 dB	30.35 dB	44.14 dB	20.01 dB
Input Referred noise	0.194 nV	3.69 µV	14.6 nV	0.712 µV
Common Mode Rejection Ratio	26.5 dB	174 dB	100.7 dB	115.4 dB
Power Consumption	5 µW	19.4 µW	4.06 µW	17.8 µW

CHAPTER 5

CONCLUSIONS AND RECOMMENDATIONS

5.1 Conclusion

This project focused on the design and simulation of a low-noise chopper-stabilized amplifier intended for MEMS pressure sensor interfacing, specifically targeting the MS5803-14BA sensor. The main objective was to amplify the low-level sensor output signal while minimizing noise, preserving signal integrity, and ensuring compatibility with a high-resolution 24-bit ADC. The design was implemented and simulated using Cadence Virtuoso, leveraging the GPDK 90nm CMOS technology for layout, verification, and post-layout extraction.

The core of this design is the chopper stabilization technique, which plays a critical role in minimizing low-frequency flicker noise (1/f noise). The amplifier works by periodically modulating the low-frequency input signal to a higher frequency using a chopper switch, where the noise contribution is significantly lower. After amplification in this modulated domain, the signal is demodulated back to its original frequency, effectively shifting the noise out of the signal band. This approach enables the amplifier to maintain high accuracy and low noise performance, even with weak sensor signals.

Besides that, the key parameters, such as gain, low-pass filter cutoff frequency, and bandwidth, were specifically selected to align with the input range and resolution of a 24-bit ADC. The amplifier’s bandwidth was constrained to match the sensor's signal frequency range, and the gain was calibrated to ensure that the amplified output occupies the full input span of the ADC, thereby maximizing resolution and signal fidelity during digitization.

Beyond circuit-level functionality, the project also demonstrated competency in post-layout validation. The post-layout simulation results closely matched those from the schematic-level design, confirming the robustness of the design against parasitic effects.

Overall, the project achieved its core objectives by delivering a low-noise, precision amplifier. It is also compatible with the MS5803-14BA sensor

and suitable for integration into high-resolution pressure sensing systems. The results support its feasibility for real-world MEMS applications, particularly in underwater environments where reliable and noise-immune signal acquisition is critical.

5.2 Recommendations for Future Work

While the current design successfully demonstrates a functional and low-noise chopper-stabilized amplifier for the MS5803-14BA sensor, several enhancements can be explored in future iterations. One recommendation is to proceed with full-chip fabrication and silicon validation, allowing experimental verification of the simulated performance and identifying any discrepancies introduced during manufacturing. Additionally, the integration of auto-zeroing or offset cancellation circuits can further improve accuracy and stability over time and temperature.

To support broader application scopes, future designs may also consider adaptive gain control to accommodate sensors with varying output ranges. Expanding the system to include a fully integrated analog-to-digital converter (ADC) on-chip would streamline signal processing and reduce external dependencies. Lastly, migrating the design to a more advanced CMOS technology node could yield benefits in power efficiency, area reduction, and performance, making it more suitable for compact and low-power embedded systems.

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