DESIGN AND IMPLEMENTATION OF AN NMOS-BASED LOW DROPOUT REGULATOR WITH INTEGRATED CHARGE PUMP FOR SOC APPLICATIONS

LIEW JIN WEI

UNIVERSITI TUNKU ABDUL RAHMAN

DESIGN AND IMPLEMENTATION OF AN NMOS-BASED LOW DROPOUT REGULATOR WITH INTEGRATED CHARGE PUMP FOR SOC APPLICATIONS

LIEW JIN WEI

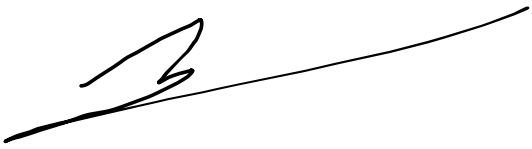
A project report submitted in partial fulfilment of the requirements for the award of Bachelor of Electronic Engineering

Faculty of Engineering and Green Technology
Universiti Tunku Abdul Rahman

May 2026

DECLARATION

I hereby declare that this project report is based on my original work except for citations and quotations which have been duly acknowledged. I also declare that it has not been previously and concurrently submitted for any other degree or award at UTAR or other institutions.

Signature : 

Name : Liew Jin Wei

ID No. : 2201897

Date : 6th of May 2026

APPROVAL FOR SUBMISSION

I certify that this project report entitled **"DESIGN AND IMPLEMENTATION OF AN NMOS-BASED LOW DROPOUT REGULATOR WITH INTEGRATED CHARGE PUMP FOR SOC APPLICATIONS"** was prepared by **LIEW JIN WEI** has met the required standard for submission in partial fulfilment of the requirements for the award of Bachelor of Electronic Engineering with Honours at Universiti Tunku Abdul Rahman.

Approved by,

Signature	:	
Supervisor	:	Tan Yee Chyan
Date	:	10/5/2026

ACKNOWLEDGEMENTS

I would like to express my deepest gratitude to my supervisor, Tan Yee Chyan, for his invaluable guidance, continuous support, and insightful feedback throughout this final year project. My sincere appreciation also goes to my onsite supervisor, Lai Li Fang, for her practical mentorship and technical direction, which greatly facilitated my work on this NMOS-based low-dropout (LDO) regulator design. Additionally, I would like to thank all my colleagues for their shared knowledge, assistance, and encouragement. This project would not have been possible without your collective support.

Lastly, I want to express my deepest gratitude to my parents and my sister for their unwavering love, patience, and understanding. Navigating the final stages of my engineering degree and completing this project would have been immensely difficult without their constant emotional support, encouragement, and the sacrifices they have made for my education.

DESIGN AND IMPLEMENTATION OF AN NMOS-BASED LOW DROPOUT REGULATOR WITH INTEGRATED CHARGE PUMP FOR SOC APPLICATIONS

ABSTRACT

This project presents the design and implementation methodology of a low-dropout regulator (LDO) employing an NMOS pass transistor, targeted for low-voltage and low-power system-on-chip (SoC) applications. Conventional PMOS-based LDOs suffer from large area requirements and limited transient response. While NMOS-based regulators are more area-efficient, they require a boosted gate drive at low supply voltages. To address this challenge, a charge pump was integrated into the design to provide sufficient gate overdrive. A cross-coupled charge pump and a folded-cascode operational amplifier (op-amp) were developed and compared in terms of boosting efficiency, load capability, and noise injection. The LDO utilizes the designed folded-cascode error amplifier, which can provide high gain under typical process corners. The regulator was specified to deliver a maximum load current of 5 mA with a stable output voltage of 1.2 V, while maintaining a power supply rejection ratio (PSRR) of at least –20 dB across the operating range. Comprehensive simulations were carried out in Silterra 130 nm CMOS technology using thick-oxide devices, with process and temperature corners spanning from –40 °C to 125 °C. The design methodology demonstrates how combining NMOS pass devices with efficient charge pump boosting and low-power Operational Transconductance Amplifier (OTA) architectures can achieve robust regulation, low quiescent current, and a wide operating voltage range, making the proposed LDO suitable for modern SoC and IoT applications.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF APPENDIXES

LIST OF SYMBOLS / ABBREVIATIONS

g_m	transconductance of transistor, S
r_o	output resistance of transistor, Ω
t_{rise}	rise time, s
t_{fall}	fall time, s
V_{GS}	gate to source voltage of transistor, V
V_{DS}	drain to source voltage of transistor, V
V_{TH}	threshold voltage of transistor, V
V_{DD}	supply voltage, V
IoT	Internet of Things
Op-amp	Operation Amplifier
OTA	Operation Transconductance Amplifier
PSRR	Power Supply Rejection Ratio, dB
SoC	System on Chip

CHAPTER 1

INTRODUCTION

1.1 General Introduction

The Internet of Things (IoT) has rapidly become one of the most transformative technologies in recent years, connecting billions of devices worldwide. From smart homes and wearable health monitors to industrial automation and transportation, IoT enables real-time data exchange and intelligent decision-making across diverse sectors. Its rapid expansion is driven by advances in wireless communication, low-power electronics, and cloud computing, making it a key driver of innovation in modern society (Gokhale et al., 2018).

Power management circuits are essential in modern electronic systems as the demand for high integration, energy efficiency, and reliable operation continues to grow. Devices such as smartphones, wearables, IoT nodes, automotive systems, and communication equipment all require stable voltage supplies to ensure the correct functionality of digital, analog, and RF subsystems. To address this need, power management integrated circuits (PMICs) incorporate various regulation techniques, with low-dropout regulators (LDOs) being one of the most widely used solutions (Chyan et al., 2022).

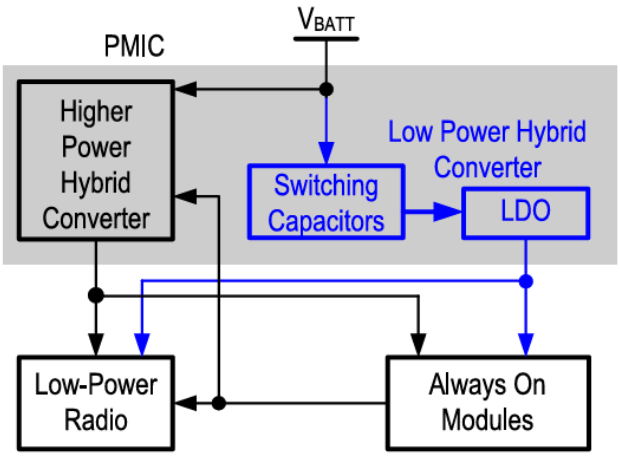


Figure 1.1: PMIC for IoT Applications (Chyan, et al., 2022)

As shown in Figure 1.1, the power management of the system-on-chip (SoC) module is essential for IoT applications, supplying power to other blocks with various voltage and current requirements. Compared to other DC-to-DC converters, a low-dropout regulator (LDO) is a linear regulator typically placed at the output stage of the PMIC.

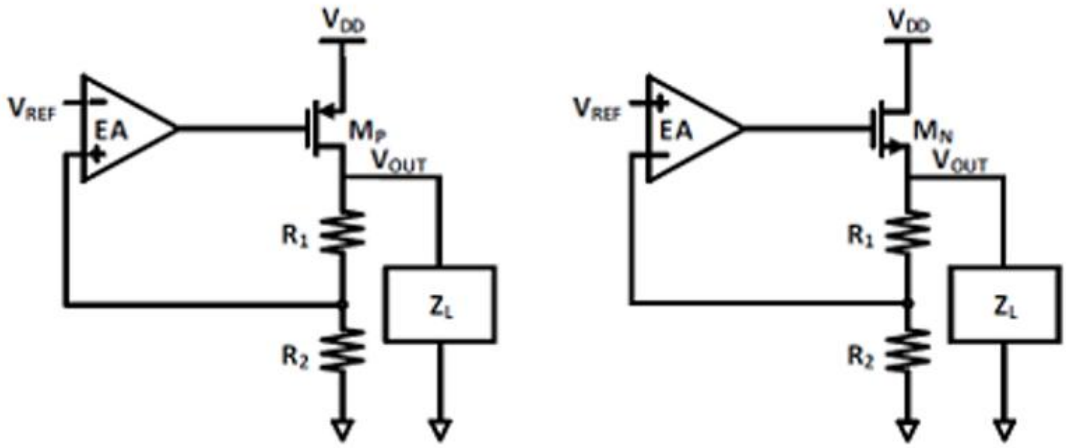
LDOs are linear regulators that provide a stable output voltage even when the input voltage is only slightly higher than the output voltage, typically maintaining a dropout voltage between 50 mV and 200 mV (Chyan et al., 2022). They are preferred in many applications due to advantages such as low noise, simple implementation, fast transient response, and small silicon area (H. Kamel et al., 2019). These properties make them suitable for noise-sensitive circuits, including RF front-ends, ADCs, and mixed-signal systems. LDOs are also used as post-regulators after switching converters to suppress ripple and improve supply quality.

Recent industrial developments have focused on improving LDO performance to meet evolving requirements. Portable devices need ultra-low quiescent current regulators to extend battery life, while automotive and industrial uses require LDOs with wide input ranges, robustness, and high reliability. At the same time, integrating multiple power domains in SoC designs has increased the need for on-chip LDOs for localized supply regulation and noise isolation (Chyan et al., 2022). These demands

highlight the importance of constant innovation in LDO architectures and design strategies.

1.2 Problem Statements

Compared to switching regulators, an LDO provides a stable power supply to other blocks in the SoC while occupying a smaller active area. This is due to the fewer capacitors and inductors required, thereby reducing the overall footprint of the PMIC.



(a) (b)

Figure 1.2: Main Topologies of LDO (a) PMOS pass transistor (b) NMOS pass transistor (H. Kamel et al., 2019)

As illustrated in Figure 1.2, there are two main LDO topologies: the PMOS pass transistor in Figure 1.2(a) and the NMOS pass transistor in Figure 1.2(b). The PMOS pass transistor topology behaves like a common-source amplifier, while the NMOS pass transistor topology behaves like a common-drain amplifier (source follower). PMOS designs typically possess at least two low-frequency poles—one at the pass-transistor gate and another at the LDO output—which can cause stability issues and often require Miller compensation.

Conversely, an LDO with an NMOS pass transistor provides lower output resistance and inherently better stability. While its transconductance increases with the load current (H. Kamel et al., 2019), it generally yields lower parasitic gate capacitance and resistance, improving transient response and reducing chip area. Consequently, the smaller parasitic gate capacitance of the NMOS transistor enhances the response time of the regulator (Yan et al., 2016). In short, NMOS-type LDOs offer higher transconductance and lower on-resistance than their PMOS equivalents, improving power supply noise rejection for noise-sensitive blocks.

However, several design challenges exist in NMOS LDO topologies. The primary downside is the source-follower configuration, where the gate voltage must exceed the output voltage by at least the threshold voltage. To maintain low dropout voltage, the gate must be driven above the input rail, typically requiring an on-chip charge pump or a boosted gate drive (Yan et al., 2016). While a charge pump increases voltage, it introduces design complexity, static power consumption, and switching noise. NMOS LDOs also tend to have a lower Power Supply Rejection Ratio (PSRR) than PMOS counterparts because the output node is less isolated from supply noise. Furthermore, although the low output impedance of the NMOS device can shift the dominant pole to higher frequencies—thereby improving loop stability—compensation can still be complex.

To ensure efficient gate boosting, a clean and accurate clock signal is required. This clock is usually obtained from an oscillator, and a well-designed clock circuit is critical to charge pump efficiency. Utilizing circuits such as a single-to-differential converter (SDC) or a level shifter can reduce rise and fall times, providing a sharp clock signal that allows the charge pump to deliver sufficient voltage to the error amplifier.

With voltage downscaling, circuits become increasingly noise sensitive. Achieving a high PSRR, wide stability margins, and robust performance under process, voltage, and temperature (PVT) variations is progressively difficult. Balancing these requirements while maintaining low dropout voltage and energy efficiency remains the central challenge in modern LDO design.

1.3 Aims and Objectives

The primary aim of this report is to design and implement a low-dropout (LDO) regulator using an NMOS pass transistor, addressing the limitations of conventional approaches while meeting the performance requirements of modern applications. The specific objectives are as follows:

- To design and simulate a multi-voltage NMOS-based LDO regulator capable of delivering a stable 1.2 V output and driving a maximum load current of 5 mA across input supply voltages of 1.8 V, 2.5 V, and 3.3 V.
- To develop an integrated charge pump (CP) architecture that generates an elevated supply voltage for the error amplifier to ensure sufficient gate overdrive.
- To implement a robust, isolated 1.2 V clock generation and conditioning domain to drive the charge pump efficiently.
- To evaluate the output noise and power supply rejection ratio (PSRR) performance across process and temperature variations.

1.4 Flowchart of Research Activity

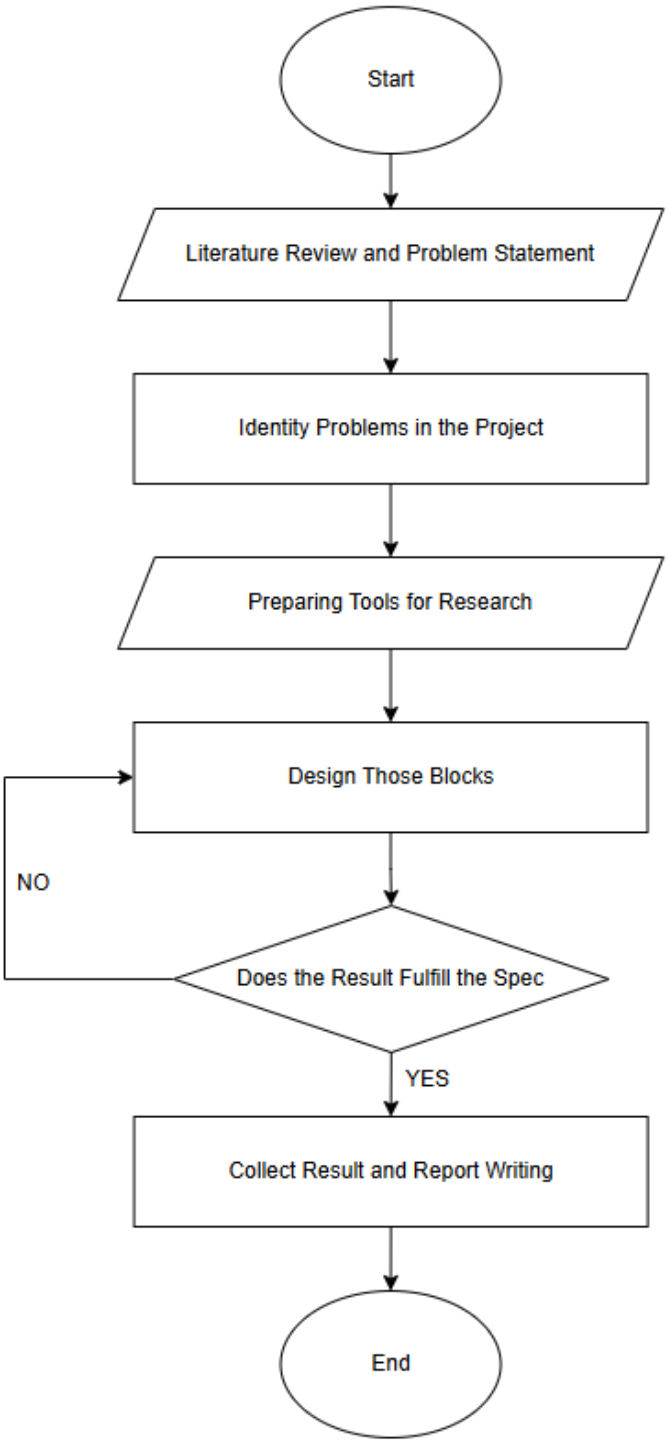


Figure 1.3: Flow chart of Research Methodology

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

With the growing popularity of portable devices and IoT systems, low-dropout (LDO) regulators have become essential for delivering stable, low-noise supply voltages. Research on LDO design has explored various pass devices, error amplifier topologies, and frequency compensation methods to balance power, area, and stability. Charge pump circuits are also critical for NMOS-based LDOs operating at low supply voltages, as they ensure sufficient gate-drive voltage. This chapter provides a review of prior work on LDO architectures, operational transconductance amplifier (OTA) designs, and charge pump topologies, highlighting their trade-offs and relevance to this project.

2.2 Low Dropout Regulator (LDO) Design

Low-dropout (LDO) regulators are linear voltage regulators designed to provide a stable, regulated output voltage even when the input voltage is only slightly higher than the output voltage. As shown in Figure 2.1, they typically consist of three core blocks: a pass transistor (PMOS or NMOS), an error amplifier, and a feedback network. The error amplifier (EA) compares the feedback voltage with a reference voltage (V_{ref}) and adjusts the gate of the pass transistor to maintain regulation. LDOs are widely used in mixed-signal and RF systems because of their low noise and fast transient response. They play a critical role in ensuring that sensitive analog circuits and processors

receive a clean power supply, free from voltage ripple and disturbances from switching converters (Chyan et al., 2022).

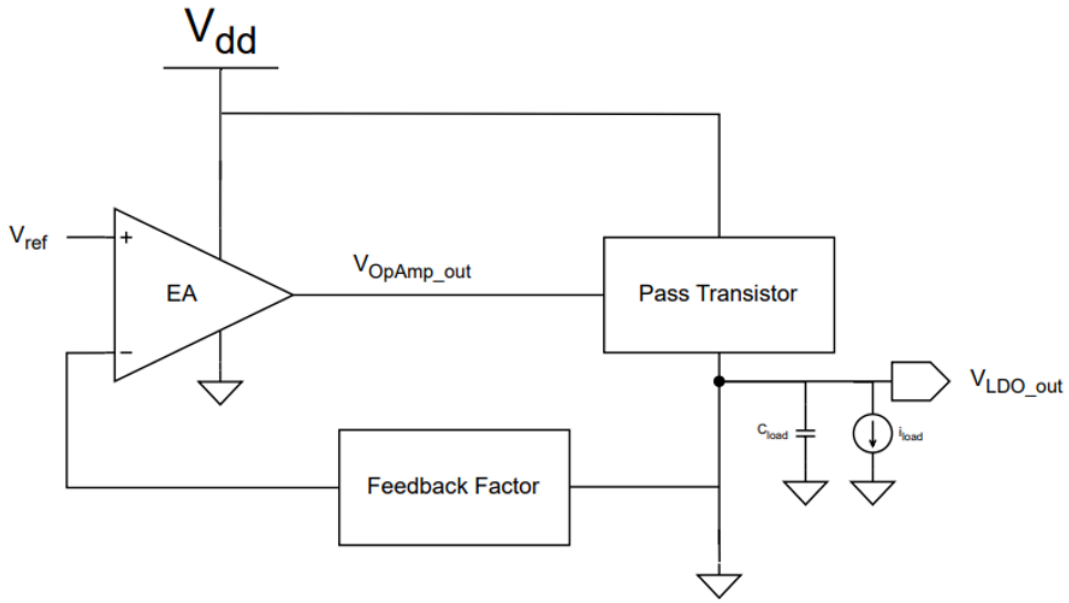


Figure 2.1: Block Diagram of LDO

Furthermore, the feedback factor and the polarity of the feedback system depend on the type of pass transistor employed. A PMOS transistor requires a low gate voltage to turn on; therefore, the error amplifier (EA) must be capable of swinging its output toward the lower voltage rail. Conversely, an NMOS pass transistor requires a high gate voltage to turn on. To operate in the saturation region, the conditions in Equation (2.1) must be satisfied (Yao, 2023). If the supply voltage (V_{DD}) of the error amplifier is lower than the sum of the output voltage and the threshold voltage (V_{TH}), the pass transistor cannot operate in saturation region. A charge pump is therefore integrated to provide the necessary gate overdrive voltage.

$$|V_{DS}| \geq |V_{GS}| - |V_{TH}| \tag{2.1}$$

where

V_{GS} = gate to source voltage of the transistor, V

V_{DS} = drain to source voltage of the transistor, V

V_{TH} = threshold voltage of the transistor, V

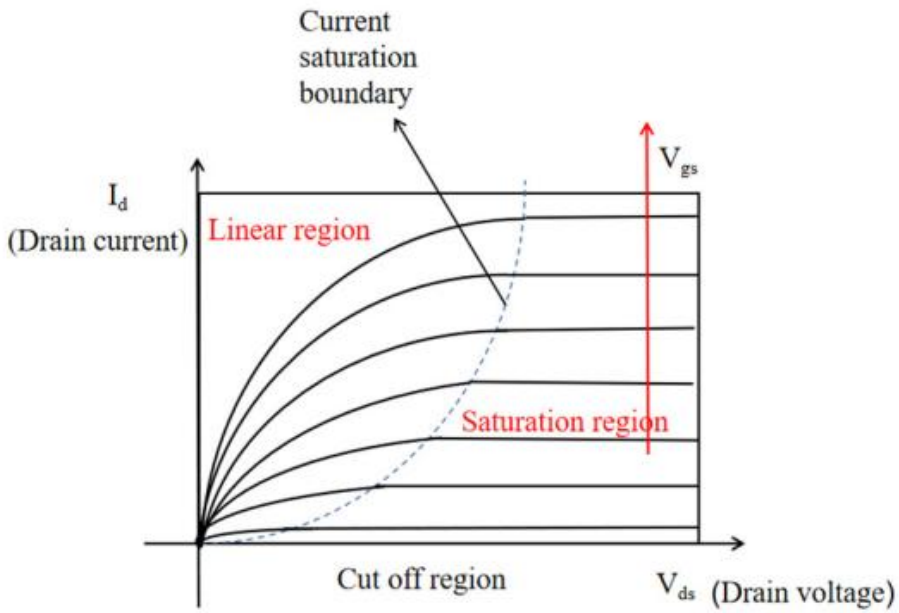


Figure 2.2: Output Characteristic of MOSFET (Yao, 2023)

2.2.1 LDO Design Parameter

To design an LDO, which is one of the most suitable linear regulators and widely used in the Power Management Integrated Circuit (PMIC), some parameters need to be calculated and considered. The following parameters are most critical in LDO regulator design.

Dropout Voltage (V_{DO}) is one of the important parameters in designing the LDO, which is interconnected with the system parameter, dropout performance and device parameter. In detail, the system parameter will affect the LDO's dropout performance, which in turn influences other device parameters. The dropout voltage is the difference between the input/supply voltage to the LDO and the output voltage. (Chyan, et al., 2022)

$$V_{DO} = I_{LOAD} * R_{DS} \tag{2.2}$$

where

V_{DO} = dropout voltage of the LDO, V

I_{LOAD} = load current of the pass transistor, A

R_{DS} = drain to source resistance of the transistor, **Ω**

The V_{DO} can be defined as the multiplication of load current (I_{LOAD}) and drain to source resistance (R_{DS}) of the pass transistor, as shown in Equation (2.2). (Bhuiyan, et al., 2022)

Quiescent Current (I_Q) is the current consumed by the LDO, which is also the difference between the input and output current. To ensure the LDO functioning, the input current needs to supply the internal circuitry in the LDO such as the EA and output voltage divider, serving as the feedback network of the LDO (Bhuiyan, et al., 2022). It can be expressed as:

$$I_Q = I_{IN} - I_{OUT} \tag{2.3}$$

where

I_Q = quiescent current of the LDO, A

I_{IN} = input current of the LDO, A

I_{OUT} = output current of the LDO, A

Line Regulation is the parameter determining how well the LDO maintains a specific output voltage as the input voltage changes. It can be defined as:

$$Line\ Regulation\ = \Delta V_{OUT} / \Delta V_{IN} \tag{2.4}$$

where

V_{IN} = input voltage of the LDO, V

V_{OUT} = output voltage of the LDO, V

Load Regulation is the parameter determining how well the LDO in maintaining a particular output voltage across a range of output currents under each simulation conditions. It can be expressed as:

$$Load\ Regulation\ = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \tag{2.5}$$

Power Supply Rejection Ratio (PSRR) is the parameter indicating the ability of the LDO in suppressing the noise from the input to the output. An LDO with good PSRR can minimize the noise from the input signal (Bhuiyan, et al., 2022).

$$PSRR(dB) = 20\log_{10}(\frac{\Delta V_{OUT}}{\Delta V_{IN}}) \quad (2.6)$$

where

$PSRR$ = power supply rejection ratio of the LDO, dB

2.2.2 Advantages of PMOS Pass Transistor

When comparing the PMOS and NMOS as the pass transistor used in the LDO, the lower source to drain saturation voltage in a PMOS pass transistor type of LDO can achieve lower V_{DO}, typically in the range of 50 mV to 200 mV, while the NMOS pass transistor type of LDO needs a higher V_{GS} to drive the NMOS transistor operating in saturation region, resulting in higher V_{DO}, typically in the range of 300 mV to 800 mV (Yao, 2023).

Furthermore, a PMOS pass transistor type LDO does not require additional driving circuit to drive the EA, resulting in simplicity for the schematic design.

2.2.3 Advantages of NMOS Pass Transistor

However, PMOS transistor has a higher drain to source on resistance ($R_{DS(ON)}$) and slower switching speed. Hence, to achieve the same switching speed with NMOS pass transistor, PMOS pass transistor needs to be larger in terms of gate dimensions which also increases the sizing and active chip area.

NMOS pass transistor LDO regulator functions as a common drain amplifier circuit, which has lower output impedance, better PSRR and often better load regulation, whereas PMOS pass transistor LDO regulator functions as a common source amplifier, which has a higher loop gain, but suffering in terms of bandwidth. Hence, with the smaller gate capacitance and low output resistance in NMOS pass transistor LDOs, stability is improved (Chyan, et al., 2022).

2.3 LDO Performance Review

The continuous developments of the SoC and IoT technology demand stronger performance for PMIC to have a stronger driving capability and lower noise. Thus, many researchers have proposed various architectures and topologies of LDO to address the demands. Different LDO topologies yield varying performance results, especially regarding stability, transient response, and power supply rejection. By focusing on these parameters of performance and trade-offs between them, different reported works have various performance enhancements for their designed LDO.

2.3.1 NMOS LDO Designed with Folded Cascode Error Amplifier

According to the research by H. Kamel et al. in 2019, using the standard 130 nm CMOS technology, both LDOs were designed to provide an output voltage of 1 V with a 1.2 V input voltage. Furthermore, the load current range of the designed LDO was limited to 30 µA to 100 mA, with a load capacitor up to 5 µF. In addition to the LDO architectures, this work also evaluates three different topologies of charge pump: Dickson, bootstrapped, and cross-coupled, used to raise the supply voltage from 1.2 V to 2 V, while supporting the maximum load current of 5 µA.

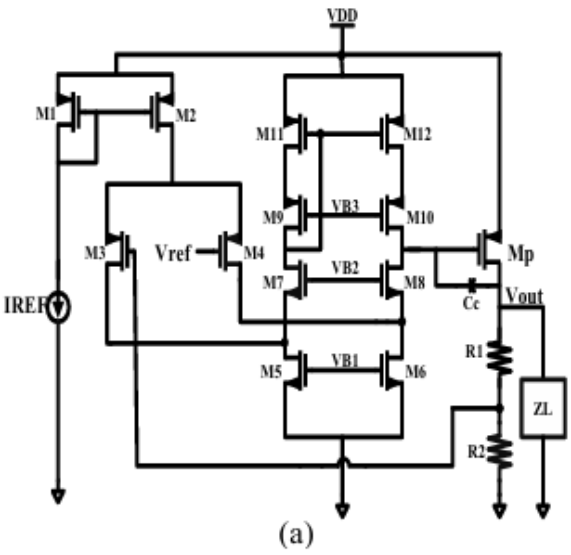


Figure 2.3: Transistor Level Architectures of PMOS-based LDO (H. Kamel et al., 2019)

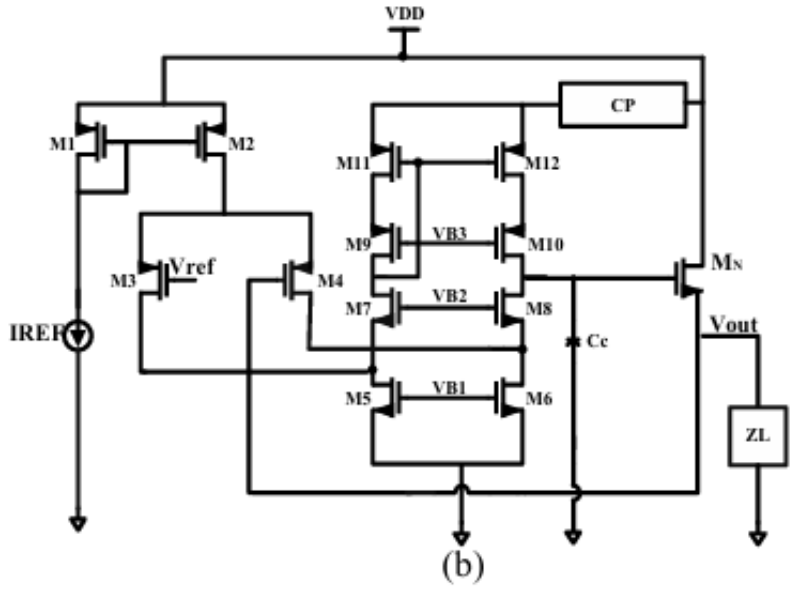


Figure 2.4: Transistor Level Architectures of NMOS-based LDO (H. Kamel et al., 2019)

Figures 2.3 and 2.4 illustrate the PMOS and NMOS-based LDO architectures. Both architectures use the same op-amp architecture, the folded-cascode error amplifier, which affects the LDO's noise rejection. Compared to PMOS-based LDOs, NMOS-based LDOs require a charge pump to address the critical issue of high gate-driving voltage required by the pass transistor.

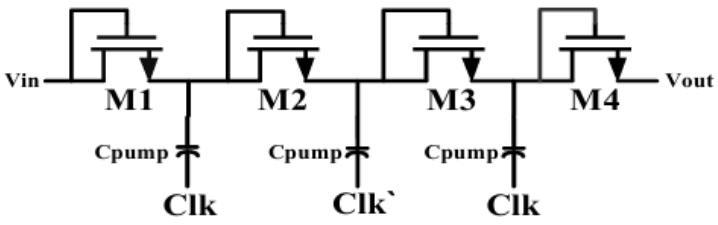


Figure 2.5: Dickson Charge Pump based on MOS (H. Kamel et al., 2019)

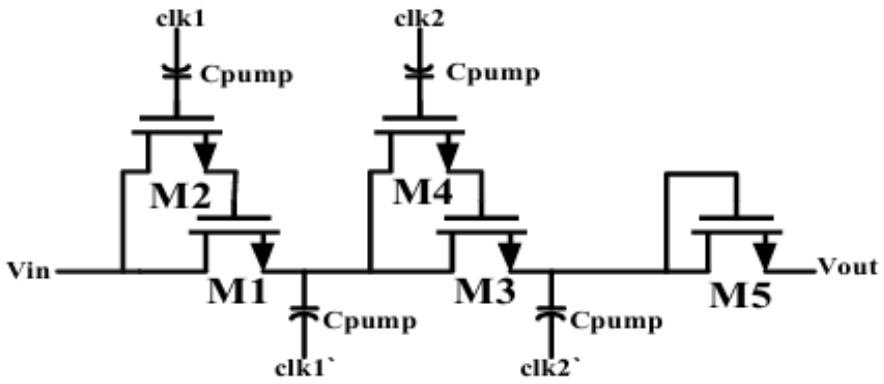


Figure 2.6: Bootstrapped Charge Pump based on MOS (H. Kamel et al., 2019)

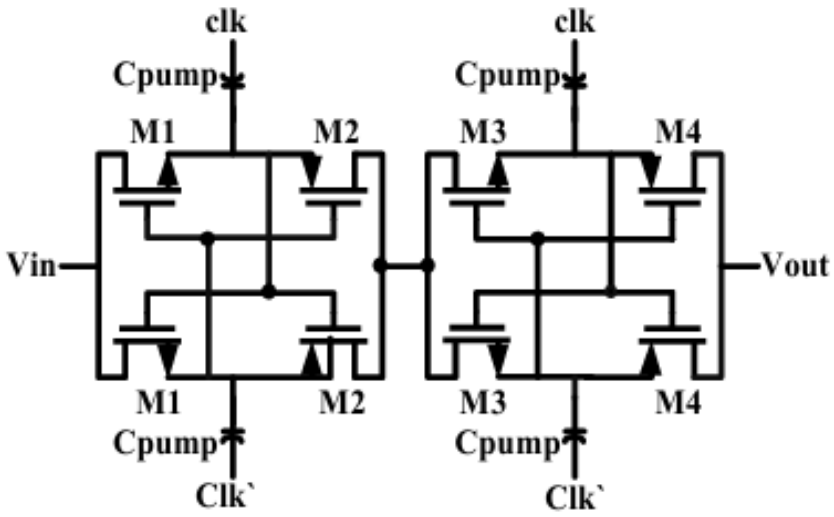


Figure 2.7: Cross-Coupled Charge Pump based on MOS (H. Kamel et al., 2019)

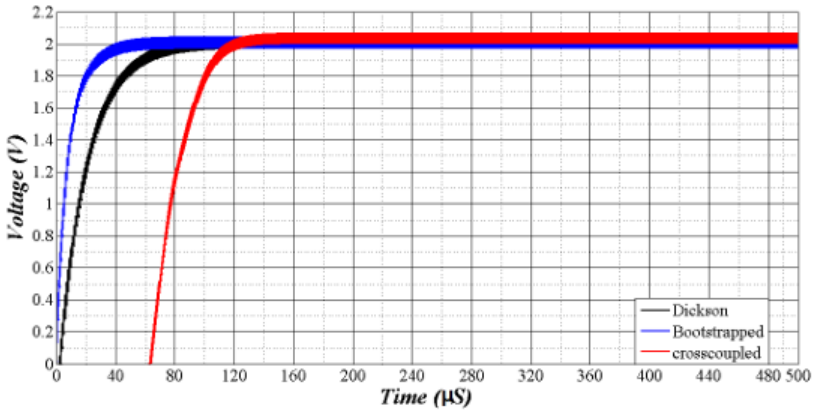


Figure 2.8: Transient Response of Three Charge Pump Architectures Using a Load Capacitor of 50 pF (H. Kamel et al., 2019)

In terms of the transient response of three charge pump topologies, the startup time for bootstrapped, Dickson's and cross-coupled are 43.95 µs, 80 µs and 108 µs, respectively. In short, bootstrapped has the best performance in terms of startup time, also known as the rise time, allowing the LDO to stabilize faster while the load current changes.

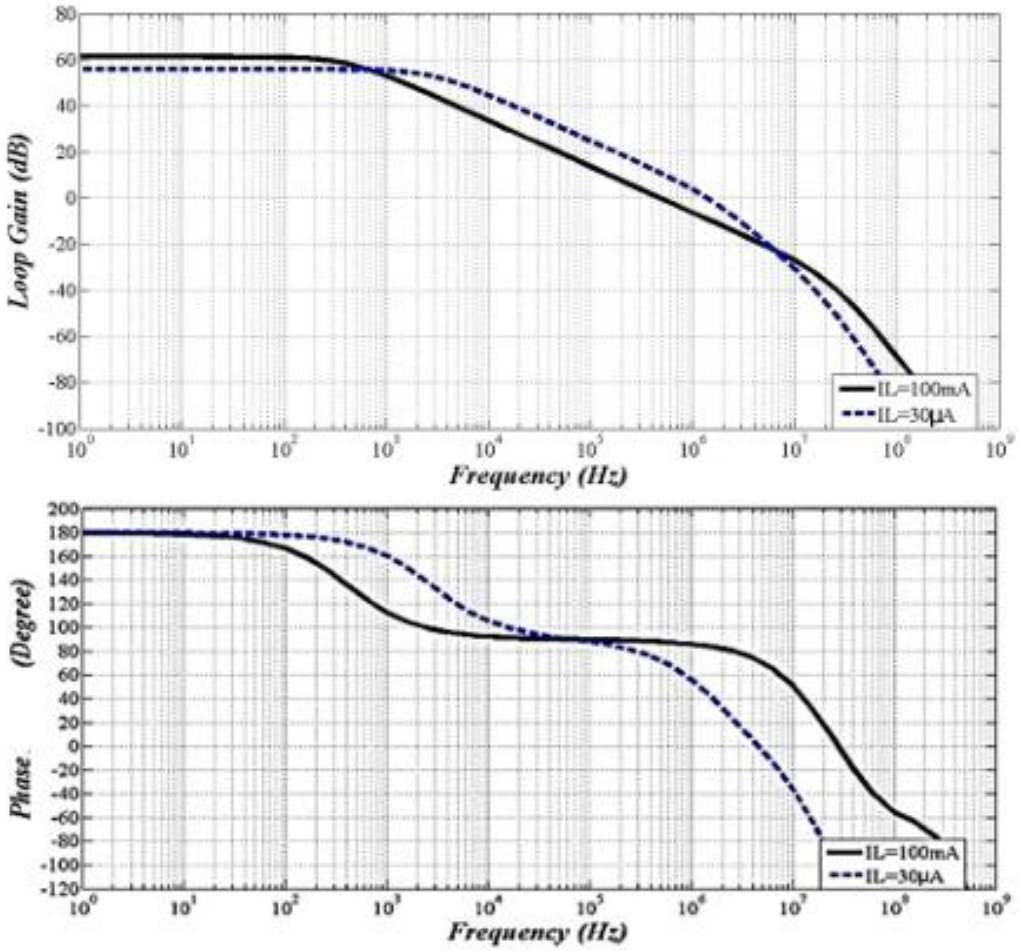


Figure 2.9: Simulated Loop Gain and Loop Phase of PMOS-based LDO (H. Kamel et al., 2019)

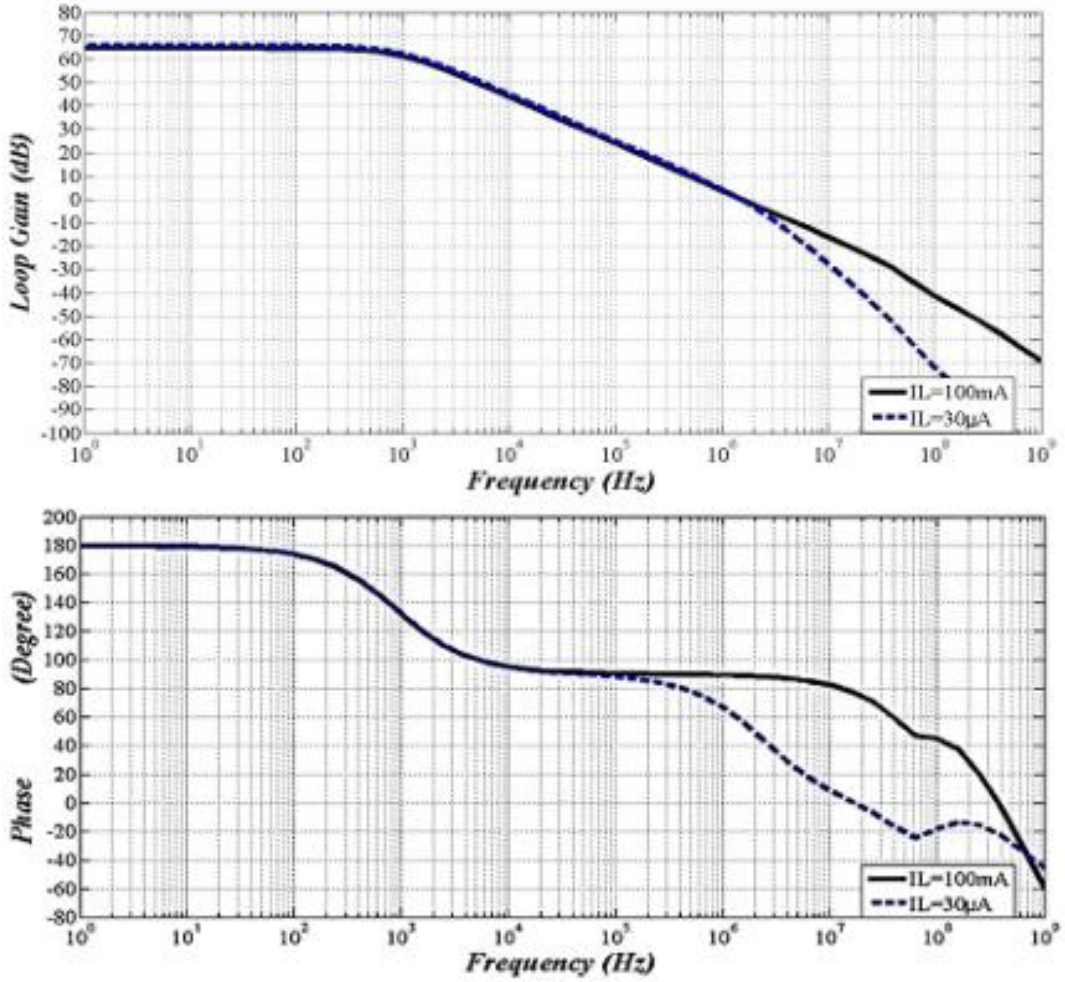


Figure 2.10: Simulated Loop Gain and Loop Phase of NMOS-based LDO (H. Kamel et al., 2019)

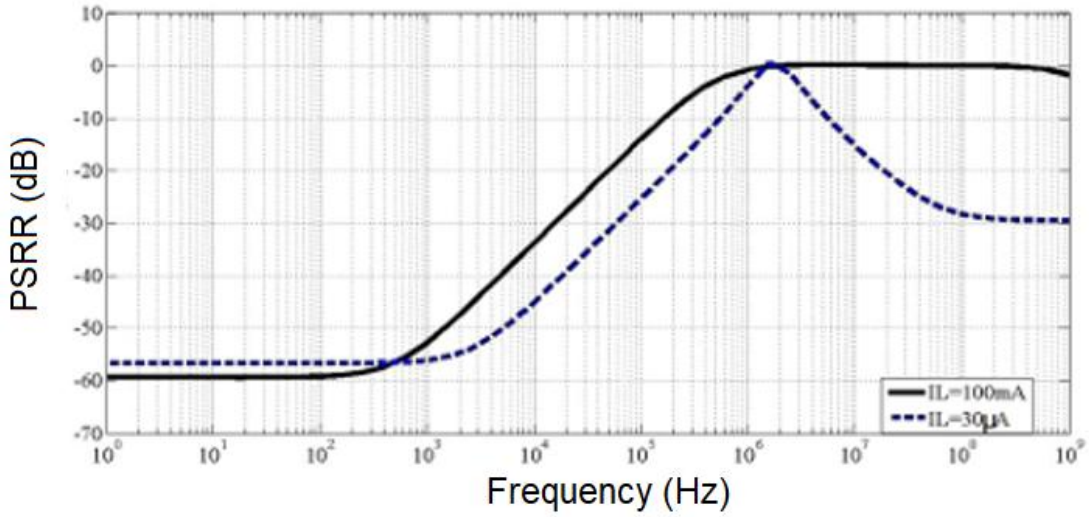


Figure 2.11: PSRR Result at light and high load current for PMOS-based LDO (H. Kamel, et al., 2019)

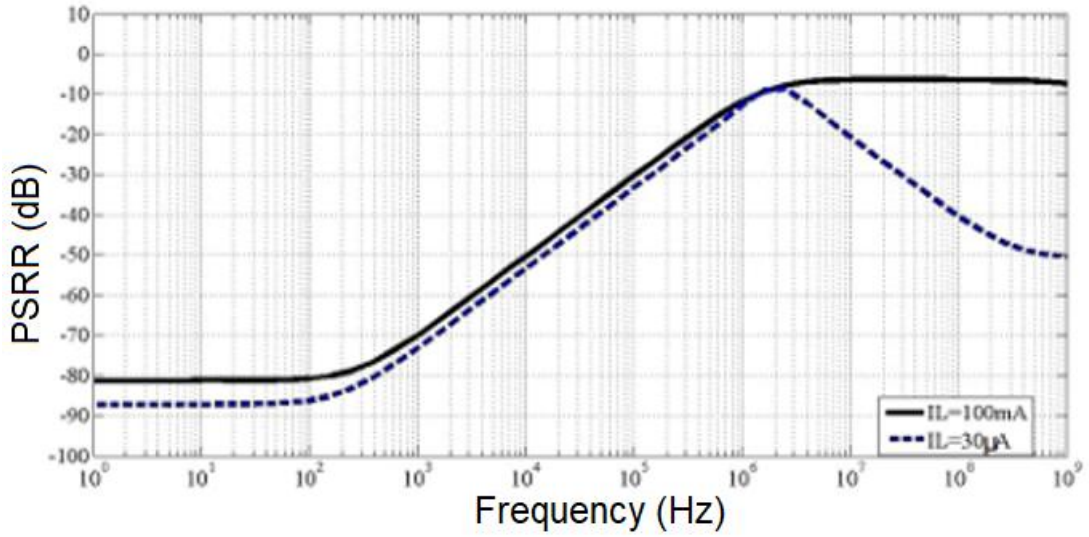


Figure 2.12: PSRR Result at light and high load current for NMOS-based LDO (H. Kamel, et al., 2019)

The loop gain and phase margin for the worst-case load capacitance of 50 pF are shown in Figure 2.9 and Figure 2.10. For the PMOS-based LDO, the loop gain and phase margin are 55.9 dB and 46º at light load (30 µA), and 61 dB and 88.1º at high

load current (100 mA). In comparison, the NMOS-based LDO has better performance, achieving a loop gain of 65.7 dB and a phase margin of 57.3° at a light load current (30 μA). At a high load current (100 mA), the loop gain and phase margin are 64.7 dB and 88.8º, respectively, for the designed NMOS-based LDO. This stability performance delivers a better PSRR for the NMOS-based LDO, achieving -53.2 dB at a light load current (30 μA) and -50.3 dB at a high load current (100 mA) at 100 kHz. Meanwhile, the PSRR of the PMOS-based LDO at 10 kHz is –45 dB (light load current 30 μA) and –33.6 dB (full load current 100 mA).

In summary, H. Kamel et al. (2019) demonstrated that the NMOS-based LDO outperformed the PMOS-based LDO in PSRR, despite using the same folded cascode error amplifier topology. Hence, the findings by H. Kamel et al. (2019) confirm the advantages of the NMOS pass transistor in noise rejection.

2.3.2 Low-Dropout Linear Regulator Design with Bandgap and Power Regulator

In the work by Xu and He (2020), an LDO was designed with the process technology of Shanghai Huali Integrated Circuit Corporation (HLMC) 40 nm, operating at a supply voltage of 2.5 V. In this work, the critical performance factors of LDO in circuit level such as startup overshoot, loop stability and PSRR were discussed, and opinions for the trade-off inherent in high performance regulator design were provided.

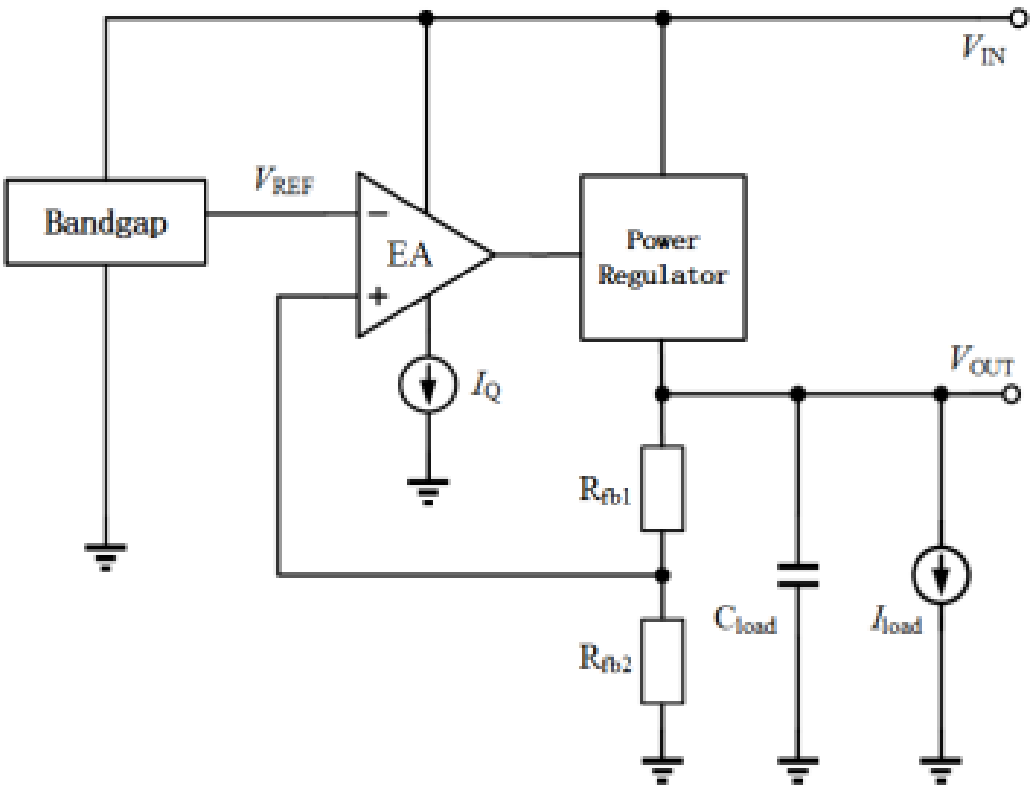


Figure 2.13: Circuit Structure of LDO by Xu and He (2020)

Figure 2.13 illustrates a full LDO structure, that requires a bandgap reference, error amplifier and power regulator, also known as pass transistor. Bandgap reference circuit was used to generate a temperature independent reference voltage (V_{REF}). The feedback network samples the output voltage, the error amplifier compares the feedback voltage and V_{REF}, providing an error signal which modulates the gate voltage for the power regulator to maintain the stability of the output voltage while the load is changing.

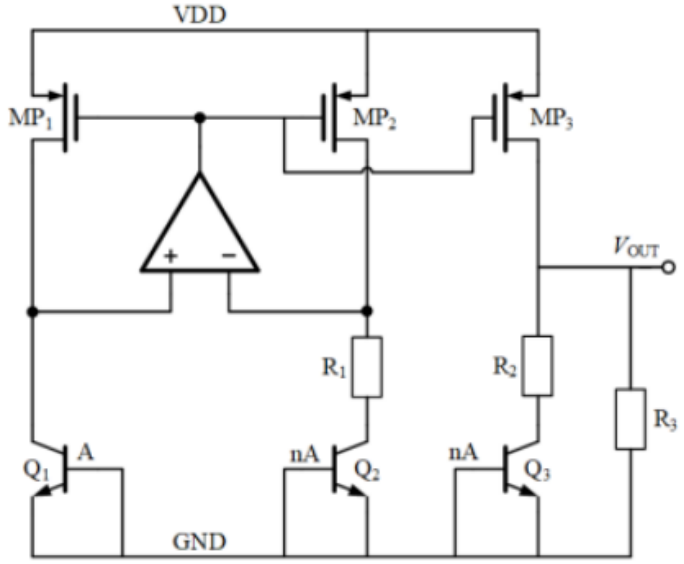


Figure 2.14: Schematic of Bandgap Reference by Xu and He (2020)

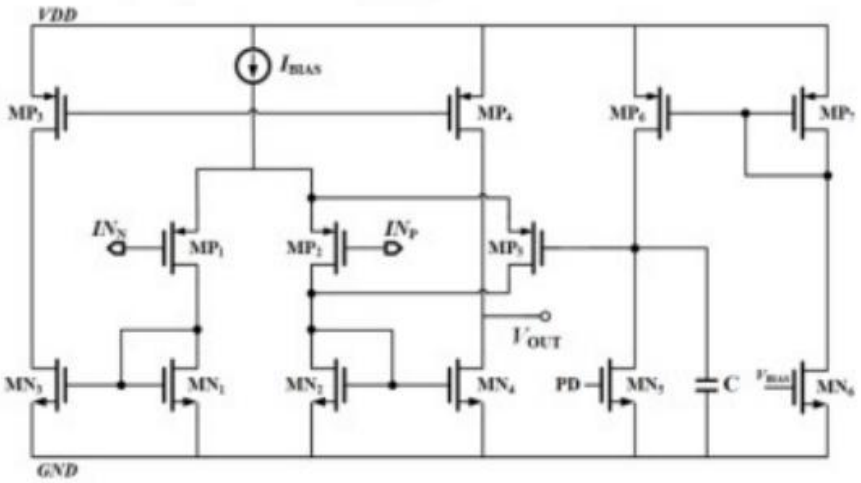


Figure 2.15: Schematic of Error Amplifier by Xu and He (2020)

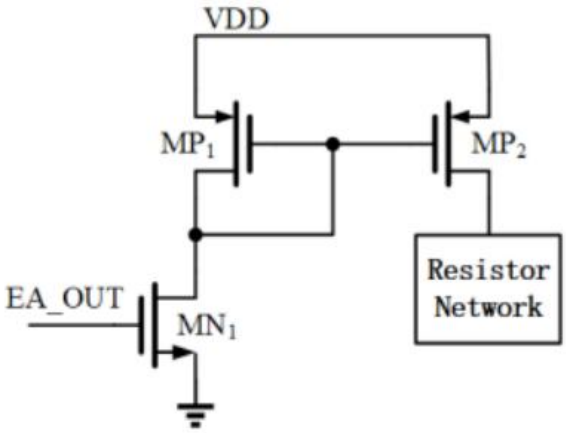


Figure 2.16: Schematic of Power Regulator by Xu and He (2020)

A two-stage error amplifier was proposed in this work, as illustrated in Figure 2.15, introducing an input cascode structure to reduce the influence of parasitic capacitance from the two input PMOS transistors on the first output pole. Besides, this cascaded structure can enhance PSRR performance by shifting the poles to higher frequencies, thereby improving overall stability. A basic current mirror was used as a load, improving the output voltage margin.

The bandgap reference, shown in Figure 2.14, produces a DC reference voltage for the op-amp that is independent of temperature and process variations by combining a certain propagation factor, positive and negative temperature coefficients, and a voltage. The last block of the designed LDO is the power regulator, which consists of the pass transistor shown in Figure 2.16, serving as the critical block for the LDO's overall performance and affecting the stability and driving capability of the LDO's output stage.

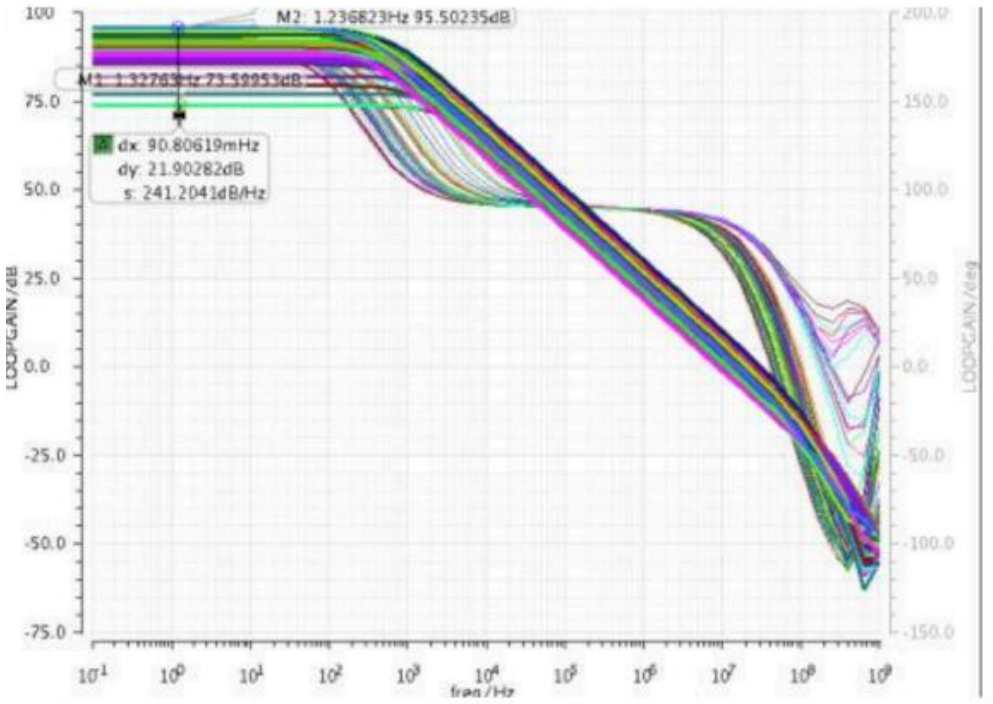


Figure 2.17: Simulation Result of Gain and Phase Response (Xu & He, 2020)

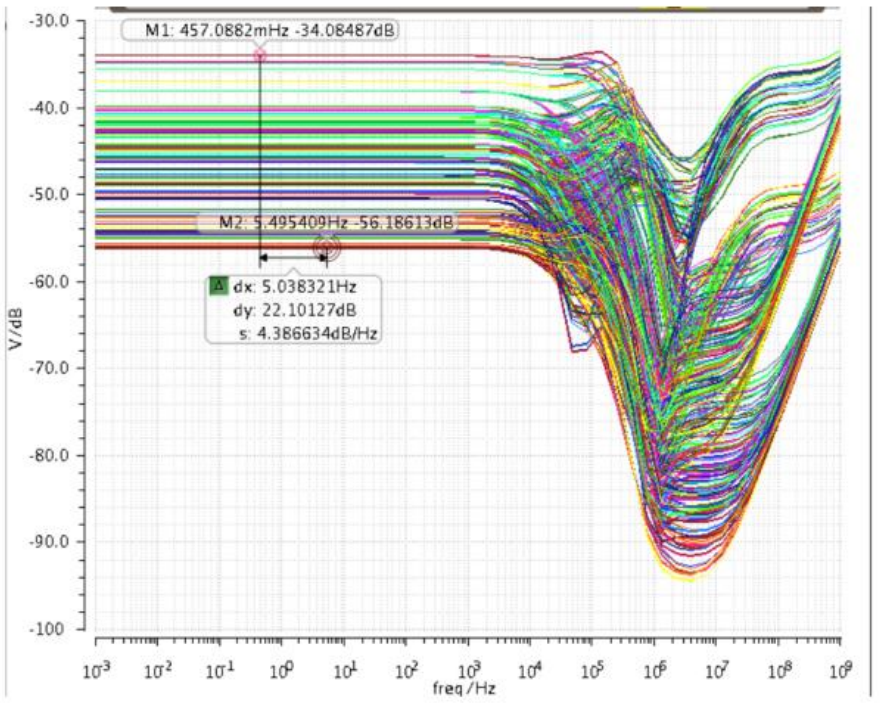


Figure 2.18: Simulation Result of PSRR (Xu & He, 2020)

The simulation results for the LDO proposed by Xu & He (2020) are shown in Figures 2.17 and 2.18, which present the gain and phase response and the PSRR performance of the circuit. From Figure 2.17, the loop gain performance is in the range of 73.7 dB to 95.5 dB, with a minimum phase margin of 57.7º and a maximum phase margin of 79º across all simulation conditions, including temperature, load, and process corners. Furthermore, the designed LDO has the worst-case PSRR of -35 dB. These results confirm the stability of the designed LDO in all conditions.

In short, Xu and He successfully designed an LDO regulator that balances factors such as area, stability, driving capability, and noise suppression, while supporting a load current of 10 mA. By controlling each block in the LDO, integrating an overshoot circuit, and optimizing the power regulator, the design provides a solution for a PMIC using 40 nm technology.

2.4 Charge Pump (CP) Design

In NMOS-based LDO, to ensure the pass transistor operating in the saturation region, the V_{GS} need to be higher than the V_{TH} and the V_{DS} should be larger or equal to the difference between V_{GS} and V_{TH}, as shown in Equation 2.1. Therefore, to increase the gate voltage of the pass transistor, charge pump was introduced in this type of LDO topology.

Charge pump is a type of DC-DC converter using switch-capacitors, to boost the voltage without using the inductor. Of the typical charge pumps topologies such as Dickson charge pump, bootstrapped charge pump and cross-coupled charge pump have multiple stages to boost the voltage. In an ideal case, neglecting the voltage drop across the diodes or transistors, these charge pump can increase the output voltage according to the number of stages of the charge pump. For example, to increase the output voltage to be 2 times higher than the input voltage, then the number of stages of the charge pump should be 2 stages. But in real applications, due to the voltage drop across the diodes or the transistors, the output voltage will be lower than the designed values. (Palumbo & Pappalardo, 2010)

2.4.1 Dickson Charge Pump

The architecture of a simplified Dickson charge pump consists of a series of capacitors and charge transfer switches controlled by clock signals. By precisely modulating the clock frequency and phase, the system regulates the energy transfer between stages, enabling the multiplication of the input voltage. Higher frequencies reduce the effective output impedance, while synchronized clock phases ensure that charge is pushed forward through the chain without significant backflow losses.

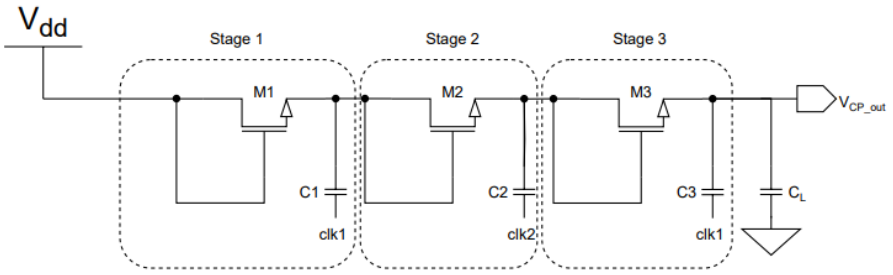


Figure 2.19: Three-Stage Dickson Charge Pump with Diode-Connected NMOS Transistors

Figure 2.19 illustrated the simple 3-stage Dickson charge pump where the transistor is used at here as a switch and the clk1 and clk2 have a 180° of phase shift. In the first clock cycle, C1 will be charged and it will discharge the voltage to C2 in the second clock cycle, thus the C2 voltage shall be equal to $2V_{DD}$, and then at the third clock cycle, the output voltage will be $3V_{DD}$. However, due to the V_{DS} of each transistor, resulting in additional voltage drop, the output voltage will be lower than the expected (Palumbo & Pappalardo, 2010).

This topology of charge pump is the simplest design of charge pump, in which the designer needs to calculate the node voltage to ensure the transistor operating in the saturation region. However, this topology has a low load capacity, in which when the charge pump is required to supply a medium or high load current, which is larger than 5 µA, the charge pump will not function properly due to the low load capacity. In addition, the ripple of the output waveform will be quite large in which a large load capacitor is required to filter the high frequency noise, resulting in large area.

2.4.2 Cross-Coupled Charge Pump

The cross-coupled charge pump utilizes a pair of complementary switches that form a flying double-charge pump. In the simplest form, one PMOS and one NMOS transistor are driven in opposite phases so that each half-cycle transfers charge with virtually zero threshold loss.

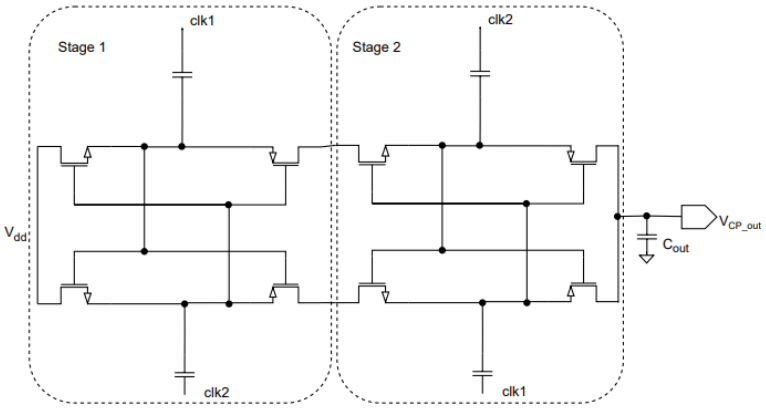


Figure 2.20: 2 Stage Cross-Coupled Charge Pump

The cross-coupled architecture inherently reduces the required capacitance per output current by half as compared to Dickson's charge pump, since the two capacitors are being pumped in parallel. In effect, one branch is charging while the other branch is discharging, and vice versa, resulting in a latch that only transfers when a switch is actively on. This means the transistors are fully on during transfer and fully off otherwise, greatly reducing the backward leakage, which is an inherent drawback of Dickson's charge pumps. Cross-coupled pumps typically offering much higher efficiency and output drive than Dickson's charge pump at the same input voltage (Ballo, et al., 2019).

2.5 Clocking System Design

According to the schematic or system architecture of the NMOS LDO design, the op-amp requires a charge pump to increase the supply voltage to ensure the NMOS pass transistor operating in the saturation region. Two clock signals with a 180° of phase shift are required by the charge pump to charge and discharge for the capacitor in the charge pump as shown in previous section. Besides, the efficiency of the designed charge pump is affected by the quality of the clocking signal, where these two 180° phase shift clocking signals should not overlap, and must adapt to the provided V_{DD}, which is 1.8 V, 2.5 V or 3.3 V. To produce a high-quality clock signal to maximize the efficiency of the designed charge pump, clocking system circuit should be well designed.

2.5.1 Single to Differential Converter (SDC)

To produce two non-overlapping 180° phase-shift signals, a single to differential converter (SDC) was introduced to solve this issue. A well designed SDC can provide two different 180° phase-shift clock signals from only a single input oscillating signal, that can be a sine wave or a square wave. While the input clocking signal of the charge pump was well designed, both branches of the charge pump can charge and discharge the capacitor simultaneously, avoiding the shoot through current which can reduce the pumping efficiency of the charge pump (Ballo, et al., 2019).

2.5.2 Level Shifter

To achieve the best efficiency of the charge pump, except for a low rise and fall time, two non-overlapping input clock signals for the charge pump, the accuracy of the voltage also act as one of the important factors for the charge pump. A well-designed level shifter can pull up the clock signal voltage as near as the supply voltage, V_{DD}, providing a high voltage to charge the capacitor and driving those MOS transistors to

switch on or off as to avoid any current leakage that will reduce the efficiency and power delivered (Palumbo & Pappalardo, 2010).

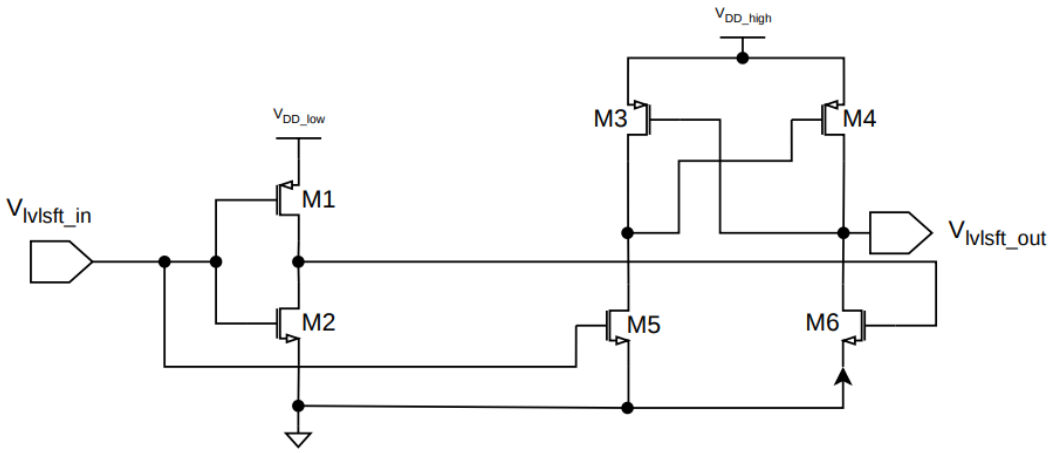


Figure 2.21: Schematic Diagram of Conventional Voltage Level Shifter

Figure 2.21 illustrated the schematic diagram of the conventional voltage level shifter. This circuit can shift up the input signal almost same as the V_{DD_high} by controlling the switching of the PMOS and NMOS transistors. In other words, it can accept a low-voltage signal and generate a high output voltage swing, employing the technique of cascode voltage swing logic (CVSL) structure, in which 4 high voltage transistors are connected to the high voltage in cascode. When the logic of V_{in_p} remains as high, it will pull down the M_5, M_6 will close, which operate in the cutoff region, M_4 will turn on, thus the V_{out} is in high voltage. Meanwhile, when the V_{in_p} remain as low, M_5 will turn off and M_6 will pull down and the V_{out} will be in low level which is 0 V (Shahithi, et al., 2018). The switching transitions of the transistor introduce propagation delay. Therefore, the device dimensions must be carefully optimized through proper transistor sizing to meet the timing requirements.

In short, level shifter can accept a low-voltage signal and generate a high output voltage swing, providing a high voltage of clock signal to enhance the efficiency of the charge pump.

2.6 Error Amplifier Design

An error amplifier (EA), utilizing the op-amp, is the circuit block serves to amplify the difference between the two input signals. Therefore, a small difference will result in a large output voltage signal at the output stage. To ensure the LDO output signal is at the designed voltage, the gain of the EA should be high enough to amplify the small difference between the reference voltage and the output voltage. Besides, the stability of the designed EA is also important for the stability performance of the designed LDO, which normally the zeros and poles will affect the output stage. Therefore, the EA design is important for the LDO, in which selecting the suitable topologies is crucial to achieve the design requirements of the LDO.

2.6.1 Basic Differential Pair

The simplest op-amp topology is the single stage differential pair, incorporating one differential pair with the active load, typically utilizing a current mirror, to provide a single ended output as shown in Figure 2.22. Due to the single stage design, this OTA offers excellent stability, however, the single stage design leads to limited loop gain, though having a high bandwidth. As a result, the PSRR in this OTA is limited due to the low loop gain (Sharma, et al., 2012).

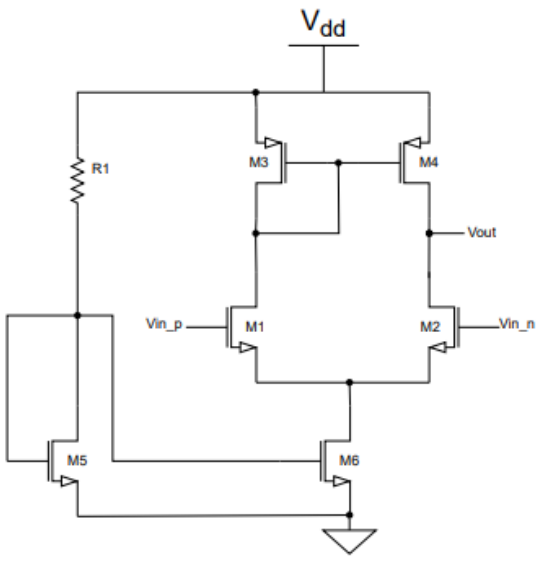


Figure 2.22: Basic Differential Pair Op-amp

2.6.2 Two Stages OTA

Due to the limited gain in the basic differential pair OTA, a common source amplifier was introduced as the second stage of the OTA as shown in Figure 2.23, to increase the gain where the loop gain is shown as:

$$A_v = A_{EA} * A_{CS} \tag{2.7}$$

According to Equation (2.7), the second stage boosts up the loop gain. But on the other hand, due to the second stage introduced, stability was compromised, due to an additional pole contributed by the second stage, degrading the stability, in which the phase margin and gain margin will decrease. To address stability issues, frequency compensation needs to be considered in the design, typically by employing a Miller RC circuit to alter the pole and zero frequencies to ensure stability (Yadav, 2012). Besides, the high gain of the OTA improves the PSRR performance of the LDO.

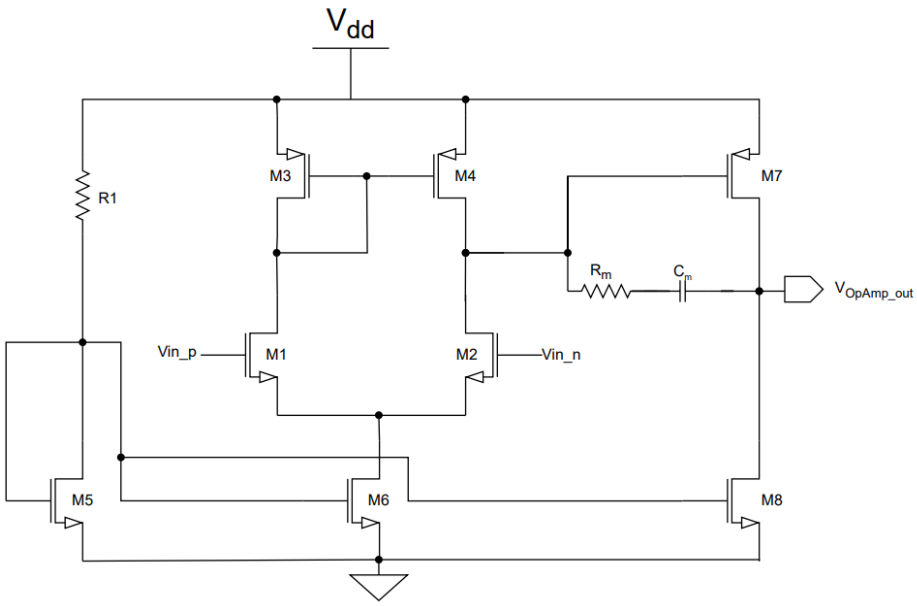


Figure 2.23: Schematic Diagram of Two Stage OTA with Miller RC Compensation

2.6.3 Folded Cascode OTA

The folded-cascode topology stacks or folds a cascode transistor under the input pair so that the input pair can be biased nearer to ground (or the opposite rail) while the cascode transistors being biased near the opposite rail. This topology offers high loop gain and large output voltage swing at low supply voltage. In a typical folded-cascode OTA, the differential pair (NMOS or PMOS) drives opposite-type cascode devices (Dammak, et al., 2008). Folded cascode topologies achieve very high gain and output swing with only one high-impedance pole, hence they are intrinsically stable (Jusoh & Ruslan, 2019). They also have excellent PSRR and low noise due to the cascading transistor. The downside is complexity and increased power consumption: folded cascode requires extra current branches, separate tail current sources and a cascode current, increasing the transistor count.

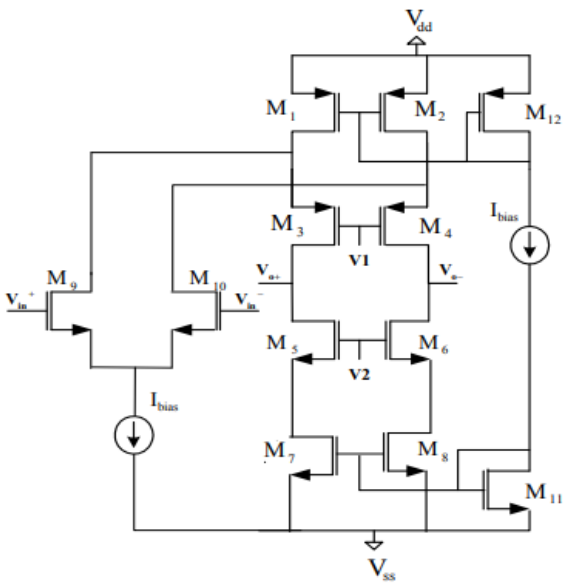


Figure 2.24: Schematic Diagram of Folded Cascode Op-amp (Dammak, et al., 2008)

Despite the advantages offered by folded cascode OTA as discussed above, there are several drawbacks of this topology, which is the most significant issue of this OTA is the headroom problem. Because of the stacking of multiple transistors, the supply voltage drops across each transistor, this limits the output voltage swing, which the DC point of designing the OTA was limited, especially in the low input voltage technologies. Besides, the multiple transistors increase the complexity of designing the

OTA, folded cascode OTA required additional biasing circuit to bias the transistor, which also increasing the power consumption of the OTA (Sharma, et al., 2012).

2.6.4 Current Based Symmetrical OTA

Current based symmetrical operational transconductance amplifier (OTA), also known as “symmetrical” or “current-mode” OTA, is one of the topologies of OTA using a single differential pair and with the output driving the circuit of current mirror loads, as shown in Figure 2.25. Essentially, the normal load replaced by multiple mirror loads, thus the output node can sink or source the high current and increasing the gain of the OTA. This topology of OTA is a single stage thus it consumes lower static power, and the stability performance is good compared to the 2-stage OTA.

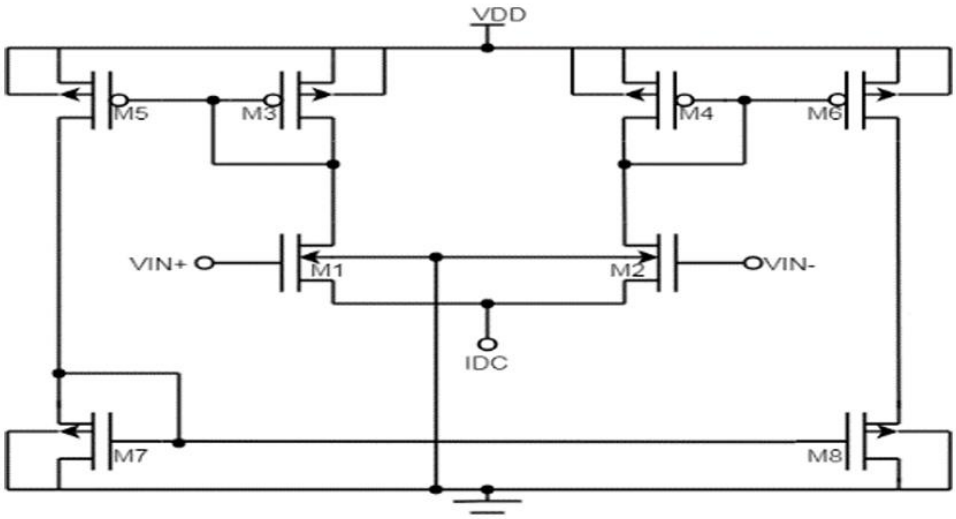


Figure 2.25: Schematic Diagram of Current Based Symmetrical OTA (Jusoh & Ruslan, 2019)

Moreover, this OTA requires a high current to enhance its gain, as increasing the current is fundamental to improving the gain of this design. Compared to the basic differential pair OTA, it uses a current mirror to increase the gain. Thus, with a higher current, this OTA can achieve higher gain. In other words, when the input current was

limited, the gain of this OTA will also be limited which is similar to the basic differential pair OTA, but in terms of the transistor number and the sizing of the OTA. (Jusoh & Ruslan, 2019).

2.7 Summary

This chapter reviewed the fundamental aspects of LDO design, with focus on the advantages and disadvantages between PMOS and NMOS pass devices, charge pump topologies, and OTA performance trade-offs in modern applications. Four operational amplifier topologies were discussed, including the basic differential pair, two-stage op-amp, folded cascode, and current-mirror symmetrical OTA, with emphasis on gain, bandwidth, and power efficiency. Additionally, two charge pump architectures, which is Dickson and cross-coupled, were compared in terms of efficiency, voltage boosting capability, and suitability for NMOS LDO gate drive. The review highlights how different design choices impact stability, PSRR, area, and power, providing a foundation for the methodology adopted in this project.

CHAPTER 3

METHODOLOGY

3.1 Introduction

According to the findings in the literature review, the proposed LDO was designed to meet specific targets for stability, PSRR, and load regulation across wide voltage and temperature ranges. The design incorporates an NMOS pass transistor, charge pumps for low-voltage operation, and several OTA topologies as error amplifiers. Implemented in Silterra 130 nm CMOS with thick-oxide devices, the circuits were verified through process, voltage, and temperature simulations. This chapter outlines the design flow, key building blocks, and simulation setup used to achieve the specifications.

3.2 Simulation Corners

The design specifications of this project are based on the performance requirements of the designed LDO, and have the simulation corner to ensure that the designed LDO is able to operate under all condition such as full load or high temperature. This LDO needs to provide a stable 1.2 V output voltage with 5 mA of maximum load current.

The performance of the circuit is affected by various parameters. To ensure the designed LDO is able to operate in the designed temperature range, the simulation condition of the temperature is set from –40 °C to 125 °C. Additionally to improve the

practicality of the LDO, different input voltage was required in this LDO, where the LDO needs to work in these various of input voltage, which is 1.8 V, 2.5 V and 3.3 V.

Furthermore, the process corners are also important in the design phase of the LDO before sending for fabrication. These process corners can be categorized into typical & typical (TT), fast & fast (FF), fast & slow (FS), slow & fast (SF), and slow & slow (SS) corners, with the first and second parameter showing the performance of NMOS and PMOS transistor in terms of V_{TH}, respectively. In the typical corner, the NMOS and PMOS will have the theoretically V_{TH} as designed. In slow corners, the V_{TH} will be larger, while in fast corner, V_{TH} will be smaller. Thus, when designing the LDO, these corners need to be considered to validate that the fabricated LDO is functional.

Table 3.1: Design Specifications of This Project

Technology	Silterra 130 nm CMOS (Thick Oxide Devices)
Input voltage	1.8 V, 2.5 V or 3.3 V
Output Voltage	1.2 V
Maximum Load Current	5 mA
Power Supply Rejection Ratio (PSRR)	< -20 dB (up to 1 GHz)
Operating Temperature	-40 °C ~ 125 °C
Clock Frequency	150 MHz
Process Corners	TT, FF, FS, SF, SS
Spot Noise of entire system	< 90 V^2/Hz
Integrated Noise of entire system	< 130 V^2/Hz

3.3 System Architecture

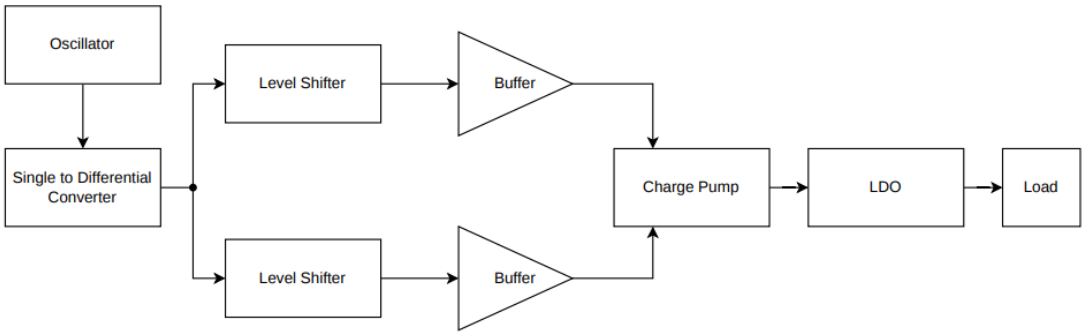


Figure 3.1: Architecture of Designed System

Figure 3.1 shows the entire system architecture of this design. The proposed system architecture is a multi-input voltage NMOS-based transistor low dropout voltage regulator, designed to achieve a low noise output signal while delivering a stable output voltage of 1.2 V while driving the load in the designed range, 0 A to 5 mA., across wide supplying voltage (V_{DD}) of 1.8 V, 2.5 V and 3.3 V. Due to the limitations of NMOS-based LDO discussed in Chapter 2, the system integrates a charge pump to provide a higher supply headroom for the op-amp in the LDO. The architecture introduces a single to differential converter (SDC), to process the signal from the oscillator or clock source, and to generate two differential clock signals that have a phase shift of 180º. These generated clock signals are buffered by SDC to produce high quality square waves, thereby enhancing the efficiency of the charge pump. This SDC block was designed in the technology of 1.2 V, which is supplied by a voltage of 1.2 V, to improve the quality and performance of this SDC block. Furthermore, these 1.2 V differential clocks are stepped up by the following block, level shifter. This SDC block functions to step up the differential signals up to the variable V_{DD}, followed by the output buffer, that provides the drive capability to start up the capacitor in the charge pump.

The designed LDO can maintain a strong regulation in different V_{DD} conditions by using this partitional separation method, avoiding the noise affecting the clock signal and preventing the noise from the clock signal to interfere the output signal, improving the noise suppression and stability of the entire design.

3.4 LDO Design

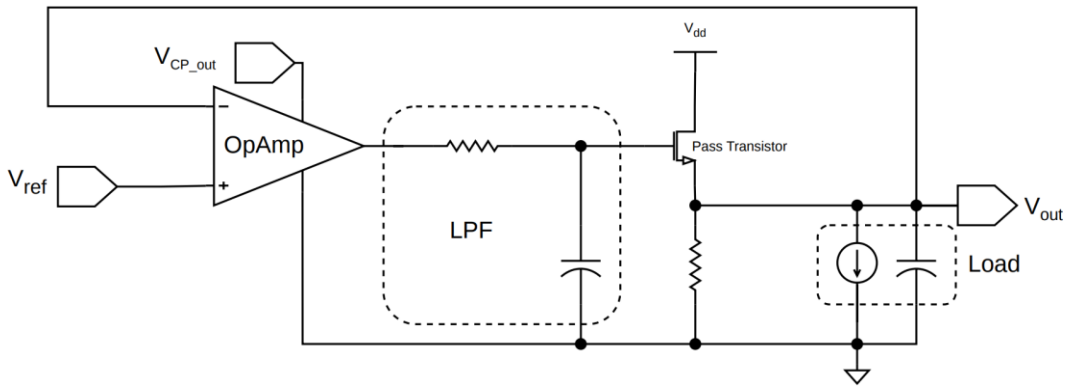


Figure 3.2: Architecture of Designed LDO

The proposed LDO integrated several critical blocks, including op-amp and a low pass filter (LPF), a pass transistor and the output load. These blocks were designed to optimize and enhance the overall performance, stability, noise suppression and the transient response of the LDO. The op-amp is powered by the proposed charge pump, while other blocks are powered by V_{DD}.

When the system supply voltage is 1.8 V, a headroom problem will arise in the pass transistor, to ensure the NMOS pass transistor operate in saturation region:

$$V_{GS} \geq V_{TH} \tag{3.1}$$

The process technology used in this LDO is Silterra 130 nm technology and due to the maximum design value of input voltage is 3.3 V, a thick device was used in this LDO. In typical condition, the threshold voltage (V_{TH}) of the transistor is around 800 mV. Therefore,

$$V_{GS} \geq 0.8\,V \tag{3.2}$$

Since the V_{GS} at this point is calculated as:

$$V_{GS} = V_G - V_S \tag{3.3}$$

where

V_G = gate voltage of the transistor, V

V_S = source voltage of the transistor, V

And the source of the NMOS transistor was connected to output and the gate was connected to the output of the EA, thus

$$V_{G(min)} = 1.2 + 0.8 = 2\ V \tag{3.4}$$

where

$V_{G(min)}$ = minimum gate voltage of the transistor, V

The minimum requirement of the gate voltage of the pass transistor is 2 V but in the at 1.8 V supply voltage, the gate voltage is unable to achieve the requirement to overcome the threshold voltage. To address this problem, a charge pump was introduced in this situation. Besides, the same problems will occur in the condition of V_{DD} in 2.5 V, which requires a wide swing in the cascading op-amp, which is limited by the supply voltage. Thus, the charge pump is used to supply the op-amp, and using some switch to control avoiding overcharge in the condition of V_{DD} in 3.3 V.

The gate voltage of the NMOS pass transistor should be higher than 2 V, thus the DC point of the output node of the OTA was set in the minimum value of 2 V. In calculation to ensure the NMOS pass transistor operates in saturation region using Equation 2.1, the gate voltage should in the range of 2 V to 2.6 V.

On the other hand, the drain current of the NMOS pass transistor flow to the pull-down resistor was designed to be 50 μA to provide a balance between the trade-offs of the sizing and current flow of the pass transistor according to the drain current equation in saturation region:

$$I_d = \frac{K_n}{2} * \frac{W}{L} * (V_{GS} - V_{TH})^2 \tag{3.5}$$

where

K_n = transistor gain, $\frac{A}{V^2}$

W = width of the transistor, m

L = length of the transistor, m

Once the drain current flowing across the NMOS pass transistor is established, the load resistance can be calculated as:

$$R_{load} = \frac{V}{I} = \frac{1.2\ V}{50\ \mu A} = 24\ k\Omega \tag{3.6}$$

where

R_{load} = load resistor, **Ω**

The range of the drain current will be in between 50 μA to 5.05 mA, which is the minimum load and maximum load of the NMOS pass transistor. The gate dimensions of the NMOS pass transistor need to be large enough to cater for the maximum load current at 5.05 mA. Lastly, the load capacitor used for enhancing the stability and high frequency response, may decrease the bandwidth by pushing the poles to a lower frequency, which improves the stability of the system, which is one of the trade-offs designing this LDO circuit.

Besides, an RC LPF is placed between the output of op-amp and the gate of the pass transistor. This LPF was integrated to attenuate those high frequency noise, especially the high frequency ripple arising from the charge pump, and clock system, from being injected into the gate of the pass transistor. Furthermore, this LPF block also able to introduce a pole to assist the frequency compensation and enhancing the overall stability performance in the close loop system.

3.5 Clocking System Design

In this proposed NMOS-based LDO, a gate voltage of the NMOS pass transistor should be significantly larger than the V_{DD} to drive the pass transistor efficiently. To achieve this specification in this design, a charge pump was introduced, to increase and charging the supply voltage significantly. According to the findings in Chapter 2, to enhance the efficiency or performance of the charge pump, two high quality differential square wave with a phase shift of 180º are required. To ensure the amplitude of the clocking signal varies with the V_{DD}, several blocks are required.

3.5.1 Single to Differential Converter (SDC) Design

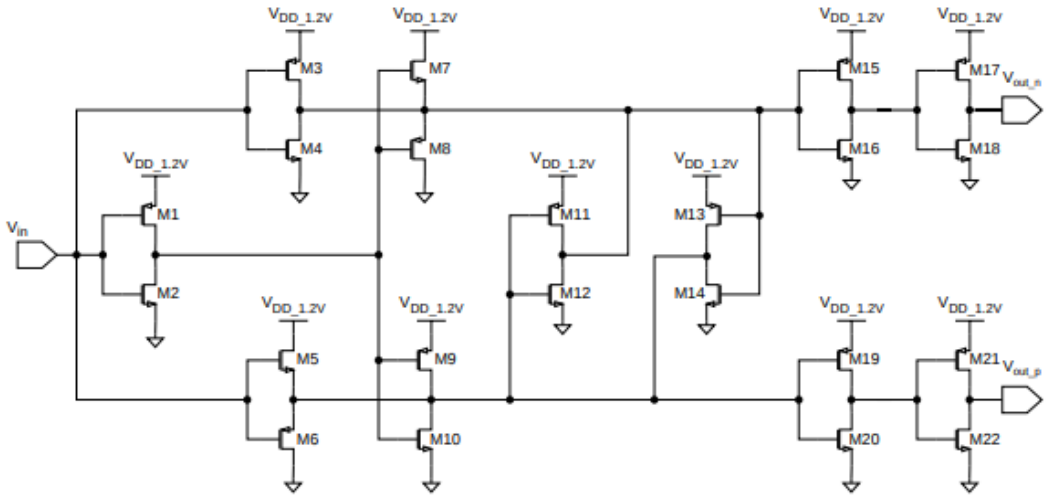


Figure 3.3: Schematic Diagram of Designed SDC in Transistor Level

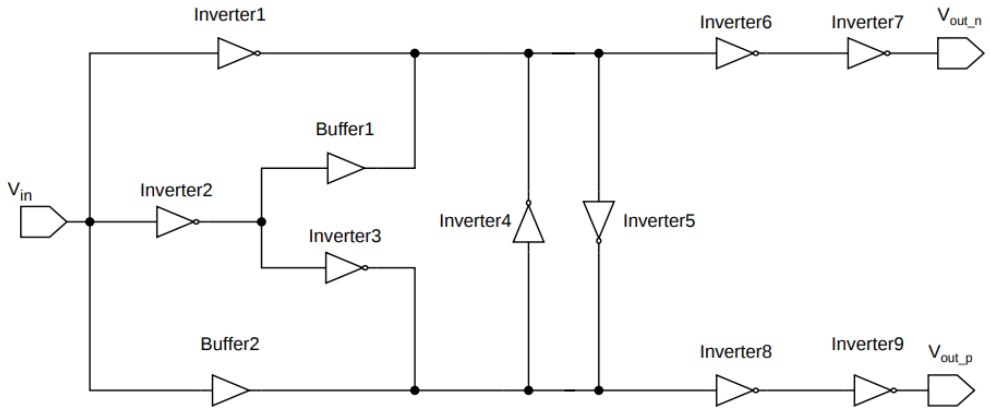


Figure 3.4: Schematic Diagram of Designed SDC in Block Level

The primary function of this single to differential converter (SDC) is to generate two high quality differential square waves with the phase shift of 180º, while received an oscillating signal from oscillator or ideal clock signal generator. The schematic diagrams of the designed SDC in transistor level and block level are shown in Figure 3.3. and Figure 3.4 respectively. As shown in Figure 3.4, the designed SDC consists

of 2 buffers and 9 inverters, with 22 transistors in total for this block. By the combination and arrangement of this buffer and inverter, this SDC can generate a high-quality square wave in the same frequency with the signal received from previous block which is set in 150 MHz in this design.

Besides, the designed SDC is designed entirely in the V_{DD} at 1.2 V to minimize the dynamic power consumption while those transistors were switching in high frequency. The design of the loop from the input signal to the negative output signal (V_{out_n}) should be symmetrical to the loop of the positive output signal (V_{out_p}) to avoid the propagation delay cause by those logic gates. If the transistor from these two loops was not designed properly, it will affect the efficiency of the charge pump.

In short, this SDC block is a single input and duo output block which can generate two high quality square wave while received a single input signal.

3.5.2 Level Shifter and Buffer Design

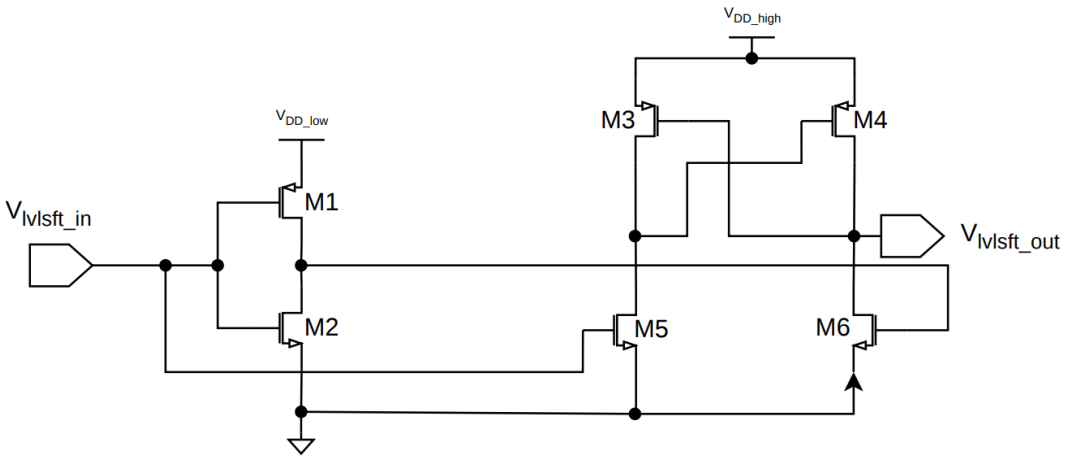


Figure 3.5: Schematic Diagram of Designed Level Shifter

As the SDC was designed in the V_{DD} at 1.2 V, the amplitude of the output signal from the SDC will be aligned at 1.2 V. This voltage level is lower than the output amplitude required to drive the capacitor in the charge pump to operate in the main V_{DD}. This level shifter block acts as a bridge between the stable 1.2 V clocking core domain and

the variable V_{DD} (1.8 V, 2.5 V and 3.3 V) domain. A well-designed level shifter can raise the low-voltage signal to the high voltage signal.

The designed level shifter should be able to operate in different temperature and process corners to ensure the reliable state transition. Specifically, the NMOS transistor must have the capability to overcome the latching force generated from the PMOS transistor cross coupled load, that will be powered up to 3.3 V. To enhance the driving capability of the level shifter, which is required to drive the large capacitor in the charge pump, due to the capacitor is being charged and discharged in high frequency, requiring current flowing in the rising and falling stage, a 4-stage output buffer was introduced.

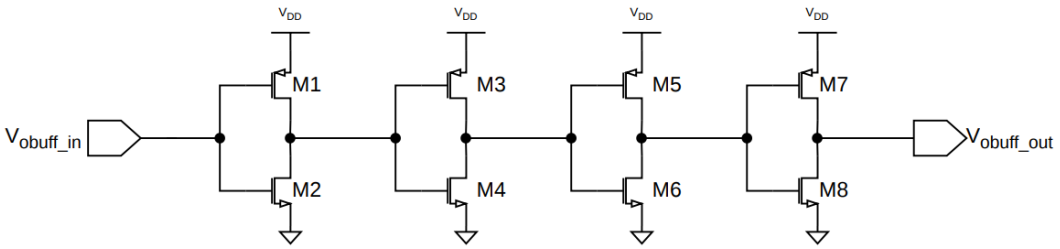


Figure 3.6: Schematic Diagram of 4-Stage Output Buffer in Transistor Level

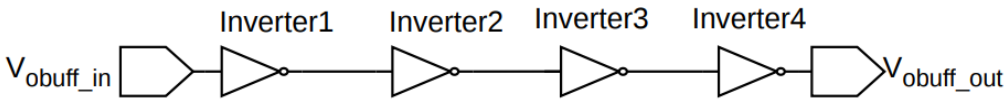


Figure 3.7: Schematic Diagram of 4-Stage Output Buffer in Block Level

Following the level shifter, a cascading inverter chain output buffer, powered by the V_{DD} is implemented. This output buffer consists of 4 inverters, and the transistor size in each stage must be designed according to the proportion as 1:2:4:16 to drive the large capacitive load in and flying capacitor in the charge pump without distorting the quality of the square wave.

3.6 Charge Pump Design

The charge pump is the final stage in the voltage boosting architecture, used to increase the voltage headroom for the op-amp by multiplying the V_{DD} and clock signal generated in previous blocks. This charge pump should be designed to operate efficiently in all process, voltage and temperature (PVT) corners, especially due to the amplitude of the clock signal varies with the V_{DD}. In other words, this proposed charge pump needs to provide a supply voltage to the op-amp, that can drive the pass transistor to operate in saturation region in low V_{DD} condition, while to ensure the supply voltage will not cause oxide breakdown in high V_{DD} corner.

3.6.1 Cross-Coupled Charge Pump Design

According to the needs and requirements of the design, this cross-coupled charge pump is used to address the issue while the V_{DD} is 1.8 V. The charge pump needs to supply a stable voltage of minimum 3 V for a maximum load of 30 µA with the lowest ripple in the output voltage. According to the discussions in literature review, cross-coupled charge pump is the most suitable design topology to fulfil the requirements for this design.

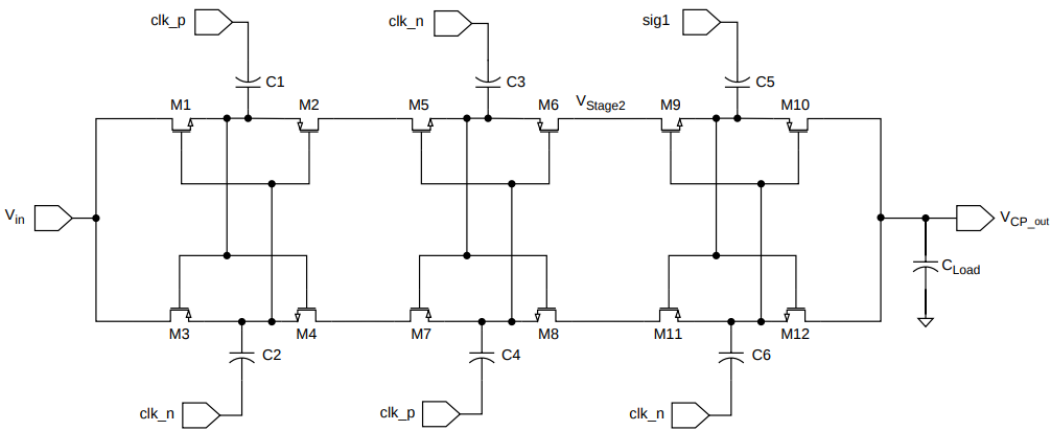


Figure 3.8: Schematic Diagram of Designed Cross-Coupled Charge Pump

The designed two stage cross-coupled charge pump was shown in Figure 3.8, incorporating 6 NMOS and 6 PMOS transistors, and 7 capacitors. This design minimizes the voltage drop in the charge pump by ensuring that the voltage drop in this cross-coupled charge pump is kept below 800 mV. Accordingly, the V_{DS} of each transistor is designed to be less than 200 mV, while still maintaining operation in the saturation region. As calculation, the output voltage will be:

$$V_{OUT} = 3V_{IN} - 6V_{DS} \tag{3.7}$$

where

V_{OUT} = output voltage of the charge pump, V

V_{IN} = input voltage of the charge pump, V

V_{DS} = drain to source voltage of the transistor, V

The minimum output voltage of this charge pump was designed to be higher than the saturation requirement of the NMOS pass transistor, which requires a gate voltage in the range of 2 V and including the voltage dropped in the design OTA, the output voltage of OTA will be in 2 V, that have a wider output swing voltage.

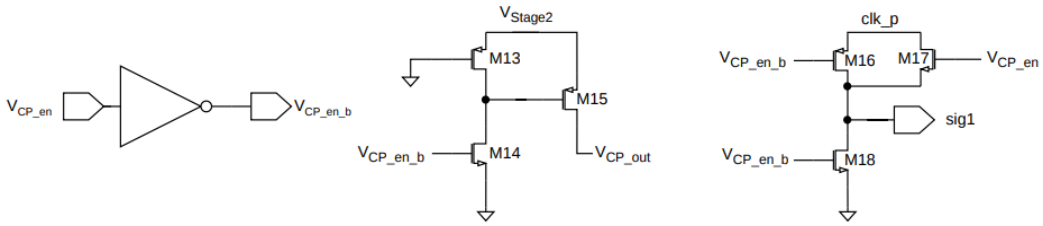


Figure 3.9: Control Circuit of Proposed Charge Pump

To prevent the charge pump overcharging in high V_{DD} condition, the control circuit shown in Figure 3.9 is designed. This control circuit was designed to be enable low, controlled by 1 bit signal, V_{CP_en} is in 0 when V_{DD} is in 3.3 V (high voltage). This control circuit will pull down the sig1, close the third stage and short the output net with the second stage signal (V_{Stage2}). While the V_{DD} in low-voltage (1.8 V and 2.5 V), V_{CP_en} will be set as '1' and the designed charge pump will operate as usual as a 3-stage charge pump.

3.7 Op-amp Design

In LDO, the op-amp plays the critical role in determining the performance of the LDO. In other words, choosing the most suitable topologies of op-amp and designing accordingly the requirement spec of the LDO will enhance the LDO performance. The DC point setting in the op-amp is very important such as the current flow across each net and total current flow, the voltage at each nodes need to be calculated to ensure all the transistors operate in the saturation region, and the DC point setting also affecting the gain, bandwidth and PSRR of the op-amp, indicating a good DC point setting will enhance the op-amp performance.

3.7.1 DC Point Setting

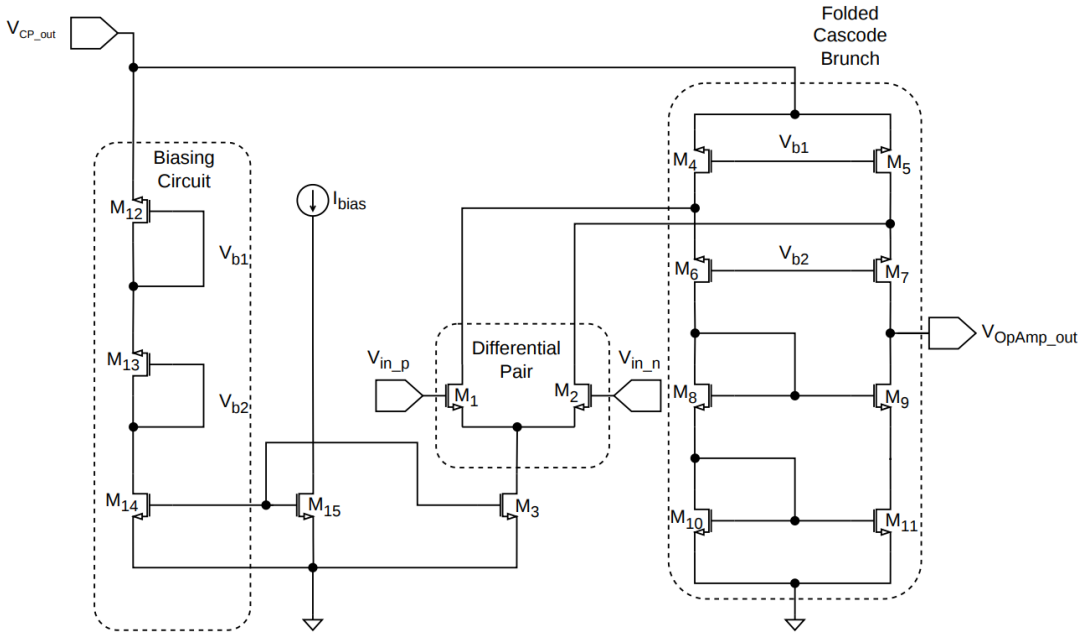


Figure 3.10: Schematic Diagram of Designed Folded Cascode Op-amp

A folded cascode op-amp topology was selected in this project, which can achieve a high loop gain and better stability performance. As compared to the traditional two-stage op-amp, folded cascode was designed in single stage while providing a wider input common mode range and pushing the non-dominant pole to a higher frequency.

This architecture simplifies the frequency compensation of the overall LDO design while reducing the silicon area by eliminating the Miller compensation network, that typically requires a large and area intensive capacitance.

The designed folded cascode op-amp consists of a differential input pair, a folded-cascode stage and a biasing network. The input stage utilizes the NMOS differential pair. This differential pair compares the difference between the referencing voltage (V_{REF}) at 1.2 V and the feedback voltage from the LDO output node. These transistors were sized in a large width to length ratio of $\frac{30\mu}{4\mu}$ to maximize the transconductance, enhancing the overall DC gain and reducing the input offset voltage. The current flow in this loop was designed to be 5 µA in each transistor.

The signal, being in current derived from the differential pair will be sent to the folded cascode stage. In this cascading stage, two PMOS transistors are connected in a common gate configuration, yielding a high overall gain without cascading to another amplifying stage. The total current flowing in this cascading stage was set at 30 µA. The DC point settings for the transistors are critical to ensure all the transistors operate in the saturation region, enhancing the gain and stability of overall system.

A current mirror network providing a stable biasing current for the input differential pair and the biasing network circuit. The biasing network is used to provide a stable DC point for the cascading stage to stabilize the performance of the op-amp in each PVT corner.

3.7.2 Small Signal Analysis

To perform small signal analysis of the folded cascode op-amp, the superposition method can be used to simplify the small signal circuit to reduce the complexity in the calculations, by separating the folded cascode op-amp into the amplifier and current mirror parts.

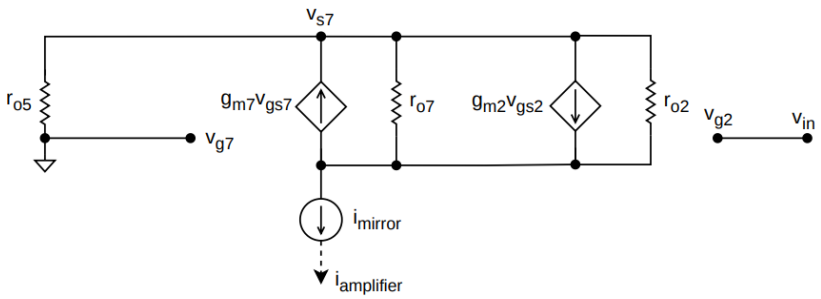


Figure 3.11: Small Signal Analysis Circuit in Amplifier Part

Since the gate of M7 was connected in a constant DC biasing point, thus, in small signal analysis, the M7 gate can be assumed to be connected to the AC ground, and the gain of this amplifier part can be calculated as:

KCL at node v_{out}:

$$\frac{v_{out} - v_{s7}}{r_{o7}} - g_{m7}v_{s7} = 0 \tag{3.8}$$

where

v_{out} = output voltage of the op-amp, V

v_s = source voltage of the op-amp, V

g_m = transconductance of the transistor, S

r_o = output resistance of the transistor, Ω

Simplify Equation 3.3:

$$v_{s7} = \frac{v_{out}}{1 + g_{m7}r_{o7}} \tag{3.9}$$

KCL at node v_{s7}:

$$-\frac{v_{s7}}{r_{o5}} + \frac{v_{out} - v_{s7}}{r_{o7}} - g_{m7}v_{s7} - g_{m2}v_{in} - \frac{v_{s7}}{r_{o2}} = 0 \tag{3.10}$$

Substitute Equation 3.3 into Equation 3.4 and simplify:

$$A_{vamp} = \frac{v_{out}}{v_{in}} = -g_{m2}(r_{o2}//r_{o5})(1 + g_{m7}r_{o7}) \tag{3.11}$$

where

A_{vamp} = gain of the amplifier, $\frac{V}{V}$

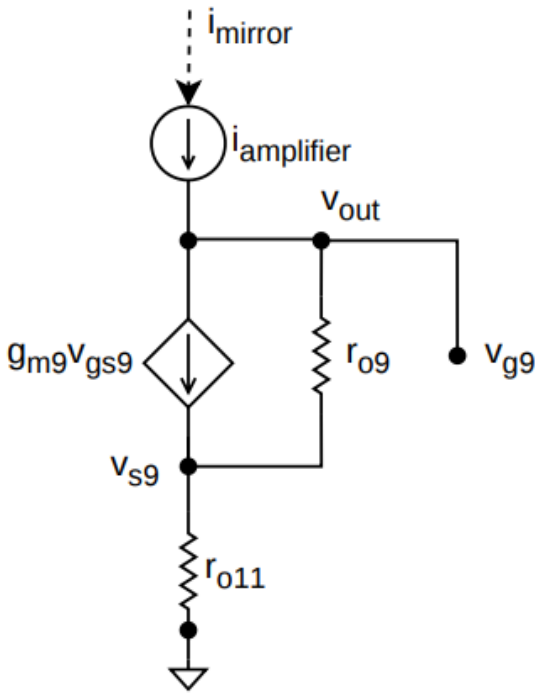


Figure 3.12: Small Signal Analysis Circuit in Current Mirror Part

Similar to transistor M7, the gate of transistor M11 is also connected to the AC ground, and the current mirror part can be analysed as follows:

KCL at node V_{out}:

$$\frac{v_{out} - v_{s9}}{r_{o9}} + g_{m9}v_{gs9} = 0 \tag{3.12}$$

Simplify Equation 3.7:

$$v_{s9} = \frac{v_{out}}{1 + g_{m9}r_{o9}} \tag{3.13}$$

KCL at node V_{s9}:

$$\frac{v_{out} - v_{s9}}{r_{o9}} + g_{m9}v_{gs9} - \frac{v_{s9}}{r_{o11}} = 0 \tag{3.14}$$

Substitute Equation 3.8 into Equation 3.9 and simplify:

$$v_{out} = v_{s9}(g_{m9}r_{o9} + 1 + \frac{r_{o9}}{r_{o11}}) \tag{3.15}$$

Calculate i_{out}:

$$i_{out} = \frac{v_{s9}}{r_{o11}} \tag{3.16}$$

where

i_{out} = output current, A

Calculate r_{out}:

$$r_{out} = \frac{v_{out}}{i_{out}} \tag{3.17}$$

where

r_{out} = output resistance, Ω

Substitute Equation 3.10 and Equation 3.11 into Equation 3.12

$$r_{out} = \frac{v_{s9}(g_{m9}r_{o9} + 1 + \frac{r_{o9}}{r_{o11}})}{\frac{v_{s9}}{r_{o11}}} \tag{3.18}$$

Simplify Equation 3.13

$$r_{out} = g_{m9}r_{o9}r_{o11} \tag{3.19}$$

Combining amplifier and current mirror part:

$$A_v = g_{m2}\{[(r_{o2}//r_{o5})(1 + g_{m7}r_{o7})]//(g_{m9}r_{o9}r_{o11})\} \tag{3.20}$$

where

A_v = gain of the op-amp, $\frac{V}{V}$

Thus, the overall DC gain of the proposed folded cascode op-amp is expressed in Equation 3.15. These derivations show the critical parameters that might affect the DC gain of the folded cascode op-amp, and designing the op-amp to achieve a precise balance between the gain and silicon area.

3.8 Summary

This chapter presented the design methodology developed to implement the proposed LDO regulator. The system specifications, including supply voltages of 1.8 V, 2.5 V, and 3.3 V, stable output voltage at 1.2 V, a load current up to 5 mA, phase margin above 45°, PSRR below –20 dB, and a wide temperature range, were established as design constraints. To meet these requirements, two charge pump topologies (Dickson and cross-coupled) were designed for gate boosting at low supply voltage, while four OTA topologies were evaluated under a maximum bias current of 30 µA. All circuits were implemented in Silterra 130 nm CMOS technology with thick-oxide devices and validated across process, voltage, and temperature variations. The methodology ensures that the regulator design is robust, power-efficient, and suitable for integration in modern SoC and IoT systems.

CHAPTER 4

RESULTS AND DISCUSSIONS

4.1 Introduction

This chapter presents the simulating result and performance of this proposed multi-input voltage NMOS-based low dropout (LDO) voltage regulator system. To validate the robustness and efficiency of the complete system, including the clocking generation system, level shifter, charge pump and LDO was simulated and analysed. This proposed system was evaluated under across the variable V_{DD} while operating under no load (0 A) and full load (5 mA).

The subsequent section discusses the detail performance and functional verification of each critical sub-block. First, the 1.2 V clock generation and conditioning domain, including the SDC, and level shifter was evaluated. Besides, the performance of the voltage boosting block, charge pump, will be analysed including the ripple and efficiency. Finally, the closed loop performance of the LDO system was presented, focusing on key regulatory performance such as transient response, load regulation, line regulation, PSRR, stability and noise analysis to confirm the design meets all targeted specifications.

4.2 Clock Generation and Conditioning

This subsection shows the result of the output signal from the SDC, level shifter and output buffer, which operate in 1.2 V supply voltage. Besides, this subsection also discusses about the performance and quality of the output signal from each block including the frequency, rise and fall time and the duty cycle, ensuring and proving this proposed foundational timing signals are clean and robust to supply the clock signa to following blocks.

4.2.1 Single to Differential Converter (SDC)

As discussed in previous section, this SDC is used to generate two differential square wave signal in 180º phase shift and short rising and falling time. The foundational timing signal required to evaluate, ensure the flowing blocks can receive clean and robust clocking signal, and enough to drive the subsequent voltage boosting stages.

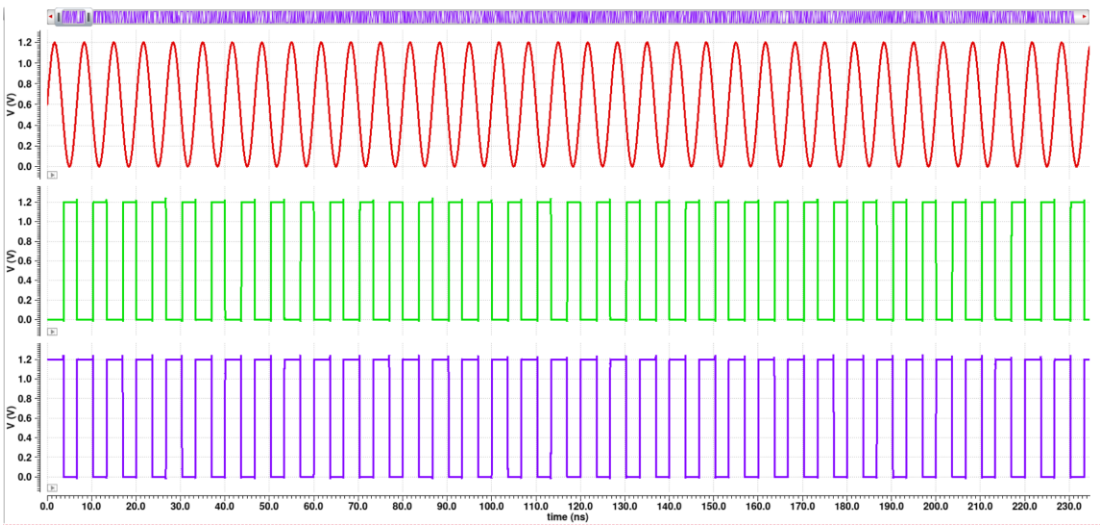


Figure 4.1: Transient Response of Input Clocking Signal (Red), V_{out_n} (Green), and V_{out_p} (Purple)

Figure 4.1 illustrated the duo differential output signal of proposed SDC, while the SDC received the clocking signal from the oscillator or ideal clock source with the

designed frequency, 150 MHz, this SDC can generate two stable and high quality differential square wave with the phase shift of 180º.

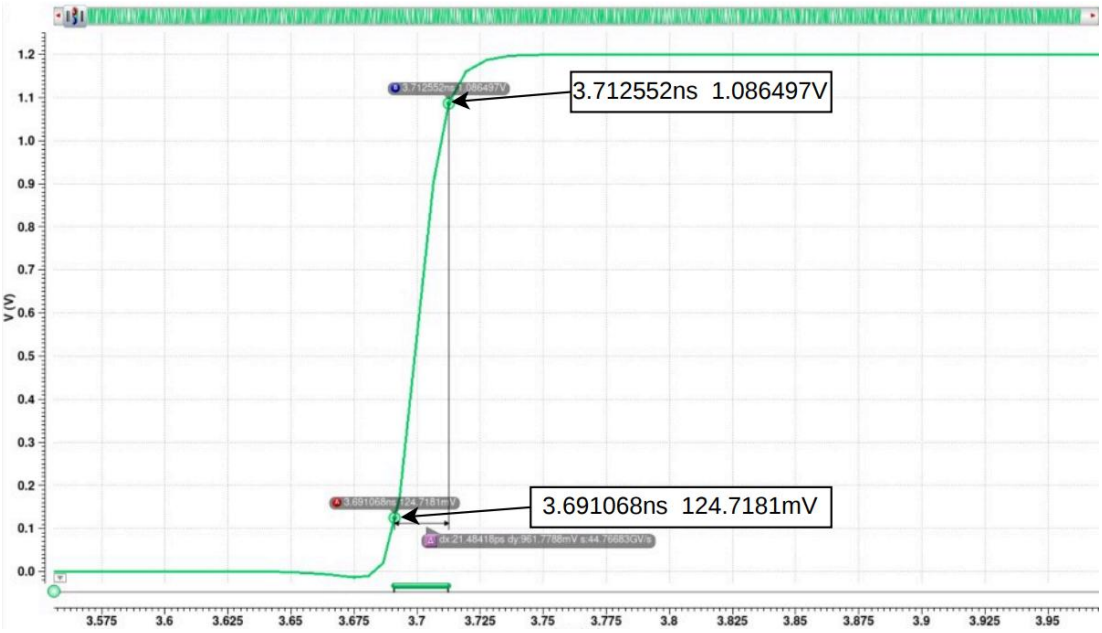


Figure 4.2: Rising Edge of V_{out_n}

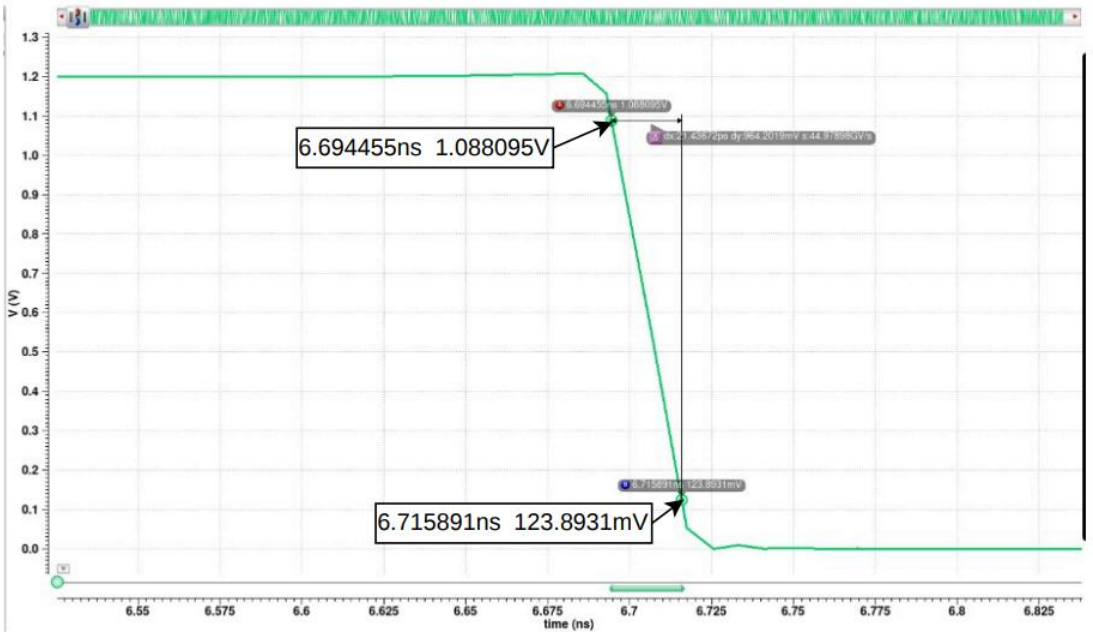


Figure 4.3: Falling Edge of V_{out_n}

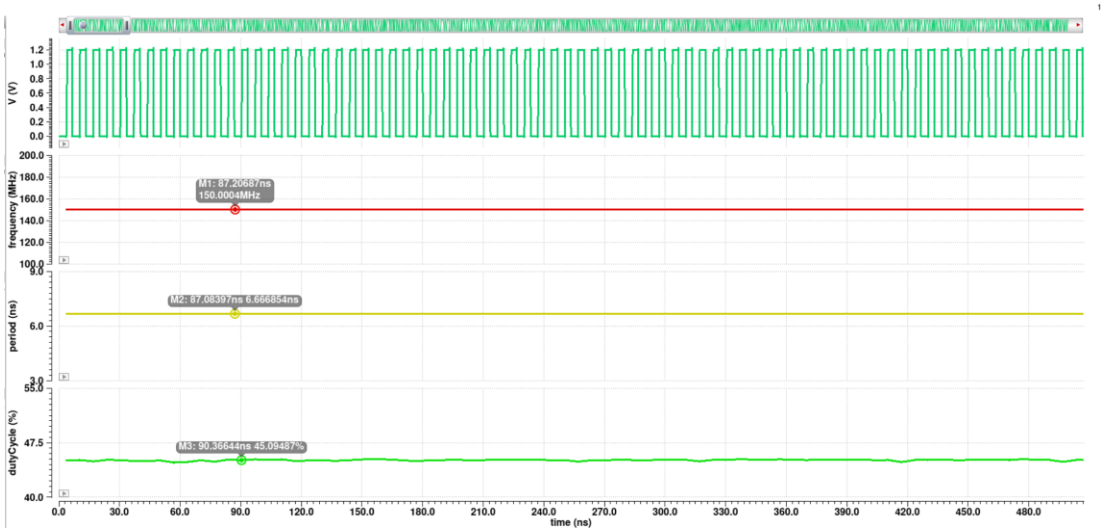


Figure 4.4: Measurement Result of V_{out_n}, Frequency (Red), Period (Yellow) and Duty cycle (Green)

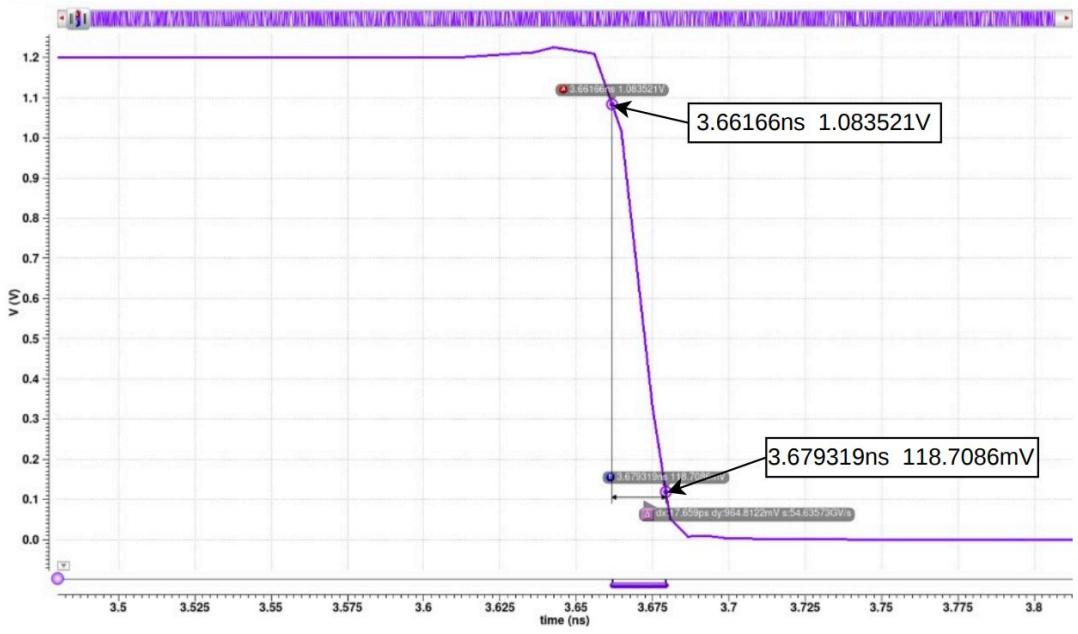


Figure 4.5: Falling Edge of V_{out_p}

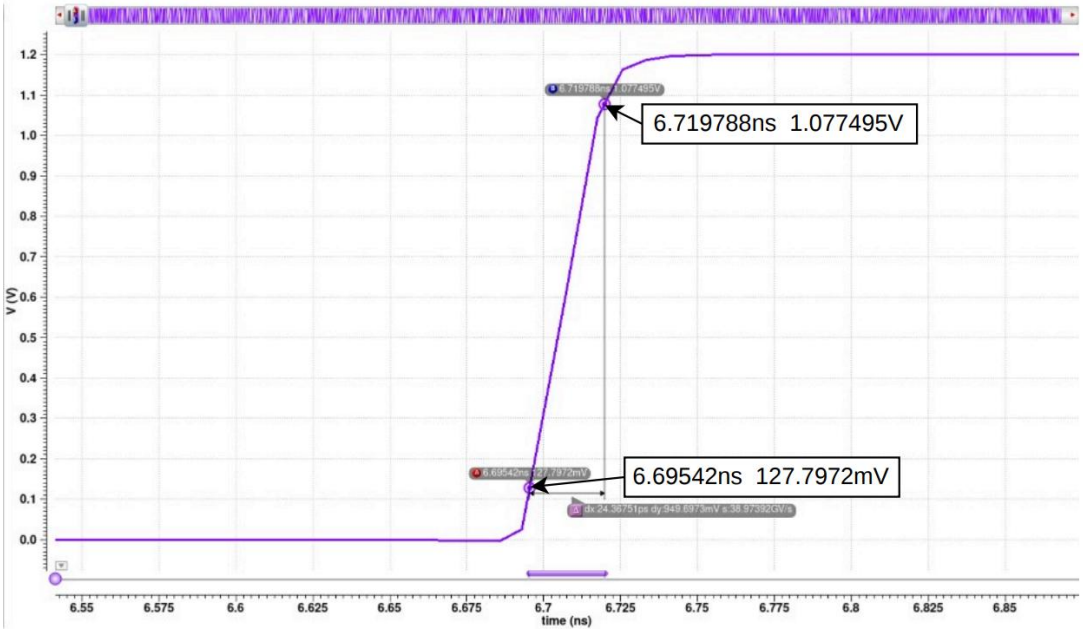


Figure 4.6: Rising Edge of V_{out_p}

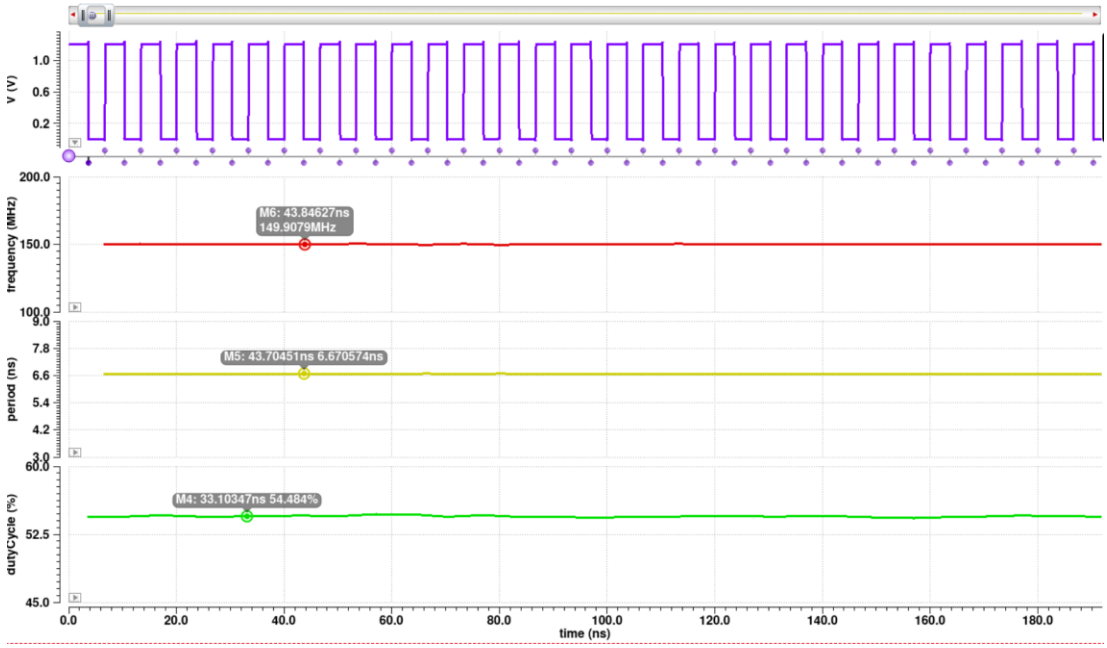


Figure 4.7: Measurement Result of V_{out_p}, Frequency (Red), Period (Yellow) and Duty cycle (Green)

The Single to Differential Converter (SDC) effectively processes the input oscillating signal to generate two differential high-quality square waves with a precise 180° phase shift. Operating at a stable frequency of 150 MHz, the designed SDC generates signals with a period of 6.67 ns and duty cycles maintained between 45% and 54%. Detailed transition analysis shows sharp signal integrity, with a rise time of approximately 21.48 ps and a fall time of 21.43 ps in the negative output of SDC. On the other hand, due to the symmetrical design in the SDC, the positive loop has the same frequency and period compared with the negative output signal, but the duty cycle was increased to 55.5% instead of 45%. This is due to the V_{out_n} and V_{out_p} was inverting to each other. Furthermore, the rise and fall time for this positive output signal is in 24.36 ps and 17.66 ps respectively.

According to the performance of the designed SDC, the output square wave is in short rising and falling time, which minimizing the switching losses within the transistor, enhancing the efficiency for the following blocks. Meanwhile, the output signal shown in Figure 4.1, exhibits some overshoot and undershoot during voltage transitions, while the signal changing from high voltage to low-voltage and the same problem occur while the voltage switching from low-voltage to high voltage, known as overshoot. These transient effects are primary due to the parasitic capacitance in the transistor specifically the gate to source (C_{GS}) and gate to drain (C_{GD}). During high-speed switching, these parasitic elements undergo rapid charging and discharging cycles which might cause the oxide breakoff in the transistor. Since these parasitic capacitances is proportional with the transistor dimensions, therefore the sizing is very important. In these implementations, however, the proposed SDC achieves a well-regulated transistor with small overshoot and undershoot, ensuring the long-term reliability for the devices.

Furthermore, two of the output clocking signals was oscillating in the same frequency and period with the input signal, ensuring no frequency instability occurs in this block. Besides, both output signals have the duty cycle of 45% to 55%, which ensuring the flying capacitor in the Charge Pump have enough time to charge and discharge. This optimization ensuring the SDC provides a high-quality clocking signal to subsequent blocks to maximize the power conversion efficiency and minimize the required start-up time for the charge pump.

4.2.2 Level Shifter

The level shifter functioning as a key voltage regulation interface between the clocking architecture, used to bridging the low-voltage supply, 1.2 V, clocking core domain of the SDC to the variable V_{DD} domain. As the result shown in the previous section, the proposed SDC can generate two high qualities differential clocking quare wave with the amplitude and frequency in 1.2 V and 150 MHz respectively. This clocking amplitude is unable to drive the flying capacitor in the charge pump. This proposed level shifter successfully increases the amplitude scale with the variable V_{DD}, ensuring a full rail-to-rail voltage swing across all the voltage corners.

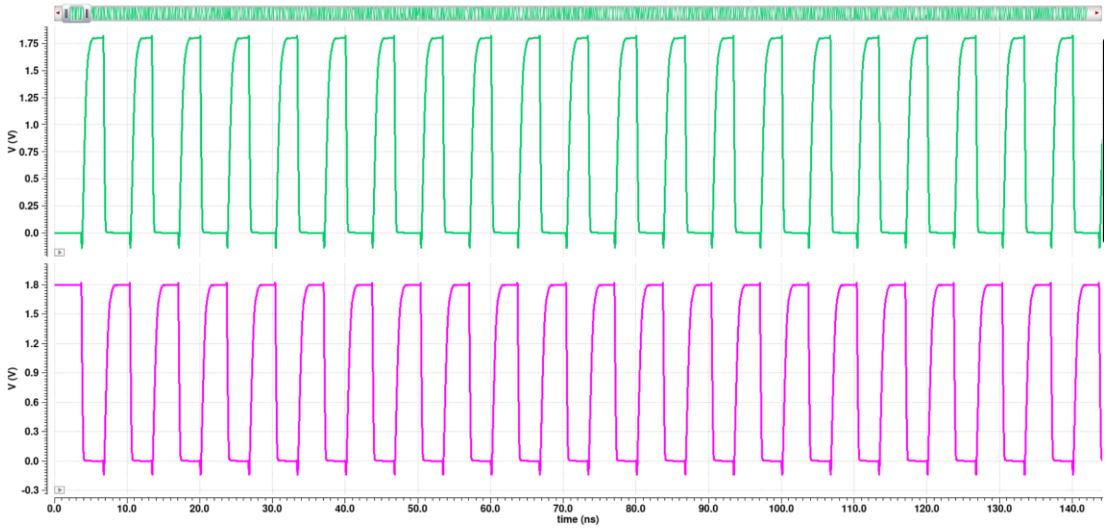


Figure 4.8: Transient Response of Level Shifter, $V_{lvlsft\_out\_n}$ (Green) and $V_{lvlsft\_out\_p}$ (Pink) with V_{DD} at 1.8 V

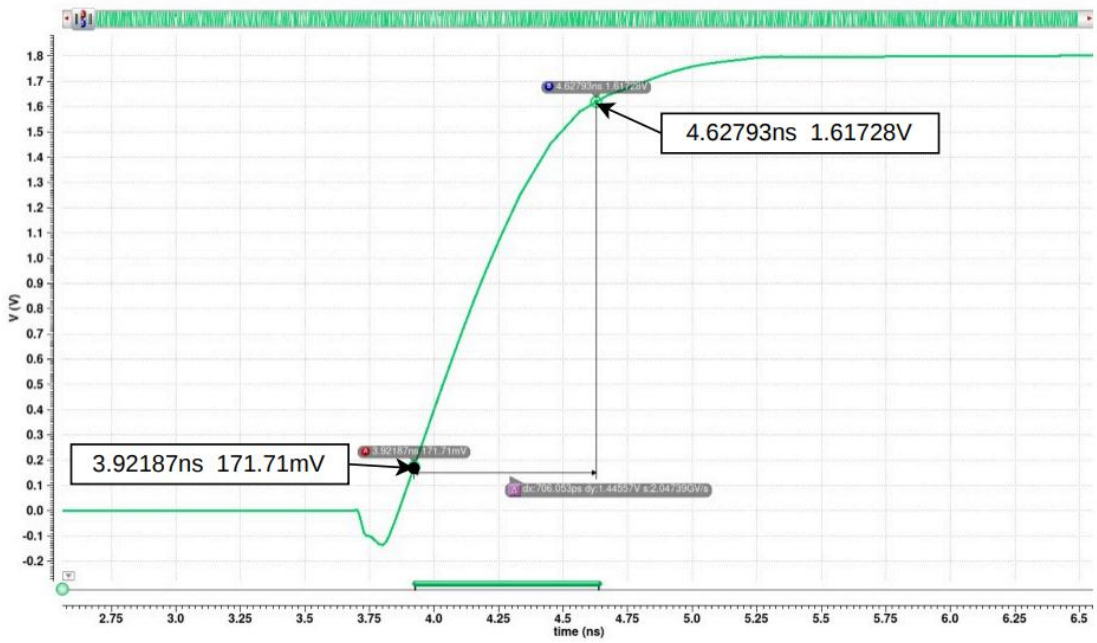


Figure 4.9: Rising Edge of $V_{lvlsft\_out\_n}$ with V_{DD} at 1.8 V

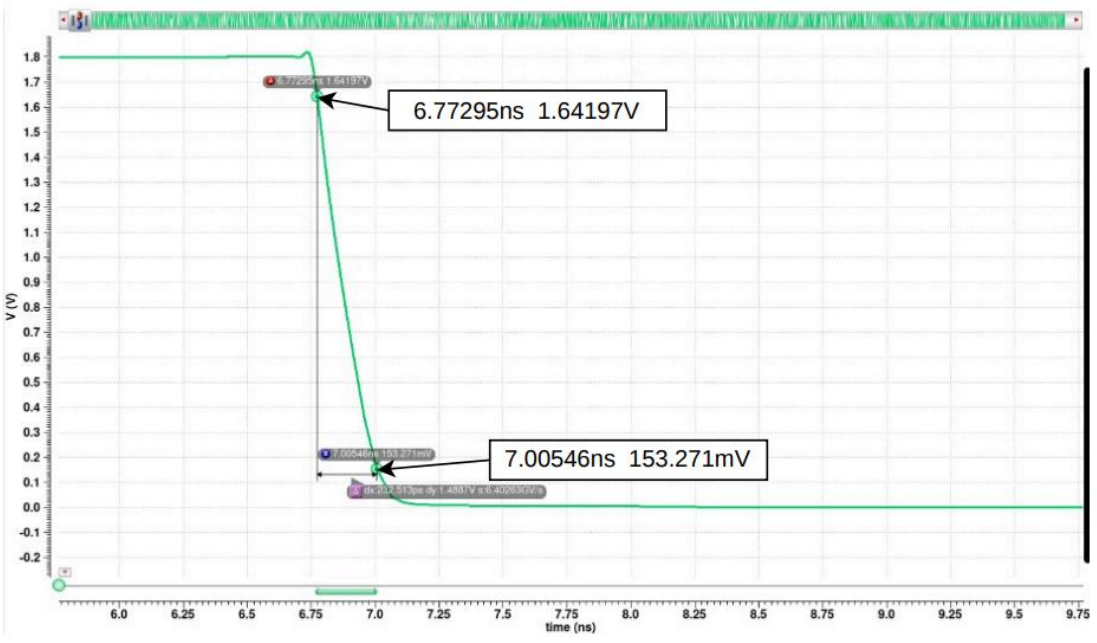


Figure 4.10: Falling Edge of $V_{lvlsft\_out\_n}$ with V_{DD} at 1.8 V

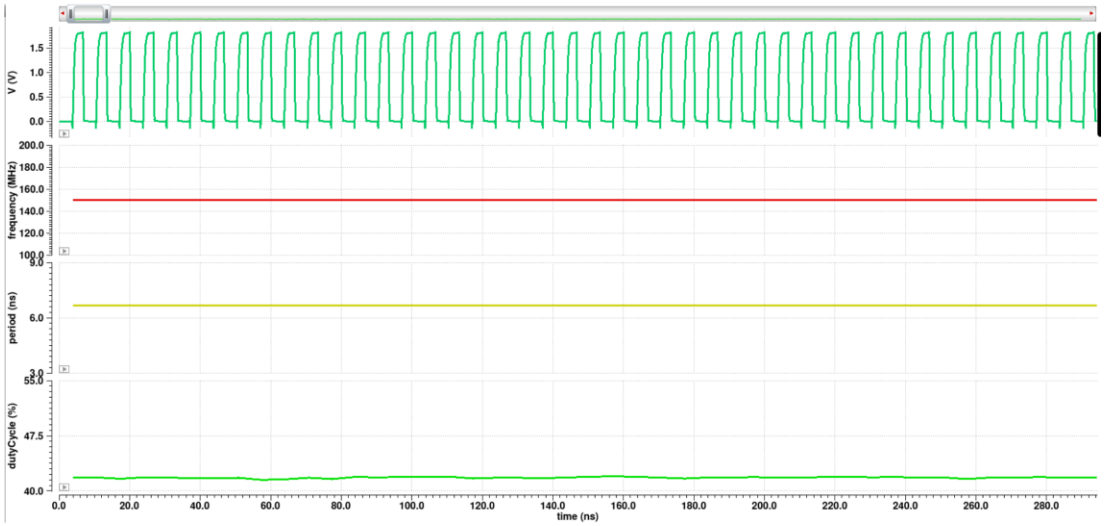


Figure 4.11: Measurement Result of $V_{lvlsft\_out\_n}$, Frequency (Red), Period (Yellow) and Duty cycle (Green) with V_{DD} at 1.8 V

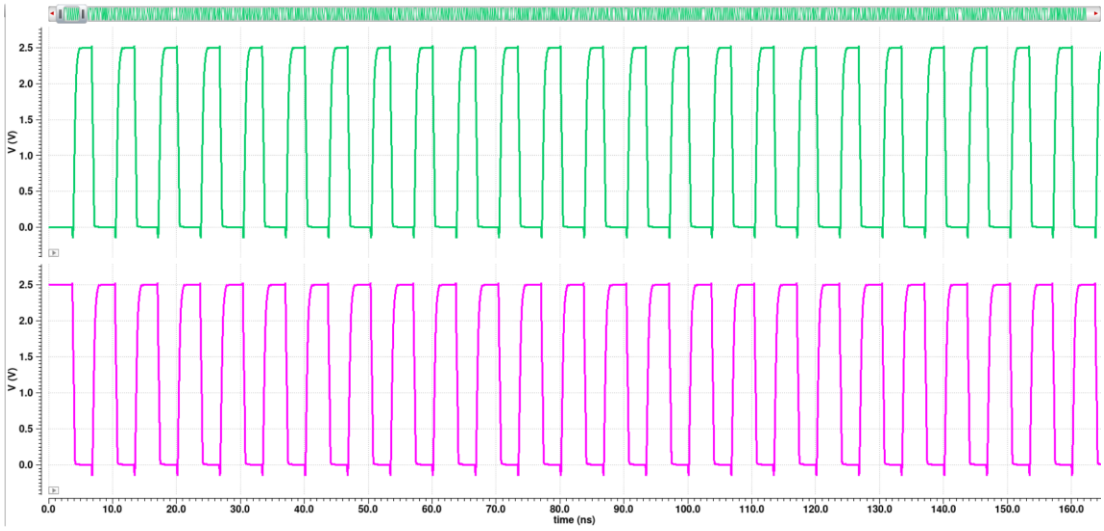


Figure 4.12: Transient Response of Level Shifter, $V_{lvlsft\_out\_n}$ (Green) and $V_{lvlsft\_out\_p}$ (Pink) with V_{DD} at 2.5 V

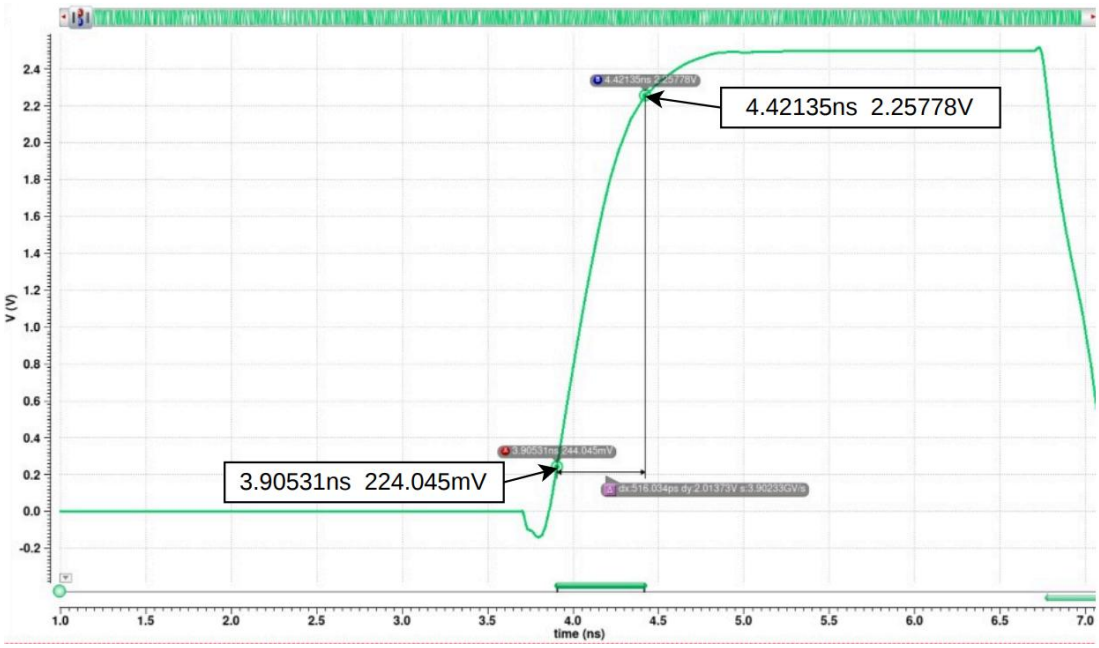


Figure 4.13: Rising Edge of $V_{lvlsft\_out\_n}$ with V_{DD} at 2.5 V

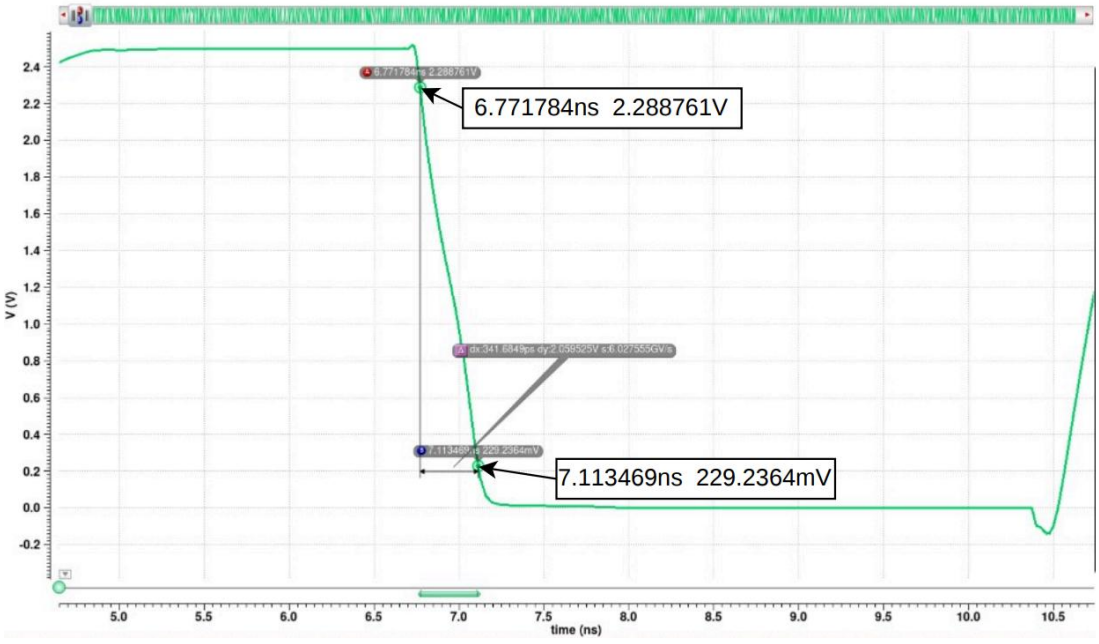


Figure 4.14: Falling Edge of $V_{lvlsft\_out\_n}$ with V_{DD} at 2.5 V

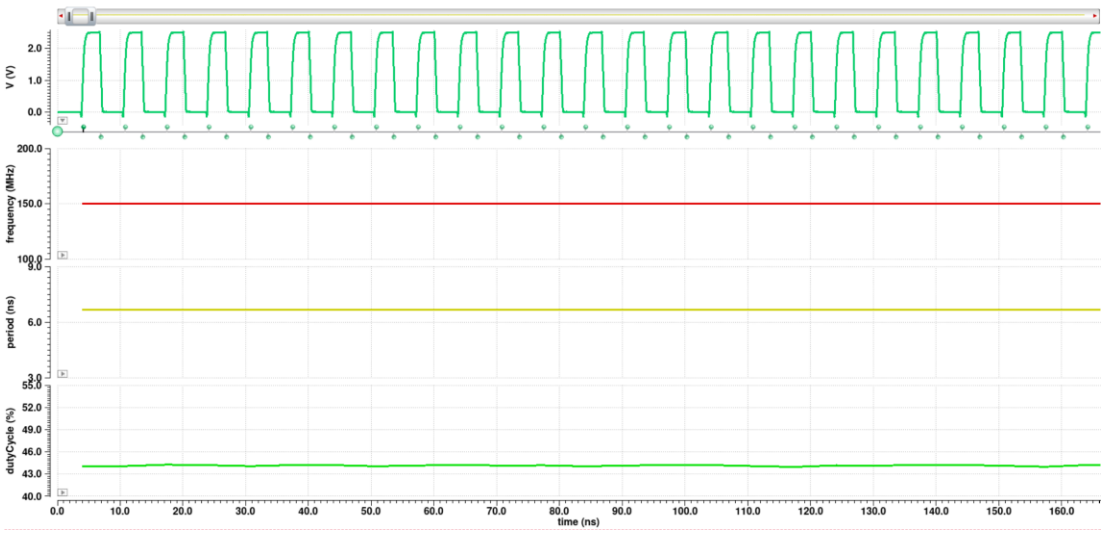


Figure 4.15: Measurement Result of $V_{lvlsft\_out\_n}$, Frequency (Red), Period (Yellow) and Duty cycle (Green) with V_{DD} at 2.5 V

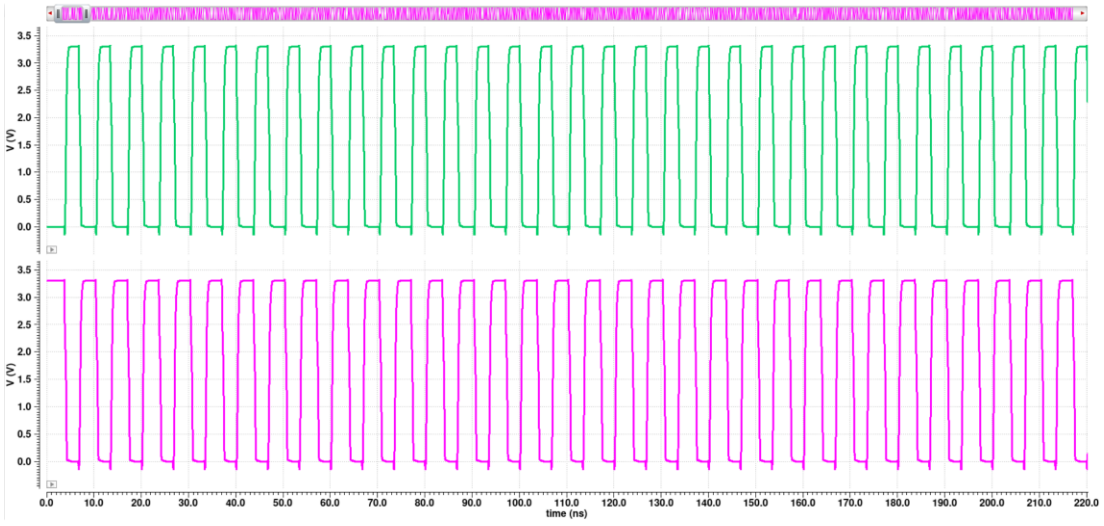


Figure 4.16: Transient Response of Level Shifter, $V_{lvlsft\_out\_n}$ (Green) and $V_{lvlsft\_out\_p}$ (Pink) with V_{DD} at 3.3 V

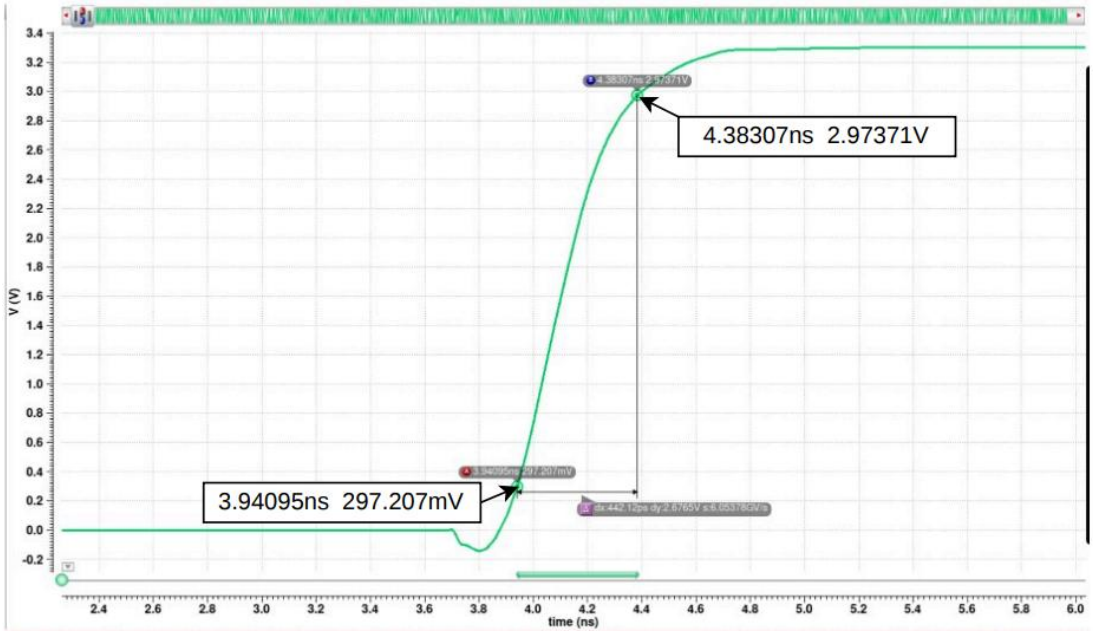


Figure 4.17: Rising Edge of $V_{lvlsft\_out\_n}$ with V_{DD} at 3.3 V

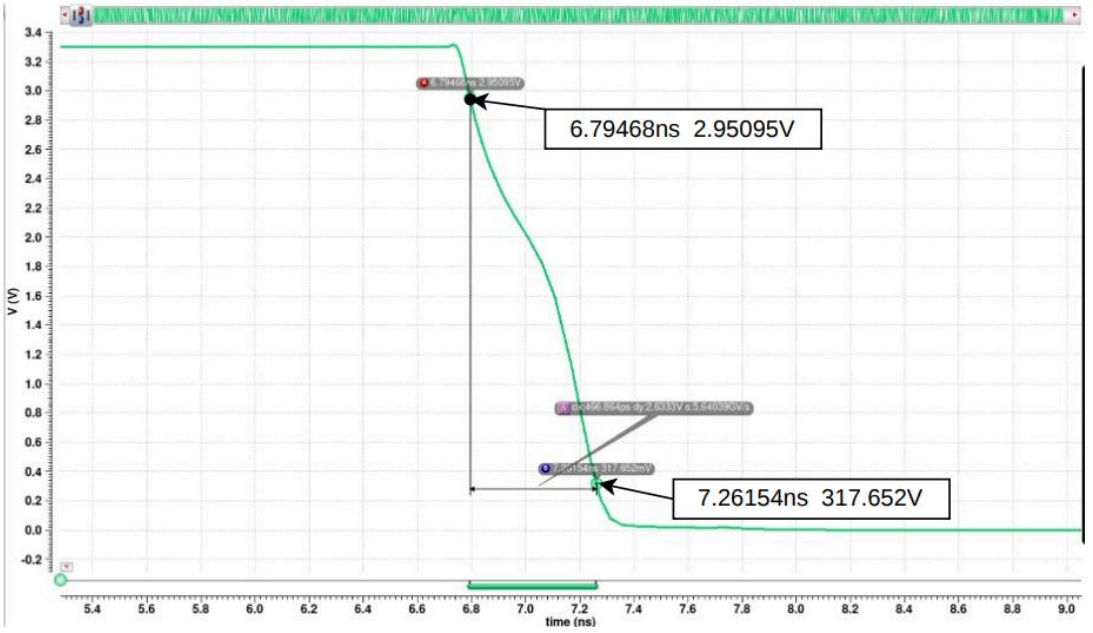


Figure 4.18: Falling Edge of $V_{lvlsft\_out\_n}$ with V_{DD} at 3.3 V

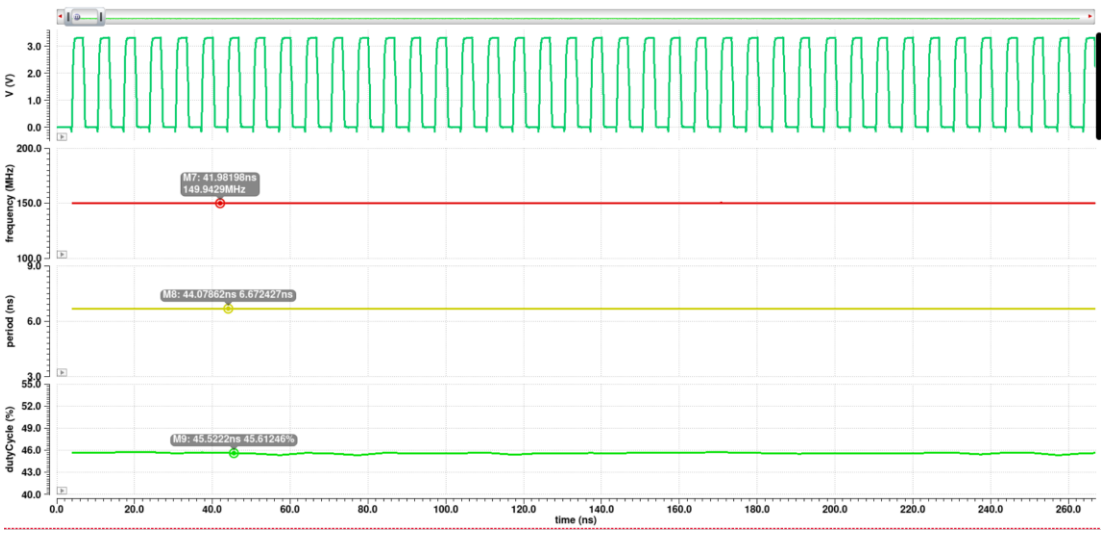


Figure 4.19: Measurement Result of $V_{lvlsft\_out\_n}$, Frequency (Red), Period (Yellow) and Duty cycle (Green) with V_{DD} at 3.3 V

Figures 4.8 through 4.19 illustrate the simulated transient response of the clocking signals generated by the level shifter, including the frequency, period, duty cycle, and the rising and falling time. Because the positive and negative differential clock signals exhibit highly symmetrical performance, the subsequent analysis focuses primarily on the negative clocking signal for simplicity. Across all variable voltage corners, the level-shifted signal successfully maintains the target operating frequency at 150 MHz. The duty cycle is well-regulated between 40% and 45%, which provides a sufficiently balanced charging and discharging window to ensure symmetrical charge transfer in the following cross-coupled charge pump.

On the other hand, the rise and fall times of this level-shifted signal show an increase when compared to the raw output of the SDC, exhibiting rise times of approximately 300 ps and fall times near 103 ps at a 1.8 V supply voltage. This increase is an expected dynamic trade-off, which is a direct result of the cross-coupled PMOS transistors load in the level shifter translating the voltage amplitude, combined with the heavier parasitic capacitive load, present in the subsequent 4-stage output buffer. However, despite this slight increase in transition time, the edges remain sharp enough to effectively mitigate shoot-through currents in the charge pump.

By delivering a clean and stable full swing square wave to the output buffer, this block ensures the transistor in the charge pump will eventually operate as a switch, and the flying capacitor can charge and discharge in every cycle. If this level shifter is unable to scale the amplitude of the clocking signal with the variable voltage corners, it will reduce the efficiency of the charge pump. In the worst-case scenario, the charge pump will be unable to pump the voltage to reach the target value, rendering the entire LDO system inoperable.

4.2.3 Output Buffer

Following the voltage translation, a 4-stage output buffer is implemented to increase the driving capability to ensure the level shifter can drive the high capacitance load in the charge pump. While the level shifter can scale with the variable voltage supply, it lacks the raw of the current capability that required to drive the flying capacitor directly. This output buffer performs as a high-power current amplifier, effectively isolating the sensitive level shifter from the heavy capacitive load of the charge pump and preventing the high-frequency square waves from becoming rounded or heavily distorted under load.

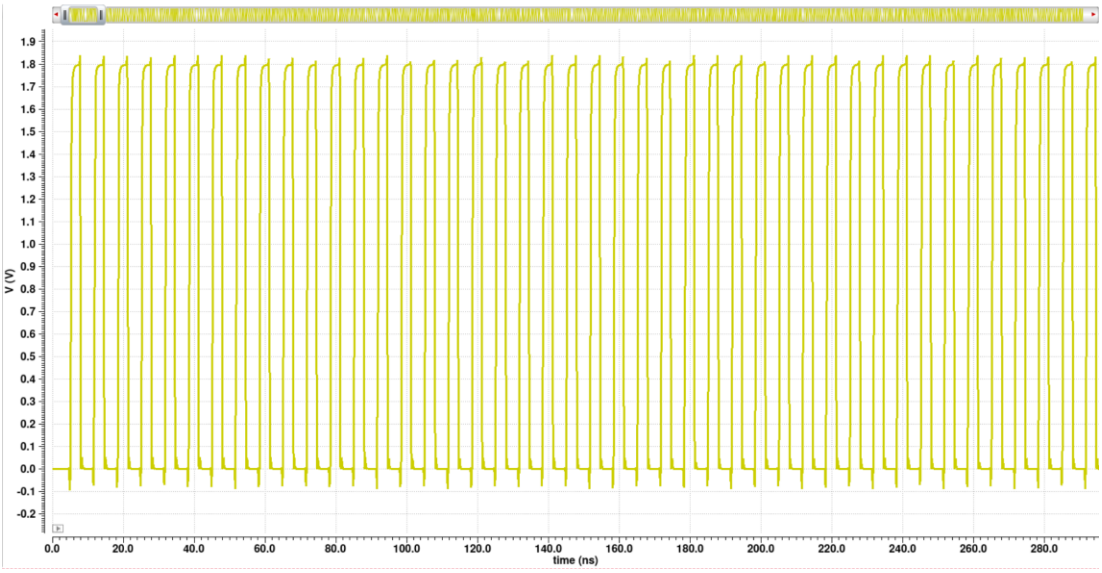


Figure 4.20: Transient Response of Output Buffer, V_{obuff_out} with V_{DD} at 1.8 V

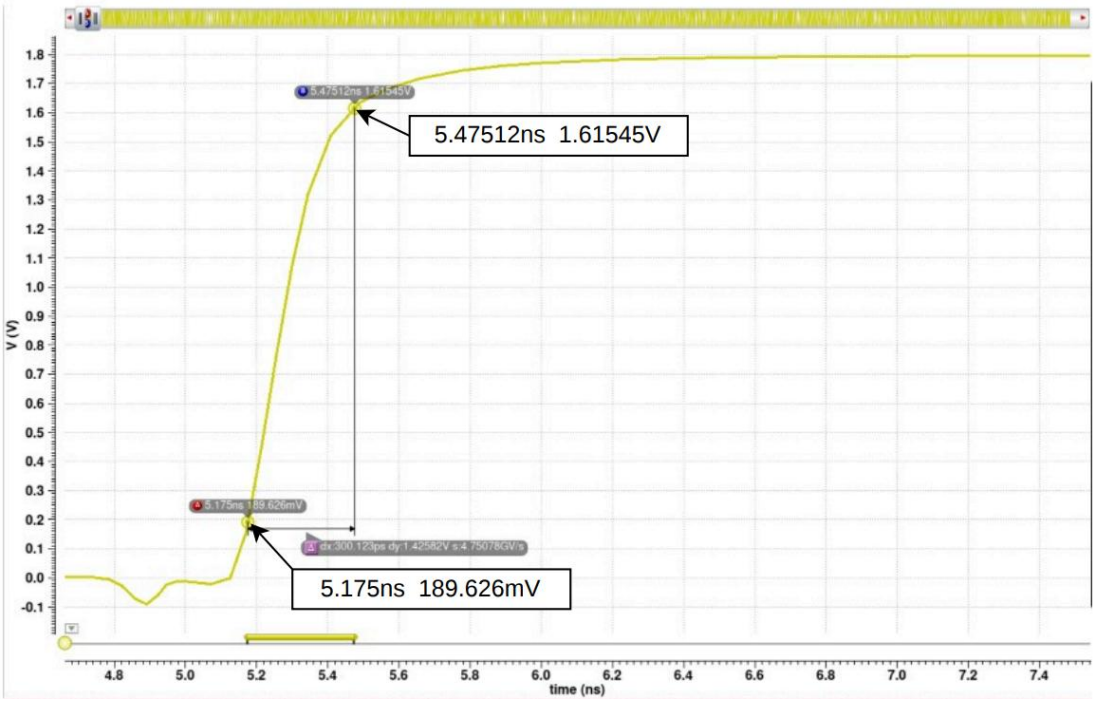


Figure 4.21: Rising Edge of V_{obuff_out} with V_{DD} at 1.8 V

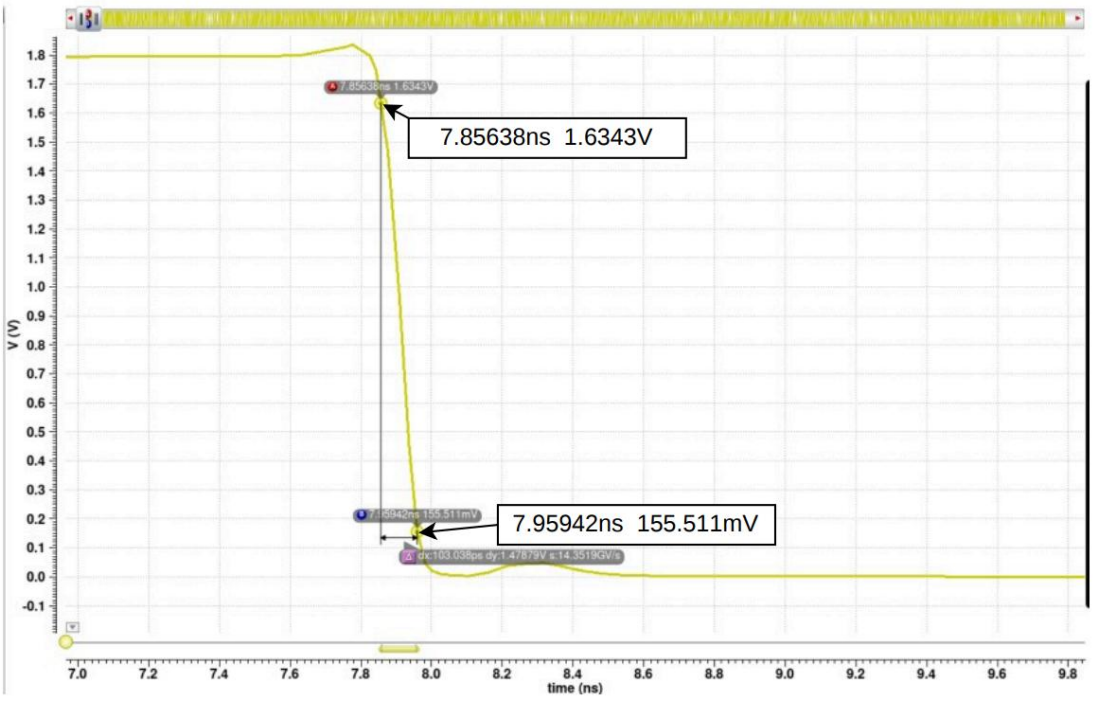


Figure 4.22: Falling Edge of V_{obuff_out} with V_{DD} at 1.8 V

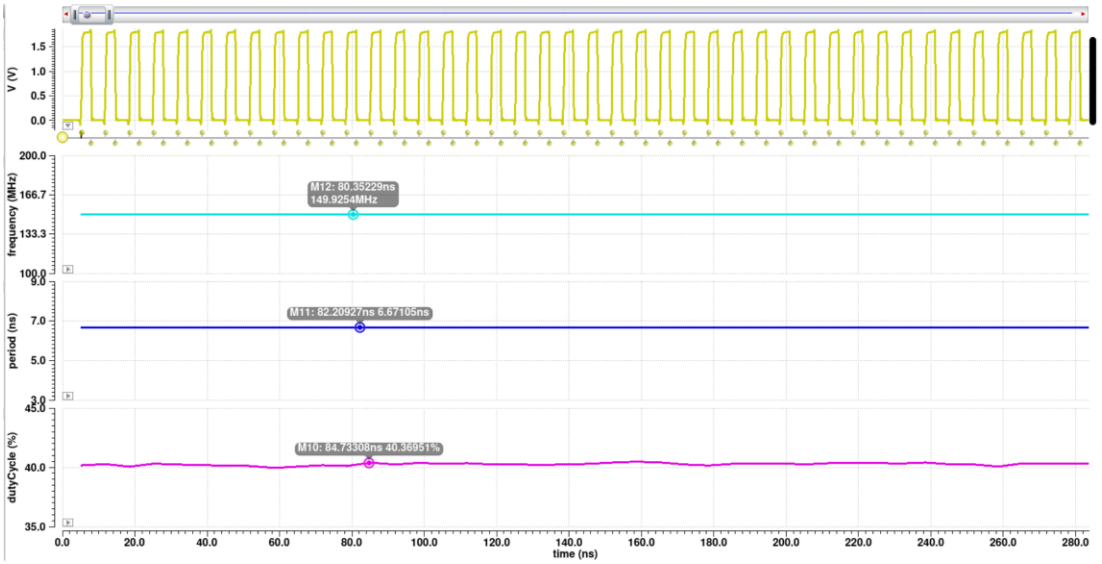


Figure 4.23: Measurement Result of V_{obuff_out}, Frequency (Cyan), Period (Blue) and Duty cycle (Pink) with V_{DD} at 1.8 V

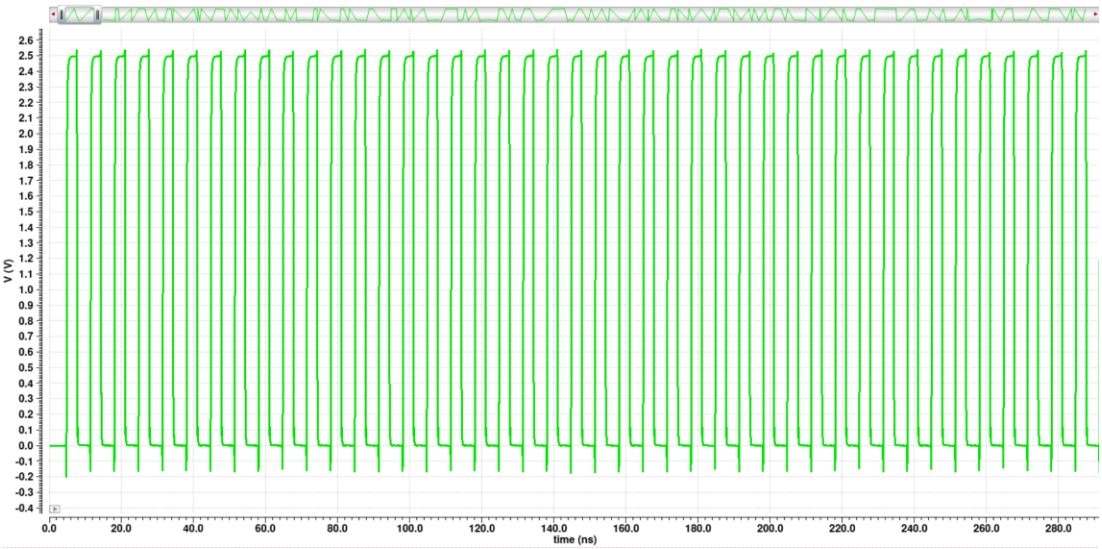


Figure 4.24: Transient Response of Output Buffer, V_{obuff_out} with V_{DD} at 2.5 V

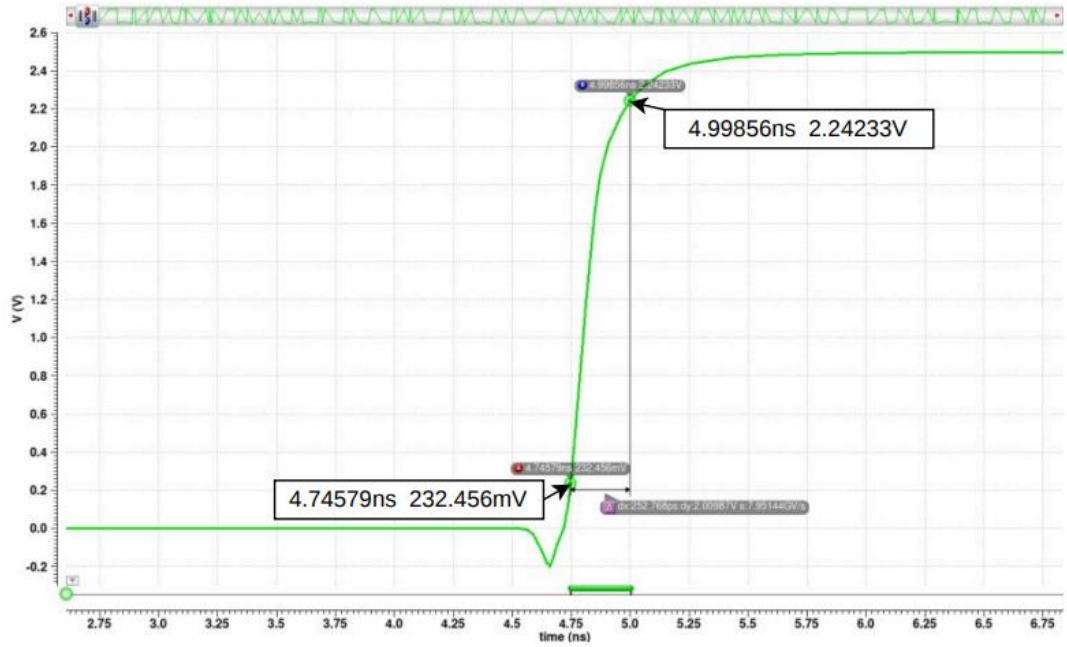


Figure 4.25: Rising Edge of V_{obuff_out} with V_{DD} at 2.5 V

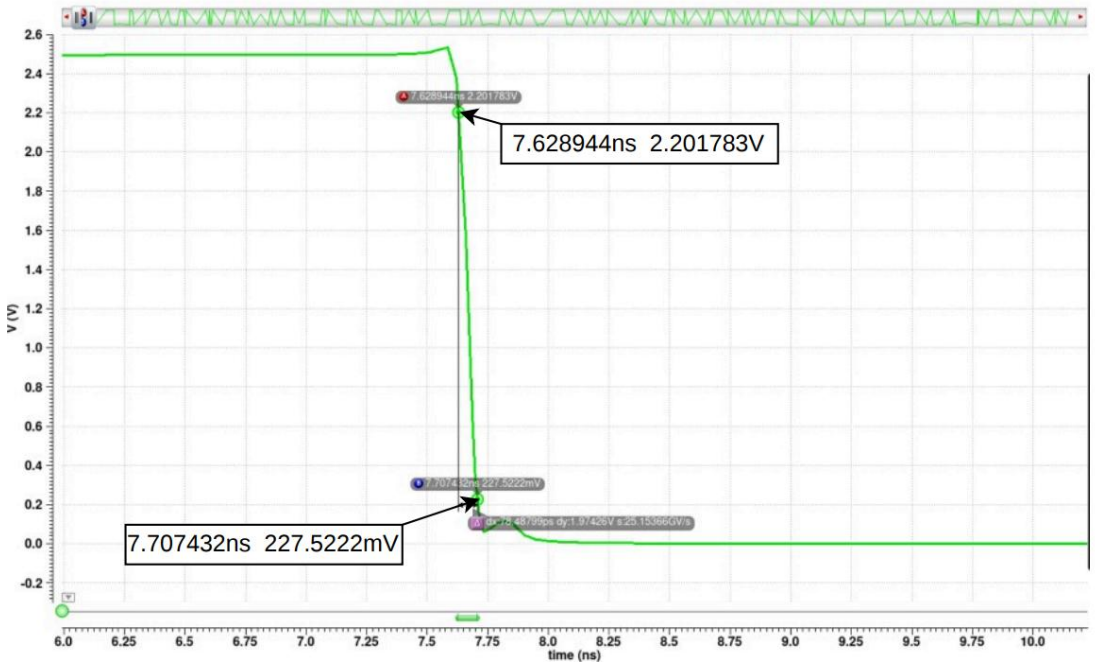


Figure 4.26: Falling Edge of V_{obuff_out} with V_{DD} at 2.5 V

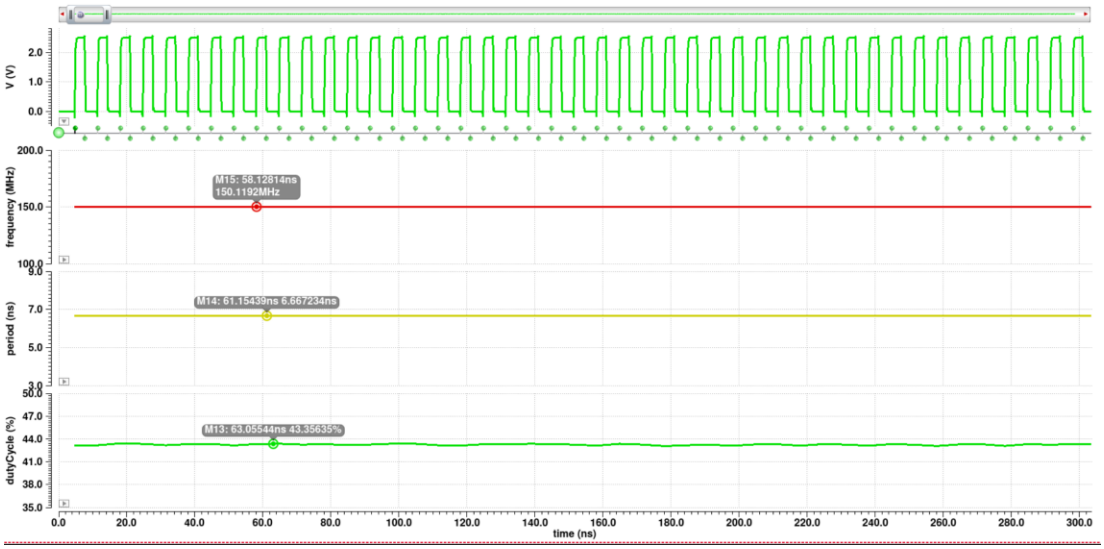


Figure 4.27: Measurement Result of V_{obuff_out}, Frequency (Red), Period (Yellow) and Duty cycle (Green) with V_{DD} at 2.5 V

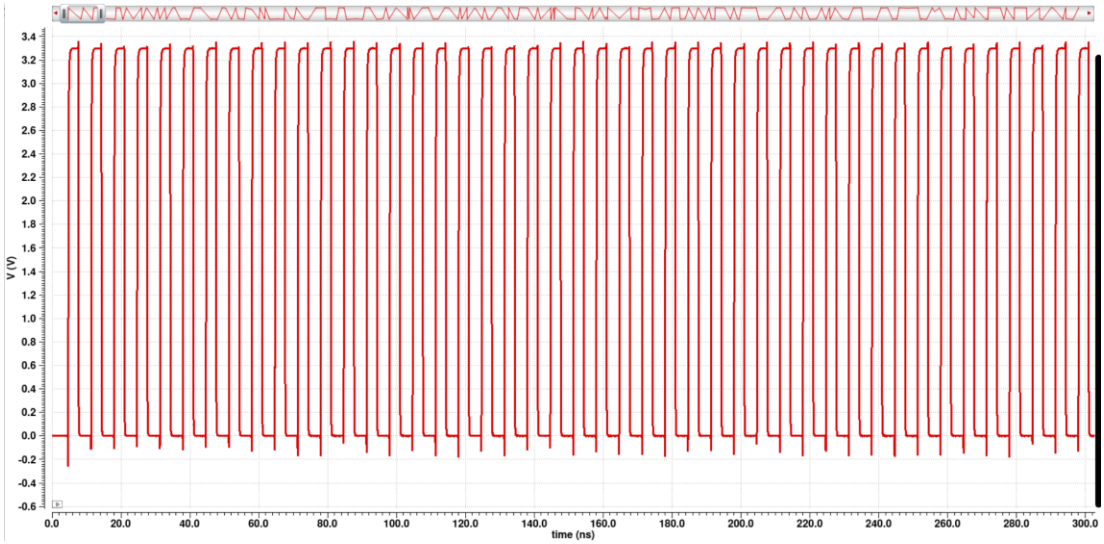


Figure 4.28: Transient Response of Output Buffer, V_{obuff_out} with V_{DD} at 3.3 V

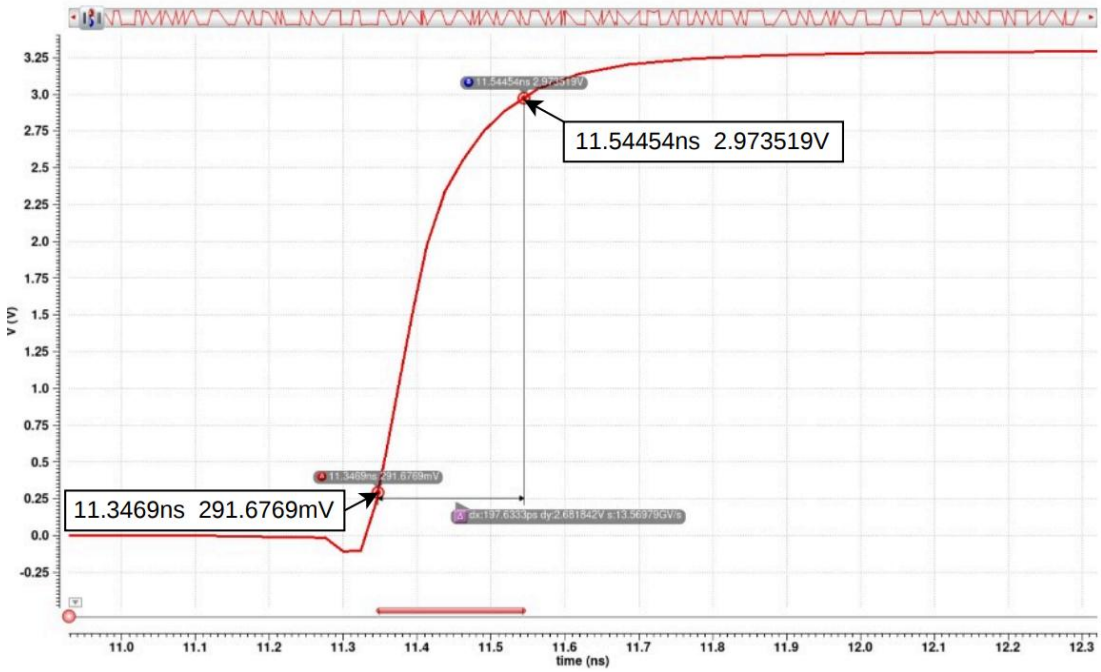


Figure 4.29: Rising Edge of V_{obuff_out} with V_{DD} at 3.3 V

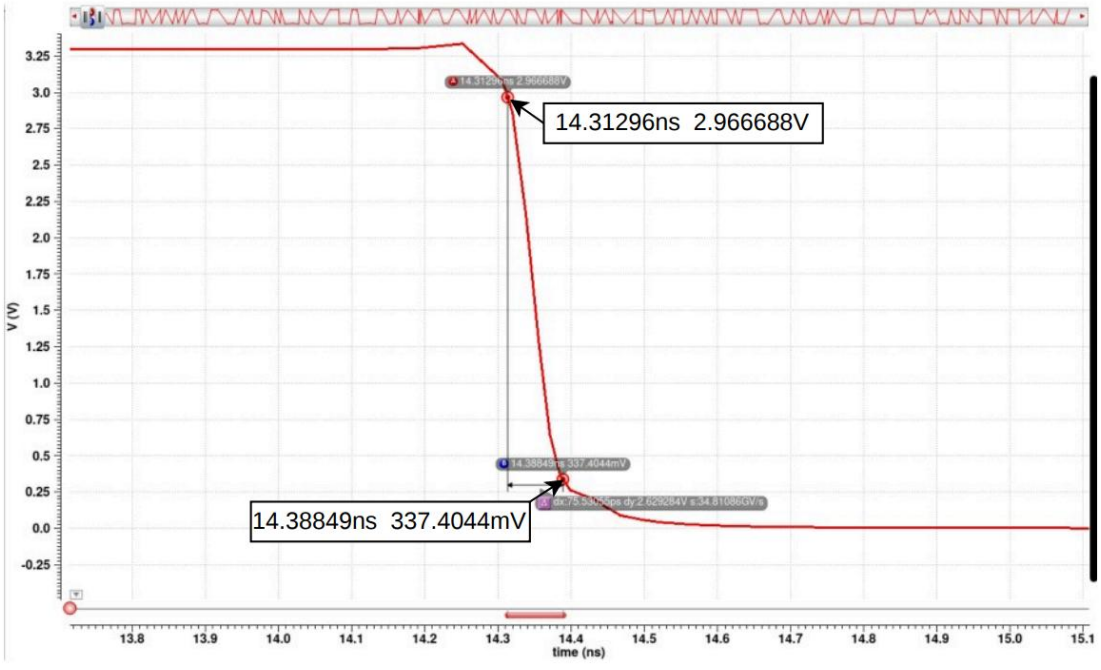


Figure 4.30: Falling Edge of V_{obuff_out} with V_{DD} at 3.3 V

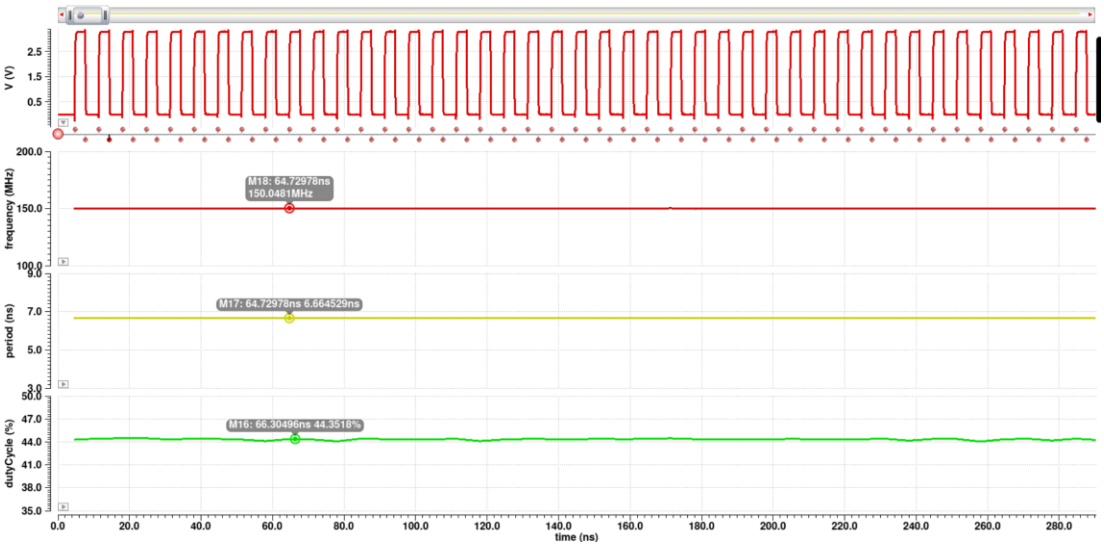


Figure 4.31: Measurement Result of V_{obuff_out}, Frequency (Red), Period (Yellow) and Duty cycle (Green) with V_{DD} at 3.3 V

The simulation results of the output buffer are shown in Figures 4.20 to Figure 4.31. This output buffer improves the clocking square wave quality by reducing the rising time from 706.05 ps to 300 ps in 1.8 V supply voltage, while operating in the same frequency. Furthermore, analysing the performance across variable voltage corners reveals a critical synergy between the level shifter and the output buffer. The transition performance of the level shifter fluctuates significantly depending on the supply voltage. Where, it performs poorly at 1.8 V but improves significantly at 3.3 V due to the stronger pull-up ability of the PMOS transistors. In contrast, the output buffer effectively normalizes the signal across all corners. Regardless of how much the level shifter struggles with propagation delay at lower voltages, the progressive inverter chain absorbs the timing penalty and consistently outputs a sharp, high quality square wave. Together, these two blocks ensure that the rigorous voltage and current demands of the 150 MHz charge pump are met securely, establishing a highly stable foundation for the entire NMOS LDO system.

4.2.4 Summary of Each Clocking Block Performance

Table 4.1: Summarized Result of Each Blocks in Clocking Generation and Conditioning

Outputs	V_{DD} Corner (V)	Frequency (MHz)	Duty Cycle (%)	Rise Time (t_r) (ps)	Fall Time (t_f) (ps)
SDC	1.2 (Core)	150	45.10	21.48	21.43
Level Shifter	1.8	150	43.80	706.05	232.51
	2.5	150	43.30	516.03	341.68
	3.3	150	45.60	442.12	466.86
Output Buffer	1.8	150	40.30	300.12	103.04
	2.5	150	43.30	252.77	78.49
	3.3	150	44.30	197.63	75.53

In short, the clocking system successfully generates and conditions a robust 150 MHz differential clock signal across all variable voltage corners (1.8 V, 2.5 V, and 3.3 V). The Single to Differential Converter (SDC) initiates the process within a low-power 1.2 V domain, producing pristine square waves with ultra-fast transition time around 21 ps. The level shifter accurately scales this 1.2 V amplitude to match the main supply, though it inherently introduces propagation delays, such as a rise time of 706 ps at the lowest 1.8 V corner, due to the NMOS network fighting the cross-coupled PMOS load. To counteract this signal degradation, the progressively sized (1:2:4:16) output buffer acts as a critical signal conditioner. It effectively absorbs the level shifter's delay, sharpening the sluggish edges back down to 300 ps and maintaining a balanced 40 % to 45 % duty cycle. Together, these blocks ensure the massive capacitive load of the

downstream charge pump is driven efficiently without catastrophic high-frequency ringing or shoot-through currents.

4.3 Charge Pump Result

Following an analysis of the clock signal integrity from previous blocks, the charge pump was optimized for the highest efficiency which minimize the voltage drop across the transistor and maximize the efficiency for the charge pump. Besides, the transient characteristics of the output signal and voltage are also important, including the setup time and output voltage ripple. These parameters are critical to maintaining the signal integrity and noise performance of the overall LDO system.

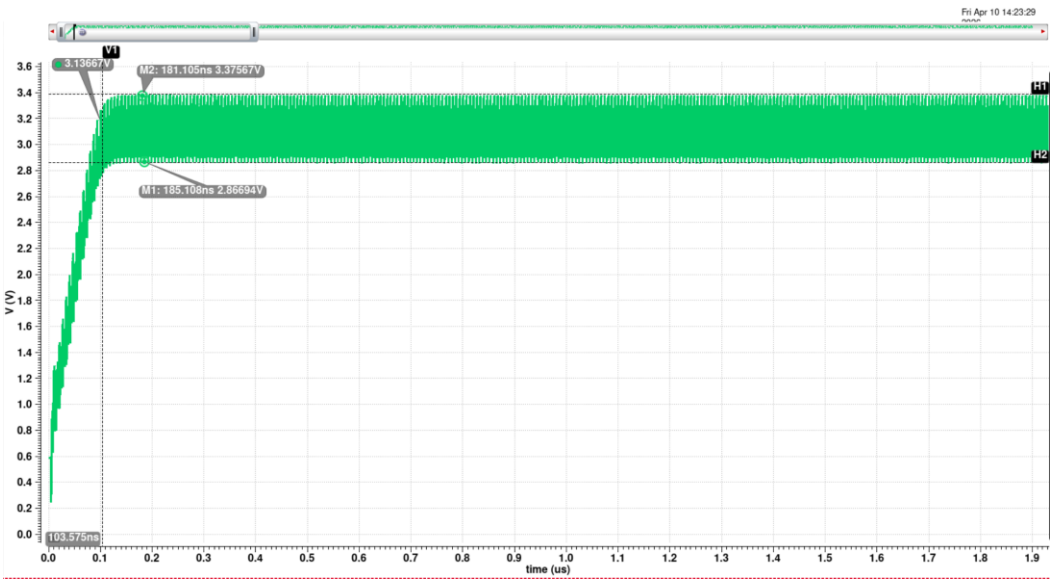


Figure 4.32: Transient Response of Charge Pump Output Signal with V_{DD} at 1.8 V

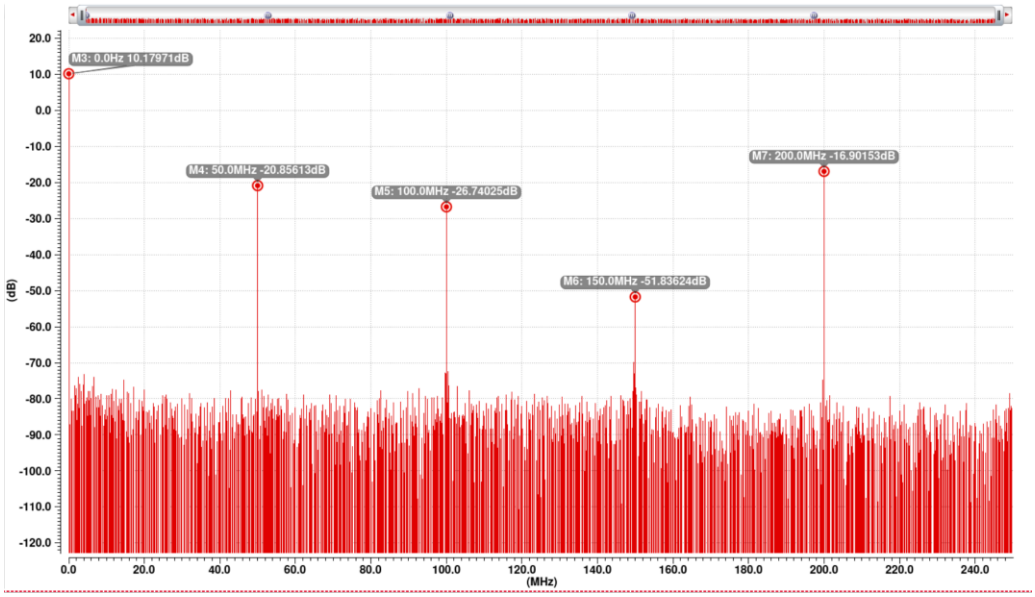


Figure 4.33: FFT Result of Charge Pump Output Signal with V_{DD} at 1.8 V

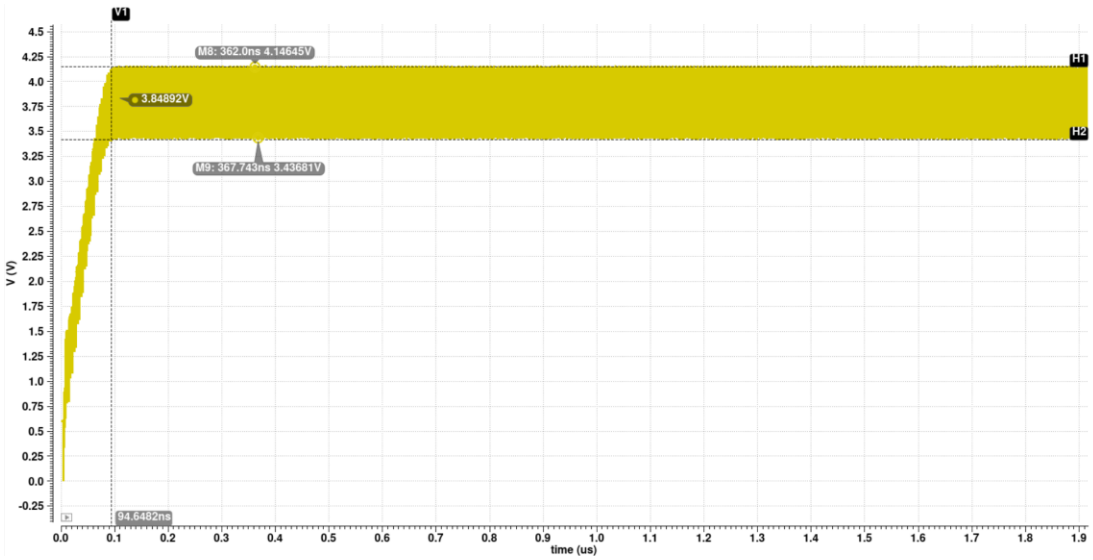


Figure 4.34: Transient Response of Charge Pump Output Signal with V_{DD} at 2.5 V

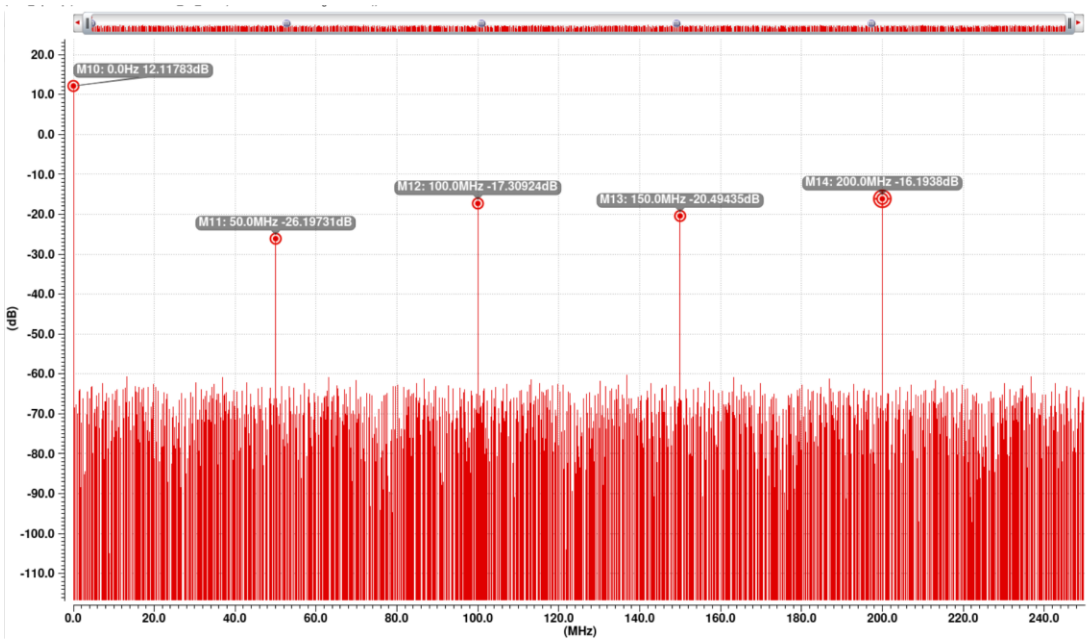


Figure 4.35: FFT Result of Charge Pump Output Signal with V_{DD} at 2.5 V

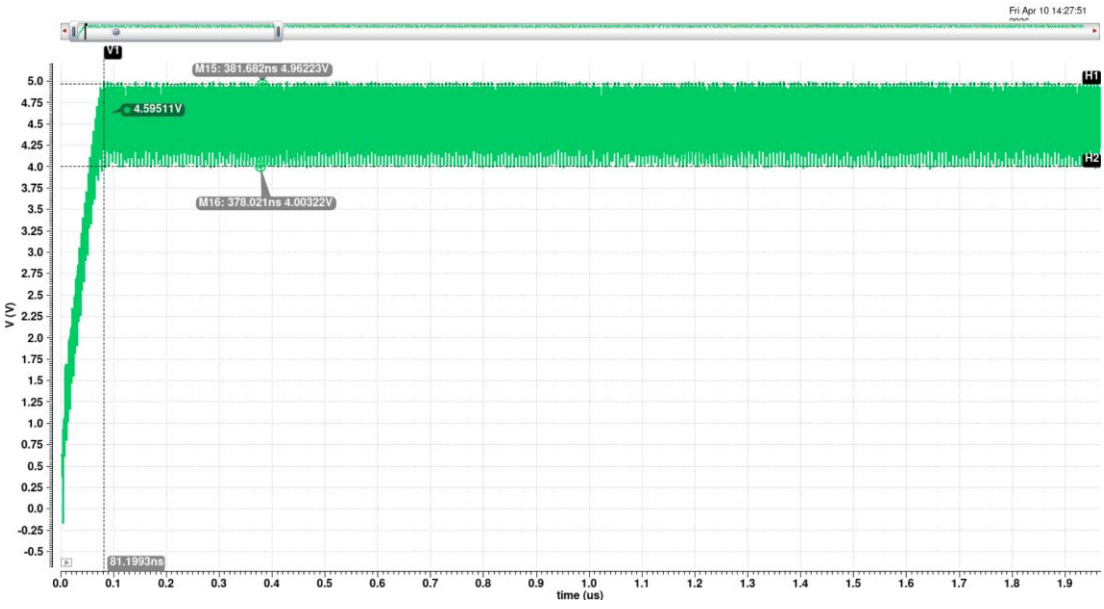


Figure 4.36: Transient Response of Charge Pump Output Signal with V_{DD} at 3.3 V

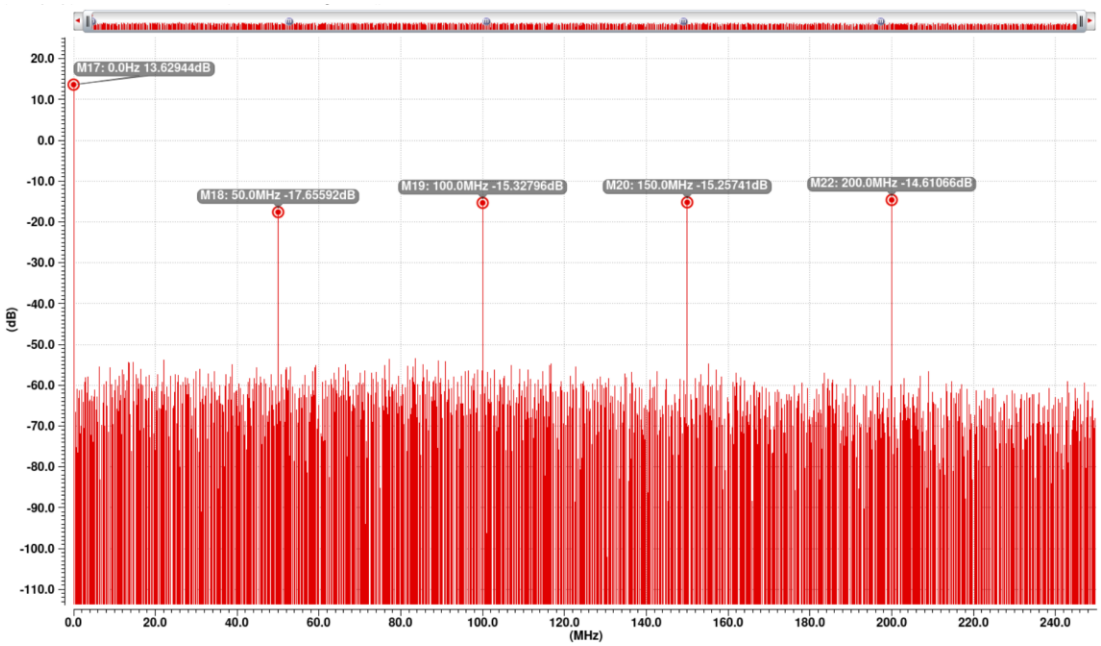


Figure 4.37: FFT Result of Charge Pump Output Signal with V_{DD} at 3.3 V

Figure 4.32, Figure 4.34 and Figure 4.36 show the transient response of the charge pump output signal at 1.8 V, 2.5 V and 3.3 V respectively. In the 1.8 V corner, which is the most critical corner, the charge pump needs to provide enough headroom for the NMOS pass transistor and the cascading stage in the op-amp in saturation region. This simulation result shows that this proposed charge pump achieves the startup time of approximately 103.58 ns. When it was stabilized, the output voltage is oscillating between the maximum of 3.37 V and minimum of 2.87 V, having a 508.7 mV peak-to-peak voltage ripple. The average output voltage is around 3.236 V, which exceed the minimum requirement for the NMOS pass transistor and op-amp.

Besides, in 2.5 V corner, with a higher supply voltage, the charge capability increases. The startup time improves to approximately 94.65 ns. The output voltage ranges from 3.44 V to 4.15 V, exhibiting an increased peak-to-peak ripple of 709.6 mV, and average output voltage is 4.05 V. On the other hand, At the highest supply corner, 3.3 V corner, the control circuit actively intervenes to short the third stage and operate the pump as a 2-stage architecture to prevent oxide breakdown. The startup time is the fastest at 81.20 ns. The output voltage operates safely between 4.00 V and 4.96 V, with a peak-to-peak ripple of 959.0 mV.

To evaluate the noise profile injected by the charge pump switching, a fast Fourier transform (FFT) analysis was conducted on the output signals. Figures 4.33, 4.35, and 4.37 present the frequency spectrum across the three voltage corners. In all the corners, the highest magnitude occurs at DC, with the value of 10.18 dB, 12.12 dB, and 13.63 dB for 1.8 V, 2.5 V, and 3.3 V respectively. These results show the proposed charge pump successfully performs DC-to-DC conversion. Due to this charge pump was driven by the clocking signal of 150 MHz, a significant harmonic spike shows at exactly 150 MHz across all corners. The magnitude of this switching noise is –51.84 dB at 1.8 V, –20.49 dB at 2.5 V, and –15.26 dB at 3.3 V. Additional sub-harmonics and higher-order harmonics are also observed at 50 MHz, 100 MHz, and 200 MHz, largely caused by the clock feedthrough and charge injection from the parasitic capacitances of the switching transistors.

The results show that the proposed charge pump have a better performance at higher supply voltages with improved efficiency and startup time, increasing the peak-to-peak ripple and the magnitude of the 150 MHz switching harmonic. This high-frequency ripple is primarily driven by clock feedthrough, where the 150 MHz square wave being coupled through the C_{GS} and C_{GD} parasitic capacitances of the pumping transistors. If this ripple of 950 mV is fed directly into the gate of the NMOS pass transistor, it would severely modulate the LDO output and causing the PSRR performance to fail. Therefore, these FFT results strongly justify the decision to include the RC low pass filter (LPF) between the error amplifier output and the pass transistor gate. The LPF is explicitly required to attenuate these high frequency harmonics, ensuring that the heavy switching ripple produced from the charge pump does not compromise the sensitive analog regulation of the LDO.

In summary, the proposed charge pump can boost up the supply voltage to the necessary level as to the op-amp to overcome the headroom limitation inherent in the NMOS-based LDO in all the voltage corners.

4.4 Overall LDO System Result

After discussing about the performance of the individual blocks, such as the clocking signal generation and enhancement system and the charge pump, this section shows the comprehensive revolution for the whole integrated NMOS-based low dropout (LDO) voltage regulator system. This system level analysis is used to verify and analyse the proposed folded cascode op-amp and overall LDO block is able to meet the high noise reduction performance for the IoT or SoC applications. The following results were obtained by performing the detailed simulations of the entire system under various of power supply ranging in 1.8 V, 2.5 V and 3.3 V, a full temperature spectrum, including -40 ºC, 40 ºC and 125 ºC, and across the process corners. These results present to ensure the loop stability and noise suppression of the entire system, to maintain a stable 1.2 V output while delivering a load current up to 5 mA.

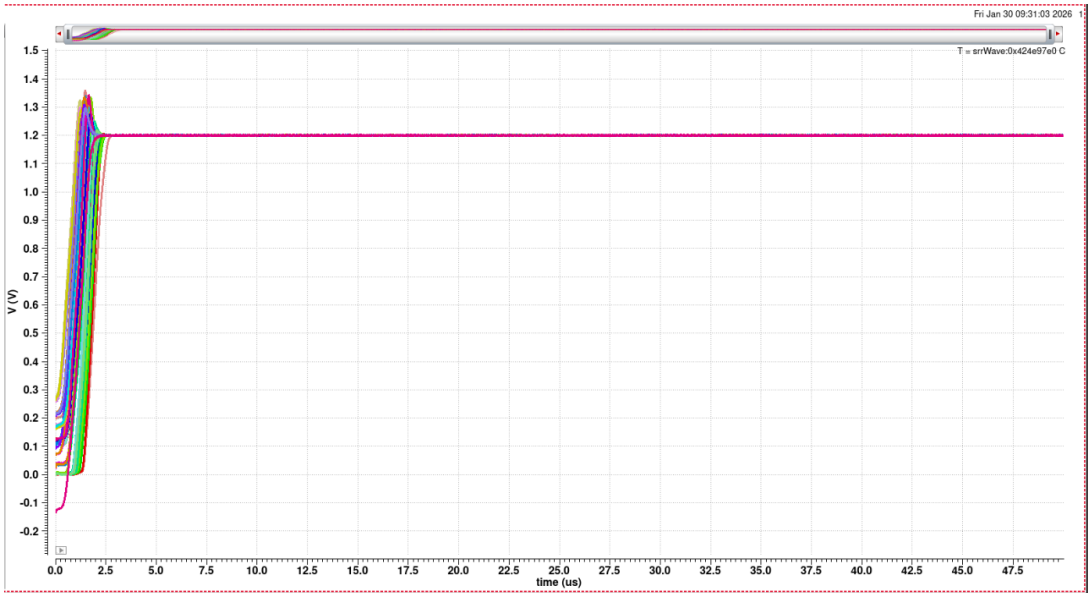


Figure 4.38: Transient Response of Full LDO System in Full Corners

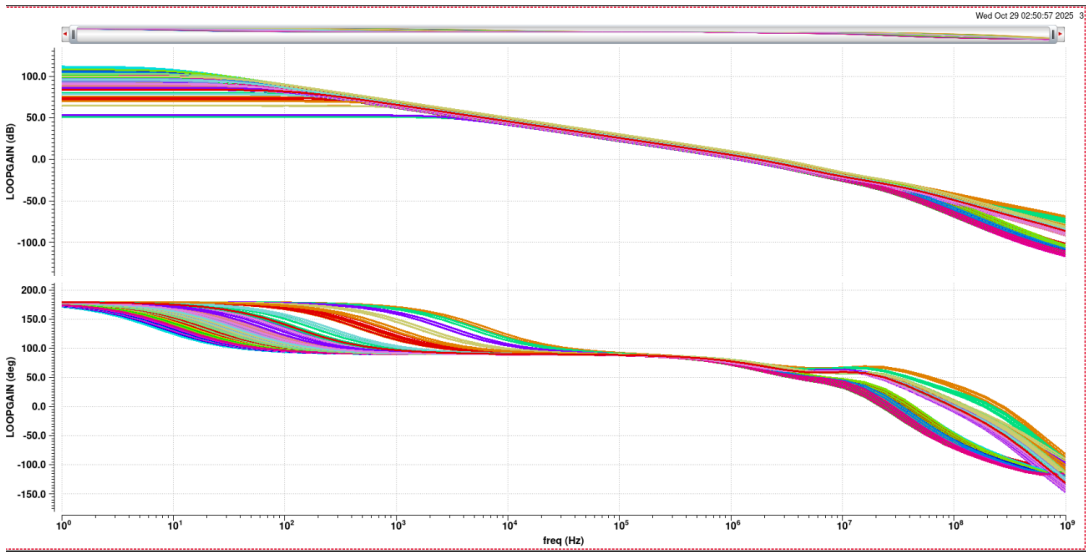


Figure 4.39: Gain and Phase Response of Full LDO System in Full Corners

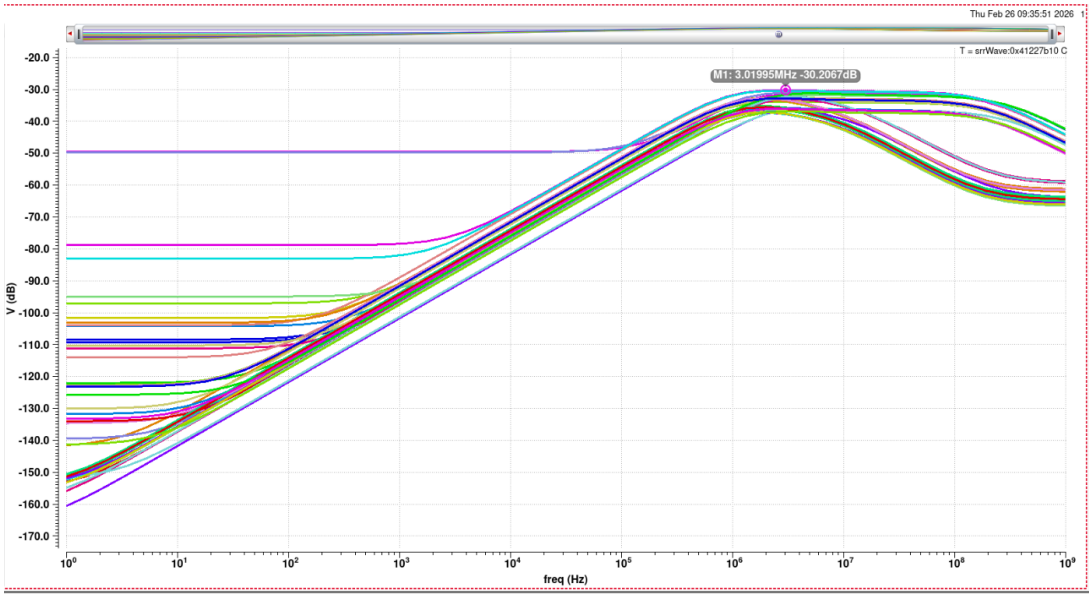


Figure 4.40: PSRR of Full LDO System in Full Corners

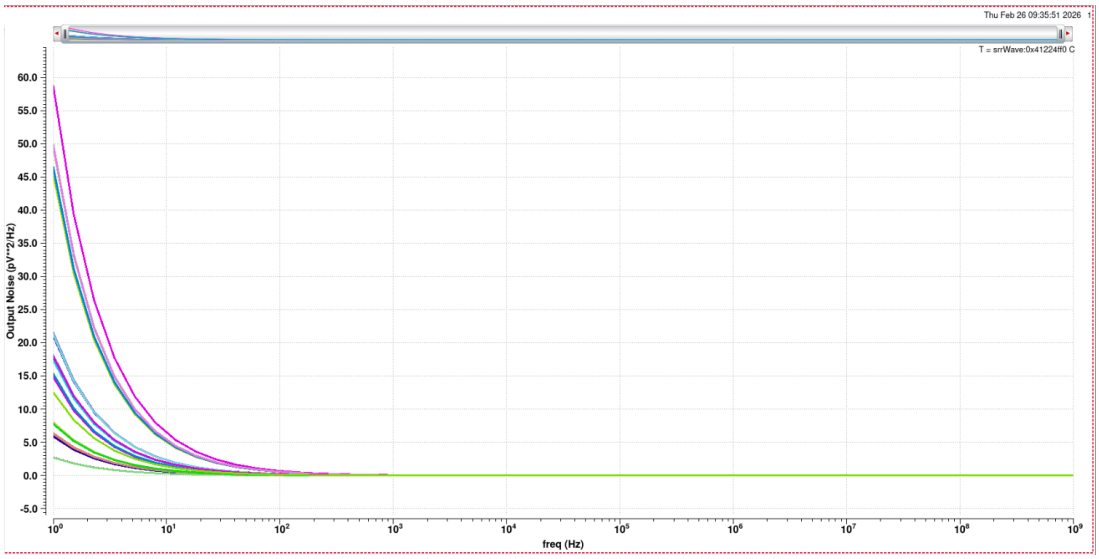


Figure 4.41: Spot Noise Analysis of Full LDO System in Full Corners

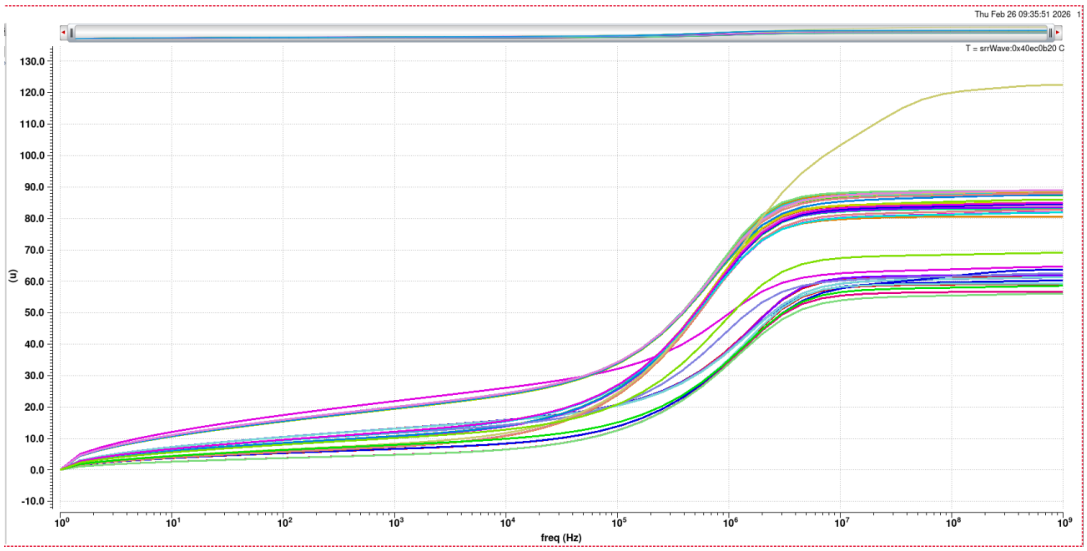


Figure 4.42: Integrated Noise Analysis of Full LDO System in Full Corners

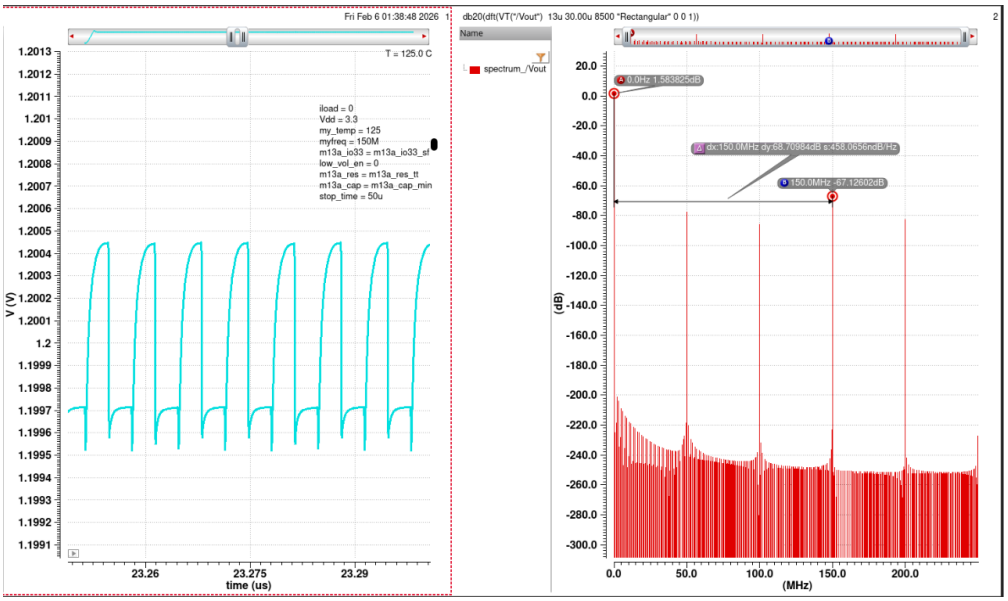


Figure 4.43: Worst-Case Transient Response (left) and Its Corresponding FFT analysis (right)

Table 4.2: Summarized Result of Full LDO System in Full Corners

Outputs	Proposed LDO System			
	0 A load		5 mA load	
	Minimum	Maximum	Minimum	Maximum
Average of V_{out} (V)	1.197	1.2	1.2	1.2
Gain_Margin (dB)	33.38	40.03	46.37	56.92
Phase Margin (º)	64.34	71.65	68.01	74.15
Phase Dip (º)	89.5	91.65	56.94	66.59
Frequency of Phase Dip Located (Hz)	72.44 k	47.863 k	10.47 k	6.91 k

Table 4.2: Summarize Result of Full LDO System in Full Corners (cont'd)

Outputs	Proposed LDO System			
	0A load		5 mA load	
	Minimum	Maximum	Minimum	Maximum
PSRR in DC (dB)	-160.6	-101.7	-151.5	-49.58
PSRR in 100MHz (dB)	-59.95	-50.64	-38.1	31.53
Maximum PSRR (dB)	-37.22	-32.2	-36.82	-30.21
Frequency of Maximum PSRR Located (Hz)	1.955 M	3.02 M	3.02 M	3.02 M
Spot Noise at 1KHz ($\frac{V^2}{Hz}$)	4.785 f	69.52 f	4.746 f	81.05 f
Spot Noise at 10KHz ($\frac{V^2}{Hz}$)	1.556 f	11.46 f	1.547 f	11.46 f
Spot Noise at 100KHz ($\frac{V^2}{Hz}$)	1.209 f	5.276 f	1.202 f	5.252 f
Integrated Noise at 1MHz ($\frac{V^2}{Hz}$)	33.81 µ	68.73 µ	33.4 µ	67.73 µ
Integrated Noise at 100MHz ($\frac{V^2}{Hz}$)	56.57 µ	88.75 µ	55.45 µ	119.9 µ

Table 4.2 summarizes the simulation results conducted for the proposed LDO design, demonstrating highly precise static regulation across all of the simulation corners. The LDO successfully maintains a stable output voltage with an average value

between 1.197 V to 1.2 V, regardless in no load or full load (5 mA) conditions. The simulation results confirm this LDO can produce a stable 1.2 V output with a small error of 3 mV, under full process, voltage and temperature corners, ensuring the robustness of the unity feedback network and op-amp to tracking the difference between the feedback voltage (V_{fb}) and the reference voltage (V_{REF}), despite of external fluctuation.

In addition, regarding the frequency response and loop stability, the LDO demonstrates the exceptional performance, exceeding the initial design spec significantly. The system can achieve a minimum phase margin of 64.34º at no load and rising to 74.15º under full load, which is well beyond the standard stability requirement of 45º for this project. The gain margin ranges from 33.38 dB to 56.92 dB across all the corners. These stability performances validate the architecture decision of choosing the folded cascode op-amp as the error amplifier in this work. This topology provides good stability and high loop gain without requiring any Miller network by pushing the non-dominant pole to a higher frequency, optimizing the overall area while maintaining a high performance.

The power supply rejection ratio (PSRR) and noise analysis further highlighting the noise performance for the high-performance applications. The proposed system can block the supply noise, with the PSRR values are able to achieve as low as -160.6 dB under light load conditions. In high frequency conditions, especially in 100 MHz, the PSRR maintains generally between -38.1 dB to -59.95 dB. Moreover, the integrated noise analysis shows the value of 119.9 μ$\frac{V^2}{Hz}$ at 100 MHz in full load condition, and the spot noise was controlled between 1.202 $f\frac{V^2}{Hz}$ to 5.252 $f\frac{V^2}{Hz}$. Besides, Figure 4.43 shows the worst case transient and its corresponding FFT result. Under the worst-case scenario, the LDO system having the output voltage at 1.2 V with the ripple of 1 mV, while having the FFT in the steady state of the output voltage, the spectrum reveals the same harmonic component at 50 MHz, 100 MHz, and 150 MHz, being carried from the charge pump. However, the magnitudes of these harmonics are suppressed to a maximum of -67.13 dB, which is considerably lower than the levels observed in typical process corners. The effectiveness of this noise suppression is largely attributed to the strategic placement of the RC low pass filter (LPF) between the OTA output and the pass transistor gate, which filters out high-

frequency ripples, particularly the 150 MHz switching noise from the charge pump, before they can modulate the output.

In the final analysis overall system performance, the integration of the cross-coupled charge pump and the proposed clocking blocks successfully overcomes the primary limitations of NMOS pass transistors. The charge pump ensures the NMOS device remains securely in the saturation region for optimal current drive and regulation by generating a steady gate overdrive voltage that exceeds the required 2 V threshold even when the main supply is at its lowest corner of 1.8 V. While the charge pump introduces significant switching noise at 150 MHz due to clock feedthrough and charge injection, the FFT and PSRR results justify the necessity of the LPF to attenuate these harmonics. In short, the system meets all targeted specifications for stability, transient response, and noise rejection, proving that this architecture is a robust and power-efficient power management solution for modern SoC and IoT devices.

4.5 Regulatory Performance and Power Analysis

This subchapter evaluates the static regulatory capabilities of the LDO, especially focus on the ability to maintain a stable output across all conditions. The key performance parameter discussed include quiescent current (I_Q), load and line regulation, and overall power consumption, which are critical for the efficiency of the power management system in IoT applications.

4.5.1 Quiescent Current

The quiescent current is the current consumed by the LDO itself to maintain regulation in no load condition, defined by the difference between input and output current. For this work, the total I_Q is primarily dominated by the bias currents in the folded cascode op-amp and the switching current of the charge pump. The OTA is designed with a total cascading branch current of 30 μA, with the input NMOS differential pair consuming 5 μA for each transistor. This low-power biasing strategy ensures that the

regulator remains energy-efficient during idle states, which is a key requirement for extending battery life in portable SoC devices.

4.5.2 Load Regulation

Load regulation measures the LDO's ability to maintain a constant 1.2 V output while the load current changes from no-load (0 A) to full-load (5 mA). As discussed in previous section, the average output voltage remains remarkably consistent, rolling between 1.197 V and 1.2 V across all simulation corners.

This high level of precision indicates that the NMOS-based regulator possesses a very low output impedance, allowing it to respond rapidly to current steps without significant voltage drop or undershoot. The intrinsic transconductance of the NMOS pass transistor actually increases as the load current rises, which enhances loop gain and improves regulatory accuracy under heavy loads. This results in a stable supply voltage that is essential for preventing functional errors in sensitive digital and analog subsystems within a System on Chip (SoC).

4.5.3 Line Regulation

Line regulation evaluates the stability of the 1.2 V output voltage as the input supply voltage varies across the designed range of 1.8 V to 3.3 V. The simulation data confirms that the LDO maintains excellent regulation throughout this wide input spectrum. The successful integration of the charge pump is the primary driver for this performance; by providing a gate overdrive voltage that scales dynamically with the input supply, the system ensures the NMOS pass transistor never enters the linear region, even when the input voltage is at its minimum of 1.8 V.

4.5.4 Power Consumption

Table 4.3 illustrated the average power consumption of each sub-block and the total system across the supply voltage and load conditions. This analysis showcasing and evaluating the efficiency of the NMOS LDO, with the high frequency clocking system and charge pump included which introduce additional power requirement and penalties to achieve the gate overdrive.

Table 4.3: Average Power Consumption in Each Block

	Average Power Consumption (W)					
Load	0 A	5 mA	0 A	5 mA	0 A	5 mA
SDC	5.4972 m	5.4972 m	7.755 m	7.7525 m	10.1904 m	10.2003 m
Level Shifter	128.33 µ	128.34 µ	256.14 µ	58.349 µ	73.71 µ	73.755 µ
Output Buffer	24.066m	24.066 m	56.45 m	56.475 m	125.73 m	125.565 m
Charge Pump	140.56 µ	139.73 µ	258.25 µ	255.75 µ	198.33 µ	90.321 µ
LDO	84.67 µ	9.08 m	117.95 µ	12.62 m	156.55 µ	16.68 m
Total	54.24 m	63.24 m	121.80 m	133.75 m	262.23 m	278.32 m

According to the results shown in Table 4.3, majority of the power is consumed by the clocking system specifically in the SDC and output buffer. In the 1.8 V supply corner, the SDC consumed 5.497 mW, while the output buffer accounts for a 24.07 mW per branch. While increasing the V_{DD} from 1.8 V to 3.3 V, the power consumption of the output buffer jumps to 125.73 mW, because this power consumption of each block increases with V_{DD}. This high-power consumption is an architecture trade-off

between the frequency and the efficiency of the charge pump, which the charge pump requires a high-quality clocking signal and frequency to enhance the efficiency of the flying capacitor, Consequently, the output buffers must provide significant driving strength to maintain sharp transition edges, which inherently increases the dynamic power dissipation of the system.

Besides, the power consumption of the LDO block is heavily dependent on the load current. In 1.8 V V_{DD} corner, the LDO block consumes only 84.67 µW in no-load condition. With the load increased to 5 mA, the power consumption of the LDO block increases significantly to 9.08 mW. This increase is expected for the NMOS pass transistor to handle the full current load. Furthermore, the charge pump and level shifter blocks maintain a low power consumption in the range of µW in all conditions, showing the efficient voltage translation and charge transfer with a minimal leakage loss.

In overall, the total power consumption ranging from 54.24 mW in 1.8 V no-load condition, to 278.32 mW at 3.3 V with full load. Because of the clocking system circuit has a certain power consumption requirement, this proposed variable voltage supply NMOS-based LDO with clocking system can achieve the primary objectives, which this system is able to operate in a low-voltage up to 1.8 V. The results confirm that the system is robust and capable of delivering a stable 1.2 V supply, with the higher power consumption being a necessary cost for the improved transient response and smaller silicon area offered by the NMOS architecture.

4.6 Summary

In short, this chapter showing the simulation result of each block and entire system level, ensuring the proposed system is able to achieve a high performance across all of the simulation corners, including different process, voltage and temperature (PVT) corners. The designed clocking enhancing system is able to generate a robust 150 MHz square wave with a sharp rising and falling edge, enhancing the Charge Pump performance. Besides, the Charge Pump was designed to overcome the headroom issue faced by the NMOS-based LDO, by maintaining a steady supply exceeding a 3 V to

increasing the headroom of Folded Cascode op-amp, and the pass transistor, ensuring all the designed transistor work in the saturation region. On the other hand, the overall system simulation result validates the architecture selection of the folded cascode op-amp instead of using a traditional two-stage op-amp, archiving a high loop stability without any Miller compensation network, reducing the silicon area, and good noise reduction. Although the high frequency clocking system required a high-power consumption, the regulator showing a highly precise line and load regulation with a minimal of 3 mV of error output, proving the robustness as a power management solution for modern SoC and IoT applications.

CHAPTER 5

CONCLUSION AND RECOMMENDATIONS

5.1 Conclusion

In conclusion, the four objectives of this project have been successfully achieved. This project demonstrates the design and implementation of robust and high performance of NMOS-based low dropout (LDO) voltage regulator, by integrating a charge pump in Silterra 130nm CMOS technology. The primary objective of this project was to overcome the limitations of NMOS pass transistor in low-voltage supply, which achieved effectively in this work through a specialized voltage boosting architecture.

In addition, the simulation results confirm that the overall integrated system is able to maintain a highly stable 1.2 V output across a wide range input voltage supply range including 1.8 V, 2.5 V and 3.3 V, a full temperature range of -40 ºC to 125 ºC, and all the process corners. The proposed cross-coupled charge pump provides a gate overdrives voltage exceeding the requirement of 2 V threshold at the gate voltage of the NMOS pass transistor, even in the low-voltage supply corners, ensuring the pass transistor work in the saturation region for optimal regulation.

Furthermore, the implementation of the folded cascode op-amp as the error amplifier was proved highly effective. The system achieved exceptional loop stability with the minimum phase margin of 64.34º exceeding the design target of 45º significantly, without using any area intensive Miller network. Moreover, the noise performance was also excellent, highlighted by a PSRR of -160.6 dB at DC and effective high frequency suppression through a strategic RC low pass filter.

Although the high frequency clocking blocks introduced a baseline power requirement, but the overall designed system demonstrates excellent regulatory accurate and robustness, that fulfilling all of the aims in this project and proving its suitability for the modern SoC and IoT power management applications.

On the other hand, the outcomes of this research align with the United Nations Sustainable Development Goals (SDGs), particularly Goal 9: Industry, Innovation, and Infrastructure, and Goal 12: Responsible Consumption and Production. The development of a stable, multi-voltage power management architecture contributes to continuous innovation in semiconductor infrastructure, supporting the miniaturization and advancement of modern microelectronics. Additionally, by engineering hardware-level over-voltage protection and strict noise suppression mechanisms, the system significantly enhances integrated circuit reliability and lifespan. Preventing the premature breakdown of sensitive analog components directly combats the growing global issue of electronic waste (e-waste), promoting more sustainable engineering practices and responsible consumption within the electronics industry.

5.2 Recommendation

Although the proposed NMOS-based LDO design fulfilling the target performance specifications, several enhancements could further improve its efficiency and versatility for future improvement. A primary part for improvement is the optimization of the clocking network's power consumption. Since the single to differential converter (SDC) and output buffer required for a significant portion of the total power consumption, that is scaling with supply voltage, in the future work could explore low-swing clocking techniques or adaptive stage-sizing in the buffer chain to reduce switching losses without compromising signal integrity.

Additionally, implementing a more effective control logic for the cross-coupled charge pump could minimize output voltage ripple at higher supply levels. By adjusting the number of active pumping stages or the switching frequency based on the input voltage separately, the system could maintain optimal efficiency while further reducing frequency-domain noise injection.

Further research could also focus on extending the regulator's dynamic performance and integration level. Although the single-stage folded cascode OTA provides excellent stability, exploring advanced frequency compensation techniques, such as active compensation or nested Miller loops, could further enhance the transient response bandwidth for ultra-fast load steps.

To maximize the design's applicability in modern System-on-Chip (SoC) environments, migrating the circuit to smaller process nodes like 90 nm or 45 nm would allow the design to leverage higher device mobility and significantly reduce the total silicon footprint.

Finally, future implementations should integrate a dedicated on-chip bandgap reference circuit and oscillating circuit to provide a fully self-contained, temperature-independent reference voltage, and oscillating signal instead of using additional off ship circuit thereby eliminating the need for an external referencing source and completing the power management system.

REFERENCES

Ballo, A., Grasso, A. D. & Palumbo, G., 2019. A Review of Charge Pump Topologies for the Power. *electronics,* 8(480), pp. 1-15.

Bhuiyan, M. A. S., Hossain, M. R., Minhad, K. N. & Haque, F., 2022. CMOSLow-DropoutVoltage Regulator Design Trends: An Overview. *electronics,* 11(193), pp. 1-30.

Castro-López, R., O. Guerra, E. Roca & F. V. Fernández, 2008. An Integrated Layout-Synthesis. *IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS,* 27(7), pp. 1179-1189.

Chyan, T. et al., 2022. Evaluation and Perspective of Analog Low-Dropout Voltage Regulators: A Review.. *IEEE Access,* Volume 10, p. 114469–114495.

Dammak, H. D., Bensalem, S., Zouari, S. & Loulou, M., 2008. Design of Folded Cascode OTA in Different Regions of Operation Through gm/ID Methodology. *International Journal of Electrical and Electronics Engineering,* 1(3), pp. 178-183.

Gokhale, P., Bhat, O. & Bhat, S., 2018. Introduction to IOT. *International Advanced Research Journal in Science, Engineering and Technology,* 5(1), pp. 41-44.

H.Kamel, M. et al., 2019. Comparative Design of NMOS and PMOS Capacitor-less Low Dropout Voltage Regulators (LDOs) Suited for SoC Applications. *NATIONAL RADIO SCIENCE CONFERENCE,* Volume 36, pp. 305-314.

Jusoh, W. M. E. A. W. & Ruslan, S. H., 2019. Design and analysis of current mirror OTA in 45 nm and 90 nm. *Bulletin of Electrical Engineering and Informatics,* 9(1), pp. 221-228.

Palumbo, G. & Pappalardo, D., 2010. Charge Pump Circuits: An Overview on Design Strategies and Topologies. *IEEE CIRCUITS AND SYSTEMS MAGAZINE,* Volume 1, pp. 31-45.

Shahithi, P., Kishore, K. H., Raghuveera, E. & Krishna, P. G., 2018. Design of voltage level shifter for power-efficient applications. *International Journal of Engineering & Technology,* 7(2.8), pp. 103-108.

Sharma, S., Kaur, P., Singh, T. & Kumar, M., 2012. A Review of Different Architectures of Operational. *ResearchGate,* 3(4), pp. 384-388.

Xu, E. & He, X., 2020. Design of a Low-Dropout Linear Regulator. *IEEE International Conference on Artificial Intelligence and Information Systems,* pp. 717-720.

Yadav, A., 2012. A REVIEW PAPER ON DESIGN AND SYNTHESIS OF TWO-STAGE CMOS OPAMP. *International Journal of Advances in Engineering & Technology,* 2(1), pp. 677-688.

Yan, L., Hung Ki, W. & Yue, P., 2016. An NMOS-LDO Regulated Switched-Capacitor DC–DC Converter With Fast-Response. *IEEE TRANSACTIONS ON POWER ELECTRONICS,* Volume 31, pp. 1294-1303.

Yao, J., 2023. Working principle and characteristic analysis of SiC. *Journal of Physics: Conference Series ,* Volume 2435, pp. 1-12.

APPENDICES

Appendix A: Figures

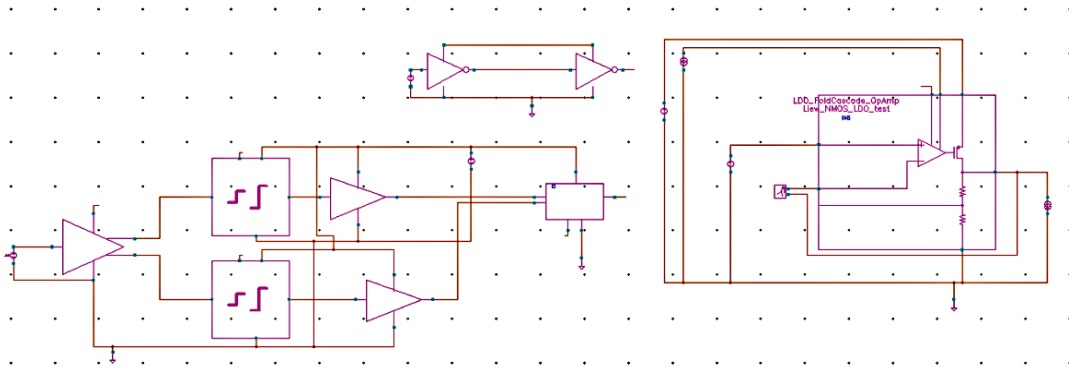


Figure A-1: Testbench of Whole System in Cadence

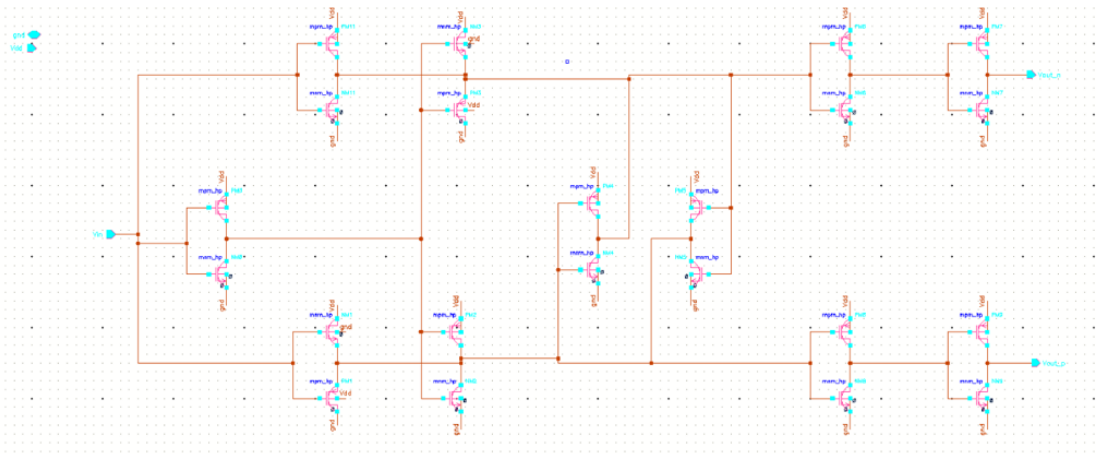


Figure A-2: Schematic Diagram of Proposed SDC in Cadence

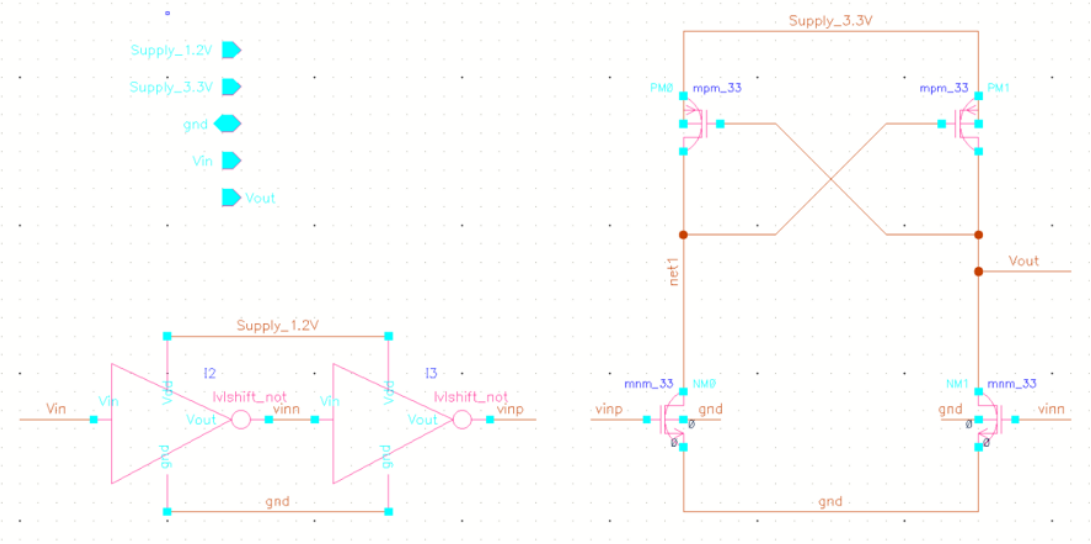


Figure A-3: Schematic Diagram of Proposed Level Shifter in Cadence

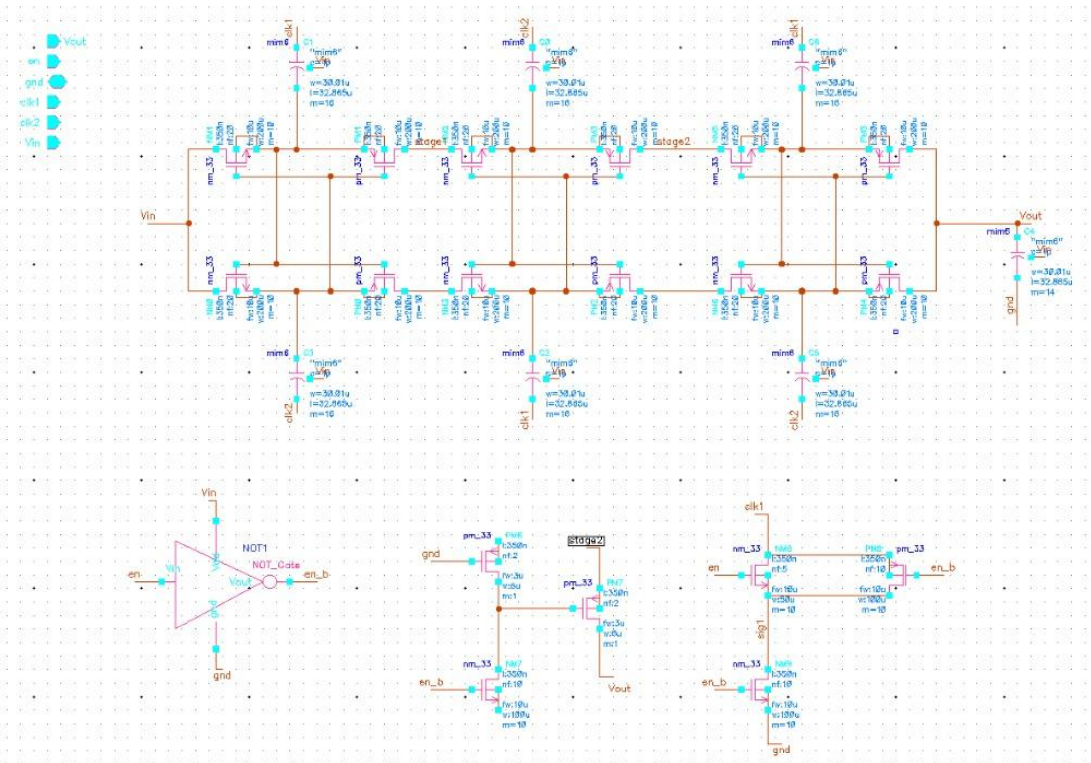


Figure A-4: Schematic Diagram and Transistor Sizing of Proposed Charge Pump in Cadence

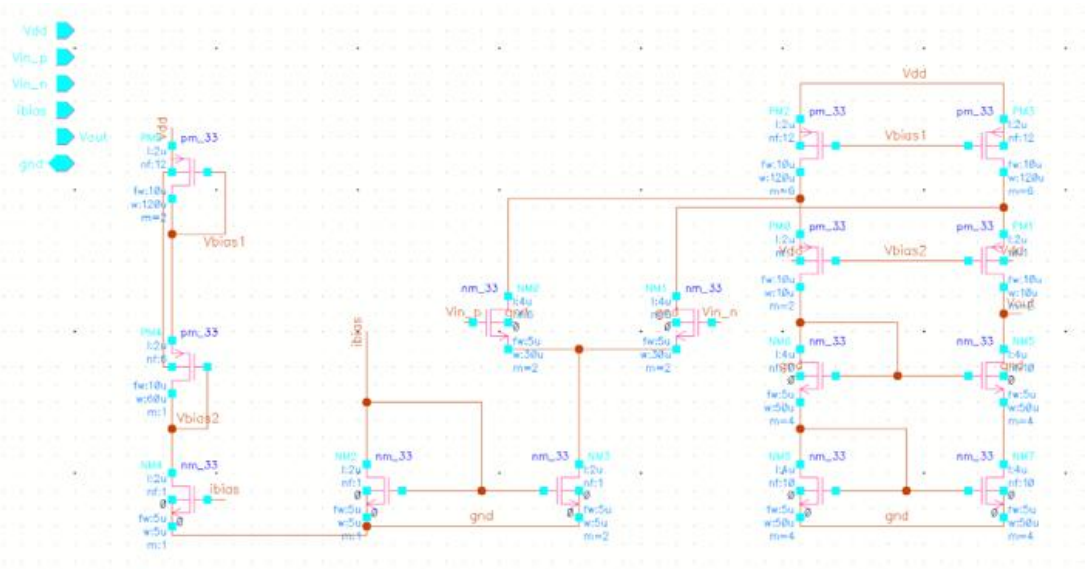


Figure A-5: Schematic Diagram and Transistor Sizing of Proposed Folded Cascode Op-amp in Cadence

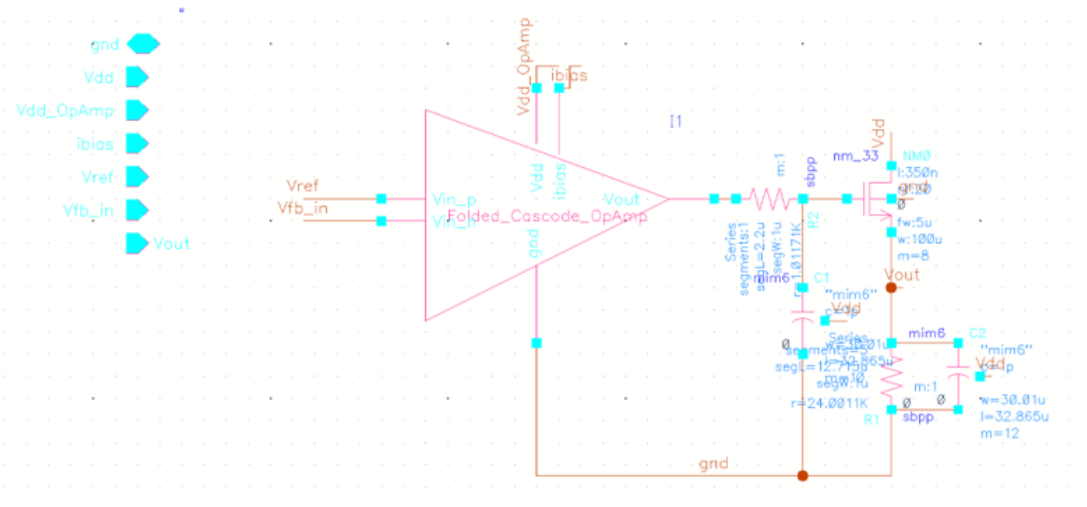


Figure A-6: Schematic Diagram and Transistor Sizing of Proposed LDO in Cadence