FET CURVE TRACER

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A project report submitted in partial fulfilment of the requirements for the award of Bachelor of Engineering (Hons.) Electronics Engineering

Faculty of Engineering and Science
Universiti Tunku Abdul Rahman

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DECLARATION

I hereby declare that this project report is based on my original work except for citations and quotations which have been duly acknowledged. I also declare that it has not been previously and concurrently submitted for any other degree or award at UTAR or other institutions.

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APPROVAL FOR SUBMISSION

I certify that this project report entitled **"FET CURVE TRACER"** was prepared by **GABRIEL GAN KOK WAI** has met the required standard for submission in partial fulfilment of the requirements for the award of Bachelor of Engineering (Hons.) Electronics Engineering at Universiti Tunku Abdul Rahman.

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Date : _____

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FET CURVE TRACER

ABSTRACT

A FET curve tracer is a specialised piece of electronic test equipment used to analyse the characteristic of the FETs. It displays the so-called V-I (voltage versus current) graph on an oscilloscope screen. Whilst the voltage level at “Gate” terminal contributes different characteristic, the curve tracer is specifically designed to plot a series of 8 curves on the screen. These graphs depict vital information regarding to the FET such as the dc current gain, ohmic region, saturation region, transconductance, channel length modulation and etc.

The three terminal device require 2 inputs in order to excrete the output. A stepped voltage is used to supply the control terminal of the Device Under Test (DUT). By sweeping through the full range of main terminal voltage with each step of the control signal, a family of V-I curves can be generated. This project aims for a low-cost terminal device which capable of handling the FETs and the BJTs.

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LIST OF SYMBOLS / ABBREVIATIONS

BJT	Bipolar Junction Transistor
CLM	Channel Length Modulation
DAC	Digital to Analogue Converter
DUT	Device Under Test
etc.	et cetera
FET	Field Effect Transistor
PCB	Printed Circuit Board
RM	Ringgit Malaysia (Malaysia's currency)

CHAPTER 1

INTRODUCTION

1.1 Background

Transistors, nowadays, serve as an important asset from electronic to mass communication field, from mechanical to prestige nanotechnology field. It is virtually a semiconductor device used to amplify and switch electronic signal.

The first generation transistor was known to be vacuum tube, otherwise called electron tube (in North America) or thermionic valve (in Britain) (*Vacuum Tube*, 2010).

Figure 1.1: Early 20th Century Vacuum Tube

http://www.answers.com/topic/vacuum-tube, Retrieved August 20, 2010

Figure 1.1 shows the early 20th century vacuum tube. An American inventor, Lee De Forest, invented the Audion 1906 (*The complete Lee de Forest*, 2005). The vacuum tube triode preceded the transistor by nearly 50 years. It played an important role in the emergence of home electronics and in the scientific discoveries as well as technical innovations which are the foundation for our modern electronic technology.

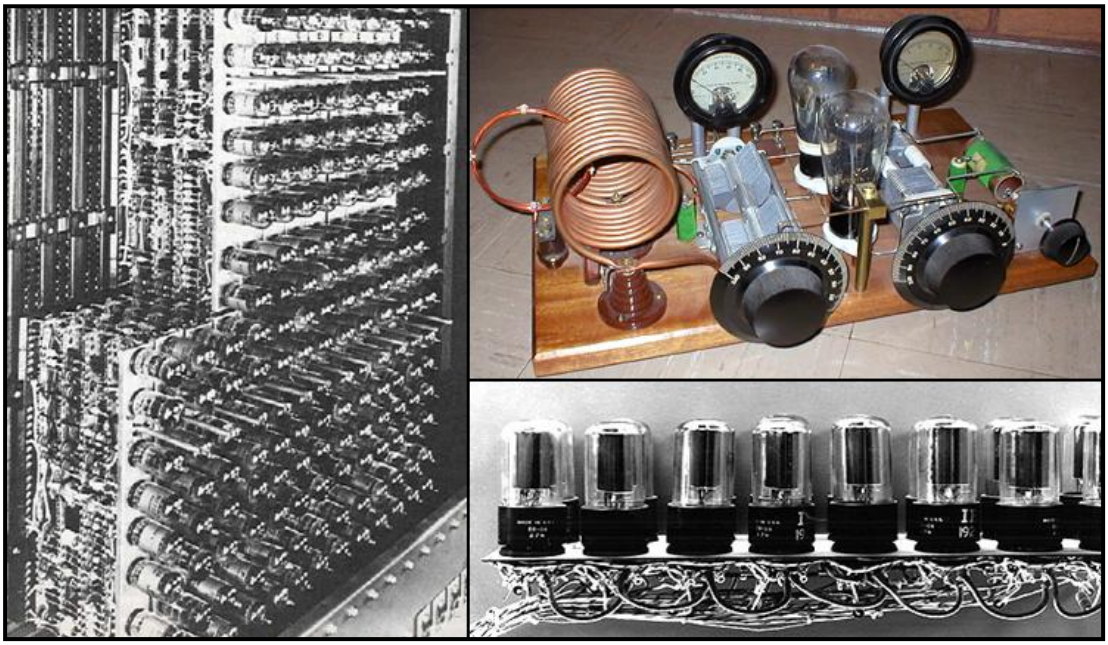


Figure 1.2: (a) Vacuum Tube Computer (Left) (b) Vacuum Tube Radio (Top Right) (c) Vacuum Tube on Computer (Bottom Right).

http://www.plyojump.com/classes/hardware.html, Retrieved August 20, 2010

Figure 1.2 above shows the early computers and radios which use the vacuum tube. The vacuum tube gave the advancement in home electronic devices and military technologies back in the olden days.

Later on, the soared of solid state electronic studies in the mid 20th century contributed to the rose of modern day transistors (*The Transistor in a Century of Electronics*, 2002). The transistor is made of a solid piece of semiconductor material with at least three terminals for connection to an external circuit. There are many types of transistors, namely Bipolar Junction Transistor (BJT) and Field Effect Transistor (FET). Although the technology behind BJT and FET was different, they shared a close relation in their behaviour. Both of them can be used as switch or amplifier. These characteristics provide a total replacement to the vacuum tube. Thus,

modern day transistors led to the revolution of contemporary miniature home electronic devices. Figure 1.3 shows the assortment of several transistors. It varies from encapsulated to high power transistors.

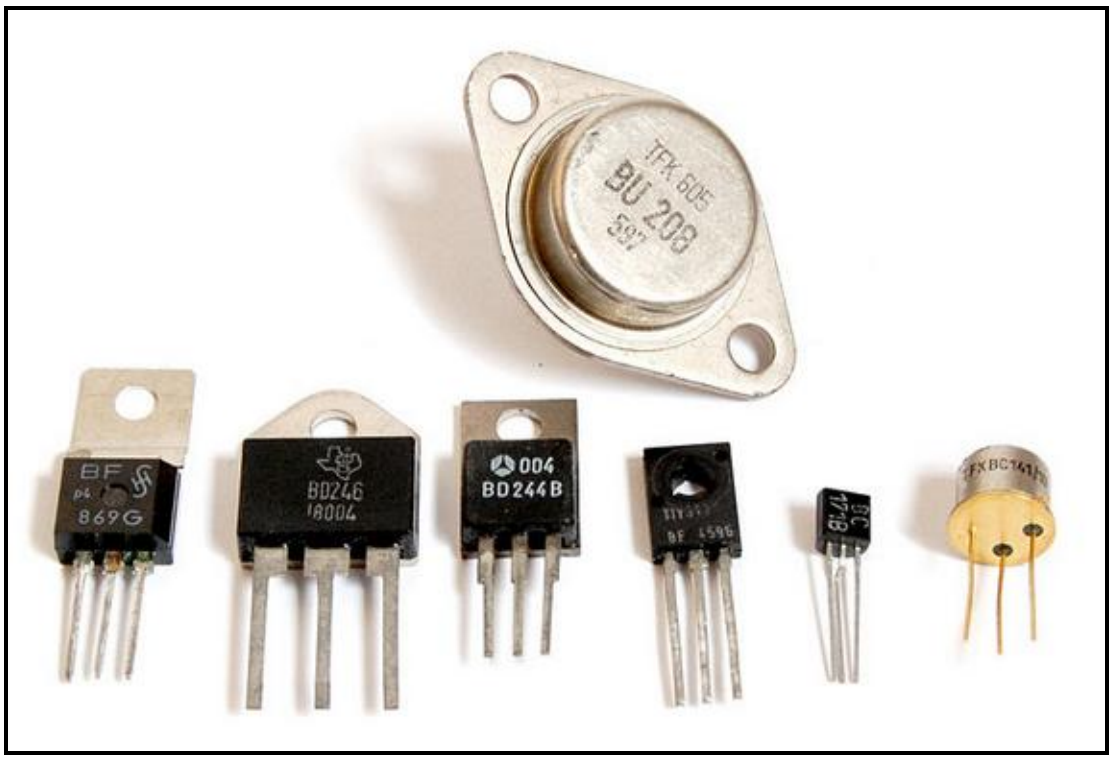


Figure 1.3: Assortment of Transistors

http://www.mikroe.com/old/books/keu/04.htm, Retrieved August 20, 2010

One of the important concepts of judging the characteristic of a transistor is the IV curve. The IV curve displays various information regarding to the transistor. IV curve is essentially the graph of drain current (I_D) against the drain-to-source voltage (V_{DS}) for the FETs or graph of collector current (I_C) against the collector-to-emitter voltage (V_{CE}) for the BJTs. In the case of MOSFET, a type of FET, IV curve displays information such as the ohmic region, saturation region, transconductance, channel length modulation and etc (*nMOSFET (enhancement) Characteristic Curves*, 2008). This vital information exhibits the characteristics and is helpful in recognising the limitations on how far the transistor could go. Understanding the maximum limits enables one to control it properly and thus, further applications can be designed to be robust in such that it could survive in a harsher environment.

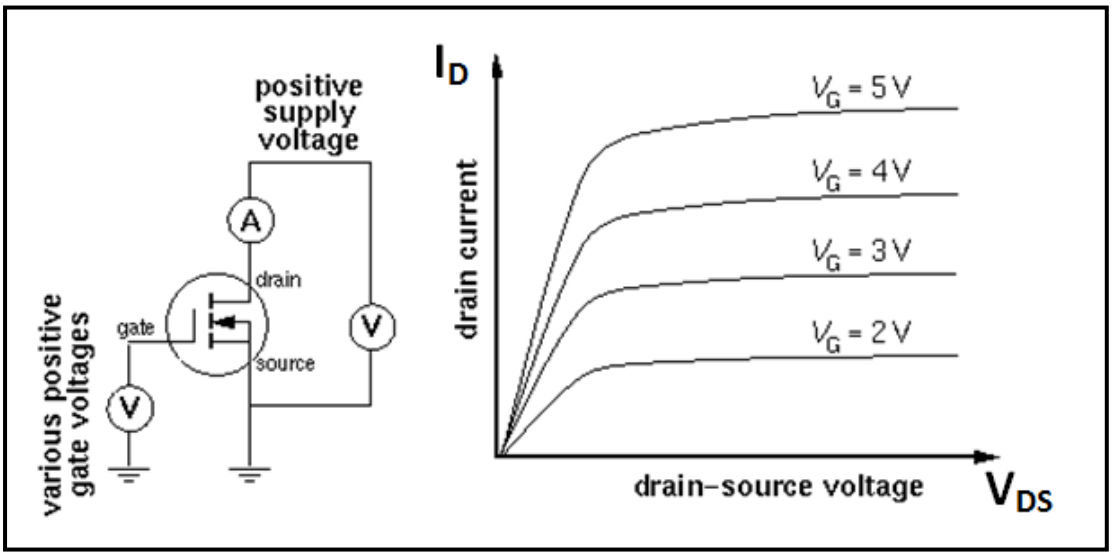


Figure 1.4: IV curve of the FETs (n-channel MOSFET)

http://www.physics.csbsju.edu/trace/nMOSFET.CC.html, Retrieved August 20, 2010

Figure 1.4 depicts the IV curve of a n-channel MOSFET. With various gate voltages (V_G), one could see how does the drain current (I_D) corresponds to the increment of drain-source voltage (V_{DS}).

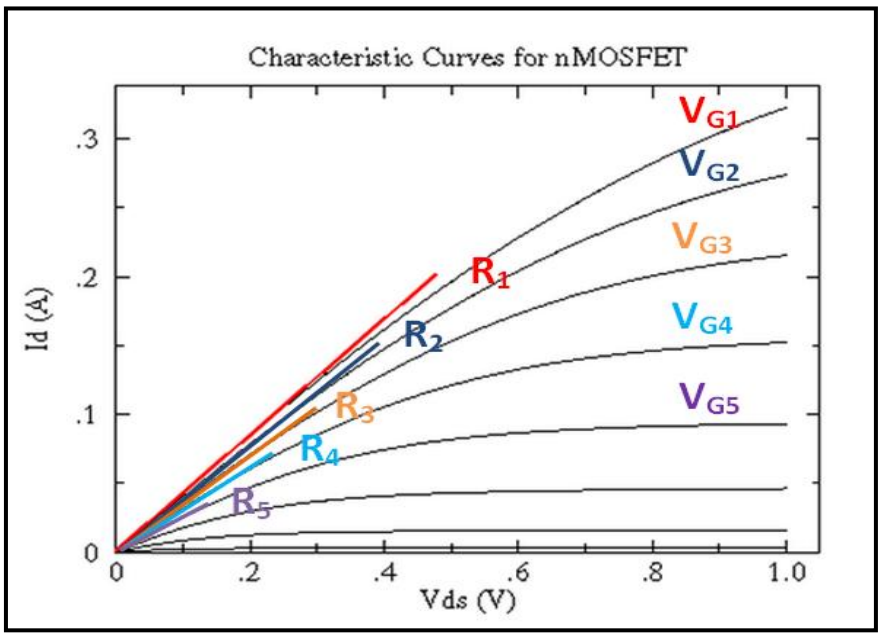


Figure 1.5: Ohmic Region of nMOSFET

http://www.physics.csbsju.edu/trace/nMOSFET.CC.html, Retrieved August 20, 2010

Putting the saturation region aside, the ohmic region shows the ohmic characteristic of the transistor for various gate voltages (V_G). Figure 1.5 shows the resistance feature of the MOSFET before entering saturation point. As it is shown, V_{G1} has a R_1 relation between I_D and V_{DS} while V_{G2} has R_2 so on and so forth. This entails different gate voltage provides a different resistance effect upon the MOSFET. It can be seen that the IV curve depicts such vital information.

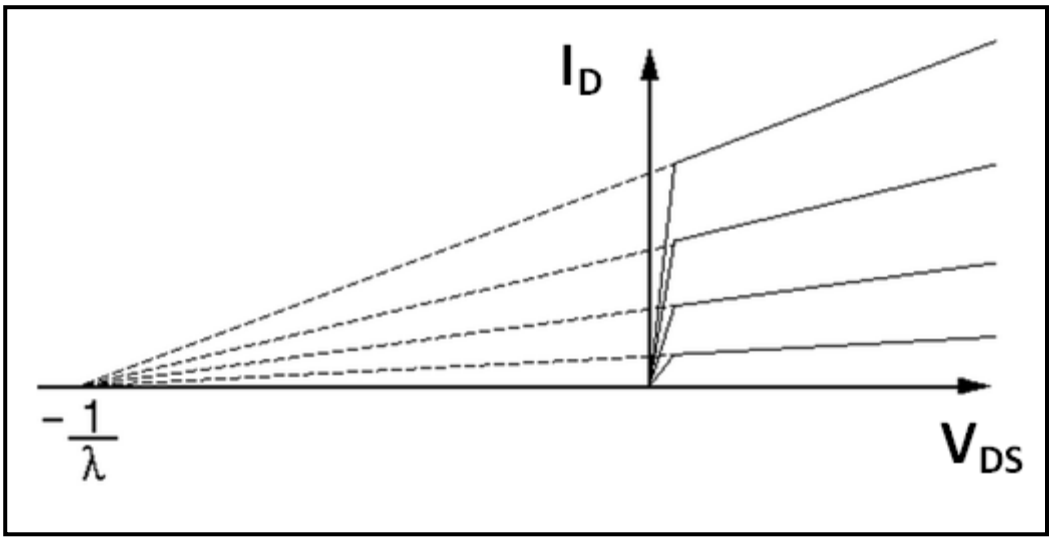


Figure 1.6: Saturation Region- Channel Length Modulation of nMOSFET

http://www.physics.csbsju.edu/trace/nMOSFET.CC.html, Retrieved August 20, 2010

Another important aspect of the IV curve is the saturation region. Apart from informing the maximum limit, it reveals the channel length modulation, λ. All of the V_G, when extended as the dotted line shown in Figure 1.6, will eventually meet to a common point. This common point yields the value of the channel length modulation. Channel Length Modulation (CLM) is a shortening of the length of the inverted channel region with the increase in drain bias for large drain biases. The result of CLM is an increase in current with drain bias and a reduction of output resistance.

1.2 Aims and Objectives

The overall aim of the project:

- To obtain the IV curve of the transistor.

Specific Aims:

- To plot the IV curve on static screen.
- To get the reading of the IV curve of every particular point.

Objectives:

- To build a device to plot the IV curve of the FET on an oscilloscope.
- To build a device to plot the IV curve of BJT on an oscilloscope.
- To build a universal device to plot the IV curve of various transistors on an oscilloscope.

The aim of this project is to obtain the IV curve of the transistor on a screen. This helps in identifying faulty transistor, specifically FETs, and to know the characteristic of the transistor.

The objective goes by building a low-cost terminal device which plots the IV curve of a FET. This medium, called the FET curve tracer, is an electronic device which feeds a transistor as input and then outputs the IV curve on a conventional oscilloscope. BJT corresponds to a great similarity with FET. The next objective is to build a universal transistor curve tracer which is applicable for both FETs and BJTs.

CHAPTER 2

LITERATURE REVIEW

2.1 Transistor Curve Tracer

The study of simple transistor curve tracer is rather vital in this project. T. Wimor (1989) had researched in finding such device to provide the ease of faulty detection of the transistor.

With so many transistors used in today's equipment, a good tester for these devices is a must in every electronics workshop. And yet, most of us use a multimeter to check transistor. Although such a test is usually adequate for a quick ok or faulty test, it fails to provide information on the characteristic of the device under test. The curve tracer presented here works in conjunction with an oscilloscope, and is capable of performing a stepped current amplification test on pnp as well as on npn transistors. The instrument so allows unknown or unmarked types to be matched to known ones, which is a frequent requirement in fault-finding and repair work.

2.2 Transistor and FET Curve Tracer

Research on Daniel Metzger's (2002) journal revealed much of extra feature exists as compared to a typical transistor curve tracer. Nothing provides more information about a transistor than its family of collector characteristic curves. Typical characteristic curves are often given in manufacturers' data sheet, but these are of limited value because transistor characteristic may vary by as much as a factor of three or four either way from unit to unit. Temperature variations also cause considerable change in transistor characteristics, especially with germanium types.

The adapter to be described will allow you to obtain an immediate display of the characteristic curves of any transistor or FET on a conventional oscilloscope. The following are some of the uses to which the curve tracer can be put:

- Determine the a.c. and d.c. beta, collector-to-emitter saturation voltage, collector breakdown voltage (up to 35 volts), and dynamic collector output resistance of a transistor.
- Observe the effects of temperature on transistor characteristics, either by applying heat externally or overbiasing the transistor and allowing it to generate its own heat.
- Observe the base-emitter input characteristics of a transistor.
- Selectively match transistor on input or output characteristics.
- Spot transistor with low breakdown or high saturation voltage as well as those with low beta or high leakage.

2.3 A CAI System for Electronic Circuit Design

Ono et al. (1991) have conducted an experiment in using monitor instead of oscilloscope in the transistor curve tracer. The research describes CAI system which supports electronic circuit design using measure active device data from a curve tracer.

2.4 Low-Cost Curve Tracer uses PC-Based Scope

Peter D. Hiscocks and James Gaston (2007) research on a very versatile curve tracer. There are times when it is extremely useful to know the voltage-current characteristic of some semiconductor device. The journal from Peter D. Hiscocks and James Gaston find a versatile device which can include the curve of not only transistor, but diode, LED, schottky diode, zener diode and incandescent lamp. Truthfully, it depicts a very helpful device in a very convenient way and all things are based on PC-scope.

CHAPTER 3

METHODOLOGY

An IV curve of a transistor is to be plotted on a conventional oscilloscope. It is therefore worthwhile to study the operational principle of an oscilloscope. It gives the opportunity to take measurements in tackling the necessity ingredients that are to be fed into the transistor.

3.1 Oscilloscope

Oscilloscope is an instrument that observes a constantly varying signal voltage over time (*Oscilloscope*, 2009). This delicate contraption plays the major role in developing the project as it was the big screen that displays the desirable curves. Figure 3.1 shows the basic internal structure of an oscilloscope.

An electron gun shoots a beam out and it displayed on a phosphor-coated screen as small green dot. The waveform showed on screen is governed by 4 deflecting coils: 2 horizontal deflecting coils and 2 vertical deflecting coils. The intensity of voltages that are applied to the terminal determines how far the beam would get deflected.

Typical application of measuring waveform is by using the time division on the X-axis. A conventional oscilloscope has a built-in sawtooth generator. This voltage is fed to the horizontal deflecting coils while the waveform that was intended to be measured is fed to the vertical deflecting coils. Thus, the waveform can be shown on screen.

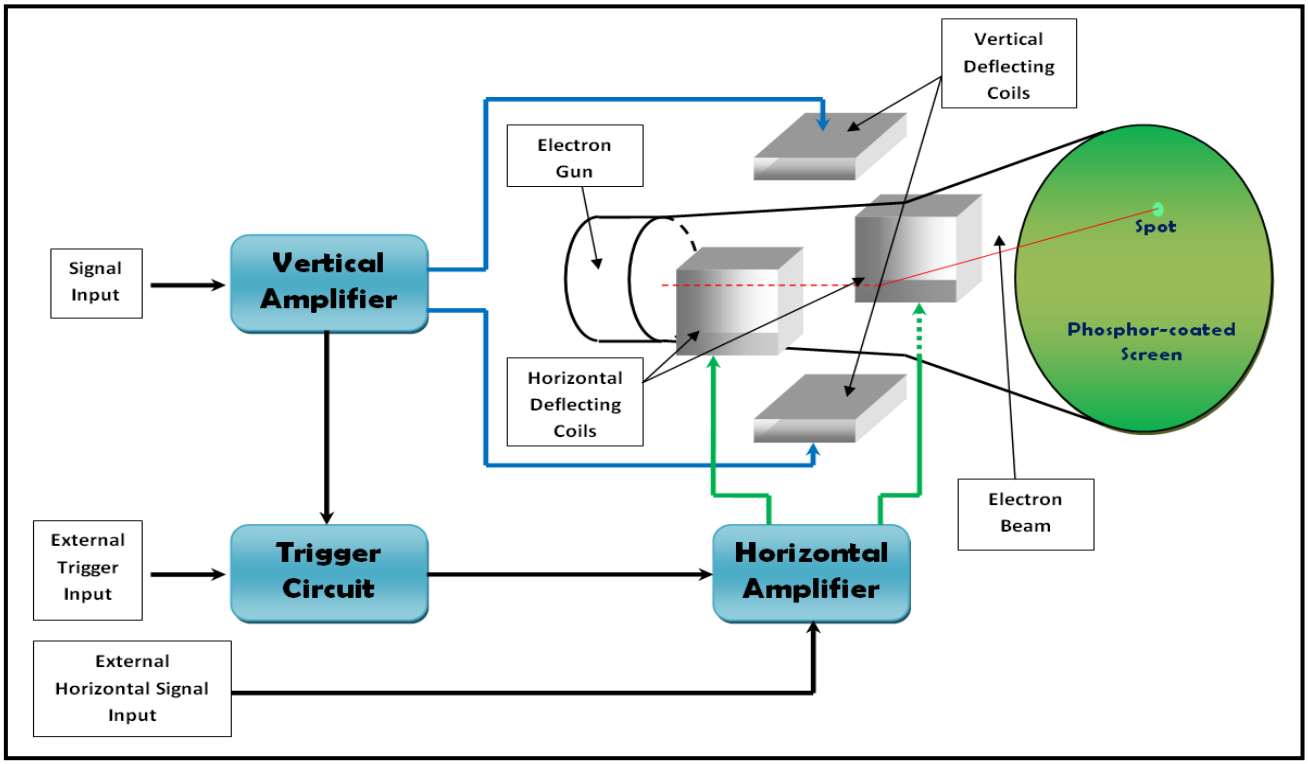


Figure 3.1: Internal Structure of an Oscilloscope

http://www.piclist.com/images/www/hobby_elec/e_oscillo0.htm, Retrieved November 11, 2010

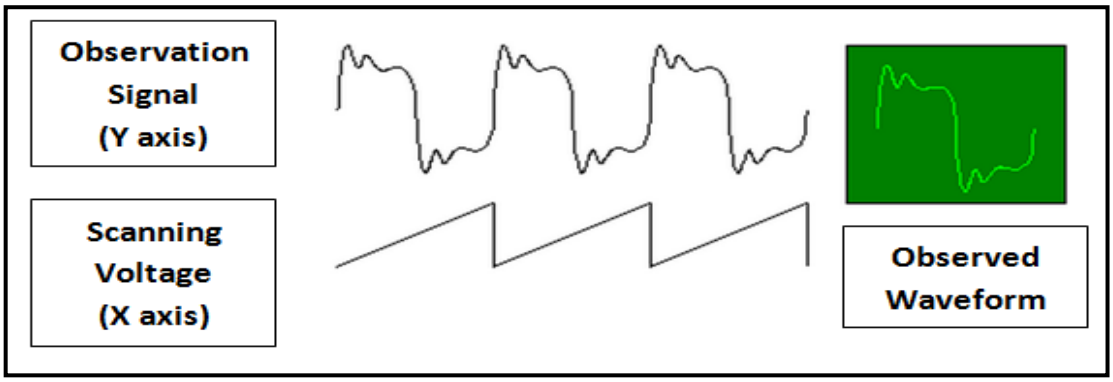


Figure 3.2: Typical Application on Measuring Waveform

http://www.piclist.com/images/www/hobby_elec/e_oscillo0.htm, Retrieved November 11, 2010

As shown in Figure 3.2, as the voltage in X-axis increases across time, the beam got deflected in the horizontal orientation from left to right. In the mean time, the inputted voltage at the Y-axis results in deflection of beam in the vertical orientation. When both of them are combined, the result can be observed as shown in the Observed Waveform.

3.2 Proposition

As mentioned earlier, a typical application on displaying a waveform is to supply the built-in sawtooth wave at the horizontal deflecting coils. The problem of this on the main topic is that the observed waveform is not a single static display but a series repetition of continuous running waveform. This is not desired. Solution to this is by supplying a triangular waveform instead. The negative slope of the triangular wave deflects the beam back to the origin point. Thus, whatever that is shown in screen will be static, not rapidly moving waveform. This triangular waveform shall be applied to the "Drain" terminal of a FET to see the resultant waveform from the "Source" terminal.

As the "Drain" terminal of n-channel FET can receive only positive supply while p-channel FET for negative, positive and negative triangular waveform shall be sorted out.

Apart from that, it is desirable to plot several curves with a series of different V_G. The solution to that is to supply staircase voltages to the "Gate" terminal. The overall idea is illustrated in Figure 3.3 below.

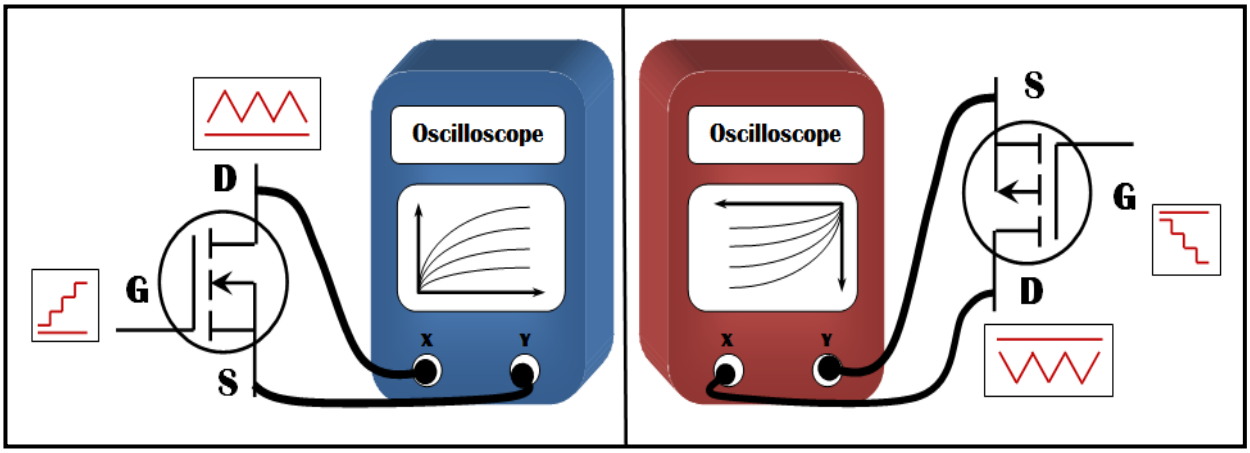


Figure 3.3: Idea of Operation

3.3 Block Diagram

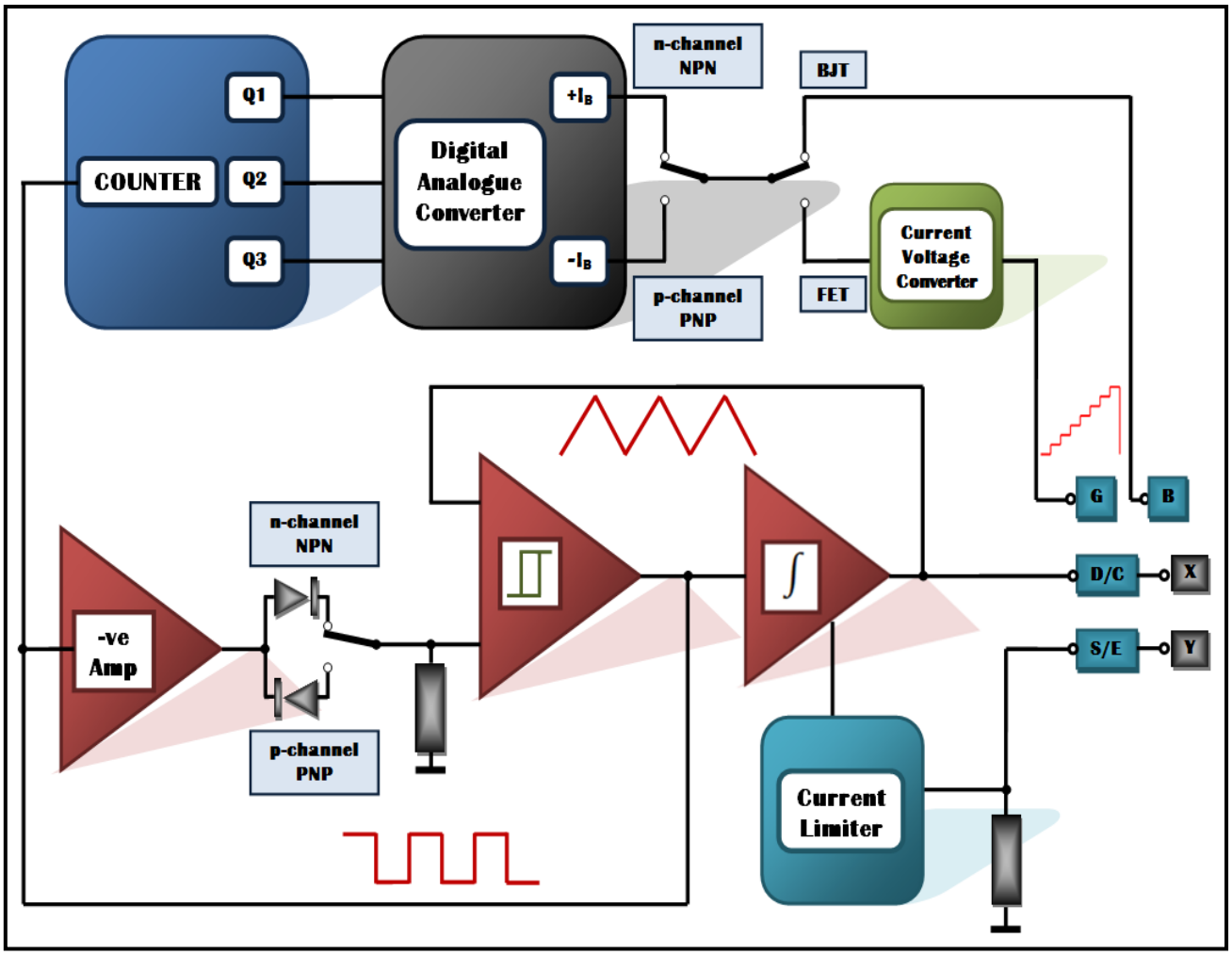


Figure 3.4: Block Diagram

This design comprises 7 main components in the play as depicted in Figure 3.4. They are counter, digital to analogue converter (DAC), current to voltage converter, amplifier, comparator, integrator as well as current limiter. This block diagram shows a thorough layout on the creation of certain waveforms that are required to feed into the device.

A simple overview is that, the counter takes in square wave to produce 3 different frequencies square waves at the output. They are then combined and

converted from digital to analogue through DAC to create a staircase current. Next, it undergoes conversion from current to voltage, and this is fed to “Gate” terminal of the FET.

Square wave is produced by the comparator. The comparator feeds in the feedback-inverted square wave and the converted triangular wave from the integrator. The comparison on both waves yield a square wave. This wave is then fed to integrator to perform integration. The integration of square wave is triangular wave and therefore the output. The negative amplifier plays 2 roles in particular:

- To tune back the phase-shifted wave.
- To control the frequency of the wave.

Thus, the output from the negative amplifier is fed back to comparator for further operation. It is noted that the 3 components: amplifier, comparator, and integrator go hand-in-hand. They are interdependent to each other and cannot be disintegrated. The output of the integrator connects to a power driver, which is not shown in Figure 3.4, and is fed to the “Drain” terminal of the FET as well as the X-axis of the oscilloscope. Power driver does nothing but to drive the sufficient power for the FET. It will otherwise not able to display the curve due to power deficiency.

Last but not least is the protection circuit: current limiter. As the name implies, it limits the current of the device. When a large amount of current flows in the circuit, current limiter shorts the whole circuit and thus save the whole contraption. The output is connected to the “Source” terminal of the FET. It also connects to the Y-axis of the oscilloscope. This is because the current from the “Source” terminal holds all of the information regarding to the characteristic of the transistor. The resistor located beside the current limiter as shown in Figure 3.4 plays the role of converting current from the “Source” terminal to voltage. Oscilloscope is capable of reading only voltage signal. Therefore, a conversion is required. The value of the resistor happens to be 1 Ω. So, when V = IR, the voltage and current value appear to be the same.

3.4 Schematic Diagram

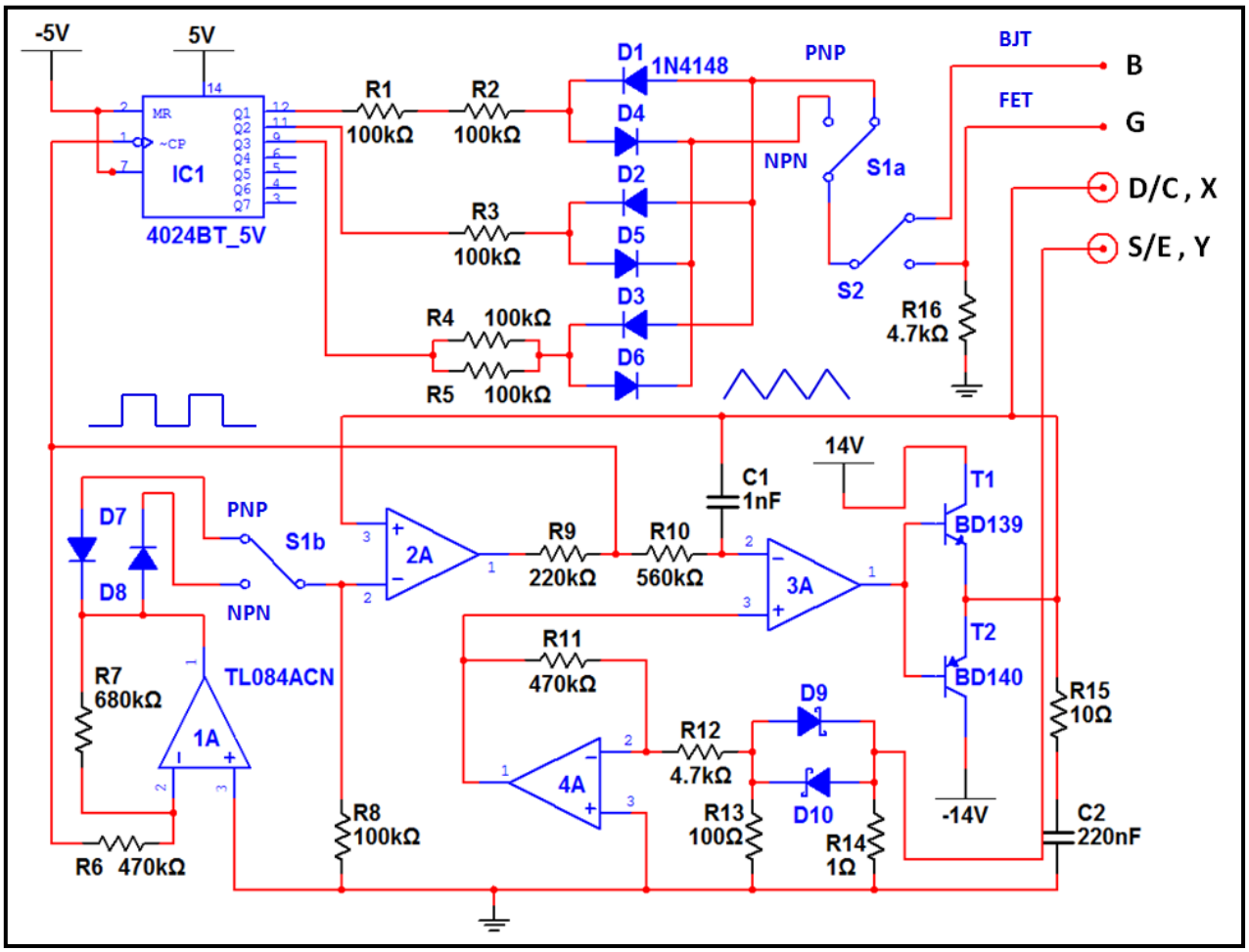


Figure 3.5: Schematic Diagram

Figure 3.5 shows the schematic diagram of the transistor curves tracer circuit. It works for both BJT and FET as test devices. While switch S1 controls it to be n-type or p-type, switch S2 controls it to be in either BJT mode or FET mode. The complication of this design is that it requires 2 different voltage supplies: ± 5V and ± 14V. An external power supply is therefore built to appease the requirement.

IC1 on Figure 3.5 is a ripple counter, modelled 4024.

Op-amps 1A, 2A, 3A and 4A come in an integrated chip named IC2, goes with the model TL084. They are high speed J-FET input quad op-amps with high input impedance J-FET stage. The high slew rate (16 V/μs) with internal frequency compensation and as well as output short circuit protection are the main reasons for this device to be chosen. In this project, speed is all that matters. Fast reaction demands for high slew rate. Whilst internal parasitic capacitance may affect the frequency of the wave, the internal frequency compensation contras this problem. Short circuit protection is essential for safety purposes.

Apart from that, D1-D8 are typical 1N4148 diodes. The switching speed can go as fast as 4 ns with maximum forward current of 450 mA. Again, speed is all that matters. Therefore, 1N4148s are selected.

Next, BD139 and BD140 are NPN and PNP transistors respectively that are designed for drivers, utilising only complementary circuits.

Last but not least, D9 and D10 are the BAT85 Schottky diodes. They have a low forward voltage, as low as 0.4V, which is ideal for the current limiter.

3.4.1 Counter and Digital-Analogue Converter

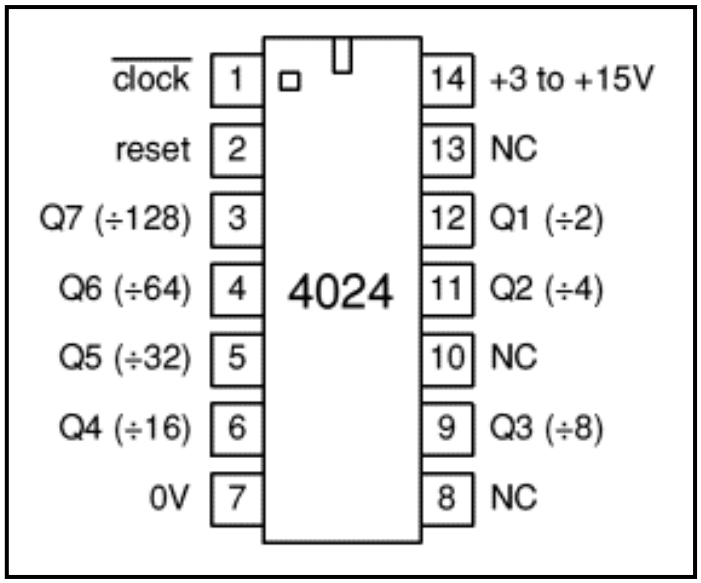


Figure 3.6: 4024 7 bits (÷128) Ripple Counter

http://www.kpsec.freeuk.com/components/cmos.htm, Retrieved November 11, 2010

Figure 3.6 depicts a 4024 7 bits ripple counter. A ripple counter essentially comprises a series of JK Flip-Flops. The main function is to alter the frequency of the input clock (*Counters asynchronous (ripple) Counters*, 2010).

Ripple counter has a JK Flip-Flop with its inverted output connected to a second JK Flip-Flop's input clock terminal. Both J and K inputs are set HIGH, and thus presenting a toggling state. When a clock is input to the first JK Flip-Flop, the output yields a "÷ 2" clock frequency. However, this ripple counter goes beyond by "÷ 2". Pins 12, 11, 9, 6, 5, 4 and 3 in Figure 3.6 depict a variety of division. For instance, if the input clock frequency is set to be 1000 Hz, the output at pin 12 (Q1) will be 500 Hz, pin 11 (Q2) will be 250 Hz, pin 9 (Q3) will be 125 Hz, so on and so forth (*4000 series CMOS Logic ICs*, 2010).

This concept is very advantageous in producing the staircase gate voltages or base currents with a simple aid from the DAC.

3.4.1.1 Working Principle of Counter and Digital-Analogue Converter

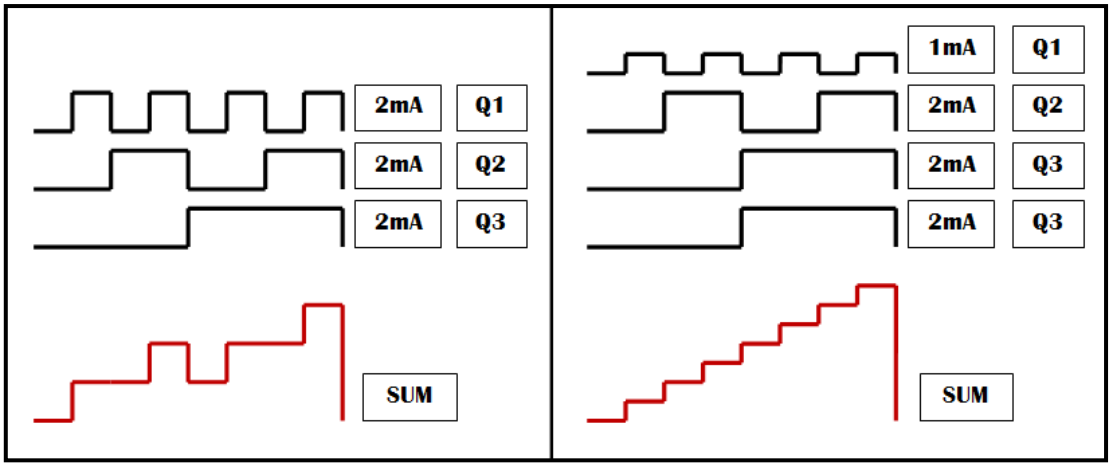


Figure 3.7: SUM of outputs Q1, Q2 and Q3

Building a staircase of voltages is not as simple as directly adds them up together. Adding them up together without any amendment would yield a result as shown on the left of Figure 3.7. Output of Q1, Q2 and Q3, say 2 mA, when add them up will in fact results in a lumps and holes graph which is not desirable.

The solution to this is having output of Q1 changed to "half" the amplitude of current as compared to the Q2 while two Q3s are shared at the same output, the sum would produce a staircase graph as shown on the right of Figure 3.7 (*Thomas L. Floyd*, 2008). It reveals a nice and undistorted staircase current level that can be used for BJT or undergoes current to voltage conversion for FET transistors.

Resistors R1- R5 essentially are the DAC as depicted in Figure 3.5. It plays 2 roles in particular: to change digital to analogue signal; and in the mean time to add the resultant current up in producing the desired graph. Two 100 kΩ resistors, R1 and R2, connected in series makes a 200 kΩ resistor. The 5 V outputted at Q1 leads to a flow of 25 μA current at Q1 terminal in accordance with ohms law. 50 μA current flows at Q2 terminal for having only one 100 kΩ resistor. The branching out of two parallel 100 kΩ resistors, R4 and R5, results in a flow of 100 μA current at Q3 output.

Diodes D1-D6 sorts the “positive” and “negative” currents out. They go for the implementation of n-type and p-type respectively. This was illustrated in Figure 3.3. It is therefore a necessity to supply -5 V to pin 7 of the 4024 ripple counter. It will otherwise not having negative current and p-type Device Under Test (DUT) cannot be used.

Table 3.1: Digital Current and Voltage Control

Counter State	**BJT**		**FET**	
	pnp	**npn**	**p-channel**	**n-channel**
000	-175	0	-0.8225	0
001	-150	25	-0.7050	0.1175
010	-125	50	-0.5875	0.2350
011	-100	75	-0.4700	0.3525
100	-75	100	-0.3525	0.4700
101	-50	125	-0.2350	0.5875
110	-25	150	-0.1175	0.7050
111	0	175	0	0.8225
	base current (μA)		**gate voltage (V)**	

Table 3.1 indicates the value of staircase current. It varies from 0 to 175 μA with a step current of 25 μA. Likewise, the voltage varies from 0 to 0.8225 V with a step voltage of 0.1175 V. It is noted that a 4.7 kΩ resistor is used for the conversion of current to voltage. In accordance to ohms law, V = IR, the step voltage is thus as mentioned above.

3.4.1.2 Simulation for Counter and Digital-Analogue Converter

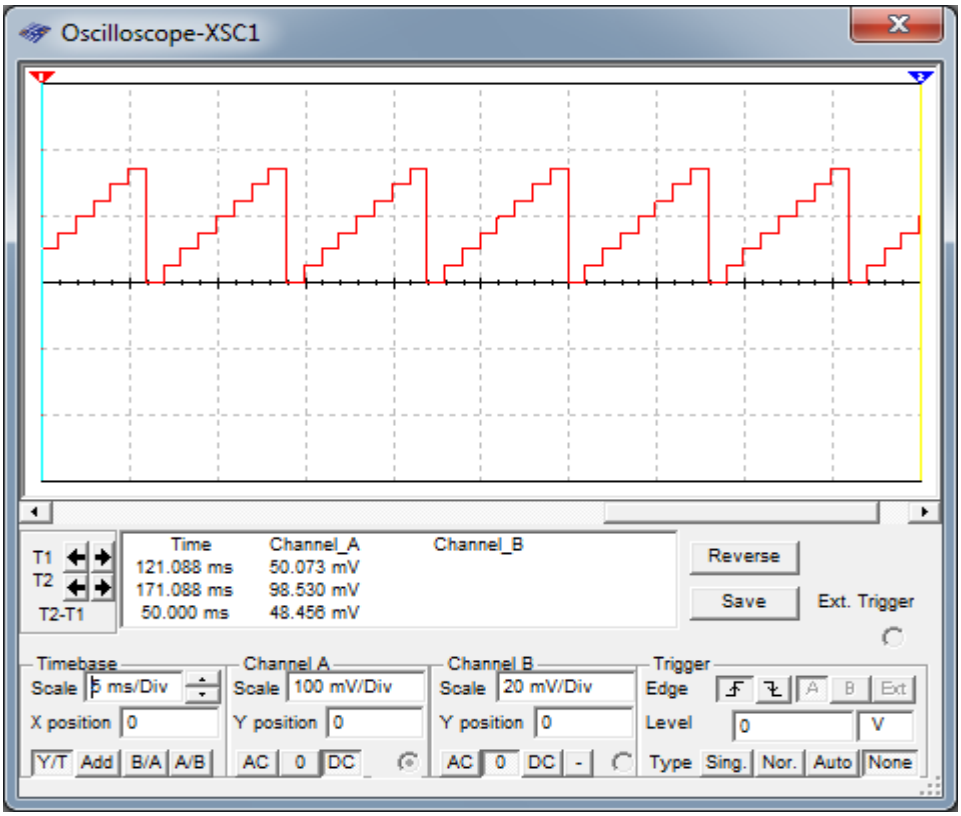


Figure 3.8: Perfect Staircase Current or Voltage

Simulation from Multisim, Retrieved November 12, 2010

Figure 3.8 shows the desired wave. The output from DAC is a current signal for the base of BJT. A 1kΩ resistor is used to convert current to voltage. Thus it has a step of 25 mA.

If the output of Q1, Q2 and Q3 in Figure 3.5 is connected as shown in Figure 3.9, the output can be seen in Figure 3.10. Again, ripple counter essentially comprises JK Flip-Flop connected as shown in Figure 3.9. Output of U1 shows a "÷ 2" frequency while U2 is "÷ 4" and U3 is "÷ 8".

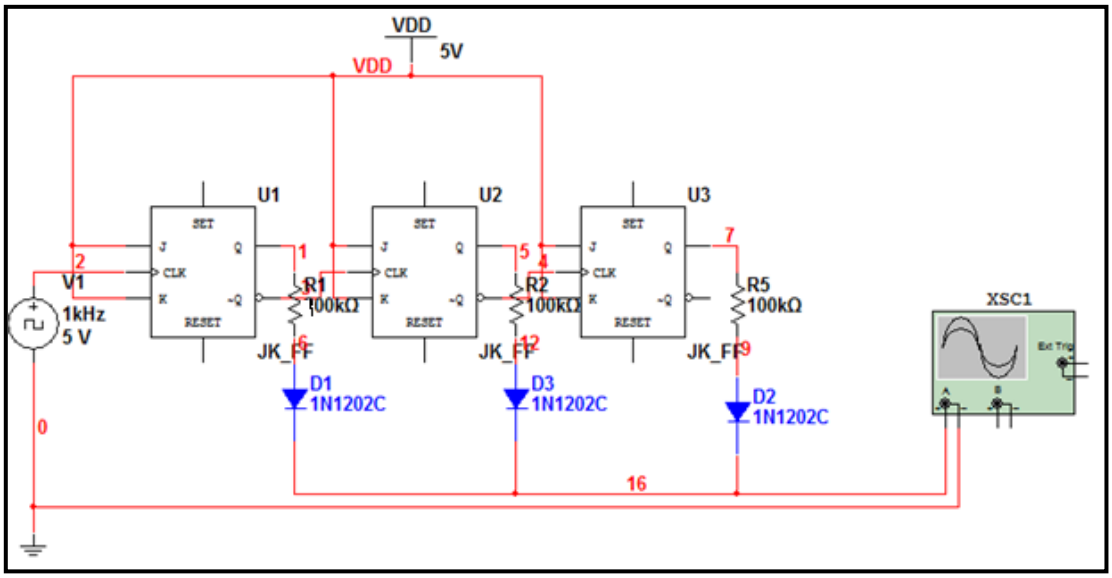


Figure 3.9: Faulty Circuit for Counter and Digital-Analogue Converter

Multisim, Retrieved November 12, 2010

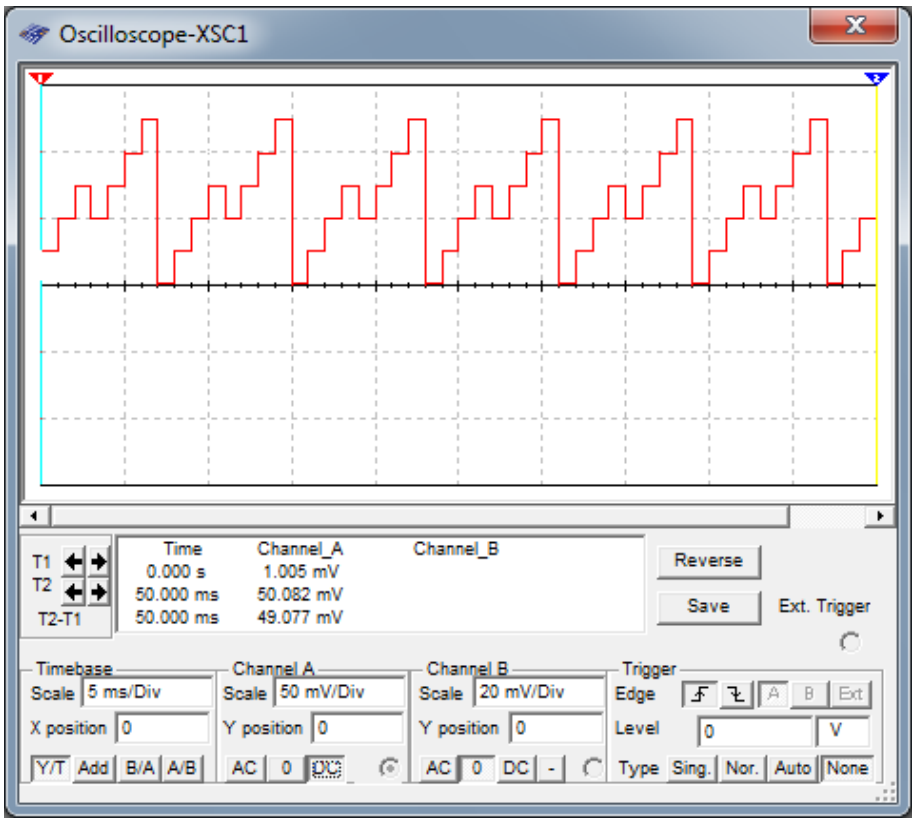


Figure 3.10: Imperfect Staircase Current or Voltage

Simulation from Multisim, Retrieved November 12, 2010

3.4.2 Current to Voltage Converter

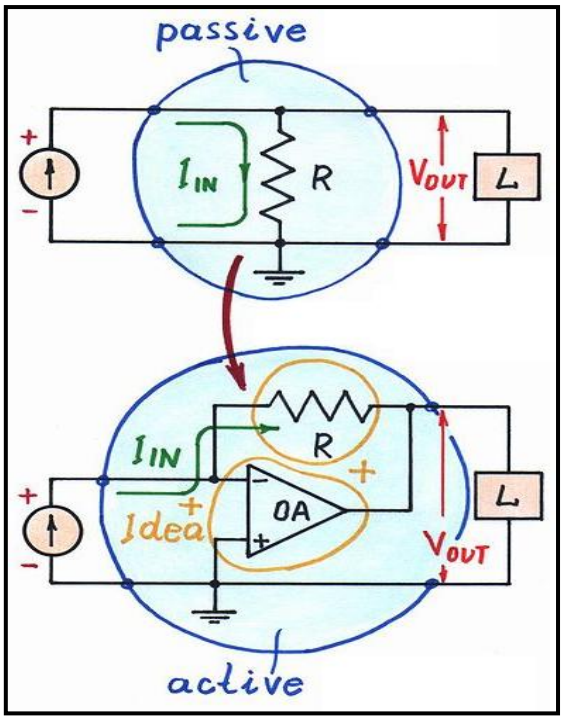


Figure 3.11: Current to Voltage Converter Passive (Top) and Active (Bottom)

http://en.wikibooks.org/wiki/Circuit_Idea/Op-amp_Inverting_Current-to-Voltage_Converter, Retrieved December 10, 2010

Figure 3.11 shows the Passive (Top) and Active (Bottom) Current to voltage converter. Current to voltage converter can be as simple as using a single resistor, or it could be as complicated as using an op-amp.

Ohm's law said if a current I flows through the resistor R, a voltage drop V = IR will appear across the resistor R that is proportional to the magnitude of the current (*Current-to-Voltage Converter*, 2001). Therefore, one can harvest the voltage signal through the resistor. It is, however, very detrimental for certain application by using the passive method. The problem is due to the loading effect of the current supply to the resistor. The internal resistance of the current supply might consume some of the voltage, and thus reduces the output load voltage.

Active current to voltage converter, on the other hand, behaves better than the passive. It acts as a buffer. The loading effect is eliminated because of the inheritance of high input impedance and low output impedance. However, it is not necessary for this project to use the active one as it does not affect much and is to consider as negligible.

3.4.3 Oscillator and Integrator

The oscillator, virtually, consists of a comparator and an inverting amplifier. Oscillator and integrator are not independent circuit which cannot be dismantled. This system is responsible for producing square wave, known to be the clock, to feed into the counter. It also produces triangular wave for the collector of the BJT and FET.

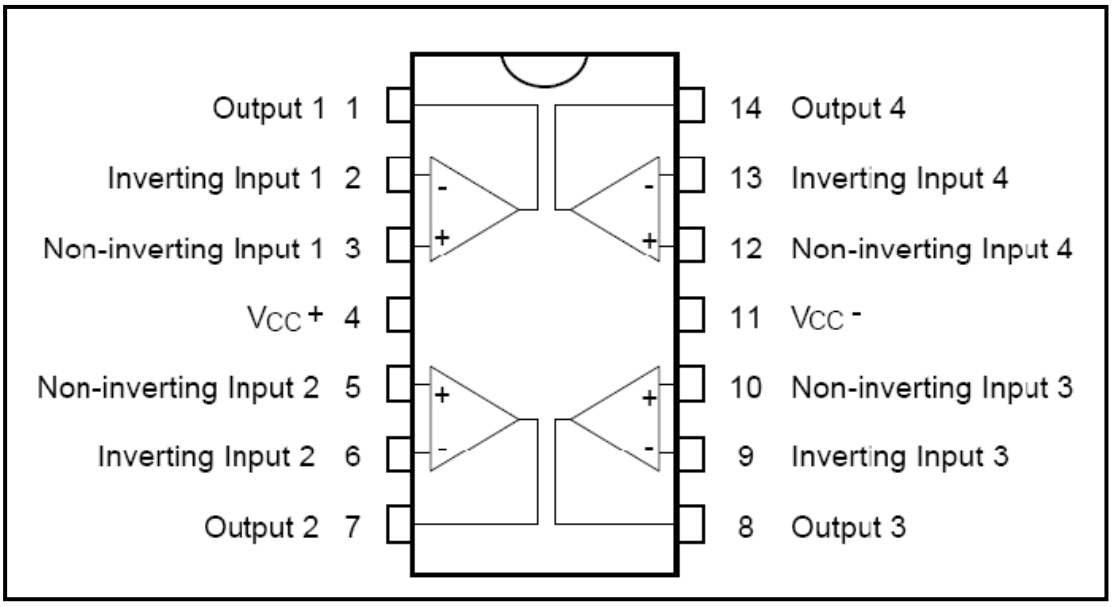


Figure 3.12: TL084 JFET Op-Amp

http://www.datasheetcatalog.org/datasheet/SGSThomsonMicroelectronics/mXyzvvvu.pdf, Retrieved December 10, 2010

Figure 3.12 shows a TL084 JFET op-amp. It is an IC consisting four JFET op-amps. JFET op-amps play an upper-hand in 2 major roles: it has a high input impedance and most importantly high slew rate than a conventional 741 op-amp

(*TL084*, 1999). For the production of square and triangular wave, 3 op-amps are sufficient. The fourth op-amp is used for current limiter design.

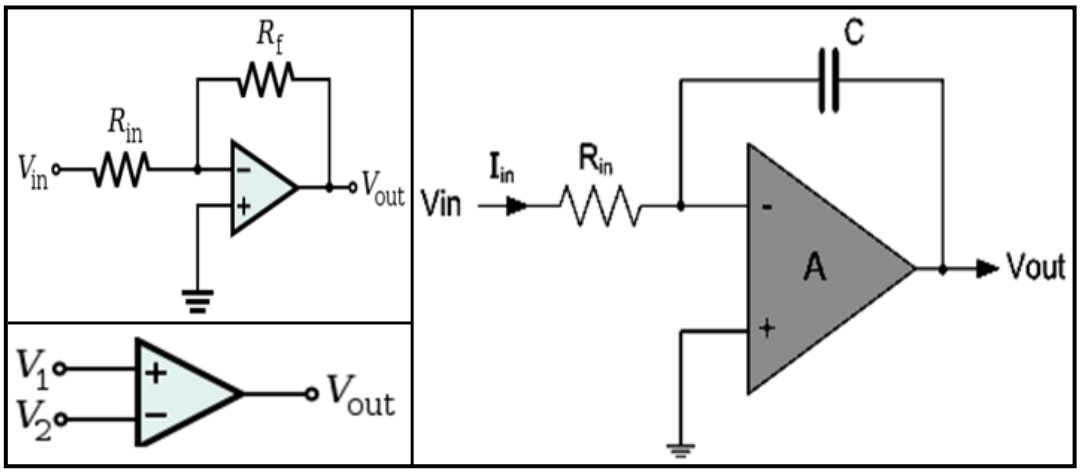


Figure 3.13: (a) Negative Amplifier (Top Left) (b) Comparator (Bottom Left) (c) Integrator (Right)

http://en.wikipedia.org/wiki/Operational_amplifier_applications, Retrieved December 10, 2010

Whenever a square and triangular wave is required, the first and foremost basic foundation is the 3 components as shown in Figure 3.13.

The inverting amplifier shown in Figure 3.13 (a) on the top left corner amplifies signal that is fed to V_{in} terminal. It does amplification and inversion or phase shifting for 180^0. The formula goes by:

$$V_{out} = -\frac{R_f}{R_{in}}(V_{in}) \tag{3.1}$$

Comparator, on the other hand, takes in V_1 and V_2 to compare the voltage level. It is shown in Figure 3.13 (b) on the bottom left. When the non-inverting input (V_1) is at higher voltage than the inverting input (V_2), the high gain of the op-amp causes the output to saturate at the highest positive voltage. Likewise, when the non-inverting input (V_1) drops below the inverting (V_2), the output saturates at the most

negative voltage. Therefore, $+V_{CC}$ and $-V_{CC}$ must be supplied to pin 4 and pin 7 of TL084 if negative current is required.

The integrator in Figure 3.13 (c), in advanced, works as the name implies: integrate. Whatever current flows in R_{in}, it gets integrated across the capacitor C. The output voltage V_{out} is simply the voltage across C. The formula goes with:

$$V_{out} = -\frac{1}{C}\int_0^T \frac{V_{in}}{R_{in}}\,dt \tag{3.2}$$

Eventually, the output peak would be V_{CC}. However, time taken for integration is controlled by the values of C and R_{in}.

3.4.3.1 Working Principle of Oscillator and Integrator

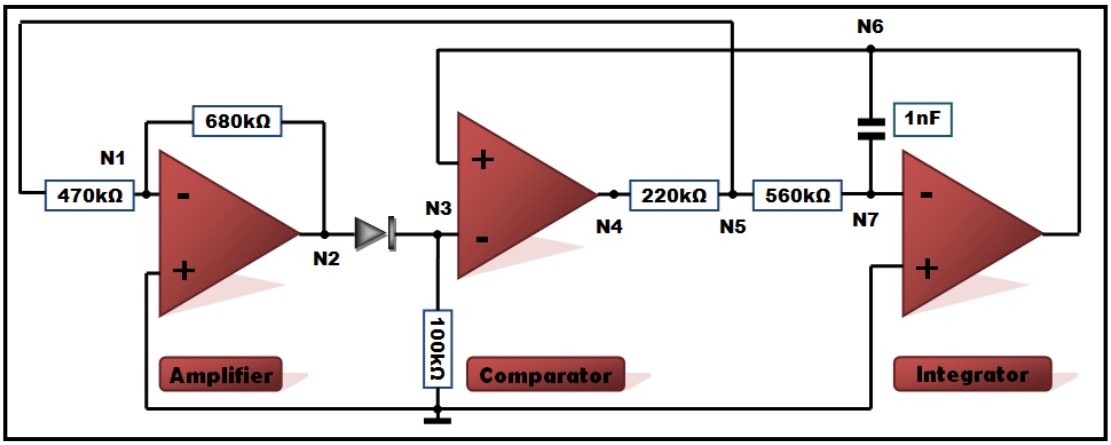


Figure 3.14: Amplifier, Comparator and Integrator

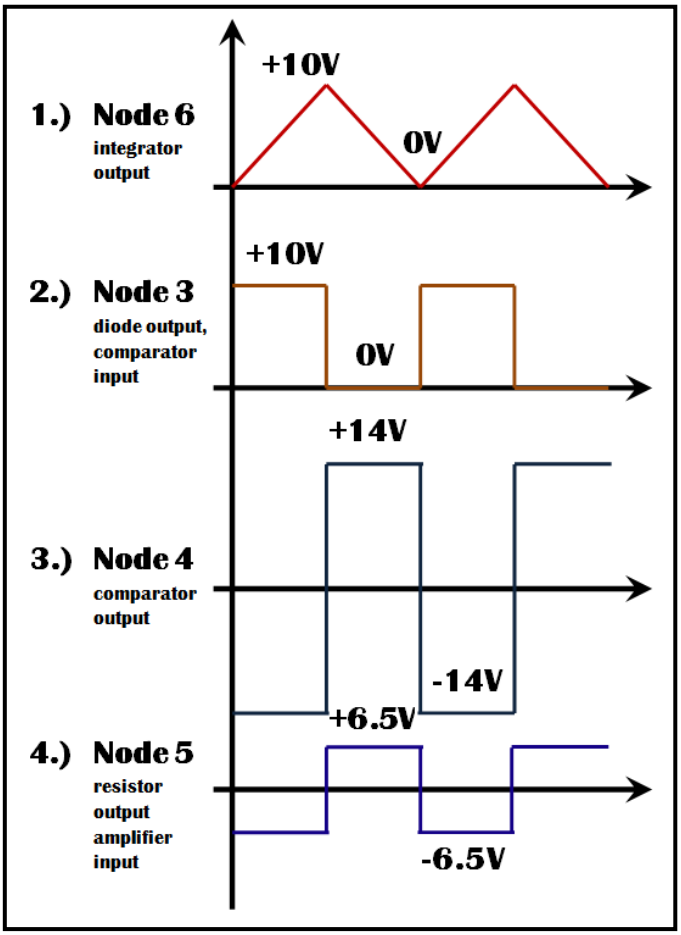


Figure 3.15: Waveform from Several Nodes

Figure 3.14 shows the amplifier, comparator and integrator. It has been dismantled for simplicity purposes. Figure 3.15 shows the waveform of several modes. Ultimately, the goal goes with 2 outputs:

1. To produce square wave (clock)
2. To produce triangular wave

The key role on producing square wave lies in the hand of the comparator. Initial value of every parts are 0 V, it needs some starter to kick the circuit to start. Say, the output of the comparator gives a –14 V. This voltage is translated to current by the 220 kΩ resistor. A drop of approximately 7.5 V is sent to the integrator as shown in Figure 3.15 Node 5. The formula of the integrator goes with:

$$V_{out} = -\frac{1}{C}\int_0^T \frac{V_{in}}{R_{in}}\,dt \tag{3.3}$$

Therefore, –6.5 V results in a positive slope at Node 6 from 0 V to V_{CC}. At the same time, the –6.5 V at Node 5 is sent to the amplifier.

The inverting amplifier has the formula of $V_{out} = -\frac{R_f}{R_{in}}(V_{in})$. Hence, –6.5 V gives an output of approximately 10 V by the 2 resistors, 680 kΩ and 470 kΩ, which have a gain of roughly –1.5. This was illustrated in Figure 3.15 Node 3. The diode plays the role in eliminating negative signal, presuming this handle for n-type transistor.

As the voltage from Node 6 increases, it compares with the maintaining +10 V voltage from Node 3. As soon as the non-inverting input (Node 6) of the comparator exceeds the inverting input (Node 3), the output of the comparator flips from $-V_{CC}$ to $+V_{CC}$ as illustrated in Figure 3.15 Node 4.

This cycle keeps repeating and eventually produces square wave from Node 5 and triangular wave from Node 6.

From the frequency point of view, it seems that the integrator controls the frequency on both square and triangular wave. This is however not true as the amplifier plays an imminent role in affecting the wave frequency. As the formula goes, $V_{out} = -\frac{1}{C}\int_0^T \frac{V_{in}}{R_{in}}\,dt$. One may trace back the formula to find the frequency but the resultant frequency has been restrained from the amplifier. By right, the output from the integrator should achieve +14V as provided by the V_{CC}. However, as soon as the slope voltage exceeded the output from the amplifier, the comparator swaps the output from negative to positive. So, the not-finished-conversion of the positive slope voltage was forced to convert to negative slope voltage. Overall, it affects the wave frequency.

Frequency of the triangular wave plays a critical role. High frequency wave displays the graph without a problem. This is because our eyes cannot perceive the rapid motion of the single beam. Therefore, it creates a phenomenon known as persistence of vision. On the contrary, if a low frequency were used, one may observe a tiny dot of the beam moving up and down from left to right to draw the resultant graph.

It is much desire to have high frequency wave. However, high frequencies may induce a stray capacitance or any parasitic capacitance on the device, which might eventually lead to malfunction. Therefore, it is wise to use the range in between 300 Hz to 1 kHz.

3.4.3.2 Simulation for Oscillator and Integrator

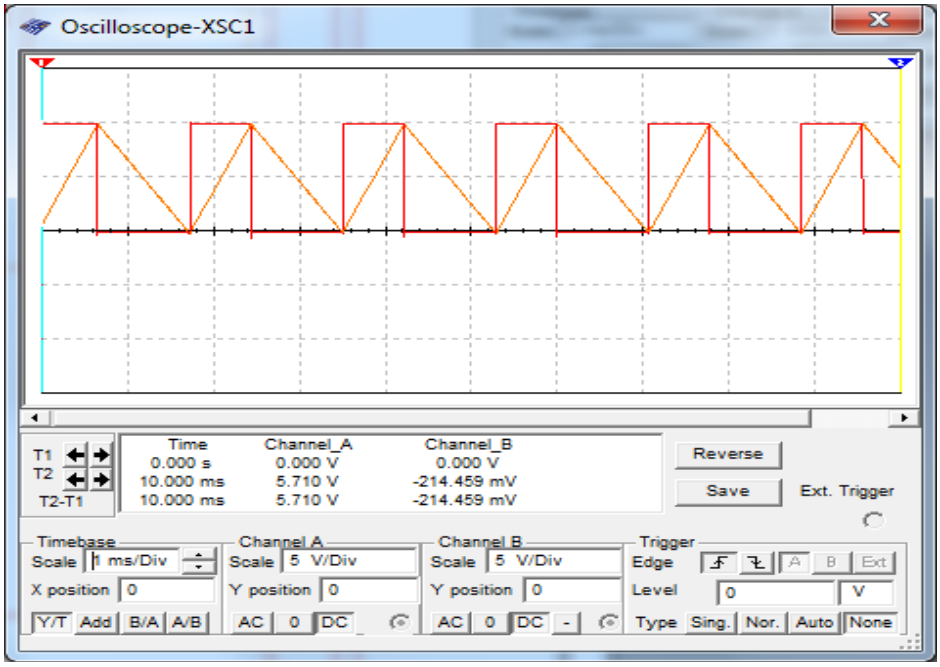


Figure 3.16: Output of Integrator and Amplifier after Diode

Simulation from Multisim, Retrieved August 12, 2010

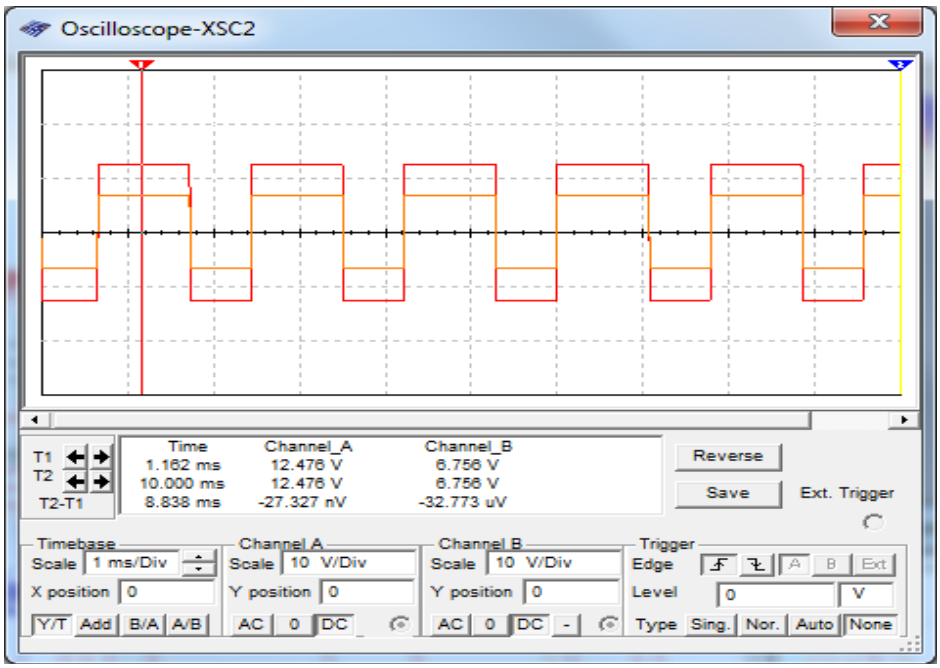


Figure 3.17: Output of Comparator Before and After the Resistor

Simulation from Multisim, Retrieved August 12, 2010

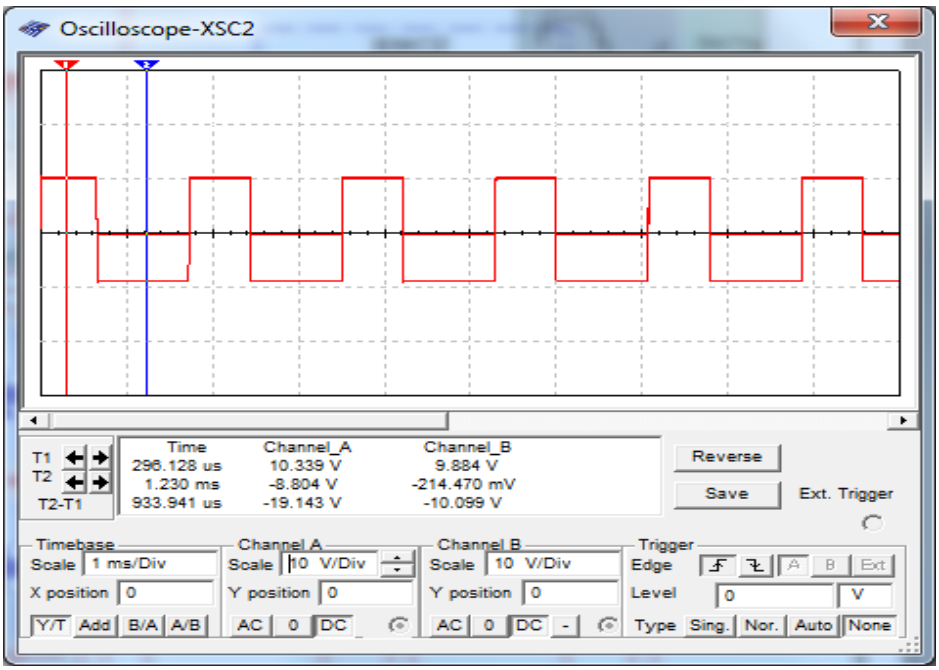


Figure 3.18: Output of Amplifier Before and After Diode

Simulation from Multisim, Retrieved August 12, 2010

Figure 3.16, Figure 3.17 and Figure 3.18 are the simulation result from several nodes. They are explained as in Figure 3.15.

3.4.4 Current Limiter

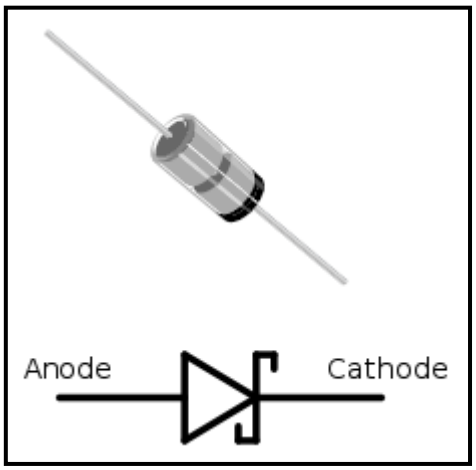


Figure 3.19: Schottky Diode

http://en.wikipedia.org/wiki/Schottky_diode, Retrieved August 12, 2010

Figure 3.19 shows a typical BAT85 Schottky Diode. This is the main component for constructing the current limiter circuit. The low forward voltage, V_F = 0.4 V (*BAT85*, 2000), makes it ideal for this design.

As depicted in Figure 3.5, current limiter utilises the last op-amp of the TL084. Current limiter consists of 2 Schottky diodes which are connected parallel with different direction, 1 Ω, 100 Ω, 4.7 kΩ and 470 kΩ resistors and an op-amp.

The "Source" of the FET or the "Emitter" of the BJT is connected to 1 Ω resistor. Since oscilloscope is capable of reading only voltage signal, a conversion of I_E or I_S to voltage form is required. The 1 Ω resistor does nothing but to convert the current I_E or I_S into a voltage form. So, when V = IR, the current and voltage value appears the same.

Say, when a large current flows through the Device Under Test (DUT), this current is translated into voltage through 1 Ω resistor and is fed to Schottky diode.

Typically, I_E or I_S larger than 400 mA would conduct the diode and cause op-amp 4A to shift the voltage at the non-inverting input of integrator 3A to a level where the integration operation stops. The non-inverting input is normally 0 V. When actuated, the protection circuit cause the oscilloscope to show only a fixed bright spot instead of eight traces. The back-to-back parallel connection of the Schottky diodes make it usable for both n-type and p-type transistor.

3.5 Power Supply

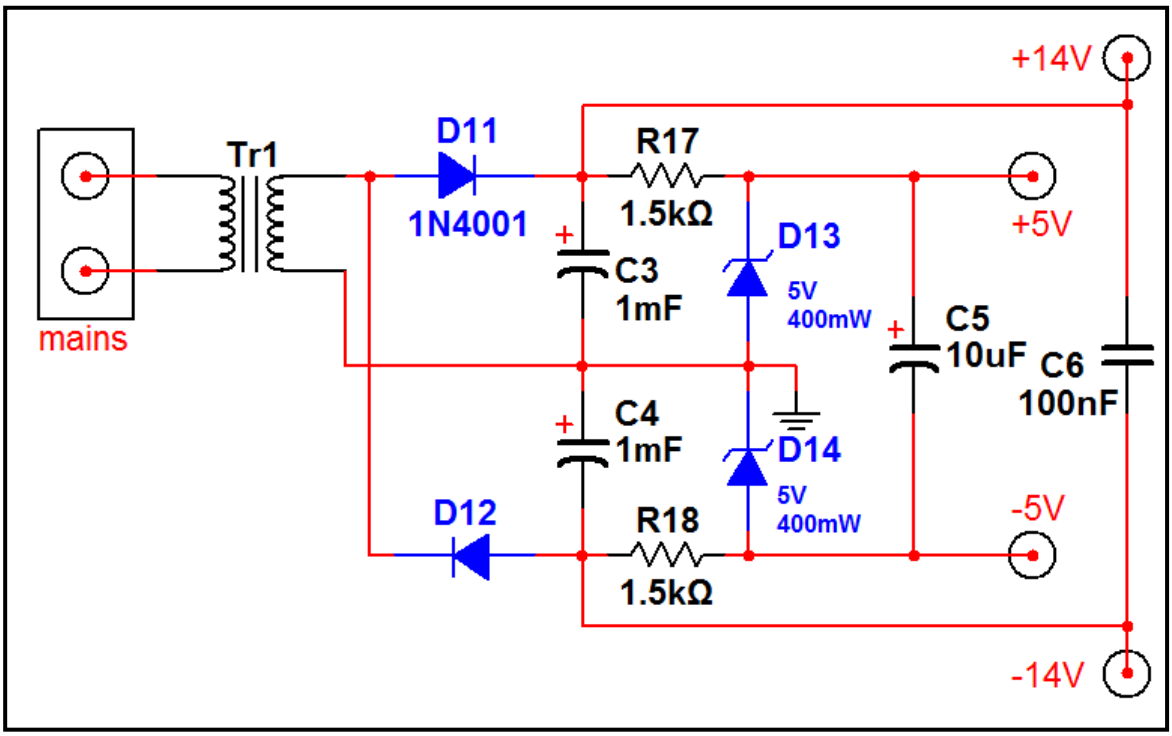


Figure 3.20: Schematic Diagram for Power Supply

Figure 3.20 shows the schematic diagram for the power supply. The goal is ultimately to produce ±5 V and ±14 V for 4024 ripple counter and TL084 op-amp respectively. Battery could have the insufficient current for 2 reasons:

- It has ±14V which a normal battery could not supply
- The current of a battery is too low to drive BD139 and BD 140 power transistors as showed in Figure 3.5.

Therefore, power supply is essential for this project.

The power supply takes in AC 240 V, 60 Hz voltage from the main power socket in Malaysia. It feeds into Tr1, the transformer which steps 240 V down to 14 V. It has a turn ratio of 16 : 1 from primary to secondary. D11 and D12 are typical 1N4001 diodes which behave as rectifier. D11 allows only the positive half cycle of the AC to pass through while D12 is responsible for the negative half. The capacitors (C3 and C4) and resistors (R17 and R18) are basically filters. Filtering AC component, the result is a DC supply. Therefore, the selection of capacitors and resistors values is crucial for the wrong choices may lead to a high ripple effect on the DC supply.

C3 and C4 are selected to be 1000 μF or 1 mF while R17 and R18 are 1.5 kΩ. When positive half cycle of the AC is sent to capacitor C3, it charges up to V_{peak} of the AC. As the negative half cycle comes, C4 got charged up instead. However, this also means the discharging of capacitor C3 through resistor R17 for the negative half. The time constant for discharging state is $\tau = RC$. Thus, the discharging time for capacitor C3 would be $\tau = (1.5\ k\Omega)\ (1000\ \mu F) = 1.5$ s. Since the frequency of AC power supply in Malaysia is 60 Hz, the period T_p is therefore 0.01667 s. The discharging time is much larger than the period of the AC, hence there would be an insignificant ripple effect and the output will appear as DC. ±14 V DC can be harvested at C3 and C4.

D13 and D14 are zener diodes and are chosen at specifically 5 V. This pulls the ±14 V to ±5 V.

Capacitor C5 and C6 are 10μF and 100nF respectively. Their purpose is to enhance the loading effect of ±5 V and ±14 V to 4024 ripple counter and TL084 op-amp respectively.

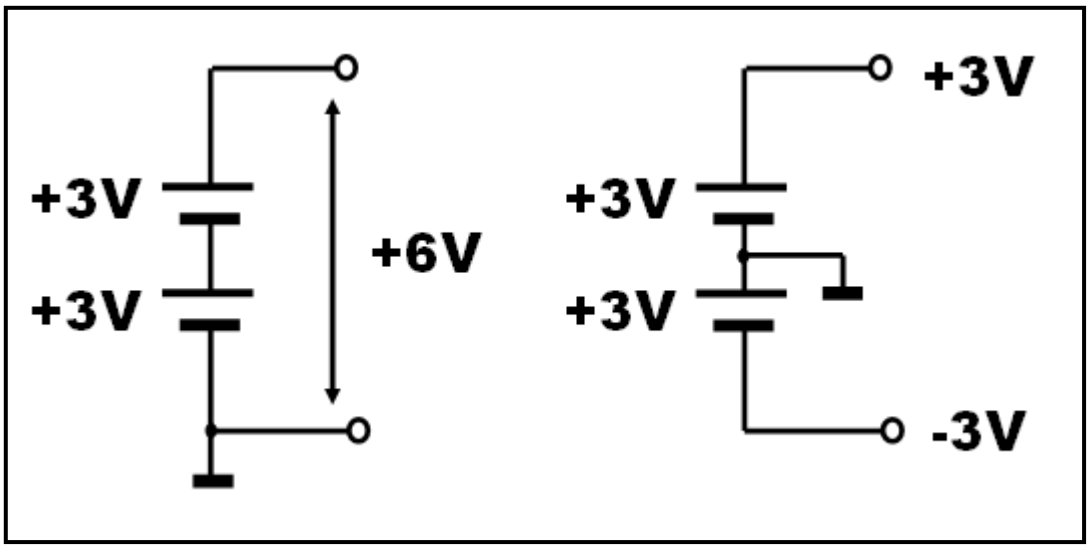


Figure 3.21: (a) Addition Connection (Left)
(b) Positive and Negative Connection (Right)

The reason for being able to harvest a negative supply can be explained in Figure 3.21. It resembles the connection of two batteries, when two of them are connected in series, the voltage is just simply adding up as shown in Figure 3.21 (a). However, if two batteries were to connect in series and the ground is pulled out from the middle, positive and negative supplies can be obtained as shown in Figure 3.21 (b).

Same analogy is applied to the connection in Figure 3.20. The two capacitors C3 and C4 are connected in series with the middle pulled to ground. Thus, ±14 V and ±5 V can be obtained.

3.6 Simulation on Transistors

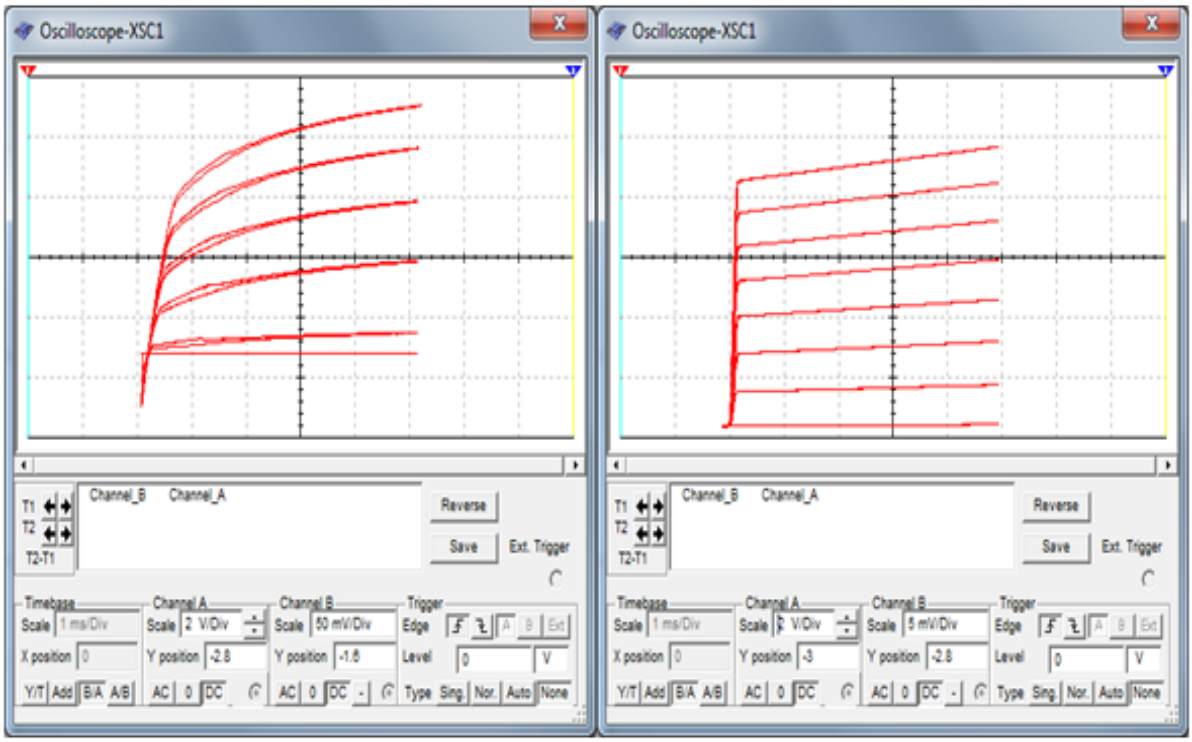


Figure 3.22: (a) Simulation of 2N6669 nFET (left)

(b) Simulation of 2N3904 NPN (right)

Simulation from Multisim, March 10, 2011

Figure 3.22 (a) shows a 2N6669 n-channel FET simulated in Multisim. Figure 3.22 (b) shows a 2N3904 NPN BJT also simulated from Multisim. It is to be distinguished that FET has a slope curve as compared to the straight line BJT.

CHAPTER 4

RESULTS AND DISCUSSIONS

4.1 Bread Board Trial

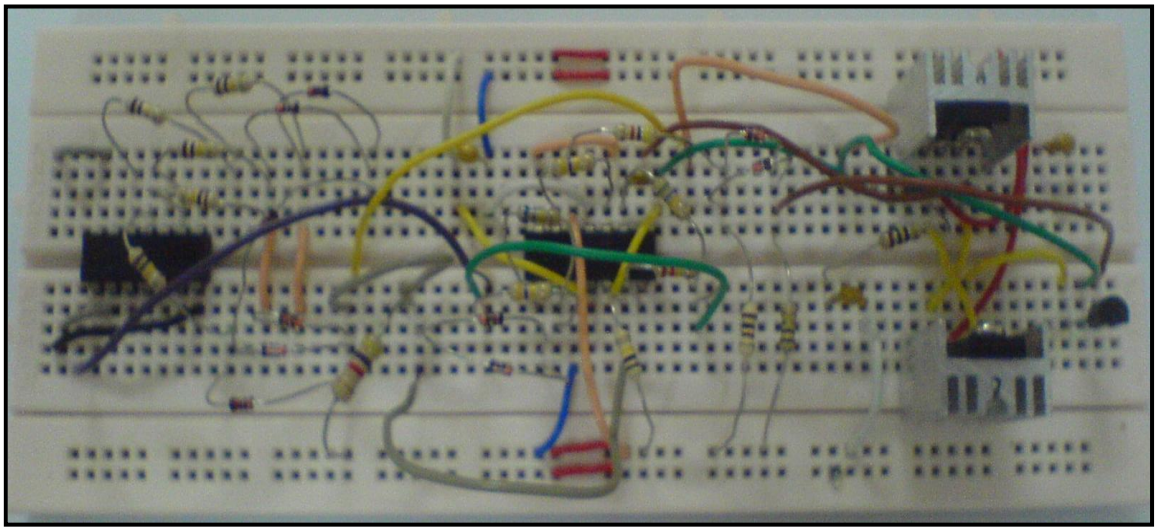


Figure 4.1: Bread Board of Transistor Curve Tracer

Retrieved December 20, 2010

Figure 4.1 shows the bread board connection. Rather messy as it is, but this is a necessity to test the usability of the circuit. It is also essential to obtain the square and triangular waveforms at every terminal. Troubleshooting on problems can be done easily and effectively for PCB does not afford to give the waveforms. When system validation is completed, it proceeds with PCB.

4.2 Printed Circuit Board (PCB)

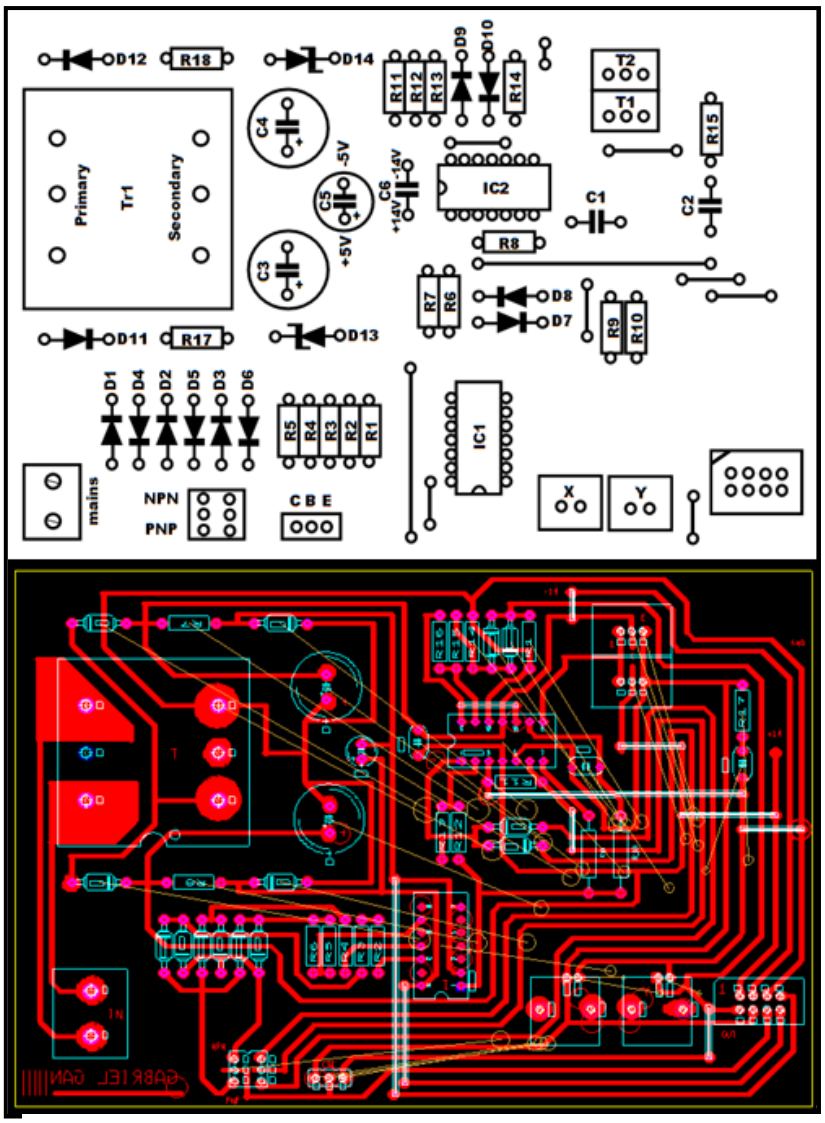


Figure 4.2: (a) PCB Sketch (Top)

(b) PCB Design (Bottom)

Retrieved March 20, 2011

Figure 4.2 shows the design of the transistor curve tracer. It was manually sketched (Top) before being drawn in the software called Ultiboard (Bottom). It was a triumph for the PCB over bread board in many aspects such as connection stability, power sustainability, aesthetics, miniature and etc. Hence, PCB is built.

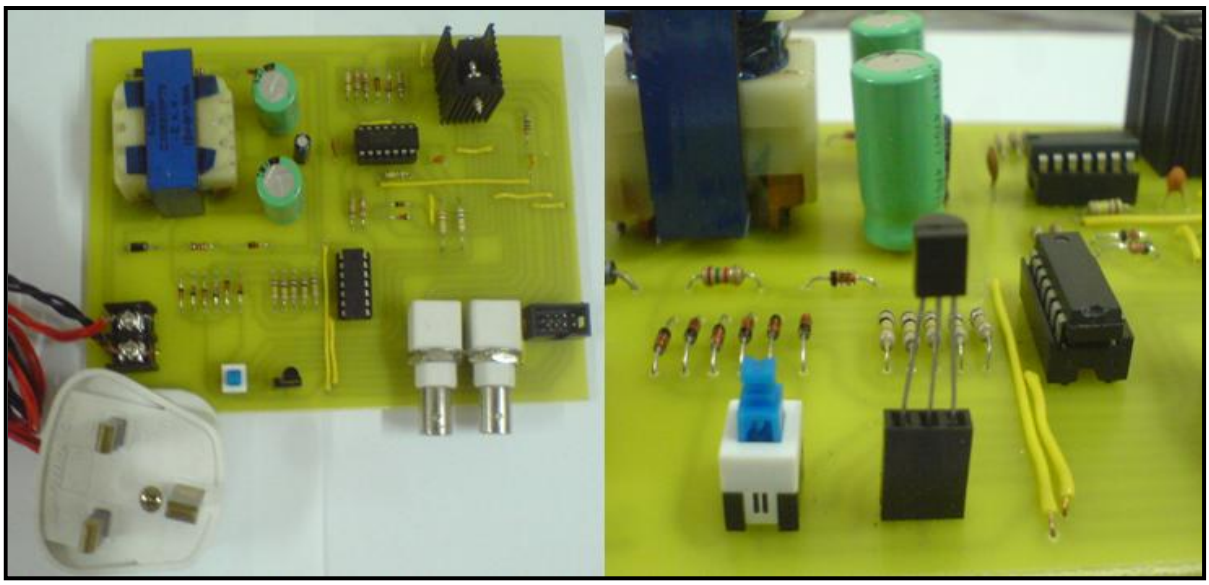


Figure 4.3: (a) Transistor Curve Tracer PCB (Left)

(b) Device Under Test (DUT) (Right)

Retrieved April 2, 2011

Figure 4.3 (a) shows the built transistor curve tracer on PCB. It has built-in power supply which take the main AC 240V, 60Hz power socket. The transformer steps down the 240V to approximately 14V and 5V. It is then being rectified and filtered to change from AC to DC. This is to feed the TL084 JFET op-amp IC and 4024 counter IC respectively.

Figure 4.3 (b) shows the DUT. The switch beside the DUT controls the polarity of base current and triangular wave (positive or negative) for the suitability of the device (n-type or p-type).

BNC sockets are attached for the signal that is to be fed into oscilloscope.

4.3 Waveforms

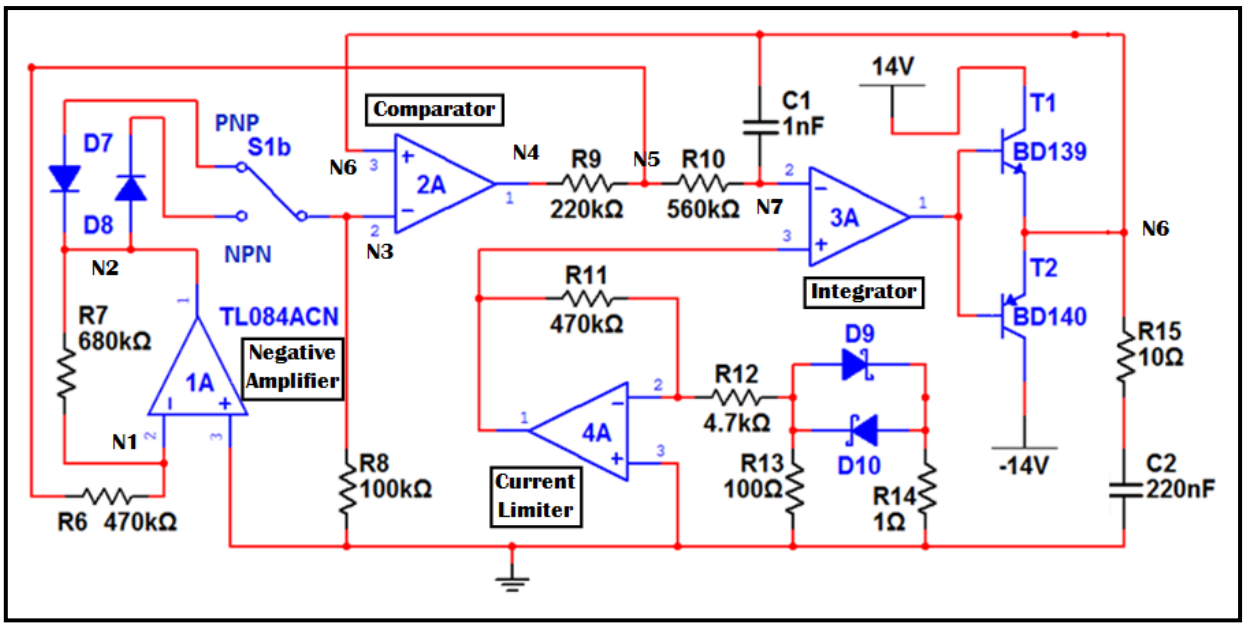
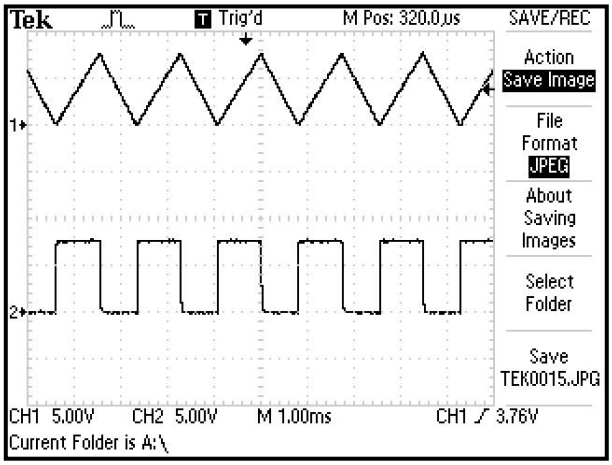


Figure 4.4: Schematic Diagram of Oscillator and Integrator

Figure 4.4 shows the schematic diagram of the oscillator and integrator. Throughout this session, this schematic will be used as a reference for all waveforms.



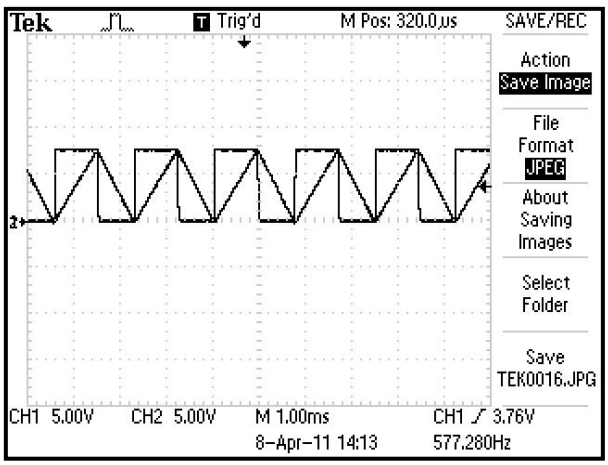


Figure 4.5: Inputs of Comparator (2A) (NPN Test Device)

Figure 4.5 shows the waveform that is inputted to comparator 2A as shown in Figure 4.4. They are Node 6 and Node 3. These actual waveforms were taken from bread board. The triangular waveform is the output of the integrator (N6) while the square wave is the output from the amplifier after rectified by diode (N3).

It is noted that the voltage division of the oscilloscope is 5 V/div. It tells that the triangular wave has a maximum of approximately 7.5 V and a minimum of 0 V. It is a DC voltage.

The square wave, on the other hand, has a minimum of 0 V and maximum of approximately 7.5 V as well. The frequency of the wave is approximately equal to 588 Hz as 1 full cycle is about 1.7 ms. This is about the same for calculation-wise. Formula for integrator is given by $V_{out} = -\frac{1}{C}\int_0^T \frac{V_{in}}{R_{in}}\,dt$. The input voltage to the integrator is 5 V (Figure 4.7). As it is a constant voltage,

$$T = -V_{out}\frac{C\,R_{in}}{V_{in}} \tag{4.1}$$

where

V_{out} = –7.5 V

C = 1 nF

R_{in} = 560 kΩ

V_{in} = 5 V

Upon calculation, T = 0.84 ms, T_p = 2T = 1.68 ms, f = 595 Hz. This result is very close to the frequency as shown in oscilloscope. The right figure shows the relation of the 2 waves. The comparator compares both waves to produce a square wave.

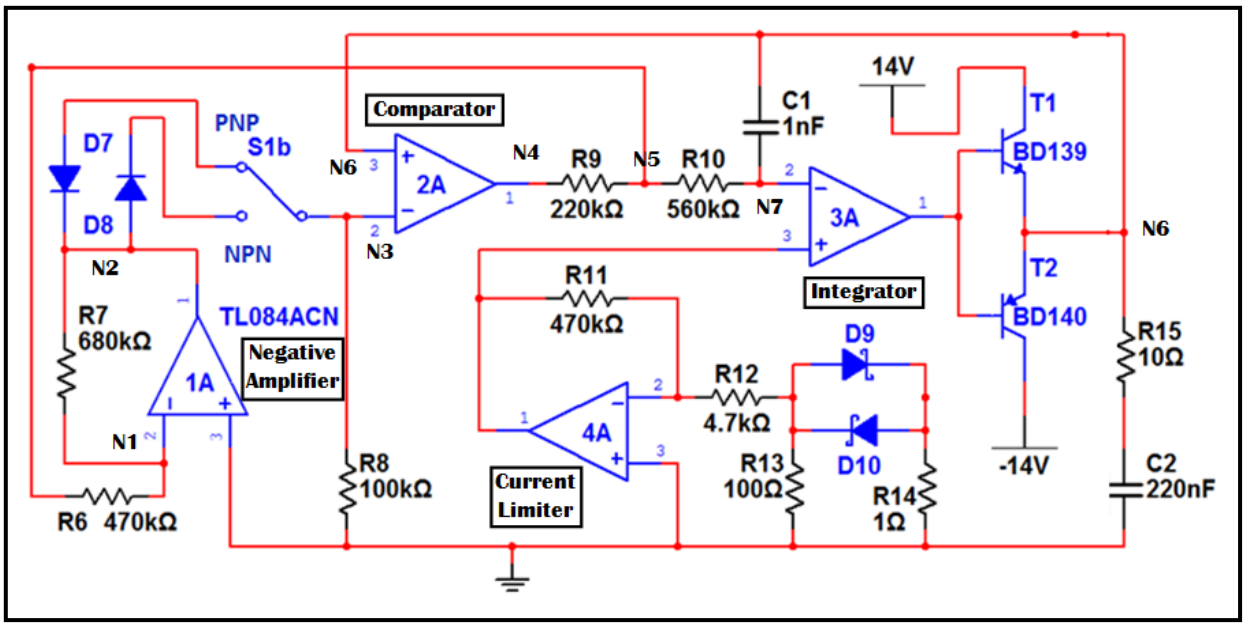


Figure 4.6: Schematic Diagram of Oscillator and Integrator

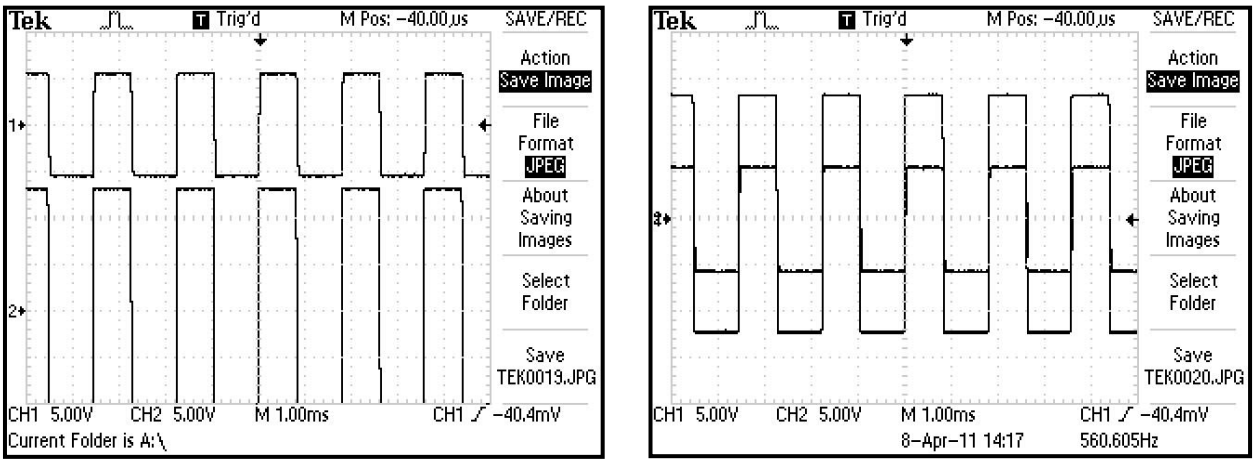


Figure 4.7: Outputs from Comparator (Before and After Resistor R9)

The output from the comparator results from the DC triangular and DC square wave can be seen in Figure 4.7. The top portion is the wave after resistor R9 (Node 5), a current limiting resistor. The bottom part is the wave just right after the comparator, before resistor R9 (Node 4).

From Figure 4.7, the output from Node 4 has a maximum of +12 V and a minimum of –12 V. It is an AC wave. This is rather true as the output of comparator will saturate to the positive-most or negative-most voltage. On the other hand, the

output from Node 5 has a reduced maximum of +5 V and minimum of –5 V. It is also an AC wave. Resistor R9 in Figure 4.6 plays the role of limiting the current. It could be observed that at Node 5, 560 kΩ and 470 kΩ resistors are connected in parallel to ground while 220 kΩ resistor is connected in series with them. The reduced voltage across resistor R9 is thus:

$$V_{red} = \frac{R9}{R9 + (R10//R6)} (V_{N4}) \tag{4.2}$$

where

R9 = 220 kΩ

R10 = 560 kΩ

R6 = 470 kΩ

V_{N4} = 12 V

The reduction in voltage across R9 is approximately 5.55V which is rather close to the waves from oscilloscope, 12 V – 5 V= 7 V. Slight difference could be due to the non-ideal characteristic of the op-amp. In ideal case, the inverting and non-inverting input can be considered as ground. This imperfection of the op-amp causes the slight difference in between theory and practical cases.

Figure 4.7 on the right shows that both of them are aligned but with a reduction in voltage level.

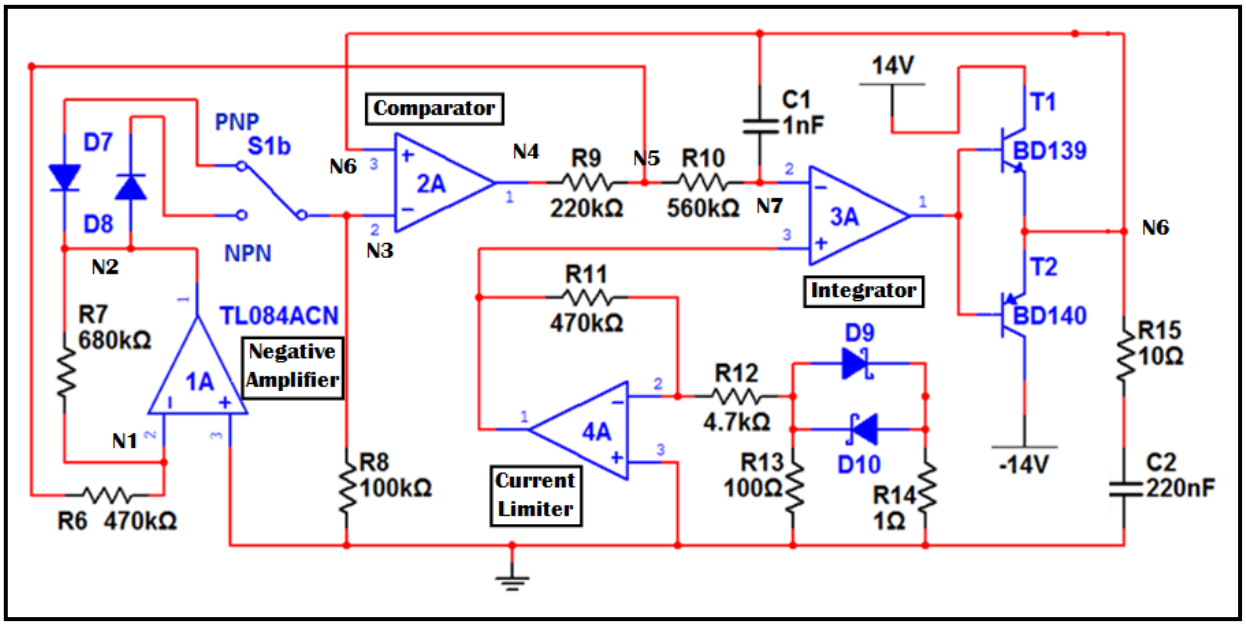


Figure 4.8: Schematic Diagram of Oscillator and Integrator

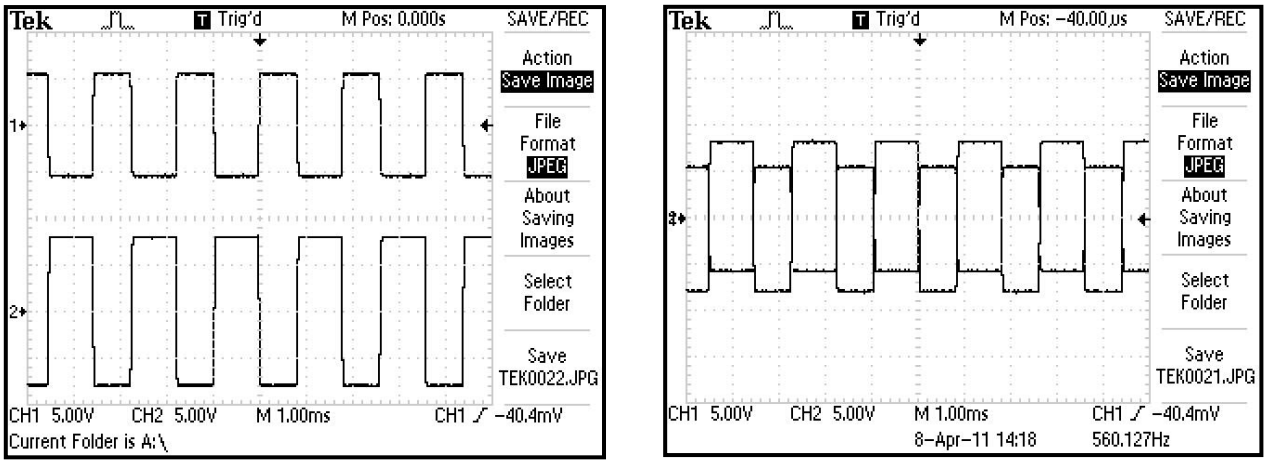


Figure 4.9: Input and Output of Amplifier (1A)

Figure 4.9 shows the wave from the amplifier. They are in Node 5 (Top Wave) and Node 2 (Bottom Wave) as depicted in Figure 4.8.

The top waveform is essentially the output from the comparator after resistor R9 (N5). Thus, it is a ±5 V AC voltage. The bottom waveform, on the other hand, is the output from the amplifier (N2). The connection of the amplifier, shown in Figure

4.8, is known to be inverting feedback amplifier. 680 kΩ is the feedback resistor while 470 kΩ is the input resistor. The formula goes with:

$$V_{out} = -\frac{R_f}{R_{in}}(V_{in}) \tag{4.3}$$

where

R_f = 680 kΩ

R_{in} = 470 kΩ

V_{in} = ±5 V

V_{out} is ±7.5 V, a gain of approximately –1.5. It is shown that the bottom wave has a maximum and minimum of ±7.5 V and is inverted or a phase shift of 180^0. Therefore, the theoretical and practical cases coincide.

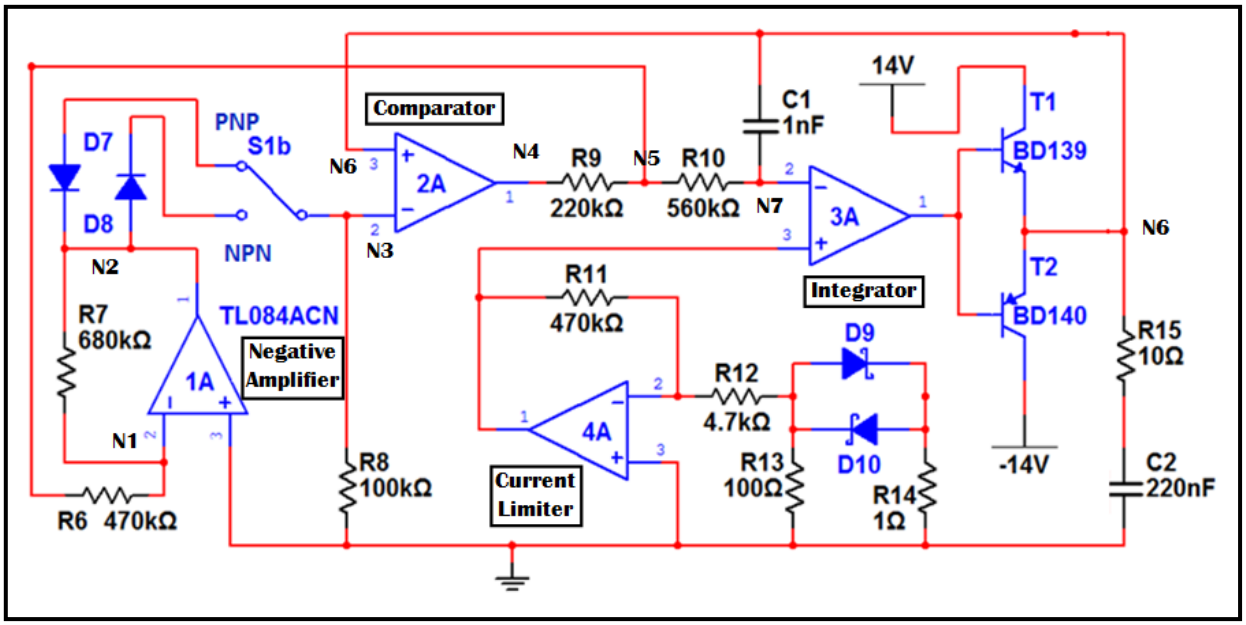


Figure 4.10: Schematic Diagram of Oscillator and Integrator

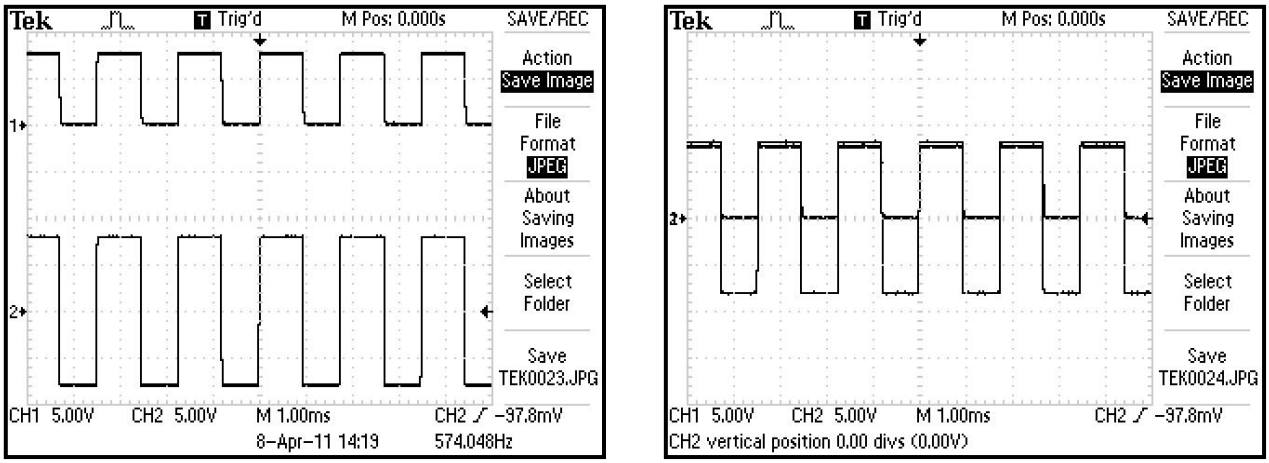


Figure 4.11: Outputs from Amplifier (Before and After Diode)

D7 and D8 diodes from Figure 4.10 are responsible in eliminating the reverse biased portion (npn or pnp). Figure 4.11 shows the waveforms from the amplifier: eliminated waveform (N3) (Top Wave) and not-eliminated waveform (N2) (Bottom Wave). It is shown on the right of Figure 4.11 that both waves were identical excluding the eliminated portion results from the action of diode.

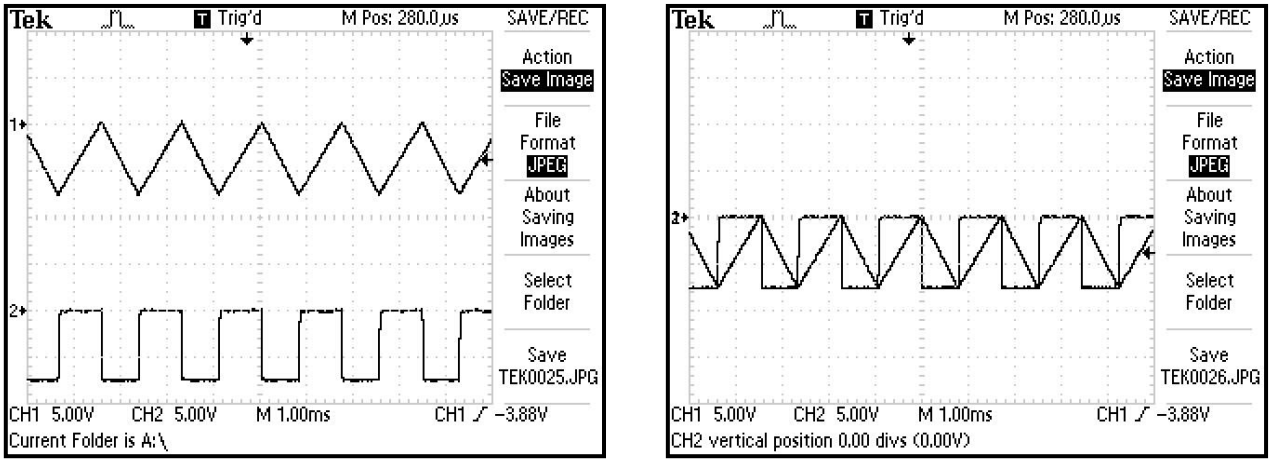


Figure 4.12: Inputs of Comparator (2A) (PNP Test Device)

Figure 4.12 shows the inputs of comparator waveforms. It is identical as Figure 4.5 except for being a negative DC voltage. It can be seen that the triangular wave has maximum of 0 V and minimum of –7.5 V while the square wave has maximum of 0V and minimum of –7.5 V. The switch S1b in Figure 4.10 is responsible for governing the npn and pnp operation.

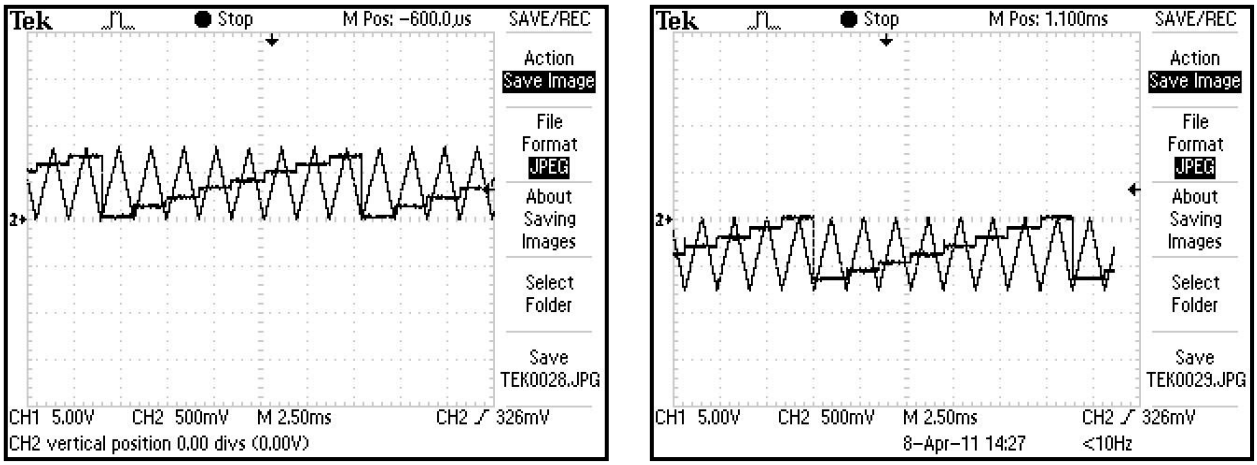


Figure 4.13: Triangular Wave and the Staircase Base Current

(a) NPN Test Device (Left) (b) PNP Test Device (Right)

Figure 4.13 shows the triangular wave and staircase base current. On the left is positive DC voltage and current for NPN. On the right is negative DC voltage and current for PNP.

As shown in the graph, the triangular wave and staircase base current are synchronised. Every step of current is linked to a positive and negative slope. This denotes that "every single behaviour" of the transistor (+ slope and – slope) is tied to a single step current. Therefore, the 3 synchronised waveforms can display the transistor curves.

4.4 Interpretation on Results

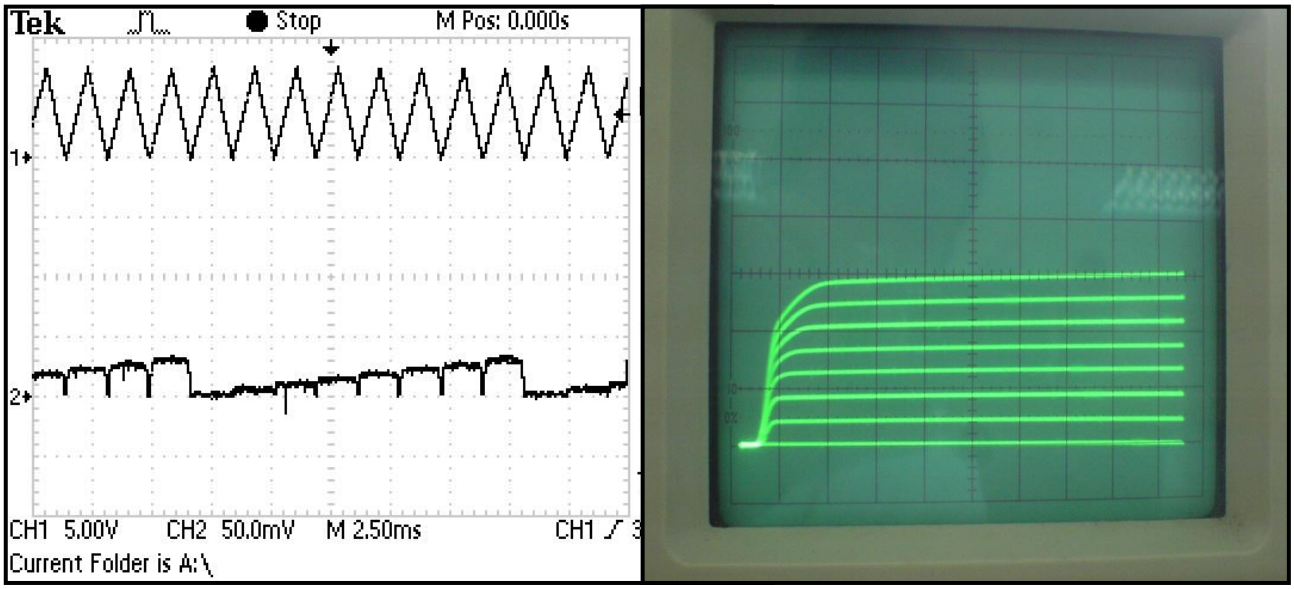


Figure 4.14: (a) V_{CE} and I_C waveforms (Left)
(b) 2N3904 NPN BJT curves (Right)

Figure 4.14 shows the collector-emitter voltage waveform and the collector current waveform.

As mentioned earlier, sawtooth waveform generated internally from the oscilloscope cannot be used as it is a rapid moving wave that does not return to origin. Essentially, the curve can be seen as shown in Figure 4.14 (a), a series of resultant collector current, I_C. This is not desirable as we want a static waveform something resembles in Figure 4.10 (b). Therefore, a triangular wave is built. The tricky part of a triangular wave is that upon the negative slope of the triangular wave, the beam on oscilloscope is deflected back from right to left. It is therefore visible and perceptible with our eye. Nonetheless, this will be discussed later.

Figure 4.10 (b) shows the curves of 2N3904 NPN transistor (*2N3904*, 2001). The X-axis is V_{CE} with oscilloscope division of 0.5 V/div. Y-axis is I_C with current division of 5 mA/div. It can be seen that 2N3904 transistor requires roughly 0.4 V in

the V_{CE} for conduction. For a base current of 175 μA, the maximum I_C it could conduct is 15 mA. It is at saturation state. Voltage of 1 V in the V_{CE} sends the whole transistor into saturation mode. Apart from that, it is noticed that it has a "quasi-saturation" region for a base current of 175 μA. Base currents of 0 to 150 μA were not so obvious though.

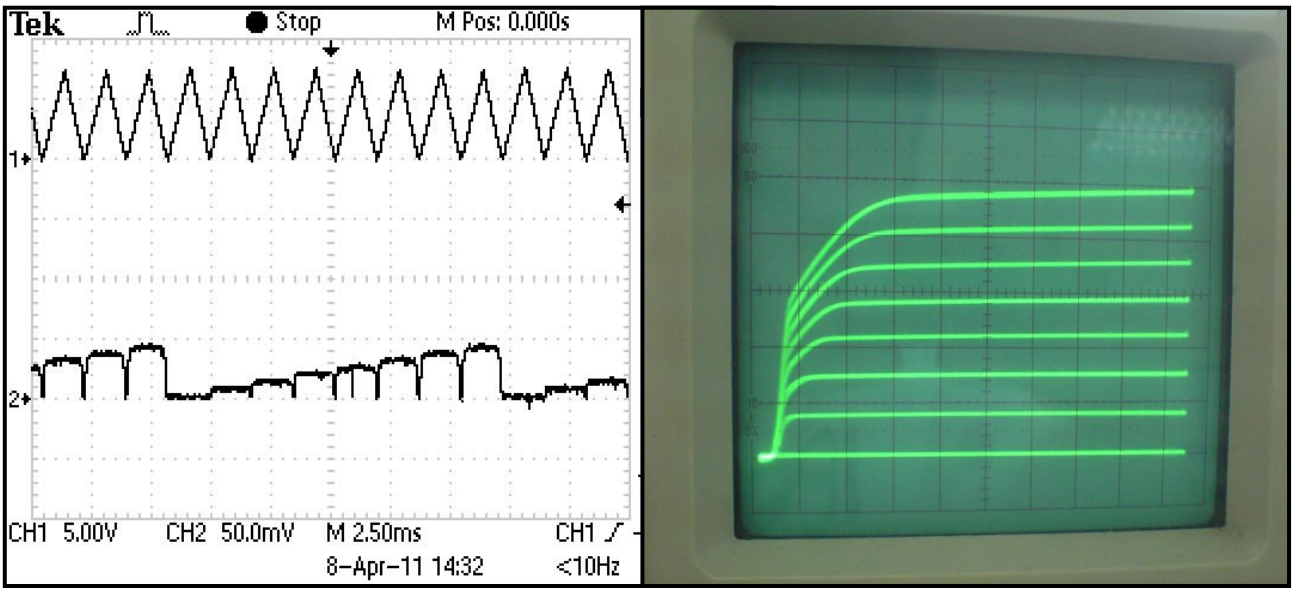


Figure 4.15: (a) V_{CE} and I_C waveforms (Left)
(b) BC547 NPN BJT curves (Right)

Figure 4.15 shows the curve of a NPN BC547 BJT (*BC547*, 2002). As compared with 2N3904, it can be seen that the collector current is larger for BC547.

The X-axis division is 0.5 V/div and Y-axis is 5 mA/div. It is shown that this transistor has a threshold V_T of 0.25 V which is lower than 2N3904. Besides, the maximum collector current can go up until 25 mA for the same 175 μA base current. Furthermore, it reaches saturation mode when V_{CE} exceeded 1.5 V. This portrays advantages of BC547 transistor to 2N3904.

The quasi-saturation region is rather significant for this transistor. Quasi-saturation region is a region whereby the transistor is in between the linear and saturation region. Typically, power transistor exhibits a rather significant quasi-

saturation feature. It is assumed that BC547 might not be as great as power transistor but is in the upper-end of a normal transistor.

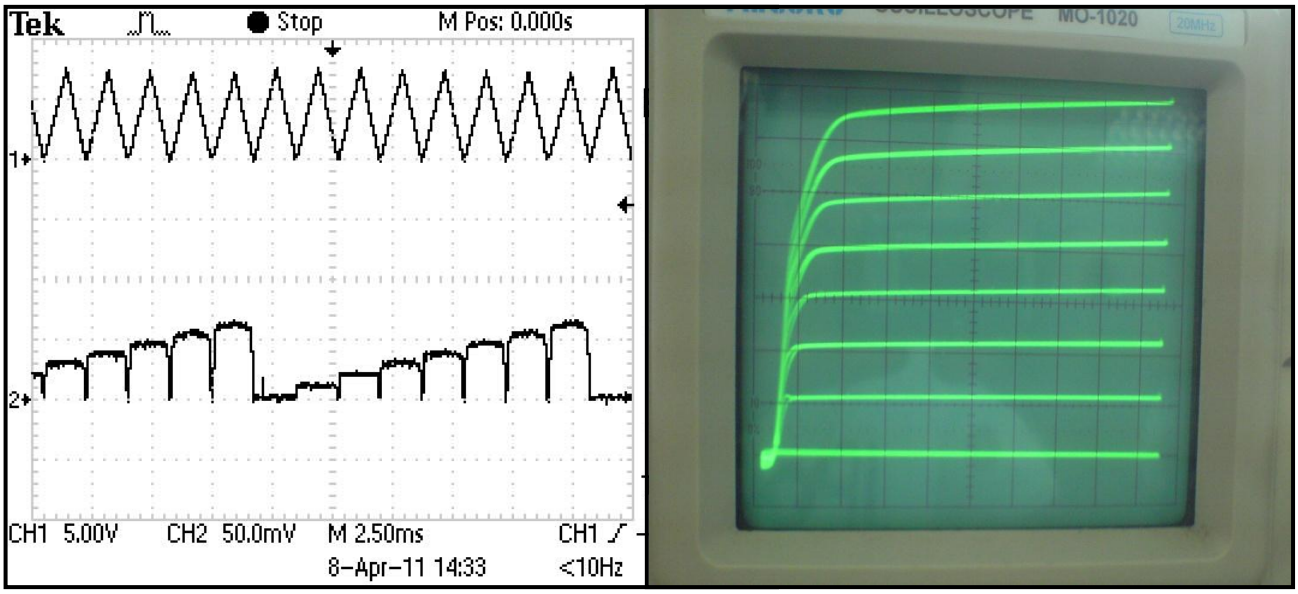


Figure 4.16: (a) V_{CE} and I_C waveforms (Left)
(b) PN100 NPN BJT curves (Right)

Notice that the collector current in Figure 4.16 is significantly larger than 2N3904 and BC547. As expected, the curves will be larger as shown on the right.

The X-axis division is again, 0.5 V/div and Y-axis is 5 mA/div. It reaches saturation at V_{CE} = 1 V. However, it has a threshold voltage of 0.2 V and a maximum of 35 mA of collector current to conduct for a base current of 175 μA. By comparing on 2N3904, BC547 and PN100 (*PN100*, 1998), PN100 established a higher gain pronouncedly. Comparison amongst the three NPN transistors is illustrated in Table 4.1.

Table 4.1: Comparison of 3 NPN Transistors

		2N3904 (NPN)	BC547 (NPN)	PN100 (NPN)	Units
V_T (Threshold)		0.4	0.25	0.2	**V**
V_{sat} (I_B= 175 µA)		1	1.5	1	**V**
I_C (sat)	**I_B (µA)**				
	0	0	0	0	**mA**
	25	2	4	6	**mA**
	50	4.5	7.5	11	**mA**
	75	6.5	11	16	**mA**
	100	8.5	14	21	**mA**
	125	11	17.5	26	**mA**
	150	13	21.5	31	**mA**
	175	15	25	35	**mA**
β (Average)		86.14	146.14	214	**-**

From Table 4.1, it compares the threshold voltage V_T, saturated voltage V_{sat} for base current of 175 µA, collector current I_C for different base current I_B, and last but not least the dc current gain, β.

The tabulated results show that PN100 NPN transistor prevails in every aspect shown in Table 4.1. It has the lowest threshold and saturated voltage and the highest collector currents with respect to every base current and has the highest gain in average.

2N3904 and BC547 are considered to have a low dc current gain as compared to PN100. However, suitable transistor can still be chosen depending on the application. Some application, such as switch, necessitates a low dc current gain and low collector current makes 2N3904 NPN transistor ideal for the case. This will be power saving as compared to PN100.

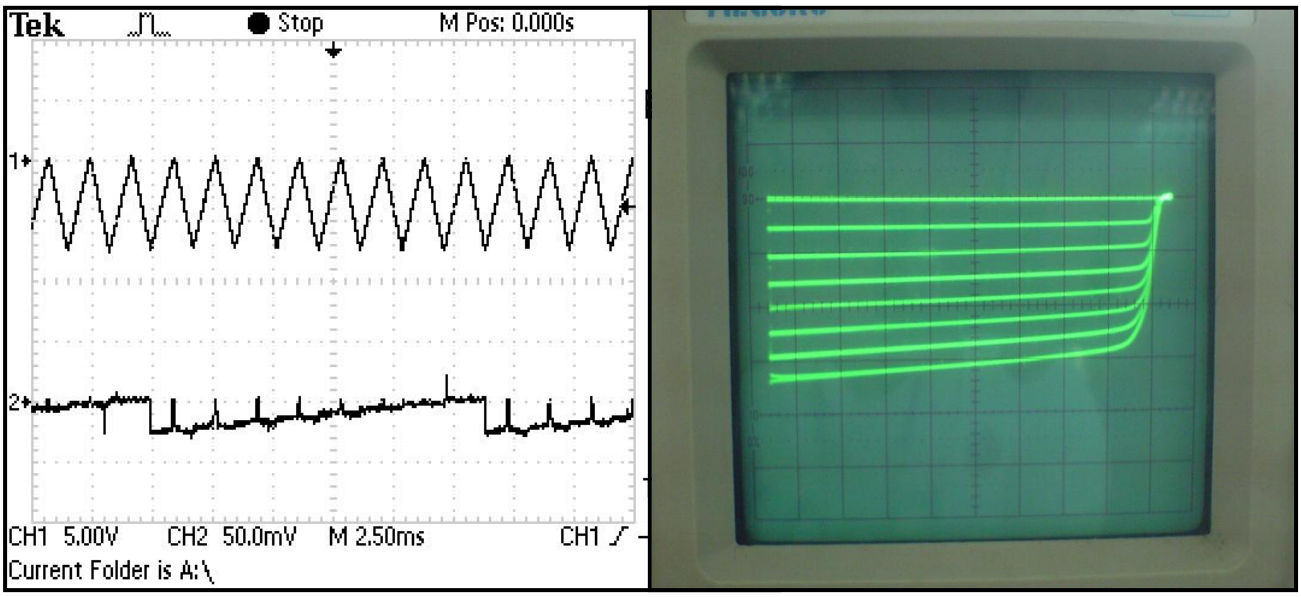


Figure 4.17: (a) V_{CE} and I_C waveforms (Left)
(b) 2N3906 PNP BJT curves (Right)

Figure 4.17 shows the curve for a 2N3906 PNP transistor (*2N3906*, 2003). Notice the collector current at Figure 4.17 (a) is sort of an inverted "Y" shape. The collector current for NPN is indeed, however, sort of an "n" shape. Both cases coincide because NPN works in positive current while PNP works in negative current.

The X-axis division is 0.5 V/div and Y-axis is 5 mA/div. It shows that this transistor has a threshold V_T of –0.3 V and saturated voltage of V_{sat} = –0.6 V. Besides, the minimum collector current for a base current of –175 μA is –17.5 mA.

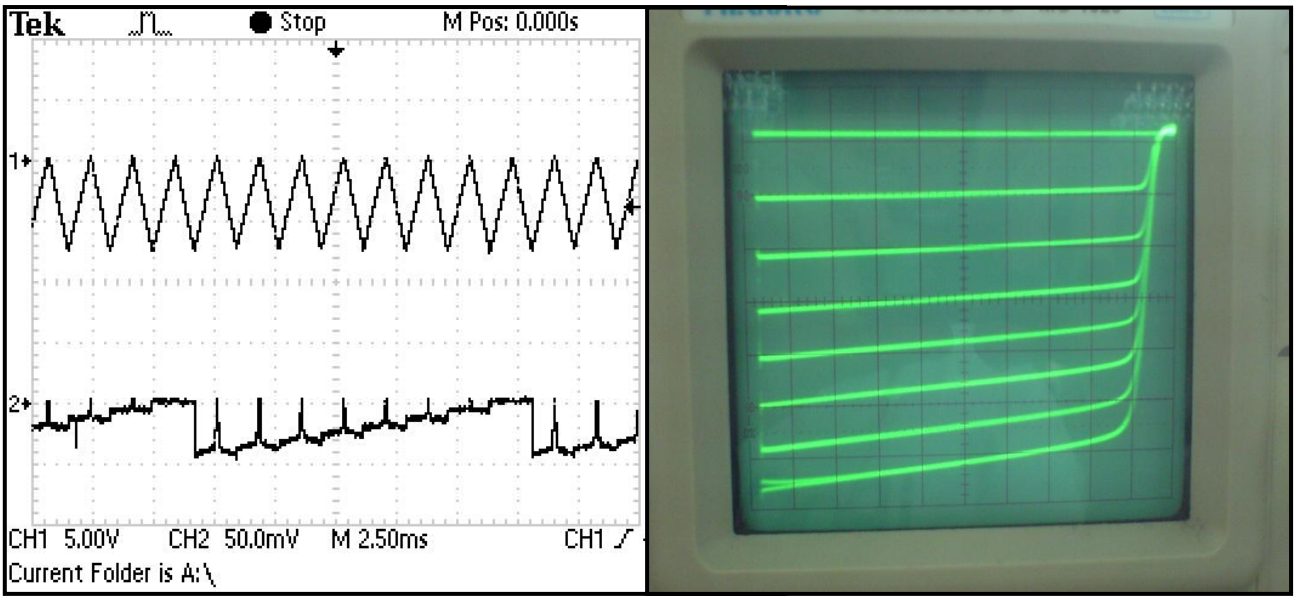


Figure 4.18: (a) V_{CE} and I_C waveforms (Left)
(b) C557B PNP BJT curves (Right)

It is quite apparent that the collector current wave is, literally, an inverted "Y" shape as mentioned above. The amplitude is bigger. Thus, Figure 4.18 (b) shows a larger amplitude curves.

The X-axis division is 0.5 V/div and Y-axis is 5 mA/div. It has a threshold of –0.2 V. The saturation voltage is roughly –0.5 V. The minimum collector current would be –32.5 mA for a base current of –175 μA. By comparing the C557B (*C557B*, 2005) and 2N3906, C557B is said to be able to sustain a higher negative current.

Table 4.2: Comparison of 2 PNP Transistors

		2N3906 (PNP)	C557B (PNP)	Units
V_T (Threshold)		–0.3	–0.2	V
V_{sat} (I_B= –175 μA)		–0.6	–0.5	V
I_C (sat)	**I_B (μA)**			
	0	0	0	mA
	–25	–2.5	–5	mA
	–50	–5	–11	mA
	–75	–7.5	–16	mA
	–100	–10	–20	mA
	–125	–12.5	–25	mA
	–150	–15	–28	mA
	–175	–17.5	–32.5	mA
β (Average)		100	200.86	-

Table 4.2 compares the threshold voltage V_T, saturated voltage V_{sat} for base current of –175 μA, collector current I_C for different base current I_B, and as well as the dc current gain, β.

The tabulated results show that C557B transistor prevails in every aspect shown in Table 4.2. It has the lowest threshold and saturated voltage and the highest collector currents with respect to every base current and has the highest gain of 200.86 in average.

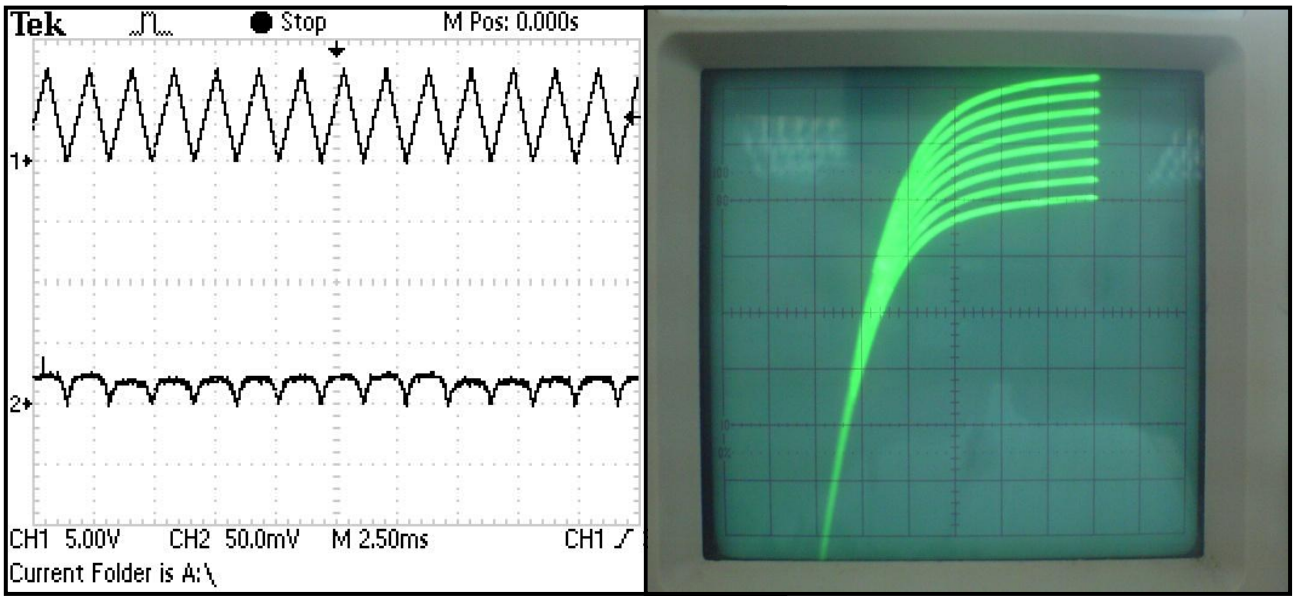


Figure 4.19: (a) V_{DS} and I_D waveforms (Left)
(b) 2N3819 n-channel JFET curves (Right)

Figure 4.19 (a) shows the supplied drain-source voltage and "Drain" current graph across the 2N3819 n-channel JFET transistor.

The supplied "Gate" voltage was described in Table 3.1. They are 0, 0.1175 V, 0.2350 V, 0.3525 V, 0.4700 V, 0.5875 V, 0.7050 V, and 0.8225 V. It is because the range of the supplied "Gate" voltage is small than causes the insignificant changes of "Drain" current in Figure 4.19 (a). There is however an increment of current though.

Figure 4.19 (b) shows the transistor curves. The X-axis of the oscilloscope is 0.5 V/div while the Y-axis is 5 mA/div which is very small. The maximum current is approximately 40 mA for a "Gate" voltage of 0.8225 V. The "Drain" current could have achieved higher for a higher gate voltage.

It is noted there is current for V_G = 0V. 2N3819 is in fact an n-channel enhancement JFET transistor. It can operate at "Gate" voltage equal to zero. In accordance with 2N3819 datasheet, the typical gate-source cutoff voltage is –3 V or a maximum of –8 V (*2N3819*, 2002). Thus, this justifies this is an n-channel enhancement JFET transistor.

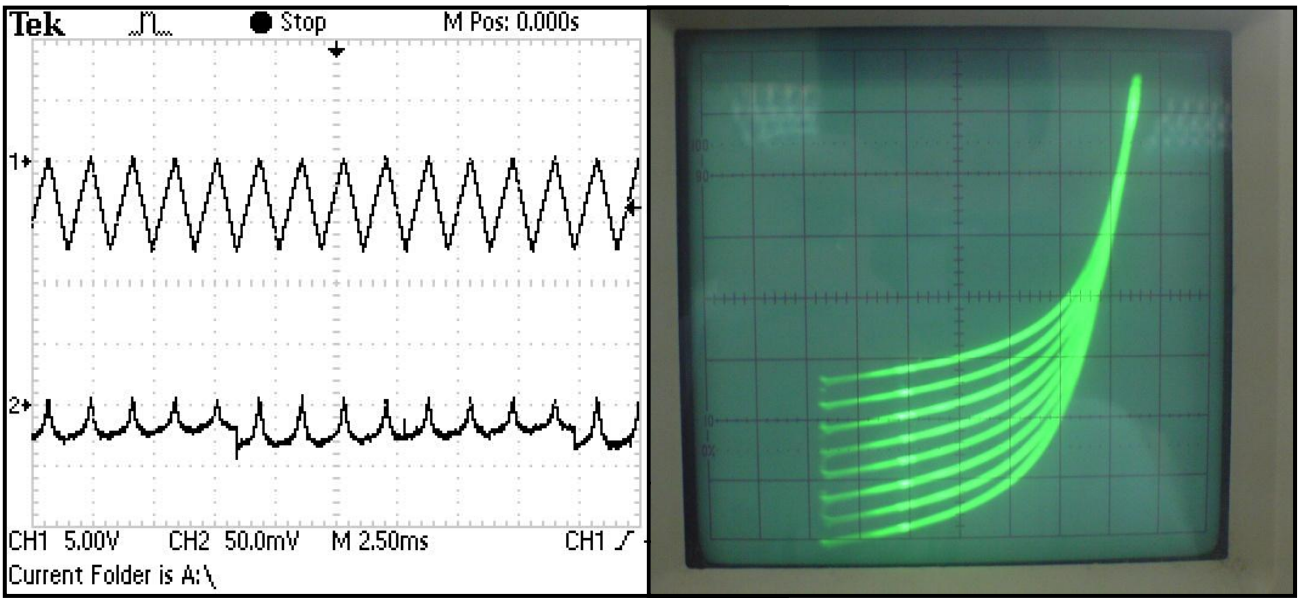


Figure 4.20: (a) V_{DS} and I_D waveforms (Left)
(b) J175 p-channel silicon FET curves (Right)

Figure 4.20 (a) shows the waveform of J175 p-channel silicon FET. Again, the supplied "Gate" voltages are 0, –0.1175 V, –0.2350 V, –0.3525 V, –0.4700 V, –0.5875 V, –0.7050 V, and –0.8225 V. It is not obvious for the decrement of "Drain" current in Figure 4.20 (a).

Figure 4.20 (b) shows the transistor curves. The X-axis of the oscilloscope is 0.5 V/div while the Y-axis is 5 mA/div. The minimum current is approximately –37.5 mA for a "Gate" voltage of –0.8225 V. The "Drain" current could have achieved higher for a higher gate voltage.

It is again noted there is current for V_G = 0V. This tells that J175 is a p-channel enhancement silicon FET transistor. J175 datasheet reveals that it can operate at "Gate" voltage equal to zero and the typical gate-source cutoff voltage is 3 V or a maximum of 6 V (*J175*, 1997). Thus, this justifies this is an n-channel enhancement JFET transistor.

4.5 Comprehension on Results

The main objective for this project is to plot curves of the transistors. A conventional oscilloscope has built-in sawtooth generator in measuring voltages or waveforms. It is however inappropriate for the transistor curve as does not display in a single static graph but a series of repetition graphs. In fact, the normal voltage measurement of circuit uses this sawtooth waveform as the time division. This is illustrated in Figure 4.21.

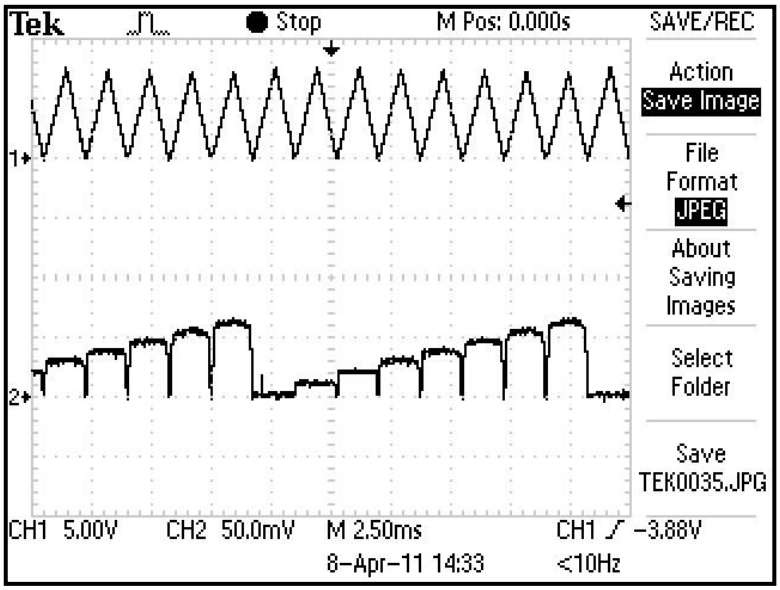


Figure 4.21: V_{CE} and I_C waveforms for PN100 NPN Transistor

It is clearly shown that the series of pulses cannot reveal the information that is desired but simple patterns that are needed to be translated. Triangular wave prevails primarily in the inheritance of the gradual gradient of the negative slope. This negative slope pushes the electron beam of the oscilloscope back to the origin and when the positive slope comes in, it starts to deflect again, appear to draw a static graph. This is the reason frequency of the triangular wave plays a vital role in draw the line.

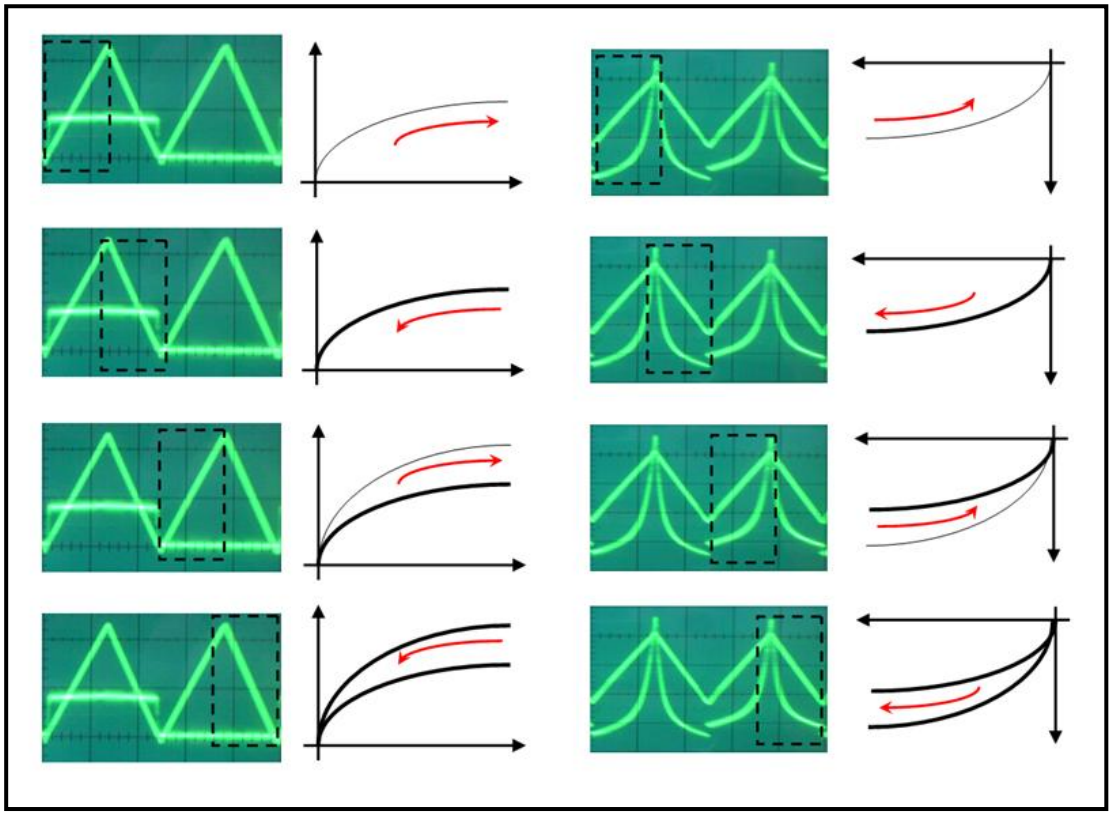


Figure 4.22: Operation in Oscilloscope

Figure 4.22 illustrates the basic operation of the oscilloscope. Initially the electron beam got deflected to the right with a particular vertical deflection. When the negative slope comes in, it got pushed back to the origin with the same orientation. Basically, in every cycle of the triangular wave, the oscilloscope draws twice in the exact position. It then continues with a different gate voltage.

4.6 Discussions

4.6.1 Capacitance effect

Stray capacitance causes high impact in this project. As mentioned earlier, it is wise to use high frequency waves as eyes cannot perceive the high speed deflecting beam. However, the high frequency (5 kHz) introduces stray capacitance effect. The result is a huge attenuation suffered in the triangular wave and results in distorted output curves.

The stray capacitance originated particularly from the messy interconnection of the copper wire (jumper) at bread board in Figure 4.1 and the near located copper strips of PCB in Figure 4.2 (b). Fundamentally, a capacitor consists of a pair of conductors separated by a dielectric. When a potential difference is applied to the terminal pairs, it behaves as a capacitor. The reactance of a capacitor is $X_C = 1/j\omega C$. Therefore, interconnections of wires or near-located copper strips reacts as if in short-circuit at high frequency. This affects the overall connection and thus distortion occurred.

Ways to overcome this problem go with 2 methods:

1. Use lower frequency to reduce the effect of stray capacitance, but not too low to deteriorate in the vision at oscilloscope.
2. Place a filter to eliminate unwanted noise.

The original frequency of 5 kHz is hence reduced to approximately 600 Hz in such that the stray capacitance does not play an imminent role in attenuation. Furthermore, resistor R15 and capacitor C2 in Figure 3.5 are the major role in remove noise and to comply with the parasitic capacitance of the probes of the oscilloscope.

4.6.2 Heat Sink

Heat sink is a necessity for the power transistors BD 139 and BD 140 in Figure 3.5. This is because while the power transistor may withstand high current flow, the components within the power transistor might not able to withstand the heat. Therefore, heat sink plays the role in dissipating heat.

4.6.3 Alternative Design

4.6.3.1 555 Timer

There are always alternative ways in producing the desired outcome. For this topic, the main ingredients are square and triangular wave that are to be fed into transistors. When square wave comes in mind, the basic idea for creating such a wave falls into comparator. Having the characteristic of comparing, square wave can be outputted through proper measurement. It is because the comparator outputs the positive-most voltage when the inverting input is smaller than the non-inverting input and vice versa.

Alternative way in producing square wave falls under a single IC chip 555 timer. Using astable mode, 555 timer was able to produce a desired frequency square wave with the aid of some components. However, one can notice that components in 555 timer are actually comparators. It consists of 2 op-amps which response to the maximum and minimum limits. Unlike the design showed in Figure 3.5, triangular wave cannot be harvested in anywhere within the 555 timer. An extra op-amp is needed to perform integration. Figure 3.5 shows that 2 op-amp can perform comparison and integration. For the sake of circuit miniature and simplicity,

comparator is used instead of 555 timer. Table 4.3 compares the implementation of 555 timer with the comparator circuit.

Table 4.3: Comparison between 555 Timer and Comparator Circuit

	555 Timer	**Comparator Circuit**
Comparator	Can be built by using astable mode.	Integrator and inverting amplifier are required.
Integrator	Required	It is within in the design
Current Limiter	Required	Required
Inverting Feedback Amplifier	Not required	Required

Since that a single TL084 chip incorporates comparator, inverting amplifier, integrator and current limiter while 555 timer requires 2 addition op-amps for integrator and current limiter, it is wise to use the comparator circuit for the sake of saving cost.

4.6.3.2 Journals

The transistor and FET curve tracer by Daniel Metzger (2002) gives much complication in the design. It goes for a larger boundary whereby:

- Able to observe effect of temperature on transistor.
- Able to observe curves of diodes, zener diodes and photocells.

His intuitive design gives a wider specification on the device but the design is way too complicated. Moreover, it is bulky due to the built-in oscilloscope within the device. It is much costly for the objective of this project. However, the simple idea on displaying the characteristic curves is referred and is illustrated in Figure 3.3.

The journal of CAI system for electronic circuit design written by Ono et al. (1991), on the other hand, spare all of the design on computer software. It plots the

graph of various devices on monitor screen and uses C language to interpret the result. Although the inputs to the base and collector terminal are manually adjusted, this provides an innovative idea for this project.

The main objective in this project is to build a low-cost transistor curves tracer. Table 4.4 shows the cost of the components and it is evidenced that they are relatively cheap.

Table 4.4: Cost of Components

Items	**Qty.**	**Cost Each**	**Cost**
TL084	1	RM1.50	RM1.50
CD4024	1	RM1.20	RM1.20
IC socket 14pins	2	RM0.15	RM0.30
BD139	1	RM0.80	RM0.80
BD140	1	RM1.00	RM1.00
Heat Sink	2	RM0.60	RM1.20
BAT85	2	RM0.50	RM1.00
1N4148	8	RM0.10	RM0.80
Zener Diode 5V6; 400mW	2	RM0.90	RM1.80
1N4001	2	RM0.90	RM1.80
Electrolyte Capacitor 1000µF/ 25V	2	RM0.70	RM1.40
Electrolyte Capacitor 10µF/ 16V	1	RM0.20	RM0.20
M/L capacitor 102	1	RM0.15	RM0.15
M/L capacitor 104	1	RM0.15	RM0.15
M/L capacitor 224	1	RM0.20	RM0.20
Resistors 1/4W 5%	20	RM0.03	RM0.60
BNC socket	2	RM2.20	RM4.40
DPDT switch Push on Button	4	RM0.40	RM1.60
Transformer 1.5VA, 15V	1	RM12.00	RM12.00
2-way screw terminal block	1	RM0.60	RM0.60
		Total	**RM32.70**

CHAPTER 5

CONCLUSION AND RECOMMENDATIONS

5.1 Conclusion

In this project, FET curves tracer has been successfully developed with a series of 8 different gate voltages. The next objective of building a BJT curves tracer has been successful as well. The FET utilises converted voltage from current of the BJT. The designed PCB is relatively simple to use. Two switches: one to control the type of transistor (BJT or FET), the other controls the polarity type of transistors (n-type or p-type). Two BNC sockets: X-axis socket to be connected to oscilloscope's X-axis and Y-axis socket to be connected to oscilloscope's Y-axis via probes. Lastly, place the transistor in the transistor holder. Clearly it is user-friendly for only several steps are required before the tracer could be used. The size of the PCB measures 15cm×10.5cm (one quarter of an A4 paper) and the height rise to 3.5cm tall. Evidently it is portable and cheap which have achieved the project objectives.

Obviously the downside of the design is the limitation on the specification. Commercial high-end curves tracer can perform more than adopting only transistor such as resistors, diodes, zener diodes and photocells but it is much more bulky and expensive.

In conclusion, mid-end, low cost transistor curves tracer which incorporates BJTs and FETs has been successfully built. The objective goal has been achieved.

5.2 Recommendations

Clearly there is a lot of additional development work that can be done to improve the design of this low cost transistor curves tracer. This chapter will briefly highlight areas of the design that merits improvement and additional features to make the tracer more powerful, reliable, flexible, and commercially marketability.

5.2.1 Monitor as Display Screen

The downside for this design is that it requires an oscilloscope for display. The globalised era in this modern society has it be almost all people have personal computers because of the rose of modern technology which makes computers a global necessity. However, not everyone has a conventional oscilloscope at home. Therefore, it is recommended that the display of this transistor curves tracer can be transferred from oscilloscope to monitor screen. The intuitive idea in translating analogue signal from oscilloscope to digital signal for computer purposes is by using a PIC as an ADC. It then feeds into the computer via RS-232 port. Visual Basic programming can be used to plot the graph.

The upper-hand to this idea does not fell into convenient sake alone, but digitised value in the computer allows the manipulation of graph. For example, the points on every line can be displayed; it can have internal calculation on the DC current gain of the transistors and etc. Undeniably this depicts huge benefits over using the oscilloscope screen.

5.2.2 Device Suitability

Apart from that, the design can be changed or improved for plotting the curves of other devices as well. High-end commercial marketable curves tracer does not restrict itself to transistors alone but other devices such as resistors, capacitors, inductors, diodes, photocells and etc. Such integration of devices into one curves tracer will be very profitable in the market.

The flaw on this project design is caused by the current limiter. Whenever huge current flows through the device, current limiter takes place in stopping the whole operation. Transistors will restrict limited amount of current to pass but it does not happen for other devices: resistors, capacitors and etc. Therefore, oscilloscope screen will not display anything when resistor is used as DUT. Noted that the topic of this project specifically ask to build a transistor curves tracer which has been achieved. Nonetheless, improvement can still be done.

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