HIGH SPEED SERIAL LINK CHARACTERIZATION ON MERGED POWER RAILS PLATFORM CONTROLLER HUB (PCH) PACKAGE

By

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ABSTRACT

HIGH SPEED SERIAL LINK CHARACTERIZATION ON MERGED POWER RAILS PLATFORM CONTROLLER HUB (PCH) PACKAGE

Tan Fern Nee

The Platform Controller Hub (PCH) is a family of Intel® Microchips. It serves as a central hub that houses multiple I/O functions; namely Serial-ATA (SATA), PCI-Express (PCIe), Universal Serial Bus (USB), Fast Flash, integrated clock, Peripheral Chip interface (PCI) etc. (Anon., 2012). This chip has an interesting combination of high speed and low speed I/O buffers all built into one single piece of silicon, mixing a handful of different power domains from as high as 5V, to 3.3V, and as low as 1.8V and 1.05V. In recent development, the features have increased so much that the silicon could contain more than 50 power rails, in both digital and analogue domains.

The number of power rails and pin counts are increasing at an alarming rate when new features are introduced. Year over year, the increase features on a PCH increases the power rails to about 80, and lead to increasing package size and board design complexity. In the modern engineering world, the Power Delivery Network (PDN) design goal is no longer sufficient just to achieve the

best electrical performance, but the need to achieve a smaller and lighter possible platform that can easily fit into mobile and hand-held devices such as netbook and ultrabook™. The electrical and mechanical goals become two contending requirements that must be balanced to achieve a design win in the marketplace.

In this research, two radical packages are designed and fabricated to challenge many known rules of thumb that governs good PDN performance, such as avoid merging of analogue and digital power rails; proper isolation of digital phase-locked loop (PLL) and analogue PLL power rail and maintaining at least 2:1 signal to ground ratio on the ball-map. The first package merges the high speed I/O and I/O power rails together; and core and core power rails together and reduces 24 power rails to 7 power rails. The second package aggressively merges high speed I/Os and core power rails as one, and reduces 25 power rails to 4 power rails. In a nutshell, these 2 test packages are tested and stressed while benchmark with the original package which fulfils all the rules of thumb.

Most simultaneous switching output noise (SSO) validation of high speed interfaces such as PCIe, SATA, USB, and Core logic are approached as case to case basis. It is not always clear when these interfaces are put in a common validation eco-system and stressed concurrently, what will be the functionality and performance limiter. A new methodology that maximizes the power supply noise droop of each High Speed I/O interfaces is introduced; by

implementing a concurrent test in exercising PCIe, SATA and USB to actively transmit data on all the lanes on the electrical board; and at the same time; exerting power gate/ungate noise onto the chip to serve as a natural aggressor from the core logic into the I/O interfaces. As the test packages are designed with merge power rail, the injected and coupling noise becomes maximized.

The results of on-die noise and eye diagram show both packages are passing the electrical stress test with occasional failures on one or two marginal ports; which are later recoverable using a special technique. Both packages not only survived the stress tests but the PCIe, SATA and USB have been showing exceptionally robustness against a pre-defined noise target; and many I/Os which exceeded 60% of its original noise target were able to meet the eye diagram specification. The added robustness is largely attributed by the merged power rails and larger pool of on-die decoupling capacitance (Cdie) sharing, a fact that is not critically considered by many industrialists during the design phase. Alternatively, the method of merger and having a good power grid design becomes essential to ensure the effective Cdie across multiple power rails could be leveraged to a full extend.

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In the laboratories, I have been aided in running the equipment by Chai Ming Dak, a fine technician who kept the probes and boards in good conditions that is always ready for measurement data collection. The smooth running of concurrent I/O and core validation tests is a guidance given by many: Tan Wooi Jou and Ng Yee Chun on PCIe, Catherine Chai and Tan Kheng Huat on SATA, Mazlan Jalaluddin and Beh Yng Yng on USB, Lee Chee Hoo on legacy interfaces, Abdul Rahman Muhammad Kamaruzaman and Beh, Elbert Ein-hao on Display Port and Display Link.

Special thanks to Dominic Chin, Wong Shin Guey and Quah Lay Ching for helping me on software debug whenever the software fails to run the routines required owing to bios setting or false registers setting.

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members whom has lend a helping hand on various data collection; Wong Wai Keat and Kok Chee Kwan for USB, Abdul Hamid Muhammad Dzulkarnaen for PCIe, Selvam Veenaratchagi for SATA. Also, due to persistency of Chin Long, we re-formulated PMC to reverse the failure on USB ports; allowing me to see one step further and realized that the USB noise to eye diagram is frequency spectrum dependent.

Beyond the analogue lab support team, I am also very blessed to be working with the logic team or the System validation (SV) team members Chee Pik Shen, Ng Kok Lim, Ho Wei Hann whom have rendered their support beyond their job scope to help me in verifying the core and logics are functioning per expectation; thereby completing the full cycle of test from analogue to digital lab approval that the chip is not only surviving but is meeting standard industrial test specification.

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APPROVAL SHEET

This dissertation entitled **"HIGH SPEED SERIAL LINK CHARACTERIZATION ON MERGED POWER RAILS PLATFORM CONTROLLER HUB (PCH) PACKAGE"** was prepared by TAN FERN NEE and submitted as partial fulfilment of the requirements for the degree of Master of Engineering Science at Universiti Tunku Abdul Rahman.

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SUBMISSION OF FINAL YEAR PROJECT /DISSERTATION

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I understand that the University will upload softcopy of my dissertation in pdf format into UTAR Institutional Repository, which may be made accessible to UTAR community and public.

Yours truly,

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(Tan Fern Nee)

DECLARATION

I, TAN FERN NEE hereby declare that the dissertation is based on my original work except for quotations and citations which have been duly acknowledge. I also declare that it has not been previously or concurrently submitted for any other degree at UTAR or other institutions.

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(TAN FERN NEE)

Date: ____________________

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LIST OF ABBREVIATIONS

Cdie	On-die capacitance
Cpkg	On-package capacitance
DP	Display Port
DL	Display Link
I/O	Input/ Output
PDN	Power Delivery Network
PCH	Platform Controller Hub
PCIe	PCI-express
Rdie	On-die resistance
Rpkg	On-package resistance
Rgrid	On-die grid resistance
SATA	Serial-ATA
SSO	Simultaneous Switching Output Noise
SSN	Simultaneous Switching Output noise
USB	Universal Serial Bus
Vpp	Peak-to-peak noise
HSSL	High Speed Serial Link
DUT	Device under test
SRAM	Static Read Access Memory
PMC	Power Management Controller
CLB	Compliance load board
ATE	Automated Test Equipment
BGA	Ball grid array

DSC	Die-side capacitance
EC	Edge capacitance
LSC	Land side capacitance
BSC	Back side capacitance
BC	Bulk capacitance
PMOS	P-type metal oxide semiconductor
NMOS	N-type metal oxide semiconductor
VCCS	Voltage control current source
PTH	Plated through hole
PCB	Printed circuit board

CHAPTER ONE

ELECTRICAL CHALLENGES IN HIGH-FREQUENCY INTEGRATED CIRCUIT PACKAGING AND BOARD DESIGN

1.1 Introduction

Intel co-founder Gordon Moore's bold prediction, popularly known as Moore's Law (Moore, 1965), states that the number of transistors in an integrated circuit chip (IC) will double approximately every two years. Intel, uses this golden rule as guiding principle, expanded functions on a chip at lower cost and power by introducing new materials and transistor structures (Anon., 2011). In this article, it is described that the ability to pack more and more transistors into the same area of die size is triggered by the introduction of 3-D Tri-Gate transistor on a 22nm process in 2011, which resulted in smaller geometries transistors; than the 32nm process. The ability to produce 3-D Tri-Gate transistor is in turned supported by a new processor generation in every two years and its massive fab network worldwide.

The more transistors are packed within the IC, the more processing power and memory capacity is achieved. In the early 1970s, Intel's first microprocessor, the 4004 had 2300 transistors to power the Busicom calculator chips (Anon., 2006) (Anon., 2012). In January 29, 2007 Intel revealed breakthrough transistor materials where high-k metal gate was used on hundreds of millions of microscopic 45nm transistors in Intel® Core™ 2 Duo. In May 4, 2011, Intel introduced tri-gate transistor to boost performance

and energy efficiency in a whole range of computers, from servers to desktops, and from laptops to handheld devices (Anon., 2011). The increase in transistor count, on one hand, indicates that more functions and features are built-in on the silicon. On the other hand, it has also indicated that the processing speed and bandwidth has advanced to the next level. As the silicon grows, the metal gate shrink in size, bringing in larger transistors count onto the same silicon area. While the shrinkage of metal gate cause the operating voltage to drop, the current density increases due to the higher density of transistor packed into the same silicon area (Packan, et al., 2009) (Anon., 2010).

Intel® Architecture (Anon., 2009) comprises of 3 components system (Figure 1.1). The two other chipsets which connect and interface with CPU, are the Memory Controller Hub (MCH) and I/O Controller hub (ICH). ICH was Intel South-bridge on motherboards. It has communicated with CPU via Memory controller Hub (MCH), while connected and controlled peripheral devices. Figure 1.2 shows the configuration of an ICH, which acts as the hub that connect between multiple I/O interfaces such as USB2, SATA, PCI Express, high definition Audio Codec, Clocks, SPI Flash, PCI, GPIO and DMI. Amongst these interfaces, USB2, SATA and PCI Express are Giga-hertz (GHz) busses designed to communicate with external chip and peripheral to ensure that the overall computing system is optimized to achieve its fullest processing capability.

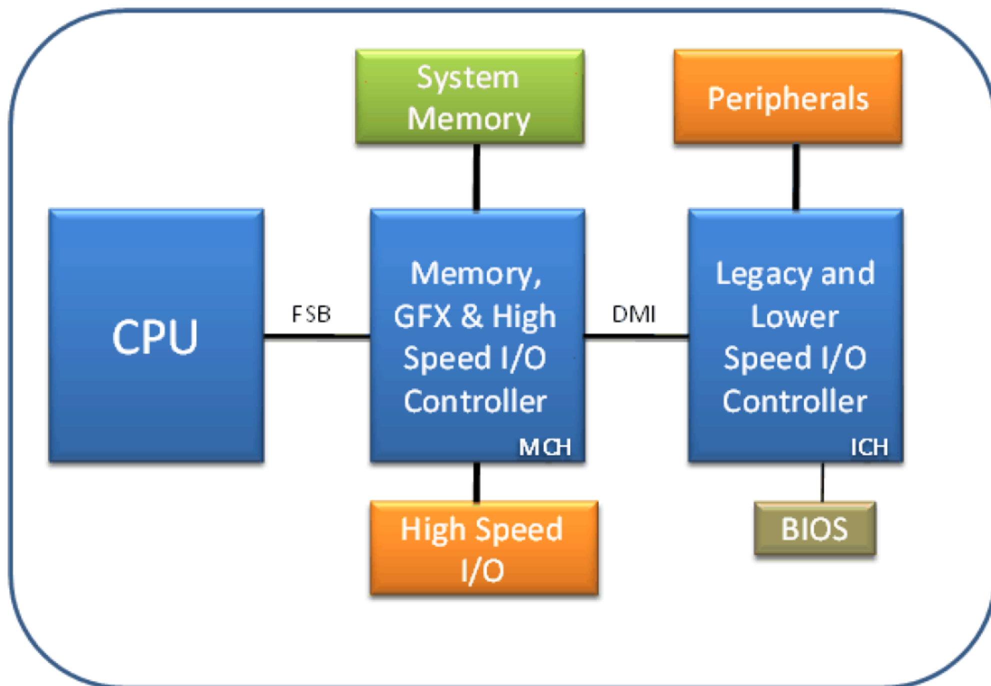


Figure 1.1: Intel® Architecture

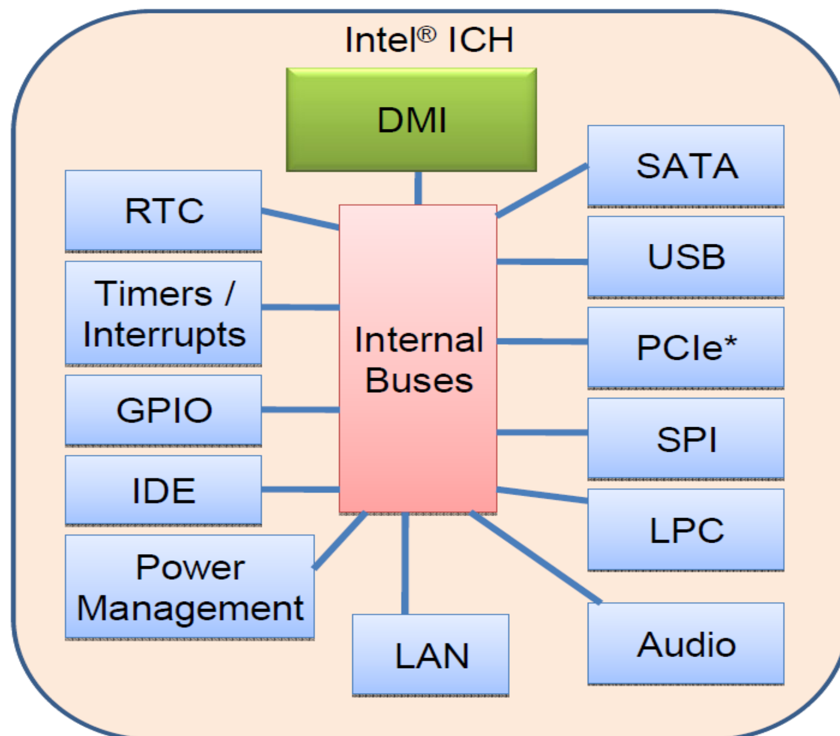


Figure 1.2: Intel® ICH Internals

Beginning 2010, a major computer architecture evolution happened whereby a two-chips system was introduced. Figure 1.3 shows the pre and

post evolution computer architectures. In the new architecture, the MCH is completely gone. The graphics hub and memory hub functionality all moved onto the processor die. The Southbridge/ICH has been renamed as the ‘Platform Controller Hub’ (PCH).

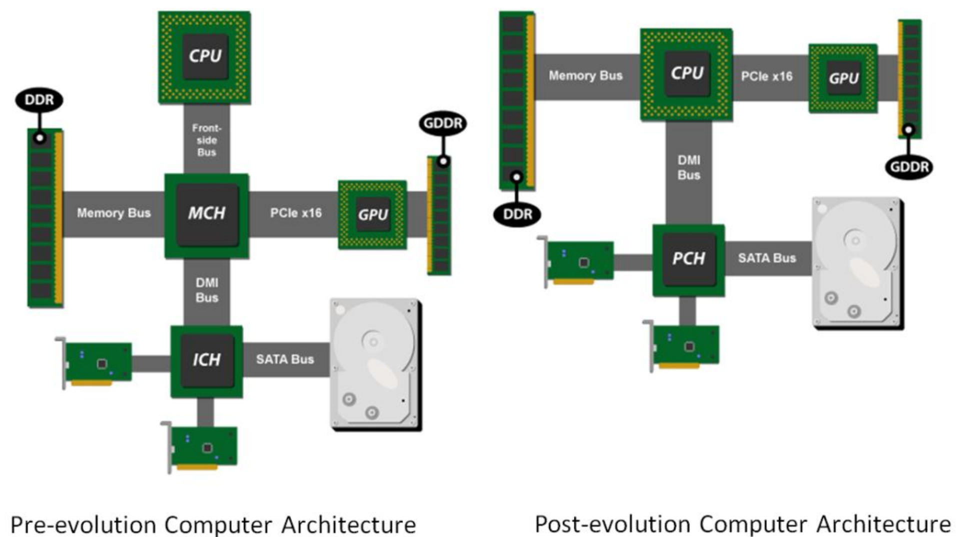


Figure 1.3: Pre and post evolution computer architecture

Today, PCH is unofficially known as the co-processor. It does not only house the Intel ® Management Engine (ME) (Anon., 2012), but also houses many high speed I/O buffers, namely, the Serial-ATA (SATA), PCI-Express (PCI-e) and Universal Serial Bus (USB), Fast Flash, integrated clock, Peripheral Chip interface (PCI), General-purpose I/O (GPIO), Low-Pin-Count (LPC) and many more (Anon., 2012). As these I/O buffers speed advances, the power increases year on year. (Figure 1.4 and 1.5)

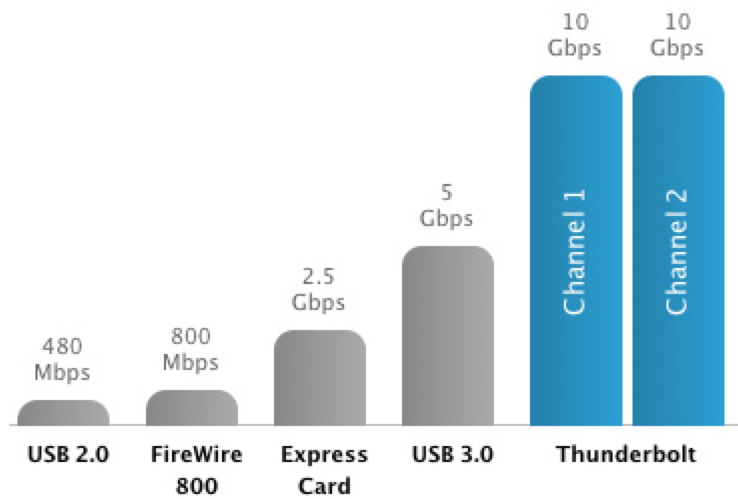


Figure 1.4: High Speed I/O performance advances over years (Anon., 2011)

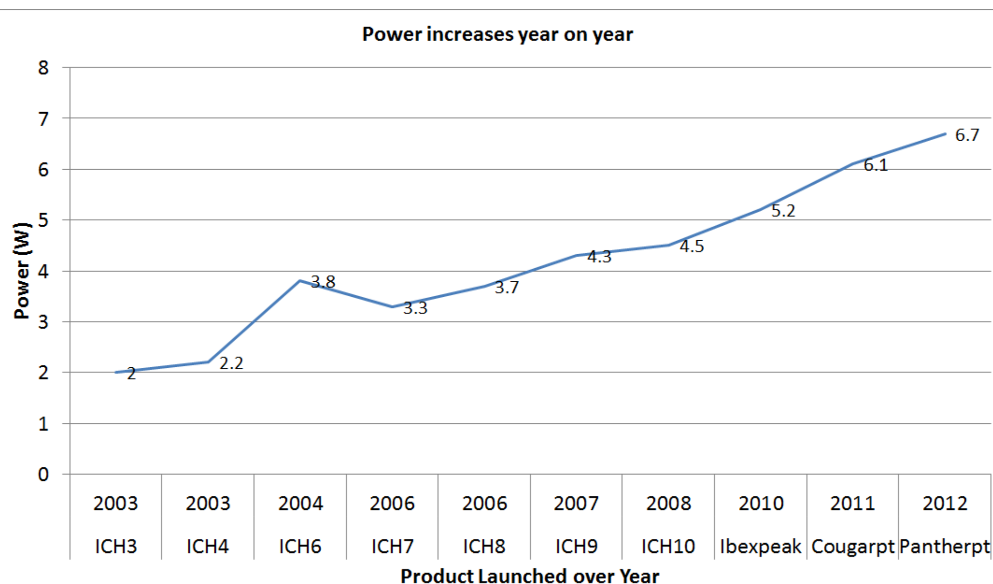


Figure 1.5: Power consumption on silicon increases year by year (Anon., n.d.)

This creates an interesting combination of high speed and low speed I/O buffers being built into one single piece of silicon, mixing a handful of different power domains from as high as 5V, to 3.3V, 1.5V and 1.05V. Depending on the product feature, a total of 15+ different I/O buffers are built-

in to support the massive platform features and technologies (Anon., 2012). In recent development, these features have increased so much that a single silicon can easily contain many small and isolated power rails, in both digital and analogue domains. In this dissertation, there are approximately 25+ different power rails excluding Vss or ground power planes (Anon., 2007). In June 2012, Intel 7 Series Chipset family PCH datasheet published approximately 31 different power rails excluding Vss (Anon., 2012).

1.2 Problem Description

The increase in power rails and pin counts are expected in the coming years with continual increase in features and performance. No doubt, the continual power increase and I/O bus speed increase will demand for more power island or power plane segmentation for proper isolation. This in turn will demand for more power and ground pins on package and board design (Cui, et al., 2003) (Sasaki, et al., 2007).

Meanwhile, with the continuous growth in silicon technology together with the market demand for smaller, lighter, more mobile and lower power computing services (Figure 1.6); the electronic packaging and board design is facing several challenges to keep pace with it. To maintain competitive advantage, the packaging and board size has to shrink in size too (Figure 1.7) (Anon., 2013). Most common practice today is by reducing power pin counts to a minimum, driving packaging technology with higher density and smaller pitch and randomizing ball-map to fit within the smallest package form-factor

possible (Beelen-Hendrikx, 2009), (Furuta, 2010), (Laine, et al., 2006). Some Taiwanese semiconductor corporation venture into 3D stacked high density packages with bump-less interconnect technology in order to achieve more interconnect density within a package (Lin, et al., 2003), while some venture into high density package-on package (POP) and package stacking technology (Dreiza, et al., 2007). These methods described by Lin et al. and Dreiza et al. are highly sophisticated and involve years of engineering development working with vendors to improve the assembly and manufacturing machines. In order to ensure they pass the electrical and mechanical, as well as reliability tests, it will take several months to years of effort to make ends meet.

Figure 1.6: Laptop varies from 1980's to 2010's on sizes and thickness.

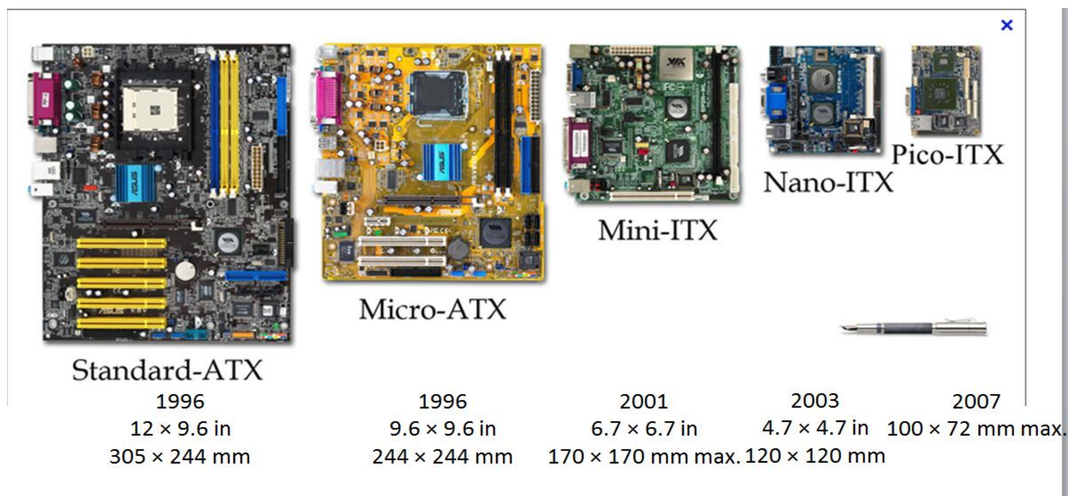


Figure 1.7: Motherboard shrinking in sizes over the years. Same for packages which is soldered on the motherboard have to shrink in proportion.

While shrinking packages and motherboard form-factors is one of the efforts that contribute directly to a smaller and lighter platform design, the electrical performance of these shrink platforms have to be maintained or even improved. As electrical performance is generally characterized as signal integrity and power delivery, the tighter pitch and higher density packages

design have invariably contribute to more crosstalk and coupling noise from one domain into another domain. Many universities and multi-national corporations have invested students and engineers to be specialized in characterizing the high frequency electrical performance of these packages. This is to understand the parasitic inductance and capacitance associating with these high speed/ density interconnect, and how it could affect the ultimate electrical performance of the device (Ahn, et al., 2000), (Li, et al., 2010). In lieu, Signal Integrity and Power integrity modelling and analysis become part of the design disciplines that are associated with the package and platform development.

Signal integrity analysis comes in many dimensions. Some focus on modelling the microscopic level of package/board design such as studying the impedance mismatch at via transition, pitch size, via diameter, via height, excess via stub, antipad size and ground via locations. They believe that these impedance discontinuities will cause signal reflections/ distortions, generate additional jitter and decrease the data eye opening and eventually jeopardizes the reliability of the data (Shen & Tong, 2008). (Chun Sunghoon *et al.*, 2009) proposed a new high-level signal integrity fault model to estimate noise effects based on process variation and interconnect signal transition. Another dimension of signal integrity analysis focuses on parameters for health monitoring of digital electronics. This type of signal integrity analysis looks into parameters associated with signal distortion, power plane integrity and signal transmission quality (jitter) and considered them for prognostics and

health monitoring (PHM) in high-speed digital applications. Utilizing signal integrity parameters in PHM implementation enables the health of system to be monitored from a single point of view at the device, interconnect and transmission level. Utilizing jitter measurements, high-frequency losses are captured, and jitter (with respect to operational functions) is deterministic and bounded, thus reducing the complexity of PHM algorithms and enabling remaining useful life estimation (Torres & Bogatin, 2008). To get complete signal integrity analysis and optimization requires repeated simulation of distributed networks which can be very CPU intensive. Back then, (Zhang & Nakhla, 1994) had presented an efficient approach by using neural network models to describe the signal integrity behaviour of a distributed network. In this work, a continuous neural network model was used to model the nonlinear functions such as signal delay, crosstalk and ground noise; which was then combined with optimization to enhance the performance of high-speed interconnects. Recently, (Kumar, et al., 2006) revisited neural network interconnect model and used it to capture the relationship between the physical and signal integrity characteristics of interconnects to produce the capacitance, characteristic impedance and inductance matrices; while proposes that these interconnects be optimized using Genetic algorithm (GA) using the trained ANN models. All papers described above have covered many different aspects and dimensions of signal integrity analysis, from microscopic level to test, and later to a very sophisticated neural network models and later optimized using Genetic algorithm. Nevertheless, they do not incorporate the power integrity model into the analysis, which could contribute to some extent the overall

electrical performance of the high speed interconnects on package and printed circuit board.

Power integrity design has evolved into an engineering discipline not too long ago. Exactly how much does power integrity matters? The complexity of the subject is illustrated in four textbooks (M. Swaminathan, 2007), (R. Nair, 2010), (V. Pandit, 2010), (Bogatin, 2009), each covering a different dimension of the importance of power integrity design. For a gate-dominated circuit, a 1% drop in the gate voltage results in nearly a 1% drop in frequency. In other words, the Power Delivery Network (PDN) causing the variations on the power supply terminals of the IC results in the slowdown of the chip. Likewise, a voltage rise or bounce across the power supply of the IC, if exceeds the maximum allowable voltage, causes the IC to malfunction (M. Swaminathan, 2007). In the recent work published by (Chen & He, 2007), it is quoted that "Power Integrity becomes increasingly important for the performance of integrated circuits with higher integration density and lower noise margins. Compromised power integrity may lead to logic and timing errors. Nowadays, integrated circuit chips operate at very high frequencies and consume a large amount of power. The number of I/Os is increasing. A large number of I/Os lead to serious simultaneous switching noise (SSN)".

Having realized the increasing importance of power integrity on package and PCB design, many researchers started power integrity analysis to look at the various perspectives in an attempt to catch on and resolve the

potential electrical problems before the product was built. Power integrity analysis too, comes in many different dimensions. (Popovich & Friedman, 2005) described that multiple supply voltages were used in high performance ICs to decrease power consumption. The multi-voltage power delivery system, when interacted with each other, could cause power and signal integrity problems in the overall system. It was recommended that the coupling coefficient which was represented by magnitude of voltage transfer function and parasitic inductance be considered across a wide range of operating frequencies so that the voltage response could be properly controlled. Another dimension of power integrity study was proposed to optimize the power grid in 3D ICs design. A study was done exploring the trade-offs between MIM and traditional CMOS decap, and thus a congestion-aware 3D power supply network optimization algorithm was proposed to optimize this trade-off (Zhou, et al., 2009). (Song, et al., 2008) had explored the design and implementation of using embedded discrete capacitor in multilayer boards to achieve low noise solutions over a wide range of frequency. Careful floor-planning during the integration of full electronic systems on a single chip was proposed by (Chen, et al., 2005) to achieve zero static IR drop violation. These studies from Popovich et al. through Chen et al. were generally done to obtain an optimized power delivery network, which however, did not account for computational time and memory consumption. In the work of (Wang, et al., 2006), proposed a fast approach to accelerate the calculation of the summation associated with large number of higher-order modes. Combining the fast calculation of the cavity models or regularly shaped planer circuits, a

segmentation method and closed-form expressions for the parasitic, an efficient approach was proposed herein to analyse an arbitrary shaped power distribution network. The result was a truncation of many hours for full-wave method to several minutes using the proposed method.

With growing concerns on system level power integrity problems and how it could impact the overall electrical package and PCB performance, it has become more and more popular among the multi-national companies that signal and power integrity combined analysis be carried out. (Choi, et al., 2008) proposed an analysis method which combined signal integrity (SI) and power integrity (PI) analysis by utilizing response decomposition in the time domain with worst case pattern consideration. Meanwhile, (Tripathi, et al., 2010) described how system level signal integrity and power integrity of USB HSLink can be developed by including parameters like board, package, measurement environment which influence the performance of the channel. Parameters variations appearing from manufacturability constraints, material property constraints, design tolerance etc. affecting the serial link performance be optimized using Taguchi statistical techniques and optimized for desired performance. On the other hand, (Rangaswamy & Prathaban, 2006) described the problems of ever decreasing rise times errors creep into signal quality and timing analysis by ignoring the effects of the PDN. In his work, he outlined the necessity and the impact of including power delivery network effects for signal quality and timing analysis to obtain optimal topology, terminations and decoupling solution for motherboard implementation of 533MT/s DDR2

devices. (Schmitt & Hai Lan, 2012) described their work on design and characterization of the power supply system for high speed 1600Mbps DDR3 interface in wire-bond package. The superiority of this journal paper lies in the fact that not many industrialists believe that a wire-bond package could support 1600Mbps transmission rate for DDR3 and with the comprehensive work by Schmitt and Lan, it became a reality.

The articles from Shen et al. through Schmitt et al. have studied using different approaches and methodologies in signal integrity, power integrity, and co-Signal and power integrity analysis, covering from modelling, test, simulation and measurements to improve the package and PCB interconnect design. The ultimate objective is to reduce impedance mismatch, coupling noise, SSN so that jitter is minimize. The perception of decreasing system noise will improve jitter performance become a common belief that must be fulfilled. However, exactly how much noise and at which frequency is never been root-caused. This gives the general perception to fight a never-ending battle in keeping the system noise low.

Conventional Power Delivery Network Design (PDN) aims to achieve +/-5 or 10% Vpp on the DC supply (Mohamood, et al., 2007), or an equivalent of 500mV on a 5V power supply rail. As the HSSL speed continue to increase year on year (Figure 1.4) and the voltage margin and jitter margin at which the HSSL buffer is operating becomes lower as the speed increases (Froelich, 2005), the PDN Vpp target has to be adjusted accordingly. For example, a 1V

power supply rail is looking at 40mV (instead of 100mV or 10% of Vpp) design target for the HSSL PDN design. Using this ac noise target, it then governs the PDN design and limit the jitter and eye diagram from violation. Many high speed design principles developed since early 1990's are still being practiced today (Dr. H. Johnson, 1993). Recent white paper which was published by Intel in 2009, stated that these general high speed design principles such as using ideal ground plane as reference plane ((Venkataramani, 2009), rule 2 on page 10), avoid routing over voids or slots ((Venkataramani, 2009), rule 5 on page 10) and proper isolation of digital power rail from analogue power rail ((Venkataramani, 2009), rule 8 on page 10) should be practiced. Another publication by Intel recommended maintaining good signal to ground ratio was a must on the ball-map and should be abided (Sun, et al., 2012). Besides these common design principles, it becomes increasingly common that SIPI system level simulation is employed to optimize the PDN to reduce coupling and SSN noise to a minimum (Lim & Wong, 2010). In the work published by (Chen & He, 2007), it mentioned that there was overdesign of PDN if impedance metric was used where noise bound was not. They have proven that by improving their algorithm, 3x decoupling capacitor cost could be reduced. In another publication by (Shi, et al., 2007) pointed out that previous works which considered only worst case design would lead to overdesign. The input of both process variation and operation variation such as current model, clock cycles, logic event between ports were amongst the important input parameters that

must be modelled carefully to achieve an optimal power integrity design without causing too much overdesign.

In short, the problem statements of the study are aimed to re-evaluate the validity of these design principles and to what extend it remains valid:

a) Power rails isolation between digital and analogue domain
b) The need to isolate power rail of one from another interfaces
c) The need to keep the power supply rail noise to within +/-5% of the nominal operating voltage (Vcc)
d) A must to isolate core logic from I/O power supplies

1.3 Motivations and Scope of the Study

The contributions of this work are aimed primarily at studying the power supply noise or simultaneous switching noise (SSN) impact on several actively switching High Speed Serial Links (HSSL) when traffics are running concurrently, i.e. using the actual data patterns that are transmitting between transmitter and receivers on an operating motherboard.

It is intended to find the limit of the system break point thru practical implementation and stress validation, using bench data to verify the passing and failing of electrical specification. It is known that many power integrity design approaches described in the work from Chen et al. through Rangaswamy et al.have been focusing on optimization of PDN to achieve the lowest noise target. However, these optimization focus narrowly on a microscopic structure, like via transition impedance mismatch (Shen & Tong,

2008), introduction of capacitor internally to a package (Chen & He, 2007), or an enhanced capacitor structure in the silicon (Popovich & Friedman, 2005), floor-plan design (Song, et al., 2008) or an advance modelling methodology (Chen, et al., 2005). It is close to non-existent that an operating system is used to verify if the design has achieved an optimization or overly achieved the optimization stage; which then leads to PDN over-design. The danger of over-design would not be realized if a system level verification is never been checked or investigated.

Exactly how does the optimization impact the jitter performance and to what extend do they contribute to the final electrical performance is not well associated. (Schmitt & Hai Lan, 2012) did a good correlation study to understand the simulation and measurement correlation and are able to predict accurately how the PDN noise is associated with the jitter performance. However, the focus of the work was limited to one single I/O interface, i.e. DDR, and in a standalone and isolated PDN setup. The modelling methodology would become very complicated if multiple I/O interfaces are operating together. When multiple HSSL operates simultaneously, the iterations that need to be considered became so huge that a modelling or simulation setup could grow so complicated that any existing computing resource will not be able to crunch the data efficiently. More details will be discussed in Chapter 2 later.

The objectives of the study are:

e) To validate the need of power rails isolation between digital and analogue domain

f) To validate the need to isolate power rail of one from another interfaces

g) To validate the need to keep the power supply rail noise to within +/-5% of the nominal operating voltage (Vcc)

h) To validate if it is a must to isolate core logic from I/O power supplies

To ensure the research achieve the above objectives, two additional packages are re-designed and fabricated; each giving a different level of integration, i.e. by merging power rails to a moderate level and having all power rails of common voltage merged together; therefore bypassing the design principles that have been governing the package design for the past 20 years.

The scope of the investigation is extended to introduce huge amount of SSN noise developed on a full-chip level and have it propagated across the entire package to multiple operating I/O interfaces at the same time. The huge amount of SSN noise is the real-time system noise produced by the functional transmit and receive of each of the on-chip I/O interfaces; not any pessimistic model created from simulator or known algorithm (Chun, et al., 2009), (Zhang & Nakhla, 1994), (Kumar, et al., 2006). When multiple HSSL operates in the same eco-system, all these different I/O interfaces not only generates self-noise, but also the cross-coupling noise are there to form the 'largest possible' SSN noise on a system. 'Largest possible' noise is governed to some extend by the operating system, and largely contributed by the test content that is transmitting between these HSSL. Therefore, they are bounded and realistic.

By comparing a few data content that the HSSL typical delivers, it is not difficult to find out what is the realistic worst case SSN noise that a system could generate. However, would the operating SSN be larger than the modelled SSN using a known worst case algorithm, or would the operating SSN noise actually be much smaller than the modelled SSN, remains an unknown now. The importance of realizing the difference between operating SSN and our modelled SSN is very critical in deciding if we have been over-designing/under-designing the PDN for the past years.

All in a nutshell, the goals of this study are to:

1) Analyse the difference between "what is believed to be needed" versus "what is really needed" on existing design principles
2) Understand what effect the PDN have on jitter and eye diagram when the SSN noise exceeded +/-5% target Vpp

Apart from the above goals, the practical design principles for the new generation of form-factor packages/platforms which are targeting to achieve higher density routing would be recommended:

a) Recommend if there is a need to isolate power rails between digital and analogue power supply. If no, what are the criteria to watch out for in determining the optimized PDN design and achieve win-win.
b) Recommend if there is a need to isolate the power rail of one interface from another interface. If no, what is the design approach for PDN optimization

c) Recommend if there is a need to keep the power supply rail noise to within +/-10% of the nominal operating voltage (Vcc). If no, what is the new limit to apply for future product of similar process technology
d) Recommend if there is a must to isolate core logic power supply from I/O power supplies. If no, what is the new guideline or methodology to use for PDN design

1.4 Project Strategy

As the scope of this project is based on the PCH die, the practical usage model is bounded by the maximum data ports available for each particular I/O buffers on the die. The I/O buffers will be exercised according to the standard test-script that is customized by design team which maximize the I/O transaction to its fullest bandwidth possible.

As the objective of the research is to get a general understanding of SSN to jitter impact on the PCH die, the original package which have all the power rails of each I/O interfaces isolated is chosen to be re-designed. The details of the package will be illustrated later in Chapter 3. Two test-packages are designed and fabricated while the original package will be used as the baseline for comparison of data later.

A comparison of 3 packages will be studied:

a) Standalone I/Os PDN (original package)
b) Merged I/Os PDN (test-package 1)

c) Merged I/Os and Core PDN (test-package 2)

After the package redesign is put in place, the following strategy is planned in the laboratory to bring out the maximum SSN possible where the test results of self-induced noise and coupling noise from across the different PCH interfaces could be compared and studied to the fullest extent.

a) A validation environment and methodology that could be used to induce SSO using actual transistors switching activities is developed
b) The intensity of the SSN is increased by introducing more I/O switching activities by increasing the number of participating I/O traffic on the system. When there is no jitter violation happens, core noise would be injected as aggressor to elevate the SSO impact on all the I/O interfaces till failure is observed.
c) In order not to mask off the noise by aggressors, the PDN is stripped down step by step to increase the exposure of PDN to maximum induced noise generated by the switching activities on die; till a failure or jitter violation is observed. This will include removal of package capacitor and board capacitor.
d) If a violation of eye or jitter is observed, the validation data is post-processed using simulation approach to determine whether the high noise is ‘PDN-induced’ or ‘current excitation induced’. This diagnostic step is necessary to help pinpoint the actual root-cause of failure when one arises. This analytical approach is reported in Chapter 4, using both time domain and frequency domain approach.

e) The findings should be concluded with explanation of whether the I/O PDN is over-designed with margin or is easily violated with little margin left. The margin remains should be regarded in noise magnitude at its specific frequency weak-spot. The details will be captured in Chapter 5.

This report consists of 6 Chapters and 4 Appendices. Chapter 1 explains the introduction and background of existing PDN design challenges and constraints. Chapter 2 explains the power delivery modelling background, theory and why it is important. Chapter 3 describes the setup of experiments, test packages, stress programs and test hardware. Chapter 4 focuses on results, analysis using time and frequency domain. Chapter 5 explains the root-cause of failure by furthering experiments that are customized to trace the break-point. Chapter 6 summarise the findings and present the recommendation of new sets of design principles to conclude the study. The appendices contain the details of lab instruments setup, stress program setup, as well as some photographs of the test setup in the lab.

CHAPTER 2

THEORETICAL BACKGROUND AND PRESENT METHODOLOGIES IN DESIGNING A POWER DELIVERY NETWORK

2.1 Introduction

Over the years, the power delivery modelling and analysis are built based on the understanding of these theories and understanding that I/O and Core circuits operate as a transistor. These transistors are the basic building cell that form a full I/O interface. The Power Delivery Network (PDN) is a combination of these transistors model and building blocks such as capacitance, inductance, resistance and AC current which is governed by system level architecture.

In this chapter, the operational theory of transistor and the difference between a transistor that works as an I/O and core will be described. After

that, the translation of these into transistors behaviour into practical modelling and analytical model, and what assumptions that are used to provide the solutions to the packaging and interconnect industry today. It will be followed by the modelling gap with validation and why this research is setup to find the gaps.

From the design perspective, the PDN model is typically bounded by many criteria (rule of thumbs) that are either an assumption which has never been validated; or a word-of-mouth passed down by the earlier generations. How the assumptions are affecting our electrical solutions today and are these design principles really the foundation needed to achieve the best cost and electrical optimized solution, is part of the puzzle for this research study.

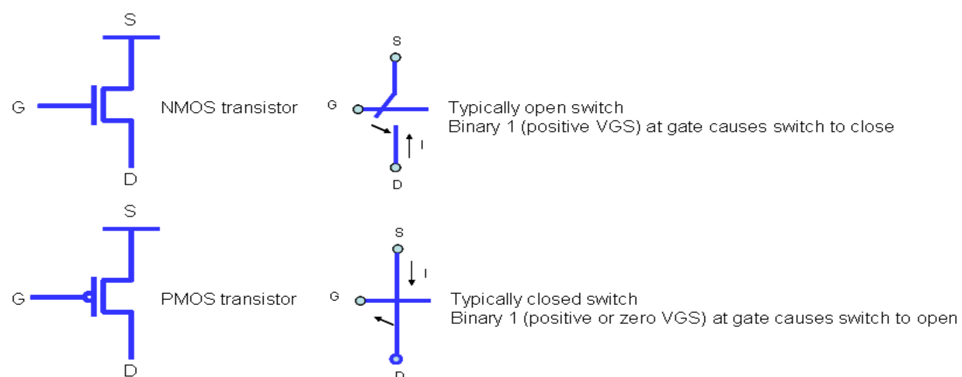
In this chapter, the operational principle of the integrated circuits (IC) is first presented. This is followed by power delivery problems and how SSN will impact the timing and voltage margin on the IC. In order to fully model the SSN and timing impact, the PDN is setup to characterize the amount of SSN noise generated, while the signal integrity model is attached to fully comprehend the flow of AC current. To get the best accuracy, transistor schematic is modelled to serve as functioning High Speed Serial Link (HSSL). Next, an in-depth PDN theoretical analysis in both time and frequency domain will be discussed, to explain how the current and PDN interaction can be translated into a frequency spectrum, and using this information, what type of decoupling capacitance selection can be made. Finally, the limiting factors of

the PDN design will be discussed to point out the flaw and how the gaps should be closed using this research study.

2.2 Theoretical Background

2.2.1 How transistors function?

Integrated circuits (ICs) on PCH are created by transistors. Transistors are switches with multiple terminals, and can be turned on or off using a control bit signal. The turning on or off of the transistor determines how the AC current is flowing through the device. The most commonly used complementary metal oxide semiconductor (CMOS) field effect transistor (MOSFET) is constructed with two types of transistors; namely the NMOS (n-channel) transistor and the PMOS (p-channel) transistor. Both transistors have three-terminal which are called the gate, source and drain. When a voltage is applied between the gate and source, the current through the transistor (from drain to source for NMOS and reversed for PMOS) can be turned on and off. Hence, if a 0 (logic level low) signal is applied at the gate, NMOS is OFF and PMOS is ON; and when a binary 1 (logic level high) is applied at the gate, NMOS is ON and PMOS is OFF. The combination of NMOS and PMOS



forms the basic building blocks of an inverter. This is the simplest building block that explains how current would flow when the transistors turns ON and OFF.

Figure 2.1: NMOS and PMOS transistors can be represented as switches.

Figure 2.1 shows the inverter circuit. The gate connection is named as input node, while the drain connection is named as output node. The output node is connected to the input node of the succeeding stage of transistor circuits. Since the gate of the transistors is used to charge and discharge the input capacitance of the succeeding stage, the succeeding stage transistor can be modelled as a "capacitor". In order to charge the "capacitor" to reach the binary 1 voltage level and discharge to 0 voltage level, the inverter circuit have to be connected to a power supply (shown as Vcc and Vss terminals). In Figure 2.2, a metal interconnection between the two inverters acts as a conductor for the charge. The circuit speed is determined by how quickly a charge can be supplied or removed from the capacitor through the switches. A PDN in a system provides the electrical network in supplying the transistors with sufficient voltage and current for them to function as smoothly as intended.

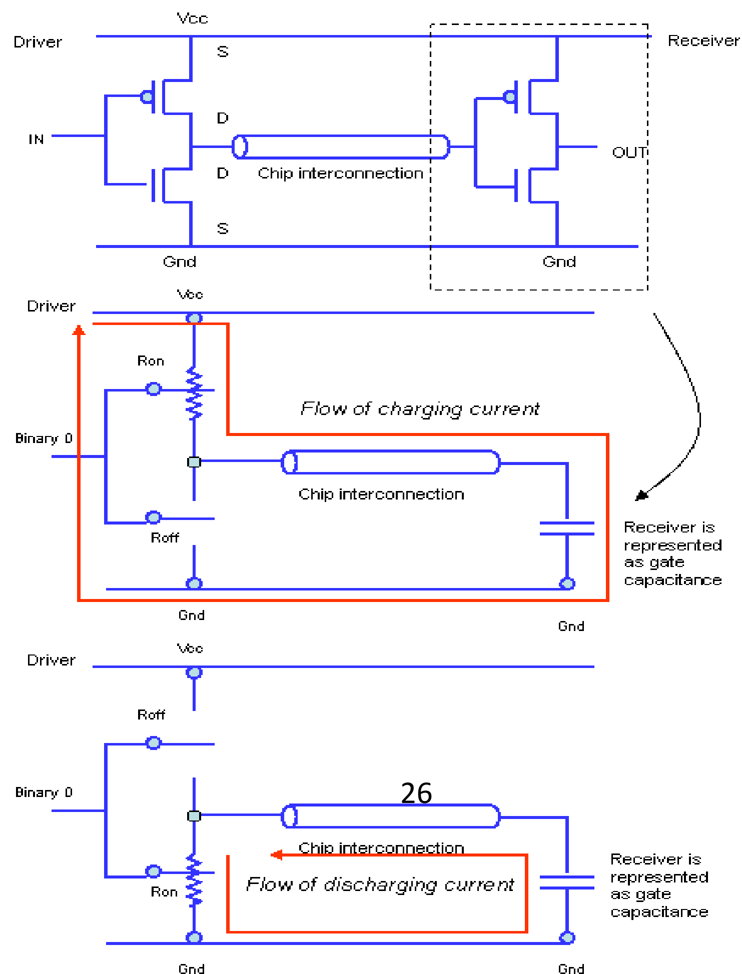


Figure 2.2: Current flow in a CMOS inverter.

A typical driver (inverter) connected to a succeeding receiver (another inverter) is illustrated (Figure 2.2 top). When PMOS is turned on (Figure 2.2 middle), the input capacitance of the receiver is changed to Vcc and the red arrow shows how the current flows. On the other hand, the input capacitance of the receiver is discharged to ground and the red arrow shows how the current flows when NMOS is turned on and PMOS is turned off

2.2.2 Power Delivery Problems

The voltage regulator typically cannot be hooked directly to the Vcc and ground terminals of each pair of these transistors. Therefore, an interconnection (package and motherboard) will be used to establish the connection. These interconnects provide a mechanical support and connectivity from silicon to I/O interfaces transistors as well as power supply, to form the complete electrical path. Unfortunately, these interconnects have resistance and inductance. The current flowing through these interconnects suffers both a DC drop and a transient droop across the Vcc and Vss terminals. This is detrimental to the transistors in the IC. Hence, a carefully designed PDN must be created to minimize the voltage fluctuation across the Vcc and Vss terminals to prevent the following problems:

- Large transient voltage droop across the IC terminals can slow down the transistors from switching states correctly;
- Large transient voltage bounce across the IC terminals can create reliability problems;
- Coupling of transient noise into an adjacent quiet transistor, causing it to incorrectly switch state and
- Timing margin errors due to poor waveforms transmitted at the drivers' output

The voltage fluctuation across the power supply of the silicon is called power supply transient noise, voltage droop or simultaneous switching noise (SSN), since it occurs when many transistors are switching simultaneously.

2.2.3 Definition of a Power Delivery Network (PDN)

The power delivery network (PDN) is defined as the structure that is made up of the system's power and ground structure. A PDN contains the voltage regulator modules (VRMs or sometimes called DC-to-DC converters), die or silicon, package, motherboard and various stages of decoupling. Decoupling capacitors are assigned on motherboard, package, and silicon to act as reservoirs where charge can be stored. The typical decoupling components which are involved in the system are on-die capacitance (Cdie) (Hu, 2009), (Anon., 1997), (Larsson, 1997), on-package die-side capacitance (DSC), edge capacitance (EC) which is placed at edge of package on the motherboard, on-package Land-side capacitance (LSC), back-side capacitance (BSC) which is placed directly opposite the footprint underneath the

motherboard, and bulk capacitance (BC) which are placed close to the voltage regulator module. Occasionally, a filter is built in to prevent external coupling noise onto the silicon. Figure 2.3 shows the block diagram of a typical PDN and the definition of each of the components on the system.

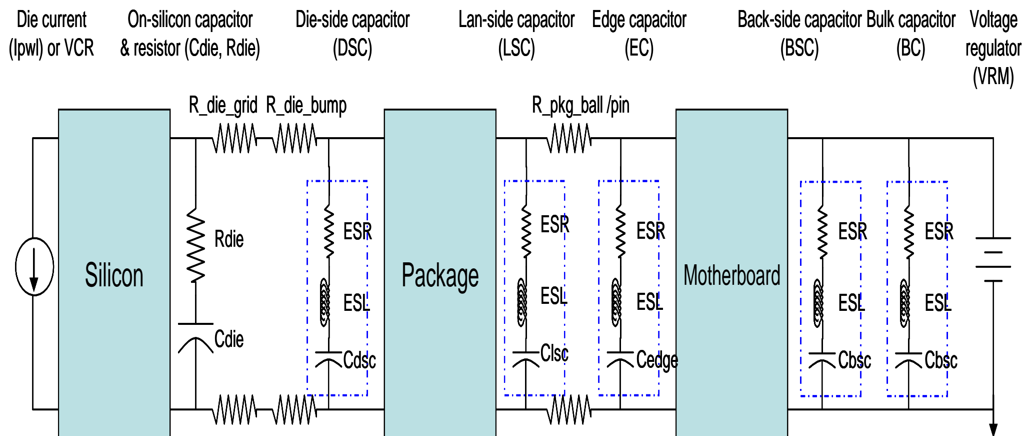


Figure 2.3: Block diagram of a cascaded PDN and its various interconnects involve in the current path.

The PDN can be expressed as a physical model as well as an electrical model. Knowledge of the physical model is needed to create and understand the electrical model. While the electrical model can be represented as a schematic drawing made up of capacitors, resistors, and other components, the physical model is often represented by a CAD database. Figure 2.4 shows the cross-section view of multi-layer package and motherboard, and the various components location on a physical layout of a PDN. Figure 2.5 zooms into the package structure and its nomenclature used to define each vertical and lateral composite of a Flip-chip ball/pin-grid array (BGA)/(PGA) substrate.

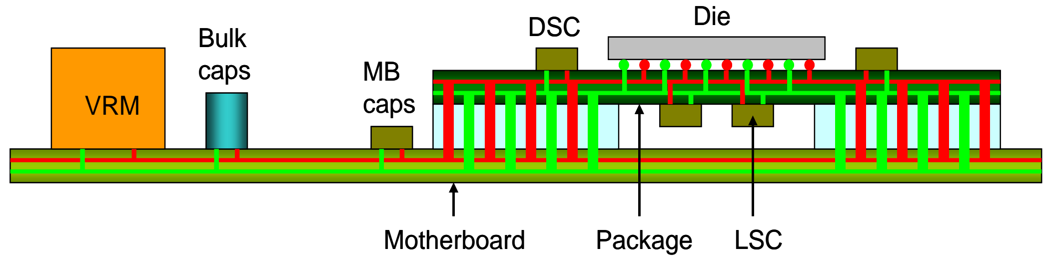


Figure 2.4: The decoupling capacitors location on a physical layout of a package and motherboard, representing the PDN.

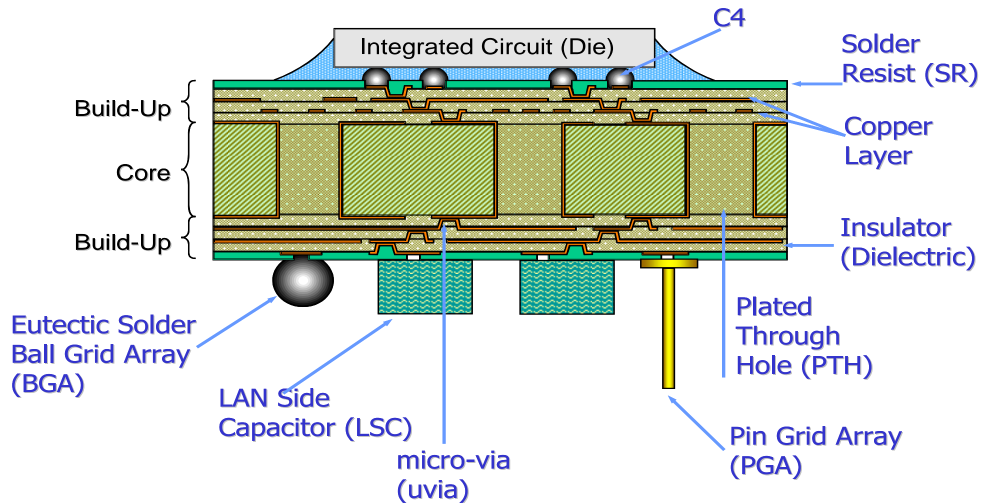


Figure 2.5: The cross sectional view of a 6 layer package and its nomenclatures that decribe the internal structure of a package.

The transient current flowing through an inductor, L causes the voltage drop, V_L, given by

$$V_L = L\frac{dI}{dt} \quad \text{.........(1)}$$

where dI/dt is the rate of change of current in the circuit. The inductor L can be modelled to represent L_{Vcc} or L_{Vss} separately, or as a single L that combines both L_{Vcc} and L_{Vss} depending on how the PDN model is setup. A positive ramping dI/dt through the inductor causes a voltage droop across it, resulting in a reduction in the supply voltage across the transistors terminals.

Similarly, a negative ramping *dI/dt* through the inductor increases the supply voltage across the transistors terminals, resulting in a positive spike.

In any silicon, two kinds of circuits need to be powered: the core and I/O. The core consists of transistors that are contained within the silicon and that communicate with each other within the core logic of the chip. The I/O, meanwhile, has to communicate with other chips externally, and be interconnected through the package and motherboard. Because the I/O circuits exit the silicon and interfaces with other chips, they are isolated from the core circuits using a separate PDN. In the next section, simple relationships of voltage fluctuations on a power supply for both the core and I/O circuits are shown.

2.2.4 Core Circuits

The simplest building block of a core circuit is illustrated in Figure 2.6. The core circuits are a contiguous stages of transistors or flip-flops that is mainly constructed like a chained of driver (2) and receiver circuits (1) respectively; as shown in Figure 2.6 (a). The PMOS is represented by a switch, the on-resistance of the transistor is represented by *R*, and the input capacitance of receiver circuit 1 is represented by *C*. The total inductance of the voltage and ground paths is represented by an inductance *L*.

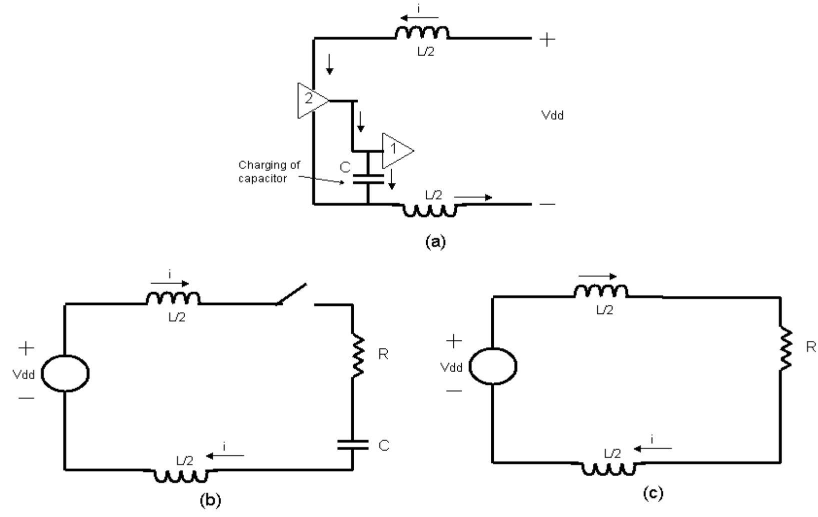


Figure 2.6: (a) Core transistors basic building block (b) Equivalent circuit when t = 0 (c) Equivalent circuit when the L/R time constant << RC delay of the transistor

A good PDN will ensure that sufficient charge is supplied to the switching core circuit with minimum delay. The circuit in Figure 2.6(b) has two time constants: *L*/*R* and *RC*. The delay of the transistor circuit is defined by the *RC* delay while the *L*/*R* is defined as the PDN delay. Since the *L*/*R* time constant should have minimum impact on the *RC* delay of the transistor, it is desired that

$$\frac{L}{R} \ll RC \quad \text{(2)}$$

Under this assumption, the simplified equivalent circuit in Figure 2.6 (c) can be used, where the voltage drop across the inductor can be obtained by solving Eq. (3)

$$v_L(t) = L\frac{di(t)}{dt} \quad \text{(3)}$$

where the current is obtained by solving the differential equation:

$$L\frac{di(t)}{dt} + Ri(t) = v(t) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4)$$

In Eq. (4), v(t) is an equivalent source voltage with rise time t_r (that combines the switch and Vdd) given by

$$v(t) = \begin{cases} \frac{Vdd \times t}{t_r} & 0 \le t \le t_r \\ Vdd & t \ge t_r \end{cases} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (5)$$

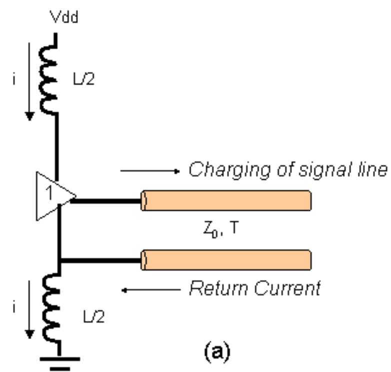
The rise time is dictated by the speed of the switch. The maximum voltage across the inductor occurs at time t = t_r and is given by

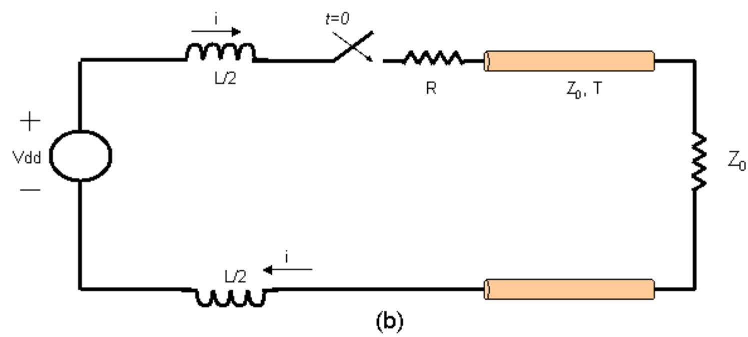
$$v_{L\max} = \Delta v = \frac{L \times Vdd}{Rt_r}(1 - e^{-t_r/(L/R)}) \quad \ldots\ldots\ldots\ldots\ldots (6)$$

2.2.5 I/O Circuits

Unlike Core circuits, I/O circuits drive off-chip interconnects. As frequency increases, the interconnections behave like transmission lines where the delay becomes significant. The PDN used to drive an I/O circuit with transmission lines has a characteristic impedance of Z_0 and delay *T*, is shown in Figure 2.7(a). The termination resistor $R = Z_0$ is placed at the far end of the transmission line, where the inductance *L* represents the PDN loop inductance. As usual, the transistor is represented as a switch with an on-resistance *R*, where *R* is much less than Z_0, to allow for the maximum voltage to be launched on the transmission line, as shown in Figure 2.7(b).

Figure 2.7: (a) I/O circuit basic building block (b)





Equivalent circuit of a switching I/O circuit

When the transistor turns on, the power supply inductance L acts as an open circuit and behaves as a short circuit at time t = infinity. Now, the voltage source and the transistor can be combined and be represented as a pulse with rise time t_r. Since the far end of the transmission line is terminated in the characteristic impedance of the transmission line, there are no reflections. The maximum voltage drop across the inductor occurs at time $t = t_r$ and can be calculated as in the previous section by replacing R with Z_0:

$$V_{L\max} = \Delta v = \frac{L \times Vdd}{Z_0 t_r}(1 - e^{-t_r/(L/Z_0)}) \qquad (7)$$

Based on Eq. (7), a signal line with low Z_0 (highly capacitive) will always results in a larger voltage drop across the inductor, assuming the inductance is fixed. When t_r is much greater than L/Z_0, the maximum voltage drop across the inductor simplifies to

$$\Delta v \approx \frac{L \times Vdd}{Z_0 t_r} \qquad (8)$$

When N parallel transmission lines of characteristics impedance Z_0 are switched simultaneously, it is equivalent to switching a single transmission line of impedance Z_0/N. Hence the voltage drop across the inductor can be obtained by replacing Z_0 by Z_0/N in Eq. (7) and (8).

2.2.6 Delay Due to SSN

The presence of the inductor increases the delay of the I/O circuit. The voltage at the input end of the transmission line for a pulse with rise time t_r can be computed as

$$v(t)=\frac{Z_0\times Vdd}{Lt_r}\left(\frac{L^2}{{Z_0}^2}\left[e^{\frac{-t}{(L/Z_0)}}-1\right]+\frac{L}{Z_0}t\right)\qquad t\le t_r \text{ ………………… (9)}$$

and

$$v(t)=A+B(1-e^{\frac{-t}{(L/Z_0)}})\qquad t\ge t_r \text{ ……………………………….. (10)}$$

where

$$A=Vdd-\left[Vdd-v(t_r)\right]e^{\frac{t_r}{(L/Z_0)}}$$

$$B=\left[Vdd-v(t_r)\right]e^{\frac{t_r}{(L/Z_0)}}$$

and $v(t_r) = v(t=t_r)$ from Eq. (9).

A transistor circuit at the receiver requires a minimum voltage at its input to switch states. Let's assume that the minimum voltage required for this to happen at the driver output V_{chip} (input end of the transmission line) is 0.5 x *Vdd*. Eq. (9) and (10) can be used to calculate the time required to reach 0.5 x *Vdd* and hence represent the delay incurred because of the power supply inductance. Eq. (9) can be used when t_r is greater than L/Z_0, and Eq. (10) can be used when t_r is less than L/Z_0 to calculate a 50% delay. This delay does not include the transmission line delay and is valid for a matched load, as in Figure 2.7.

2.2.7 Timing and voltage margin due to Simultaneous Switching Noise (SSN)

Timing and voltage margin are affected by SSN. SSN as shown in Figure 2.8; can affect voltage margin because power supply noise can corrupt the voltage levels of the signal waveform. SSN increases with a larger number of switching I/O buffers; and at 50% V_{out}, the delay caused by the SSN is known as jitter. For example, consider if a 16-bit wide bus simultaneously switch from bit 0 to 1 (0000 0000 0000 0000 to 1111 1111 1111 1111), the maximum transient current is drawn from the power supply, resulting in maximum noise and thus maximum delay. If only the alternate bits are transitioning between 1 and 0 (0000 0000 0000 0000 to 0101 0101 0101 0101), fewer I/O buffers switch and therefore lower noise is seen compare to earlier case.

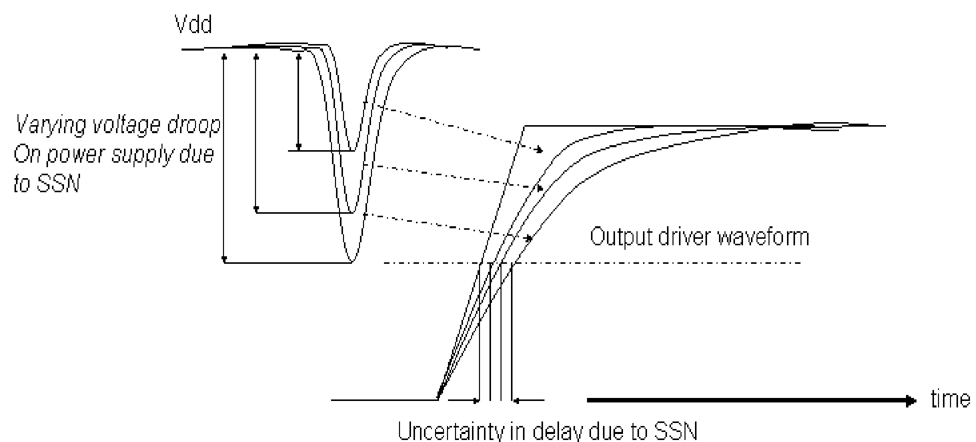


Figure 2.8: Timing margin is affected by SSN.

2.2.8 Power Delivery Network Characterization

There are multiple ways in characterizing a PDN. PDN can be modelled as lumped or distributed LRC components or in frequency domain as impedance (Ohm) versus frequency (Hz). Since a computer system supports multiple frequencies, a PDN is best designed in the frequency domain. A frequency domain analysis will reveal design issues in the form of resonances and the corresponding impedance. The I/O buffer may excite this resonance resulting in a significant voltage drop that can affect performance. Figure 2.9 shows an example of the frequency domain PDN characterization in Z(f) plot. The impedance (Ohm) versus frequency (Hz) plot which highlights the PDN resonance and its corresponding impedance profile across the frequency range allows the designer to interpret all the resonance and anti-resonances in the system that is produced by the various forms of inductances and capacitances in the PDN. By doing a Fast Fourier transform (FFT) of the switching current in the PDN, the designer can evaluate the importance of the anti-resonances in the system and decide if the source (switching circuit) will ever be threaten by these anti-resonances. The response of the PDN to switching circuits can then be viewed in the time domain to evaluate the transient noise voltages generated on the power supply terminals of the IC or between any other nodes in the system.

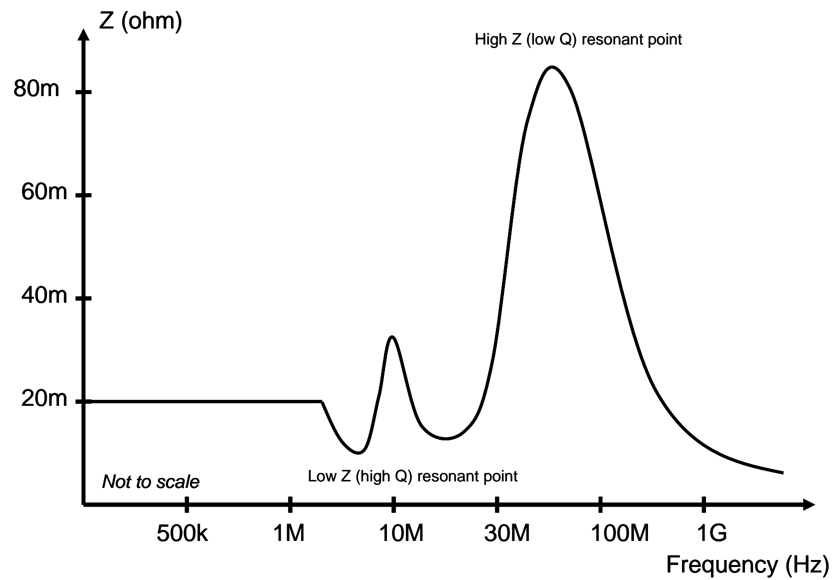


Figure 2.9: Frequency domain PDN characterization in Z(f) plot.

The PDN's behaviour can be modified by changing the components selection: Cdie, package PTH count, DSC quantity, board power plane's width, voltage regulator's location and many more. Each one of these components has a frequency response and together they form the resonance and anti-resonance as shown in Figure 2.10. The peak and valley of the PDN Z(f) is represented by the PDN components, package and Cdie/Rdie. The power supply and board components are typically ranging from 1 kHz-10 MHz, while package response in 10 MHz-100 MHz, and anything beyond is governed by the silicon's Cdie/Rdie.

Understanding the frequency response of the individual PDN components can help the designer focuses on the appropriate part of the electrical model, and hence the physical model. In general, the design goal is to have a low |Z| across the frequency range of interest. The frequency range of interest depends on the switching frequency of the I/O buffers as well as the

rise-time; fast rise-time give rise to higher harmonics. A good understanding of the spectral content created by the buffer model is important.

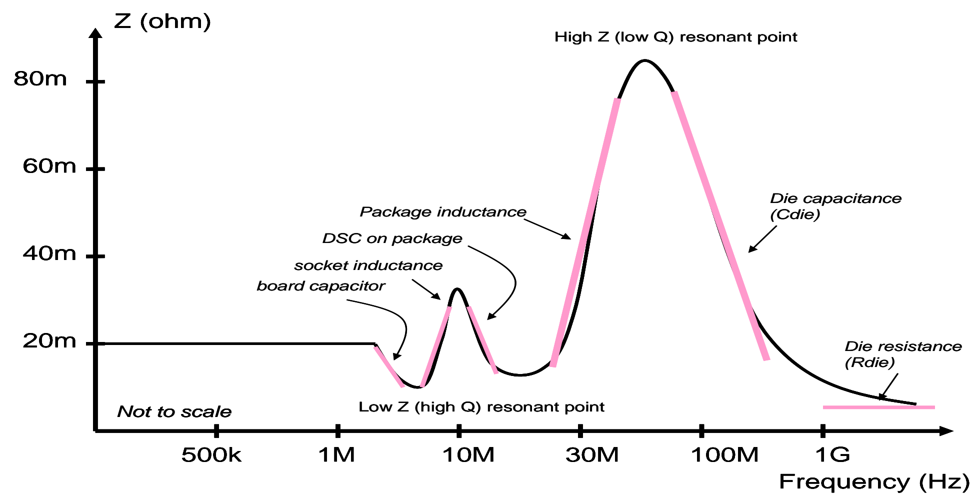


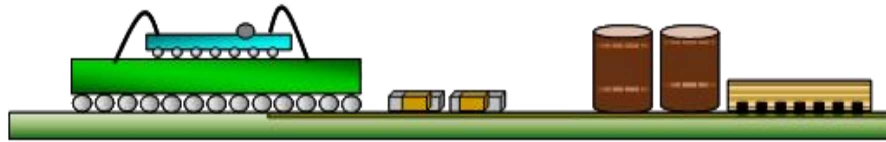
Figure 2.10: The peak and valley of the resonance response of the PDN is represented by the PDN components, package and Cdie/Rdie.

2.3 Power Delivery Network Design process and optimization techniques

A general process that is used for the design of power delivery network for package and printed circuit boards (PCB) is shown in Figure 2.13. The package and board physical layout (CAD database) are translated into electrical model using commercially available electromagnetic simulation tool, for e.g. Ansys SiWave (Anon., 3013) or Sigrity's PowerSI (Anon., 2012). These tools analyse the entire design paths from package to board and voltage regulator using a 2.5D electromagnetic solver; realizing the S-/Y-/Z-parameters of the packages and boards, and the coupling effects between power rails. Electrical issues such as trace and via coupling, power/ground bounce caused by simultaneous switching outputs, and locations of voltage droop hotspots can be identified. These tools support extraction of frequency

dependent network parameter models and enables visualization of complex spatial relationships. To model an accurate PDN current path, it is essential that the forward and return path of the current loop be modelled to its completeness. In many practical designs, the forward current path could be different from the return current path. Especially when vias and voids are introduced on the return path, the voids on the ground planes will lead to a higher inductance than a full complete solid ground plane path. A good PDN model takes into consideration all of the above.

Modelling is a process in translating the physical layout package and board into full-wave electromagnetic model. Figure 2.11 shows how the multiple layer package and board physical layout database is translated into its equivalent electrical model; preserving the locations of the chip, the package and board just like how the actual product is being designed. As such, the coupling coefficient from power to ground, or plated-thru-hole via (PTH), or the coupling from package to board can be modelled. By using multiple ports configuration, the package bump, the package ball, each and every decoupling components can be assigned as an independent port, and thus, conveniently allows one to decide the optimum locations on how a decoupling capacitor should be placed to reduce self-induced noise, SSN and coupling noise. The output from the tool is a black box model. The black box model is a distributed PDN that can be in the format of S, Y or Z parameter.



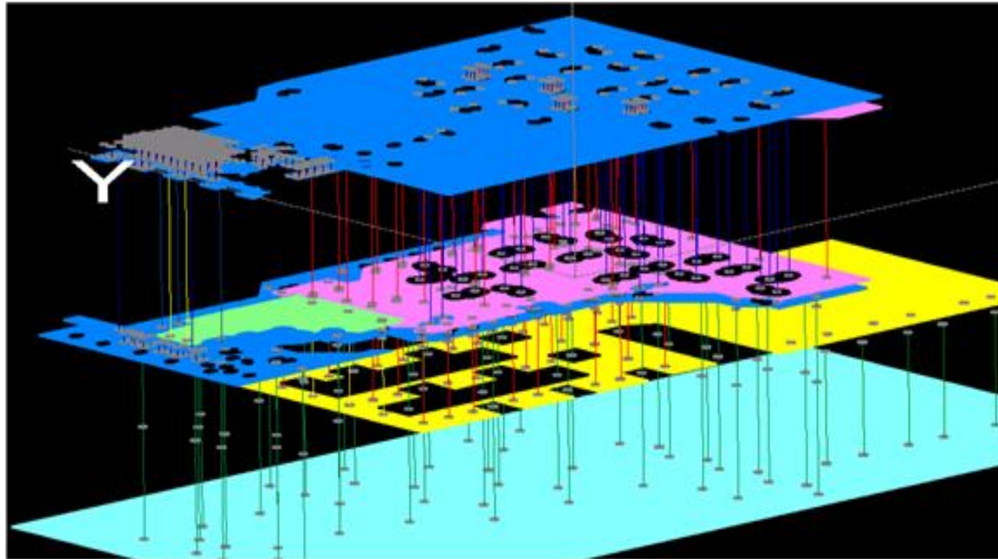


Figure 2.11: The multiple layer package and board layout database is translated into its equivalent electrical model which represents the PDN.

However, these tools have their limitations. To model the basic power delivery path and understanding its detrimental effect to the overall electrical performance, there are many other parameters which are critical in PDN design and yet not incorporated in the package and board territory. For example, the IC power grid network resistance (Rgrid), the piecewise linear (PWL) transient current profile (Icc(t) or Voltage Controlled Current Source (VCCS) (Anon., 1998), the implicit on-die decoupling capacitance such as a MOS capacitance (Hu, 2009), the intrinsic on-die capacitance (Anon., 1997), the on-die resistance (Rdie) (Larsson, 1997) and the discrete decoupling capacitor (Anon., 2012) that are placed on package, motherboard and the power supply. Figure 2.3 illustrates what a basic PDN should look like. The cascaded network is all passive in nature.

When timing and jitter impact of the PDN design becomes a concern, the transistor level I/O buffers are modelled into the PDN as a replacement for Icc(t) or VCCS. The current drawn by the transistors which was formerly represented by Icc(t) is now represented by the actual transistor schematic, whereby data pattern transmitted by the circuit draws the current transients from the power delivery network. These data pattern could excite the package-chip resonance and the impact is directly sent into the circuit to detect the sensitivity of the output drivers to the supply noise. Depending on the sensitivity of the output drivers to the supply noise, especially when multiple drivers are switching simultaneously (SSO), the impact on system margin of the interface could be quantified as either jitter or eye diagram. Figure 2.12 illustrates the transistor spice model which is designed for timing/ jitter and eye diagram impact analysis due to PDN.

To ease the modelling effort, the above process is divided into two stages. First, the basic PDN is designed to allow decoupling components selection and optimization using Icc(t)/VCR. This way, many cases of what-if analysis can be quickly done in optimizing the PDN. The final check-out on timing/jitter/eye diagram is done when the transistors I/O buffers model becomes available. The transmission lines and loads are added to the PDN to form the complete ac current paths. At this stage, an active model is included, thus adding complexity and many analogues IC design considerations. It is

most accurate but time consuming, and it is not easy to debug if there is any miscorrelation due to its complexity.

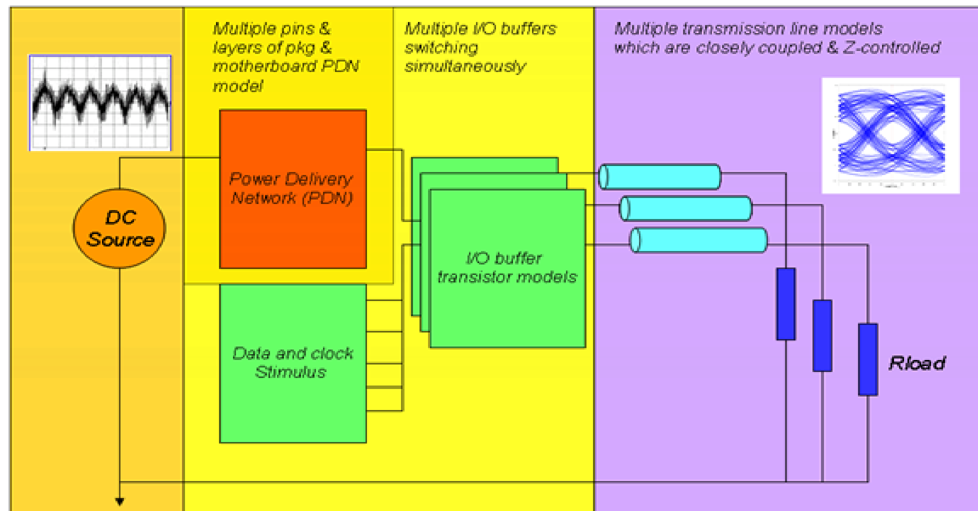


Figure 2.12: Block diagram of a transistor spice model use for timing/jitter/eye diagram impact determination due to SSN.

When all ac noise, jitter and eye diagram specifications are meeting the requirement, the PDN is considered passed and the decoupling solutions will be employed for the final product built. The final stage involves electrical validation in which lab data is collected and verified against the simulation results. Upon completion of validation process, the product is ready to be shipped.

However, if the AC noise becomes too severe that it fails to meet jitter and eye diagram specifications, the PDN has to be re-designed. The simplest option is (1) altering decoupling capacitor selection (2) physical package and motherboard PDN re-design. The latter involves major change of physical design structure, such as layer change, PTH number increment, pin position

placement and return path optimization. These major changes will cause PDN resonance shift, and the entire PDN analysis has to start over (Figure 2.13).

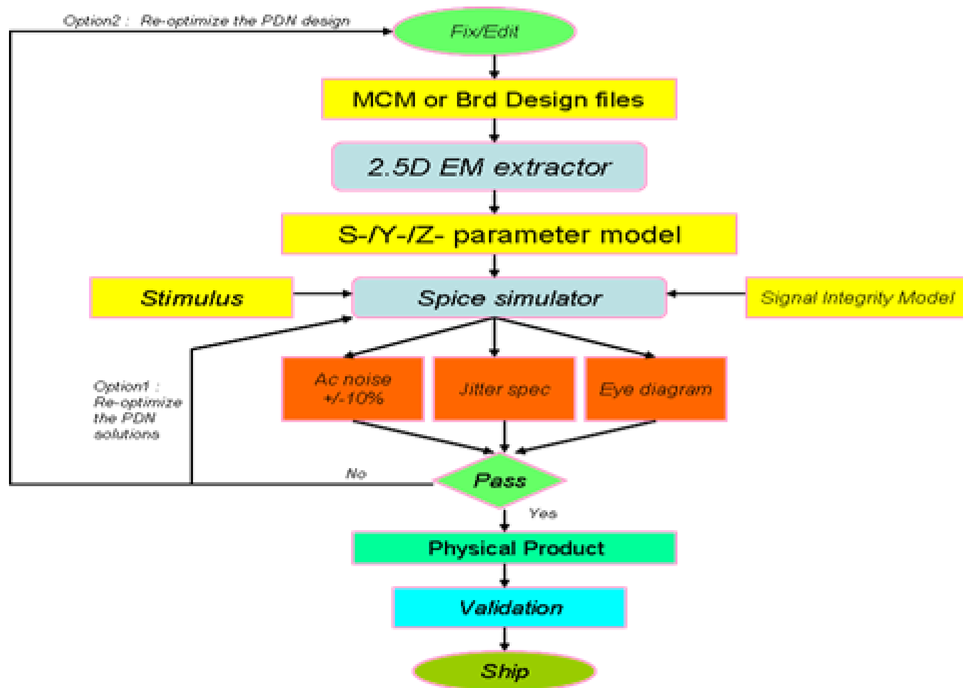


Figure 2.13: A general process that is used for the design of PDN

2.4 How good is PDN modelling today?

To more advanced level, there are many questions remains unanswered like the number of I/O buffers which would be switching simultaneously at each time. In the work of (Schmitt & Hai Lan, 2012), the scenario is narrowed down to when DDR3 is in WRITE mode. As the scope is reasonably bounded within a specific interface family, the critical timing relationships could be defined in DDR3 Specification. In the work of (Zhang, et al., 2004), the timing jitter could be quantified accurately as the scope is bounded by a nine-stage CMOS differential ring oscillator. As such, it is not difficult to assume that HSSL interfaces on PCH such as PCIe, SATA and USB, where its PDN

design is setup for a specific READ or WRITE mode, their timing relationship could be quantified individually according to their respective Specification too. However, quantifying trans-HSSL family timing relationship between PCIe, SATA and USB could be difficult as it has never been defined. Thus, this is posting the first challenge in this research study, whereby quantifying the SSO at the system level when multiple I/O interfaces are operating simultaneously is quite impossible. In other words, a better methodology to quantify this SSO impact is to use a validation setup for eye/jitter study. Very limited or almost no article/journal paper has been found publishing on trans-HSSL SIPI analysis thus far.

Next, these HSSL when put in operation, are highly governed by the core logic, the operating system, and the surrounding devices that these HSSL are interfacing with. The core logic, the operating system and the device interaction with the HSSL, and changes its upstream/downstream transmission is difficult to be predicted. The situation will be even more complicated if some HSSL are transitioning from one power states to another when no active data is detected for an extended time. The opportunity that one of the HSSL be put into idle state from active state, or vice versa will have some substantial impact to the overall PDN design too. This is translated to some ports will wake up (power on) or put to sleep (power off) when other HSSL are actively transmitting. Any of these events would generate a transient on the PDN and cause a droop/ bounce which could be detected by another HSSL which are sharing the same PDN. How much noise to jitter/ eye impact is caused by

these transition on signalling and power state change is best to be characterized using an actual operating platform. Some related research work which was published (Ramaswamy, 2003) and (Shin, et al., 2010) suggested ways of quantifying noise to jitter performance analysis. The work of (Ramaswamy, 2003) quantified the impact of supply noise on the jitter performance of a SERDES macro placed in a large ASIC chip and a core noise generator; whereby the noise generator was specially designed and thus, the noise injected was predictable and bounded. In the work of (Shin, et al., 2010), they have focused on DLL and thus, the scope was relatively bounded and small. The research work by (Chand, et al., 2010) had focused on the analysis of coupling-induced jitter in FPGA transceiver where a large numbers of single-ended I/Os were involved. In the work's finding, it had described how additional jitter was seen at adjacent HSSL when multiple single-ended I/Os (SEIOs) were toggling simultaneously. In this FPGA test-chip, the sensitive clock network supply (VCCA) pin was purposely built one ball away from VCCIO (the supply that supplies to SEIOs). Therefore, it was an aggressor to a victim case study. In both research works from (Ramaswamy, 2003) through (Chand, et al., 2010), the on die noise was stimulated using SSO whereby the toggling of data was deterministic. In this research study, besides stimulating deterministic SSO of multiple I/Os HSSL, and introduction of core noise as aggressor, the un-deterministic noise such as those caused by signalling and power state change will be included.

An accurate PDN model is described as a PDN that is able to predict the actual SSO performance and matches with the timing impact. The PDN is essential in representing the full current loop model; starting from the voltage regulator located on the board, through the package and silicon that houses the integrated circuit. Very often, the input parameters are very crucial in determining how accurate that the PDN would be. As mentioned in Figure 2.13, the PDN modelling involves a series of process, starting from translating the physical package and board layout into the electrical model. With the advancement of CAD design techniques and computing resources, it is no longer a difficult job to predict the full path impedance to within 90%-98% accuracy. Next, getting the right piece-wise-linear or Icc(t) profile is considered challenging, especially when multiple process corners such as voltage setting (high, nominal, low) and temperature setting (high, nominal, low) each plays a different role in influencing the CMOS characteristics, and thus changes the transient current profile behaviour. Much of these modelling depends on the combinations of the Process, Voltage and Temperature (PVT) setting, the designer must be experienced enough to decide which corner cases should be used for the PDN design. For simplicity, the chip designer will derive a piece-wise-linear "Icc(t)" which represents the worst case scenario for PD analysis. As quoted by (Ketkar & Chiprout, 2009), "Alternatively, designs also employs piece-wise linear waveforms which are estimated by chip designers….however suffer from main drawback: they do not result in actual instruction streams. This limits their use in power delivery design and verification". In addition, the worst case Icc(t) model given will lead to one

decoupling solution to cater for all designs as this decoupling solution would be able to comprehend all the different permutated transients that would likely to occur on a system. As such, using the very pessimistic stimuli setup leads to a very optimistic solution PDN design. For example, a high temperature, fast skew, and low voltage is chosen to generate the current stimuli (Icc(t)) in order to represent the most pessimistic model for use in PDN design. Inevitably, more decoupling capacitance; be it on silicon, or on package or on board are added to provide a comfortable solution for this worst case design. Unfortunately, the selected worst case corner, typically only represent 5-10% of the total silicon volume manufactured.

Other possible aspects which contribute to the PDN overdesign are the cumulative effect of the design chain, each trying to achieve their best design solutions. The IC design is a process that involves floor-planning, circuit design, logic design and many more. Each of these design development performs to the task and ensure that they would deliver a piece of healthy silicon before passing it on to the subsequent engineering discipline. Occasionally, it is not difficult to realize that every team uses a worst case assumption in their design, and thus leaving some guard-band in each discipline. When the design moves downstream, more and more guard-band are added and eventually, these cumulative design margin becomes so substantial that it provides the silicon extra performance without anyone realizing it. On the other hand, it is also possible that a reverse in electrical margin could happen. That is possible when the front-end silicon design team

does not do a good job in preserving their needed performance target; they could be intruding into the downstream performance envelope, and thus, taking away valuable design margins from the subsequent engineering discipline. If this happens, it propagates as one of the disadvantage of PDN design, where the margin remains so small, that many times the design target given to meet the noise specification, is limited to 20-30 mV of the nominal operating voltage.

To summarize, the problem that many packaging and board industries are seeing today is to keep pace with the exponentially increase in features and power pins while struggling to stay afloat by reducing package size and manufacturing cost. The electrical behaviour of the packaging and board interconnect performance is able to be modelled using advance 3D electromagnetic modelling tools, while helping to achieve an optimized solution space. However, using only peak-to-peak or root-mean-square (rms) voltage as design targets is no longer sufficient in PDN design (Li & Wilstrup, 2003). As the rms keeps fading in magnitude, as the data rates increases >Gbps, jitter magnitude and signal amplitude noise must decrease to maintain the same bit error rate (BER) (Ou, et al., 2004). Eventually this tiny margin will expire, and continuous practising of the existing design principles today will be difficult to sustain in the near future.

Therefore, it is essential that this research work is conducted to help to decipher how the actual system behaves before it is decided that if the system

performance has come to a limit. The research finding may or may not answer all the doubts above; however, it is one of the most direct approach to help draw the line between pass or fail and the ultimate design rules of truth.

CHAPTER 3

RESEARCH PLAN, METHODOLOGY AND STRATEGY

3.1 Introduction

This chapter aims to discuss the research plan, methodology and strategy of setting up the system to examine the research objectives (Section1.3) and quantify the gap of modelling via validation approach as outline in Section 2.4. The content in this chapter is broken into 3 major sections; namely the research plan, the methodology and the strategy involved when any unexpected events shows. The objectives of this chapter is to give an overview of what is planned to be done (Section 3.2) to investigate SSO impact on jitter/eye when multiple HSSL are operating on an isolated, semi-merged and fully merged packages, and how each of the different PDN design will influence the jitter and eye. In order to enhance the coupling noise from one HSSL interface to another, the details on how these test packages are designed (Section 3.3) to promote the coupling noise is outlined in full detail. While package design is one key driver that drives the SSO increment, Cdie measurement method (Section 3.4) and the test setup to concurrently excite multiple HSSL to toggle simultaneously (Section 3.5) are methodologies that needs to be looked closely into. Besides the concurrent stress tests methodology, the step by step approach in handling the test software and oscilloscope setting for eye diagram measurement, as well as the eye diagram plotting tool will be described in detail. After this, on-die noise measurements method will be revealed (Section 3.6) to give an overview how SSO is

measured. If in case the above plans are proven insufficient to bring failure to any of these HSSL interfaces, alternative strategies are suggested to overcome the unexpected event. Design of Experiment for Signal Integrity Power Integrity (SIPI) Research Study which suggests ways to increase the SSO intensity by introducing hand scripted core noise into the HSSL and on-package capacitor removal and Strategy for comprehending the diagnostic of failure event is added (Section 3.7). Next, three strategies will be discussed to put forward possible suggestions that help root-cause any failure in the event that SSO becomes overwhelming and a reverse margining is one of the approaches necessary to find and mark the limit. Subsequent approaches involve reconstruction of current profile using de-convolution technique and a detail examination of PDN resonance when power gate/ungate happens.

3.2 Research Plan

The research plan has 4 major steps:

1) Design and fabrication of special test packages that maximizes the coupling noise

   Two test packages are specially designed to enhance coupling noise from HSSL. Probe pads are built on these test packages to provide access point to on-die noise measurement. Section 3.3 outlines the design of these test packages compare with its baseline.

2) Measurement of On-die capacitance (Cdie)

   As the test packages PDN are merged, while the silicon design remains unchanged; the PDN behaviour is changed due to the amount of Cdie

that is now shared across a common PDN has changed. In order to have a good understanding on how SSO magnitude and PDN resonance would vary with the Cdie variation, it is important that the On-die capacitance be measured prior to any on-die noise measurement is measured. The Cdie has a direct impact to changing the SSO magnitude and frequency content of the SSO. Section 3.4 outlines the detail on Cdie measurement setup and how S-parameter is translated into Cdie parasitic

3) Development of Concurrent stress tests validation approach

Concurrent stress tests validation approach is developed to promote highest possible amount of SSO on the PDN system, using a handful of test software running simultaneously on a fully functional board. The concurrent stress tests should involve the maximum number of lanes possible, while the jitter/eye is measured at the receiver. The measurement would be complaint to the validation specification: such as “250 UI” using cable length of 1m, etc. [Appendix B and C]. The design of test sequence is also important, such that self-noise will first be measured, and followed by coupling noise. The SSO intensity is designed in a way that it will starts from low to high. The HSSL of interest will first be toggled, follow by additional lanes from neighbouring HSSL, and then all HSSL that are presence on the chip. The SSO magnitude will be an increment from low to high, such that the jitter impact could be monitored in incremental steps. Further detail to be discussed in Section 3.5.

4) Measurement of On-die noise and jitter/eye

While the concurrent tests are running, jitter and eye for each HSSL which are toggling simultaneously is measured and captured, the peak-to peak SSO is measured on the package probe pad. As the peak-to-peak noise (mV) is the PDN design target while the jitter/eye is compliant specification; both measurement parameters are equally important for characterization. In the event that both jitter and eye passes the compliant standard, and the magnitude of SSO is contained within the peak-to-peak noise target, a “passed” is graded. Otherwise, when either one of the design target or specification is violated, the SSO impact will be considered a violation and thus, a “failed” will be graded. The root-cause of the violation will be investigated in length. In the event that any of the measurements does not show up as expected, more investigations will also be launched to understand the root-caused of each before proceeding to the next level of research. Section 3.6 gives the in-depth details on this study.

3.3 Design and fabrication of special test packages that maximizes the coupling noise

The research project begins with the design and fabrication of three packages, where two are test packages, and one package retain the original PDN design to serve as a baseline for benchmarking purpose. These packages are identified using the following package names:

1) Lucerne
2) Jasper
3) Milford Sound

Lucerne is the first package which preserves the original design that has individual power rails isolated as it is routed on an actual product. It serves as a baseline for performance benchmark required for Jasper and Milford Sound.

Jasper is the first test package that merges I/O and I/O as one power rail, and core to core as one power rail. It is a simple merger where most mergers are considered low risk and with little electrical impact.

Milford Sound is the second test package that merges I/O and core as one power rail. This is the most aggressive merger that binds all the common voltage rails as one. It combines the core power rail to the I/O power rails as one, stretching the risk of SSO contamination beyond Jasper. Therefore, Milford Sound has all the merged rails implemented on Jasper, but Jasper will not have all the mergers that are implemented on Milford Sound. In short, if Milford Sound is able to pass the peak-to-peak and jitter/eye specification under the aggression of the concurrent tests, needless to say, Jasper should be

able to survive without problem. Nevertheless, nothing is concrete at the moment until the validation data becomes available. As these 2 test package mergers are aggressive and have violated most of the high speed design principles (Dr. H. Johnson, 1993) and (Venkataramani, 2009), they are considered high risk with little confidence to pass. Therefore, it would not be a surprise if the motherboard system could not be booted at all, or if it is booted, it may be seeing lots of intermittent errors.

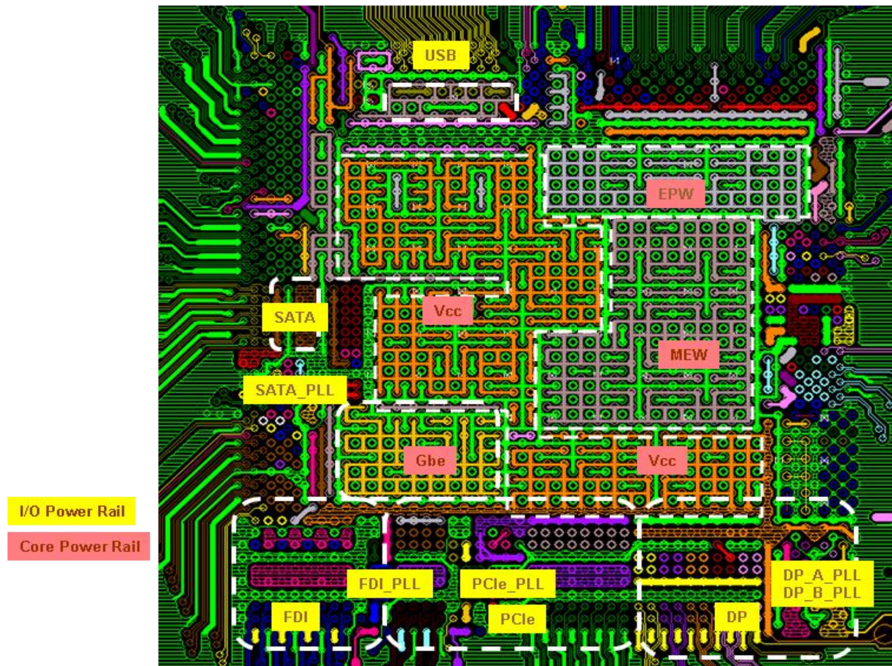
Figure 3.1 gives a bird eye view of the three packages that will be used in the research study. Each of the power rails is identified using a different colour and is labelled either using their interfaces name. In general, it is also identified as I/O power rail v.s. core power rail. All the I/O power rails are labelled in yellow boxes, and core power rails in red boxes. The difference between them is I/O are sensitive to SSO noise and has very tight peak-to-peak noise target, for e.g. <80 mV - <40 mV. While core power rails are less sensitive and could withstand a larger peak-to-peak noise, for e.g. 200 mV. Amongst the I/O power rails, the digital PLLs and analogue PLLs are the DC power rails, which are specially designed to be standalone on Lucerne. These power rails are especially sensitive to jitter and have strict requirement to be isolated according to high speed design principles. In Jasper, these PLLs rails are merged with their I/O families (first level of risk) and in Milford Sound, these PLLs rails do not only merges with its own I/O families, but with adjacent I/O families as well as core logic (maximum risk level). In order to

provide detail merger plan, the power rails which are merged will be listed in tables form, comparing to the baseline design on Lucerne.

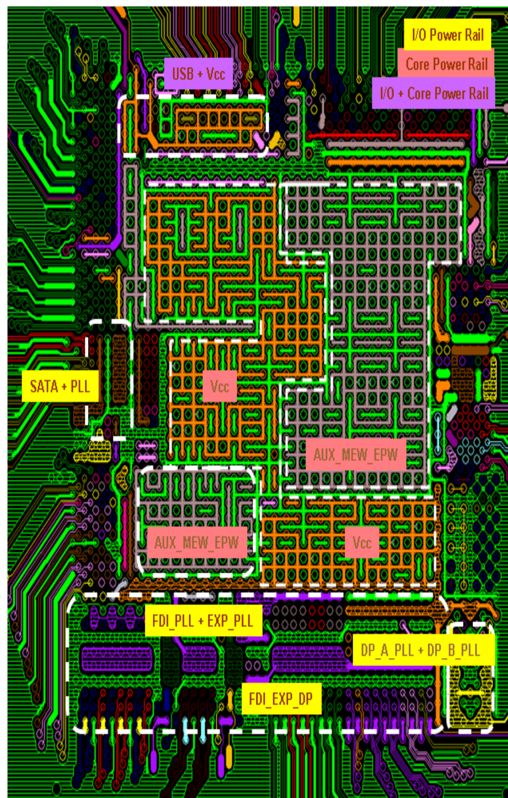
In Figure 3.1, it is easy to note that there are a lot of different colours identifying the different power rails, but it is not easy to quantify exactly how many power rails are there in Lucerne. The objective of the figure is just to provide a high level overview, and with a glance, it is easy to note that comparing Lucerne and Milford Sound, Milford Sound has one colour (orange) and this represents that most power rails which are originally standalone are merged under one big PDN. Note that now a purple label has appeared, which signifies that the I/O and core power rails are merged.

All in all, Jasper is a moderately merged power rails package to serve as a control package, in case Milford Sound sees problem to boot. By comparing the colour coding in these three packages, the least colour variant it has, means it has less power island on the package. Therefore, allowing a bigger PDN power plane to be designed thus increases the number of platted – through-hole vias (PTHs) and ball grid array (BGA) to support the merged PDN. The merger simplifies the package design but it also encourages sharing of decoupling capacitors that is placed on package and on-silicon.

Lucerne Package Design: Standalone IO, PLL and Core Power supplies



Jasper Package Design: I/O and PLL merged & Partial Core merged



Milford Sound Package Design: All Core and All I/O Merged

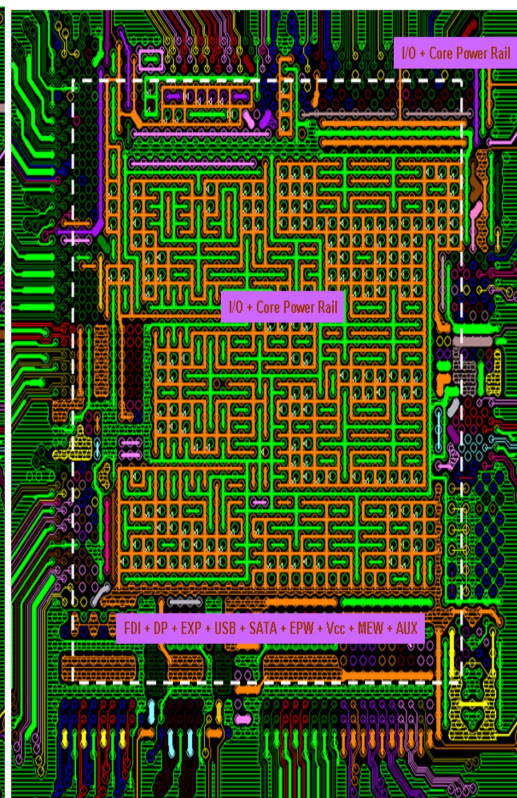


Figure 3.1: An overview of 3 different package test vehicles: Lucerne (top), Jasper (lower left) and Milford Sound (lower right). (Courtesy of Intel Microelectronics Sdn. Bhd.)

The following merger cases provide a zoom in view of the power rails selected for merger on Jasper and Milford Sound respectively.

Merger Case 1: Analogue supply channel A and B

Test packages on which this is implemented:

Lucerne ☐ Jasper ☒ Milford Sound ☐

Table 3.1: Merger of analogue PLLs of the Display Port

Cases	Before Merger	After Merger	Comments
Merger Case 1	Vcca_A_dpl	Vcca_dpl	Merger of Analogue PLL and Analogue PLL
	Vcca_B_dpl		of the same IO

The objective of merging display port channel A and B analogue PLLs is to find out if this will cause jitter/eye violation. Not so much on peak-to-peak noise as they are very quiet rails which consumes mostly DC current. These two analogue supplies are usually routed as two separated power rails. The before and after merged designs are shown in Figure 3.2, from 2 colours (red and yellow) into a single yellow power rail and is renamed as Vcca_dpl. The implementation of merger happens on Jasper, but not on Lucerne. Therefore, a comparison either between Jasper against Lucerne will be able to explain if this merger is a threat or a prospect.

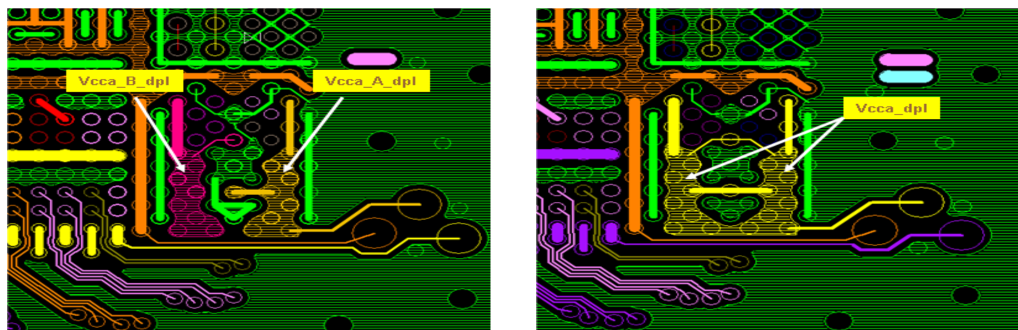


Figure 3.2: Display Port Analogue PLLs before merge (left) and after merge (right).

Merger Case 2: Merger of digital I/O, Analogue I/O, Digital PLL and Analogue PLL power rails within the same I/O family

Test packages on which this is implemented:

Lucerne ☐ Jasper ☒ Milford Sound ☐

Table 3.2: Merger of digital and analogue I/O, digital PLL and analogue PLL of SATA I/O.

Cases	Before Merger	After Merger	Comments
Merger Case 2	VccARX	Vccsata	Merger of Digital IO, Analogue IO,
	VccATX		Digital PLL and Analogue PLL of the same IO
	Vccsata		
	Vccdpll		
	Vcc_satapll		

The objective of merging the digital and analogue PLLs together with the I/O power rails on SATA is to understand if the PLLs would be affected by SSO coupled from SATA main supply. In case 1, only the analogues PLLs are merged. Now, both digital and analogue PLL are merged with the I/O supply. Typically, high speed design principle (HSDP) advises strongly against mixing analogue and digital power rails as one (Venkataramani, 2009).

The before and after merged designs are shown in Figure 3.3, from 3 colours (red, light blue and yellow) into a single yellow power rail and is renamed as Vcc_sata. The implementation of merger happens on Jasper, but not on Lucerne. Therefore, a comparison either between Jasper and Lucerne will be able to explain if this merger is a threat or a prospect.

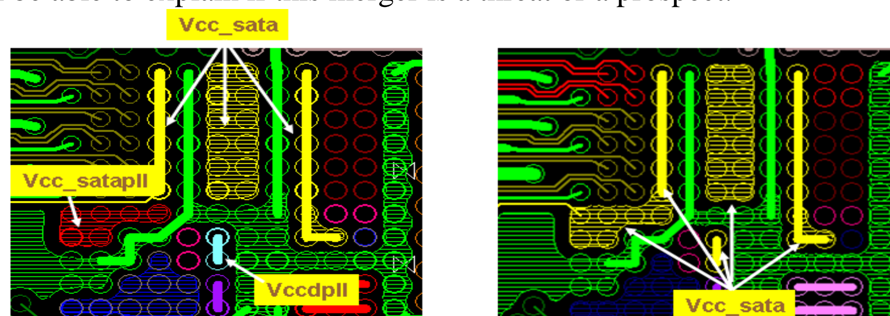


Figure 3.3: SATA supply, digital and analogue PLLs power rails before merge (left) and after merge (right)

Merger Case 3: Merger of digital PLL and digital PLL and analogue PLL and analogue PLL of 2 different I/O families.

Test packages on which this is implemented:

Lucerne ☐ Jasper ☒ Milford Sound ☐

Table 3.3: Merger of both digital PLL and analogue PLL of Display Link and PCIe.

Cases	Before Merger	After Merger	Comments
Merger Case 3	Vccdpll_fdi	Vccapll_exp	Merger of digital PLL and Analogue PLL
	Vcc_dpll_exp		of two different IO families
	Vccapll_fdi		
	Vccapll_exp		

The objective of merging digital and analogue PLLs of Display Link and PCIe is to understand if the PLLs would be affected by SSO coupled from its neighbour. Case 2 merges digital and analogue PLL within its own I/O family. While in this case, a second family of PLLs supplies are added to the merger. Now, there are two digital and two analogue PLLs supplies merged as one power rail, and is renamed as Vccapll_exp. (Figure 3.4)

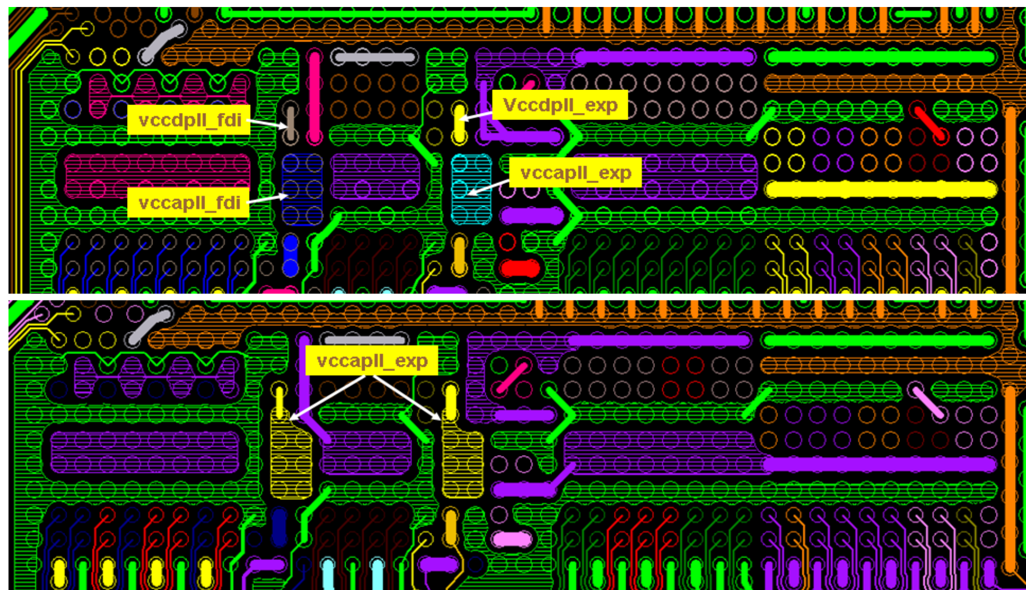


Figure 3.4: Four digital and analogue PLLs of Display Link and PCIe power rails before merge (top) and after merge (bottom).

Merger Case 4: Merger of I/O and I/O power rails

Test packages on which this is implemented:

Lucerne ☐ Jasper ☒ Milford Sound ☐

Table 3.4: Merger of I/O and I/O power rails: PCIe, Display port and Display link.

Cases	Before Merger	After Merger	Comments
Merger Case 4	Vcc_exp	Vccexp	Merger of IO and IO families
	Vcc_dp		
	Vcc_fdi		

The objective of merging Display Link, Display Port and PCIe to a single power supply is to understand if any of these HSSLs would be affected by SSO coupled from its neighbour. This merger on Jasper excluded the digital and analogue PLLs but the merger on Milford Sound includes the PLLs. On Jasper, it is renamed as Vccapll_exp after the merger. (Figure 3.4)

It is interesting to note that these three I/Os are operating at almost the same frequencies and any coupling noise from each other could be a threat. If it turns out to be a prospect, the decoupling solution can be leveraged easily as any decoupling capacitor added will be shared across the three I/O families.

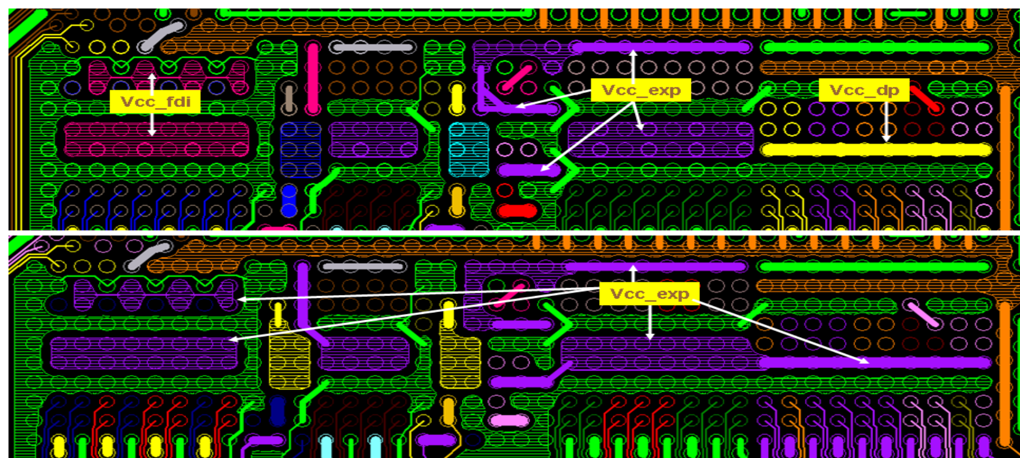


Figure 3.5: Display Link, Display Port and PCIe power rails before merge (top) and after merge (bottom).

Merger Case 5: Combination of I/O and Core power rails

Test packages on which this is implemented:

Lucerne ☐ Jasper ☒ Milford Sound ☐

Table 3.5: The merger of I/O and Core power rail: USB and Core.

Cases	Before Merger	After Merger	Comments
Merger Case 5	Vcc	Vcc	Merger of IO and Core power rails
	Vccusbcore		

The objective of merging USB power rail with core power rail is to understand if USB will be aggressed by Core. It is a common HSDP that core and I/O supply should not be merged (Venkataramani, 2009). However, to serve the objective of this research, it will be interesting to find out of the SSO noise is really a threat or a prospect in view that the merger will give USB additional Cdie (leveraging from Core) and the Cdie is at least 10x-20x greater than what USB's has by its own (chapter 4 will explain Cdie variation). Figure 3.6 shows the package design before and after merger on Jasper. This is the first case study that merges Core and I/O supply as one.

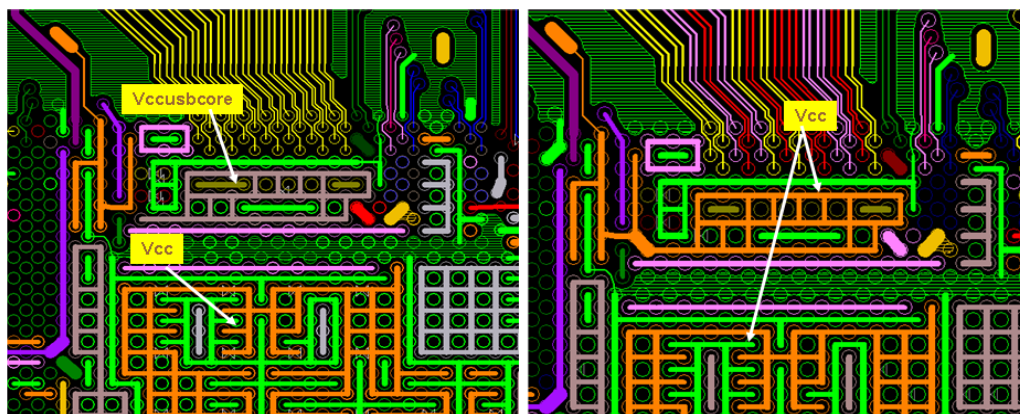


Figure 3.6: USB and Core power rail before merge (left) and after merge (right)

Merger Case 6: Combination of 3 Core power supplies

Test packages on which this is implemented:

Lucerne ☐ Jasper ☒ Milford Sound ☐

Table 3.6: Merger of three core power rails as one: AUX, EPW and MEW.

Cases	Before Merger	After Merger	Comments
Merger Case 6	Vccaux	Vccaux_mew_epw	Merger of Core and Core power rails
	Vccepw		
	Vccmew		

The objective is to study if the 3 core domains could be merged and if there is any threat to be noted. Typically, merger of core with core power rails should be harmless. The research intends to find out if there is any pitfall that has not been realized. Figure 3.7 shows the 3 core domains Vccmew, Vccepw and Vccaux. After the merger is done on Jasper, it is renamed as Vccaux_mew_epw. There is another core domain power rail, Vcc, and this remains standalone.

Figure 3.7: Three core domains power rails namely the VccMEW, VccEPW and VccAUX before merge (left) and after merge (right).

Merger Case 7: Combination of all 1.05V power rails

Test packages on which this is implemented:

Lucerne ☐ Jasper ☐ Milford Sound ☒

Table 3.7: Merger of all digital, analogue, I/O, core and PLLs power rails

Cases	Before Merger	After Merger	Comments
Merger Case 7	Vcc	Vcc	Merger of all Core and IO power rails inclusive
	Vccusbcore		digital and analogue PLLs as one power rail
	Vccsata		
	Vcc_exp		
	Vcc_dp		
	Vcc_fdi		
	Vccaux		
	Vccepw		
	Vccmew		

The objective of this merger is to combine all common voltage power rails on the package as one. Earlier case studies does the merger in incremental steps, this case study is to merge all digital and analogue PLLs and all digital core power rails with I/O power rails. It bypasses the HSDP and gives the research an opportunity to study how core would threaten the I/Os and PLLs when all are merged into one PDN. The implementation is done on Milford Sound to provide access route for maximum SSO coupling.

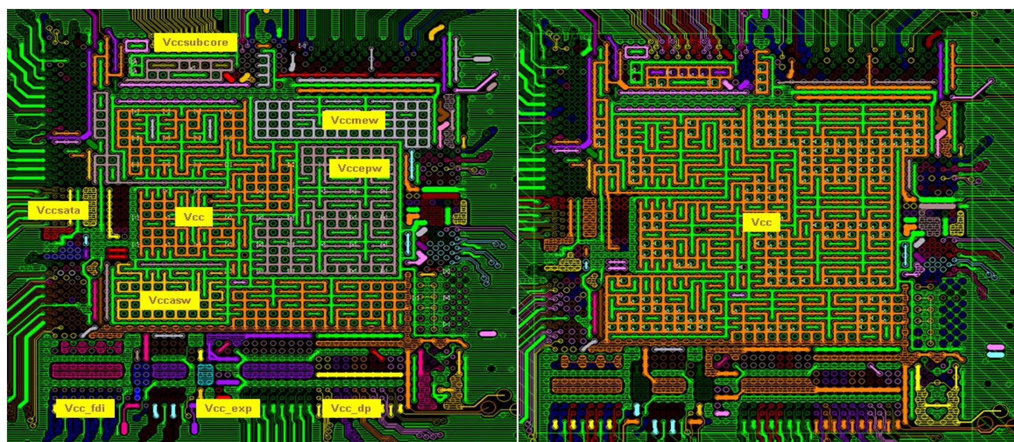


Figure 3.8: All common voltage power rails on PCH before merge (left) and after merged (right).

These test packages are sent for fabrication by a third party supplier, courtesy of Intel Microelectronics. Whether the merger of power rails will provide more optimized PDN design will be the main interest of this research project. If the advantage is taking precedence over the disadvantage, it will mark as first milestone in unfolding the unlimited potential to exploring new design principles. This aligns with the aggressive system-on-chip (SOC) integration need in achieving the smaller and sleeker form-factor design with high density of integration and lower package complexity.

3.4 Measurement of On-die capacitance (Cdie)

Section 3.3 has shown the various power rails merger implementations that are specially designed on Jasper and Milford Sound and the difference with Lucerne. The two significant changes that have happened when the power supply rails are merged, is the PDN impedance profile and the total amount of Cdie will change. The PDN impedance profile will be lowered, as a larger amount of vias, a larger size of power planes and pins are bounded as one single power rail or PDN. Likewise, the Cdie of a merged power rails will grow. Using one common power rail connectivity, the Cdie of one buffer is easily accessible by the other buffer family. For example, when Display Port and PCIe are sharing a common power plane design, there is a short of electrical path; thus Display port's Cdie is visible to PCIe, and vice versa, thus giving more cushion to high frequency noise suppression when these buffers are in operation. On the contrary, the supply noise from one I/O buffer is also made easier to couple from one to another.

On-chip capacitance (Cdie) is the capacitance cells specially built on silicon to ensure that the high frequency Input-output Buffers (I/O buffers) and core logic are performing and meeting high frequency noise design specifications. The continuous advancement of process technology, shrinking of gate size, and thus voltage, is suggesting that a smaller noise margin is required to maintain tip-top circuit and chip performance. One favourable approach to ensure chip's performance is by relying heavily on on-chip capacitance to help reduce coupling noise and on-chip operating noise. Modern circuits are increasingly laden with more on-chip capacitance to help meeting a small noise margin; and in turn meeting jitter and eye target; which however, is a costly solution that needs to be carefully accounted for.

In this section, the process of Cdie measurement methodology will be discussed in detail, focusing on equipment setup, and the step by step approach to arrive at the Cdie numbers. The results, however, will only be reviewed in Chapter 4.

Cdie measurement is the second most important step in this research as any changes in package design, is directly changing the amount of Cdie that each of the I/O or core power rails are exposed to. The PDN behaviour varies with Cdie variation. As mentioned earlier, in order to have a good understanding on how SSO magnitude and PDN resonance would vary with Cdie variation, it is important that the on-die capacitance be measured prior to

any on-die noise is measured. The Cdie has a direct impact to changing the SSO magnitude and frequency content.

3.4.1 Equipment setup for on-silicon capacitance (Cdie) measurement

The equipment needed for Cdie measurement is shown below:

Instruments and gadgets:

1. Performance Network Analyzer N5230C 300KHz-20GHz
2. Picosecond T-bias 5580-107
3. Topward 6302D power supply
4. GTL Calibration substrate Part# CS-11
5. GTL-4060 microprobe station
6. GTL 40A-750-GS-DS and 40A-750-SG-DS probe pair

DUTs:

1) Milford Sound (package and die)
2) Lucerne (package and die)
3) Jasper (package and die)
4) Milford Sound package substrate only
5) Lucerne package substrate only
6) Jasper package substrate only

Measurement Setup

Figure 3.9: Performance Network Analyzer (PNA) and probe station setup for Cdie measurement

3.4.2 Step by step measurement instructions on probe station:

- The Performance Network Analyser (PNA) is first calibrated to ensure that the measured output matches with its calibration standard. [Appendix A]
- PNA is connected to calibration substrate Part# CS-11 (Anon., n.d.) using sma cable, power supply, bias-T and placed on the GTL probe station (Anon., 2009)
- The microprobes (Anon., n.d.) 40A-750-GS-DS (port1) and 40A-750-SG-DS (port2) are calibrated using the calibration substrate Part# CS-11
- When the calibration is completed, only the calibration substrate is removed and replaced with the DUT.
- The two microprobes' (port 1 and port 2) are set down slowly on the 'Vcc pin' of power rail of interest; ensuring both Vcc probe tips make good contact on the Vcc pins; and both the Vss probe tips make good contact with the adjacent Vss pins on the DUT.
- The power supply voltage is slowly adjusted to set the bias from 0V to 1.05 V and leakage current from the DUT is observed. If there is no significant flow of leakage current (<500 mA), the measurement could continue as usual as it is an indicator that the DUT is healthy. If the leakage current is significant and higher than 500 mA, the measurement has to stop immediately and the DUT has to be replaced. This is to avoid using a faulty DUT for Cdie measurement.
- S21 of the DUT is measured and result is saved for post-processing to convert the S-parameter into Cdie parasitics

- The process is repeated on 3 other different units to ensure that the measurement is repeatable and consistent results could be obtained.

For more details on steps by steps guideline on how to operate a PNA and the details of each devices connection, refer to Appendix A: Detail PNA System Setup for Cdie measurement.

3.4.3 Post-Processing to convert S-parameter into Cdie parasitic

In order to find out the absolute Cdie parasitic, a software tool ‘PD express’ (Anon., n.d.) is used to read in the touchstone file i.e. the Cdie measured results from the PNA. The tool uses a lumped network as shown in Figure 3.10 (right) to represent the measured package and Cdie parasitic. By altering the Lpkg, Rpkg, Rdie, Cdie and Rleak in the table in Figure 3.10 (left), the tool will plot the S-parameter curve. The iteration continues till a match is found between the measured Z11 or Z12 to the inserted values in the table. The measured curve is highlighted in blue, while the curve-fit parasitic is in green. When both the measured and curve-fitted graphs overlap on top of each other, the corresponding Rpkg, Lpkg, Cdie, Rdie and Rleak match are found. These 5 parameters will then represent the parasitic of the measured power rail.

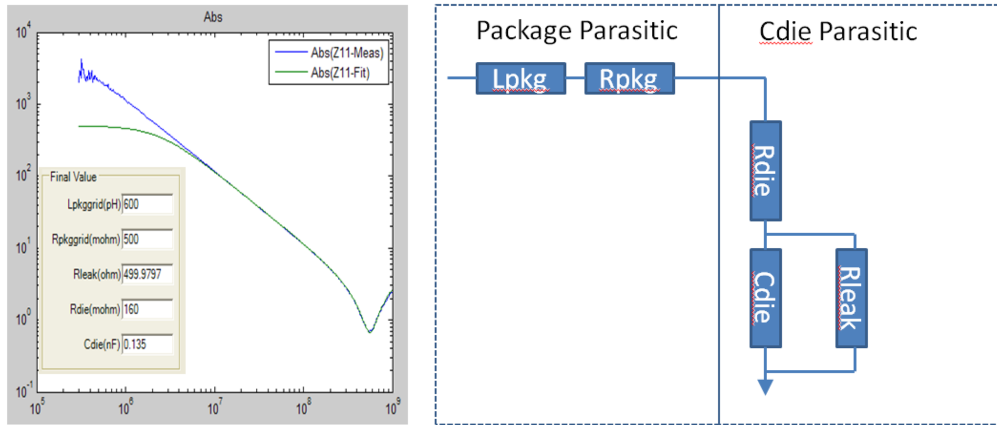


Figure 3.10: PD-express tool: Curve-matching table (left) and definition of package and die parasitic network (right)

The above measurement process is performed on these power rails on the three packages:

Table 3.8: Cdie measurement is performed on these power rails on 3 packages.

	Power Rails		
	Lucerne	**Jasper**	**Milford Sound**
Display Port PLLs	Vcca_A_dpl	Vcca_dpl	
	Vcca_B_dpl		
SATA2 (3GBps)	VccARX	Vccsata	
	VccATX		
	VccSATA		
	Vccdpll		
	Vcc_satapll		
Display Link digital PLL	Vccdpll_fdi	Vccapll_exp	
Display Link analogue PLL	Vccapll_fdi		
PCIe digital PLL	Vcc_dpll_exp		Vcc
PCIe analogue PLL	Vccapll_exp		
PCIe (2.5GBps)	Vcc_exp	Vccexp	
Display Port (2.75GBps)	Vcc_dp		
Display Link (2.75GBps)	Vcc_fdi		
USB2 (480MT/s)	Vccusbcore	Vcc	
Vcc (Core 4)	Vcc		
ME (Core 1)	Vccmew	Vccaux_mew_epw	
EP (Core 2)	Vccepw		
Gbe (Core 3)	Vccaux		

In some cases, where a more accurate measurement of Rdie is needed, additional step is taken to measure the package substrate parasitic only. The measurement is typically done to provide an absolute Rdie and Rpkg segregation. Using the approach illustrated in Section 3.4.3, the Rdie and Rpkg are estimated as there is no way that the resistance of package and silicon be separated. Sometimes, it is also useful that the package substrate parasitic be measured for diagnostic purpose if in case when the measured Rdie does not fall into the expected range. The substrate measurement procedure is highlighted in Section 3.4.4.

3.4.4 Substrate measurement

In order to investigate the influence of silicon resistance (Rdie) over the package resistance (Rpkg), the package substrate resistance has to be measured. A measurement is setup to short the package substrate according to the method below. In Figure 3.11, both power BGAs (grey) and ground BGAs (green) are shorted at the bottom layer of the package. The microprobes are landed on the power and ground bumps (indicated by the small arrows on top) to measure the close loop resistance of the bare package substrate.

Figure 3.11: Bare package substrate measurement probe points

This measurement is slightly different from Cdie measurement whereby the silicon die has been removed and only bare package substrate is measured. As the bare package substrate bump and BGA is opened when the silicon is removed, the BGAs are soldered to short together in order to form a close loop for a full path resistance measurement. Figure 3.12 shows the measurement setup for Cdie measurement, where the microprobes are landed on BGAs (power and ground respectively) while a voltage is biased to power up the on-die capacitance. The S21 parameter is captured for conversion to RLC numbers. Note that the Cdie measurement setup is slightly different from substrate measurement, whereby no voltage bias is needed as the substrate parasitic (Rpkg and Lpkg) are passive. No biasing is needed to bias the package for its parasitic measurement. During Cdie measurement, the total resistance, namely the substrate resistance (Rpkg) and silicon resistance (Rdie) are measured as one lump-sum. The exercise of substrate measurement allow the total resistance to be broken down into Rpkg and Rdie respectively.

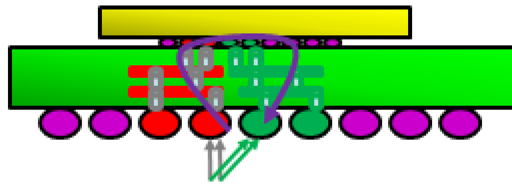


Figure 3.12: Cdie measurement setup.

After the Cdie and substrate measurement is completed, the next step is to figure out how to generate a worst possible supply noise excitation methodology to maximize the SSO for our research study.

3.5 Development of Concurrent stress tests validation approach

3.5.1 Finding the Worst Case Supply Noise Excitation Methodology

Most simultaneous switching output noise (SSO) validation of high speed interfaces such as PCIe, SATA, USB are approached on a case to case basis (Suryakumar, et al., 2004), (Suryakumar & He, 2005), (Natarajan, 2010), (Rahal-Arabi, et al., 2002) and (See Tau & Chan, 2009). Some concurrent tests make use of the device's design for test (DFT) modes to execute simultaneous tests on different interfaces like combining scan concurrently with analogue tests like RF tuners or serial ATA on an Automated Test Equipment (ATE) as discussed in (Molavi & McPheeters, 2007). Layout-aware worst case test pattern (Ma, et al., 2009), heuristic method in generating worst case power drop test pattern by accumulating high and low-frequency effects (Polian, et al., 2006), and mixed signal validation approach that comprehends both the logic and analogue aspects of the circuits during power-up sequence (Pan, et al., 2003) were attempts to develop a known worst case test environment to maximize supply noise creation in the validation setup. Recent publication (Arabi, 2010) has questioned the use of scan test mode to create a worst case test pattern "Scan test mode is vulnerable to power supply noise because switching activity is typically three to four times higher than in normal mode as a result of the DFT strategy. This leads to excessive voltage drop during scan testing. In some cases, voltage drop in scan mode has been so excessive that it has resulted in inadvertent logic value toggling and test result corruption".

Some test validation boards are setup to isolate completely one interface to another on its power rail to provide a clean path power transfusion while others choose to merge some of these power rails together on the system and to be completely ignorant of the fact that when the actual system are marketed, these luxuries of having an isolated power plane by itself is never the same as in the validation test lab. It is not always clear when these interfaces are put in a common validation eco-system and stressed concurrently, what will be the functionality and performance limiter. This section describes a new methodology that maximizes the power supply droop of each HSSL; by implementing a concurrent test in exercising PCIe, SATA and USB to actively transmit data on all the lanes on the electrical board; and at the same time; exerting power gate/ungate noise onto the chip to serve as a natural aggressor from the core logic into the I/O interfaces. The two test packages (Figure 3.13) which are designed (Section 3.2) to have merged power rails of these HSSL and core logic power rail will promote the injected and coupling noise from these concurrent tests. After this, on-die noise measurements will be measured and results will be compiled in Chapter 4 and 5 to conclude the findings of this new methodology.

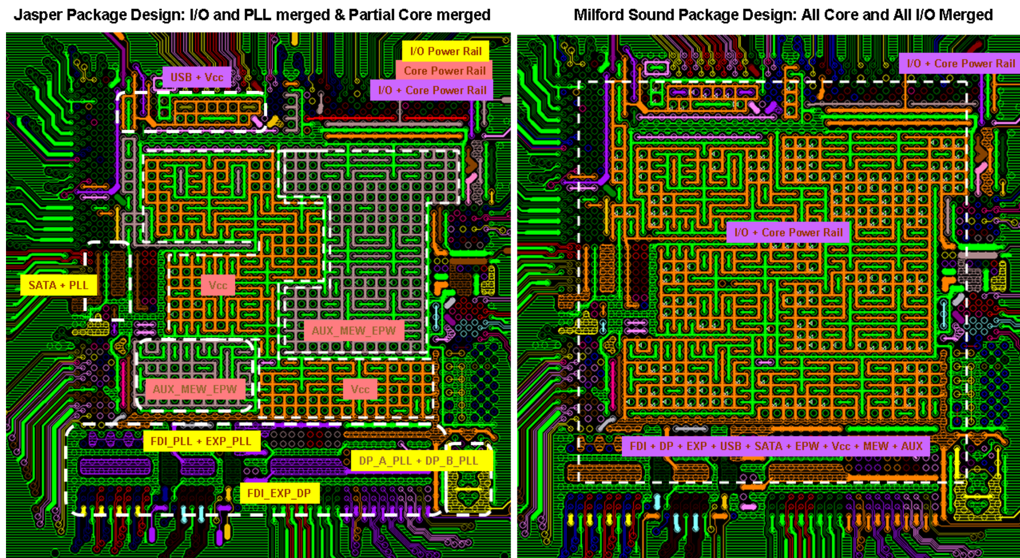


Figure 3.13: Jasper and Milford Sound are 2 test packages designed with various degree of merged power rails

3.5.2 Concurrent Stress Test Approach

By simultaneously exercising all the HSSL interfaces and having them transmitting and receiving at the same time is recommended as the approach to be used for worst possible SSO noise for PCH. PCH is an I/O hub and by using the natural events/ toggling activities on the silicon, the SSO is generated when real-time activities are running. Thus, although stressful, the concurrent stress approach by exercising these HSSL simultaneously is valid and not oversubscribing.

The proposed concurrent test on 1.05 V merged plane involves the following tests:

- “CMM4” Tx pattern to toggle all 5x PCIe ports (Section 3.2.3.3)
- “SATA Sync pattern” is exercised to toggle power state change on all SATA ports except the Operating System’s port [Appendix B & C]

- “USB Test packet” is exercised to toggle all 14 USB ports; with eye data collected on port 2 (9” cable & 19” cable) and port 12 [Appendix B & C]

In a typical test environment, the setup for eye and jitter compliance testing and noise validation for product health qualification is assigned to a single port only. To showcase how severe the concurrent test is imposed onto the system for the purpose of this research study, Table 3.9 compares side by side the difference between typical industrial product qualification execution setup and the concurrent stress test setup. Figure 3.14 shows the concurrent stress setup, where all I/O interfaces ports are populated with cards and receivers and traffics running on all ports on a standard desktop motherboard.

Table 3.9: Industrial product qualification v.s. concurrent stress validation setup

Industrial Product Qual Validation Setup	Concurrent Stress Validation Setup
One port at a time	All ports at once (worst port EYE and jitter is taken)
One interface each time	All interfaces at once
Core logic test and Analog test are tested separately	Core logic test and Analog test are tested together
All ports need to pass EYE and Jitter	All ports need to pass EYE and Jitter
One port transmitting at a time	
One port receiving at a time	All port transmitting and receiving at once
Analog Front End transmission validation	Analog Front End transmission and data bit validity check
Analog Front End receiver EYE validation	Analog Front End receiver EYE and digital data bit validity check
Power Delivery Noise validation check on one interface at a time	Power Delivery Noise validation check on all interfaces running at once
Cdie measurement on one interface	Cdie measurement on all interfaces on merged power plane
Across all temperature and skew corners	Selected known worst case temperature and skew corner only

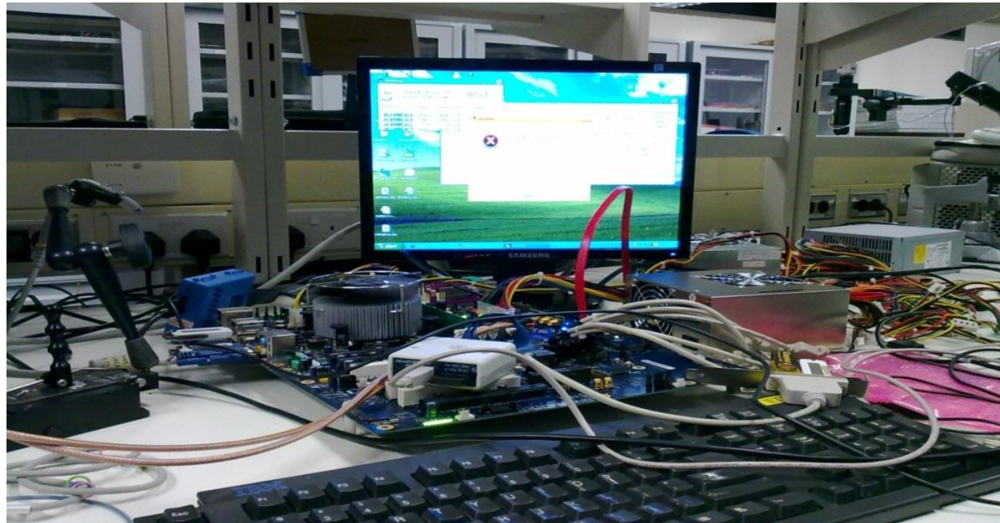


Figure 3.14: Concurrent test setup on a standard desktop motherboard

All the tests above are industrial compliance test that must be passed in order to achieve certification of product health.

3.5.3 PCIe Stress Test Approach

There are three HSSL interfaces which are being focused in this study; three stress test approaches are included in the write-up. Only PCIe stress test approach is chosen to be described in the main chapter, while two other stress approaches, namely the SATA and USB test approaches will be described in Appendix B & C. Appendix B describes stress test software setting and Appendix C describes eye measurements setup.

PCIe stress test approach is generally divided into four steps. The first step is hardware setup for on-die noise measurement, which will be described in Section 3.6. The second step is the software setup where the memory space on PCIe is changed so that a specific data pattern is transmitted through its

lanes. The third step is the oscilloscope setup, whereby eye diagram of PCIe could be captured and the noise to jitter/eye specification impact could be studied. The fourth step is eye-diagram post-processing. These four steps are common across HSSL; and the differences are the software used as well as the cable length, connectors and location on which the eye/jitter is measured.

Figure 3.15 shows a snapshot of WinMEM (Anon., n.d.). WinMEM is a software that allows the memory space on PCIe to be changed and CMM4 pattern will be transmitted. The specific step by step approach is illustrated below. Due to the memory space is highly classified, the address will be replaced.

1. Change Wimem Memory space to 0xaaaaaaaa
2. Change *0x4* column to aaaaaaaa
3. If CMM4 is not needed, change it back to 00

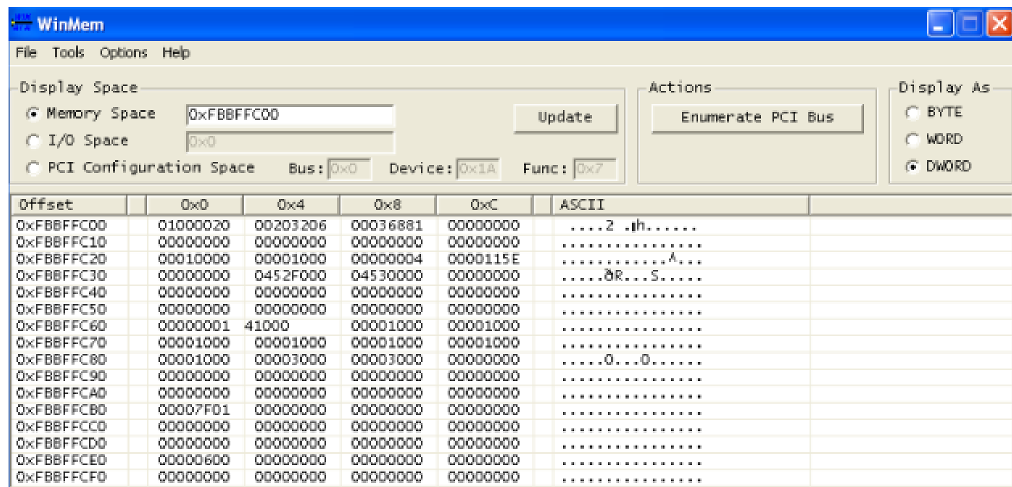


Figure 3.15: WinMEM software that changes PCIe memory space. (Courtesy of Intel)

PCIe eye diagram measurement hardware setup is shown in Figure 3.16. The hardware setup for PCIe eye diagram measurement includes an oscilloscope (8 GHz a.k.a. 20 GS/s bandwidth and 8 MB memory depth), 2 SMA cables (1m in length) and a Compliance Load Board (CLB) card.

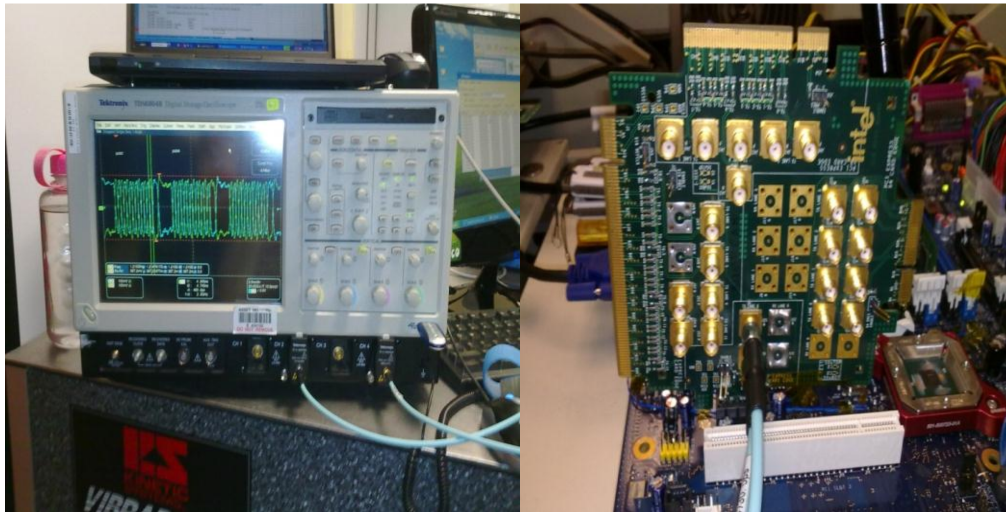


Figure 3.16: PCIe eye diagram measurement hardware setup

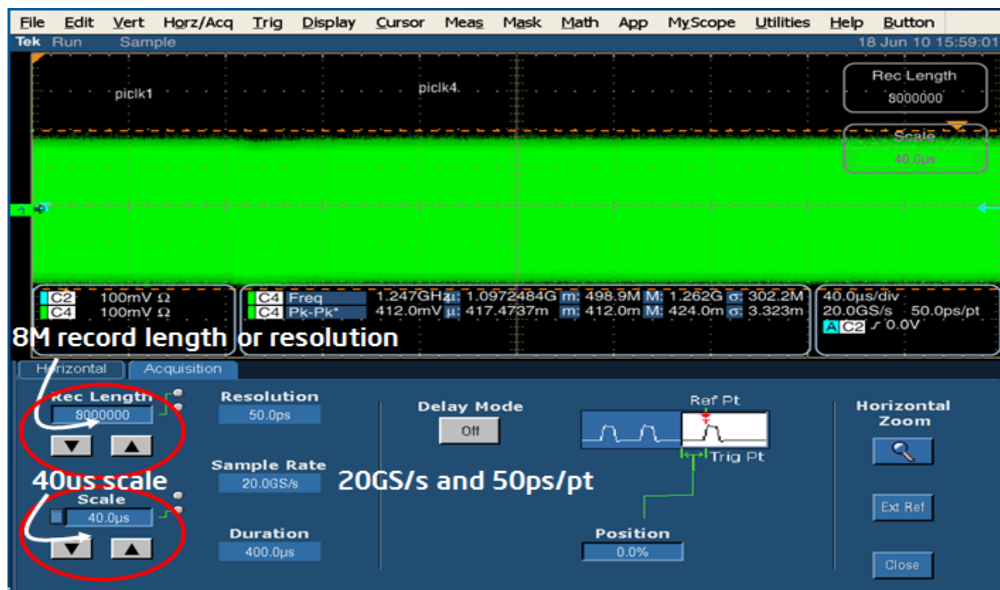


Figure 3.17: PCIe eye diagram oscilloscope’s setting.

PCIe eye diagram oscilloscope's setting is shown in Figure 3.17. Using the 2 SMA cables (1m in length), the Tx+ and Tx- eye diagram is measurement on Channel 1 and 3. The selection of channel is important, as channel 1 and 2, and channel 3 and 4 shares the same bandwidth. If channel 1 and 2 are simultaneously selected, the bandwidth 20 GS/s per channel will be halved, and left with only 10 GS/s. In order to ensure Tx+ and Tx- have equally high bandwidth for eye diagram measurement, channel 1 and 3 is selected. Likewise, channel 2 and 4 can be selected too.

The record length is set to 8 MB, and the time scale is set at 40 us. This is necessary for eye-diagram post-processing later. The savings of the data is shown in Figure 3.18. Reference waveforms and all WFms are selected for each Tx+ and Tx-, in this case, one waveform for channel 1 and another for channel 2.

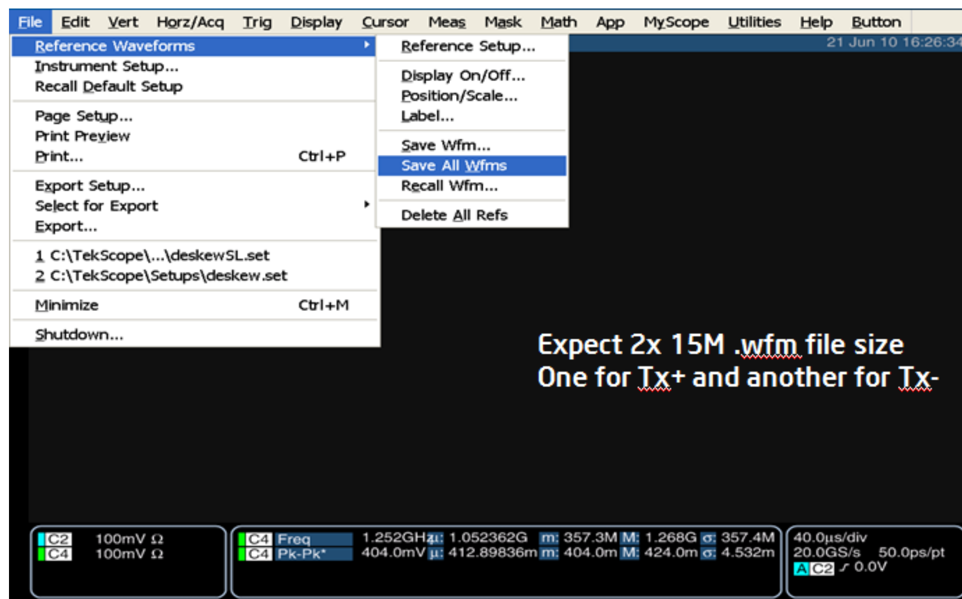


Figure 3.18: Savings of the data for eye diagram post processing

Figure 3.19 shows the PCIe eye/jitter post-processing tool. The tool launches 3 windows during the initialization. The step by step approach to convert the measurement into eye diagram is illustrated in Figure 3.20:

1) Choose input eye template definition
2) Load template file
3) Select template
4) Check PE valid
5) Select PCIe1 Tx Conn PE
6) Double confirm it is PCIe1
7) Check NPE valid
8) Select PCIe Tx Conn NPE

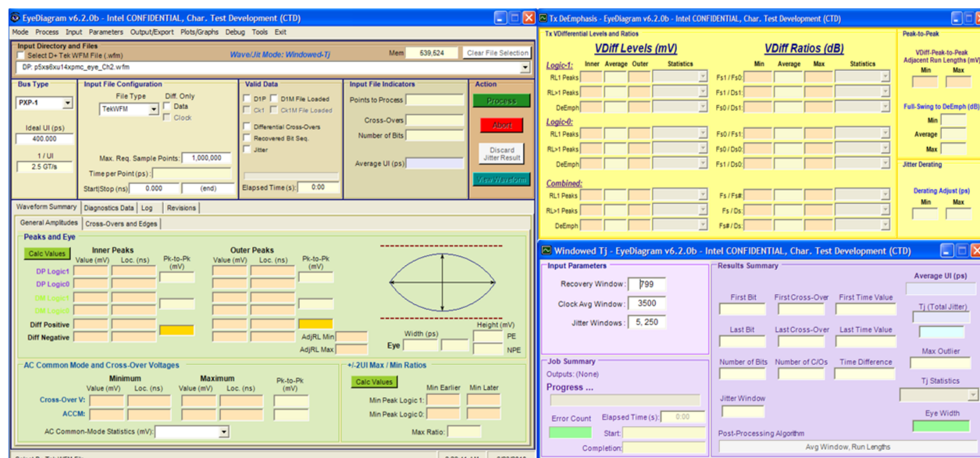


Figure 3.19: PCIe eye/jitter post-processing tool.

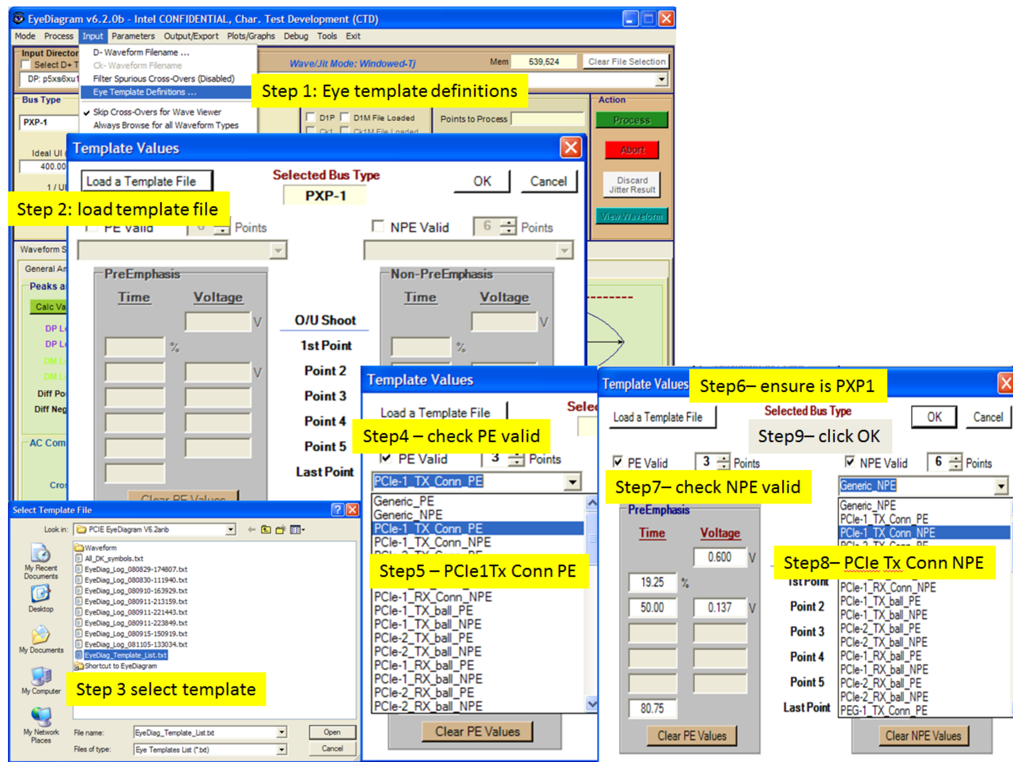


Figure 3.20: Step by step approaches in PCIe eye diagram plotting

Figure 3.21 shows steps 8 to 10 where it is the selection of measurement data for eye diagram processing. Figure 3.22 describes the remaining steps in obtaining the eye diagram. Both figures are pretty self-explanatory.

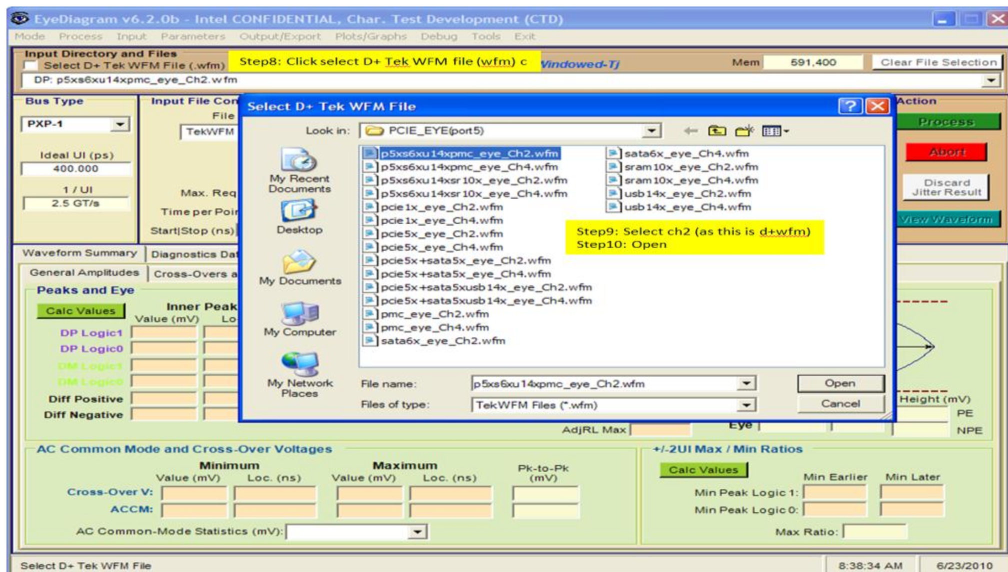


Figure 3.21:Steps 8-10 in selecting measurement data for eye processing

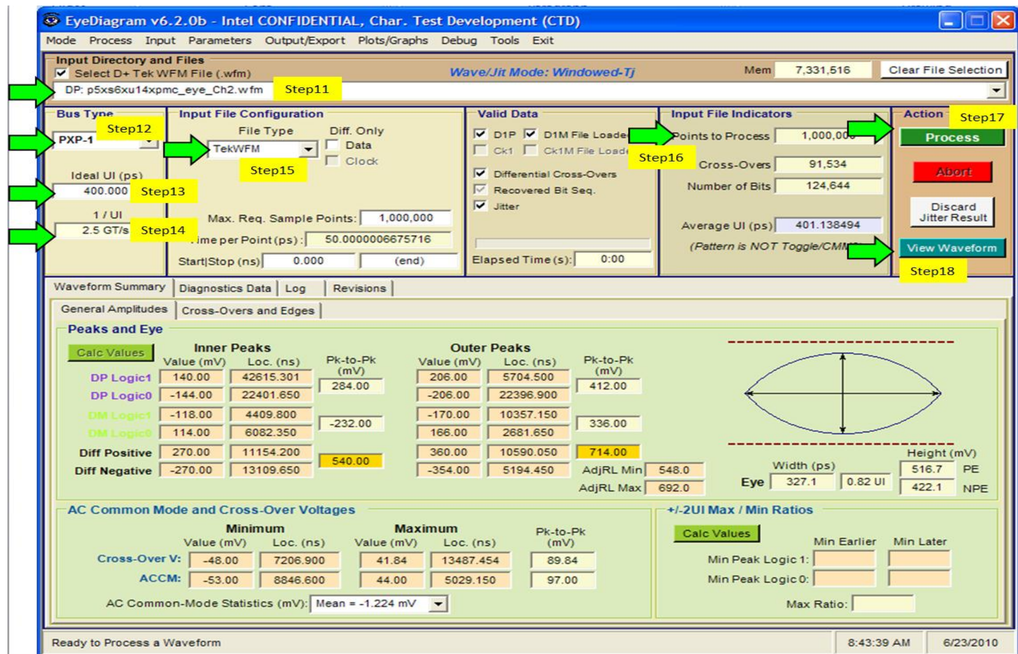


Figure 3.22: Steps 11-18 in PCIe eye processing

In this illustration, the PCIe port 5 with concurrent stress validation of 5x PCIe, 6x SATA, 14x USB and PMC is chosen for eye processing. The eye diagram is shown in Figure 3.23.

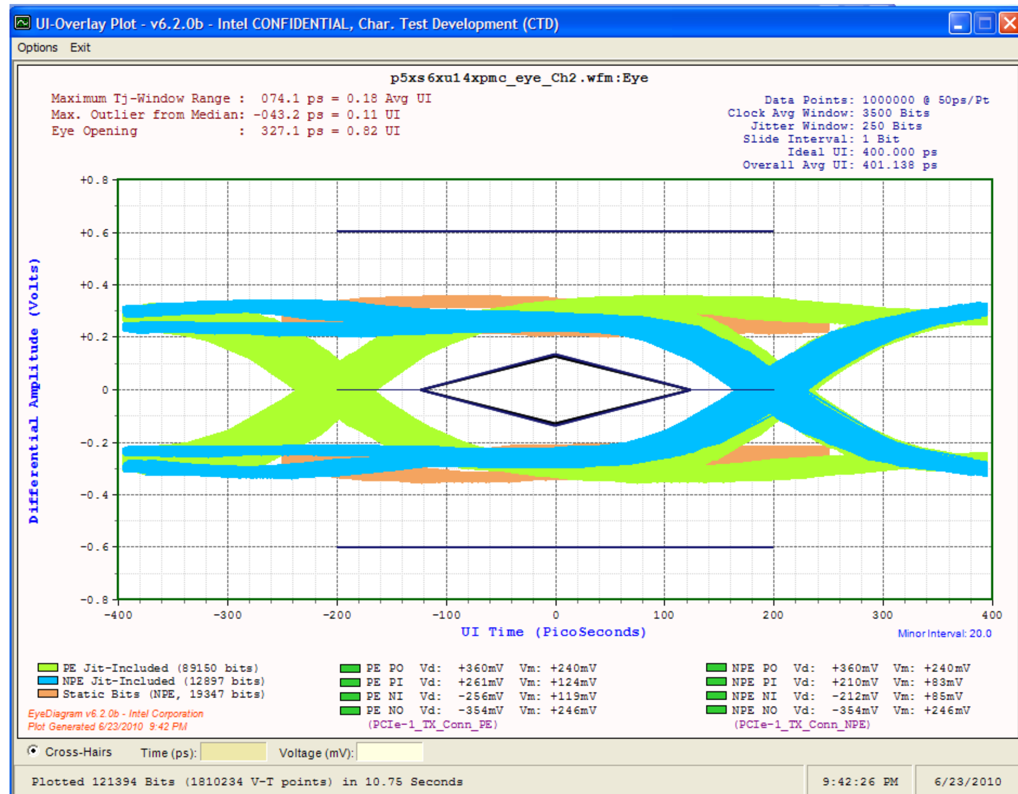


Figure 3.23: PCIe eye diagram on Port5

The setup for SATA and USB stress validation, from hardware to software and eye diagram post-processing is very similar to PCIe. The detail procedures of both are described fully in Appendix B and C.

With the setup of concurrent stress test approach described, the next step is to look into the hardware setup for on-die noise measurement.

3.6 Measurement of On-die noise

While the concurrent tests are running, jitter and eye for each HSSL which are toggling simultaneously is measured and captured, the peak-to peak SSO is measured on the package probe pad. As the peak-to-peak noise (mV) is the PDN design target while the jitter/eye is compliant specification; both measurement parameters are equally important for characterization. Section 3.5.3 illustrated in detail how HSSL Stress test setup can be performed on PCIe, and Appendix B and C continue the narrative of the Stress test setup for USB and SATA; and how jitter/eye diagram is measured and plotted. In this section, the hardware setup and on-die noise measurement will be described.

Special probe pads are built on the test packages to allow easy access to on-die noise measurement using micro-probes and a high-bandwidth oscilloscope. Figure 3.24 shows the close-up photo of how on-die noise was probed using the measurement setup.

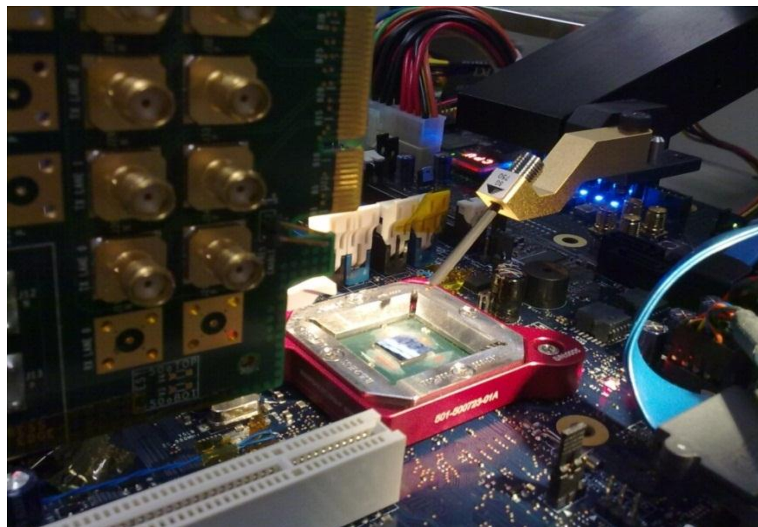


Figure 3.24: On-die noise measurement setup

Figure 3.25 shows the special probe pads which are built on the top layer of the package to provide easy access to the on-die noise probing. As the top layer is mostly Vss (green color plane), only Vcc probe pads are needed. When the microprobes are landed onto these pads, the solder mask is scrapped off using sand paper, to expose the copper contact of both the Vcc probe pads and Vss plane.

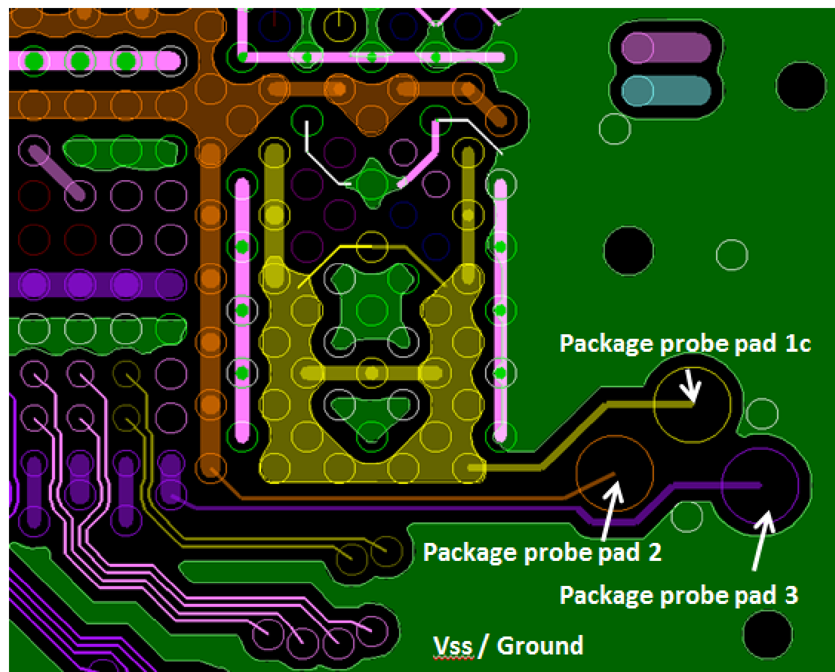


Figure 3.25: Special package probe pads are built on the 3 packages to provide easy access for on-die noise probing

As the microprobe is a differential probe S-G, the setup only uses one SMA cable to connect to the oscilloscope for on-die noise measurement. It is needed to ensure that the voltage offset is setup correctly for 1.05V and the vertical scale is setup to the highest resolution possible. Figure 3.26 shows how the oscilloscope is connected to the cable, and package probe pad.

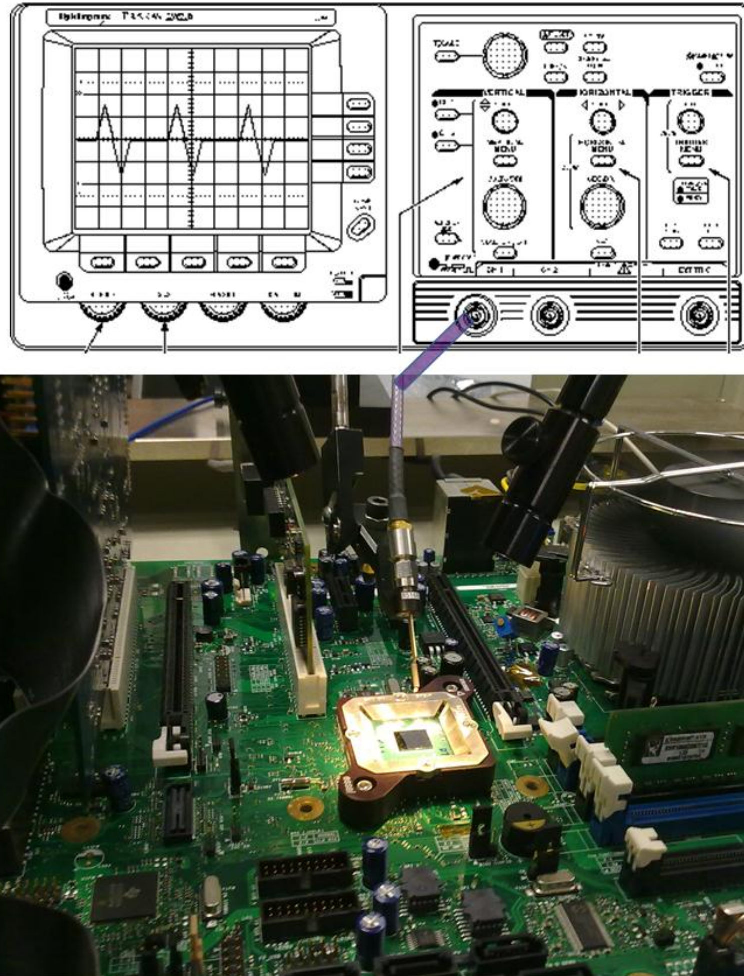


Figure 3.26: Oscilloscope is connected to the package probe pad via SMA cable and microprobe.

Sections 3.3- 3.6 have described in detail how test packages are designed and fabricated, how on-die capacitance is measured, how concurrent stress tests are developed and finally the on-die noise measurement setup methods. These 4 methods evolve further into substrate measurement, stress test software setting, oscilloscope setting for eye diagram measurement and eye diagram software setup for eye diagram plotting. All these methods above are useful for the research project but may not be sufficient for error diagnostic investigation. An additional section is added to this chapter to

explain the strategy when in case the stress validation method is insufficient to generate enough SSO and violate the eye specification; or for in case there is serious violation that needs immediate diagnostic methods to root-cause the issue. Section 3.7 – 3.7.3 will describes the flow of the research study and contingency plan on all the what-if cases.

3.7 Design of Experiment for Signal Integrity Power Integrity (SIPI) Research Study and Strategy for comprehending the unexpected scenarios

The worst case noise excitation occurs when one or more I/O interfaces' are stressed to excite enough SSO that either the peak-to-peak magnitude is violated or that its eye specification is partially or fully violated. Other possible failure to be watched for is either the transmitted traffic becomes stalled or the entire desktop system hangs and blue screen occurs.

In order to structure the research study in a proper order so that the SSO magnitude is increased in small increments, the following sequence of experiments are suggested. The system will not be put into stress by exerting all lanes to run concurrently, but a systematic approach is used to first gather the self- noise of each HSSL and core domains, and then self and coupling noise for incremental HSSLs, and lastly, the concurrent stress tests are run on all HSSL to collect the highest SSO of all interfaces operating simultaneously. The order of data collection in Chapter 4 will be prioritized in this fashion:

a. Self-noise of each individual I/O interfaces

b. Coupling noise of one interface to another interface, coupling noise of one core to another core, and coupling noise from Core to I/O.
c. SSO noise of multiple interfaces, starting from two interfaces, three interfaces and so on.... until all interfaces are turned on and excited simultaneously

At any point when a failure of eye/jitter is observed during the gradual increase of stress level with increasing of number of interfaces' excitation, this failure will be marked for further investigation.

In other words, the worst case noise excitation methodology is derived when one or more of the interfaces begin to break down or fail its eye/jitter specification due to the increase loading or cross coupling of noise from one interface to another. Likewise, the SSO noise will be studied in both time and frequency domains to help understanding the root-cause of the failure.

However, it is also a concern that the combined HSSLs SSO may or may not be sufficient to cause sufficient coupling noise and bring violation to the eye specification. This concern is valid because HSSLs target are set tightly within +/-4%, and is below the general +/-5% target suggested in (M. Swaminathan, 2007). Therefore, a contingency approach is recommended to help elevate the SSO impact in the event that all HSSLs are able to meet SSO target even when all ports are exercised to the full transmission and assisted by additional Cdie due to power rails merger on package.

3.7.1 Introducing Core Noise Injection via Aggressor Tests

In addition to the industrial compliance tests shown below (has also been described in Section 3.5.2),

- “CMM4” Tx pattern to toggle all 5x PCIe ports (Section 3.5.3)
- “SATA Sync pattern” is exercised to toggle power state change on all SATA ports except the Operating System’s port [Appendix B & C]
- “USB Test packet” is exercised to toggle all 14 USB ports; with eye data collected on port 2 (9” cable & 19” cable) and port 12 [Appendix B, C & D]

additional tests are suggested to be exercised simultaneously in attempt to inject noise into the system and serve as aggressors to the I/O HSSL PDN. These aggressor scripts are tests specially designed and customized for Intel internal stressing purpose and are not intended for certification of product health. Since these stress tests are customized, it has the flexibility in scaling the intensity from low to high extremity; which is only limited by hardware design. Two aggressor tests suggested are shown below:

- As many as 10 SRAMs is scripted to loopback power ungate/gate activities (Section 3.7.5) and injecting a periodic noise from core into I/O power rails. The noise injection from core also represents a threat of digital noise to test the eye robustness of the analogue circuit.
- PMC is scripted to loopback power ungate/ gate activities and be an aggressor to inject periodic noise at every clock cycle from core into I/O power rails and test the eye robustness. The PMC noise is at least

3x more severe than 10 SRAMs noise. The transient noise that is introduced by PMC can go as far as 100mVpp on its merged PDN.

Having all the 1.05 V power rails merged as a single power net on the package and stressing each I/Os to run at its data pattern at its fullest bandwidth; while at the same time introducing aggressors such as SRAM or PMC to inject noise as large as 30mV-100mVpp is nonetheless one of the most extreme cases that is being considered in this study. The objective is not only to stress the DUT to its fullest but also incur much stress to the board and power supply system. The board design and power supply system has to be robust enough to sustain the operation of the DUT without failing as stressing all ports of interfaces at the same time is never a guarantee on how much time it could last before the system wears out and breaks down. Careful examination of system robustness is needed to ensure that all other parts on the boards are operating as expected so that any failure related to the DUT can be determined, and not to be confused with the failure of other components.

The new concurrent stress test configurations now consist of:

- USB bus transactions on all 14 ports
- SATA bus transactions on all 6 ports
- PCIe link transaction up and running for all 5 ports
- 10 SRAMs power gate and ungate routinely in infinite cycle (expect 30-80 mVpp OR
- VccAUX power ungate event (100 mVpp) to trigger worst case eye closure on I/Os involved

3.7.2 Removing of on-package decoupling capacitor

In order not to mask off the noise by aggressors, the PDN is stripped down step by step to increase the exposure of PDN to maximum induced noise generated by the switching activities on die; till a failure or jitter violation is observed. This will include removal of package capacitor and board capacitor.

3.7.3 Reverse Margining the failed system to marginally passing the eye specification

In the event that a failure of eye specification is detected during the concurrent stress test, the number of tests applied to the system could be reduced sequentially in order to reduce the intensity of the SSO stress level. For example, 5 concurrent test routines are introduced in Section 3.7.1, and if a failure is observed when 4 tests are running concurrently, the last added test should be removed from the stress test, to lower the intensity. At this point, the eye plot can be re-examined to see if the error could be removed and system health is able to be recovered. As the Core noise scripts are also scalable in the sense that its intensity can be varied by reducing the SRAMs banks from 10 to 1, the script could be modified to lower the intensity of the stress test till a passing mark is arrived at. Likewise, PMC stress intensity could be reduced to increase the delay time from one power ungate to another power ungate, so that the interval between these SSO injection is prolonged to a longer period, and thus changing the SSO frequency content. The passing criteria and the failing criteria should be marked for analysis later.

3.7.4 Reconstruction of Current Profile using Norton's & Thevenin's Theorem

One of the diagnostic methods which may come in handy later is by using de-convolution of SSO noise to reconstruct the current profile, Icc(t). The measurements data that will be collected in the lab is confined within either a SSO or eye data, where both are represented as voltage. One is the power supply's voltage transient while the other is data toggling down the transmission line. Voltage is the measurement parameter and not current.

"As a power delivery network is a linear time invariant system. Thus, superposition principle applies. Namely if the Fourier decomposition of Icc(t) contains the these three harmonic components, the Fourier decomposition of *V(t)* will contain these three harmonic components as well but multiplied by the impedance of the power delivery network impedance at these specific frequencies. This is illustrated by Eq. (11).

$$F\{V(t)\} = Z(f) \cdot F\{I(t)\} \quad \text{...} \quad (11)$$

where *F{G(t)}* represents the Fourier transform of time domain function *G(t)"* (Waizman, et al., 2004).

In other words, if the current profile spectrum analysis contains the 27.5MHz component in its FFT plot, but there is no peak resonance at 27.5MHz on the PDN impedance profile, Z(f); then it is most likely that the 27.5MHz noise is current induced. As suggested in Eq. (11), the noise profile is generally the product of current and impedance at its frequency spectra. Any noise profile is either induced by circuit/ core current or PDN's Z(f).

In short, by de-convoluting the noise into current spectrum using an extracted PDN Z(f) (Section 2.2.8), it allows one to immediately identify if the noise V(f) is an end product due to PDN Z(f) or Icc(f). If the V(f) is caused by PDN's Z(f), removing capacitors will help to shift the PDN resonance and help us reconfirm the noise source. However, if the noise is caused by Icc(t), then, the excitation of stress test contents could be altered to confirm the noise origin. In both cases, it is a diagnostic method that allows a clear definition of whether the SSO is induced by Z(f) or I(f).

In order to develop an understanding on how de-convolution technique can be used to derive the Z(f) and I(f), Norton's and Thevenin's theorems (Anon., 2013) and (Anon., 2013) are applied. "In practice, there is no ideal current source and an ideal current source cannot be connected to an ideal open circuit. Nor an ideal voltage source can be connected to an ideal short circuit. Since no ideal sources of either variety exist (all real world examples have finite and non-zero source impedance), any current source can be considered as a voltage source with the same source impedance or PDN and vice versa. Voltage sources and current sources are sometimes said to be duals of each other and any non-ideal source can be converted from one to another by applying Norton's or Thevenin's theorems.

Norton's theorem for electrical networks states that any category of voltage sources, current sources and resistors with two terminals is electrically equivalent to an ideal current source, I, in parallel with a single resistor, R

(Figure 3.27). For AC systems the theorem can be applied to general impedances, not just resistors. The Norton equivalent is used to represent any network of linear sources and impedance, at a given frequency. The circuit consists of an ideal current source in parallel with an ideal impedance (or resistor for non-reactive circuit)"

In electrical circuit theory, Thevenin's theorem for linear electrical networks states that any combination of voltage sources, current sources and resistors with two terminals is electrically equivalent to a single voltage source V and a single resistor R (Figure 3.28). For AC systems, the theorem can be applied to general impedances, not just resistors.

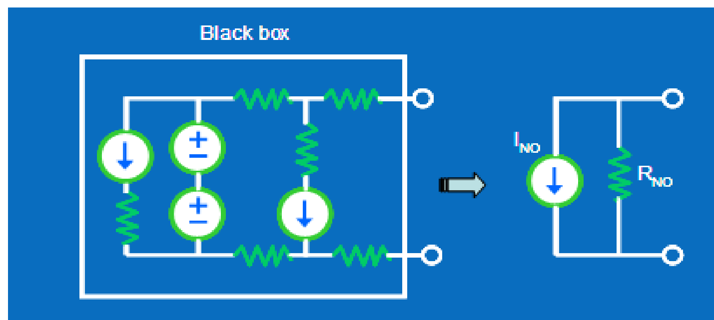


Figure 3.27: Norton's equivalent circuit.

This theorem states that a circuit of voltage sources and resistors can be converted into a Thevenin's equivalent circuit, which is a simplification technique used in circuit analysis. The Thevenin's equivalent circuit can be used as a good model for a power supply or battery (with the resistor representing the internal impedance and the source representing the electromotive force). The circuit consists of an ideal voltage source in series with a resistor.

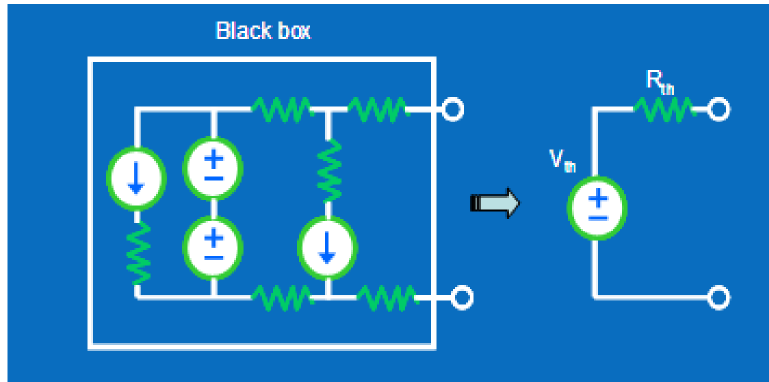


Figure 3.28: Thevenin's equivalent circuit.

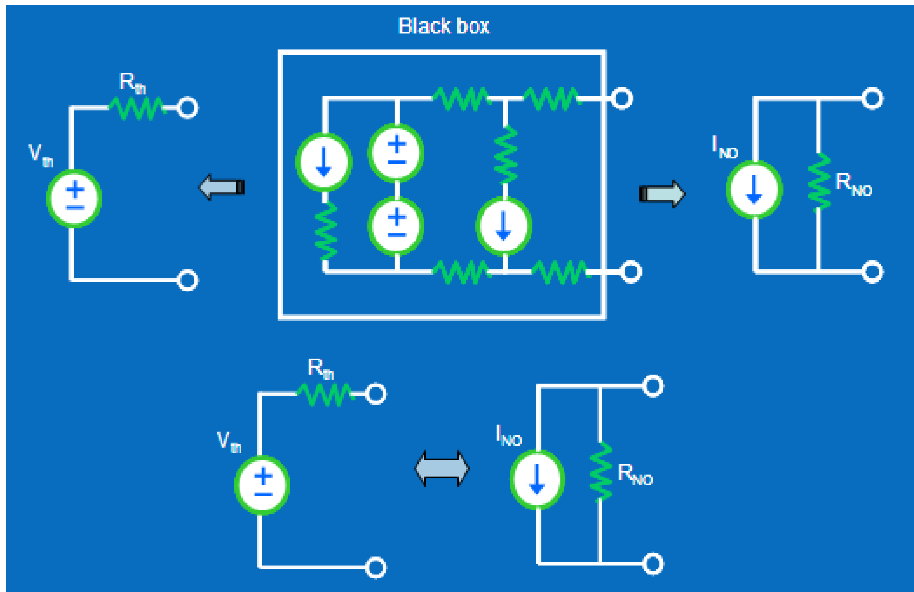


Figure 3.29: Norton's and Thevenin's theorem put together

In short, Norton's and Thevenin's theorems allow the de-convolution of voltage profile into current profile and vice versa; in a linear time invariant system. Thus, reconstruction of current profile is possible using the noise profile measured from lab (Tan, 2009).

A PDN is setup as shown in Figure 3.30, whereby the current profile is de-convoluted by replacing the PWL source with the measured Vnoise (Vpwl) and the die current is measured at the same location as the probing point on

the DUT. As the PDN is representing the Z(f) of the system, the I(f) can be reconstructed by de-convoluting the V(f) measured from the system.

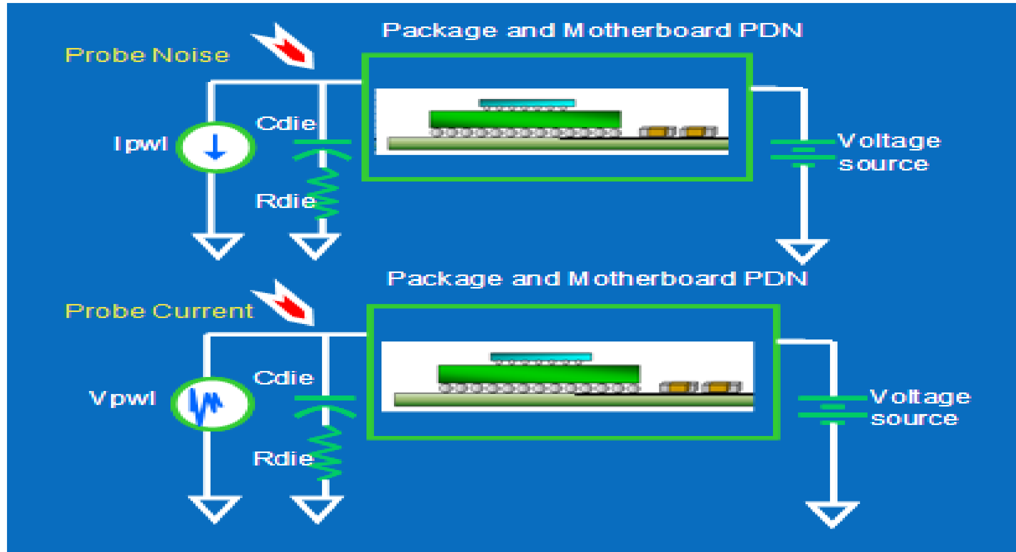


Figure 3.30: PDN setup to de-convolute the measured noise profile and reconstruct the current profile.

3.7.5 Power gating/ungating influence on PDN resonance frequency

Another supporting factor that encourages reconstruction of current profile for diagnostic purpose is the reason that power gate/ungate is used as one of the SSO noise injector. Tracking just the PDN resonance and ignoring the current profile analysis would not be accurate enough. However, determining the PDN resonance could be tricky as the PDN resonance would shift when different traffic is driven onto the DUT. Earlier discussion on Cdie parasitic measurement (Section 3.2.2) helps in quantifying the Cdie amount of the PDN when no HSSL is toggling. This Cdie number is only good for a fair modelling need. When different traffic or data pattern is driven at different occasion, the toggling activity will directly and indirectly alter the Cdie

composition; especially when all power rails are merged under a common power plane. This is driven by the fact that now that the coupling capacitance from the power to signal, or signal to ground has contributed some additional capacitance to the PDN. Besides, by power ungating and power gating the PMC, a change of Cdie by a few nF is inevitable. As a result, the power gate/ungate event will shift the PDN resonance by a few MHz (Tan, et al., 2009). Figure 3.31 shows an example of power supply noise frequency is greatly shifted when a core partition is power gated and power un-gated. During power un-gate, the voltage droop is registering a 30 ns droop period. This is translated to a 33 MHz voltage droop. The noise profile is observed as 278 MHz when the core partition is gated; where the period of the droop is reduced to as small as 3.6 ns

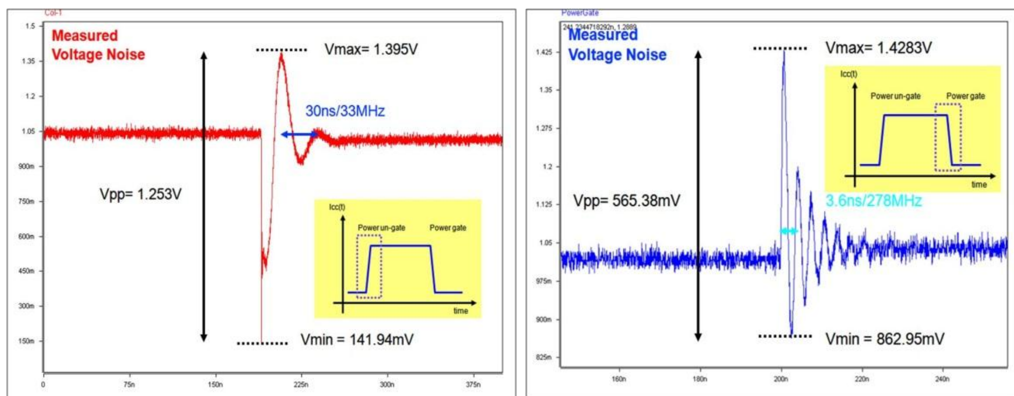


Figure 3.31: Power gate (left) and power ungate (right) shifts PDN resonance

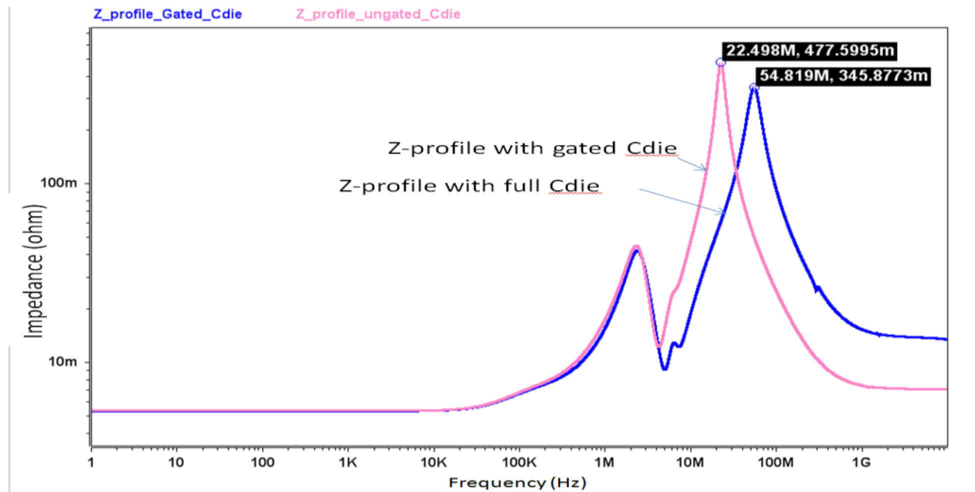


Figure 3.32: A shift of 32 MHz is noted on PDN resonance during a power gate and ungate event, on a single-isolated power rail.

Figure 3.32 shows an example of a standalone and isolated PDN's resonance which is originally captured as 54.8 MHz, a shift in PDN resonance by 32 MHz is observed when a core partition gates and ungates. As such, both current profile and impedance profile need to be fully deciphered in order to determine the noise source accurately.

Besides, the power gate and ungate event is a periodically triggered event that constantly power gate and ungate the PMC partition, thus, the PDN resonance is unlikely to settle at a specific resonance frequency during the operation. In a nutshell, it is difficult to predict the actual PDN resonance when the system is operating; especially when the shift happens in a repeating fashion; in and out according to the switching clock speed and power supply transient response.

3.8 Summary

This chapter highlights the research plan starting from test package design and fabrication, Cdie measurement and parasitic extraction, Concurrent stress tests development and on-die noise probing methodologies; which are the four major steps needed in this research study. If any of the research plan does not proceed like expected, or some unexpected events show, suggestions on how the SSO intensity could be increased and reduced is included. Finally, the chapter is wrapped up with diagnostic method such as reconstruction of current profile and PDN resonance prediction technique during power gate/ungate event.

CHAPTER 4

CDIE MEASUREMENT AND CONCURRENT STRESS TEST RESULTS ON HSSL

4.1 Introduction

In the previous chapter, test packages design and Cdie measurement method have been described in full to illustrate how power rails are merged and the effect of merger will lead to Cdie variation and PDN resonance shift. In additional, concurrent stress tests are suggested to be used to maximize SSO coupling from one PDN to another, such that when all HSSLs are fully toggling on the desktop motherboard, the worst possible but realistic SSO is brought to excitement. This sets the boundary SSO to a realizable worst case and eliminates any potential overdesign or redundancy which is usually baked in due to inaccurate modelling assumptions.

This chapter aims to discuss two topics of measurement results, i.e. the Cdie measurement results and Concurrent Stress Tests Results on all three HSSLs. The Cdie measurement findings show some deviations from its initial expectation, thus leading to an in-depth investigation to identify the root-cause of this deviation. Three hypotheses which could lead to the Cdie deviation are investigated. Next, the results of Concurrent Stress tests on the three HSSLs will be discussed. Overall, it is rather exciting to show from this initial results that almost all HSSLs are passing the eye specification although the self-noise +/-4% target is violated; which supported the objectives of the research study, whereby “what is believed to be needed” v.s. “what is really

needed” are indeed real as most of the beliefs could be compromised and the governing high speed design principles should be revisited.

4.2 On-Silicon Capacitance (Cdie) Measurement Results

In this section, the Cdie variation due to power rail merger to the overall PDN design is studied. After that, the leveraging of Cdie across the different power rails compare to isolated power rail cases is characterized.

The first package, codename ‘Lucerne’ enforces the standard design rules whereby every digital and analogue power rails are separated and properly isolated. The design is intended to provide isolation to all the power rails; which however, is traded off with lower Cdie as it could not leverage its neighbouring Cdie. The second package design, codename ‘Jasper’ contains a moderately merged power rails; whereby common voltage I/O buffers are merged with I/O buffers; especially those located adjacent to each other. Likewise, Core 1 power rail is merged with Core 2 power rail. The third package design, codename ‘Milford Sound’ contains of one single power rail, merging all the Cores and I/O buffers of common voltage as one (Table 4.1).

Table 4.1: An overview of three different packages power rail merger plan: Lucerne, Jasper and Milford Sound.

	Power Rails		
	Lucerne	**Jasper**	**Milford Sound**
Display Port PLLs	Vcca_A_dpl	Vcca_dpl	
	Vcca_B_dpl		
SATA2 (3GBps)	VccARX	Vccsata	
	VccATX		
	VccSATA		
	Vccdpll		
	Vcc_satapll		
Display Link digital PLL	Vccdpll_fdi	Vccapll_exp	
Display Link analogue PLL	Vccapll_fdi		
PCIe digital PLL	Vcc_dpll_exp		Vcc
PCIe analogue PLL	Vccapll_exp		
PCIe (2.5GBps)	Vcc_exp	Vccexp	
Display Port (2.75GBps)	Vcc_dp		
Display Link (2.75GBps)	Vcc_fdi		
USB2 (480MT/s)	Vccusbcore	Vcc	
Vcc (Core 4)	Vcc		
ME (Core 1)	Vccmew	Vccaux_mew_epw	
EP (Core 2)	Vccepw		
Gbe (Core 3)	Vccaux		

In order to ensure that the package parasitics are captured accurately, measurements of bare package substrates (Section 3.2.2.4) are done using similar probe point where the Cdie is measured. While measuring the Cdie, the leakage current from each of the power supply rails are monitored carefully to ensure that no excessive leakage occurs. In the event when excessive leakage occurs, the measurement is re-taken using another DUT or a reset is applied to alter the floating state of the power well and rectify the logic state of the DUT.

Table 4.2: Cdie efficiency reduces with power rail merger from 15%-22%.

	Lucerne	Jasper	Milford Sound
Total Cdie	115	100	100
% Cdie	100%	78%	85%

The variation of total Cdie that are measured on 3 different packages (Table 4.2) deviates from 78%-85% from its standard benchmark of 100%.

This signifies that not 100% of the Cdie that is available on standalone and isolated PDN shows up in the merged power rails PDN. Lucerne, which is the benchmarking package, is measured with 115 nF of total Cdie. Jasper's and Milford Sound's measured Cdie are 15%-22% less Cdie than Lucerne respectively. The total Cdie has reduced not because the silicon has changed, but due to the package design has changed. It is no longer optimized for the Cdie sharing across the many different I/O power rails that are scattered around the packages. Further breakdown of effective Cdie on the two merged power rails package, i.e. Jasper and Milford Sound on all HSSLs and Core are shown in Table 4.3. The Cdie efficiency on merged power rail PCIe/DP/FDI is especially low at only 56% of its expected Cdie, compare to the PDN when it is designed as single and isolated power rail.

Table 4.3: Breakdown of effective Cdie on two packages, against Lucerne

	Jasper	Milford Sound
SATA	75%	
PXP/DP/FDI	56%	
		85%
Core / USB	88%	
ASW	93%	

There are three hypotheses that explain why the expected Cdie are not achievable from the merged power rails PDN:

1. Package layout is not optimized (large Rpkg) or on-die power grid (large Rdie) layout is prohibiting an easy access to neighbouring Cdie
2. Cdie measurement probe location and biasing point is not strategic to penetrate the vast vicinity of the area and sufficiently bias the designated die area

3. Both package layout and die power grid layout are not optimized (large Rpkg and Rdie) on their mutual connectivity and thus prohibiting an easy access to neighbouring Cdie

4.2.1 Hypothesis 1: Package Routing Discontinuity Study

In order to find out what is the root-cause of the effective Cdie reduction when the power rails are merged, two power rails on Jasper package are visually compared side by side. The two selected power rails are PCIe/DP/FDI which carry only 56% of expected Cdie, while the other is ASW power rail which retains 93% of expected Cdie. These two power rails are from the same package but have an extreme Cdie variation where one has merely half the total Cdie while the other almost close to full Cdie retention. Since both power rails resides on the same package, and is designed by the same experienced designer; while the silicon design does not change, the Cdie effectiveness should not vary much. The comparison of routing continuity on both power rails is done on four selected layers on the Jasper package (Figure 4.1- Figure 4.4), eliminating the ground layers in between. The black circle highlights the ASW power rail (grey colour net) while the yellow circle highlights the merged PCIe/DP/FDI power rail (purple colour net).

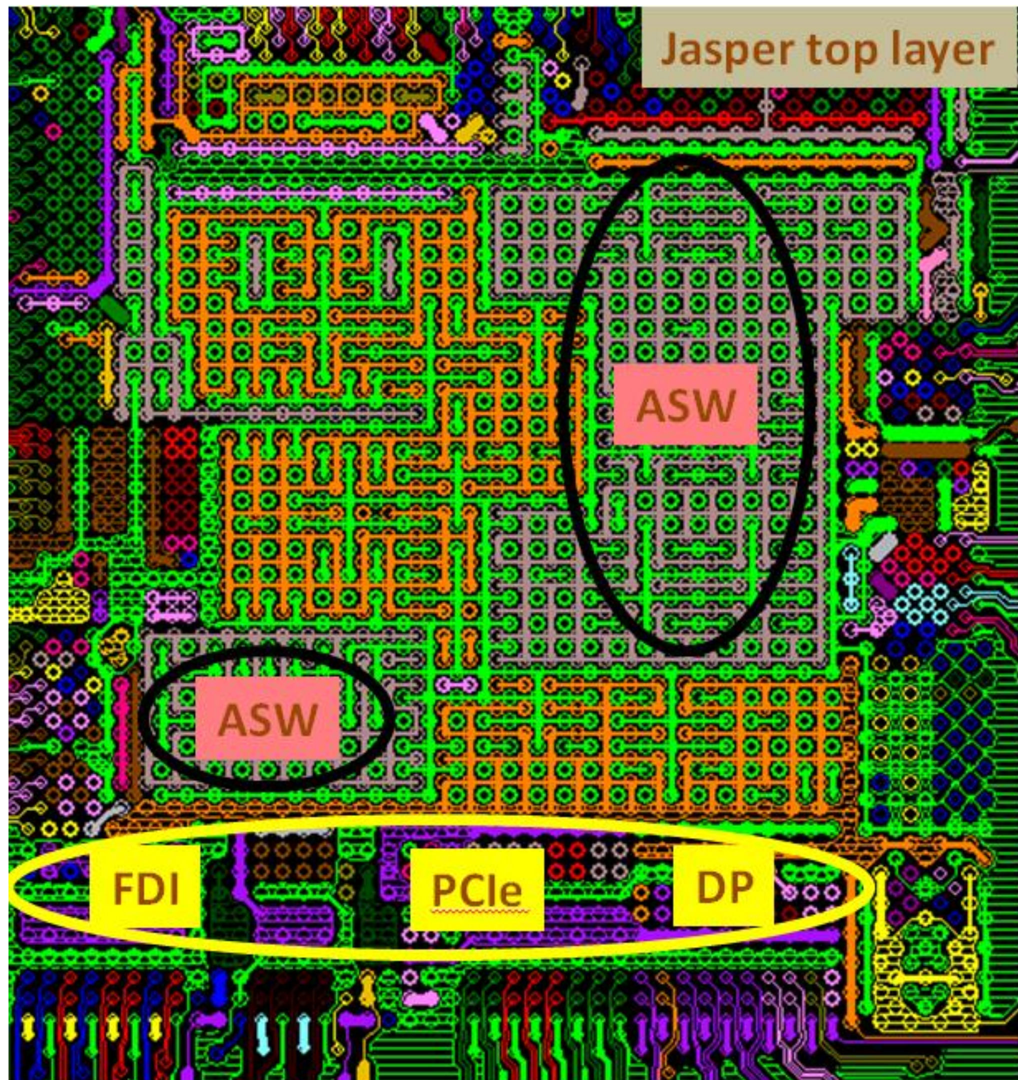


Figure 4.1: Top layer of Jasper. ASW power rail (grey net) and the merged PCIe/DP/FDI power rail (purple net) are marked in circles.

At first glance of top layer of Jasper (Figure 4.1), all the power bumps are connected to the silicon. Package and die connectivity are equally good. Both ASW and PCIe/DP/FDI power rails have different clusters that scatter across the package in different bump groups and the lateral connectivity is fairly poor on both power rails. However, the vertical connectivity remains intact where all silicon bumps are connected with micro-via to support top-down connectivity.

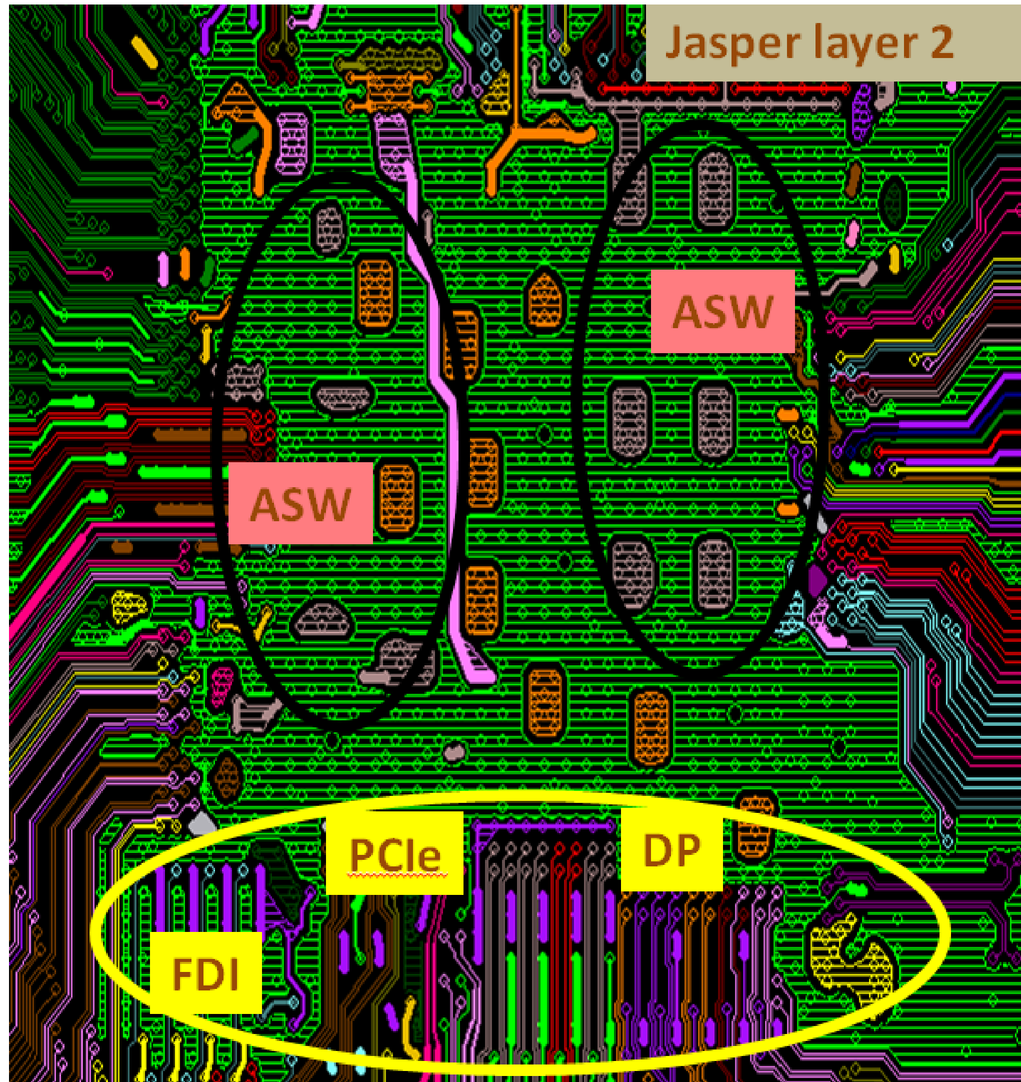


Figure 4.2: Layer 2 of Jasper. ASW power rail (grey net) and the merged PCIe/DP/FDI power rail (purple net) are marked in circles.

Next, layer 2 of Jasper is examined (Figure 4.2). Both ASW and the merged PCIe/DP/FDI power rails have no lateral connectivity between the different clusters of power islands. Both structures remain vertically connected in a top down direction. At this point, lateral resistance remains high on both power rails.

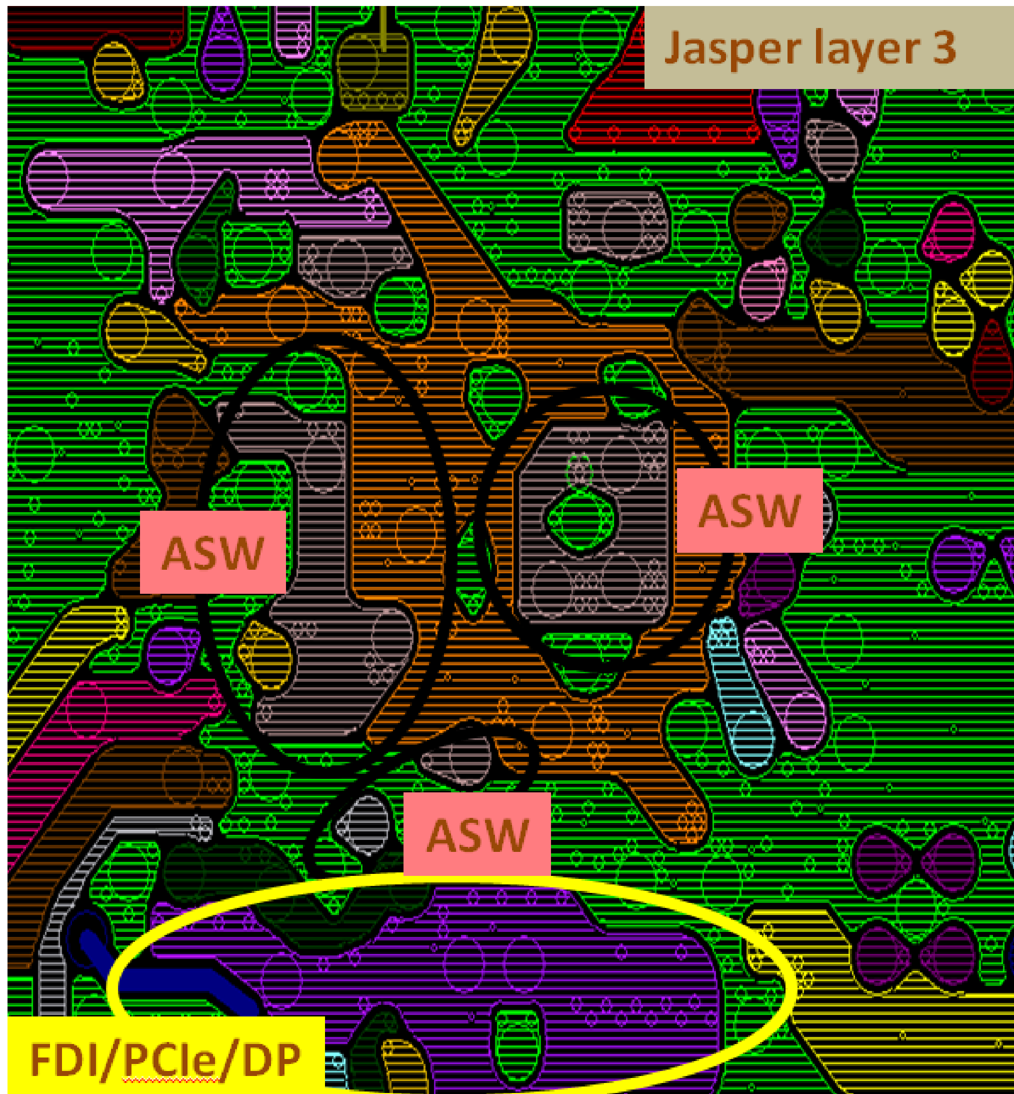


Figure 4.3: Layer 3 of Jasper, showing the lateral connection for ASW and PCIe/DP/FDI power rails.

Lateral routing on Jasper starts on layer 3 (Figure 4.3), for both ASW and the merged PCIe/DP/FDI power rails. ASW power rail's lateral routing is worse compare with the merged PCIe/DP/FDI power rail. The hypothesis that the package routing discontinuity causes the reduced Cdie being measured becomes arguable.

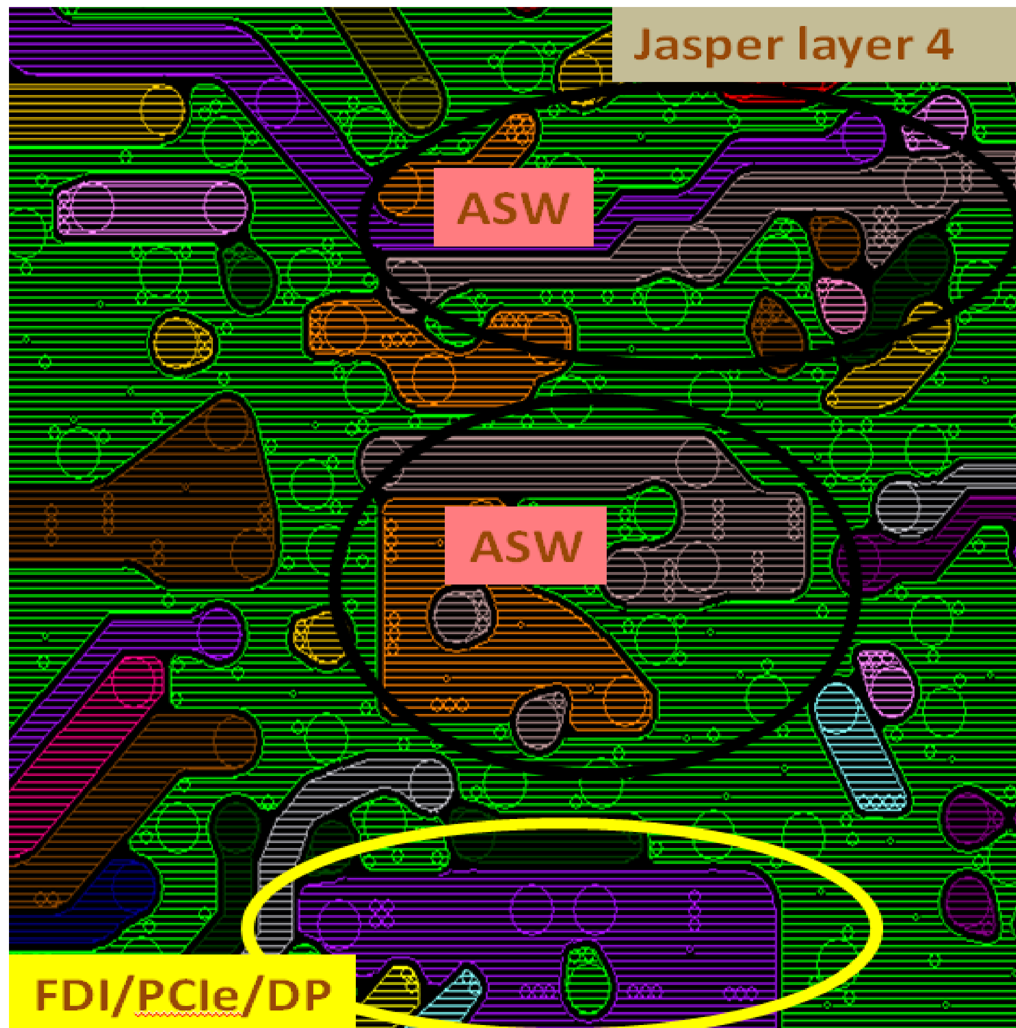


Figure 4.4: Layer 4 of Jasper, showing better lateral connectivity on PCIe/DP/FDI than ASW.

As the visual inspection moves further down to the layer 4 of Jasper (Figure 4.4), the lateral connectivity on PCIe/DP/FDI power rail remains better than ASW. This further strengthens the fact that Cdie efficiency reduction on PCIe/DP/FDI is not caused by poor package routing. The ASW power plane is more segmented than PCIe/DP/FDI on most of the layers; Therefore, hypothesis 1 is invalidated and hypotheses 2 and 3 will be investigated.

4.2.2 Hypothesis 2: Cdie measurement probe location and insufficient biasing

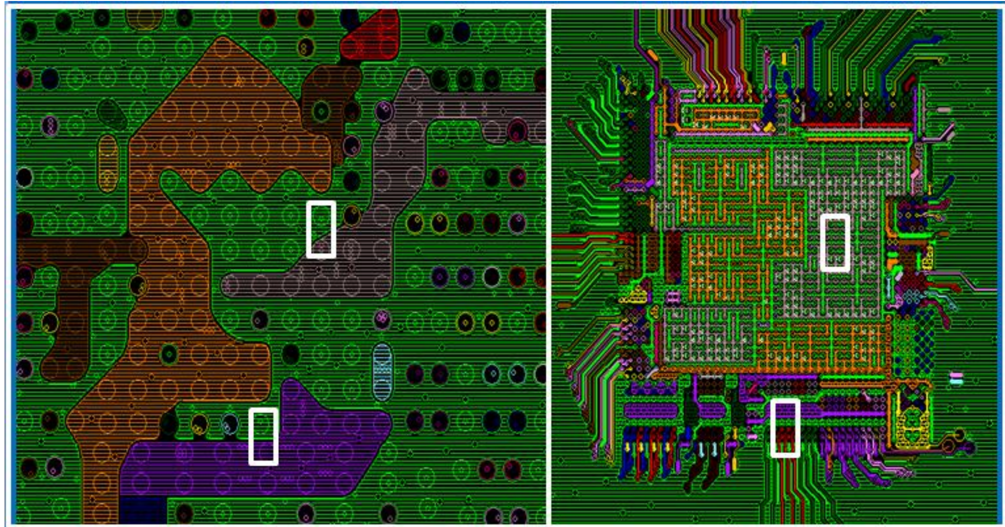


Figure 4.5: (Left) Probe location for ASW and PCIe/DP/FDI on the BGA layer. (Right) Bumps location for ASW and PCIe/DP/FDI.

Both the probe locations for ASW (grey net) and PCIe/DP/FDI (purple net) on the BGA layer are highlighted using rectangular bracket (Figure 4.5 left). Likewise, the corresponding bumps connectivity on the top package layer for both ASW and PCIe/DP/FDI are direct top-down connectivity (Figure 4.5 right). The connectivity on package bottom layer for PCIe/DP/FDI is better in comparison to ASW power plane. ASW is broken into two separated power islands which are able to achieve 93% of the expected Cdie; while PCIe /DP /FDI power rail which is very well connected at bottom layer, achieved only 56% of the original Cdie, it is unlikely that the probe location and biasing point are causing less Cdie to be measured on merged PCIe/DP/FDI power rail. The power supply should be able to penetrate the package without too much IR drop via the inner layer package connection to access biasing the full Cdie on this merged power rail.

4.2.3. Hypothesis 3: Package and Die Routing Discontinuity Study

Both hypotheses 1 and 2 which suspected poor package routing and poor biasing for Cdie measurement are validated and none of these support the reduction of Cdie efficiency on PCIe/DP/FDI. Thus, hypothesis 3 is investigated to look into the possibility of large Rdie with respect to Rpkg; which could potentially prohibit an easy access to neighbouring Cdie.

To accurately extract the Rdie parasitic, it is required that the substrate resistance (Rpkg) be measured and segregated from the existing Cdie measurement. As mentioned earlier in Section 3.2.2.3, the Cdie measurement and extraction method is able to extract Rpkg and Rdie as a lump sum but not able to segregate these two resistance into their absolute number. To accurately comprehend the pitfall, Section 3.2.2.4 which explains the methodology for bare package substrate measurement is used to extract the base package substrate resistance, thus separating the lumpsum Rdie+Rpkg into just Rpkg. The absolute Rdie can then be quantified by subtracting the Rpkg from the lumpsum Rdie+Rpkg number that is derived from the Cdie measurement parasitic.

The first graph (Figure 4.6) shows the total resistance (mOhm) or the Rdie and Rpkg plotted against the Cdie (nF). The trend is a reduced total resistance when Cdie becomes larger. Therefore, if the Cdie is small, a larger Rtotal is expected. A back of envelope equation is derived to associate the trend of Rtotal to Cdie in Eq. 13.

$$y = -0.51x + 35.19 \quad (13)$$

where y denotes the total resistance (Rpkg+Rdie) in mOhm, and x is Cdie (nF)

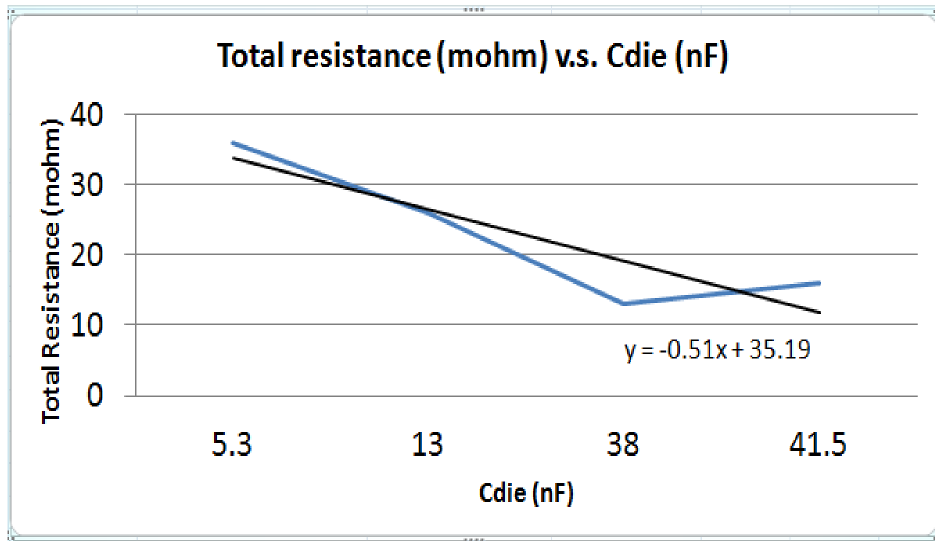


Figure 4.6: A plot of total resistance (mOhm) v.s. Cdie (nF)

The second graph (Figure 4.7) shows the total resistance plotted against the package substrate resistance only, both in mOhm. Total resistance seems high compare to package substrate resistance only. The package substrate resistance hovers around 4 mOhm-10 mOhm and is not proportional to Cdie (nF) increase.

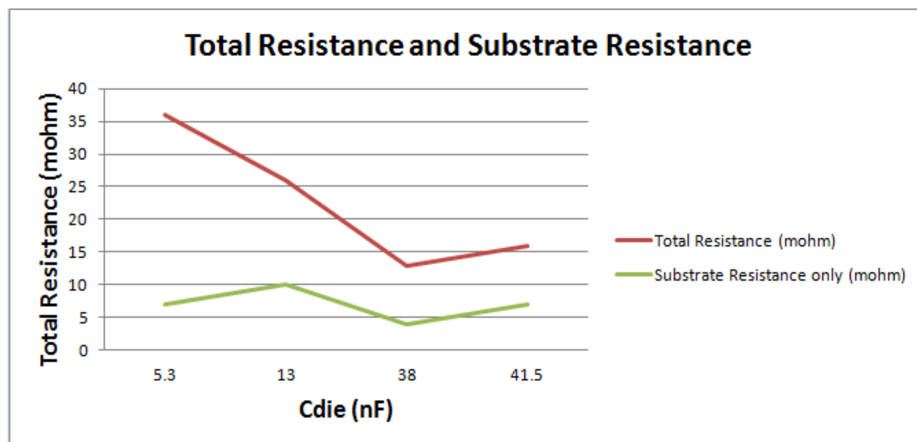


Figure 4.7: A plot of total resistance in comparison with substrate resistance v.s. Cdie.

The third graph plots only the package substrate resistance against Cdie (nF) (Figure 4.8), removing the total resistance which is presented in earlier plot (Figure 4.7). Now, the distinction of package substrate resistance becomes more obvious as it is plotted against the Cdie. A trendline is added and this clearly highlights the outlier package substrate resistances at 13 nF and 41.5 nF. The expected substrate resistance should be decreasing when Cdie increases, which makes sense as the larger Cdie means the buffer area size is larger, and thus, the package substrate area also increases in tandem with increase buffer area size. At 13 nF, the expected package substrate resistance should be measured around 5 mOhm, but it was measured at 10 mOhm. Similarly, the expected package substrate resistance when Cdie is measured at 41.5 nF has bounced off its nominal trend to approximately 7 mOhm, whereas the expected range should lies at 3 mOhm.

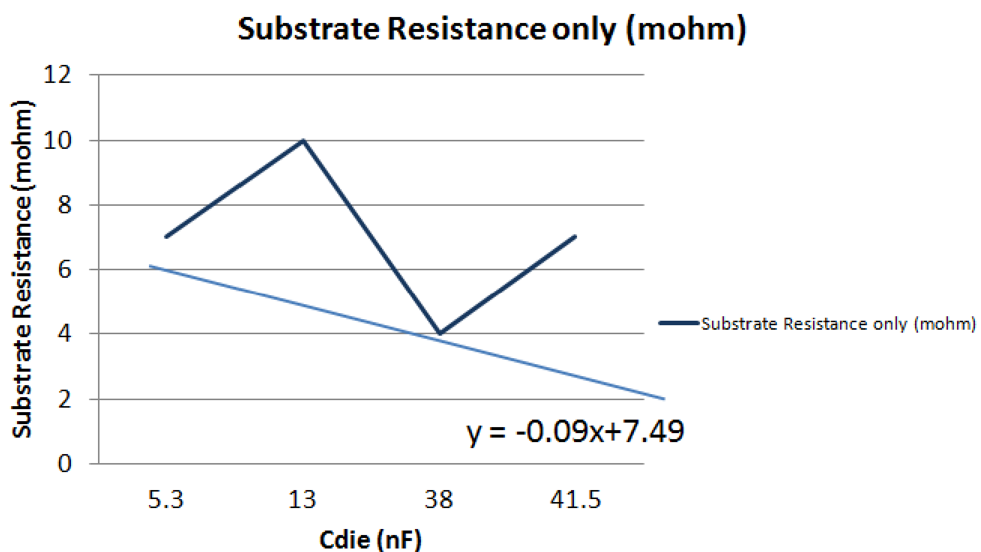


Figure 4.8: A plot of substrate resistance v.s. Cdie.

Further plot of Rdie (mOhm) against Cdie (nF) is studied (Figure 4.9). The Rdie v.s Cdie trendline is added and shows a good agreement whereby Rdie reduces with Cdie increment. This is consistent with expectation as Rdie becomes smaller when buffer area size increases (which also means Cdie increases).

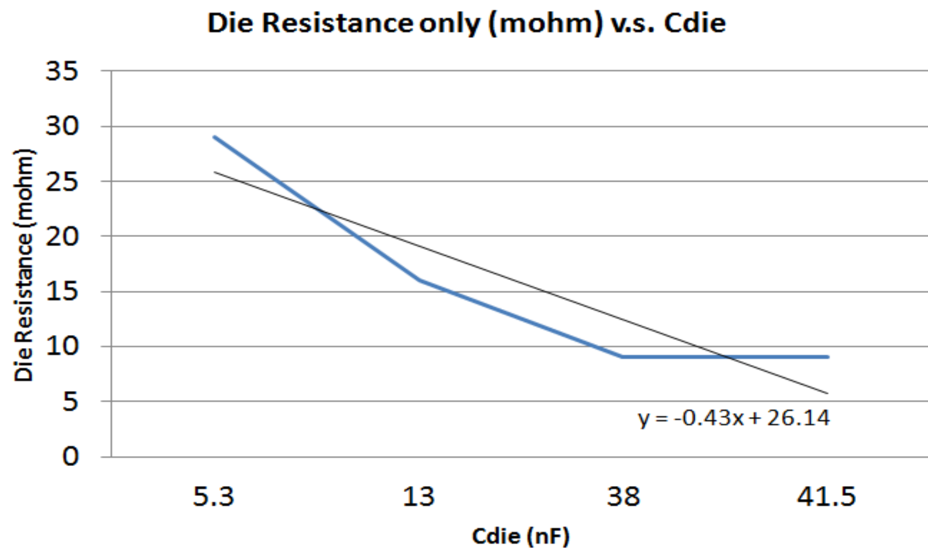


Figure 4.9: A plot of silicon resistance (Rdie) and it's trend line w.r.t Cdie value. Both are in good agreement with each other.

Since the silicon resistance (Rdie) is consistent with the trend line (Figure 4.9) but the package substrate resistance (Rpkg) is not (Figure 4.8), the package substrate resistance v.s. the effective Cdie plot is studied again. This time, the effective Cdie measured on Jasper is added to the plot (Figure 4.10).

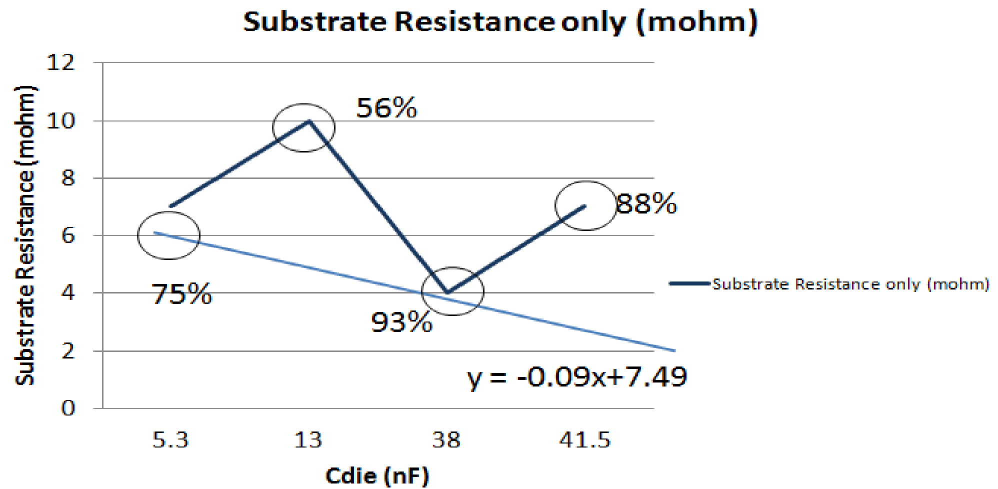


Figure 4.10: Substrate resistance v.s. Cdie plot with effective Cdie measured on Jasper.

Package substrate resistance v.s. Cdie plot when enhanced with the effective Cdie measured (%) on Jasper (Figure 4.10) clearly highlights that the poor effective Cdie measured is largely contributed by large package substrate resistance. Even a 1 mOhm additional package substrate resistance would lower the effective Cdie to 75% (applies to 5.3 nF case). When the package substrate resistance grows from 5 mOhm to 2x higher than expected, at 10 mOhm (applies to 13 nF case), the effective Cdie has reduced to merely 56% of the expected Cdie. However, if the package substrate resistance is kept up with the trend-line expectation at 4 mOhm (applies to 38 nF case), the effective Cdie achieves 93% of the expected value. Similarly, when Cdie is 41.5 nF, the expected package substrate resistance should be hovering around 3 mOhm, but the measured package substrate resistance can only achieved 7 mOhm, thus lowering the effective Cdie to only 88% of the expected range.

4.2.4 Results and findings of power rail merger impact to Cdie efficiency

Hypothesis 3 confirms that the silicon resistance (Rdie) is consistent with Cdie changes, but the package substrate resistance is trending higher than expected when the measured effective Cdie is lower. As such, it is concluded that substrate resistance plays an important role in ensuring the amount of Cdie which could be effectively leveraged across power rails, when merger is implemented. A back of envelope equation (Eq.14) is derived to estimate the package substrate resistance for its corresponding Cdie (nF) such that the design of package substrate can be optimized to maximize the leveraged Cdie on merged power rails package.

$$y = -0.09x + 7.49 \quad (14)$$

where y = substrate resistance (mOhm), x = Cdie (nF)

The investigation of lower Cdie effectiveness is concluded whereby higher than expected substrate resistance is the root-cause of lowering the Cdie leveraging efficiency across power rails. It should remain as one of the important key findings in this research study.

The Cdie measurement data will be used in Chapter 5 when PDN analysis is used to estimate the PDN resonance and help decipher if the SSO noise is induced by PDN's Z(f) or Icc(t)'s excitation. Meanwhile, SSO and eye diagram results on concurrent stress test on all 3 HSSLs will be discussed next.

4.3 PCIe, SATA and USB Stress Noise and EYE Results

Table 4.4: PCIe, SATA and USB noise and eye summary on 5 test packages

Si	Stress Combination									
	A		A + B		A + B + C		A + B + C + D		A + B + C + E	
	Noise (mV)	Eye	Noise (mV)	Eye	Noise (mV)	Eye	Noise (mV)	Eye	Noise (mV)	Eye
PCI-Express (PCIe)										
Lucerne	52.26	passed								
Jasper	57.44	passed	64	passed	64	passed	64.02	passed	72	passed
Jasper (no DSC)	85.16	passed	86.25	passed	88.19	passed	88.28	passed	85.58	passed
Milford Sound (with DSC)	56.83	passed	64	passed	64	passed	64	passed	85	passed
Milford Sound (no DSC)	60.27	passed	64	passed	69.72	passed	70.39	passed	101.4	passed
Serial- ATA (SATA)										
Lucerne	44.93	passed								
Jasper	48	passed	48	passed	48.38	passed	48.58	passed	48	passed
Jasper (no DSC)	51.89	passed	51.98	passed	51.3	passed	53.8	passed	54.05	passed
Milford Sound (with DSC)	52	passed	59	passed	56	passed	60	passed	87.84	passed
Milford Sound (no DSC)	60	passed	60.25	passed	60.31	passed	66.67	passed	94.08	passed
Universal Serial Bus 2.0 (USB) Port 12										
Lucerne	67.39	passed								
Jasper	68.41	passed	60	passed	65.34	passed	76	passed	72.84	passed
Jasper (no DSC)	76	failed	73.08	failed	77.33	failed	78.59	failed	80.69	failed
Milford Sound (with DSC)	60.17	m. passed	60.55	m. passed	60.56	passed	68.89	m. passed	97	passed
Milford Sound (no DSC)	70.23	passed	65	failed	72.03	m. passed	77.58	failed	101.6	failed
A = 5 PCIe		A + B + C = 5 PCIe + 6 SATA + 14 USB				A + B + C + E = 5 PCIe + 6 SATA + 14 USB + PMC				
A+ B = 5 PCIe + 6 SATA		A + B + C + D = 5 PCIe + 6 SATA + 14 USB + SRAM								

Legend:
A =Window+5xPCIe, D = Window+5xPCIe+6xSATA +14xUSB +SRAM10x
B =Window+5xPCIe+6xSATA, E=Window+5xPCIe +6xSATA+14xUSB+PMC
C =Window+ 5xPCIe+6xSATA+14xUSB

The summary of SSO noise and eye data collected for the 3 major interfaces such as PCIe, SATA and USB are tabulated above (Table 4.4); which all belong to the 1.05V high speed serial link (HSSL) interfaces. These HSSLs are transacting at GB/s and at the same time stressed with concurrent traffic.

In the legend (Table 4.4), the column is generally categorized as A, A+B, A+B+C, A+B+C+D and A+B+C+E, where A is Window operating system and 5x or 5 lanes of PCIe are running. This is also defined as the PCIe self-noise of PCIe when all 5 lanes are toggling and transmitting simultaneously. Other HSSLs remains quiet.

Meanwhile, column A+B means the Windows operating system, 5 lanes of PCIe and 6 lanes of SATA are toggling. This is followed by column A+B+C where the condition is similar to A+B but now 14 lanes of USB2 are toggling at the same time as 5 lanes of PCIe and 6 lanes of SATA. This column marks the original research plan, whereby all HSSLs are concurrently stressed to achieve the maximal possible SSO noise on the desktop system, leveraging only on natural aggressor which is available on the PCH die, and no more than that. This way, the redundant aggressors which is usually derived from modelling assumption is eliminated, and no overdesign element is added.

As discussed in Section 3.7.1, addition of aggressors to enhance the existing SSO intensity is possible by introducing core power-ungate noise onto these HSSLs. As some of the test packages have merged plane, the core noise coupling from core into HSSLs access are made easier. Thus, in the subsequent columns of A + B + C + D and A + B + C + E are two added columns where self-scripted aggressors are added to increase the intensity of the SSO noise onto the switching HSSLs. As a reminder, these added core aggressors noise are not part of the standard industrial test, and therefore, any failure observed on the HSSLs resulted from core noise injection needs to be studied separately. For simplicity, A + B + C + D is defined as Operating system + all 3 HSSLs toggling + 10 SRAMs power gate/ungate; and A + B + C + E is defined as Operating system + all 3 HSSLs toggling + PMC power gate/ungate. These additional core aggressor tests are added when stressing

only the HSSLs SSO is insufficient to cause any failure onto the eye specification or peak-to-peak noise target. The addition of core aggressor tests are also added when SSO noise is needed to be stressed beyond +/-5%; regardless of the eye compliance, just to put the system into full blast.

A total of 5 packages are used for data collection, namely Lucerne (baseline), Jasper, Jasper with die-side capacitor (DSC) or on-package capacitor removed, Milford Sound and Milford Sound with DSC removed.

At a glance (Table 4.4), it is found that only one interface has encountered failure (marked in orange colour), while the other two HSSL interfaces remain passing the eye diagram. With this, the concurrent stress setup has successfully shown proof of the severity of the stress level that it is sufficient to bring out the I/O buffer's vulnerability to its break-point. In the standard industrial setup, this problem has escaped the normal validation routine when each test was tested in a single and standalone fashion. For example: Lucerne USB test has passed the normal standalone validation test while failed the concurrent stress test designed for this research study.

From its standalone power plane (Lucerne) to a semi-merged power plane (Jasper) and the fully merged power plane (Milford Sound), PCIe and SATA looks pretty healthy even as the magnitude of noise has increased from ~50 mV to ~100 mV; with and without die-side-capacitor (DSC). The passing of compliance eye test has indicated that either both PCIe and SATA have

ample of margin before the eye specification is violated or the PDN design does not coincide with the sensitive operating frequency of the HSSLs. Thus, the SSO on the PDN barely makes any significant impact to the circuit operations and degrades its electrical performance.

On the other hand, the USB interface has shown eye specification compliant and violation at the same time although the noise magnitude is hovering around 67 mV (Lucerne baseline) and 65 mV (Milford Sound no DSC Column A+B), respectively. Jasper which has the semi-merged power plane and with DSC removed, has failed all eye specification; while Milford Sound (with DSC) which has the most aggressive merger of power plane is able to pass the eye specification across all types of concurrent stress tests from low to high intensity. USB eye specification started failing on Milford Sound when the DSC is removed and especially vulnerable when core noise is introduced. This shows that the failure is intermittent and is inconsistent with the SSO noise magnitude fluctuation. For example, USB eye specification fails at both 65 mV (Milford Sound no DSC, column A + B) and 101 mV (Milford Sound no DSC, column A+B+C+E), while in another occasion, USB eye specification passed at 97 mV (Milford Sound with DSC, column A+B+C+E). In other words, this is the first observation that indicates that the SSO noise magnitude is not the dominant factor that drives the failure of USB eye specification. Further eye failure root-cause will be discussed in Chapter 5.

Section 4.3.1 – Section 4.3.3 will discuss each HSSLs' characteristic in detail, breaking Table 4.4 into smaller table for individual HSSL's noise to eye specification analysis.

4.3.1 Concurrent Stress impact to PCIe interface

The summary of SSO noise and eye data collected for 5 lanes PCIe is shown in Table 4.5. The legend is similar to what is described in Section 4.3 whereby A denotes Windows Operating System and 5 lanes of PCIe toggling.

Table 4.5: PCIe noise and eye summary

Si	Stress Combination									
	A		A+B		A+B+C		A+B+C+D		A+B+C+E	
	Noise (mV)	Eye	Noise (mV)	Eye	Noise (mV)	Eye	Noise (mV)	Eye	Noise (mV)	Eye
PCI-Express										
Standalone Power Rail pkg	52.26	passed								
Jasper	57.44	passed	64	passed	64	passed	64.02	passed	72	passed
Jasper (no DSC)	85.16	passed	86.25	passed	88.19	passed	88.28	passed	85.58	passed
Milford Sound	56.83	passed	64	passed	64	passed	64	passed	85	passed
Milford Sound (no DSC)	60.27	passed	64	passed	69.72	passed	70.39	passed	101.4	passed

With the eye specification passing, the concurrent stress test proceeds with the introduction of more HSSLs such as SATA and USB. In column A+B, 5 lanes of PCIe and 6 lanes of SATA are toggling; Jasper self-noise has increased slightly from 57.44 mV to 64 mV, whereby it continues to hover around 64 mV even when USB is introduced later in column A+B+C. This is expected as Jasper has merged PCIe/DP/DPI as one power rail (Table 4.1), and any additional HSSLs (like SATA and USB) toggling, should only bring in some small amount of coupling noise, and not a substantial increase in noise. At this point, there is no eye specification violation, thus, core noise injection is started in column A+B+C+D; whereby SRAMs power gate/ungate noise is injected into PCIe/DP/FDI power rail. As Jasper has isolated core power rail from PCIe/DP/FDI, the SRAM power gate/ungate noise is not

noticeable for PCIe, thus PCIe noise continues to hover around 64 mV and the eye specification remains passing. The concurrent stress test intensity is increased further by removing SRAM power gate/ungate noise, but using PMC power gate/ungate noise. The result is shown in column A+B+C+E, and this time, the most powerful aggressor introduces some additional noise onto PCIe/DP/FDI merged power rail, bringing an additional 8 mV to PCIe/DP/FDI, from 64 mV to 72 mV. The PCIe eye specification remains passing.

On the other hand, by comparing Jasper and Jasper (no DSC) in column A, the self-noise of PCIe has increased 28 mV with the removal of DSC; from 57 mV to 85 mV. PCIe self-noise has increased from +/-2.5% to +/-4%, but the eye specification remains passing. Further increase of toggling activities from SATA, USB, SRAM or PMC do not add any more noise on PCIe/DP/FDI where the total SSO noise remain at ~86-88 mV. The eye specifications remain passing. From this study, it is observed that PCIe/DP/FDI appreciates having the DSC on the PDN. The removal of DSC adds 28 mV of self-noise almost instantaneously.

Milford Sound has all the common voltage power rails merged as one, which all HSSLs and core are sharing one common PDN. The increment of concurrent tests running on HSSLs and core has an immediate impact on the PCIe now. Looking at Milford Sound, the self-noise of 5 lanes of PCIe started at 56.83 mV, and subsequent increase of 6 lanes SATA (column A+B) and

USB (column A+B+C) and SRAM (column A+B+C+D) only have some increase in SSO noise (to ~64 mV). This is somewhat similar to Jasper. However, there is a sudden increase in SSO when PMC is introduced, where ~20 mV increment is observed when all concurrent tests from HSSLs and PMC power gate/ungate noise are introduced; bringing the total SSO noise to 85 mV. Fortunately, eye specification remains passing. Notice that the 85 mV is similar to the Jasper's (no DSC). This leads to another observation that merged power plane on Milford Sound, although increases the Cdie substantially, could only achieve an on par performance to a semi-merged PCIe/DP/FDI power rail where DSC has been removed. In other words, increasing Cdie does not bring down PCIe noise any further.

Moving on to the last row on Table 4.5 when DSC is removed from Milford Sound, the noise has increased from 56 mV to 60 mV when 5 lanes of PCIe are toggling (column A). Now, this self-noise increment is much smaller compare with Jasper when the DSC is removed; whereby Jasper sees 28 mV increase when DSC is removed, while Milford Sound only see 4 mV increase. This is attributed to the merged power rails and the larger Cdie leveraging impact. As a reminder, Jasper observes ~13 nF of Cdie on PCIe/DP/FDI while Milford Sound observes 80-100 nF of Cdie on its merged rail. In other words, the DSC effect is less significant when a large Cdie is available.

Without the DSC on Milford Sound, further increase in HSSLs stress tests, on SATA and USB pushes the noise higher by 4 mV (Column A+B) or 5

mV (column A+B+C) with each increment in HSSLs. The largest impact of additional SSO happens when PMC power ungate noise is added to the total stress tests, bringing PCIe noise all the way to 101 mV; and arrives at +/-5% mark. At the point, it is the highest SSO noise that the system could generate using all surrounding HSSLs and Core as natural aggressor. Fortunately, eye specification remains passing even-though DSC has been removed.

The key observations are that PCIe has the opportunity to have its DSC removed if there is a huge pool of Cdie being shared, and that it could pass with +/-5% without violation of eye specification.

In summary, PCIe is able to merge with USB and SATA with little noise increase observed, the noise increase is negligibly small at average 1 mV-4 mV range. PCIe noise increased ~31 mV when PMC is introduced on a merged power rail. This shows PCIe is highly sensitive to core noise. This also shows that regardless of having a bigger chunk of Cdie when the power rails are merged as one, it fails to address the core aggressor's noise impact on PCIe.

The result indicates that PCIe is able to merge with I/O power rails (USB and SATA) but dislike merging with Core power rail. Although dislike core noise, PCIe eye do not fail even noise on PCIe pad has achieved 101 mVpp. Next, SATA's SSO behaviour will be examined in detail.

4.3.2 Concurrent Stress Test impact to SATA interface

The summary of SSO noise and eye data collected for 6 lanes SATA is shown in Table 4.6. The legend is slightly different to what is described in Section 4.3 whereby A denotes Windows Operating System and 6 lanes of SATA toggling, but A+B is similar to the previous legend, whereby A+B denotes 5 lanes of PCIe and 6 lanes of SATA are toggling.

Table 4.6: SATA noise and eye summary

Si	Stress Combination									
	A		A+B		A+B+C		A+B+C+D		A+B+C+E	
	Noise (mV)	Eye	Noise (mV)	Eye	Noise (mV)	Eye	Noise (mV)	Eye	Noise (mV)	Eye
Serial- ATA										
Standalone Power Rail pkg	44.93	passed								
Jasper	48	passed	48	passed	48.38	passed	48.58	passed	48	passed
Jasper (no DSC)	51.89	passed	51.98	passed	51.3	passed	53.8	passed	54.05	passed
Milford Sound	52	passed	59	passed	56	passed	60	passed	87.84	passed
Milford Sound (no DSC)	60	passed	60.25	passed	60.31	passed	66.67	passed	94.08	passed

With the eye specification passing, the concurrent stress test proceeds with introducing more HSSLs such as PCIe, USB, SRAM and PMC; Jasper's SATA self-noise has not increased and it stays at 48 mV throughout. No coupling noise from adjacent HSSLs or core is coupled into the SATA standalone power rail. Likewise, Jasper (no DSC) SATA's noise remains similar at ~51 mV -54 mV, even when all aggressors are introduced. This is expected as Jasper's SATA power rail is designed as a single and isolated power rail.

Next, Milford Sound which has all HSSLs and core PDN sharing a common PDN, the increased SSO with increment of concurrent tests running on HSSLs and core has some impact on the SATA now. The self-noise of SATA started at 52 mV, and when 5 lanes of PCIe is added, ~7 mV addition is observed (column A+B). Continue increment of HSSLs like 14 lanes of USB does not really bring SATA's SSO any higher, and it stays at 56 mV. Fairly

negligible impact is observed with addition of SRAM, but only 4 mV addition to 56 mV is observed. Nevertheless, the addition of PMC core aggressor to the concurrent stress test adds an immediate ~28 mV to the 60 mV peak-to-peak noise; bringing the total SSO noise up to 87.85 mV. Fortunately, eye specification remains passing.

The Milford Sound (no DSC) shows that SATA self-noise and SSO noise remains at 60 mV throughout when only HSSLs are toggling. The SATA SSO noise starts seeing increment when either SRAM or PMC is introduced, at 6.6 mV and 34 mV (i.e. 66.67 mV-94.08 mV) respectively. PMC aggressor has pushed the SATA noise all time high to 94 mV, while SATA eye specification remains passing.

Compare all 4 cases of Jasper (with and without DSC), Milford Sound (with and without DSC); addition of aggressors like PCIe and USB to the SATA power rail caused only insignificant increase of SSO at ~1 mV-3 mV. Therefore, SATA is pretty much immune to PCIe and USB noise. The only occasion when SATA noise increases tremendously, is when PMC is introduced to Milford Sound, ~31 mV of SSO is observed on the merged power rail. This shows that SATA is highly sensitive to core noise.

As a result, regardless of having a bigger pool of Cdie with the power rail merge, it fails to address the core aggressor noise's impact on SATA. Therefore, the key learning indicates that SATA is able to merge with I/O

power rails (USB and PCIe) but dislike merging with Core power rail. Although dislike core noise, SATA eye diagram do not failed even when the noise on SATA has achieved 94.08 mVpp.

Next, USB SSO behaviour will be examined in detail.

4.3.3 Concurrent Stress Test impact on USB interface

The summary of SSO noise and eye data collected for 14 lanes USB is shown in Table 4.7. The legend is slightly different from what is described in Section 4.3 whereby A denotes Windows Operating System and 14 lanes of USB toggling, while column A+B denotes 5 lanes of PCIe and 14 lanes of USB are toggling. Column A+B+C denotes 5 lanes of PCIe, 6 lanes SATA and 14 lanes of USB are toggling. Likewise, A+B+C+D and A+B+C+E is exactly similar to the legend described in Section 4.3.

Table 4.7: USB noise and eye summary (port 12 only)

Si	Stress Combination									
	A		A+B		A+B+C		A+B+C+D		A+B+C+E	
	Noise (mV)	Eye	Noise (mV)	Eye	Noise (mV)	Eye	Noise (mV)	Eye	Noise (mV)	Eye
Universal Serial Bus 2.0 (port12)										
Standalone Power Rail pkg	67.39	passed								
Jasper	68.41	passed	60	passed	65.34	passed	76	passed	72.84	passed
Jasper (no DSC)	76	failed	73.08	failed	77.33	failed	78.59	failed	80.69	failed
Milford Sound	60.17	m. passed	60.55	m. passed	60.56	passed	68.89	m. passed	97	passed
Milford Sound (no DSC)	70.23	passed	65	failed	72.03	m. passed	77.58	failed	101.6	failed

On Jasper, USB is merged with Core PDN. The advantage of the merger is that the PDN enjoys sharing a large pool of Cdie. On the other hand, USB is facing the risk of core noise contamination. Surprisingly, Jasper's eye specifications are passed on all different test combinations where its SSO noise are ranging from 68 mV self-noise to 76 mV when multiple concurrent tests are running; and USB is able to withstand the strongest core noise injection when PMC power gate/ungate noise is introduced (Column A+B+C+E). As the eye specification is met on all types of concurrent test, the

DSC is removed from PCIe pads to bring the test intensity one step further. Once the DSC is removed, Jasper (no DSC) eye specification becomes violated. USB on Jasper (no DSC) could not pass any of the concurrent SSO that are injected by neighbouring HSSLs nor SRAM or PMC; although the highest SSO observed is only 80 mV peak-to-peak. Ironically, USB eye specification fails even when self-noise is exercised (column A) and the SSO is only 76 mV, which is similar to the SSO observed when Jasper (column A +B+C+D) is concurrently stressed with all 3 HSSLs and SRAMs power gate/ungate noise. This signifies that SSO noise magnitude is not the key driver that drives eye violation. Although the DSC is located at PCIe pad, and the PCIe PDN and USB PDN is separated on Jasper, the two PDN should not bother each other. Further investigation on root-cause is discussed in Section 4.4.

Meanwhile, Milford Sound which has all the HSSLs and Core PDN merged, inclusive of USB; is examined; first with DSC and later with the DSC removed. In the massively merged PDN, Milford Sounds observes 80-100 nF of Cdie; which is approximately 50% more Cdie than Jasper. The additional Cdie does not contribute much to the SSO reduction, if Jasper and Milford Sound is compared side by side along each test combination from column A to column A +B+C +E. In average, the total SSO noise is reduced by 5 mV-8 mV with 50% more Cdie, but is ineffective when PMC SSO is injected. Jasper observed 73 mV, while Milford Sound is observing 97 mV. This is attributed to the fact that USB on Milford Sound is exposed entirely to the core noise on

the merged PDN without any isolation. Nevertheless, the eye specification on USB2 remains passing throughout the various test combinations; even-though the peak SSO noise has increased to 97 mV. Unlike Jasper (no DSC), the eye specification is violated even when the SSO is only 73 mV. Again, this signifies that the SSO noise is only secondary driver to eye specification violation.

Following Milford Sound's eye specification passing all combination tests, DSC is removed to bring the stress tests intensity one level up. Now, USB eye specification starts to see violations. The overall SSO noise increases slightly compare to when Milford Sound is populated with DSC, this time, USB eye specification is violated when SSO is as low as 65 mV (column A+B), and passed when SSO is 72 mV (column A+B+C), and failed again when SSO is 77 mV and 101 mV (column A +B +C+D and column A+B+C+E) respectively.

To summarize, the PCIe DSC has a calming effect on USB that should not be neglected; as shown in both Milford Sound and Jasper. This shows that USB does not benefit much from the larger pool of Cdie. In other words, USB prefers DSC over Cdie.

Compare all 4 cases of Jasper (with and without DSC), Milford Sound (with and without DSC), addition of aggressors like PCIe and USB to the SATA power rail, the noise increment is negligibly small at ~4 mV-6 mV

max. When the DSC on Milford Sound is removed, the USB self-noise has inevitably increased ~10 mV, but with added aggressors like PCIe and USB, ~4-5 mV is added. USB is pretty much immune to PCIe and SATA added noise with or without DSC.

USB noise surges ~28 mV when PMC noise is introduced on a merged power rail. This shows that USB is highly sensitive to core noise. This also shows that regardless of having a bigger chunk of Cdie with the power rail merged, it fails to address the core aggressor noise's impact on USB.

In short, USB is able to merge with I/O power rails (SATA and PCIe) but dislike merging with Core power rail.

To summarize, Section 4.3.4 compiles the key observations and learning from all the three HSSLs behaviours and plans for next step.

4.3.4 Summary of Observations

I/Os power rails merger on package is recommended for USB, PCIe and SATA. Some HSSLs like PCIe has preferred for more Cdie while other like USB has shown a preference with DSC. Meanwhile SATA does not budge with either additional Cdie or DSC.

The general observations on HSSLs PDN are that they do observe higher magnitude of SSO when merged with Core power rails. Most HSSLs have shown sufficient tolerance of core's SSO to its jitter/eye specification impact than the original believes; where SSO and self-noise must be kept within +/-5%.

PCIe eye diagram does not fail when 100 mV noise is measured on the probe pad. SATA eye diagram does not fail when 94 mV is measured on the probe pad. USB eye diagram do not fail when 97 mV is measured on the probe pad. All these indicate that HSSLs could withstand larger noise than originally believed.

High speed design principle (HSDP) often emphasizes not to merge I/O and Core PDN as one. On Jasper, USB and Core is merged as one PDN and so does Milford Sound. USB does not fail when DSC is present on both Jasper and Milford Sound. Therefore, it is not entirely relevant anymore to always keep to the same HSDP, as there is an opportunity that I/O and core could merge, so long as appropriate decoupling solution is put in place.

Besides USB, SATA and PCIe do not violate any eye specification on Milford Sound even when all HSSLs are toggled simultaneously on top of the introduction of aggressive Core power gate/ungate noise across the one large common PDN on Milford Sound, further strengthen the proof that I/O and Core PDN can be merged as one. The concurrent stress which exercises all I/O and core at the same time is the upmost stressful environment that could be present occasionally, but not all the time. This is because not all HSSLs toggle at the same time, and even if they toggle at the same time, not all lanes toggle simultaneously. SRAMs and PMC are not set to power ungate/gate at every clock cycle as it does not do so in an actual functioning PCH. Besides, these aggressors are actual I/Os and Core which are built on the PCH chip, it is real and natural. No pessimism of stress scenario is introduced by inviting un-related noise-inducer for this research. Thus, the scope of test is already binding all possible worst case simultaneous switching activities possible to put the PCH PDN into the upmost stress possible. If any HSSLs are passing the eye specification under the circumstance, it would be sufficient to conclude that they should be passing eye specification on any other possible occasions bounded by the above concurrent stress combinations.

4.4 USB Eye Specification Failure Investigation

In Section 4.3.3, there has been some unfortunate failure of eye specification on USB occurring on Jasper and Milford Sound especially when the PCIe DSC is removed. When DSC is present, Jasper's USB port12 manages to pass eye specifications on all concurrent stress tests imposed,

regardless of SSO magnitude. Unfortunately, when DSC is removed on Jasper, none of the USB eye specification could pass the combination stress tests. The rather peculiar scenario is that on Jasper, the DSC is located at the PCIe interface, and the PCIe PDN is not merged with USB PDN on Jasper. Likewise, when DSC is presence on Milford Sound, USB is able to pass its eye specification on all different combinations of tests, but when DSC is removed; almost 60% of combination tests failed the USB eye specification. The similarity between Jasper and Milford Sound is that DSC is absent on PCIe pads and this causes USB eye specification to fail more readily. Although Milford Sounds shares PDN with USB, Core and PCIe, it is relevant that PCIe DSC would make an impact on USB eye specification on Milford Sound. However, there is very little relevance on Jasper where DSC removal on PCIe should actually be impacting the USB eye specification. As such, an in-depth investigation to root-cause the failure is done and analysed.

As the eye data is collected on USB worst case port (i.e. port12) on the motherboard system, further investigation is extended to the rest of the ports to see how far the failure is stretched across all ports. The investigation helps to identify if this particular port fails due to domestic issue (connector wear and tear/ weak socket contact / trace length mismatch etc) or is it truly a noise to jitter impact issue. By extending the horizon by looking into other ports and even revisiting the baseline product’s eye, it helps to expand understanding and gives better conclusion. The summary of eye data collected on different test packages is shown in Table 4.8.

Table 4.8: USB eye results on the system of different test packages.

Electrical Validation USB data (I/Os Concurrent + SRAM + PMC aggressor)								Passed	Waived	Failed					
		Port 0	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13
Nominal corner	Lucerne	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Waived	Passed
19" cable	Jasper	Passed	Passed	Passed	Waived	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Failed	Failed
	Milford Sound (SRAM)	Passed	Failed	Failed	Failed	Passed	Passed	Waived	Passed	Waived	Waived	Passed	Passed	Failed	Waived
	Milford Sound (PMC)	Passed	Failed	Failed	Failed	Passed	Passed	Waived	Passed	Waived	Passed	Passed	Passed	Failed	Waived

It is relatively easy to notice that eye specification failure occurs mostly on Port1/Port2/Port3 and Port12 only (Table 4.8). The other ports are passed with good margin. On the motherboard system, USB port1-7 are ports that are routed to the front-end USB connectors with ~4-5" of trace length. Port 8-12 are ports that are routed with long trace length (~14") to the back-panel of the motherboard. This eye data collected for our concurrent test in Table 4.8 uses the longest cable length (19") connecting to the front end connectors while a short 1" cable for back panel connector before it is hooked up with the probes and oscilloscope. As such, the results here can be categorized in two groups, Port0-Port7 are front-end connector with long cable, while port8-12 are back-panel connectors with short cable.

Eye results in Table 4.8 shows that port1-3 are prompted to failure, while port 0, 4, 5, 6, 7 are passing on Milford Sound when core noise are injected. Likewise, port12 eye data is prompted to marginally passing and failing on all Lucerne, Jasper and Milford Sound; whether or not core noise is injected. Not all ports fail in conjunction to core noise injection; and some ports show more vulnerability than others. Since these ports are all powered by one single PDN; it is impossible to isolate the power delivery noise on each individual port from the other; thus, the issue dissection has to be examined

from a different perspective. To understand the issue better, port 2 (9” cable and 19” cable) and port 12 are two ports selected for a detailed examination. The on die noise measured on the USB interface which ranges from 60 mV to 100 mV when different aggressors are introduced is shown in Figure 4.11; while its corresponding jitter behaviour is shown in Figure 4.12. For best interpretation on how SSO noise magnitude would correspond to each jitter increase/decrease, both Figure 4.11 and 4.12 need to be compared side by side for clearer understanding of the potential root-cause. Note that in both figures, the x-axis is labelled in short nomenclature. 5P+6S+14U+SRAM denotes 5 PCIe lanes, 6 SATA lanes, 14 USB lanes (ports) and SRAMs are toggled simultaneously, while 5P+6S+14U+PMC denotes 5 PCIe lanes, 6 SATA lanes, 14 USB lanes (ports) and PMC are toggled simultaneously.

Only one USB on-die noise measurement is plotted for each tests or combination of tests; as the noise is common across all ports regardless of port2 or port12; with 1” or 9” or 19” cables. This is because the power rail on the die is merged and shared across all ports on the package. Nevertheless, there are different jitter data for port2 and port12; with 1” or 9” or 19” cables. Therefore, there are three graphs shown in Figure 4.12; where first graph on the left shows the RMS consecutive jitter relationship to each tests or combination of tests on port 2 with 1” cable, middle graph shows the RMS consecutive jitter relationship to each tests or combination of tests on port 2 with 19” cable, and right graph shows the RMS consecutive jitter on port 12 with 1” cable. Port 2 and port 12 are selected because they are prompted to

failure of eye specification. The major difference between port 2 with 9" cable and port 2 with 19" cable and port 12 with 1" cable is that port 2 with 9" cable is a golden benchmark that passes all tests and combination of tests. Meanwhile, port 2 with 19" cable and port 12 with 1" cable are promoted to failing the eye specification. RMS consecutive jitter is one of the associating parameter that is used to describe eye specification performance.

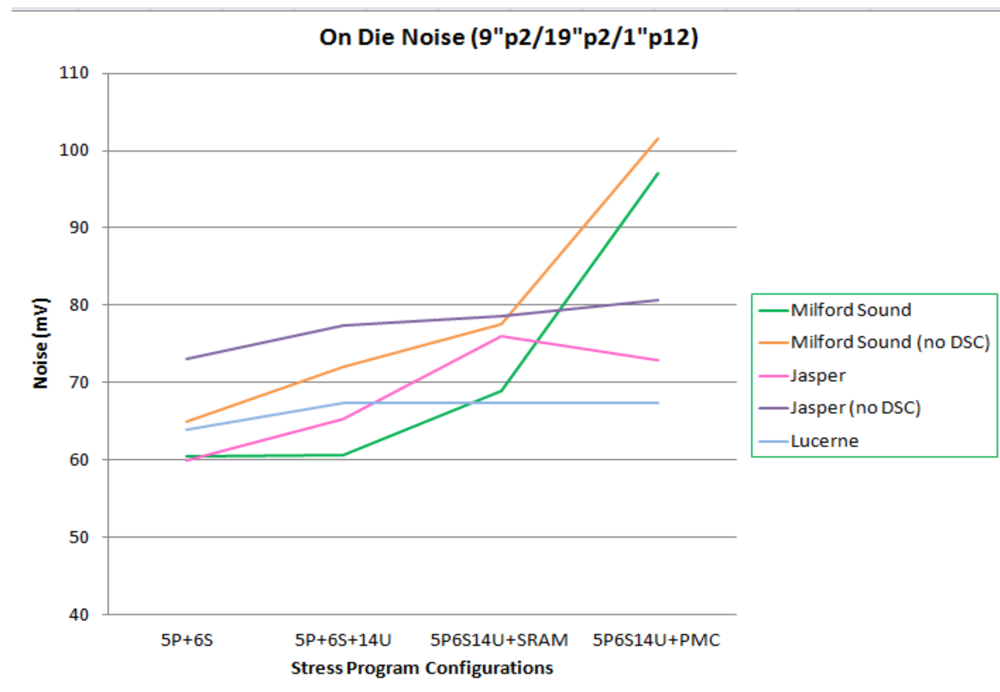


Figure 4.11: On-die noise measurement of USB interface, under different test or combination of tests.

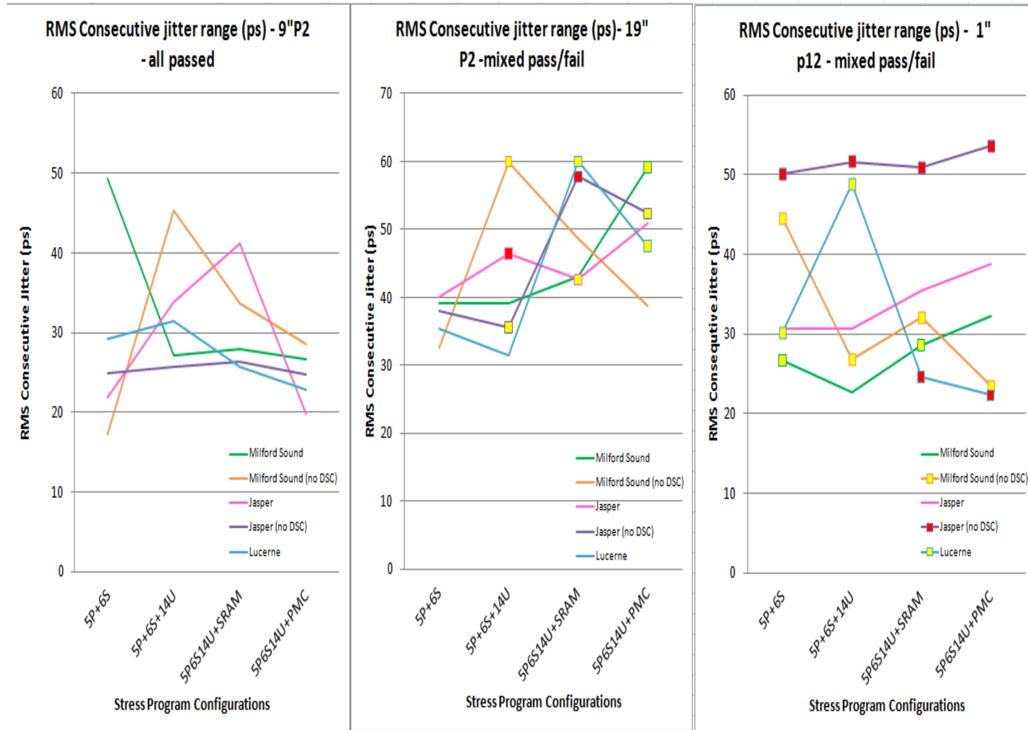


Figure 4.12: (Left) Jitter on port 2 with 9" cable length (Middle) Jitter on Port 2 -19" cable (Right) Jitter on Port 12 – 1" cable (right).

Notice that the RMS consecutive jitter is chosen for eye performance analysis. Apple to apple comparison between all passing eyes on Port2 with 9" cable against Port2 with 19" cable and Port 12 with 1" cable have easily shown the difference between the trend of RMS jitter range on passing and failing examples. Red marker indicates failing eye, yellow marker indicates marginally passing eye and no marker means passing eye. Notice that the left graph which showcases all passing eyes have RMS Consecutive Jitter all falling within 20-50ps range, while the case with Port2 and 19" cable has its RMS consecutive jitter skewed towards 30-60ps range, Meanwhile, the case with Port 12 and 1" cable has shown a clear indication that any RMS consecutive jitters that exceed 50ps or fell below 25ps are definitely a failing eye. These are good graphs that clearly indicate that the USB routing (14" of

trace length) has already achieved its maximum, and the margin to failure can be marked clearly on this graph. On the case of port2 with 19” cable, the two failing eyes are encompassed within many marginally passing eyes which are also residing within the 30-60ps jitter range. It is difficult to conclude the failing margin using this graph. Either these 2 failing eyes are outliers or the marginally passing cases are somewhat lucky escapes. Comparing port 2 and port12, both RMS consecutive jitter trends are different, whereby port2 with 19” cable is obviously able to withstand a higher RMS jitter before failing eye than port12 with 1” cable. This probably can be explained by the cable having better shielding/grounding compare to traces routed on board.

When comparing these RMS jitter data with on-die noise; Jasper (partially merged power plane) Port12 would not allow on-die noise to go beyond 75 mV before the eye fails. Meanwhile, Milford Sound (with and without DSC) on port 12 with 1” cable is a lucky escape whereby the eye did not fail even-though the on-die noise has stretched beyond 75 mV and reaching almost 100 mV; and the RMS jitter is much smaller. Therefore, there is no hard and fast rule to dictate the right specification for peak to peak noise (mV) needed to maintain system health, and on-die noise is definitely not the dominant factor that drives eye failure.

Two more case studies are presented below (Figure 4.13 and 4.14) on PCIe and SATA; showing on die noise and its corresponding Max total-jitter. Both figures show that the maximum total-jitter of PCIe and SATA, is not

correlated with increasing noise. As such, on-die noise is not a dominant factor that drives the max T-j high.

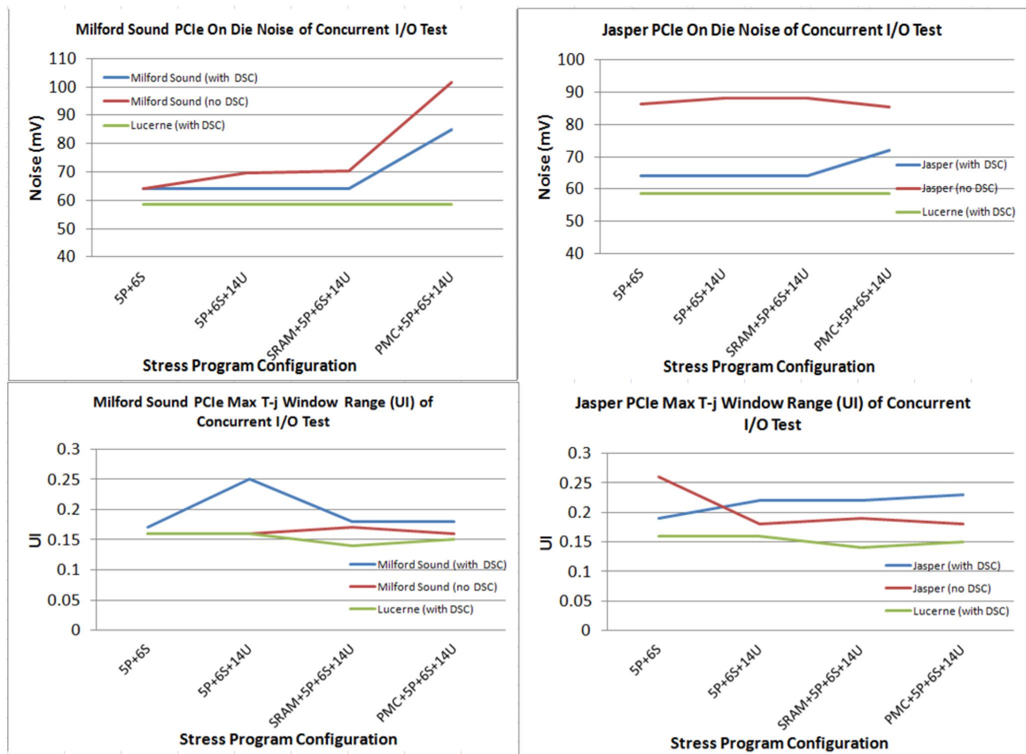


Figure 4.13: (Top) On-die noise of Milford Sound and Jasper for PCIe (Bottom) Maximum total-jitter of PCIe

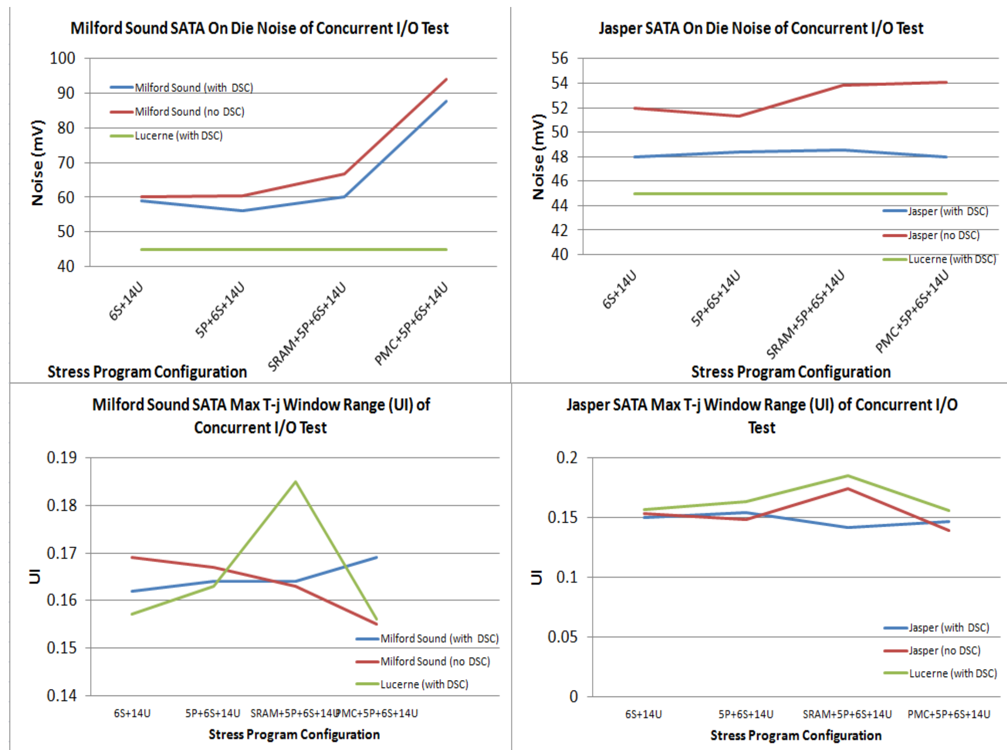


Figure 4.14: (Top) On-die noise of Milford Sound and Jasper for SATA (Bottom) Maximum total-jitter of SATA.

Both Figures 4.13 and 4.14 have shown similar trends whereby the on-die noise are not the dominant factor that drives the Max T-j high, especially on all 4 cases, the highest on-die noise; i.e Milford Sound without DSC and Jasper without DSC where on die noise are highest, are showing Max T-j lower than the other cases.

4.5 Summary

In summary, there is no hard and fast rule to dictate the right specification for peak to peak noise (mV) needed to maintain system health, and on-die noise is definitely not the dominant factor that drives eye failure. Therefore, maintaining +/-5% design target for each power rails to ensure jitter/eye specification is not violated is a belief rather than a need. It becomes

a prospect that this design principle could be ignored so that it provides a relaxation to the existing rules that bound the PDN design. However, the study in this chapter has been focusing only on the overall system performance and on die noise magnitude v.s. jitter relationship. As to what extent the SSO magnitude could be changed or be relaxed such that it still meets the eye specification has not been clearly deciphered yet. A different approach is explored in Chapter 5, whereby noise profile analysis and how much the power delivery network impedance could play a role in affecting the system performance will be studied.

CHAPTER 5

IN-DEPTH INVESTIGATION OF SSO TO EYE SPECIFICATION RELATIONSHIP

5.1 Introduction

Chapter 5 begins with an in-depth noise profile analysis and the study of the power delivery network impedance's role in affecting the system performance. It then explains how the current profile could be extracted by using de-convolution technique to segregate the root-cause of failure to either PDN induced or current induced. As many stress tests will be performed under different conditions, the platform may be stressed under different regressions of random instructions and protocol control. These iterations are difficult to be modelled using pre-silicon assumptions and the de-convolution approach (Section 3.7.4) is best used to derive an exact copy of current profile from the validation vehicle. With the current behaviour of actual system extracted using the de-convolution technique, it eliminates the various pre-silicon assumptions and protocol which are never proven. Finally, this chapter will explain the root-cause of failure by furthering experiments that are customized to trace the break-point.

The objectives are aimed at root-causing of USB eye specification violation and SSO using de-convolution method in order to clearly distinguish if the failure is caused by current excitation or PDN design shortfall and how reverse margining can be used in the investigation to help to bring the failed

HSSL back to health and passing the eye specification. With the failing HSSL recovering from failure, the difference between pass and fail criteria is examined using FFT in the frequency domain, to clearly distinguish the spectral content that exists before and after the HSSL recovers.

After this, a full health screen is conducted across all the 14x USB ports and the margin to failure is re-measured in order to ensure that the recovery is real and not temporary.

Another objective of this chapter is also the key to uncover the truth that if all the HSSLs sensitive frequency of operations could be identified in future study, it inevitably suggested that PDN optimization can now be narrowed down to governing the frequency of interest. PDN engineers can intelligently negotiate with design team to lower the spectral content of the sensitive frequency of operation until a passing mark is achieved, and not adding any extra piece of capacitor on the silicon or package or motherboard, thus greatly reducing product design complexity and congestion of component placement.

The flow of the chapter will start with self-noise analysis, followed by concurrent noise analysis, then discovering the current profile using de-convolution technique. Based on the modelled PDN Z(f), the root cause of SSO noise measured on-die could be identified to as whether it is PDN induced or excitation induced. Once the cause of SSO is identified, say if it is

PDN, PDN impedance profile will be shifted to help moving the failing HSSL out of its failing zone. By comparing the failing and passing characteristic of the HSSL, a conclusion can be drawn to clearly identify what is needed to bring a failing HSSL back to healthy state. Likewise, if the eye specification failure is due to excitation, test scripts that cause the failure will be modified to relax the SSO injection intensity; to bring the failing HSSL back to health. The difference between a pass and fail HSSL's characteristic will be compared and help understand what is the actual gap that drives success or failure. Knowing the gap would help the PDN optimization to do what needs to be done, and not do what is believed to be needed to be done.

5.2 Individual HSSLs Self Noise Profile Analysis

This section describes self-noise analysis, when the HSSL is toggling without any interference from other interfaces; to quantify the noise characteristic in the frequency domain. Having the noise FFT profile at hand, the next step is to look at current FFT profile. The objective of deriving the noise and current FFT are to help in deciding if the noise is current induced or PDN induced. As the process of generating FFT profile is similar, two HSSLs are chosen for detail explanation. The FFT profile extraction will be repeated on all HSSLs on analysing the self-noise as well as coupling noise. Table 5.1 captures the summary of the noise spectrum observed before proceed to Current FFT profile analysis in Section 5.3.

5.2.1 USB Self Noise Profile Analysis

Figure 5.1: USB 14x ports self-noise and FFT plot.

The USB self-noise and FFT plot for all 14 ports USB operating at its full bandwidth is shown in Figure 5.1. This is the on-die noise that is probed on the package probe pad on the outer edge of the silicon where the USB I/O circuits are located. The FFT plot indicates strong clock current at 125 MHz, 250 MHz, 500 MHz, 625 MHz, 750 MHz, 1 GHz, 1.5 GHz, 2.5 GHz, 3.75 GHz and 5 GHz. All the clock currents are above 100 MHz.

To understand how much noise the PDN is observing, this noise is band-pass filtered to within 10 MHz-100 MHz. This frequency range where package PDN lies within and any noise noted in this region is likely a contribution of PDN resonance. In the USB noise analysis (Figure 5.2), the 10 MHz-100 MHz noise is contributing to only 10% of the total noise. Thus, it is

decided that package PDN has very little influence to the overall USB self-noise and majority of the noise is current excited. Likewise, high-pass filtered USB noise beyond 100 MHz is showing that approximately 90% of total USB self-noise is contributed by current excitation. (Figure 5.3)

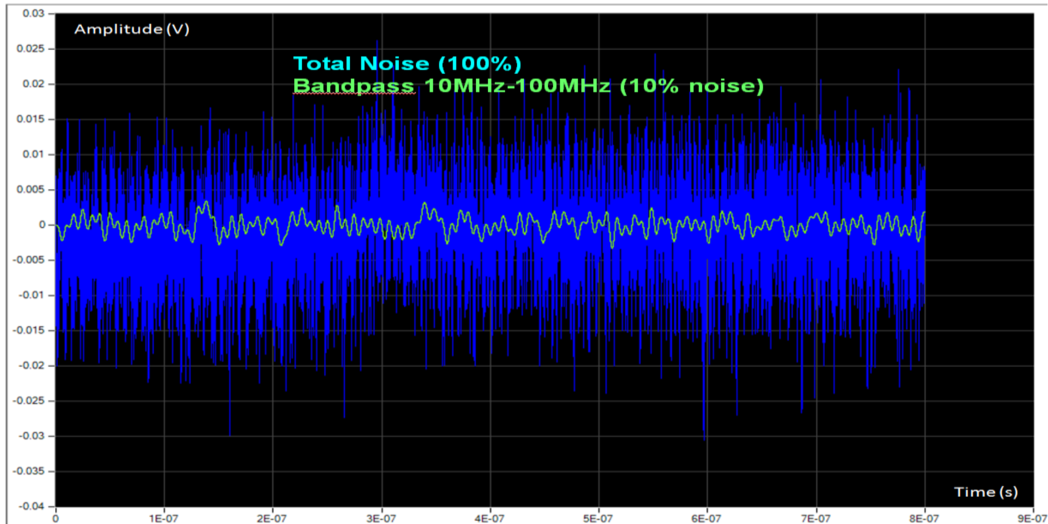


Figure 5.2: USB bandpass 10 MHz-100 MHz contributes ~10% of total noise

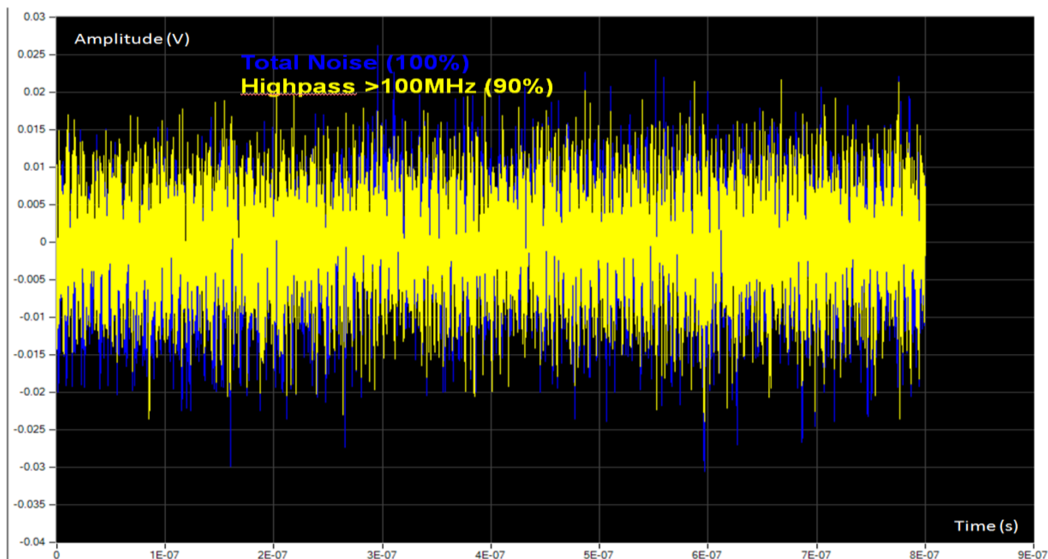


Figure 5.3: USB high-pass 100 MHz noise contributes ~90% of total noise.

Further breakdown of the USB total noise is shown in Figure 5.4. Out of the 90% noise which resides beyond 100 MHz, 60% of the total noise is

contributed by activities above 1 GHz, while only 35% of the total noise is contributed by activities above 3 GHz.

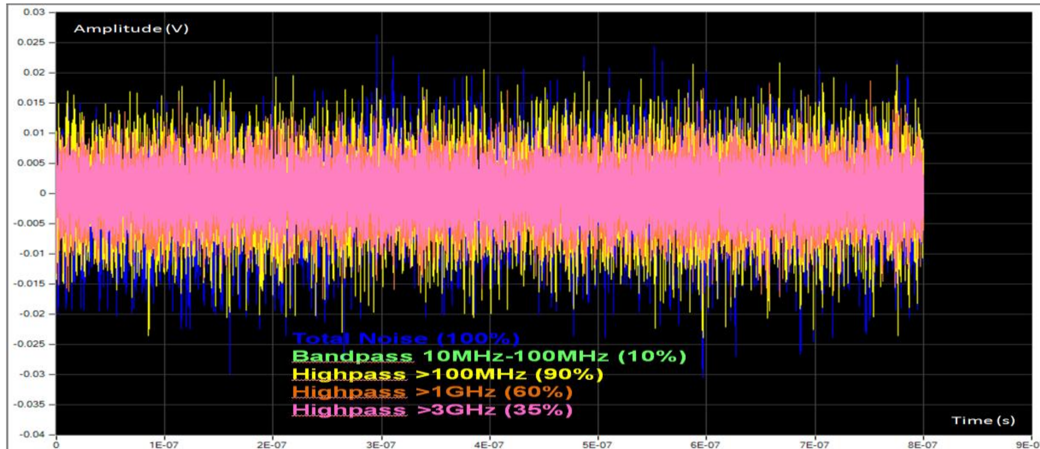


Figure 5.4: USB noise breakdown for different pass-band

Most of the clock current contributed by the USB circuits operates above 100 MHz, i.e. starting at 125 MHz. Furthermore, ~90% of the noise magnitude is above 100MHz and only 10% resides at 10 MHz-100 MHz. This data illustrates the fact that ~90% of noise is USB circuits induced, or current excited. PDN has only 10% contribution to the overall USB peak-to-peak noise.

A second example is shown using PCIe self-noise profile (Section 5.2.2)

5.2.2 PCIe Self-Noise Profile Analysis

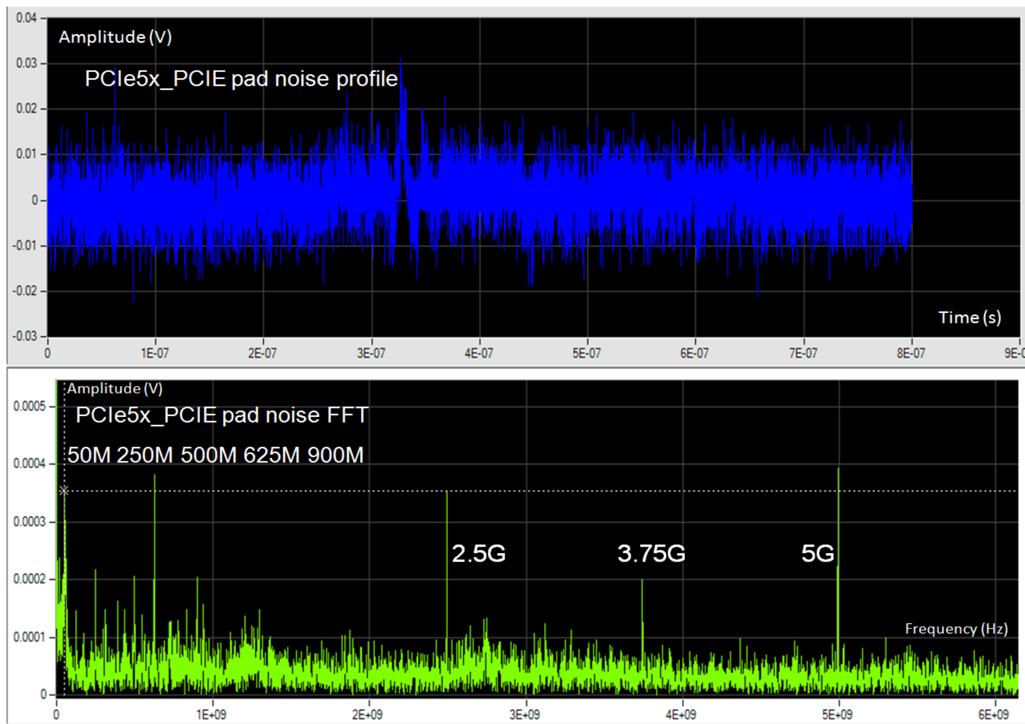


Figure 5.5: PCIe 5x ports self-noise and FFT plot.

The PCIe self-noise and FFT plot for all 5 ports operating at its full bandwidth is shown in Figure 5.5. This is the on-die noise that is probed on the package probe pad on the outer edge of the silicon where the PCIE/DP/FDI I/O circuits are located. The FFT plot indicates strong clock current at 250 MHz, 500 MHz, 625 MHz, 900 MHz, 2.5 GHz, 3.75 GHz and 5 GHz. All the clock currents are above 100 MHz.

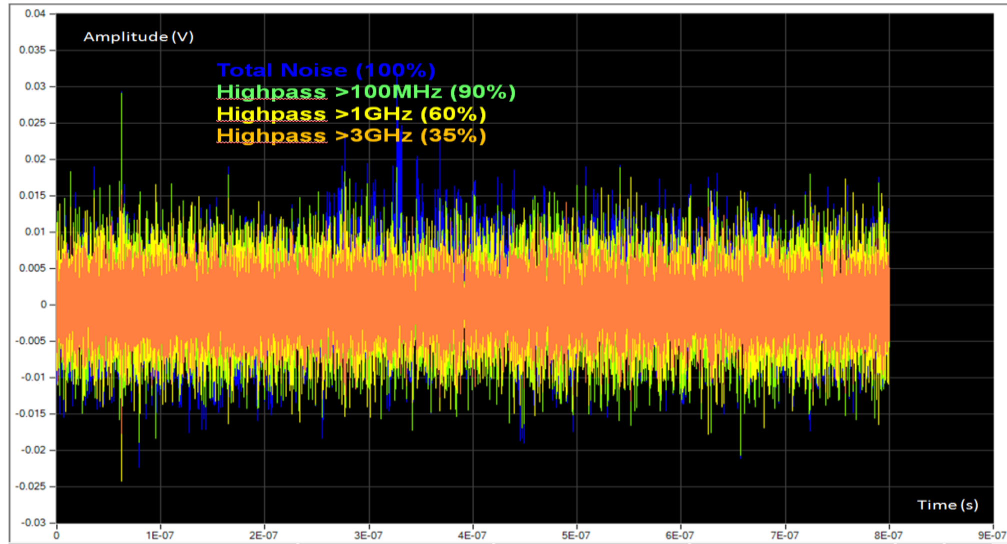


Figure 5.6: PCIe noise breakdown for different pass-bands.

The breakdown of PCIe self-noise when all 5 ports are stressed at full bandwidth is shown in Figure 5.6. Most of the clock current contributed by the PCIe circuits operates above 100 MHz, i.e. starting at 250 MHz. Furthermore, ~90% of the noise magnitude is above 100 MHz and only 10% resides at 10 MHz-100 MHz. This data illustrates the fact that ~90% of PCIe self-noise is PCIe clock current induced while ~10% of the total noise is PDN induced.

The next section (Section 5.2.3) focuses on concurrent stress test noise profile analysis. One example will be described in detail, and the rest of the analysis will be summarized in Table 5.1.

5.2.3 PCIe5x_SATA6x Concurrent Stress Noise Profile

Figure 5.7: PCIe and SATA concurrent noise and FFT plot

The PCIe and SATA concurrent noise and FFT plot for all 5+6 ports operating at its full bandwidth are shown in Figure 5.7. This is the on-die noise that is probed on the package probe pad on the outer edge of the silicon where the USB I/O circuits are located. The FFT plot indicate strong clock current at 125 MHz, 250 MHz, 500 MHz, 625 MHz, 830 MHz, 2.5 GHz, 3.75 GHz and 5 GHz. All the clock currents are above 100MHz. The reason why PCIe and SATA concurrent noise and FFT plot are probed on USB probe pad is that this data will be used for diagnostic of USB eye specification failure in Section 5.3.

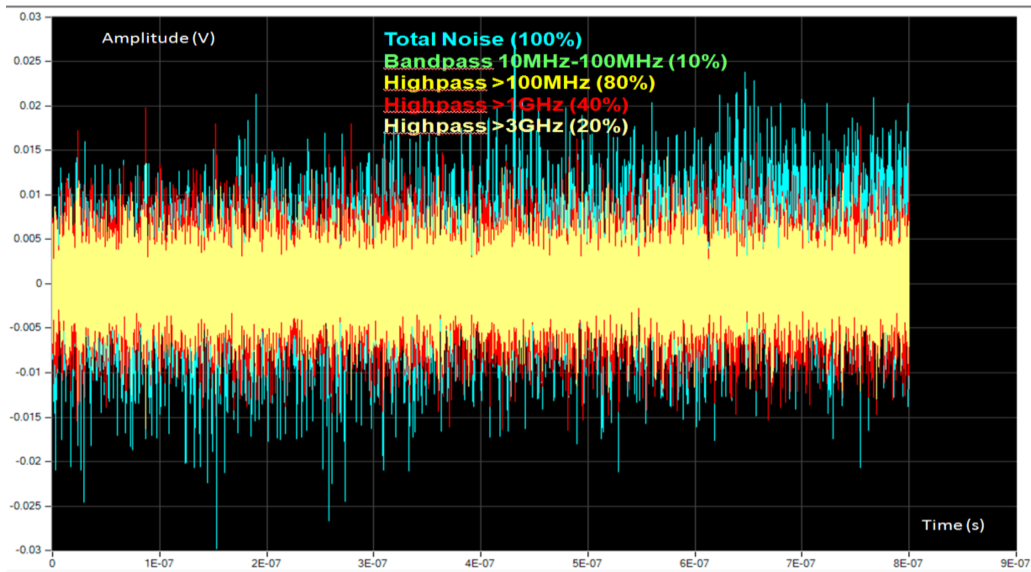


Figure 5.8: PCIe and SATA concurrent noise breakdown for different pass-bands

The breakdown of PCIe and SATA concurrent noise when all 5+6 ports are stressed at full bandwidth is shown in Figure 5.8. Most of the clock current contributed by the I/O circuits operate above 100 MHz, i.e. starting at 125 MHz. Furthermore, ~80% of the noise magnitude is above 100 MHz and only 10% resides at 10 MHz-100 MHz. This indicates that ~80% of noise magnitude is die activity induced, while ~10% is PDN induced.

Table 5.1: Summary of self-noise and concurrent stress noise FFT for Milford Sound on USB pad

	Compilation of FFT of noise profile	20M	21.3M	27.5M	33.7M	125M	145M	250M	375M	480M	500M	625M	750M	2.5G	3.75G	5G
Milford Sound Self-Noise with PCIE DSC	PCIe 5x							•			•	•		•	•	•
	SATA 6x					•		•				•		•	•	•
	USB 14x					•		•			•	•	•	•	•	•
	SRAM 10x					•	•	•	•		•	•				
	PMC			•		•	•	•	•		•	•				
Milford Sound Self-Noise without PCIE DSC	PCIe 5x		•					•			•	•		•	•	•
	SATA 6x		•	•	•	•		•				•		•		•
	USB 14x	•				•		•		•	•	•	•	•	•	•
	SRAM 10x					•		•	•		•	•	•	•	•	•
	PMC				•	•		•	•		•	•		•	•	•
Milford Sound Concurrent Noise with PCIE DSC on USB pad	PCIe 5x + SATA 6x					•		•			•	•		•	•	•
	PCIe 5x + SATA 6x + USB 14x					•		•		•	•	•	•	•	•	•
	PCIe 5x + SATA 6x + USB 14x + SRAM 10x			•		•		•			•		•	•	•	•
	PCIe 5x + SATA 6x + USB 14x + PMC			•		•		•			•			•	•	•
Milford Sound Concurrent Noise without PCIE DSC on USB pad	PCIe5x					•		•			•	•	•	•		•
	PCIe 5x + SATA 6x					•		•			•	•	•	•		•
	PCIe 5x + SATA 6x + USB 14x	•			•	•		•		•	•	•		•		•
	PCIe 5x + SATA 6x + USB 14x + SRAM 10x					•		•		•	•	•		•		•
	PCIe 5x + SATA 6x + USB 14x + PMC		•			•		•			•	•	•	•		•

Milford Sound FFT spectrum for self-noise on USB probe pad with and without PCIe DSC is shown in Table 5.1. Looking at the noise spectrum, most noise is attributed by clocks current which are exciting above 100 MHz, i.e. 125 MHz, 250 MHz and 500 MHz etc. Only when SRAM and PMC are introduced and DSC is removed, the noise spectra of 20 MHz-33.7 MHz appear.

Table 5.2: Summary of self and concurrent noise's composition on Milford Sound

	Compilation of FFT of noise profile	10M-100M	>100M	>1G	>3G
Milford Sound Self-Excitation without PCIE DSC	PCIe 5x	10%	90%	60%	35%
	SATA 6x	10%	90%	60%	35%
	USB 14x	10%	90%	60%	35%
	SRAM 10x	20%	90%	20%	15%
	PMC	65%	55%	20%	15%
Milford Sound Concurrent-Excitation without PCIE DSC	PCIe 5x + SATA 6x	10%	80%	40%	20%
	Pcie 5x + SATA 6x + USB 14x	10%	80%	60%	35%
	PCIe 5x + SATA 6x + USB 14x + SRAM 10x	40%	75%	60%	40%
	PCIe 5x + SATA 6x + USB 14x + PMC	60%	80%	30%	10%

The self-noise and concurrent noise compositions on Milford Sound are summarized in Table 5.2. The data has highlighted that most of the self-noise content (90%) of HSSLs is above 100 MHz (circuit and core operating frequency) and only 10% is below 100 MHz (PDN's bounded); except the case when SRAM and PMC are introduced.

In order to understand where the ~20 MHz-33.7 MHz noise come from, a deep dive into current profile and power delivery network analysis will be discussed in Section 5.3 and 5.4.

5.3 Current Profile Analysis

The following sections focus on current profile analysis; to confirm if the noise sources of ~27.5 MHz-33.7 MHz components are part of the current excitation excited by the stress software interacting with the PDN peak resonance. The current profile can be reconstructed by using de-convolution approach as explained in Section 3.7.4.

Two reconstructed current profiles are shown in Figure 5.9 and 5.10; together with its FFT spectrum showcasing the ~27.5 MHz-33.7 MHz spectra when PMC is included and excluded in the concurrent stress test. Each figure has two graphs, where the reconstructed current profile in time domain is plotted on the top, and the FFT spectrum of the current profile is shown at the bottom.

The reconstructed current profile and its FFT spectrum are plotted by de-convoluting the noise measured on Milford Sound on USB probe pad; when the concurrent stress tests combining PCIe, SATA, USB and PMC. The de-convolution technique is able to isolate the current profile from the PDN network, thus, separating the two as individual graphs, allowing a clear analysis of what frequency spectrum would exist in the current profile without the influence of PDN resonance (Figure 5.9).

Likewise, another reconstructed current profile and its FFT spectrum; (Figure 5.10); which noise is measured on the same package and same probe

location. However, the concurrent stress tests excluded PMC this time; i.e. only PCIe, SATA and USB stress tests are toggled. By comparing these 2 figures side by side, it is easy to observe that 27.5 MHz spectra is missing when PMC is excluded, thus confirms the PMC stress software is key to inducing the 27.5 MHz noise component.

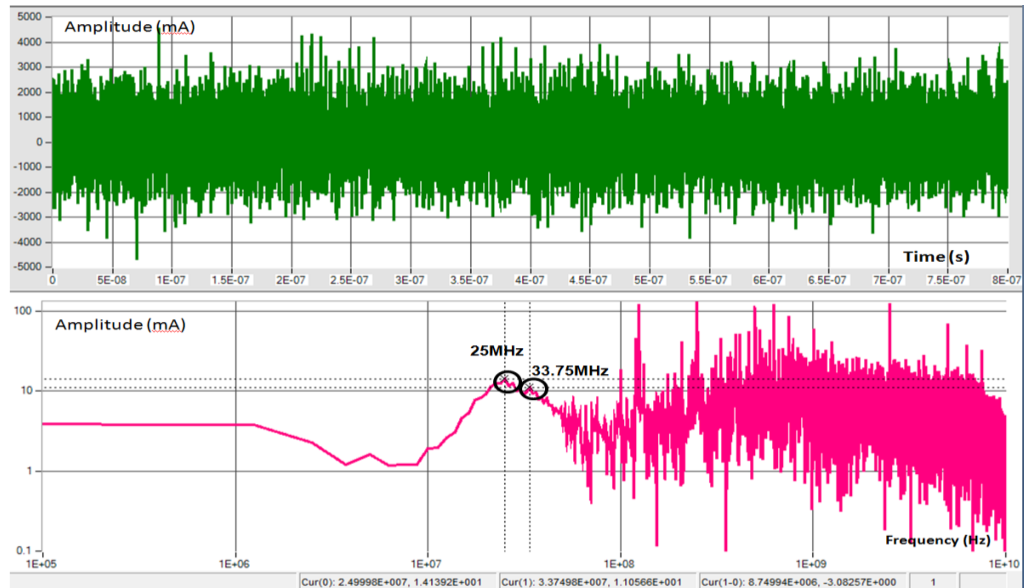


Figure 5.9: FFT of Milford Sound Concurrent stress test with PMC shows 25 MHz and 33.75 MHz spectrum in its current profile.

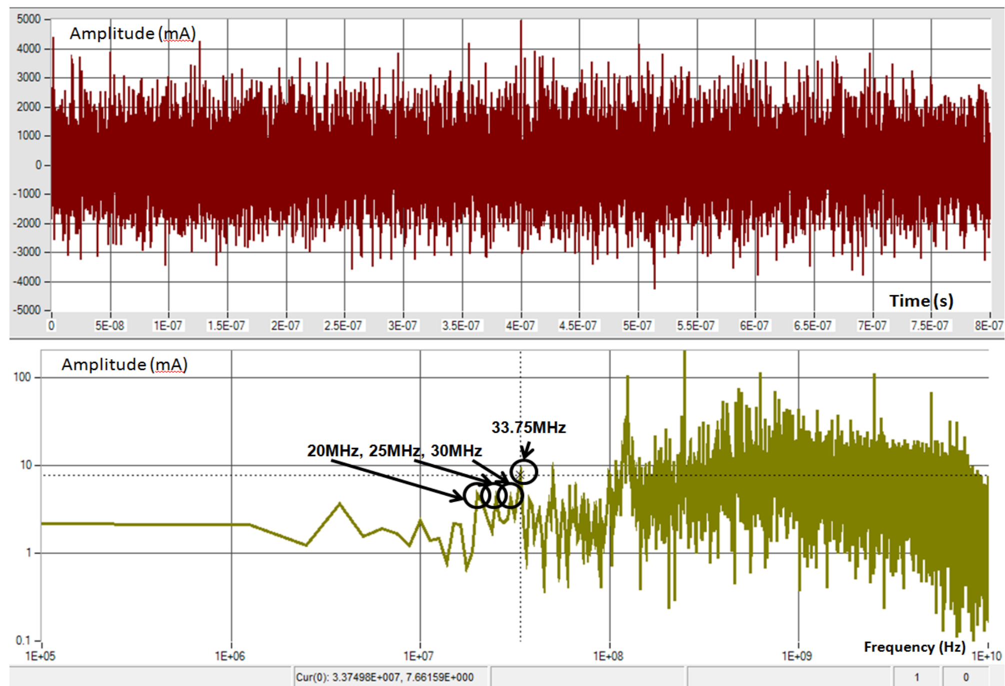


Figure 5.10 : FFT of Milford Sound Concurrent stress test without PMC shows strong 20 MHz -33.75 Mhz spectrum, but a missing 27.5 MHz.

Similar exercises of reconstruction of current profiles are carried out on Milford Sound self-noise and concurrent stress noise without PCIe DSC. The reason why Milford Sound without DSC noise profiles are selected for current profile reconstruction is because, all eye specifications which are violated (Table 4.4); are attributed mostly when PCIe DSC is removed; and PMC is running. These data are prepared for detail USB eye specification violation investigation. The details of the investigation discussion will be presented in Section 5.5 when all noise profile, current profile and PDN resonance analysis are completed in Section 5.2, 5.3 and 5.4 respectively.

The summary of current FFT spectrum for Milford Sound on USB pad for its self-induced activities and concurrent stress tests are shown in Table 5.3. The data clearly highlighted the fact that most current excitation FFT of

HSSLs are above 100 MHz, and the frequency contents which fall between 27.5 MHz-33.7 MHz occurs only when SRAM and PMC are presence; which confirms with the findings in section 5.2.

Table 5.3: Summary of current FFT spectrum for Milford Sound on USB pad

	Compilation of FFT of current profile	20M	21.3M	25M	27.5M	33.7M	125M	145M		250M	375M	480M	500M	625M	750M	2.5G	3.75G	5G
Milford Sound Self-Excitation without PCIE DSC	PCIe 5x									•			•	•		•	•	•
	SATA 6x						•			•				•		•		•
	USB 14x						•			•			•	•	•	•		•
	SRAM 10x					•	•	•		•	•		•	•				
	PMC				•	•	•	•		•	•		•	•				
Milford Sound Concurrent-Excitation without PCIE DSC	PCIe 5x						•			•			•	•	•	•		•
	PCIe 5x + SATA 6x						•			•			•	•	•	•		•
	Pcie 5x + SATA 6x + USB 14x					•	•			•			•	•		•		•
	PCIe 5x + SATA 6x + USB 14x + SRAM 10x					•	•		•	•		•	•	•	•	•		•
	PCIe 5x + SATA 6x + USB 14x + PMC				•	•	•			•			•	•	•	•		•

To summarize the FFT findings in Section 5.2 and Section 5.3, a compilation table of overall noise and current FFT spectrum for Milford Sound on USB pad is shown below. (Table 5.4)

Table 5.4: Compilation of noise and current FFT spectrum for MilfordSound on USB pad

	Compilation of FFT of noise profile	20M	21.3M	25M	27.5M	33.7M	125M	145M	240M	250M	375M	480M	500M	625M	750M	2.5G	3.75G	5G
Milford Sound Self-Noise with PCIE DSC	PCIe 5x									•			•	•		•	•	•
	SATA 6x						•			•				•		•	•	•
	USB 14x						•			•			•	•	•	•	•	•
	SRAM 10x						•	•		•	•		•	•				
	PMC				•		•	•		•	•		•	•				
Milford Sound Self-Noise without PCIE DSC	PCIe 5x		•							•			•	•		•	•	•
	SATA 6x		•		•	•	•			•				•		•		•
	USB 14x	•					•			•		•	•	•	•	•	•	•
	SRAM 10x						•			•	•		•	•	•	•	•	•
	PMC					•	•			•	•		•	•		•	•	•
Milford Sound Concurrent Noise with PCIE DSC on USB pad	PCIe 5x + SATA 6x						•			•			•	•		•	•	•
	PCIe 5x + SATA 6x + USB 14x						•			•		•	•	•	•	•	•	•
	PCIe 5x + SATA 6x + USB 14x + SRAM 10x				•		•			•			•		•	•	•	•
	PCIe 5x + SATA 6x + USB 14x + PMC				•		•			•			•			•	•	•
Milford Sound Concurrent Noise without PCIE DSC on USB pad	PCIe5x						•			•			•	•	•	•		•
	PCIe 5x + SATA 6x						•			•			•	•	•	•		•
	PCIe 5x + SATA 6x + USB 14x	•				•	•			•		•	•	•		•		•
	PCIe 5x + SATA 6x + USB 14x + SRAM 10x						•			•		•	•	•		•		•
	PCIe 5x + SATA 6x + USB 14x + PMC		•				•			•			•	•	•	•		•
	Compilation of FFT of current profile	20M	21.3M	25M	27.5M	33.7M	125M	145M		250M	375M	480M	500M	625M	750M	2.5G	3.75G	5G
Milford Sound Self-Excitation without PCIE DSC	PCIe 5x									•			•	•		•	•	•
	SATA 6x						•			•				•		•		•
	USB 14x						•			•			•	•	•	•		•
	SRAM 10x					•	•	•		•	•		•	•				
	PMC				•	•	•	•		•	•		•	•				
Milford Sound Concurrent-Excitation without PCIE DSC	PCIe 5x						•			•			•	•	•	•		•
	PCIe 5x + SATA 6x						•			•			•	•	•	•		•
	Pcie 5x + SATA 6x + USB 14x					•	•			•			•	•		•		•
	PCIe 5x + SATA 6x + USB 14x + SRAM 10x					•	•		•	•		•	•	•	•	•		•
	PCIe 5x + SATA 6x + USB 14x + PMC				•	•	•			•			•	•	•	•		•

5.4 Power Delivery Network (PDN) Analysis on Merged and unmerged packages

In order to find the root-cause of the noise spectral and determine if the noise is PDN induced or circuit current induced, the three packages PDN Z(f) profiles are simulated and studied. Figure 5.11 shows the overlapping impedance profile of the three packages, comparing its characteristic before and after power rails merger.

The Y-axis denotes the impedance (Ohm) and x-axis denotes frequency (Hz). Noticed that Jasper; which merges I/O interfaces with I/O interfaces power rails has higher impedance (from 5 MHz-54 MHz) than Lucerne (no merger) and Milford Sound which has all digital core and I/O Interfaces power rails merged as one has the lowest impedance profile. Since all the consolidated power rails' on-die-capacitance (Cdie) are now sharing amongst each other on Milford Sound, the peak resonance has also shifted left for ~40 MHz. This shift has shrunk its impedance at 100 MHz from 304 mOhm to 28 mOhm (~11x reduction), creating a reasonably small impedance profile for all clocks running above 100 MHz on the chip. The impedance profiles (Figure 5.11) are plotted with DSC populated.

As such, the power rail merger on Milford Sound has effectively shifted the PDN resonance to below 100 MHz, and away from the circuit and core operating clock current spectrum, improving the PDN performance by buying its extra margin.

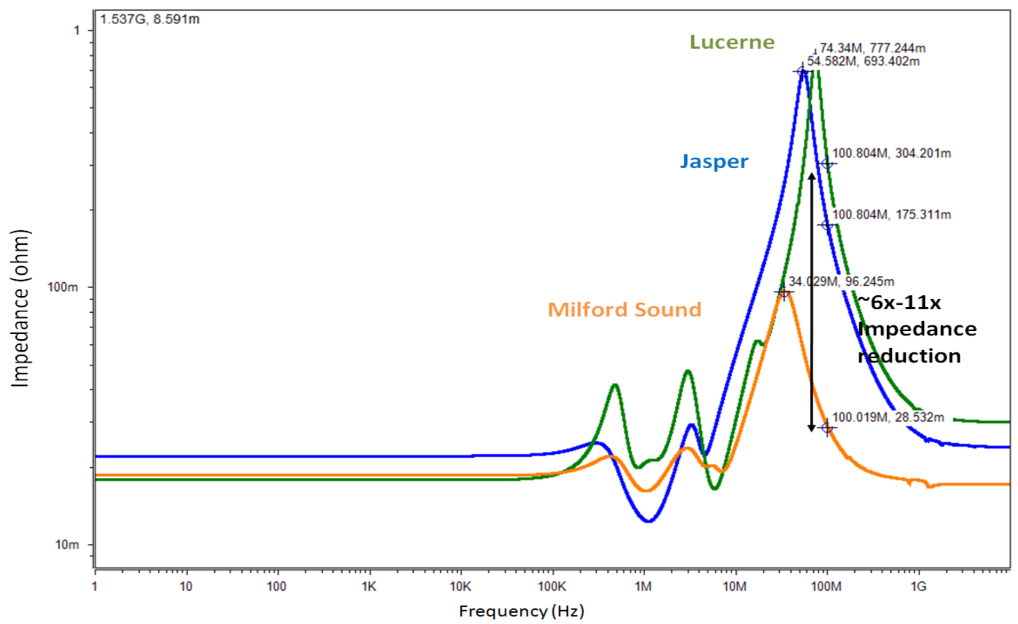


Figure 5.11: The impedance profile of 3 packages before and after merger.

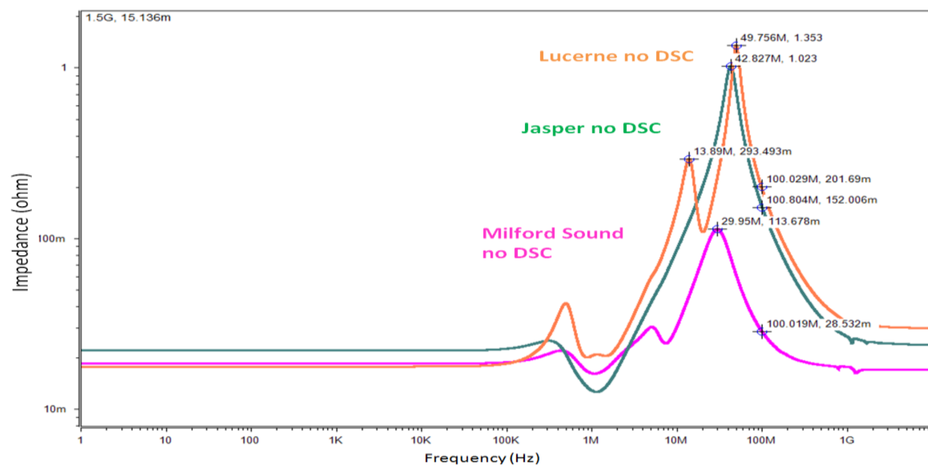


Figure 5.12: The impedance profile 3 packages when DSC is removed.

The reason why Jasper is having a higher impedance profile (Table 5.11) at the mid-frequencies is due to the presence of DSC. The impedance profile plotted when all the DSC on all three packages are removed is shown in Figure 5.12. It was clear that Lucerne had the worst impedance profile compare among all three packages. In other words, the DSC has helped tremendously on the standalone power rail package when Cdie is the smallest, besides the fact that the number of plated through hole via (PTHs) and power

plane area size are constrained. When power rails are merged on the package, the DSC impact becomes less significant.

When DSC is removed, the lower frequency noise becomes more apparent for both self-noise and concurrent noise case studies (Table 5.1). Most of the frequencies which are 35 MHz and below are suppressed by DSC. The many noise spectra appear after DSC removal showcases the importance of DSC helping to damp the noise at the lower frequency. Although the DSC is only placed on PCIe pad on the package, the effect is tremendous on a merged power plane package, where the DSC is leveraged across the many different I/O circuits at the same time.

The removal of DSC has disclosed the actual PDN's performance. It is crucial that DSC is to be removed during the concurrent stress test excitation later in order to showcase the actual performance boundary of the PDNs. The purpose of having zero DSC on the package is to ensure that the noise is not masked off by these DSC and so the actual noise could be measured, and the actual excitation could be de-convoluted.

5.4.1 Impact of Power Gate and Ungate Event on a Power Delivery Network

With reference to the noise and current spectrum of each individual I/O interfaces as listed in Table 5.3, it is discovered that the 27.5 MHz noise source is excited by the PMC stress software. However, the noise spectrum of 27.5 MHz does not appear too strongly on the FFT plot. This means that the repeatability of 27.5 MHz component excited by the current is not as regular as the 125 MHz clock.

It is believed that the power gate and ungate frequency of PMC is running at 27.5 MHz, during which a sharp di/dt is drawn and released from the power partition and interacts with PDN. A closer look on PDN resonance (Figure 5.13) shows that the PDN resonance falls in the range of 30 MHz-35 MHz depending on the Cdie variation during the power gate and ungate event.

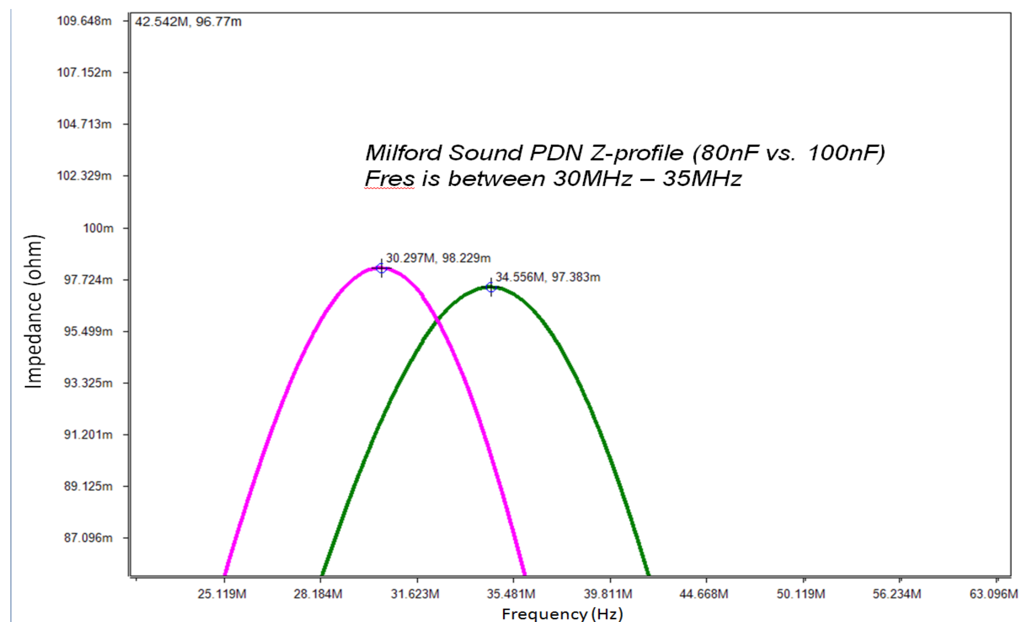


Figure 5.13: PDN resonance on Milford Sound ranges between 30 MHz-35 MHz due to effective Cdie variation during power gate/ungates.

Although the Zpeak or PDN resonance does not directly coincide with 27.5 MHz, the Zpeak varying between 30 MHz-35 MHz is very close to the 27.5 MHz PMC power gate/ungate frequency. Any large di/dt or high frequency current surges around these frequencies will likely to interact with the PDN Zpeak and form a large voltage droop on the PDN.

5.4.2 Impact of Merged Power Delivery Network to Circuit Noise above 100 MHz

The research thus far has highlighted the fact that almost all current excitation's FFT only shows frequency and its spectra components at 100 MHz and above; and >80% of noise composition is measured at >100 MHz (Table 5.2 and 5.3). Figure 5.11 further confirms that the merger power rail package (Milford Sound) is able to achieve a very low impedance of 28 mOhm at >100 MHz, while Jasper and Lucerne are falling far behind at 152 mOhm and 200 mOhm at >100 MHz. This confirms that all circuit induced noise above 100 MHz, and PDN induced noise is below 100 MHz. All noise plots above especially the I/O circuits noise plot has clearly stated the fact that ~80% of the noise magnitude is contributed by circuit clock current; while only 10% and lower noise is contributed by PDN induction.

As a summary, other than SRAM and PMC that could call out PDN resonance noise at ~20 MHz-30 MHz, most of the I/O has similar noise spectrum like those when it is running on an individual isolated power rail, at 125 MHz, 250 MHz, 375 MHz, 500 MHz etc. This agrees with earlier

observation that all HSSLs can be merged as one, while the core power rail may cause some power ungate noise occasionally and need to be addressed carefully if it is decided to merge with HSSL power rails.

5.4.3 Advantages and Disadvantage of Power Rail merger

Assuming that Cdie of a typical I/O power rail ranges from 1 nF to 10 nF, the PDN resonance on a typical FCBGA package is falling between 100 MHz-300 MHz. This is based on the fact that all power rails are standalone and separated on package. The problem with this design is that the package resonance is coinciding with the clock frequency spectrum (by the switching current). Most of the clock frequencies lie in the range of 125 MHz, 250 MHz, 375 MHz etc. would hit the package resonance and cause a large voltage swing on the power rails. Therefore, the PDN design would have to take care of PDN noise induced by the clock current. This noise is usually large and difficult to be decoupled unless much Cdie and DSC are used to suppress the mid to high frequency noise at the same time. The advantage of having the power rails merged on the package is that the Cdie is accumulated to form a larger sum, and this pushes the PDN resonance to below 50MHz; and shifting the entire noise profile away from the PDN resonance; where the clock frequency (switching current) is no longer interacting with the high PDN impedance. What remains now is the sole circuit operating noise that is induced by the switching current of the clock activity. Without the circuit current interacting with the PDN resonance, the noise magnitude is much smaller and manageable without the need of much decoupling capacitance.

The leveraging of shared on-die and on-package capacitance by having the power rail merger on package, allow room for further Cdie reduction.

For example, if 1A of excitation is considered and 50 mV noise is to be achieved at 125 MHz, the Cdie can be reduced from 100 nF to 35 nF (a reduction of 55%) while still be able to achieve the above noise target. (Figure 5.14, orange graph). The savings is a huge benefit for die size shrink on large volume production.

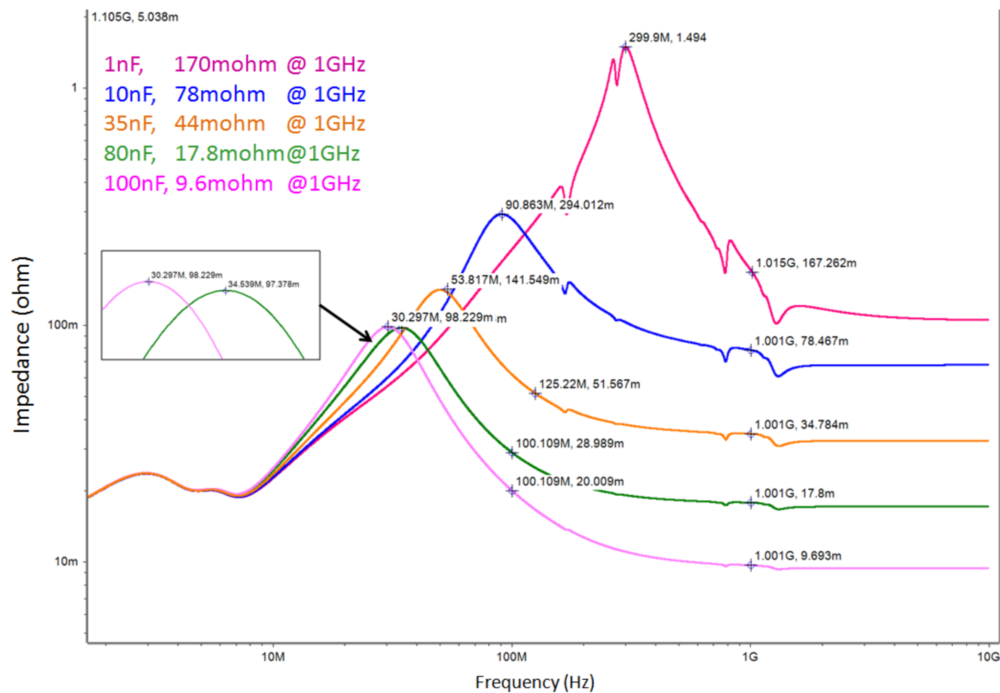


Figure 5.14: Orange graph signifies that 55% Cdie reduction and still be able to achieve 50 mV design target at 125 MHz.

Another noticeable advantage of the merged power rails (Figure 5.14) is the lowering of Rdie from ~167 mOhm to ~10 mOhm at 1 GHz and above. The substantial reduction in Rdie is mainly driven by the leveraging of more Cdie on the silicon. With this added advantage, the high frequency noise

which is governed mainly by clock current harmonics (especially >1GHz) are significantly reduced.

However, one of the disadvantages of this major shift in resonance also pushes the impedance at 35 MHz to go above its original value (Figure 5.15). Notice that the merged package power rail's impedance at 35 MHz is at 100 mOhm, while in normal package, the resonance at 35 MHz is ~60 mOhm. The drawback of this shift is that if the PDN resonance coincides with a major switching event, such as a power gate/ungate event, any large di/dt event at high speed, will still cause a large droop on the power supply rail at 35 MHz. The best approach to prevent this is to design the power ungate circuit such that the di/dt rate is reduced, and the Ipeak (peak current) is sized to a value reasonable to the circuit tolerance. For example, if the impedance is 100 mOhm during resonance frequency, and the allowable voltage tolerance is at 100 mV, then, not more than 1 A of peak current should be allowed to power ungate/ gate at each time.

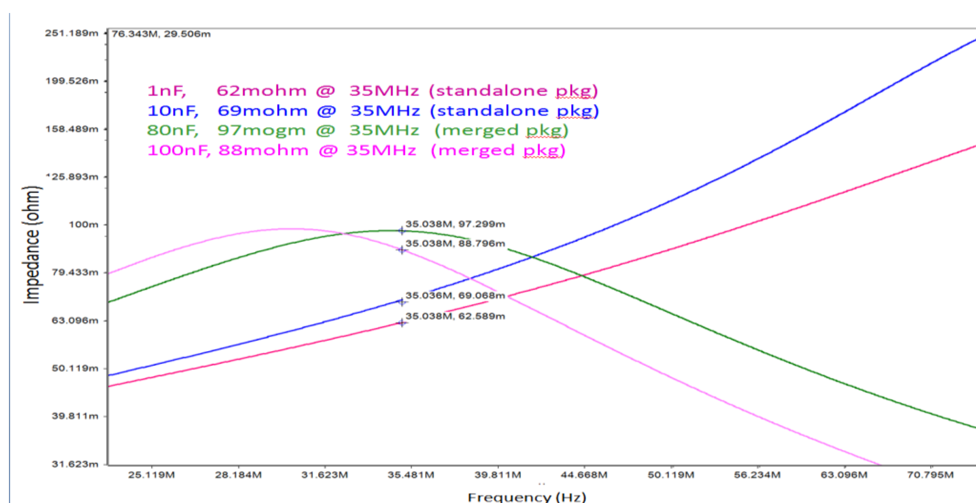


Figure 5.15: The 35MHz impedance is pushed above 69 mOhm to 100 mOhm, which is not desired in power ungate event.

All in a nutshell, the findings on noise profiling and PDN analysis has double confirmed:

- I/O power rail merger is recommended for USB, PCIe and SATA.
- I/O power rails can be merged with Core power rails with careful consideration
- Most I/Os have higher mV susceptibility to noise as long as their clock current does not coincide with the PDN resonance.
- If majority of the noise is I/O circuit induced, the mV peak to peak noise should not threaten the I/O circuit itself.
- And since many of the I/O circuit has common frequency clock current, the I/O are susceptible to I/O circuit noise. Coupling from one to another become less threatening than from Core to I/O.

In summary, Section 5.2 has decomposed the noise profile in time domain into frequency domain using FFT, and highlighted the frequency composition of the noise profile. ~80%-90% of the total noise measured are found associated with switching frequency above 100 MHz; which is I/O and Core activities triggered (or induced by current excitation). Only 10%-20% of the total noise magnitude is associated to PDN induced (<100 MHz). This is double confirmed by the discussion in Section 5.3, whereby FFT is used to decompose the current profile in time domain into its respective spectrum in frequency domain. The data clearly highlighted the fact that most current excitation FFT of HSSLs are above 100 MHz, and the frequency contents which fall between 27.5 MHz-33.7 MHz occurs only when SRAM and PMC are present. Thus, it is concluded that 27.5-33.7 MHz are the product of

SRAM and PMC excitation’s interacted with PDN resonance. The PDN resonance study described in Section 5.4 whereby PDN resonance could fall between 29-30 MHz on Milford Sound merged PDN, and could be further shifted to 35 MHz during power ungate confirms that the SRAM and PMC noise are excited by current profile and at the same time interaction head on with PDN resonance, causing a large droop on the PDN and lead to USB eye specification violation. In order to clearly define the failing criteria for USB eye specification, the proposed method is either by altering the PDN resonance or shifting the resonance away from 27.5 MHz – 33.7 MHz or by lowering the excitation content on PMC to avoid the PDN resonance. The latter method is chosen as it is straightforward than re-designing the PDN and re-build the package to shift the PDN resonance away. The diagnostic analysis is explained in Section 5.5.

5.5 Root Causing USB eye failure using System Margining Approach

Earlier, Section 5.4.3 has shown the advantage and disadvantage of power rail merger and confirms that the I/O power rail can be merged and still lies in a safe boundary from breaking down or violating jitter/eye specifications; on Milford Sound. However, the earlier observations whereby failures on USB interface have not yet been explained fully. Even-though Jasper has less power rails merged and has less noise than Milford Sound, the failure on eye is significantly higher. This indicates that Jasper might have triggered some noise sensitivities at some frequency which are shadowed by the larger Cdie on Milford Sound.

From experimental perspective, system margining is done through modification of the PMC script to reduce the intensity of power gate/ungate activity. Each time, USB eyes are gathered and checked if they could pass on Jasper and Milford Sound. After the moderation of PMC script to 300000 times slower than original version, all I/Os on the system have managed to run successfully passing all eyes for at least 30 min before system hangs. A snapshot of concurrent stress test noise profile with original PMC and the modified PMC (new) are shown in Figure 5.16, overlapping each other. Comparing the two plots, the noise profiles are generally similar in shape and its noise magnitude stays the same at ~100 mVpp.

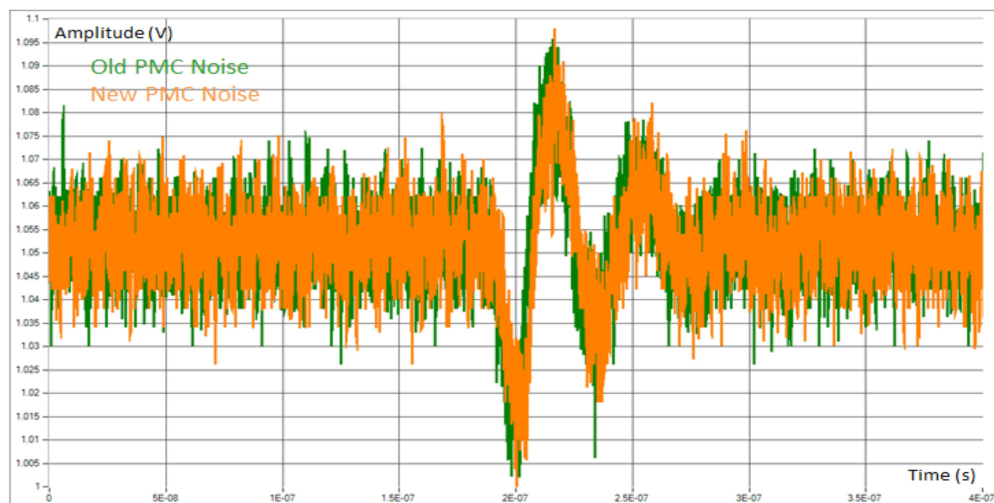


Figure 5.16: Noise droop before and after PMC script moderation where the droop remains similar and overall droop remains ~100 mVpp.

It is difficult to decipher the difference of PMC modification using noise profiles in time domain. The better approach is to translate the noise profiles into current profiles and study the frequency spectrum change due to the modification of script. (Figure 5.17)

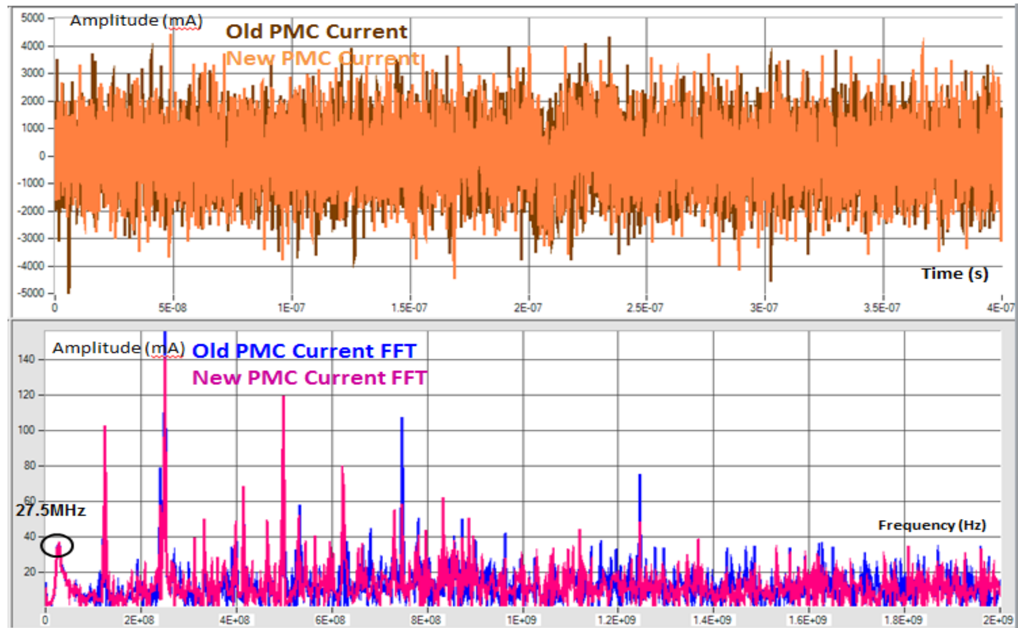


Figure 5.17: The overall snapshot of current FFT before (blue) and after (pink) PMC script modification. Note the 27.5 MHz spectra is still there.

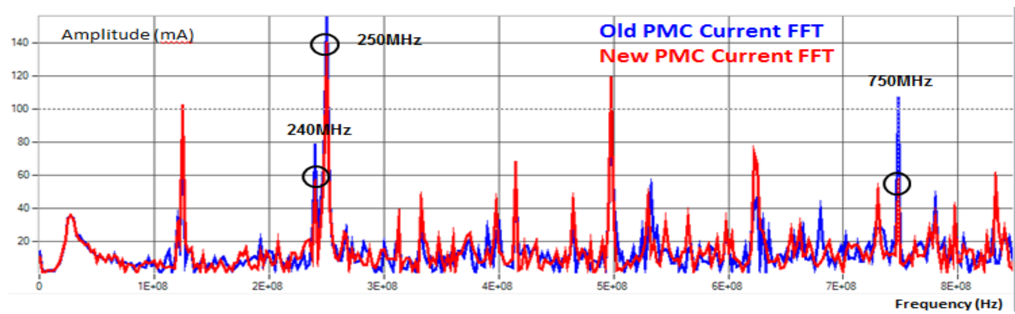


Figure 5.18: New PMC script has significantly decreased the 240 MHz, 250 MHz and 750 MHz clocks.

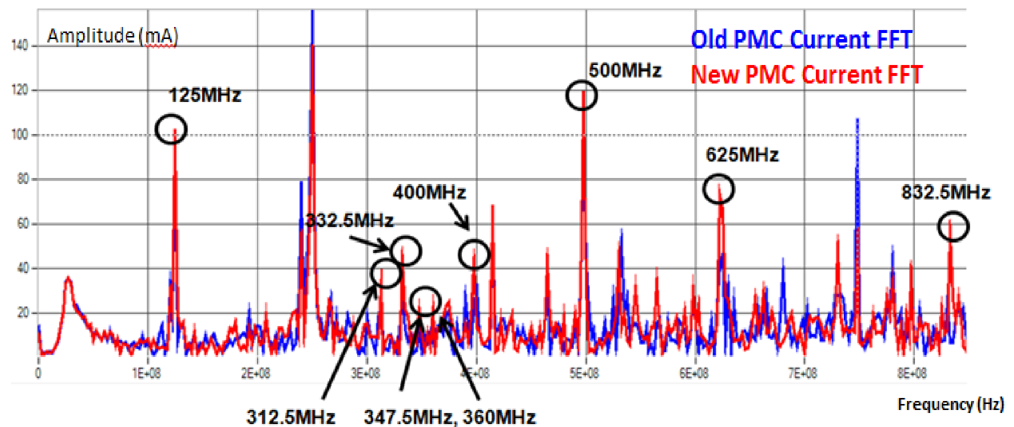


Figure 5.19: A significant increased in various frequency spectrum after PMC modification.

The modification of PMC script is attempted as it is the most aggressive aggressor that is asserted to the system. Although the time domain noise profiles do not vary at visual inspection, the frequency contents have varied by quite a bit as shown in Figure 5.18 and 5.19. The 240 MHz spectrum has reduced significantly (Figure 5.18); which is suspected to be the one of the frequencies that has a direct impact to USB eye performance. The modification of PMC script has altered the frequency content and the various other clock's intensity (Figure 5.19); where by a significant increase in 125 MHz, 312.5 MHz, 332.5 MHz, 347.5 MHz, 360 MHz, 400 MHz, 500 MHz, 625 MHz and 832.5 MHz spectrum are observed after PMC modification. Fortunately, these spectrums do not coincide with the PDN resonance or any of the sensitive operating frequency of the I/O circuits. Although the modification has helped the system run successfully without hanging for >30min, it is essential that all I/O's eye performance is on PAR.

In other words, modifying the content of PMC script has altered the frequency contents of its excitation, bringing USB eye specification back to health, and reversing the failure seen during the concurrent stress tests. This is a surprising discovery as it does not only recover the eye failure on USB to passing, but also maintain the amount of peak-to-peak noise at 100 mVpp. This validated the second objective of the research study to say that when SSN exceeded +/-5% target, it does not necessarily affect the PDN jitter and eye specification in a harmful manner. As long as the frequency content that triggers the USB eye specification failure is not present in the noise content,

the eye specification can still pass as normal. Looking back on the first objective of this research study, "what is believed to be needed" is actually not "what is really needed". This new finding confirms that the design principle could be challenged when the root-cause is clearly identified.

In order to make certain that the eye specification recovery is not a coincidental event, a final round of experiments is conducted across all USB lanes as well as all other HSSLs to ensure that the recovery is real and not a lucky escape.

5.6 Final I/O eye screen with New PMC

A final round of concurrent tests with the new PMC script is applied on all I/Os ports to confirm that the system will remain robust at the worst case voltage margin and temperature settings. Only two results will be focused on, one with I/O concurrent and SRAM test, while the other is with I/O concurrent and PMC test. The flow of the studies will start with USB, follow by PCIe and SATA.

5.6.1 USB Final Screening

The USB eye specification is re-measured using concurrent stress tests that contain five lanes of PCIe, six lanes of SATA and fourteen lanes of USB toggling with SRAM power gate/ungate noise injected (Table 5.5). The USB eye specification is also re-measured using the 2nd concurrent stress tests which contains all the HSSLs tests above but the SRAM power gate/ungate

test is now changed to the new PMC test (Table 5.6). As expected, all tests are either passed (coded in green colour) or marginally passed (coded in yellow colour).

Table 5.5: System Margining on USB ports using I/O concurrent test with SRAM aggressor. All eye passes.

SMV USB data (I/Os Concurrent + SRAM aggressor)

POR Board#SPIX9030003E		Front(4030 mil+17")	Front(4627 mil+17")	Front(3740 mil+17")	Back(12565 mil)	Front(4218 mil+17")	Front(3664 mil+17")	Back(12500 mil)	Front(3868 mil+17")	Front(3408 mil+17")	Back(14804 mil)	Front(4136 mil+17")	Back(13022 mil)	Back(13363 mil)	Back(14920 mil)
		P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13
1.103v-3.456V	POR#11	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed
100C	Milford Sound#6	Passed	Passed	Passed	M. Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed
1.103v-3.456V	POR#11	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed
0C	MilfordSound#6	Passed	Passed	Passed	Passed	Passed	Passed	M. Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed
0.998V-3.135V	POR#11	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed
100C	MilfordSound#6	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed
0.998V-3.135V	POR#11	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed
0C	MilfordSound#6	Passed	Passed	Passed	Passed	Passed	Passed	M. Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed

Table 5.6: System Margining on USB ports using I/O concurrent test with new PMC aggressor. All eye passes

SMV USB data (I/Os Concurrent + PMC aggressor)

POR Board#SPIX9030003E		Front(4030	Front(4627	Front(3740	Back(12565	Front(4218	Front(3664	Back(12500	Front(3868	Front(3408	Back(14804	Front(4136	Back(13022	Back(13363	Back(14920
		P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13
1.103v-3.456V	POR#11	Passed	Passed	Passed	M. Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed
100C	MilfordSound#6	Passed	Passed	Passed	M. Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed
1.103v-3.456V	POR#11	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed
0C	MilfordSound#6	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed
0.998V-3.135V	POR#11	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed
100C	MilfordSound#6	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed
0.998V-3.135V	POR#11	Passed	Passed	Passed	M. Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed
0C	MilfordSound#6	Passed	Passed	Passed	M. Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed	Passed

In other words, the 240 MHz clock is observed to be the most likely coinciding clock that overlaps with the USB clock and is very likely the root cause of eye failure on USB ports. And the sensitivity of the USB port in this case can be addressed by either lowering the aggressor clock at 240 MHz or lowering the impedance profile at 240 MHz.

5.6.2 PCIe Final Screening

A re-examination on PCIe is performed and all results are also passing the eye as expected. Two sets of results are collected, i.e Concurrent stress tests combining HSSLs and SRAM (Table 5.7) and Concurrent stress tests combining HSSLs and PMC (Table 5.8).

Table 5.7: PCIe data recovery clock margin for Milford Sound stressing with concurrent test and SRAM as aggressor.

DRC Margin (Data Recovery Clock)		Units: Milford Sound (SRAM)			
		Baseline		Concurrent	
VIO	Temp	Port1	Port5	Port1	Port5
0	0.997	32	33	31	31
0	1.1	35	35	32	35
60	1.05	35	35	33	37
98	0.997	37	35	34	35
98	1.1	35	35	35	35

Table 5.8: PCIe data recovery clock margin for Milford Sound stressing with concurrent test and PMC as aggressor.

DRC Margin (Data Recovery Clock)		Units: Milford Sound (PMC)			
		Baseline		Concurrent	
VIO	Temp	Port1	Port5	Port1	Port5
0	0.997	38	38	36	38
0	1.1	38	38	36	38
60	1.05	38	40	36	38
98	0.997	40	40	40	40
98	1.1	38	40	36	40

Table 5.7 and 5.8 are Design Rule Check (DRC) margin for PCIe running concurrent test using the concurrent test stimulus. There is no significant difference between baseline test and concurrent test when comparing the baseline test and the concurrent test for both cases of SRAM and PMC (new modified script) as aggressors. As the data captured for SRAM

and PMC were done on two different boards and silicon, it was not apple-to-apple comparison and the margin difference could not be compared side by side between SRAM and PMC. Nevertheless, there is not much difference between baseline and concurrent test for each respective aggressor.

Having done the DRC margin check, eye data is collected on all 5 lanes of PCIe. The result (Figure 5.20) confirms that PCIe eye passed for all the tests with Concurrent stress tests with SRAM and PMC, at worst case skew corner. PCIe Tx eye measurements on desktop board are taken from lane 1 to lane 5 with concurrent test running with SRAM and PMC aggressors. All eye passed with 0.82-0.84 UI where the Tx eye spec is min 0.75 UI.

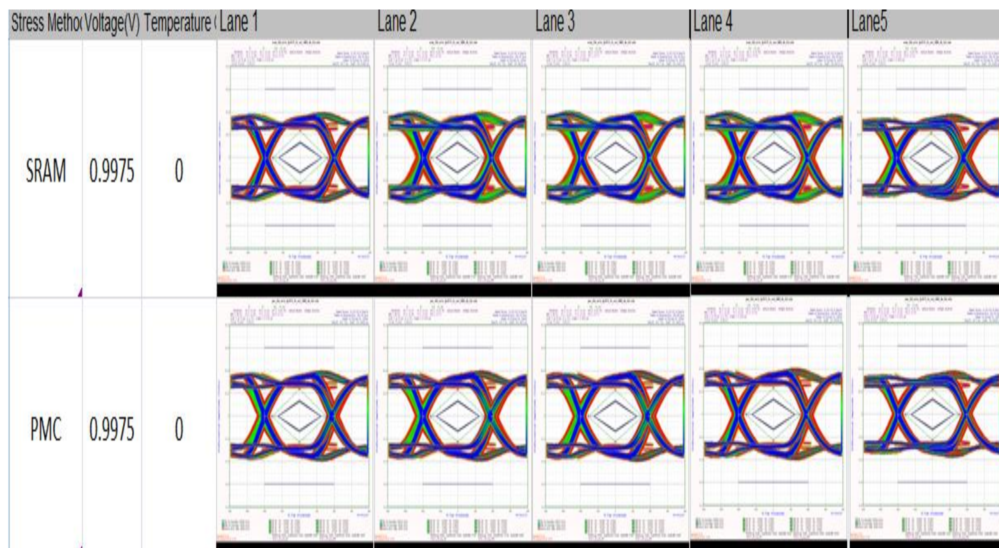


Figure 5.20: PCIe eye passes for all the Concurrent stress tests with SRAMs and PMC.

5.6.3 SATA Final Screening

Similar validation tests and system margining data are collected on SATA and results are shown below (Table 5.9 and Figure 5.21). System

margining results on SATA also passed all the various temperature and voltage settings with margin, when concurrent tests and aggressors SRAM and PMC are introduced.

SATA Tx eye (port 0 – port 5) on Milford Sound are stressed with concurrent test. At norm voltage (1.05 V) and room temp, all Tx eyes pass but some have lower margin with 1m SATA cable running lone-bit pattern.

Table 5.9: System margining validation results on SATA.

SRAM RX DRC SATA Test (Milford Sound#11 & 12)			
Temp	1.102V	1.05V	0.998V
110	(2,2)	(2,3)	(2,3)
60 (P5)	(2,2)	(2,2)	(2,2)
0	(2,2)	(2,2)	(2,2)
110	(2,3)	(2,3)	(2,3)
60 (P3)	(2,3)	(2,3)	(2,3)
0	(2,2)	(2,3)	(2,3)
110	(2,2)	(2,2)	(2,2)
60 (P3)	(2,2)	(2,3)	(2,3)
0	(2,2)	(2,2)	(2,2)

PMC RX DRC SATA Test (Milford Sound#4)			
Temp	1.102V	1.05V	0.998V
110	(2,2)	(2,2)	(2,2)
60 (P5)	(2,2)	(2,3)	(2,2)
0	(2,3)	(2,2)	(2,2)
110	(2,2)	(2,3)	(2,2)
60 (P3)	(2,2)	(2,2)	(2,3)
0	(2,2)	(2,2)	(2,2)
110	(2,2)	(2,2)	(2,2)
60 (P3)	(2,2)	(2,2)	(2,2)
0	(2,2)	(2,3)	(2,2)

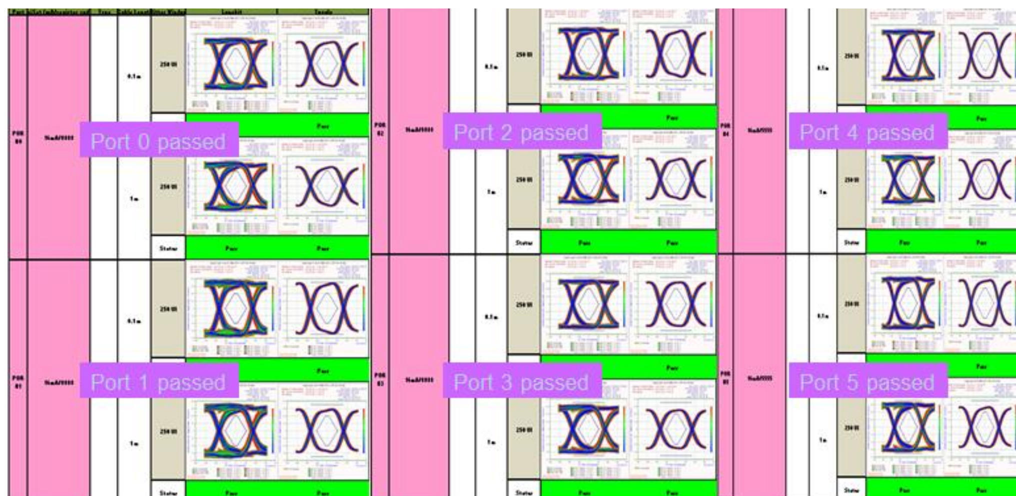


Figure 5.21: SATA Tx eye (port 0 – port 5) passes on Milford Sound when they are stressed with concurrent test

5.7 Summary

The findings supported the second objectives of the study whereby jitter and eye specification is not bounded by +/-5% noise target across the full range of frequency spectrum, but rather the specific frequency that coincides with the operating frequency of the HSSL. The full health screen is conducted across all the 14x USB ports and the findings come to an agreement that the recovery is real and no further failure is observed.

CHAPTER 6

CONCLUSIONS

6.1 Conclusions

This chapter concludes the research objectives and findings on the research goal set in Chapter 1:

1) Analyse the difference between "what is believed to be needed" versus "what is really needed" on existing design principles

   Many high speed design principles which govern the package and motherboard interconnect design rules as well as the many "believes what is needed" have been brought into this research analysis.

   Examples of commonly used High Speed Design Principles (HSDP) and "what is believed to be needed" are:

   a) Power rails isolation between digital and analogue (Venkataramani, 2009) and (Ali, 2011)
   b) The need to isolate power rail from one to another interfaces
   c) The need to keep the power supply rail noise to within +/-5% of the nominal operating voltage (Vcc) (Mohamood, et al., 2007)
   d) A must to isolate core logic from I/O power supplies (Venkataramani, 2009) and (Ali, 2011)

Three packages are customized and fabricated for this research, one package (Lucerne) abides all the high speed design principles (HSDP) and "what is believed to be needed" to serve as a baseline for benchmarking; while

the second package (Jasper) is designed to violate two of the above HSDP namely, a) and b) while the third package (Milford Sound) is designed to violate three of the above HDSP, namely a), b) and d). Jasper violated the 2 HSDPs by merging PDN of digital and analogue as one and I/O and I/O power rail as one. While Milford Sound aggressively merged all digital and analogue supply of common voltage into one single PDN, inclusive of all I/O and Core supplies. Results in Chapter 4.3 highlighted that most HSSLs like PCIe and SATA sailed through the concurrent stress tests with flying colours, whereby none of the eye specifications are violated on all 3 packages; even-though Jasper and Milford Sound have violated 3 HSDPs above. The results have proven that many HSDP are "what is believed to be needed" but not necessarily "what is really needed".

Other studies which supported the fact that "what is believed to be needed" but not necessarily "what is really needed" are summarized in Chapter 5.4 and discussed below. The study supports both objective 1 and objective 2 of this research study.

The second research objective described below says that:

2) Understand what effect the PDN have on jitter and eye diagram when the SSN noise exceeds +/-5% target

As observed in Chapter 4.3, "From its standalone power plane (Lucerne) to a semi-merged power plane (Jasper) and the fully merged power plane (Milford Sound), PCIe and SATA look pretty healthy even as the

magnitude of noise has increased from ~50 mV to ~100 mV; with and without die-side-capacitor (DSC). The passing of compliance eye tests have indicated that either both PCIe and SATA have ample of margin before the eye specification are violated or the PDN design do not coincide with the sensitive operating frequencies of the HSSLs."

On the other hand, although there are eye specification violations seen on the USB lanes, the detail diagnosis which later brought up the findings as follow in Chapter 5.4 quoted this 'modifying the content of PMC script has altered the frequency contents of its excitation, bringing USB eye specification back to health, and reversing the failure seen during the concurrent stress tests. This is a surprising discovery as it does not only recover the failing eye on USB to passing but also maintain the amount of peak-to-peak noise at 100 mVpp. This validated the second objective of the research study to say that when SSN exceeded +/-5% target, it does not necessarily affect the PDN jitter and eye specification in a harmful manner. As long as the frequency content that triggers the USB eye specification failure is not present in the noise content, the eye specification can still pass as normal.'

With all three HSSLs confirming that with SSN exceeding +/-5% target, their eye specifications are not violated means there are margins to relax these design targets and allow further "optimization" of PDN design with merged power rails and shared decoupling capacitance.

On the other hand, many HSDPs that govern the design principles of high speed packages and board interconnect design, could be overly subscribed when design parameters have been assumed incorrectly and thus lead to over-design of PDN. For example, the HSDP is developed as a rule of thumb 20 years ago (Dr. H. Johnson, 1993), and many designs are based on these principles to meet quality design. Today, sophisticated CAD tools and 3D Electromagnetic modelling and simulation tool are available throughout the market for engineering design use. These tools make possible to omit HSDPs that are put forth 20 years ago; and push the design envelope one notch higher than "what is believed to be needed". For practical design principles, it is concluded that the design margin is available and noise target is just a guideline and not mandatory. In the event that the peak-to-peak SSO has to be violated, so long as eye specification and jitter remains passing, the violation should be foregone.

6.2 FUTURE WORK

The findings in this research project has highlighted one discovery which is 'As long as the frequency content that triggers the USB eye specification failure is not present in the noise content, the eye specification can still pass as normal'. As this measurement has proven that changing the SSN frequency content could reverse and recover a failed USB eye to passing; the suspicious of 240 MHz as being the sensitive frequency has yet to be fully understood.

The future work which is worth further investigation is to uncover what frequency of SSN that truly triggers the failure of USB eye specification. Besides USB, PCIe and SATA eye should have an equivalent weak spot; i.e each of them should have a frequency of SSN that would trigger their failure on its eye specification. If these HSSLs 'sensitive SSN frequencies' could be discovered, it would help to reduce the PDN design spectrum to that limited frequency range; and thus officially narrowing the PDN design from a broadband (1 Hz – few GHz) to a narrower spectrum. The prospect is the elimination of much decoupling capacitance which does not act on the right spectrum and stand a chance to be reduced or removed.

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Appendix A

DETAIL PNA SYSTEM SETUP FOR CDIE MEASUREMENT

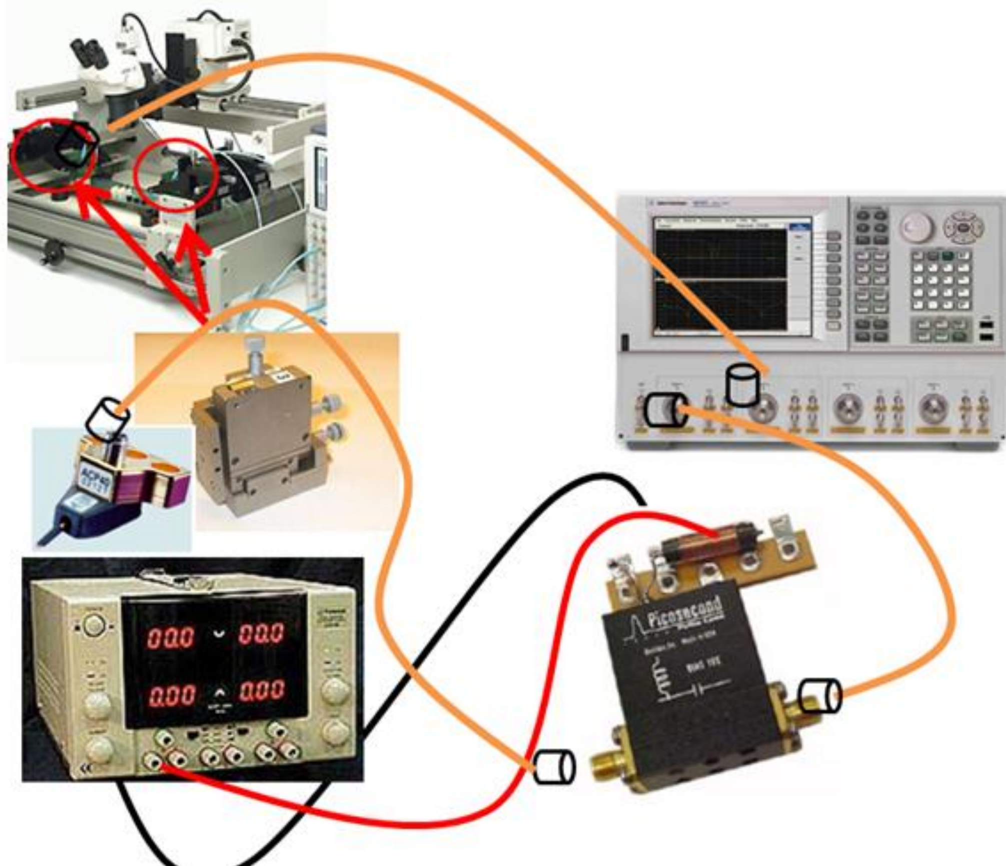

Figure A.1: Detail PNA system setup for Cdie measurement

Step by step measurement instructions on PNA:

- Start freq=30khz, stop freq = 100MHz
- Averaging factor is turned on
- Averaging factor =32 is set
- VNA is calibrated for port 1 and port 2
  - S11 and S22 1 port
    - Open
    - Short
    - Load
  - *Caution: Wait for averaging to arrive at 32, before connect the next calibration unit*
- If 50 Ohm load is measured, ensure that measurement display forms a dot at the centre of the smith chart. (Figure A.2)
- If an open load is measured, ensure that the measurement display forms a dot at the right hand side of the smith chart. (Figure A.2)

- If a short load is measured, ensure that the measurement display forms a dot at the left hand side of the smith chart. (Figure A.2)
- Repeat the above for Port 2
- Once port 1 and port 2 are calibrated, performed a S21 and S12 calibration
  - S12 and S21 2 ports
    - Thru
- Connect port1 and port 2 to ***thru*** calibration substrate, ensure that the measurement display forms a dot at the centre of the smith chart.
- When all the above calibrations have met expectation, land the 2 microprobes on the DUT Vcc and Vss balls.
- Slowly turn on the power supply from 0V to Vcc (watch-out for leakage current)
  - *Caution: leakage current beyond 100mA usually does not yield a stable and trustable result. Use Guideline 2 below for highly leaky interfaces.*
  - *Caution: Leakage current should not go beyond 1A, if yes quickly turn down the power supply or power down the power supply to avoid burning the input port of VNA.*
- Press [Meas] and turn on Z conversion
- Press [Scale Ref], **Auto scale** if the visual is not focus on the right frequency and dB/div
- Examine the Z plot to see where the resonance is
- Adjust the Start and Stop frequency if needed, and re-do the calibration before taking the Cdie measurement again.
- If the start and stop frequency are capturing the Cdie resonance:
- Press [Marker] and move the cursor till it arrive at the linear capacitance curve.
  - *Caution: Any distorted curve will not be acceptable.*
- Press [Meas] and turn off Z conversion
- Press [Format] and set to smith chart. Note the **capacitance** value as your first reference, **resonance frequency**, and **leakage current**.
- Then, save the file by following these steps:
- Press [Format] and set to **Log Mag**, **More**, **Lin**, [Save/Recall], **Save File Formats**, **Text**, **Save File**
-

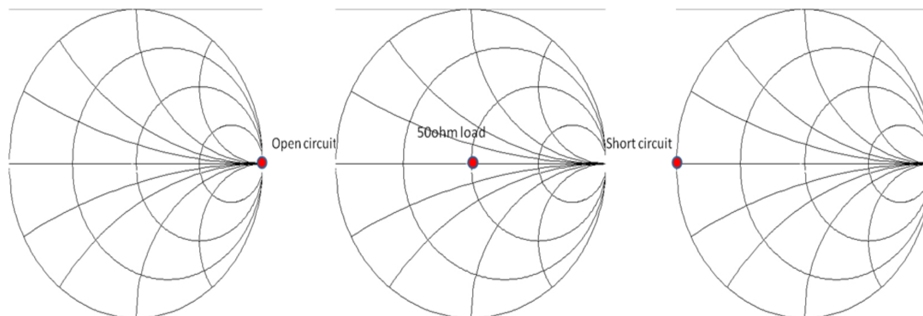

Figure A.2: Smith Chart view: (Left) Open circuit (Middle) 50 Ohm load (Right) short circuit.

Appendix B

CONCURRENT STRESS SETUP

1. USB High Speed Stress Methodology

Software: WinMEM

Hardware: USB thumb drives (# of drives depends on the # of USB port of the platform, USB front panel cable

1. Change Wimem Memory space to 0xAA and 0xBB respectively
2. Change *device and function* column to cccccccc
3. If Sync pattern is not needed, change it back to 00

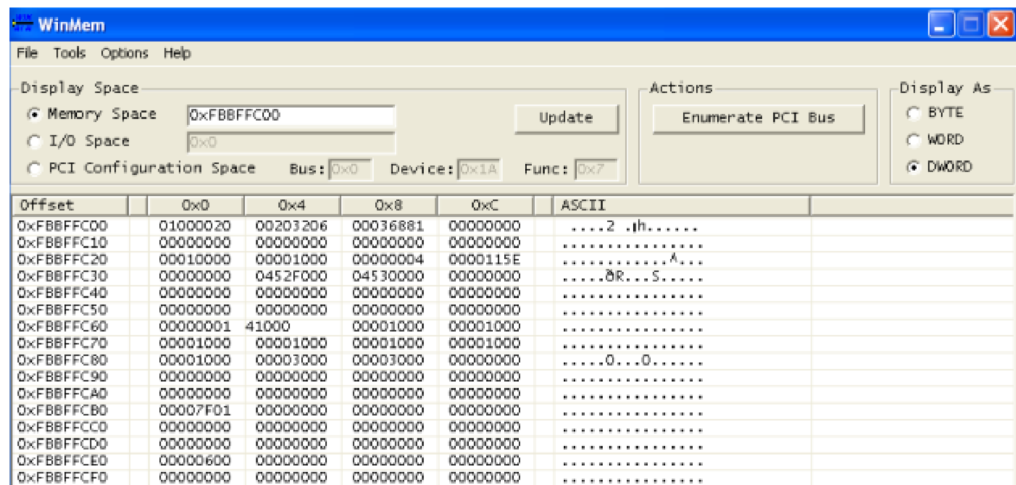

Figure B.1: WinMEM software that changes USB memory space. (Courtesy of Intel)

2. SATA Stress Methodology

Software: WinMEM

Hardware: Cruz card, SATA cable (SATA signal) & SMA cable

4. Change Wimem Memory space to 0xAA and 0xBB respectively
5. Change *device and function* column to cccccccc
6. If Sync pattern is not needed, change it back to 00

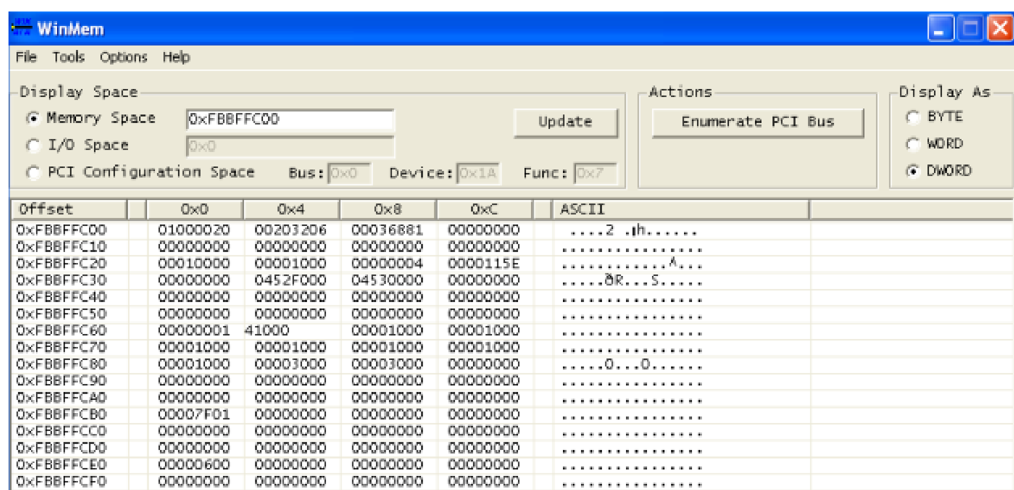

Figure B.2: WinMEM software that changes SATA memory space. (Courtesy of Intel)

3. PCIE Stress Methodology

Software: WinMEM

Hardware: Compliance Load Board (CLB) card & SMA cable for signal capturing

1. Change Wimem Memory space to 0xaaaaaaaa
2. Change *0x4* column to aaaaaaaa
3. If CMM4 is not needed, change it back to 00

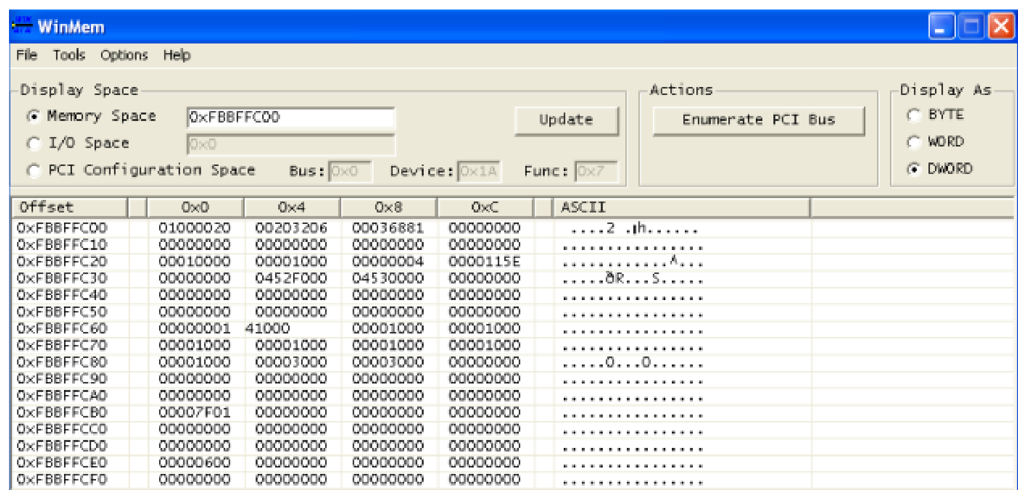

Figure B.3: WinMEM software that changes PCIe memory space. (Courtesy of Intel)

4. Core Stress Methodology (SRAM)

Software: Have stardebug 2.0.1.4 and JTAG driver installed, ‘sram_pwr1.lua’

Hardware: UTAG2+cable

1. Follow the ‘JTAG enabling’ methodology in ‘Flash’ section
2. SW VARC
3. dofile ‘sram_pwr1.lua’
4. SRAM_TEST(0x3FF)
5. CTRL-C to stop the operation
6. Unplug JTAG cable if reboot

5. Core Stress Methodology (AUX)

Software: Have stardebug and JTAG driver installed

Hardware: UTAG2+cable

To view VCCAUX power gating and ungating events

Launch stardebug

1) Switch to PMC: type sw pmc,
2) Halt the system: type h
3) Turn off watchdog (to prevent system from shutting down): type x 0xAA 0x0
4) Power gate: type x 0xAA 0xAA
5) Power ungate: type x 0xAA 0x0

Appendix C

PCIe Eye Diagram Measurement's Scope Setting

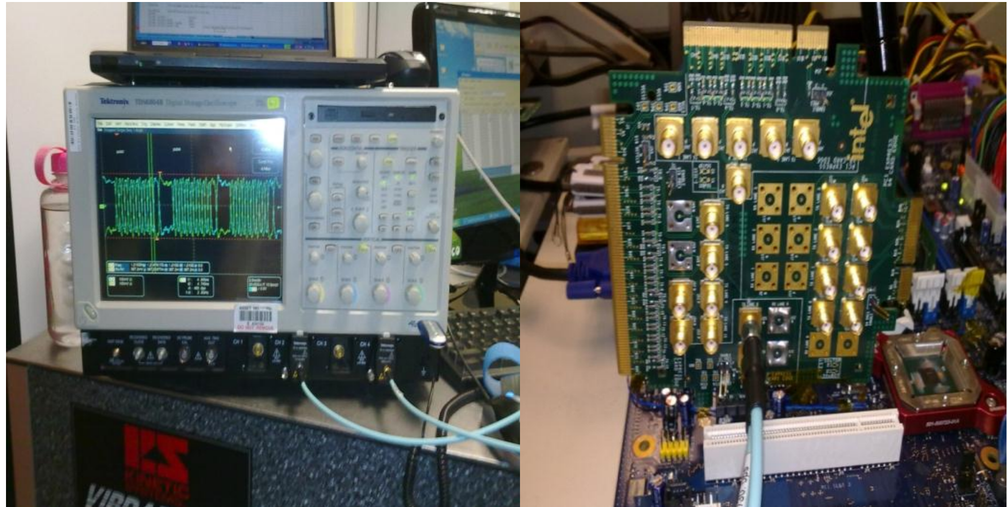

Figure C.1: Hardware setup for PCIe eye diagram measurement
(Left) An osilloscope with 8GHz a.k.a. 20GS/s bandwidth and 8MB memory depth (Right) SMA cables (1m in length) and a CLB card.

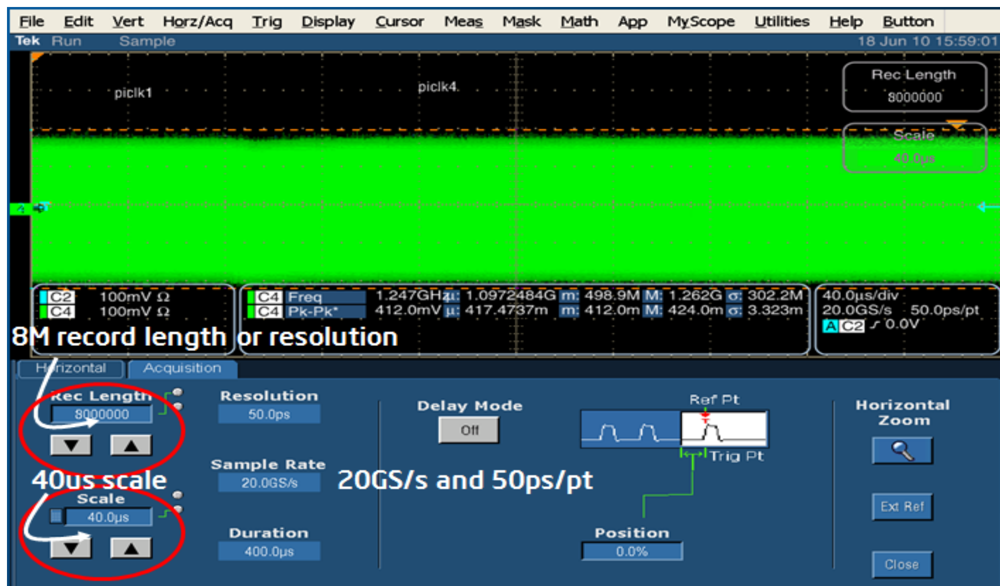

Figure C.2: PCIe eye diagram oscilloscope's setting. Channel 1/3 or channel 2/4 are used for Tx+ and Tx- eye diagram measurement to ensure full bandwidth is capitalized

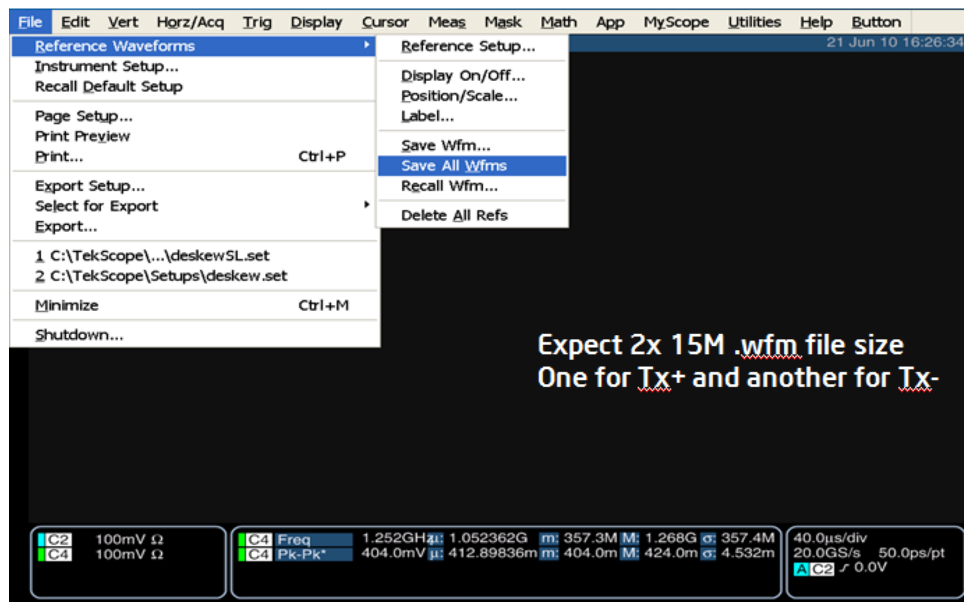

Figure C.3: Savings of the data for eye diagram post processing

SATA Eye Diagram Measurement's Scope Setting

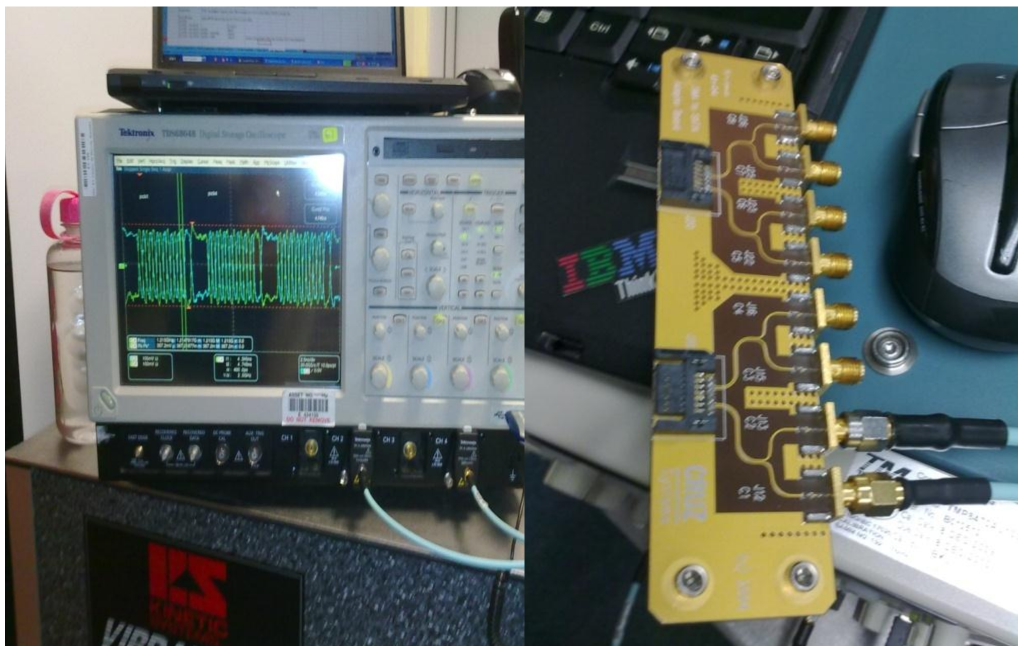
Figure C.4: Hardware setup for SATA eye Diagram measurement:
(Left) An oscilloscope with 8GHz a.k.a. 20GS/s and 8MB memory depth (Right) SMA cables (1m in length) and Cruz card.

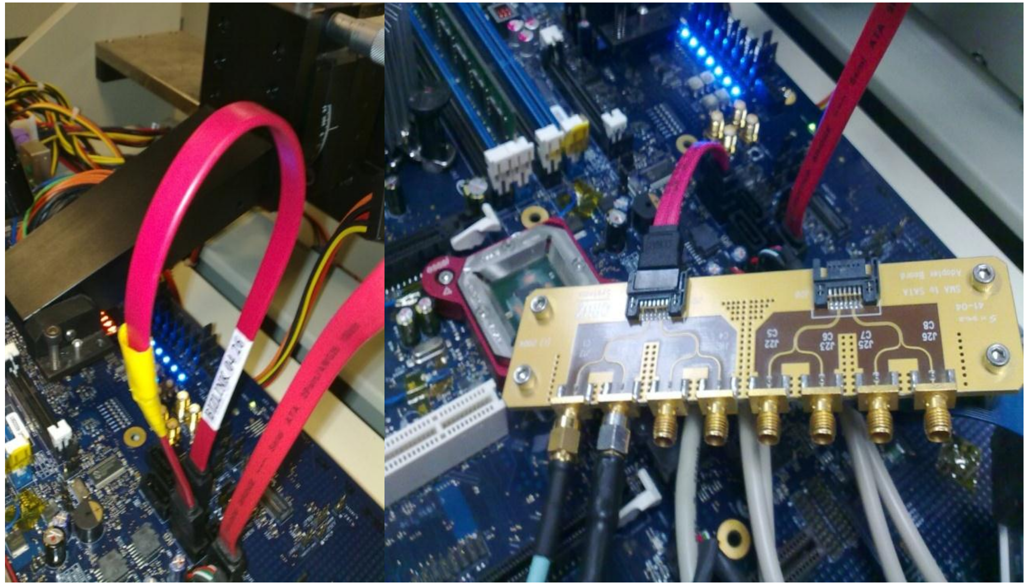

Figure C.5: Hardware setup for SATA eye diagram measurement
(Left) A twisted or loopback cable (Right) SATA cable (0.1m in length), Cruz card and SMA cables.

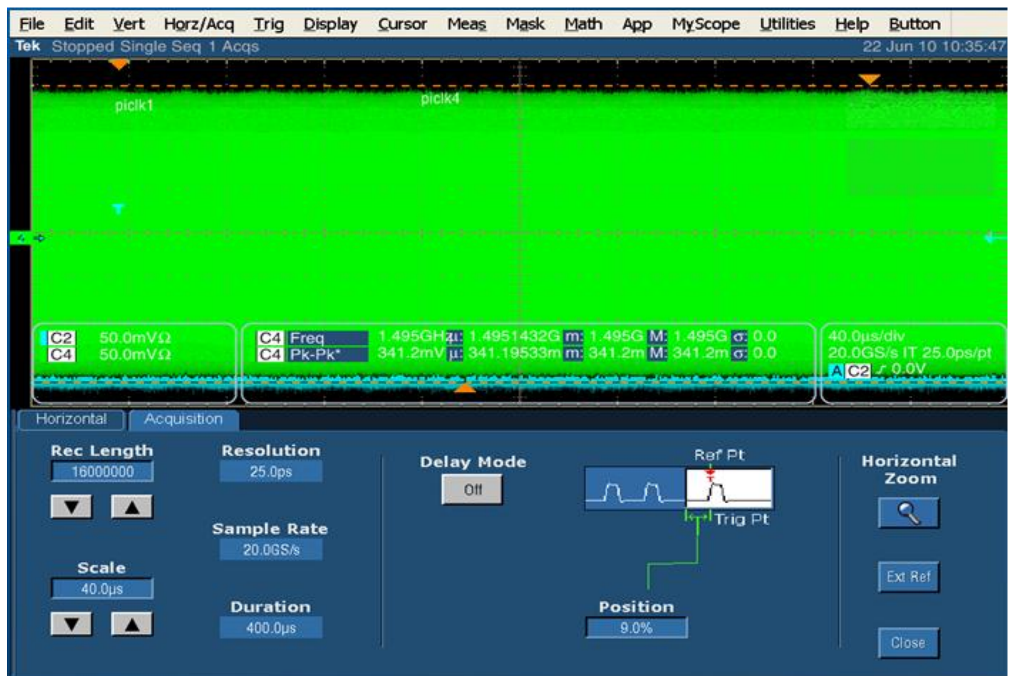

Figure C.6: SATA eye diagram oscilloscope's setting. Channel 1/3 or channel 2/ 4 are used for Tx+ and Tx- eye diagram measurement. Record length is set to 16M, at 40us scale, while sample rate is set at 20GS/s.

USB Eye Diagram Measurement's Scope Setting

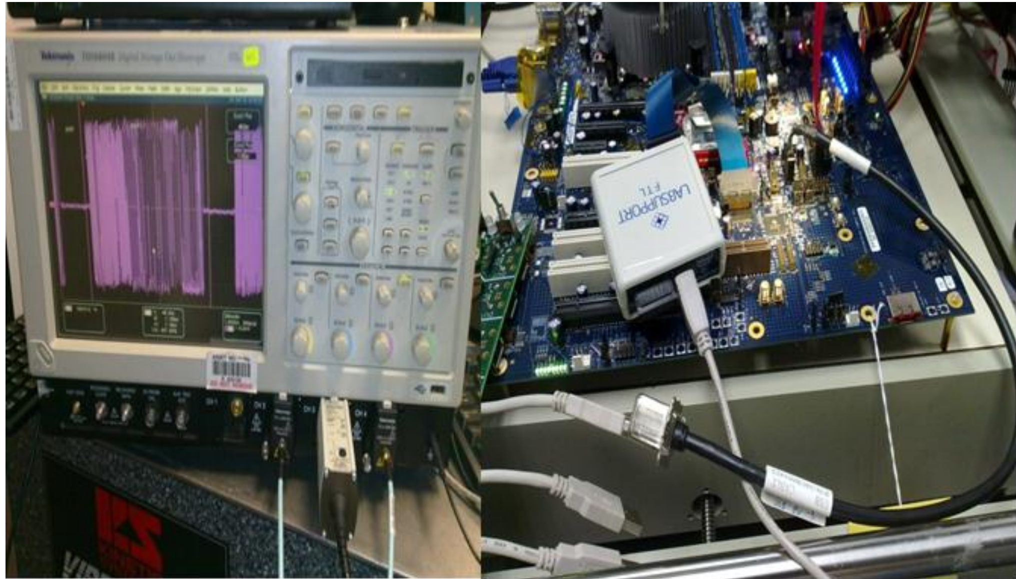

Figure C.7: USB eye diagram oscilloscope's setting
(Left) The setup of an oscilloscope and 7313 probe
(Right) A 19" cable is connected to the front panel connector

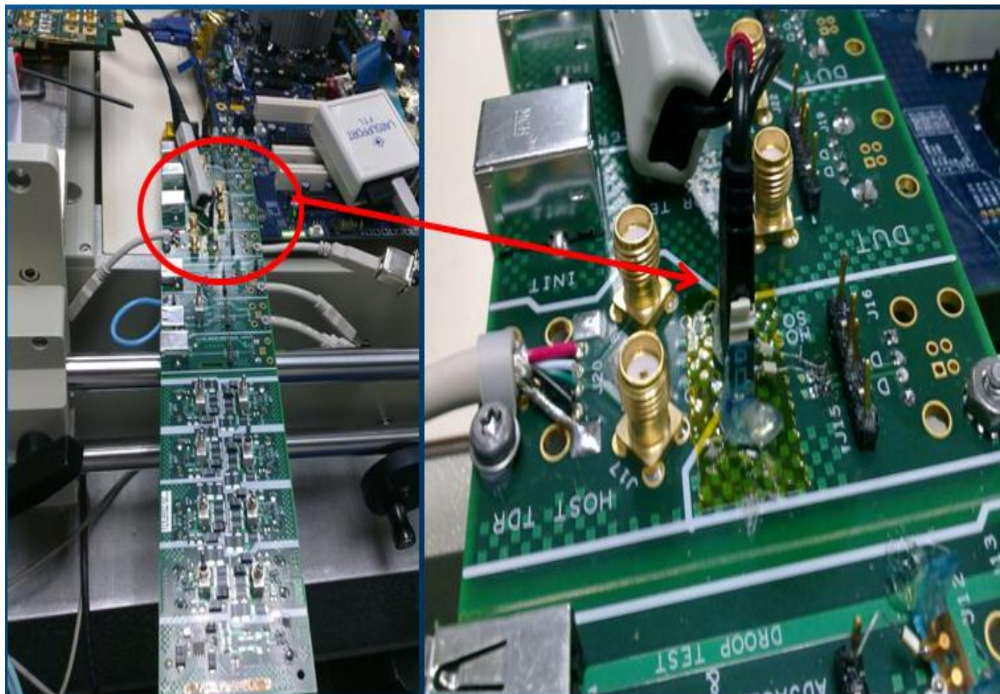

Figure C.8: (Left) The 19" cable is connected via a usb cable (0.1m in length) to the Tektronix USB Card and P7313 probe.
(Right) A zoomed in view on P7313 attaching to the Tektronix USB card.

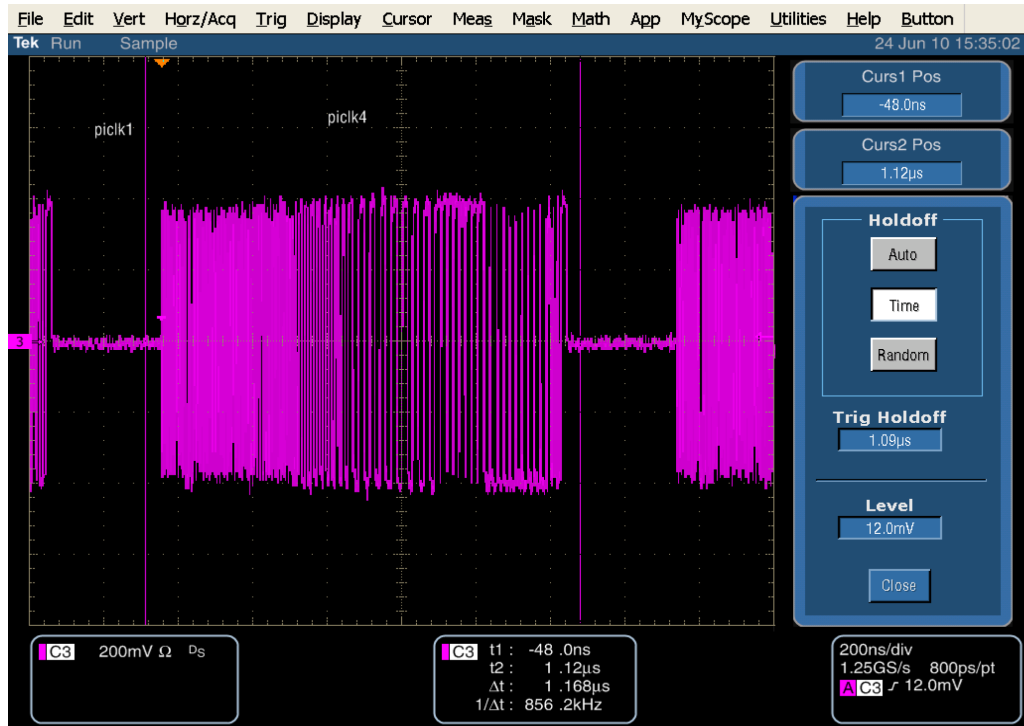

Figure C.9: USB eye diagram oscilloscope's setting The probe's gain is calibrated for the channel. Trigger is set to holdoff and holdoff time =1.09us (each packet is 1.088us)

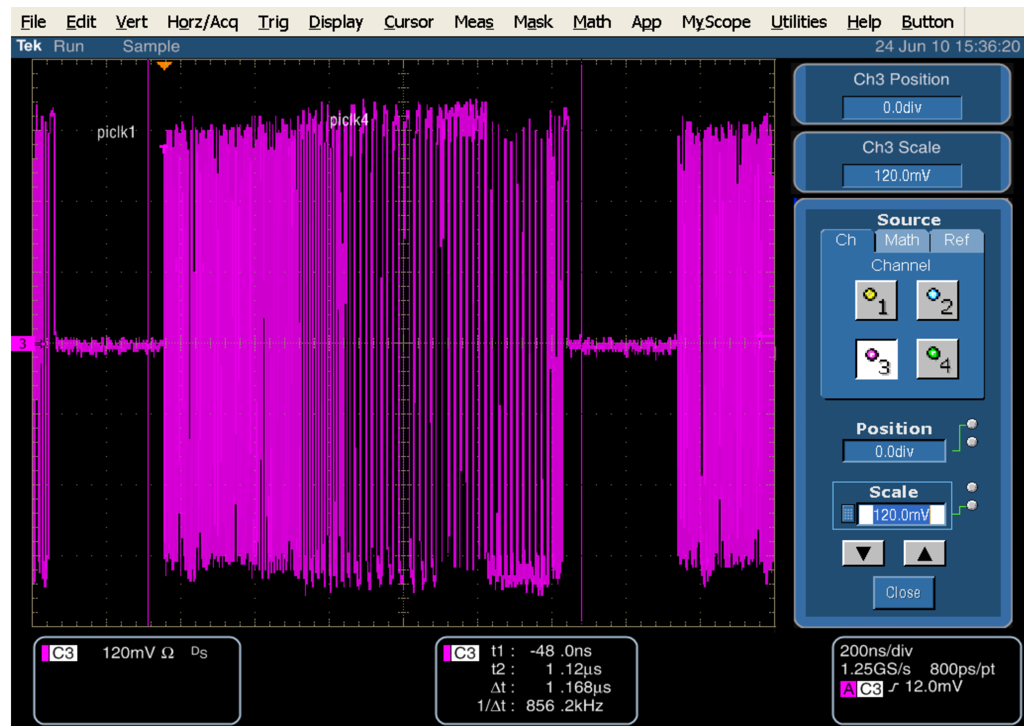

Figure C.10: Vertical scale is set to 120mV (to enlarge the amplitude of the pattern on the scope)

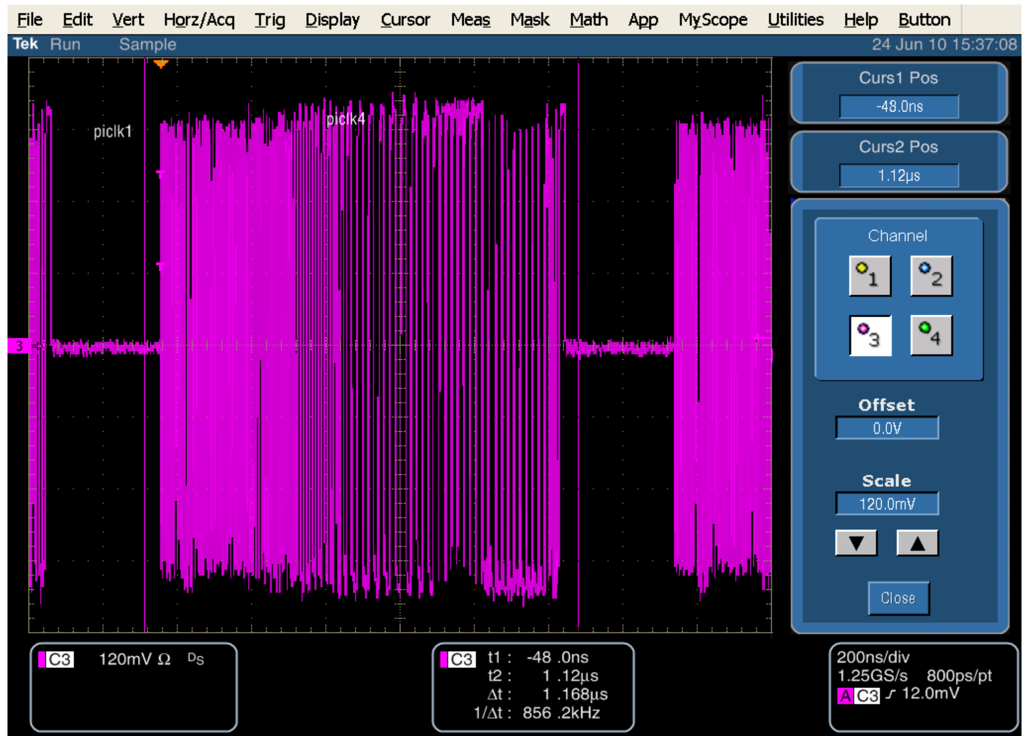

Figure C.11: Ensure offset is set to 0V

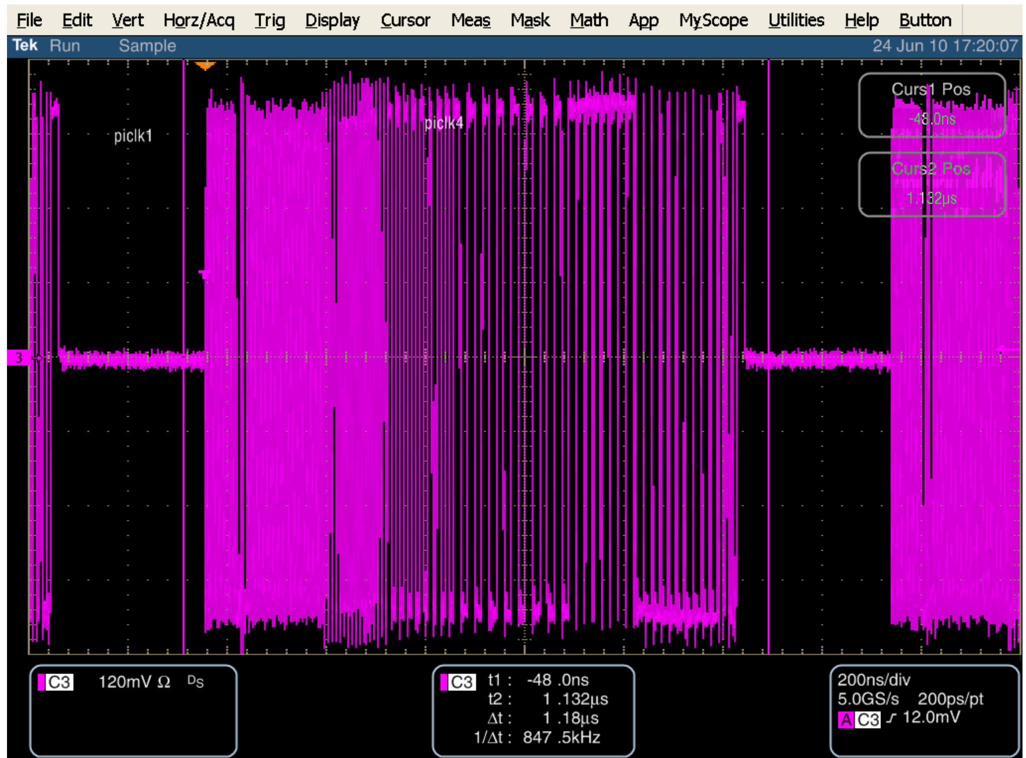

Figure C.12: The 2 cursors are positioned in between the frame of test packet and the sampling rate is set at 5GS/s and 200ps/pt.

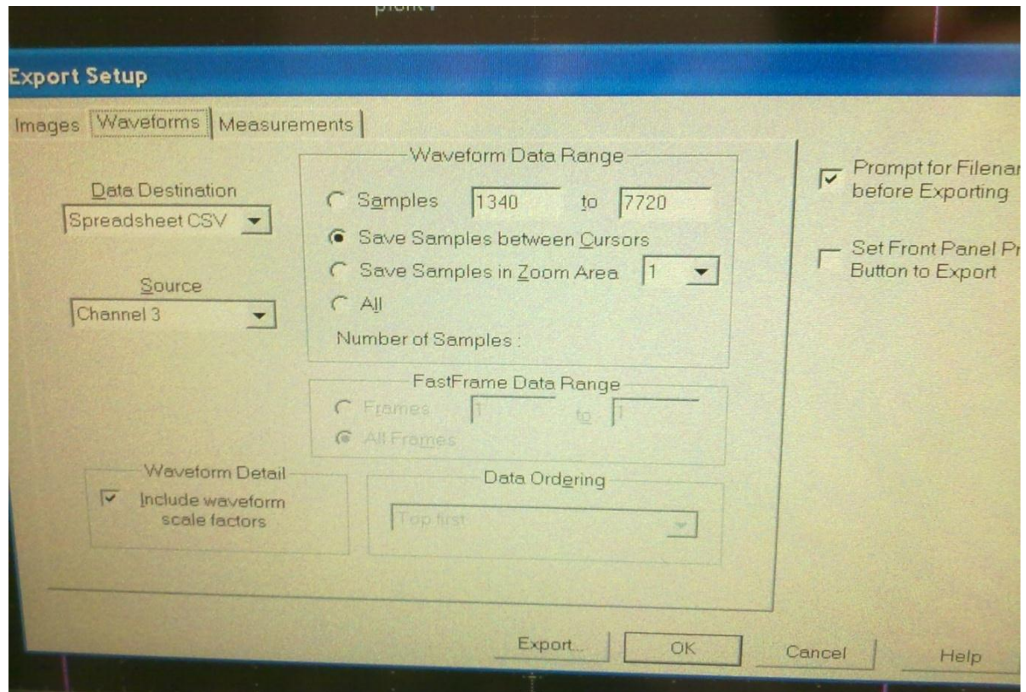

Figure C.13: Export setup: Samples between cursors are saved and results to be exported in spread sheet CSV format.

Appendix D

Publications

[1] Tan F. N., Lee S. C., Abdul Rahman F. (2011), Finding the worst case supply noise excitation methodology for High Speed I/O Interfaces *Asia Symposium & Exhibits on Quality Electronics Design (ASQED)*. Malaysia 161-166

[2] Tan F. N., Lee S. C., Abdul Rahman F. (2011), Package Design Optimization for Efficient on-silicon Capacitance Leveraging *Asia Symposium & Exhibits on Quality Electronics Design (ASQED)*, Malaysia 8-12

[3] Tan F. N. (2012), Does Power Rail Merger work for High Speed I/O Interfaces like PCIe, SATA and USB, *International Conference of Electronic Packaging* Japan